14-Bit, 40 MSPS/65 MSPS Analog-to-Digital Converter

AD6644

FEATURES

65 MSPS guaranteed sample rate
40 MSPS version available
Sampling jitter < 300 fs
100 dB multitone SFDR
1.3 W power dissipation
Differential analog inputs
Pin compatible to AD6645
Twos complement digital output format
3.3 V CMOS compatible
Data-ready for output latching

APPLICATIONS

Multichannel, multimode receivers
AMPS, IS-136, CDMA, GSM, WCDMA
Single channel digital receivers
Antenna array processing
Communications instrumentation
Radar, infrared imaging
Instrumentation

GENERAL DESCRIPTION

The AD6644 is a high speed, high performance, monolithic 14-bit analog-to-digital converter (ADC). All necessary functions, including track-and-hold (TH) and reference, are included on-chip to provide a complete conversion solution. The AD6644 provides CMOS-compatible digital outputs. It is the third generation in a wideband ADC family, preceded by the AD9042 (12-bit 41 MSPS) and the AD6640 (12-bit 65 MSPS, IF sampling).

Designed for multichannel, multimode receivers, the AD6644 is part of the Analog Devices, Inc. new SoftCell® transceiver chipset. The AD6644 achieves 100 dB multitone, spurious-free dynamic range (SFDR) through the Nyquist band. This breakthrough performance eases the burden placed on multimode digital receivers (software radios) which are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74 dB.

The AD6644 is also useful in single channel digital receivers designed for use in wide-channel bandwidth systems (CDMA, WCDMA). With oversampling, harmonics can be placed outside the analysis bandwidth. Oversampling also facilitates the use of decimation receivers (such as the AD6620), allowing the noise floor in the analysis bandwidth to be reduced. By replacing traditional analog filters with predictable digital components, modern receivers can be built using fewer RF components, resulting in decreased manufacturing costs, higher manufacturing yields, and improved reliability.

The AD6644 is built on the Analog Devices high speed complementary bipolar process (XFCB) and uses an innovative, multipass circuit architecture. Units are packaged in a 52-lead plastic low profile quad flat package (LQFP) specified from –25°C to +85°C.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 65 MSPS.
2. Fully differential analog input stage.
3. Digital outputs can be run on 3.3 V supply for easy interface to digital ASICs.
4. Complete solution: reference and track-and-hold.
5. Packaged in small, surface-mount, plastic, 52-lead LQFP.

FUNCTIONAL BLOCK DIAGRAM

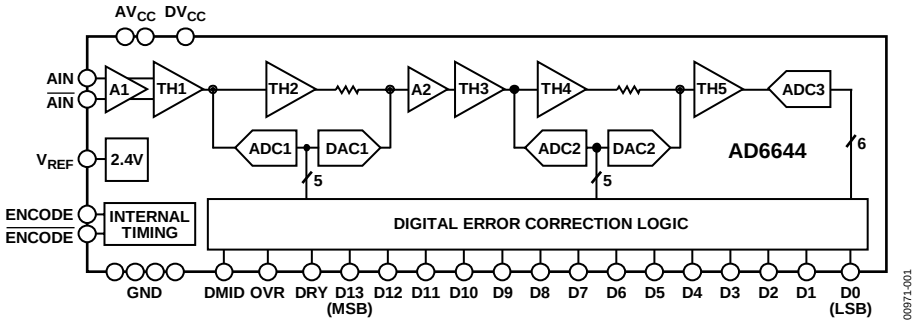


Figure 1.

Rev. D
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REVISION HISTORY

8/07—Rev. C to Rev. D

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Changes to Noise (for Any Range Within the ADC) Definition .. 13
Added Table 8 16
Changes to Evaluation Board Section 18
Changes to Ordering Guide 21

5/03—Data Sheet changed from Rev. B to Rev. C

Updated Outline Dimensions 19

3/03—Data Sheet changed from Rev. A to Rev. B

Change to Digital Specifications Note 2

3/03—Data Sheet changed from Rev. 0 to Rev. A

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SPECIFICATIONS

DC SPECIFICATIONS

AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} = −25°C, T_{MAX} = +85°C, unless otherwise noted.

Table 1.

			AD6644AST-40			AD6644AST-65			
Parameter	**Temp**	**Test Level[1]**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				14			14		Bits
ACCURACY									
No Missing Codes	Full	II		Guaranteed			Guaranteed		
Offset Error	Full	II	−10	+3	+10	−10	+3	+10	mV
Gain Error	Full	II	−10	−6	+10	−10	−6	+10	% FS
Differential Nonlinearity (DNL)	Full	II	−1.0	±0.25	+1.5	−1.0	±0.25	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		±0.50			±0.50		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		10			10		ppm/°C
Gain Error	Full	V		95			95		ppm/°C
POWER SUPPLY REJECTION RATIO (PSRR)	Full	V		±1.0			±1.0		mV/V
REFERENCE OUT (V_{REF})	Full	V		2.4			2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Differential Input Voltage Span	Full	V		2.2			2.2		V p-p
Differential Input Resistance	Full	V		1			1		kΩ
Differential Input Capacitance	25°C	V		1.5			1.5		pF
POWER SUPPLY									
Supply Voltage									
AV_{CC}[2]	Full	II	4.85	5.0	5.25	4.85	5.0	5.25	V
DV_{CC}	Full	II	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Current									
IA_{VCC} (AV_{CC} = 5.0 V)	Full	II		245	276		245	276	mA
ID_{VCC} (DV_{CC} = 3.3 V)	Full	II		30	36		30	36	mA
Rise Time[3]									
AV_{CC}	Full	IV						15	ms
POWER CONSUMPTION	Full	II		1.3	1.5		1.3	1.5	W

[1] See the Explanation of Test Levels section.
[2] AV_{CC} can vary from 4.85 V to 5.25 V. However, rated ac (harmonics) performance is valid only over the range AV_{CC} = 5.0 V to 5.25 V.
[3] Specified for dc supplies with linear rise time characteristics.

DIGITAL SPECIFICATIONS

AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} = −25°C, T_{MAX} = +85°C, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level[1]	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Unit
ENCODE INPUTS (ENCODE, $\overline{\text{ENCODE}}$)									
Differential Input Voltage[2]	Full	IV	0.4			0.4			V p-p
Differential Input Resistance	25°C	V		10			10		kΩ
Differential Input Capacitance	25°C	V		2.5			2.5		pF
LOGIC OUTPUTS (D13 to D0, DRY, OVR)									
Logic Compatibility				CMOS			CMOS		
Logic 1 Voltage[3]	Full	V		2.5			2.5		V
Logic 0 Voltage[3]	Full	V		0.4			0.4		V
Output Coding				Twos complement			Twos complement		
DMID	Full	V		$DV_{CC}/2$			$DV_{CC}/2$		V

[1] See the Explanation of Test Levels section.
[2] All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially. Reference Figure 18 for performance vs. encode power.
[3] Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF degrade performance.

SWITCHING SPECIFICATIONS

AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{\text{ENCODE}}$ = maximum conversion rate MSPS; T_{MIN} = −25°C, T_{MAX} = +85°C, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level[1]	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Unit
Maximum Conversion Rate	Full	II	40			65			MSPS
Minimum Conversion Rate	Full	IV			15			15	MSPS
ENCODE Pulse Width High	Full	IV	10			6.5			ns
ENCODE Pulse Width Low	Full	IV	10			6.5			ns

[1] See the Explanation of Test Levels section.

AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{\text{ENCODE}}$ = maximum conversion rate MSPS; T_{MIN} = −25°C, T_{MAX} = +85°C, C_{LOAD} = 10 Pf, unless otherwise noted.

Table 4.

Parameter	Name	Temp	Test Level[1]	AD6644AST-40/65 Min	AD6644AST-40/65 Typ	AD6644AST-40/65 Max	Unit
ENCODE INPUT PARAMETERS[2]							
Encode Period @ 65 MSPS	t_{ENC}	Full	V		15.4		ns
Encode Period @ 40 MSPS	t_{ENC}	Full	V		25		ns
Encode Pulse Width High[3] @ 65 MSPS	t_{ENCH}	Full	IV	6.2	7.7	9.2	ns
Encode Pulse Width Low @ 65 MSPS	t_{ENCL}	Full	IV	6.2	7.7	9.2	ns
ENCODE/DATA READY							
Encode Rising to Data Ready Falling	t_{DR}	Full	IV	2.6	3.4	4.6	ns
Encode Rising to Data Ready Rising	t_{E_DR}				$t_{ENCH} + t_{DR}$		
@ 65 MSPS (50% Duty Cycle)		Full	IV	10.3	11.1	12.3	ns
@ 40 MSPS (50% Duty Cycle)		Full	IV	15.1	15.9	17.1	ns
ENCODE/DATA (D13:0), OVR							
ENCODE to DATA Falling Low	t_{E_FL}	Full	IV	3.8	5.5	9.2	ns
ENCODE to DATA Rising Low	t_{E_RL}	Full	IV	3.0	4.3	6.4	ns
ENCODE to DATA Delay (Hold Time)[4]	t_{H_E}	Full	IV	3.0	4.3	6.4	ns
ENCODE to DATA Delay (Setup Time)[5]	t_{S_E}				$t_{ENC} - t_{E_FL}$		
Encode = 65 MSPS (50% Duty Cycle)		Full	IV	6.2	9.8	11.6	ns
Encode = 40 MSPS (50% Duty Cycle)		Full	IV	15.9	19.4	21.2	ns

Parameter	Name	Temp	Test Level[1]	AD6644AST-40/65 Min	Typ	Max	Unit
DATA READY (DRY[6])/DATA, OVR							
Data Ready to DATA Delay (Hold Time)[3]	t_{H_DR}				See note[7]		
Encode = 65 MSPS (50% Duty Cycle)		Full	IV	8.0	8.6	9.4	ns
Encode = 40 MSPS (50% Duty Cycle)		Full	IV	12.8	13.4	14.2	ns
Data Ready to DATA Delay (Setup Time)[3]	t_{S_DR}				See note[7]		
@ 65 MSPS (50% Duty Cycle)		Full	IV	3.2	5.5	6.5	ns
@ 40 MSPS (50% Duty Cycle)		Full	IV	8.0	10.3	11.3	ns
APERTURE DELAY	t_A	25°C	V		100		ps
APERTURE UNCERTAINTY (JITTER)	t_J	25°C	V		0.2		ps rms

[1] See the Explanation of Test Levels section.
[2] Several timing parameters are a function of t_{ENC} and t_{ENCH}.
[3] To compensate for a change in duty cycle for t_{H_DR} and t_{S_DR} use the following equations:
$Newt_{H_DR} = (t_{H_DR} - \%\ Change(t_{ENCH})) \times t_{ENC}/2$
$Newt_{S_DR} = (t_{S_DR} - \%\ Change(t_{ENCH})) \times t_{ENC}/2$
[4] ENCODE to data delay (hold time) is the absolute minimum propagation delay through the ADC.
[5] ENCODE to data delay (setup time) is calculated relative to 65 MSPS (50% duty cycle). To calculate t_{S_E} for a given encode, use the following equation:
$Newt_{S_E} = t_{ENC(NEW)} - t_{ENC} + t_{S_E}$ (that is, for 40 MSPS, $Newt_{S_E(TYP)} = 25 \times 10^{-9} - 15.38 \times 10^{-9} + 9.8 \times 10^{-9} = 19.4 \times 10^{-9}$).
[6] DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock correspondingly changes the duty cycle of DRY.
[7] Data ready to data delay (t_{H_DR} and t_{S_DR}) is calculated relative to 65 MSPS (50% duty cycle) and is dependent on t_{ENC} and duty cycle. To calculate t_{H_DR} and t_{S_DR} for a given encode, use the following equations:
$Newt_{H_DR} = t_{ENC(NEW)}/2 - t_{ENCH} + t_{H_DR}$ (that is, for 40 MSPS, $Newt_{H_DR(TYP)} = 12.5 \times 10^{-9} - 7.69 \times 10^{-9} + 8.6 \times 10^{-9} = 13.4 \times 10^{-9}$).
$Newt_{S_DR} = t_{ENC(NEW)}/2 - t_{ENCH} + t_{S_DR}$ (that is, for 40 MSPS, $Newt_{S_DR(TYP)} = 12.5 \times 10^{-9} - 7.69 \times 10^{-9} + 5.5 \times 10^{-9} = 10.3 \times 10^{-9}$).

AC SPECIFICATIONS

All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.

AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{\text{ENCODE}}$ = maximum conversion rate MSPS; T_{MIN} = −25°C, T_{MAX} = +85°C, unless otherwise noted.

Table 5.

Parameter	Conditions	Temp	Test Level[1]	AD6644AST-40 Min	Typ	Max	AD6644AST-65 Min	Typ	Max	Unit
SNR										
Analog Input	2.2 MHz	25°C	V		74.5			74.5		dB
@ −1 dBFS	15.5 MHz	25°C	II		74.0		72	74.0		dB
	30.5 MHz	25°C	II		73.5		72	73.5		dB
SINAD[2]										
Analog Input	2.2 MHz	25°C	V		74.5			74.5		dB
@ −1 dBFS	15.5 MHz	25°C	II		74.0		72	74.0		dB
	30.5 MHz	25°C	V		73.0			73.0		dB
WORST HARMONIC (2ND or 3RD)[2]										
Analog Input	2.2 MHz	25°C	V		92			92		dBc
@ −1 dBFS	15.5 MHz	25°C	II		90		83	90		dBc
	30.5 MHz	25°C	V		85			85		dBc
WORST HARMONIC (4TH or Higher)[2]										
Analog Input	2.2 MHz	25°C	V		93			93		dBc
@ −1 dBFS	15.5 MHz	25°C	II		92		85	92		dBc
	30.5 MHz	25°C	V		92			92		dBc
TWO-TONE SFDR[2, 3, 4]		Full	V		100			100		dBFS
TWO-TONE IMD REJECTION[2, 4]										
F1, F2 @ −7 dBFS		Full	V		90			90		dBc
ANALOG INPUT BANDWIDTH		25°C	V		250			250		MHz

[1] See the Explanation of Test Levels section.
[2] AV_{CC} = 5 V to 5.25 V for rated ac performance.
[3] Analog input signal power swept from −7 dBFS to −100 dBFS.
[4] F1 = 15 MHz, F2 = 15.5 MHz.

TIMING DIAGRAM

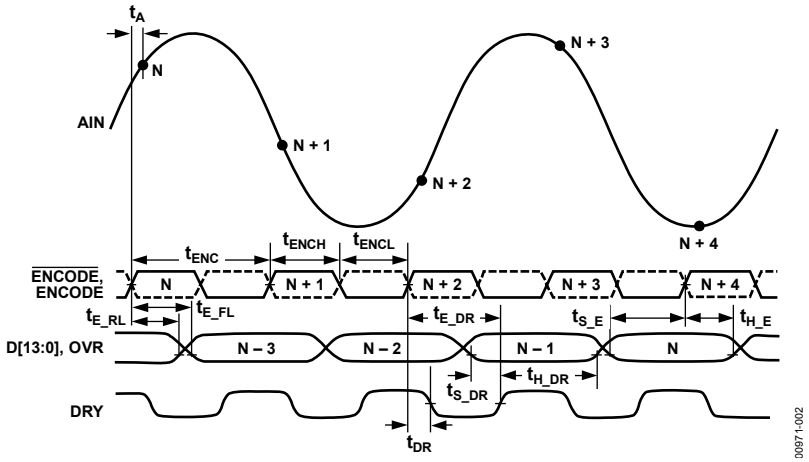


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AV_{CC} Voltage	0 V to 7 V
DV_{CC} Voltage	0 V to 7 V
Analog Input Voltage	0 V to AV_{CC}
Analog Input Current	25 mA
Digital Input Voltage	0 V to AV_{CC}
Digital Output Current	4 mA
Environmental	
Operating Temperature Range (Ambient)	−25°C to +85°C
Storage Temperature Range (Ambient)	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Maximum Junction Temperature	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.
II. 100% production tested at 25°C, and guaranteed by design and characterization at temperature extremes.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.

THERMAL RESISTANCE

The following measurements were taken on a 6-layer board in still air with a solid ground plane.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
52-lead LQFP	33	11	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

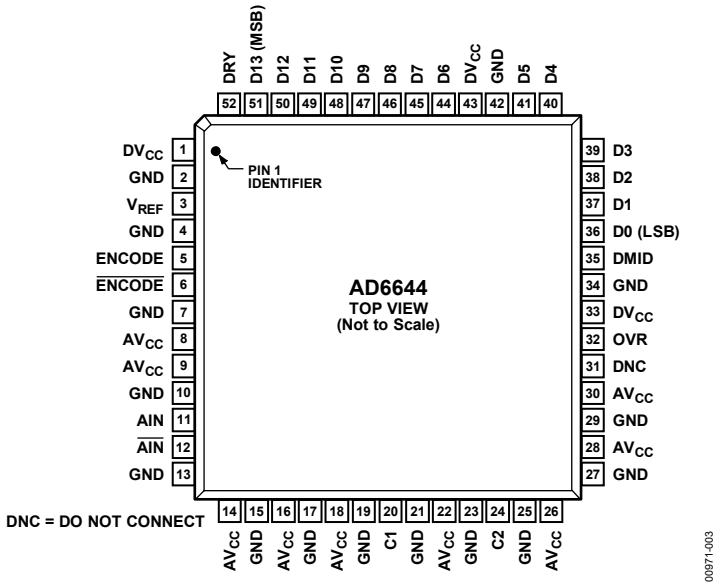


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 33, 43	DV_{CC}	3.3 V Power Supply (Digital), Output Stage Only.
2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	GND	Ground.
3	V_{REF}	2.4 V (Analog Reference). Bypass to ground with 0.1 µF microwave chip capacitor.
5	ENCODE	Encode Input. Conversion initiated on rising edge.
6	$\overline{\text{ENCODE}}$	Complement of ENCODE. Differential input.
8, 9, 14, 16, 18, 22, 26, 28, 30	AV_{CC}	5 V Analog Power Supply.
11	AIN	Analog Input.
12	$\overline{\text{AIN}}$	Complement of AIN. Differential analog input.
20	C1	Internal Voltage Reference. Bypass to ground with 0.1 µF microwave chip capacitor.
24	C2	Internal Voltage Reference. Bypass to ground with 0.1 µF microwave chip capacitor.
31	DNC	Do not connect this pin.
32	OVR	Overrange Bit. High indicates analog input exceeds ±FS.
35	DMID	Output Data Voltage Midpoint. Approximately equal to $DV_{CC}/2$.
36	D0 (LSB)	Digital Output Bit (Least Significant Bit). Twos complement.
37 to 41, 44 to 50	D1 to D5, D6 to D12	Digital Output Bits in Twos Complement.
51	D13 (MSB)	Digital Output Bit (Most Significant Bit). Twos complement.
52	DRY	Data Ready Output.

TYPICAL PERFORMANCE CHARACTERISTICS

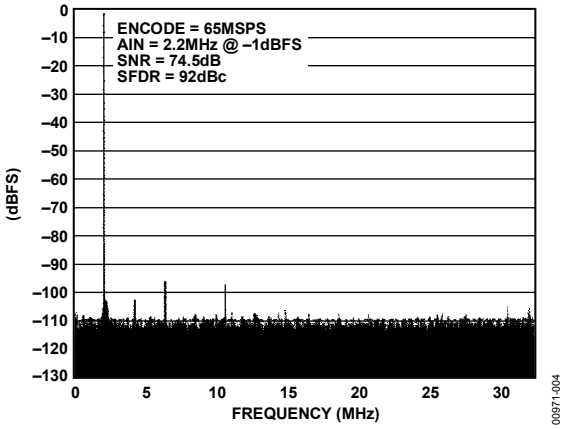


Figure 4. Single Tone at 2.2. MHz

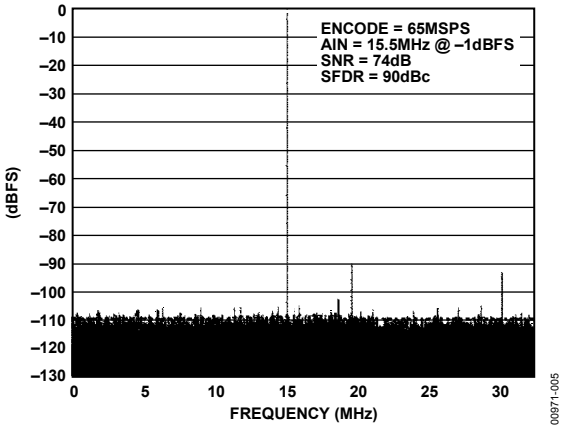


Figure 5. Single Tone at 15.5 MHz

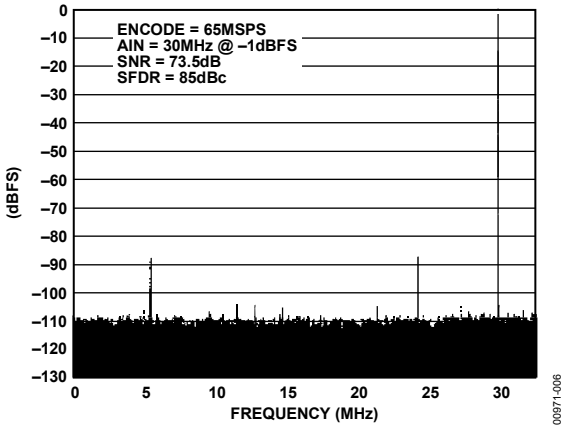


Figure 6. Single Tone at 30 MHz

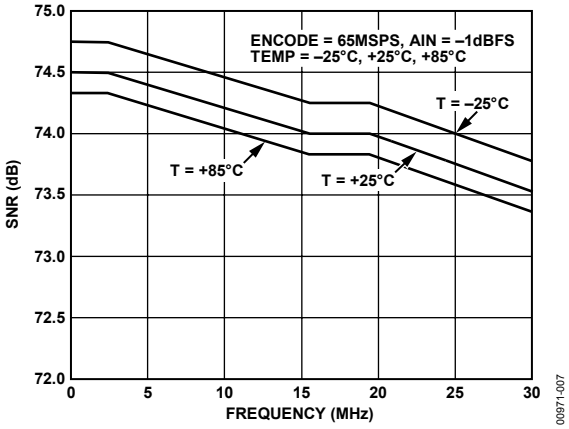


Figure 7. Noise vs. Analog Frequency (Nyquist)

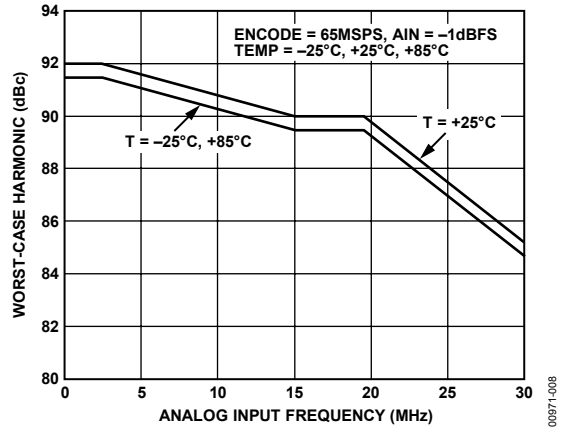


Figure 8. Harmonics vs. Analog Frequency (Nyquist)

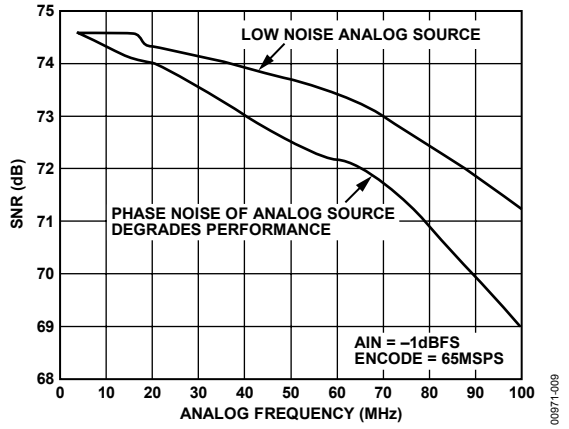


Figure 9. Noise vs. Analog Frequency (IF)

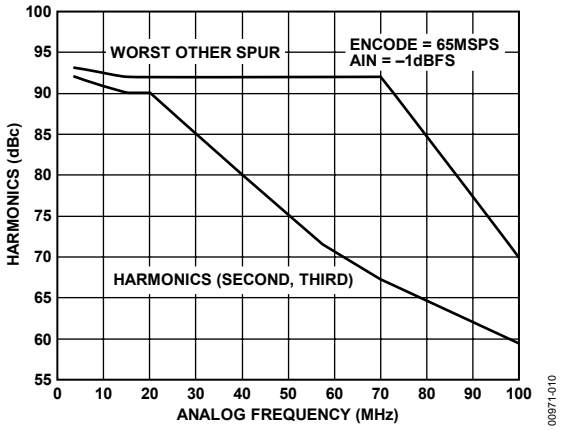


Figure 10. Harmonics vs. Analog Frequency (IF)

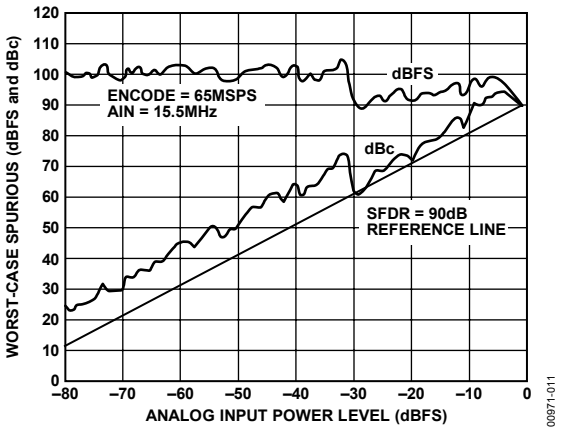


Figure 11. Single-Tone SFDR

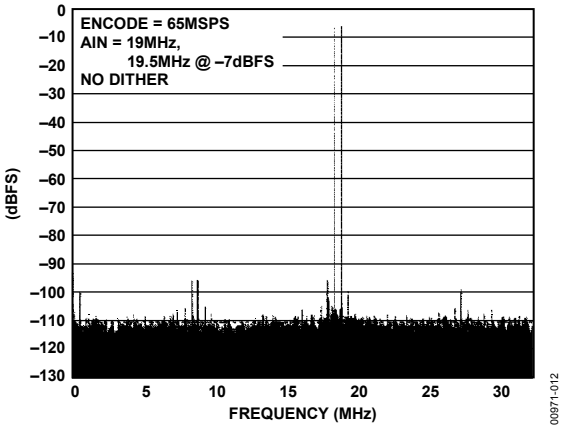


Figure 12. Two Tones at 19 MHz and 19.5 MHz

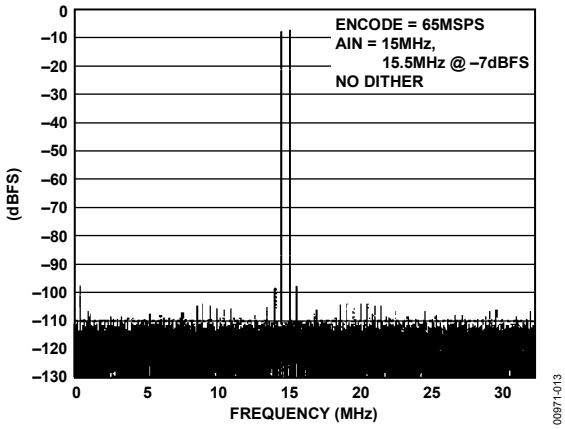


Figure 13. Two Tones at 15 MHz and 15.5 MHz

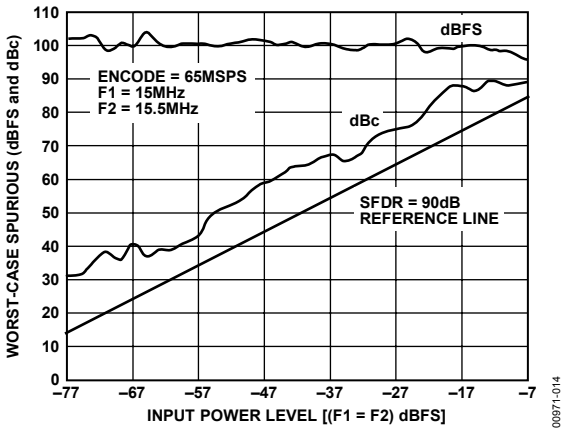


Figure 14. Two-Tone SFDR

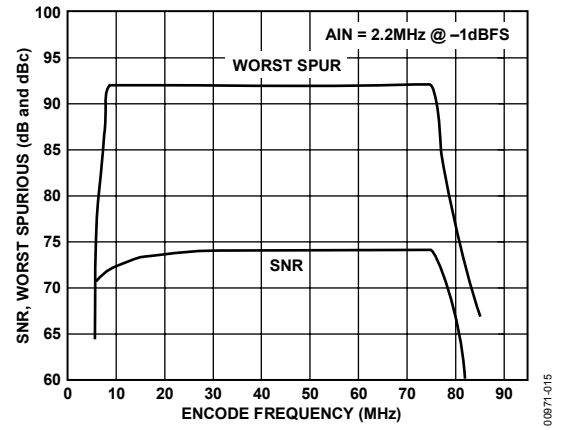


Figure 15. SNR, Worst Spurious vs. Encode

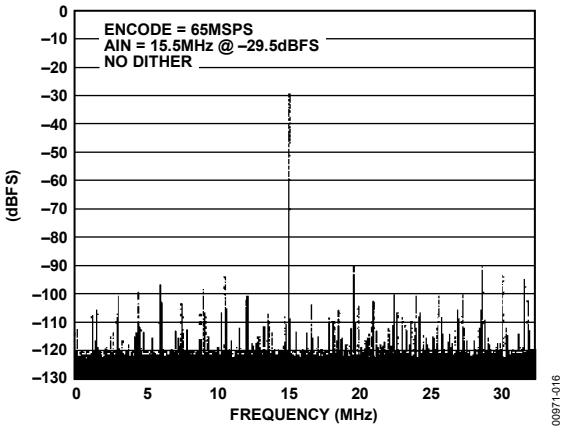


Figure 16. 1M FFT Without Dither

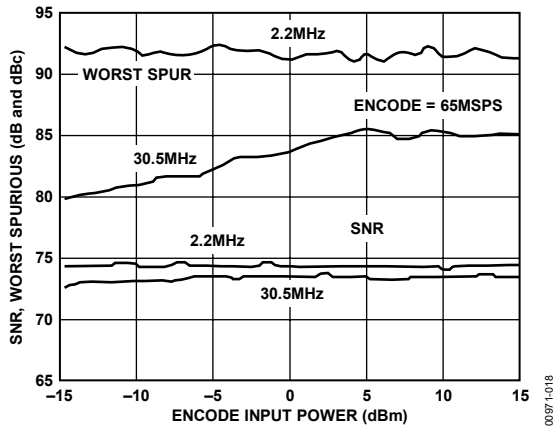


Figure 18. SNR, Worst Spurious vs. Clamped Encode Power (See Figure 27)

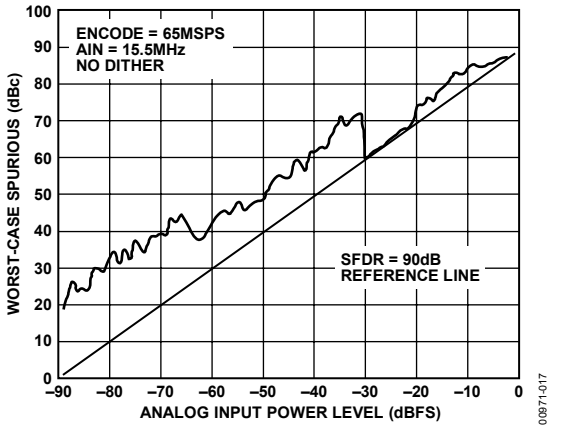


Figure 17. SFDR Without Dither

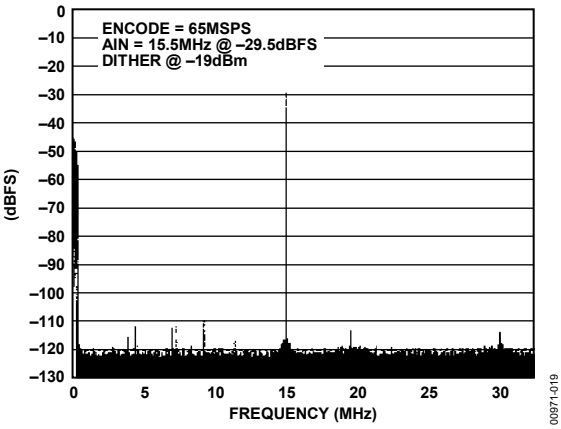


Figure 19. 1M FFT with Dither

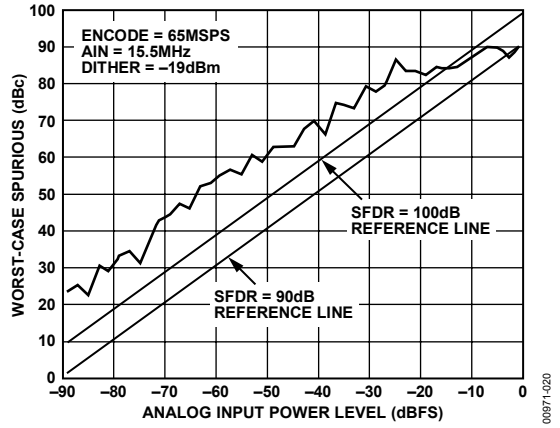


Figure 20. SFDR with Dither

EQUIVALENT CIRCUITS

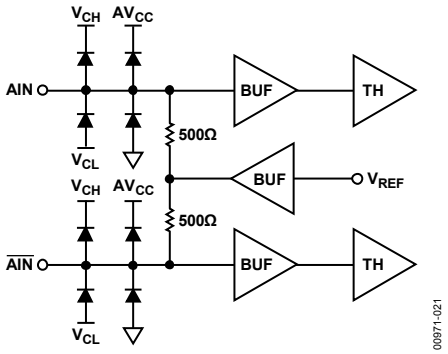


Figure 21. Analog Input Stage

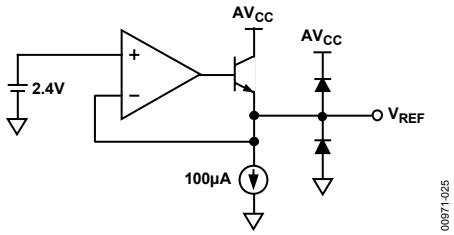


Figure 24. 2.4 V Reference

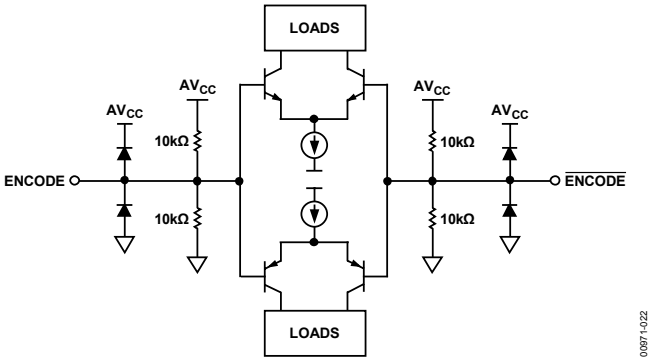


Figure 22. ENCODE/$\overline{\text{ENCODE}}$ Inputs

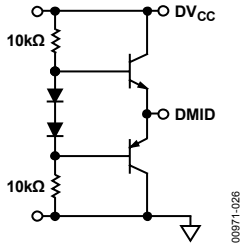


Figure 25. DMID Reference

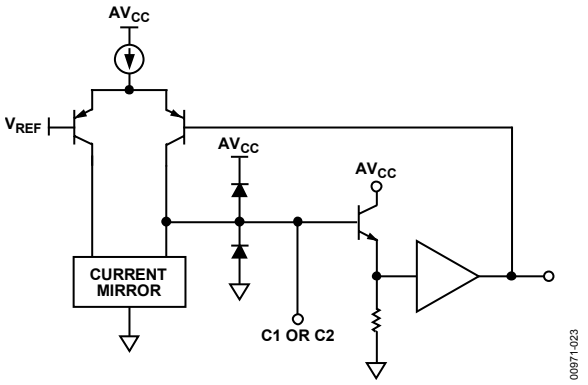


Figure 23. Compensation Pin, C1 or C2

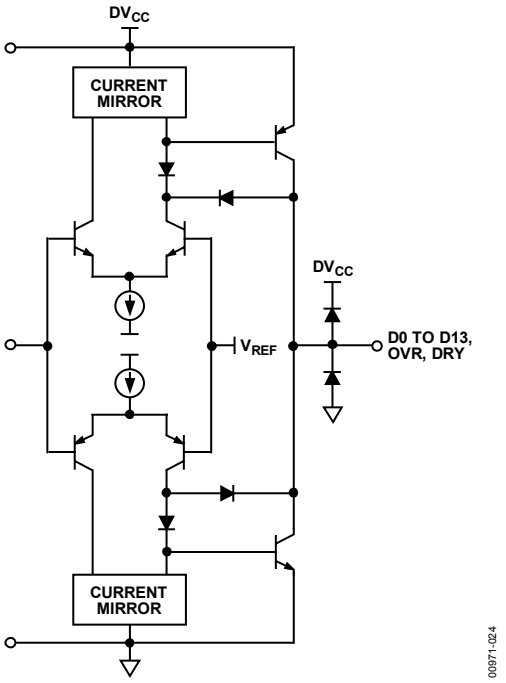


Figure 26. Digital Output Stage

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input phase 180° and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in the Logic 1 state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in a low state. Optimum performance is achieved using a 50% duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$POWER_{Full\ Scale} = 10\log\left[\frac{\frac{V^2\ Full-Scale\ rms}{|Z|_{Input}}}{0.001}\right]$$

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least-square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Noise (for Any Range Within the ADC)

$$V_{NOISE} = \sqrt{|Z|\times 0.001\times 10\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}$$

where:
Z is the input impedance.
FS is the full scale of the device for the frequency in question.
SNR is the value for the particular input level.
Signal is the signal level within the ADC reported in dB below full scale.

V_{NOISE} includes both thermal and quantization noise.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$, and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. Reported in either dBc (that is, degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. Reported in either dBc (that is, degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics) reported in dBc.

THEORY OF OPERATION

The AD6644 analog-to-digital converter (ADC) employs a three-stage subrange architecture. This design approach achieves the required accuracy and speed while maintaining low power and small die size.

As shown in the functional block diagram, the AD6644 has complementary analog input pins, AIN and $\overline{\text{AIN}}$. Each analog input is centered at 2.4 V and swings ±0.55 V around this reference (Figure 21). Because AIN and $\overline{\text{AIN}}$ are 180° out of phase, the differential analog input signal is 2.2 V peak-to-peak.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives a 5-bit digital-to-analog converter (DAC1). DAC1 requires 14 bits of precision, which is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residue signal is applied to a second conversion stage consisting of a 5-bit ADC2, 5-bit DAC2, and pipeline TH4. The second DAC requires 10 bits of precision, which is met by the process with no trim. The input to TH5 is a second residue signal generated by subtracting the quantized output of DAC2 from the first residue signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS-compatible word, coded as twos complement.

APPLYING THE AD6644

Encoding the AD6644

The AD6644 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 70 MHz input signals when using a high jitter clock source. See the Analog Devices Application Note AN-501, *Aperture Uncertainty and ADC System Performance*, for complete details.

For optimum performance, the AD6644 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

See Figure 27 for one preferred method for clocking the AD6644. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary windings of the transformer limit clock excursions into the AD6644 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD6644, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100 Ω) is placed in series with the primary winding of the transformer.

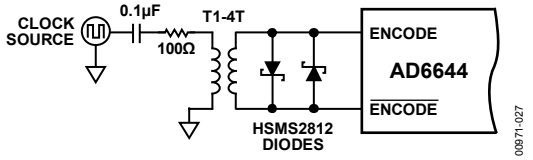


Figure 27. Crystal Clock Oscillator—Differential Encode

If a low jitter ECL/PECL clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown in Figure 28. A device that offers excellent jitter performance is the MC100LVEL16 (or another in the same family) from Motorola.

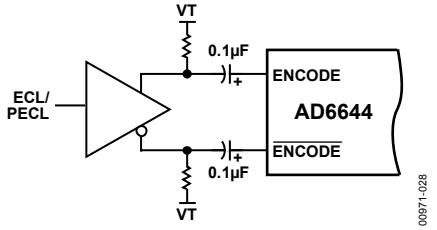


Figure 28. Differential ECL for Encode

Analog Input

As with most new high speed, high dynamic range ADCs, the analog input to the AD6644 is differential. Differential inputs allow much improvement in performance on-chip as signals are processed through the analog stages. Most of the improvement is a result of differential analog stages having high rejection of even-order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection of stray signals such as ground and power noise. In addition, they provide good rejection of common-mode signals such as local oscillator feedthrough.

The AD6644 input voltage range is offset from ground by 2.4 V. Each analog input connects through a 500 Ω resistor to a 2.4 V bias voltage and to the input of a differential buffer (Figure 21). The resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6644 should be ac-coupled to the input pins. Because the differential input impedance of the AD6644 is 1 kΩ, the analog input power requirement is only −2 dBm, simplifying the driver amplifier in many cases. To take full advantage of this high input impedance, a 20:1 transformer is required. This is a large ratio and could result in unsatisfactory performance. In this case, a lower step-up ratio can be used. The recommended method for driving the analog input of the AD6644 is to use a 4:1 RF transformer. For example, if R_T is set to 60.4 Ω and R_S is set to 25 Ω, along with a 4:1 transformer, the

input matches to a 50 Ω source with a full-scale drive of 4.8 dBm. Series resistors (R_S) on the secondary side of the transformer should be used to isolate the transformer from the ADC. This limits the amount of dynamic current from the ADC flowing back into the secondary of the transformer. The terminating resistor (R_T) should be placed on the primary side of the transformer.

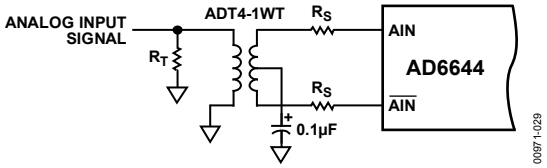


Figure 29. Transformer-Coupled Analog Input Circuit

In applications where dc coupling is required, the AD8138 differential output op amp from Analog Devices can be used to drive the AD6644 (see Figure 30). The AD8138 op amp provides single-ended-to-differential conversion, which reduces overall system cost and minimizes layout requirements.

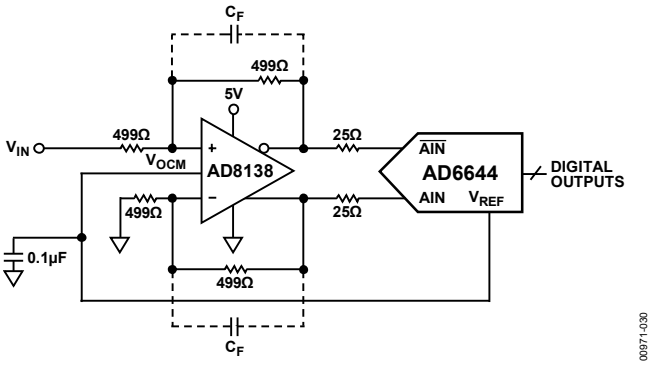


Figure 30. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be received by the AD6644. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD6644 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. AV_{CC} and DV_{CC} should have separate power supplies. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD6644 is specified for DV_{CC} = 3.3 V because this is a common supply for digital ASICs.

Digital Outputs

Care must be taken when designing the data receivers for the AD6644. It is recommended that the digital outputs drive a series resistor (for example, 100 Ω) followed by a gate like the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic of Figure 32. The digital outputs of the AD6644 have a constant output slew rate of 1 V/ns.

A typical CMOS gate combined with a PCB trace have a load of approximately 10 pF. Therefore, as each bit switches, 10 mA (10 pF × 1 V ÷ 1 ns) of dynamic current per bit flow in or out of the device. A full-scale transition can cause up to 140 mA (14 bits × 10 mA/bit) of current to flow through the output stages. The series resistors should be placed as close as possible to the AD6644 to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided because they can appreciably add to the dynamic switching currents of the AD6644. Note that extra capacitive loading increases output timing and invalidates timing specifications. Digital output timing is guaranteed with 10 pF loads.

If the analog input range is exceeded, the overrange (OVR) bit toggles high and the digital outputs retain their respective positive or negative full-scale values.

Table 9. Twos Complement Output Coding

AIN Level	$\overline{AIN}$ Level	Output State	Output Code
V_{REF} + 0.55 V	V_{REF} − 0.55 V	Positive FS	01 1111 1111 1111
V_{REF}	V_{REF}	Midscale	00…0/11…1
V_{REF} − 0.55 V	V_{REF} + 0.55 V	Negative FS	10 0000 0000 0000

Layout Information

The schematic of the evaluation board (see Figure 32) represents a typical implementation of the AD6644. A multilayer board is recommended to achieve the best results. It is highly recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6644 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6644, minimal capacitive loading should be placed on these outputs. It is recommended that a fanout of only one gate be used for all AD6644 digital outputs. The layout of the encode circuit is equally critical. Any noise received on this circuitry results in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

Jitter Considerations

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, Equation 1 accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter (see Equation 1).

$$SNR = -20 \times \log\left[\left(\frac{1+\varepsilon}{2^n}\right)^2 + \left(2\pi \times f_{ANALOG} \times t_{j\,rms}\right)^2 + \left(\frac{V_{NOISE\,rms}}{2^n}\right)^2\right]^{1/2} \quad (1)$$

where:

f_{ANALOG} is the analog input frequency.

$t_{j\,rms}$ is the rms jitter of the encode (rms sum of encode source and internal encode circuitry).

ε is the average DNL of the ADC (typically 0.41 LSB).

n is the number of bits in the ADC.

$V_{NOISE\,rms}$ is the V rms thermal noise referred to the analog input of the ADC (typically 2.5 LSB).

For a 14-bit ADC like the AD6644, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. Figure 31 shows a family of curves that demonstrates the expected SNR performance of the AD6644 as jitter increases and is derived from Equation 1.

For a complete review of aperture jitter, see Application Note AN-756, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, at www.analog.com.

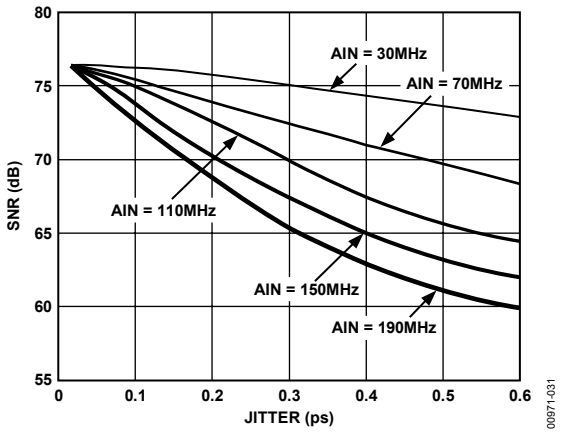


Figure 31. SNR vs. Jitter

EVALUATION BOARD

The schematic of the evaluation board (see Figure 32) represents a typical implementation of the AD6644. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6644 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

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The layout of the encode circuit is equally critical. Any noise received on this circuitry results in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

Table 10. AD6644/PCB Bill of Materials

Qty.	Reference ID[1]	Description	Manufacturer	Supplier Part No.
1	PCB	Printed circuit board, AD6644/AD6645 engineering evaluation board	Moog	6645EE01D REV D
4	C1, C2, C31, C38	Capacitor, tantalum, SMT BCAPTAJC, 10 µF, 16 V, 10%	Kemet	T491C106K016AS
8	C3, C7 to C10, C16, C30[2], C32	Capacitor, ceramic, SMT 0508, 0.1 µF, 16 V, 10%	Presidio Components	0508X7R104K16VP3
9	C4, C15, C22 to C26, C29, (C33)[3], (C34)[3], C39	Capacitor, ceramic, SMT 0805, 0.1 µF, 25 V, 10%	Panasonic	ECJ-2VB1E104K
0	(C5, C6)[3]	Capacitor, ceramic, SMT 0805, 0.01 µF, 50 V, 10%	Panasonic	ECJ-2YB1H103K
10	C11 to C14, C17 to 21, C40	Capacitor, ceramic, SMT 0508, 0.01 µF, 50 V, 0.2%	Presidio Components	0508X7R103M2P3
0	(C27, 28)	Capacitor, ceramic, SMT 0805, select		
1	CR1[3]	Diode, dual Schottky HSMS2812, SOT-23, 30 V, 20 mA	Panasonic	MA716-(TX)
1	E1	Install jumper (across OPT_LAT and BUFLAT)		
5	F1 to F5	EMI suppression ferrite chip, SMT 0805	Steward	HZ0805E601R-00
1	J1-H	Header, 6-pin, pin strip, 5 mm pitch	Wieland	Z5.530.0625.0
1	J1	Pin strip, 6-pin, 5 mm pitch	Wieland	25.602.2653.0
1	J2	Header, 40-pin, male, right angle	Samtec	TSW-120-08-T-D-RA
2	(J3), J4, J5	Connector, gold, male, COAX., SMA, vertical	Johnson Components™	142-0701-201
1	L1	Inductor, SMT, 1008-ct package, 4.7 nH	Coilcraft®	1008CT-040X-J
0	(R1)[3]	Resistor, thick film, SMT 0402, 100 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF1000V
0	(R2)	Resistor, thick film, SMT 1206, 60.4 Ω, 1/8 W, 1%	Panasonic	ERJ-8ENF60R4V
2	(R3 to R5)[2], (R8)[2], R9, R10	Resistor, thick film, SMT 0805, 500 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF4990V
2	R6 and R7	Resistor, thick film, SMT 0805, 25.5 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF25R5V
0	(R11)[3], (R13)[3]	Resistor, thick film, SMT 0805, 66.5 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF66R5V
0	(R12)[3], (R14)[3]	Resistor, thick film, SMT 0805, 100 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF1000V
1	R15[2]	Resistor, thick film, SMT 0402, 178 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF1780X
1	R35	Resistor, thick film, SMT 0805, 49.9 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF49R9V
4	RN1 to RN4	Resistor array, SMT 0402; 100 Ω; 8 ISO RES.,1/4 W; 5%	Panasonic	EXB2HV101JV
2	T2[3], T3[2]	Transformer, ADT4-1WT, CD542, 2 MHz to 775 MHz	Mini-Circuits®	ADT4-1WT
1	U1	IC, 14-bit, 65 MSPS ADC, LQFP-52	Analog Devices	AD6644
2	U2, U7	IC, SOIC-20, OCTAL D-type flip-flop	Fairchild	74LCX574
0	(U3)[2]	IC, SOIC-8, low distortion differential ADC driver	Analog Devices	AD8138ARM
2	U4, U6	IC, SOT-23, tiny logic UHS 2-input or gate	Fairchild	NC7SZ32
0	(U8)[3]	IC, SOIC-8, differential receiver	Motorola	MC100LVEL16
1	Y1	Clock oscillator, 65 MHz	CTS Reeves	MX045-65
4	Y1-PS	Pin sockets, closed end	AMP	5-330808-3
4	STDOFF	Circuit board support	RICHO	CBSB-14-01

[1] Reference designators in parentheses are not installed on standard units.
[2] AC-coupled AIN is standard: R3, R4, R5, R8, and U3 are not installed. If dc-coupled AIN is required, C30, R15, and T3 are not installed.
[3] AC-coupled encode is standard: C5, C6, C33, C34, R1, R11 to R14, and U8 are not installed. If PECL encode is required, CR1 and T2 are not installed.

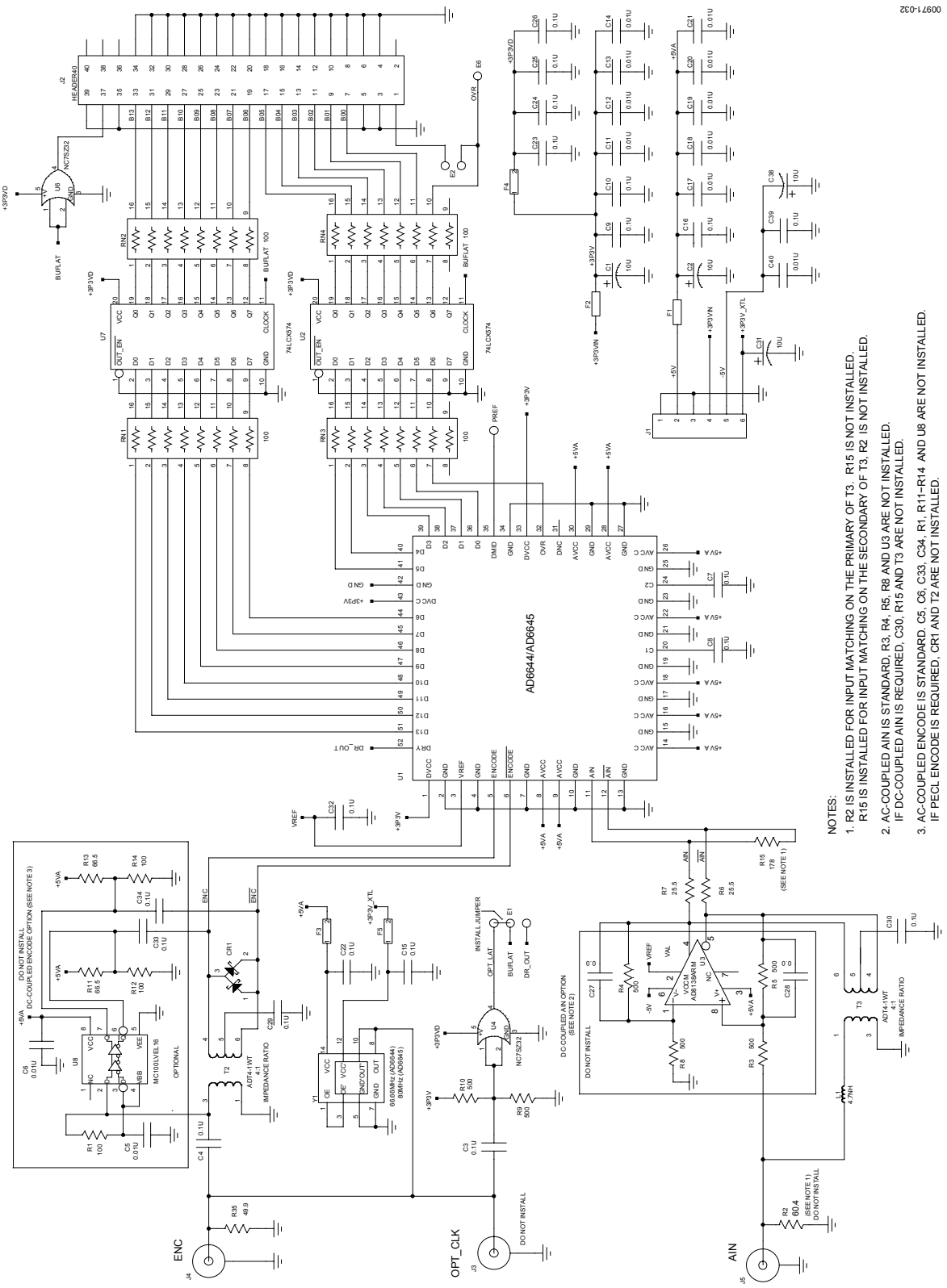


Figure 32. Evaluation Board Schematic

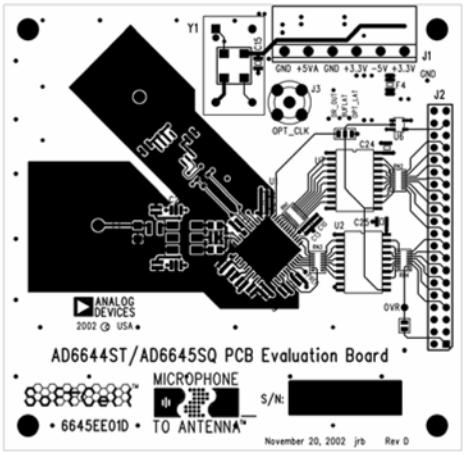


Figure 33. Top Signal Level

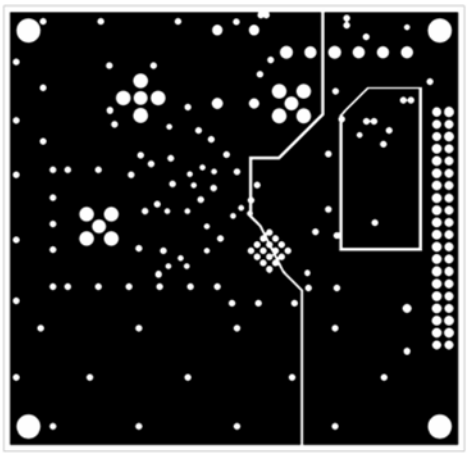


Figure 34. 5.0 V Plane Layer 3 and 3.3 V Plane Layer 4

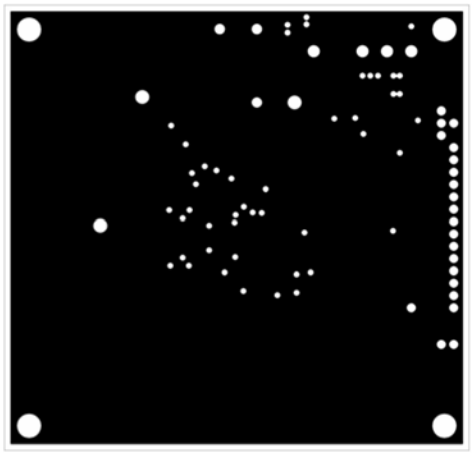


Figure 35. Ground Plane Layer 2 and Ground Plane Layer 5

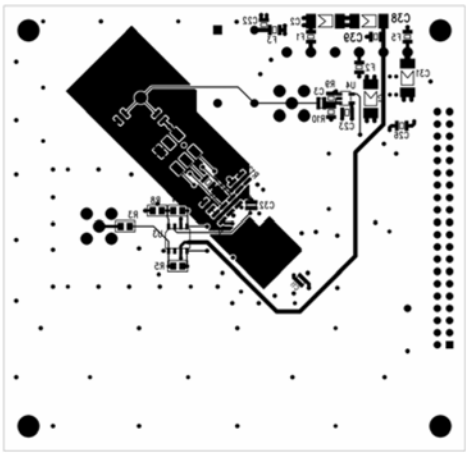


Figure 36. Bottom Signal Layer

OUTLINE DIMENSIONS

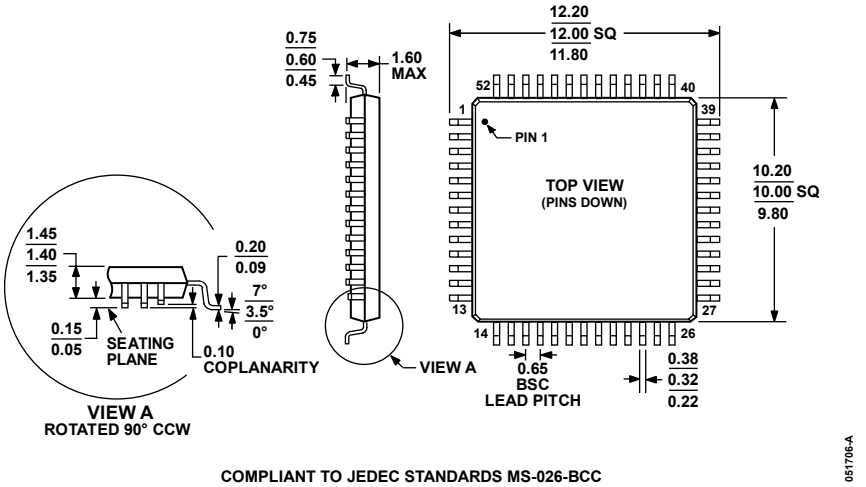


Figure 37. 52-Lead Low Profile Quad Flat Package [LQFP]
(ST-52)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6644AST-40	−25°C to +85°C	52-Lead Low Profile Quad Flat Package (LQFP)	ST-52
AD6644ASTZ-40[1]	−25°C to +85°C	52-Lead Low Profile Quad Flat Package (LQFP)	ST-52
AD6644AST-65	−25°C to +85°C	52-Lead Low Profile Quad Flat Package (LQFP)	ST-52
AD6644ASTZ-65[1]	−25°C to +85°C	52-Lead Low Profile Quad Flat Package (LQFP)	ST-52
AD6644ST/PCB		Evaluation Board with AD6644AST–65	
AD6644ST/PCBZ[1]		Evaluation Board with AD6644AST–65	

[1] Z = RoHS Compliant Part.

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