International
IOR Rectifier

Data Sheet No. PD 60321A

IRS26302DJPBF

FULLY PROTECTED 3-PHASE BRIDGE PLUS ONE GATE DRIVER

Features

- Floating channel designed for bootstrap operation, fully
- operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Full three phase gate driver plus one low side driver
- Undervoltage lockout for all channels
- Cross-conduction prevention logic
- Power-on reset
- Integrated bootstrap diode for floating channel supply
- Over current protection on: DC-(Itrip), DC+(Ground fault), PFCtrip/BRtrip (PFC/Brake protection).
- Single pin fault diagnostic function
- Diagnostic protocol to address fault register
- Self biasing for ground fault detection high voltage circuit
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- RoHS compliant

Typical Applications

- Air conditioners inverters
- Micro/Mini inverter drives
- General purpose inverter
- Motor control

Product Summary

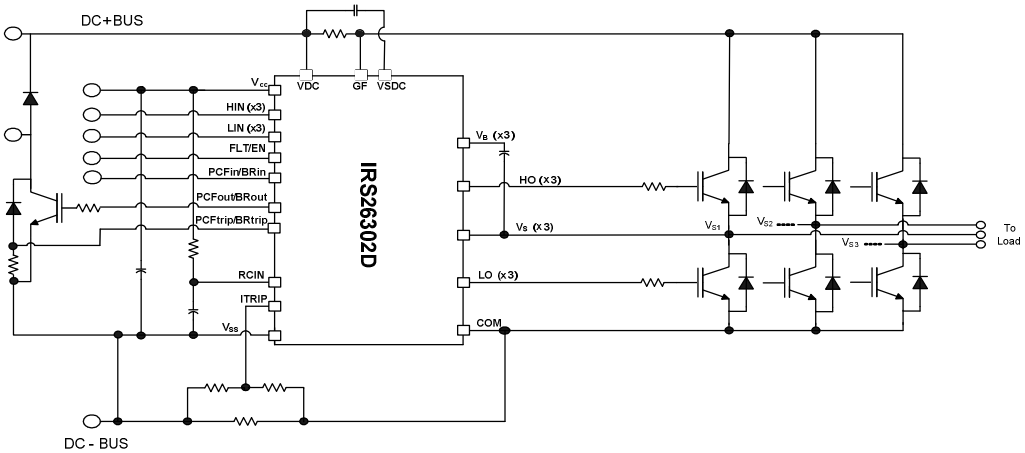
Topology	3 Phase
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	200 mA & 350 mA
Deadtime (typical)	290 ns

Package



44-Lead PLCC

Typical Connection Diagram



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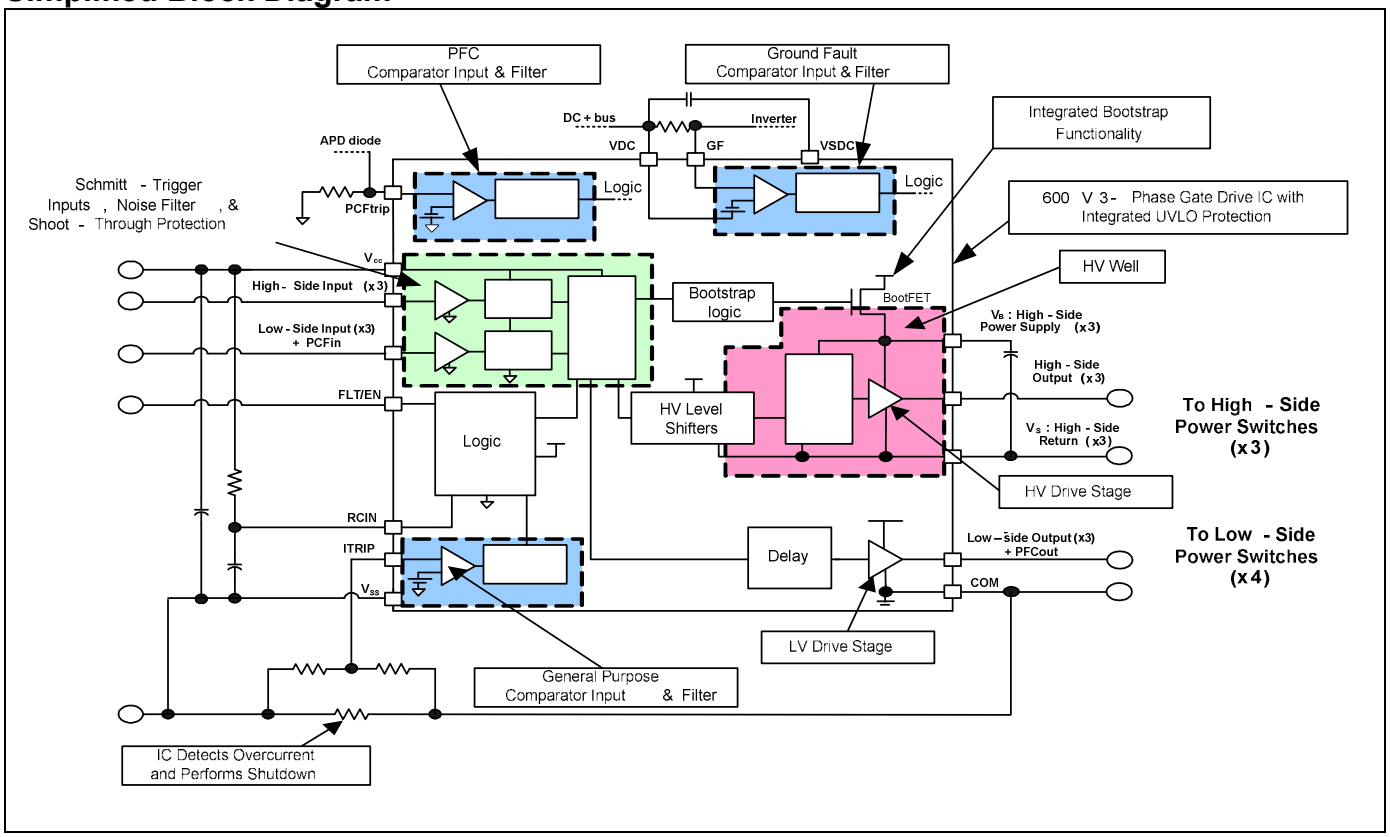
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Description

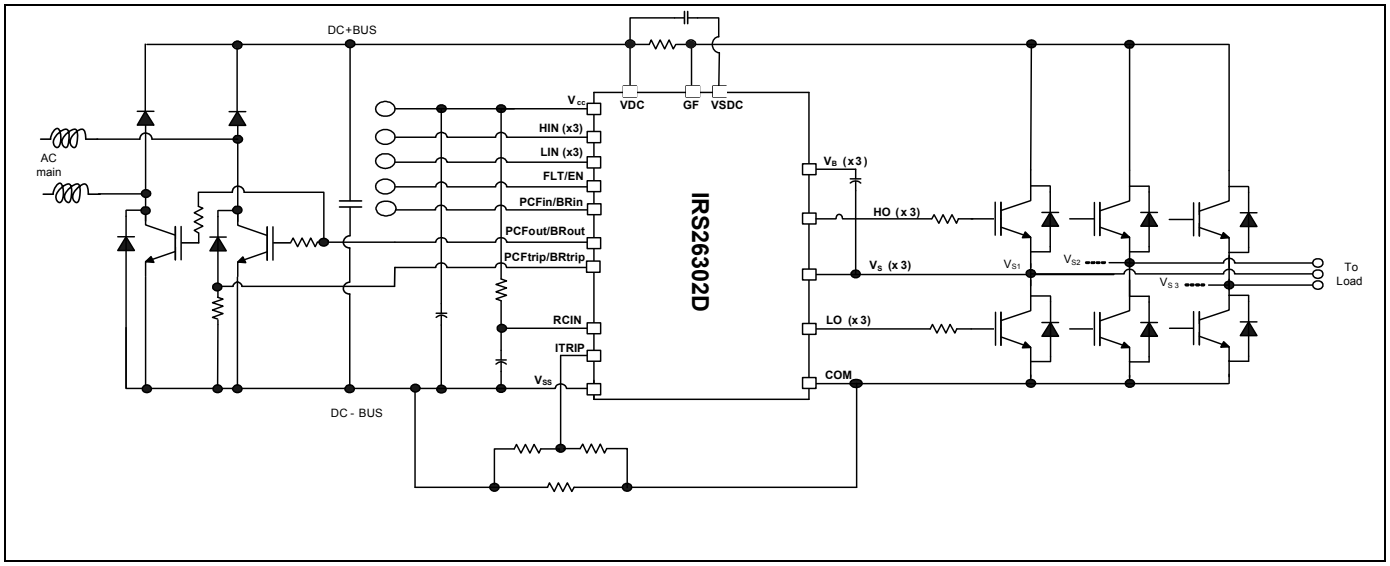
The IRS26302DJPBF are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. An additional low side driver is included for PFC or Brake IGBT driving operation. Proprietary HVIC technology enables rugged monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. Three current trip functions that terminate all seven outputs can be derived from three external shunt resistors. Each overcurrent trip functions consists of detecting excess current across a shunt resistor on DC+ bus, on DC- bus and on Brake or PFC circuitry. An enable function is available to terminate all outputs simultaneously and is provided through a bidirectional pin combined with an open-drain FAULT pin. Fault signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after an externally programmed delay via an RC network connected to the RCIN input. A diagnostic feature can give back to the controller the fault cause (UVcc, DC- or DC- overcurrent) and address a fault register. The output drivers feature a high pulse current buffer stage. Propagation delays are matched to simplify use in high frequency applications designed for minimum driver cross conduction. The floating channel can be used to drive N-channel power MOSFET's or IGBT's in the high side configuration which operates up to 600 V.

Simplified Block Diagram



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Typical Application Diagram



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Qualification Information†

Qualification Level		Industrial†† (per JEDEC JESD 47E)	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		PLCC44	MSL3††† (per IPC/JEDEC J-STD-020C)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A114D)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A115-A)	
	Charged Device Model	Class IV (per JEDEC standard JESD22-C101C)	
IC Latch-Up Test		Class I, Level A (per JESD78A)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Voltage clamps are included between V_{CC} & COM (25 V), V_{CC} & V_{SS} (20 V), and V_B & V_S (20 V).

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	-0.3	620	V
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
$V_{S1,2,3}$	High side offset voltage	$V_{B1,2,3}$ - 20	$V_{B\ 1,2,3}$ + 0.3	
VDC	DCbus Supply Voltage	-0.3	620	
GF	Input voltage for Ground Fault detection	VDC-20	VDC+0.3	
VSDC	High voltage return for Ground Fault circuit	VDC-20	VDC+0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20†	
COM	Power ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage LO1,2,3, PFCout	-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN1,2,3, HIN1,2,3, ITRIP, PFCtrip, FLTEN, RCIN	-0.3	V_{CC} + 0.3	
$V_{PFCtrip}/V_{BRtrip}$	Input voltage $V_{PFCtrip}/V_{BRtrip}$	-2	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C	—	4.6	W
R_{THJA}	Thermal resistance, junction to ambient	—	27	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

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Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC}-COM) = (V_B-V_S) = 15 V. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{HO\ 1,2,3}$	High side output voltage HO1,2,3	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{S\ 1,2,3}$	High side floating supply voltage †	Vss – 8	600	
$V_{St\ 1,2,3}$	Transient high side floating supply voltage ††	-50	600	
VDC	DCbus Supply Voltage	(TBD)	600	
GF	Input voltage for Ground Fault detection	VDC-5	VDC	
VSDC	High voltage return for Ground Fault circuit	VDC-12	VDC-11	
V_{CC}	Low side supply voltage	10	20	
$V_{LO1,2,3}$	Low side output voltage LO1,2,3, PFCout	0	V_{CC}	
COM	Power ground	-5	5	
V_{SCOM}	Negative transient Vs voltage	0	-20[1)]	
V_{FLT}	FAULT output voltage	0	V_{CC}	
V_{RCIN}	RCIN input voltage	0	V_{CC}	
$V_{HO\ 1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	COM	V_{CC}	
V_{ITRIP}	ITRIP input voltage	0	5	
PFC_{ITRIP} /BR_{ITRIP}	PFC_{ITRIP}/BR_{ITRIP} input voltage	-2	0	
V_{IN}	Logic input voltage LIN, HIN, PFCin, BRin, EN	V_{SS}	V_{SS} +5	
T_A	Ambient temperature	-40	125	ºC

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to –V_{BS}. Please refer to Design Tip DT97-3 for more details.

†† Operational for transient negative V_S of V_{SS} - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

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Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. TA = 25°C unless otherwise specified. The VIN and IIN parameters are referenced to V_{SS} and are applicable to all six channels. The VO and IO parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S. The PFCIo/BRIo and VPFC/ VBR are referenced to V_{SS} and are applicable to PFCout/BRout lead.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VIH	Logic "1" input voltage	2.5	—	—	V	
VIL	Logic "0" input voltage	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	2.5		
$V_{IN,TH-}$	Input negative going threshold	0.8	1	—		
$V_{IT,TH+}$	Input positive going threshold	0.160	0.200	0.240		
$V_{IT,TH-}$	Input negative going threshold	0.144	0.180	0.216		
$V_{IT,HYS}$	ITRIP hysteresis	—	20	—	mV	
$V_{PFCT,TH+}$ $V_{BRT,TH+}$	PFC/BR positive going threshold	-0.144	-0.180	-0.216	V	
$V_{PFCT,TH-}$ $V_{BRT,TH-}$	PFC/BR negative going threshold	-0.160	-0.200	-0.240		
$V_{PFCT,HYS}$ $V_{BRT,HYS}$	PFC/BR hysteresis	—	20	—	mV	
$V_{GFT,TH+}$	GF positive going threshold	0.140	0.180	0.220	V	$V_{GFT} = V_{DC} - V_{GF}$
$V_{GFT,TH-}$	GF negative going threshold	0.150	0.200	0.240		
$V_{GFT,HYS}$	GF hysteresis	—	20	—	mV	
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—	V	
$V_{RCIN,HYS}$	RCIN hysteresis	—	3	—		
$V_{CC,UVTH+}$	V_{CC} supply undervoltage positive going threshold	10.2	11.1	12.0		
$V_{CC,UVTH-}$	V_{CC} supply undervoltage negative going threshold	10.0	10.9	11.8		
$V_{CC,UVHYS}$	V_{CC} supply undervoltage hysteresis	—	0.2	—		
$V_{BS,UVTH+}$	V_{BS} supply undervoltage positive going threshold	10.2	11.1	12.0		
$V_{BS,\ UVTH-}$	V_{BS} supply undervoltage negative going threshold	10.0	10.9	11.8		
$V_{BS,UVHS}$	V_{BS} supply undervoltage hysteresis	—	0.2	—		
ILK	Offset supply leakage current	—	—	50	µA	VB1,2,3 = VDC = GF =600 V, VDC - VDCS = 20 V
Iqbs	Quiescent VBS supply current	—	45	120		All input/output in off status
Iqcc	Quiescent VCC supply current	—	2.5	4	mA	All input/output in off status
Io+	Output high short circuit pulsed current, HO1,2,3	100	200	—		Vout = 0 V, PW </= 10 us
Io-	Output low short circuit pulsed current, HO1,2,3	190	350	—	mA	Vout = 15 V, PW </= 10 us
VOH	High level output voltage, VBIAS – VO, HO1,2,3	—	0.9	1.4	V	IO = 20 mA
VOL	Low level output voltage, VO, HO1,2,3	—	0.4	0.6		

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Static Electrical Characteristics (continued)

(V_{CC}-COM) = (V_B-V_S) = 15 V. TA = 25°C unless otherwise specified. The VIN and IIN parameters are referenced to V_{SS} and are applicable to all six channels. The VO and IO parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S. The PFCIo/BRIo and VPFC/ VBR are referenced to V_{SS} and are applicable to PFCout/BRout lead.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$PFCI_{O+}$/ BRI_{O+}	Output high short circuit pulsed current, PFC_{OUT} /BR_{OUT}	120	250	—	mA	P_{FCOUT} = 0 V, PW </= 10 us
$PFCI_{O-}$/ BRI_{O-}	Output low short circuit pulsed current, PFC_{OUT}/BR_{OUT}	210	430	—		P_{FCOUT} = 15 V, PW </= 10 us
V_{PFCH} /V_{BRH}	High level output voltage, V_{BIAS} – V_O, PFC_{OUT}/BR_{OUT}	—	900	1400	mV	I_O = 20 mA
V_{PFCL} /V_{BRL}	low level output voltage, V_O, PFC_{OUT}/BR_{OUT}	—	400	600		
I_{IN+}	Input bias current LIN1,2,3, HIN1,2,3, PFC_{IN}/$BR_{IN,}$ (OUT=HI)	350	—	860	µA	V_{IN} = 3.3 V
I_{IN-}	Input bias current LIN1,2,3, HIN1,2,3, PFC_{IN}/$BR_{IN,}$ (OUT=LO)	—	0	1		V_{IN} = 0 V
I_{ITRIP+}	ITRIP input bias current	—	1	2		V_{ITRIP} = 1 V
I_{ITRIP-}	ITRIP input bias current	—	0	5		V_{ITRIP} = 0 V
$IPFC_{TRIP+}$/ IBR_{TRIP+}	PFC_{TRIP} /BR_{TRIP} input bias current	—	20	—		$V_{PFCTRIP}$ =-250 mV
$IPFC_{TRIP}$/ IBR_{TRIP-}	PFC_{TRIP} /BR_{TRIP} input bias current	—	0	5		$V_{PFCTRIP}$ = 0 V
I_{RCIN}	RCIN input bias current	—	0	5		V_{RCIN} = 15 V
IEN_{IN}	EN input bias current	—	0	1		V_{EN} = 3.3V
Ron_RCIN	RCIN low on resistance	—	50	100	Ω	I = 1.5 mA
R_{ON_FLT}	FLT low on resistance	—	50	100		I = 1.5 mA
RBS	Ron internal bootstrap diode	—	200	—		
IqVdcon	Quiescent VDC supply current on status	100	200	300	µA	VDC - Vgf = 250 mV, VDC+ = 40 -600 V
IqVdcoff	Quiescent VDC supply current off status	100	200	300		VDC = Vgf , VDC + = 40- 600 V

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Dynamic Electrical Characteristics

V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25°C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
LO_{ton} , HO_{ton}	Turn-on propagation delay, LO1,2,3, HO1,2,3	320	—	710	ns	LIN = 0 V ≥ **3.3 V**, HIN = 0 V
LO_{toff} , HO_{toff}	Turn-off propagation delay, LO1,2,3, HO1,2,3	320	—	710		LIN = **3.3 V** ≥ 0 V, HIN = 0 V
LO_{tr} , HO_{tr}	Turn-on rise time LO1,2,3, HO1,2,3	—	125	190		C_{LOAD} = 1nF
LO_{tf} ,HO_{tf}	Turn-off fall time LO1,2,3, HO1,2,3	—	50	75		C_{LOAD} = 1nF
P_{FCton}/B_{Rton}	Turn-on propagation delay, PFC_{OUT}/BR_{OUT} (CL = 2200pF)	300	—	660		P_{FCIN} = 0 V ≥ **3.3 V**
P_{FCtoff}/B_{Rtoff}	Turn-off propagation delay, PFC_{OUT}/BR_{OUT} (CL = 2200pF)	300	—	660		P_{FCIN} = **3.3 V** ≥ 0 V
P_{FCtr}/B_{Rtr}	Turn-on rise time, PFC_{OUT}/BR_{OUT} (CL= 2200 pF)	—	180	—		C_{LOAD} = 2.2 nF
P_{FCtf}/B_{Rtf}	Turn-off rise time, PFC_{OUT}/BR_{OUT} (CL = 2200 pF)	—	60	—		C_{LOAD} = 2.2 nF
t_{EN}	ENABLE low to output shutdown propagation delay	350	460	650		V_{IN}, V_{EN} = 0 V or **3.3 V**
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	800	—		V_{ITRIP} = **2 V**
$t_{ITRIPbl}$	ITRIP blanking time	250	400	600		V_{IN} = 0 V or **3.3 V** V_{ITRIP} = **2 V**
$t_{PFCtrip}$	PFC_{TRIP} to output shutdown propagation delay	—	800	—		
t_{PFCbl}/t_{BRbl}	PFC_{TRIP}/BR_{TRIP} blanking time	—	500	—		
t_{FILIN}	Input filter time † (HIN, LIN, PFC_{IN} /BR_{IN}, EN)	200	350	—		V_{IN} = 0 V & **3.3 V**
$t_{filterEn}$	Enable input filter time	100	200	—		
DT	Deadtime	190	290	420		LIN = **3.3 V** ≥ 0 V, HIN = 0 V ≥ **3.3 V**
MT	Ton, off matching time (on all six channels)	—	—	50		
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	—	60		
PM	Pulse width distortion ††	—	—	75		PW input = 10 us
t_{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	40	60	80	µs	R = 100 KΩ, C = 680 pF, on RCIN
$t_{ITRIPBLK}$	ITRIP blanking time	250	400	600	ns	
$t_{ITRIPFLT}$	ITRIP to fault time	800	1150	1500		V_{ITRIP} = 0 V ≥ **2 V** to FLT/En = **3.3 V** ≥ 0 V
$t_{ITRIPOUT}$	ITRIP to output shutdown propagation delay	500	720	950		V_{ITRIP} =0 V ≥ **2 V** to LOx/Hox = 15 V ≥ 0 V

† The minimum width of the input pulse is recommended to exceed 500 ns to ensure the filtering time of the input filter is exceeded.

†† PM is defined as PW_{IN} - PW_{OUT}.

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Dynamic Electrical Characteristics

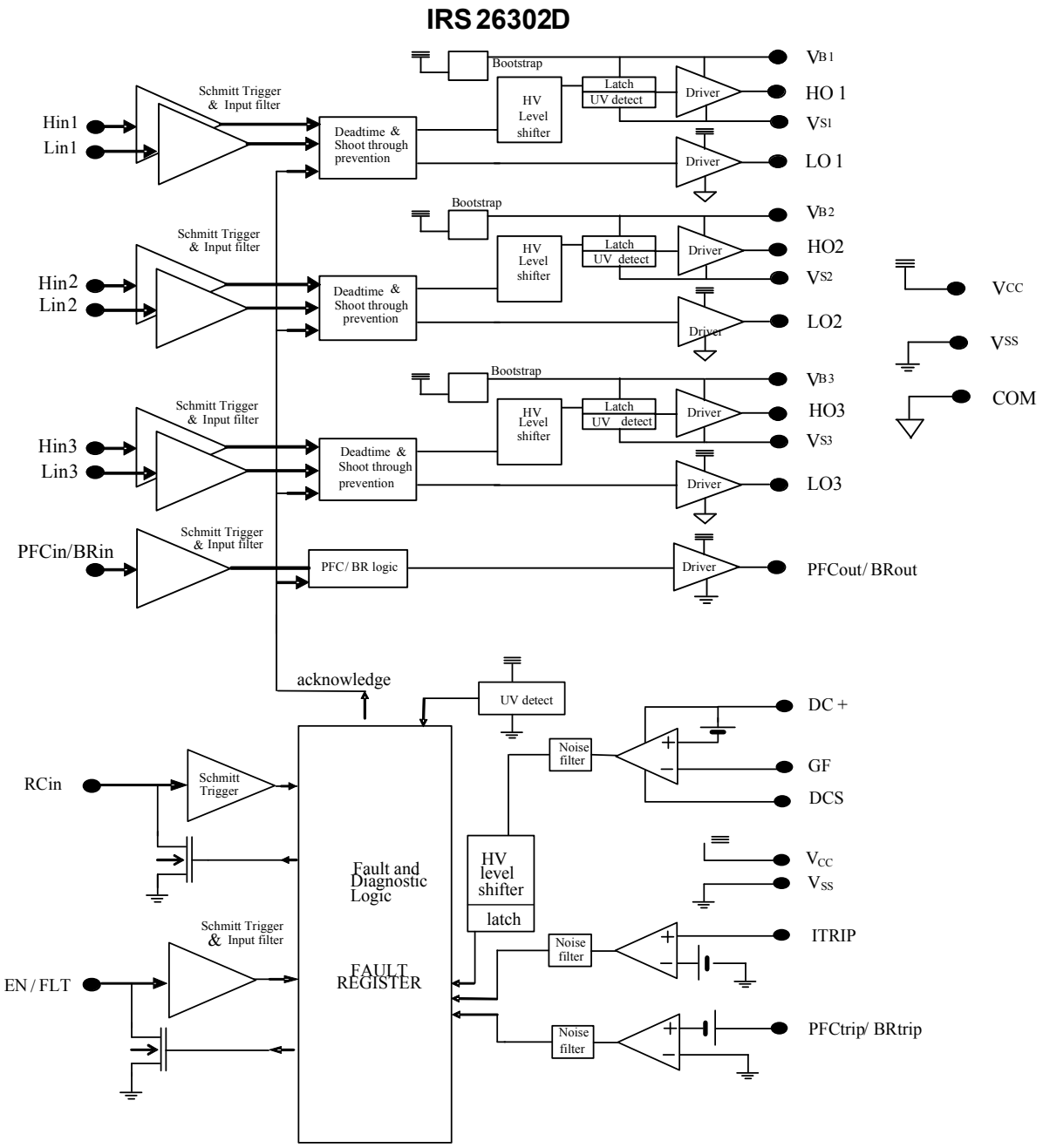
V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25 °C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{ITRIPPFC}/t_{ITRIPBR}$	ITRIP to PFCout/BRout shutdown propagation delay	400	620	850	ns	V_{ITRIP} = **-1 V** ≥ **2 V** to P_{FCOUT}/B_{ROUT} = 15 V ≥ 0 V
$t_{PFCTRIPFLT}$ /$t_{BRTRIPFLT}$	PFCTRIP/BRTRIP to fault time	700	1000	1500		$V_{PFCTRIP}/V_{BRTRIP}$ = **1V** ≥ -**1.5 V** V to FLT/En = **3.3 V** ≥ 0 V
$t_{PFCTRIPOUT}$ /$t_{BRTRIPOUT}$	PFCTRIP/BRTRIP to output shutdown propagation delay	400	600	950		$V_{PFCTRIP}/V_{BRTRIP}$ = **1V** ≥ -**1.5 V** to LOx/Hox = 15 V ≥ 0 V
$t_{PFCTRIPPFC}$ /$t_{BRTRIPPFC}$	PFCTRIP/BRTRIP to PFC output shutdown propagation delay	320	500	850		$V_{PFCTRIP}/V_{BRTRIP}$ = **1V** ≥ -**1.5 V** to P_{FCOUT} = 15 V ≥ 0 V
$t_{PFCTRIPBLK}$ /$t_{BRTRIPBLK}$	PFCTRIP/BRTRIP blanking time	150	450	750		
$t_{GFTRIPFLT}$	GFTRIP to fault time	1000	1400	1800		V_{GF} = V_{DC} ≥ **V_{DC} -1** V to FLT/En = 15 V ≥ 0 V
$t_{GFTRIPOUT}$	GFTRIP to output shutdown propagation delay	700	1000	1300		V_{GF} = V_{DC} ≥ **V_{DC} -1** V to LOx/Hox = 15 V ≥ 0 V
$t_{GFTRIPPFC}$	GFTRIP to PFC output shutdown propagation delay	600	900	1200		V_{GF} = V_{DC} ≥ **V_{DC} -1** V to P_{FCOUT} = 15 V ≥ 0 V
$t_{GFTRIPBLK}$	GFTRIP blanking time	150	300	550		
t_{ENOUT}	EN on to output propagation delay	300	400	500		V_{EN} = 0 V ≥ **3.3 V**, LINx/HINx = **3.3 V** to LOx/Hox = 0 V ≥ 15 V
t_{SDOUT}	EN off to output shutdown propagation delay	320	440	560		V_{EN} = **3.3 V** ≥ 0 V, LINx/HINx = **3.3 V** to LOx/Hox = 15 V ≥ 0 V
t_{ENPFC}/t_{ENBR}	EN on to PFC/Brake output propagation delay	200	320	500		V_{EN} = 0 V ≥ **3.3 V** , P_{FCIN}/B_{RIN} = **3.3 V** to P_{FCOUT}/B_{ROUT} = 0 V ≥ 15 V
t_{SDPFC}/t_{SDBR}	EN off to output shutdown PFC/Brake propagation delay	200	360	500		V_{EN} = **3.3 V** ≥ 0 V, P_{FCIN}/B_{RIN} = **3.3 V** to P_{FCOUT}/B_{ROUT} =15 V ≥ 0 V
$t_{HANDSHAKE}$	Input to Hand shake mode delay	300	500	700		See fault diagnostic state diagram
t_{DIAGIN}	Input to DIAG mode in delay					
$t_{DIAGOUT}$	Input to DIAG mode out delay					

Note 1: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 2: U_{VCC} is not latched, when V_{CC} > U_{VCC}, FAULT return to high impedance.
Note 3: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC} = 15 V)

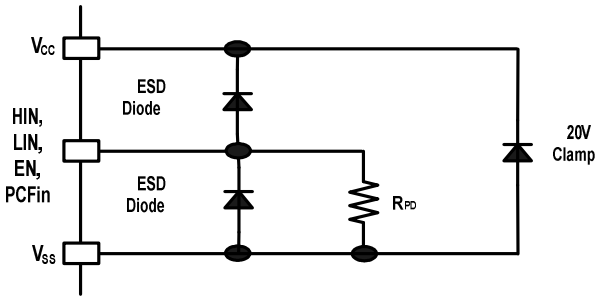
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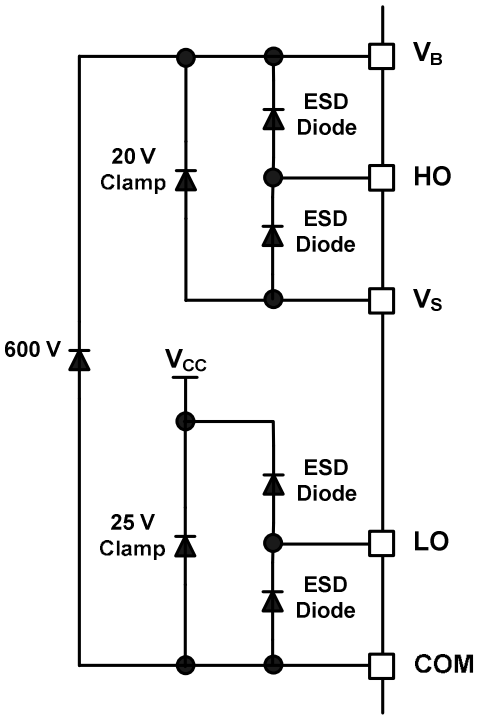
Functional Block Diagram

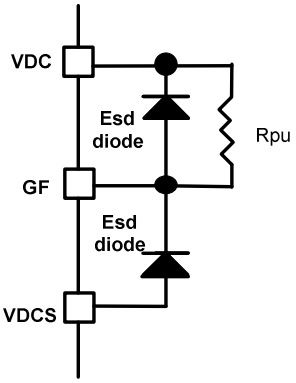


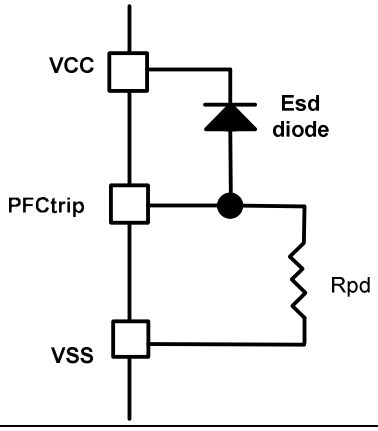
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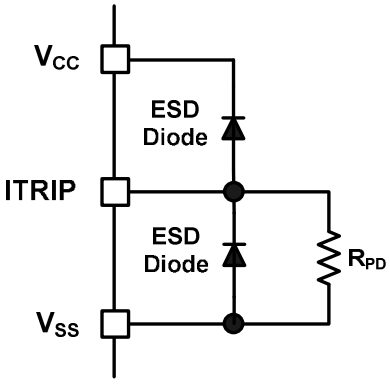
Input/Output Pin Equivalent Circuit Diagrams

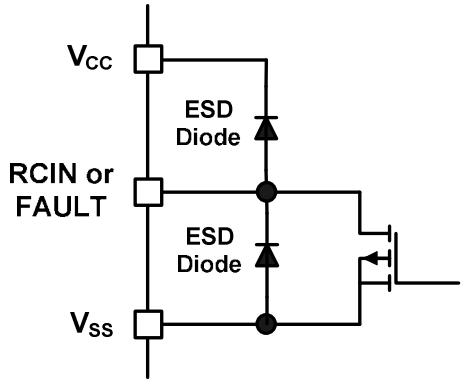












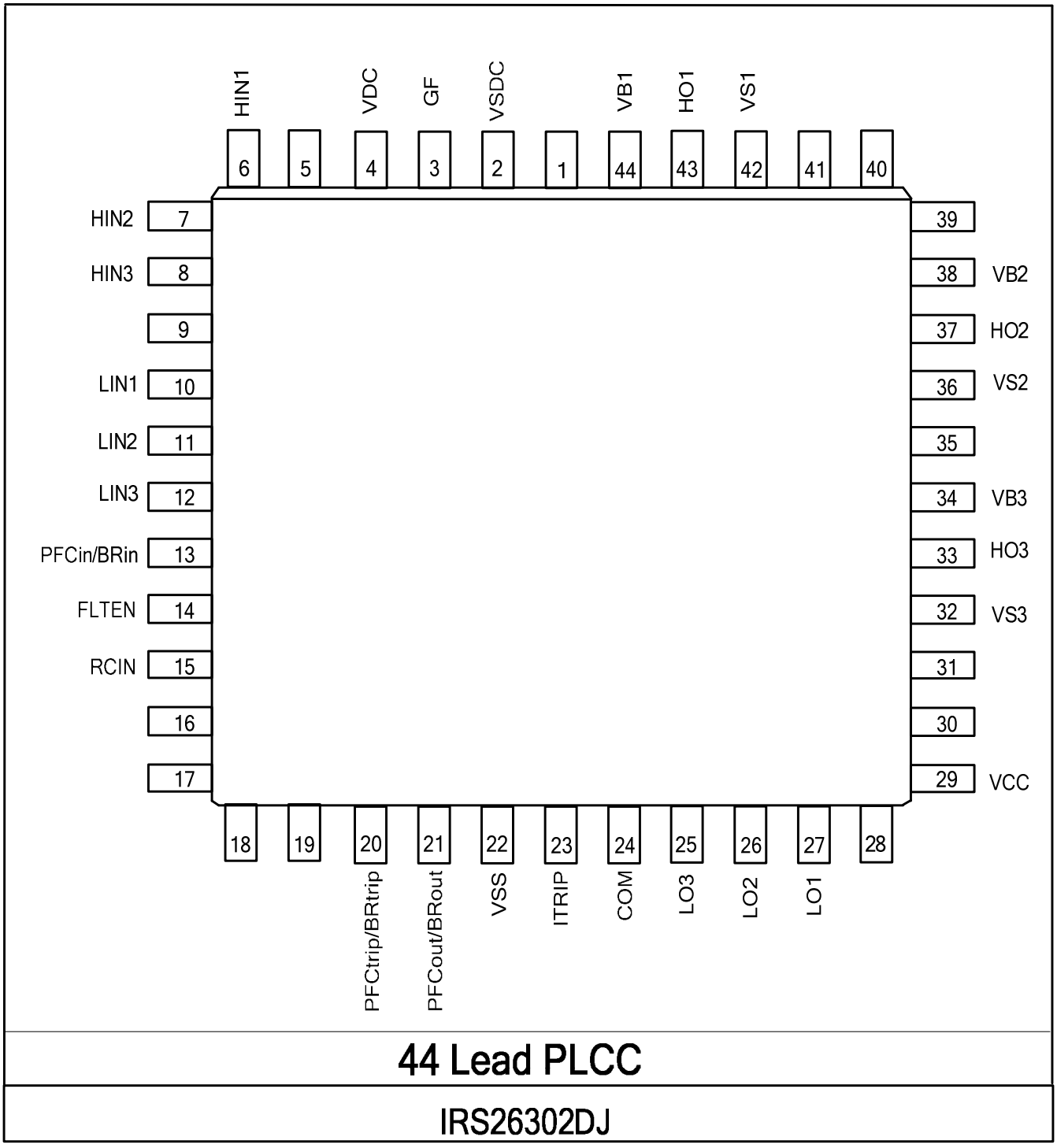
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Lead Definitions

Symbol	Description
V_{SDC}	GF supply return
GF	GF analog input for DC + overcurrent shutdown. When active, GF shuts down outputs and activates FAULT and RCIN low. When GF becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
V_{DC}	GF comparator supply (DC bus)
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), in phase
LIN1,2,3	Logic input for low side gate driver outputs (LO1,2,3), in phase
P_{FCTRIP}/B_{RTRIP}	Analog input for PCF overcurrent shutdown. When active, GF shuts down outputs and activates FAULT and RCIN low. When P_{FCTRIP}/B_{RTRIP} becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
P_{FCOUT}/B_{ROUT}	PFC/Brake output
P_{FCIN}/B_{RIN}	Input, PFC/Brake, active high
FAULT/EN	Open Drain and input, act high
ITRIP	Analog input for DC – over-current shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	An external RC network input used to define the FAULT CLEAR delay (t_{FLTCLR}) approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into an open-drain high-impedance state.
V_{SS}	Logic ground
COM	Power ground & Analog input (ITRIP)
LO1,2,3	Low side driver outputs
V_{CC}	Low side supply voltage
$V_{S1,2,3}$	High voltage floating supply return
HO1,2,3	High side driver outputs
$V_{B1,2,3}$	High side floating supply

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Lead Assignments



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Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Over-Temperature Shutdown Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Diagnostics
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Bootstrap Power Supply Design
- Separate Logic and Power Grounds
- Tolerant to Negative V_S Transients
- PCB Layout Tips
- Integrated Bootstrap FET limitation
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS26302DJ HVICs are designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

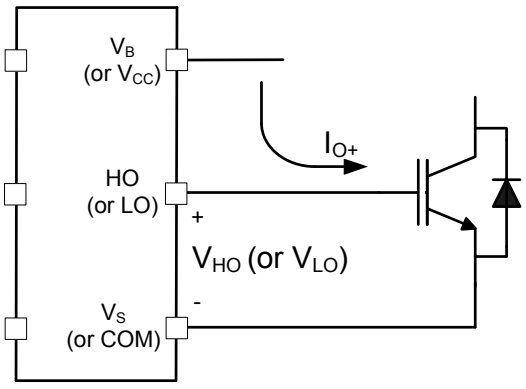


Figure 1: HVIC sourcing current

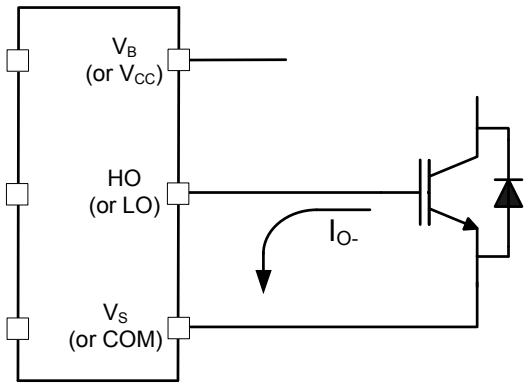


Figure 2: HVIC sinking current

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Switching and Timing Relationships

The relationship between the input and output signals of the IRS26302DJ are illustrated below in Figures 3. From this figure, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

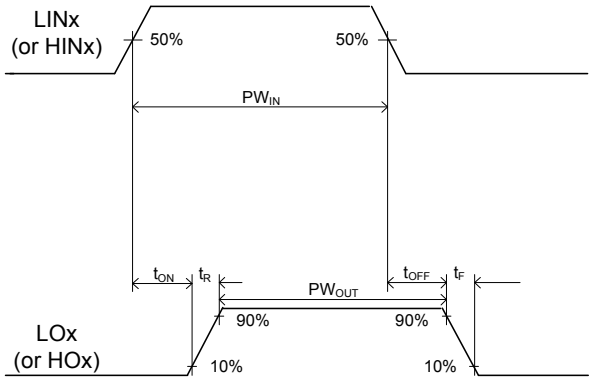


Figure 3: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the IRS26302DJ; this functionality is described in further detail later in this document.

During interval A of Figure 5, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 5 and 6 shows that the signal on the ITRIP, GF, PCFtrip input pin has gone from a not active to an active state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low), the voltage on the RCIN pin has been pulled to 0 V, and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP, GF, PCFtrip input has returned to the not active state, the output will remain disabled and the fault condition reported until the voltage on the RCIN pin charges up to $V_{RCIN,TH}$ (see interval C in Figure 6); the charging characteristics are dictated by the RC network attached to the RCIN pin.

During intervals D and E of Figure 5, we can see that the enable (EN) pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); this results in the outputs (HOx and LOx) being held in the low state until the enable pin is pulled high.

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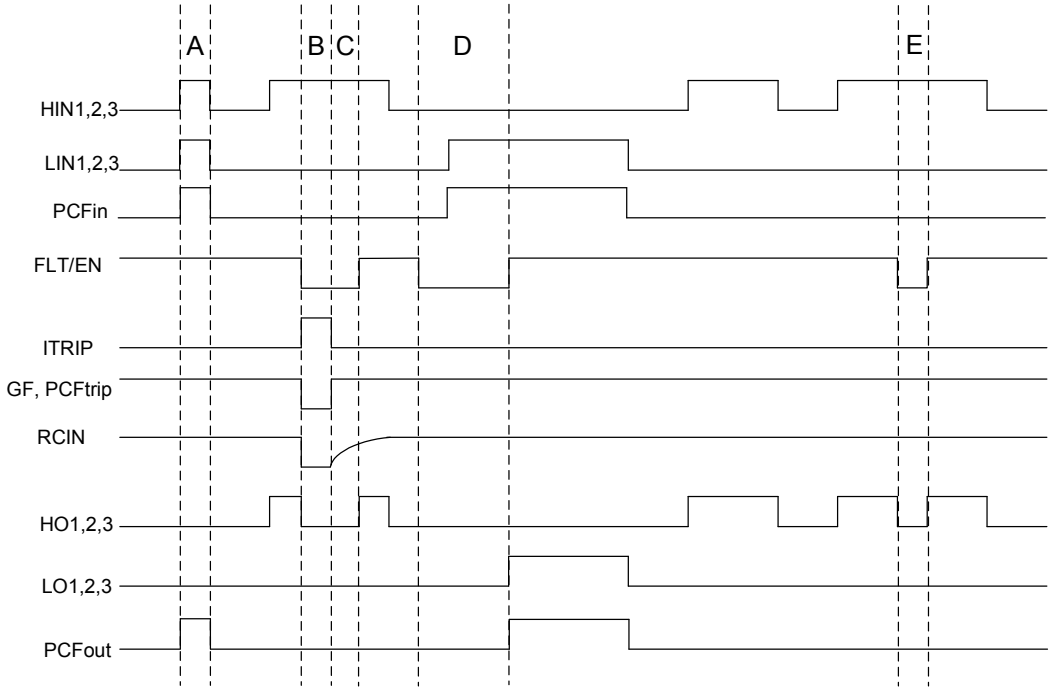


Figure 4: Input/output timing diagram

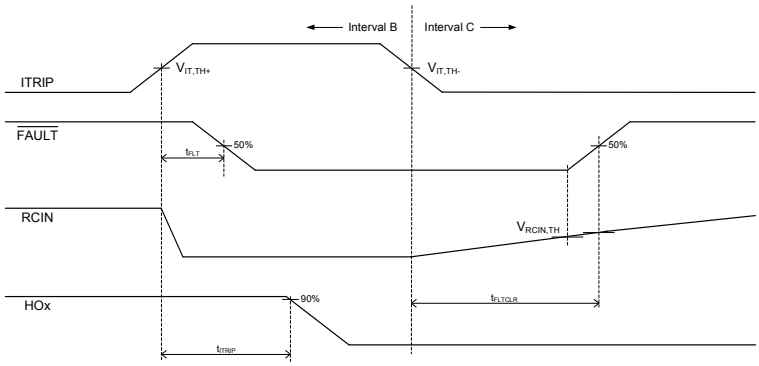


Figure 5: Detailed view of B & C intervals

Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 7 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the IRS26302DJ is matched with respect to the high- and low-side outputs of a given channel; additionally, the deadtimes of each of the three channels are matched. Figure 7 defines the two deadtime parameters (i.e., DT_1 and DT_2) of a specific channel; the deadtime matching parameter (MDT) associated with the IRS26302DJ specifies the maximum difference between DT_1 and DT_2. The MDT parameter also applies when comparing the DT of one channel of the IRS26302DJ to that of another.

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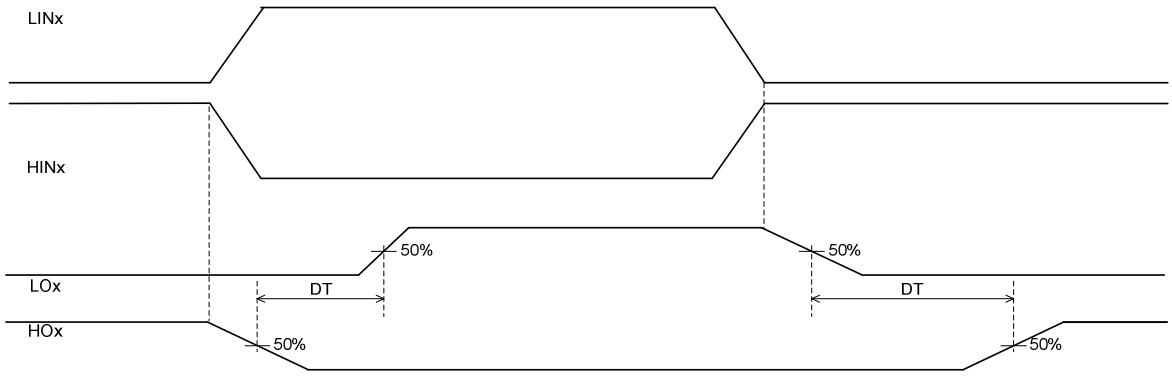


Figure 7: Illustration of deadtime

Matched Propagation Delays

The IRS26302DJ is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). Additionally, the propagation delay for each low-side channel is matched when compared to the other low-side channels and the propagation delays of the high-side channels are matched with each other; the MT specification applies as well. The propagation turn-on delay (t_{ON}) of the IRS26302DJ is matched to the propagation turn-on delay (t_{OFF}).

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS26302DJ has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 8 illustrates an input signal to the IRS26302DJ, its input threshold values, and the logic state of the IC as a result of the input signal.

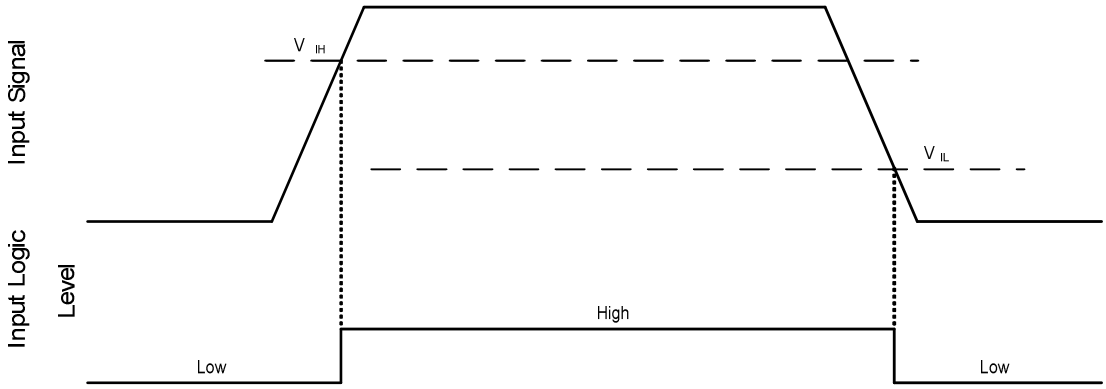


Figure 8: HIN & LIN input thresholds

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Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 9 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

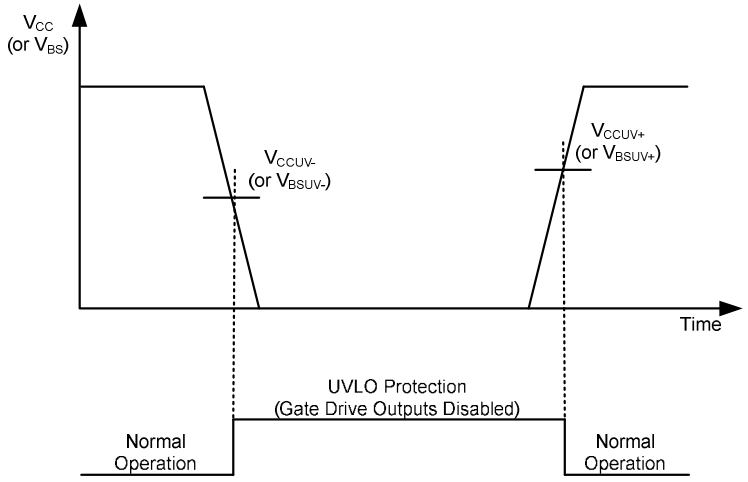


Figure 9: UVLO protection

Shoot-Through Protection

The IRS26302DJ is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 10 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table. Note that the IRS26302DJ has non-inverting inputs (the output is in-phase with its respective input).

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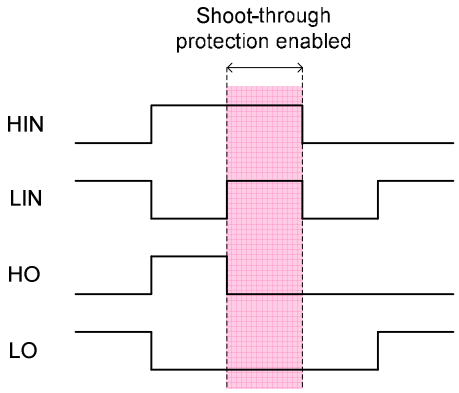


Figure 10: Illustration of shoot-through protection circuitry

HIN	LIN	HO	LO
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Table 1: Input/output truth table

Enable Input

The IRS26302DJ is equipped with an enable input pin that is used to shutdown or enable the HVIC. When the EN pin is in the high state the HVIC is able to operate normally (assuming no other fault conditions). When a condition occurs that should shutdown the HVIC, the EN pin should see a low logic state. The enable circuitry of the IRS26302DJ features an input filter; the minimum input duration is specified by $t_{FILTER,EN}$. Please refer to the EN pin parameters $V_{EN,TH+}$, $V_{EN,TH-}$, and I_{EN} for the details of its use. Table 2 gives a summary of this pin's functionality and Figure 11 illustrates the outputs' response to a shutdown command.

Enable Input	
Enable input high	Outputs enabled*
Enable input low	Outputs disabled

Table 2: Enable functionality truth table
(*assumes no other fault condition)

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Figure 11: Output enable/disable timing waveform

Fault Reporting and Programmable Fault Clear Timer

The IRS26302DJ provides an integrated fault reporting output and an adjustable fault clear timer. There are several situations that would cause the HVIC to report a fault via the FAULT pin: an undervoltage condition of V_{CC} or ITRIP, Ground Fault (GF), PCFtrip pin recognizes an overcurrent. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to V_{CC}.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RCIN} and C_{RCIN}. In Figure 12 where we see that a fault condition has occurred (ITRIP), RCIN and FAULT are pulled to V_{SS}, and once the fault has been removed, the fault clear timer begins. Figure 13 shows that R_{RCIN} is connected between the V_{CC} and the RCIN pin, while C_{RCIN} is placed between the RCIN and V_{SS} pins.

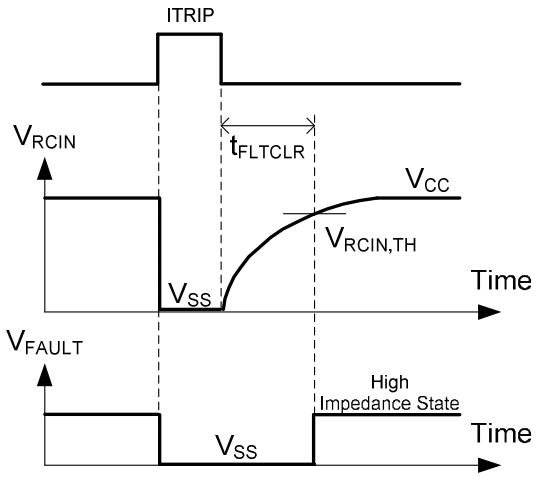


Figure 12: RCIN and FAULT pin waveforms

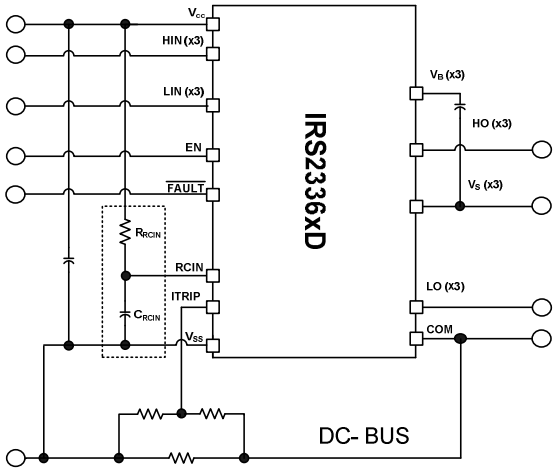


Figure 13: Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

C_{RCIN}	≤1 nF, ceramic
R_{RCIN}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 3: Design guidelines

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The length of the fault clear time period can be determined by using the formula below.

$$v_C(t) = V_f(1-e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RCIN}C_{RCIN})\ln(1-V_{RCIN,TH}/V_{CC})$$

Over-Current Protections

The IRS26302DJ HVICs are equipped with an ITRIP, GF and PFCtrip input pin. These functionality can be used to detect over-current events in the DC- bus, in the DC+ bus, in the PFC section and Ground related. Once the HVIC detects an over-current event, the outputs are shutdown, a fault is reported through the FAULT pin, and RCIN is pulled to V_{SS}.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 14, and the ITRIP threshold ($V_{IT,TH+}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold ($V_{IT,TH+}$) at that current level.

$$V_{IT,TH+} = R_0 I_{DC-}(R_1/(R_1+R_2))$$

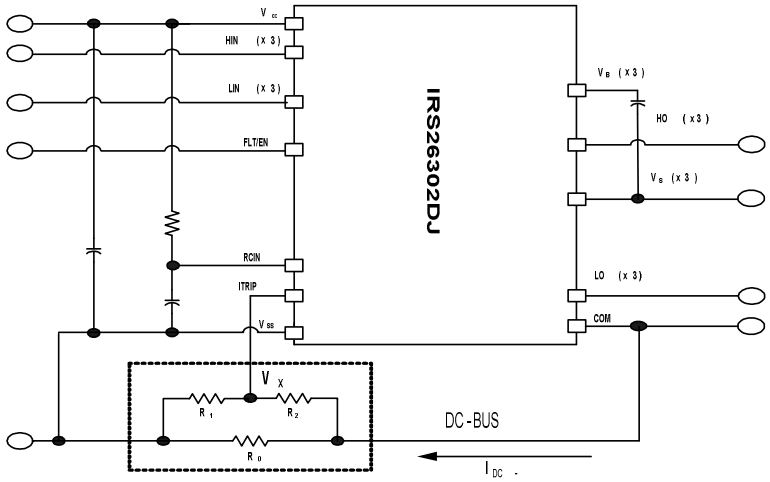


Figure 14: Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

The shunt resistor or resistor network for GF or PCFtrip can be determined according to GF, PCFtrip threshold and level of protection current. The GF pin should not be outside this range (VDC+0.3V, VDC-5V) and PCFtrip should not be outside (Vcc+0.3V, Vss-5V); if necessary, an external voltage clamp may be used.

Over-Temperature Shutdown Protection

The ITRIP input of the IRS26302DJ can also be used to detect over-temperature events in the system and initiate a shutdown of the HVIC (and power switches) at that time. In order to use this functionality, the circuit designer will need to design the resistor network as shown in Figure 15 and select the maximum allowable temperature.

This network consists of a thermistor and two standard resistors R_3 and R_4. As the temperature changes, the resistance of the thermistor will change; this will result in a change of voltage at node V_X. The resistor values should

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be selected such the voltage V_X should reach the threshold voltage ($V_{IT,TH+}$) of the ITRIP functionality by the time that the maximum allowable temperature is reached. The voltage of the ITRIP pin should not be allowed to exceed 5 V.

When using both the over-current protection and over-temperature protection with the ITRIP input, OR-ing diodes (e.g., DL4148) can be used. This network is shown in Figure 16; the OR-ing diodes have been labeled D_1 and D_2.

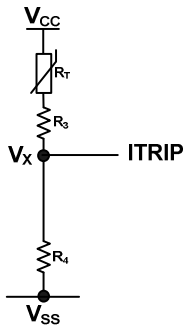


Figure 15: Programming over-temperature protection

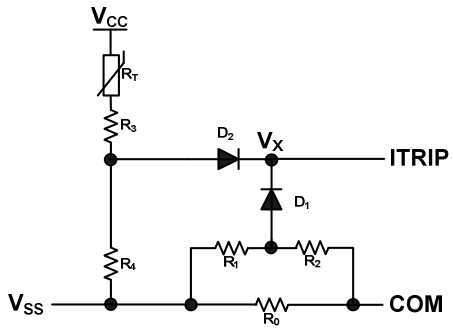


Figure 16: Using over-current protection and over-temperature protection

Truth Table: Undervoltage lockout, ITRIP, GF, PCFtrip and ENABLE

Table 4 provides the truth table for the IRS26302DJ. The first line shows that the UVLO for V_{CC} has been tripped; the FAULT output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns to the high impedance state.

The second case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive outputs have been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled and a fault has been reported through the fault pin. Same behavior if GF or PCFtrip threshold has been reached. In the last case, the HVIC has received a command through the EN input to shutdown; as a result, the gate drive outputs have been disabled.

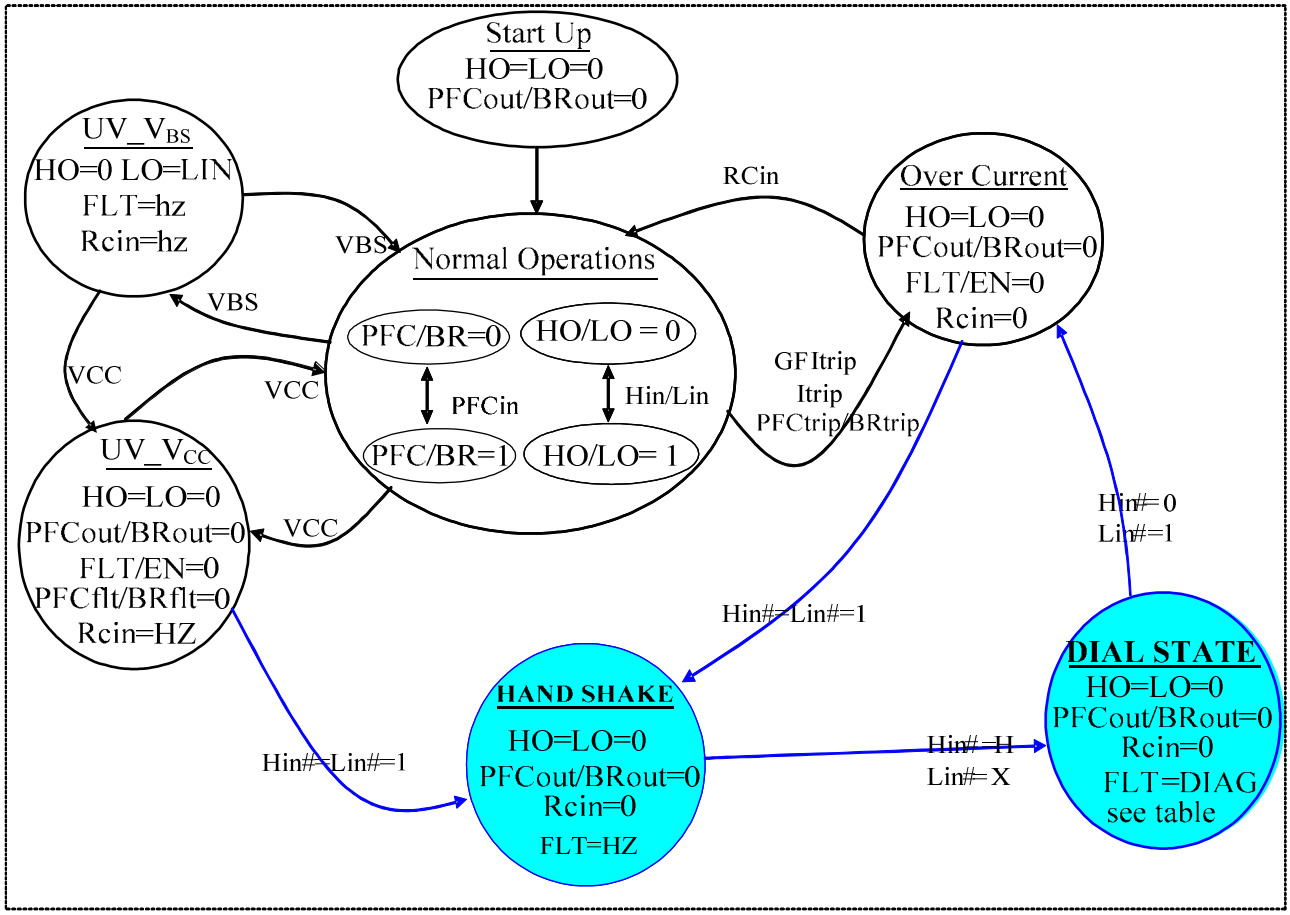
	VCC	VBS	ITRIP	GF	PFC trip	EN	RCIN	FAULT	LO	HO	PCFout
UVLO V_{CC}	$<V_{CCUV}$	---	---	---	---	---	High	0	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	0 V	0 V	5 V	High	High Z	LIN	0	0
Normal operation	15 V	15 V	0 V	0 V	0 V	5 V	High	High Z	LIN	HIN	PCFIN
ITRIP fault	15 V	15 V	$>V_{ITRIP}$	0 V	0 V	5 V	Low	0	0	0	0
GF	15 V	15 V	0 V	< GFth	0 V	5 V	Low	0	0	0	0
PCFtrip	15 V	15 V	0 V	0 V	<PCF th	5 V	Low	0	0	0	0
EN	15 V	15 V	0 V	0 V	0 V	0 V	High	High Z	0	0	0

Table 4: IRS26302DJ UVLO, ITRIP, GF, PCFtrip, EN, RCIN, & FAULT truth table

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Fault Diagnostic: DIAG STATE –State Diagram

After each fault event a diagnostic feature, if enable, can communicate to the controller which fault happened in the system (UVcc, ITRIP, GF, PCFtrip). If diagnostic is enabled forcing all HIN and all LIN = High the HVIC enters in handshake mode, all the outputs remain off, the automatic fault clear function is disabled and FLT/EN is in HZ (refer to Figure 17 for more details). The HVIC fault register is now ready for queries. A procedure to interrogate the fault register is depicted in the fault query routine (Figure 18).



FLT/EN pin and DIAG mode operation for all fault condition

LIN1,2,3	HIN1,2,3	PFCin/BRin	Condition	RCIN	Itrip	PFCtrip	GF	VCC fault	EN/FLT	Lox	Hox	PFCout/BRout
Linx	Hinx	PFCinx/BRinx		HZ	0	0		V_{CC} > UV_{CC}	HZ			
ALL=H	ALL H	PFCinx/BRinx	(^{0})	HZ	Fault register = 1 (**)				0-> HZ (^{0})	0	0	0
Linx	Hinx	PFCinx/BRinx		0	V > Vth (**)	X	X	X	0	0	0	0
Lin1=L Lin2, 3=H	ALL H	PFCinx/BRinx	(*)	0	V > Vth (**)	X	X	X	0	0	0	0
Lin1=L Lin2, 3=H	ALL H	PFCinx/BRinx	(*)	0	0	X	X	X	HZ	0	0	0
Linx	Hinx	PFCinx/BRinx		0	X	V > Vth (**)	X	X	0	0	0	0
Lin2=L Lin1, 3=H	ALL H	PFCinx/BRinx	(*)	0	X	V > Vth (**)	X	X	0	0	0	0
Lin2=L Lin1, 3=H	ALL H	PFCinx/BRinx	(*)	0	X	0	X	X	HZ	0	0	0
Linx	Hinx	PFCinx/BRinx		0	X	X	V > Vth (**)	X	0	0	0	0
Lin3=L Lin1,2=H	ALL H	PFCinx/BRinx	(*)	0	X	X	V > Vth (**)	X	0	0	0	0
Lin3=L Lin1,2=H	ALL H	PFCinx/BRinx	(*)	0	X	X	0	X	HZ	0	0	0
Linx	Hinx	PFCinx/BRinx		HZ	X	X	X	V_{CC} < UV_{CC}	0	0	0	0
Lin1,2=L Lin3=H	ALL H	PFCinx/BRinx	(*)	0	X	X	X	V_{CC} < UV_{CC}	0	0	0	0
Lin1,2=L Lin3=H	ALL H	PFCinx/BRinx	(*)	0	X	X	X	V_{CC} > UV_{CC}	HZ	0	0	0

(^{0}) HAND SHAKE SYNC
(*) Operation available only in DIAL MODE.
(**) Internal Register fault
DIAG MODE available when FLT=0
Set DIAG MODE: Hinx=Linx=H
During DIAG MODE operation Lox=Hox=0 PFCout/BRout=0 RCIN=0
Reset DIAG MODE: hold Linx=H Hinx=L

Figure 17: State Diagram

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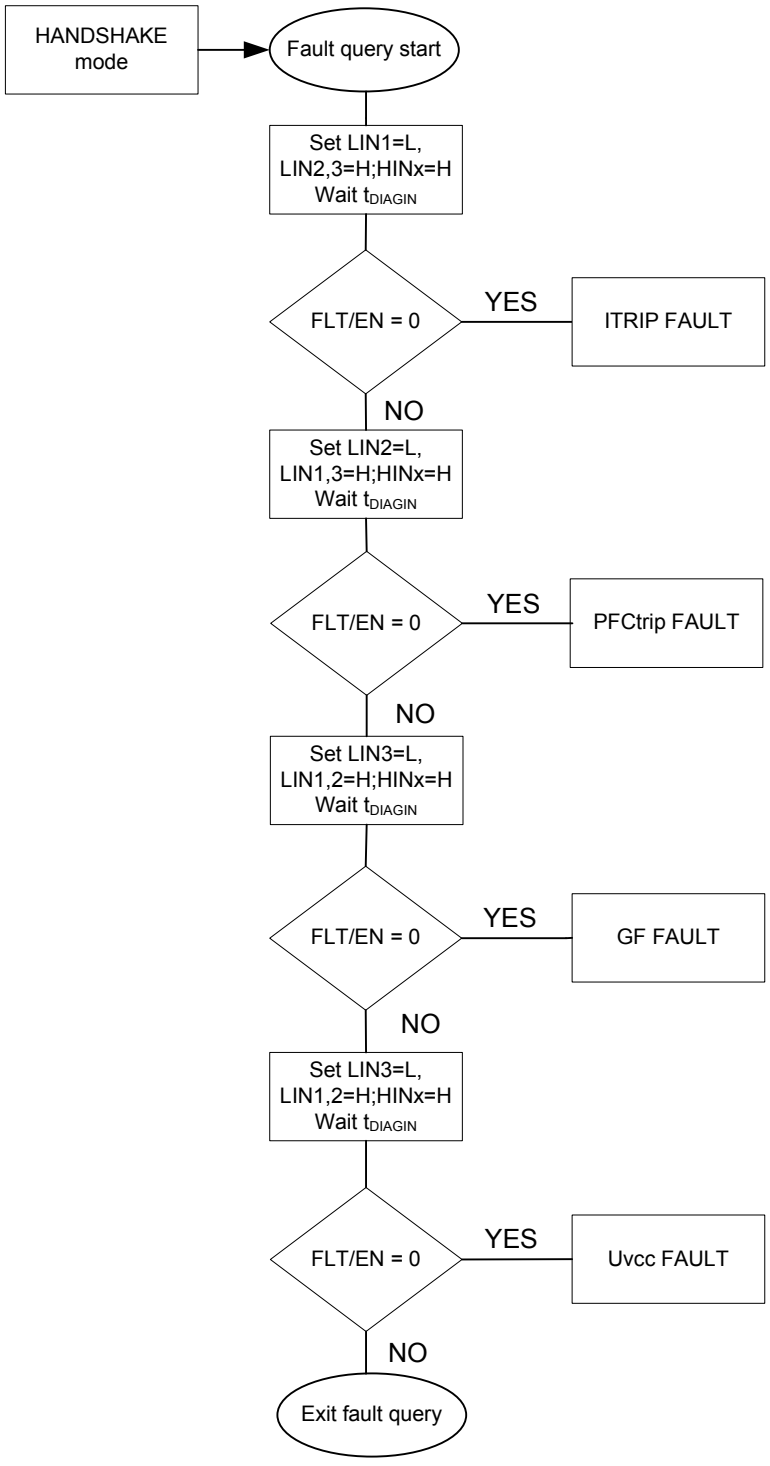


Figure 18: Fault Query Procedure

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Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN, LIN, PFCin and EN inputs. The working principle of the new filter is shown in Figures 19 and 20.

Figure 19 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 20 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

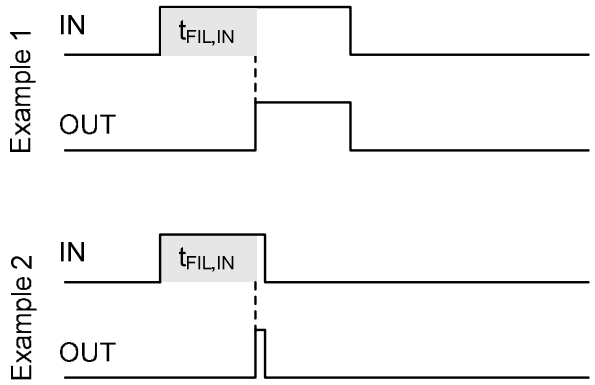


Figure 19: Typical input filter

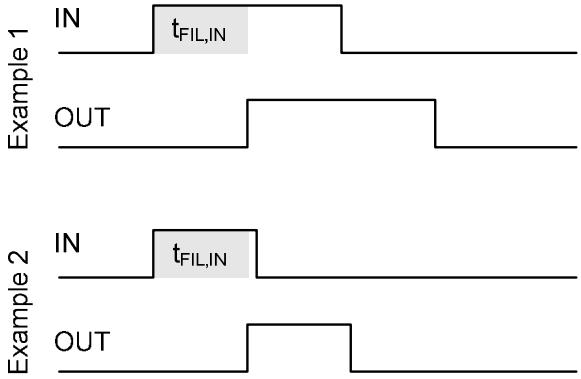


Figure 20: Advanced input filter

Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 21 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 21 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

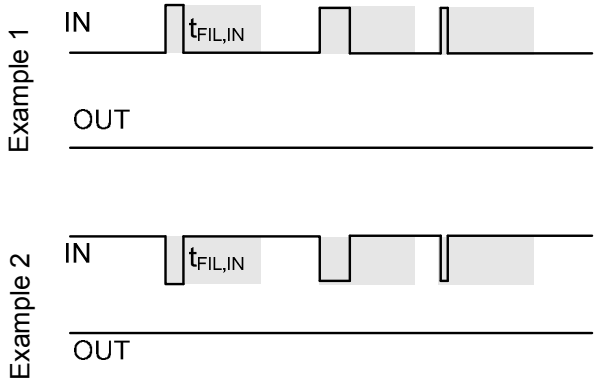


Figure 21: Noise rejecting input filters

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Figures 22 and 23 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 22; the left side illustrates the narrow pulse ON (short positive pulse) characteristic while the left shows the narrow pulse OFF (short negative pulse) characteristic. The x-axis of Figure 22 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT} duration. It can be seen that for a PW_{IN} duration less than $t_{FIL,IN}$, that the resulting PW_{OUT} duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the PW_{IN} duration exceed $t_{FIL,IN}$, that the PW_{OUT} durations mimic the PW_{IN} durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be ≥ 500 ns.

The difference between the PW_{OUT} and PW_{IN} signals of both the narrow ON and narrow OFF cases is shown in Figure 23; the careful reader will note the scale of the y-axis. The x-axis of Figure 21 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT}–PW_{IN} duration. This data illustrates the performance and near symmetry of this input filter.

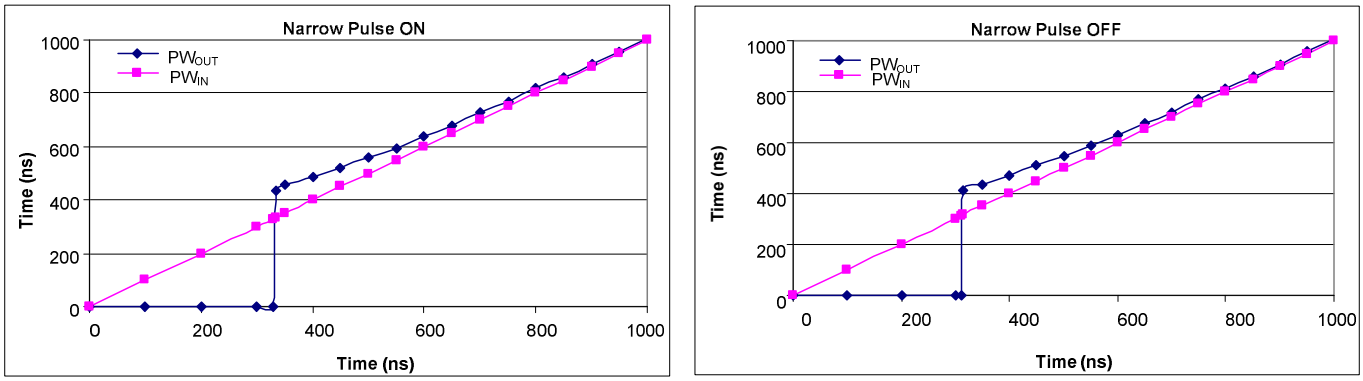


Figure 22: IRS2336xD input filter characteristic

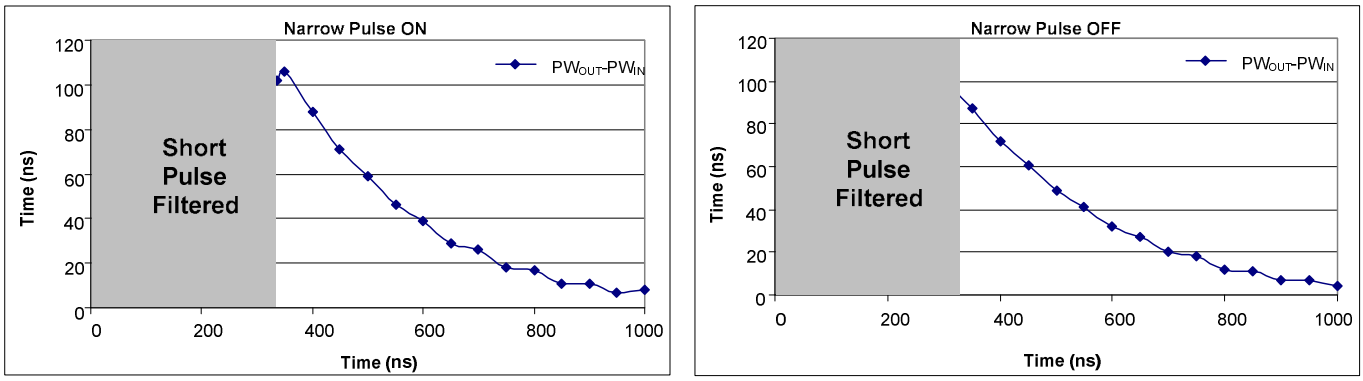


Figure 23: Difference between the input pulse and the output pulse

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Integrated Bootstrap Functionality

The IRS26302DJ features integrated high-voltage bootstrap MOSFETs that eliminate the need of the external bootstrap diodes and resistors in many applications.

There is one bootstrap MOSFET for each high-side output channel and it is connected between the V_{CC} supply and its respective floating supply (i.e., V_{B1}, V_{B2}, V_{B3}); see Figure 24 for an illustration of this internal connection.

The integrated bootstrap MOSFET is turned on only during the time when LO is 'high', and it has a limited source current due to R_{BS}. The V_{BS} voltage will be charged each cycle depending on the on-time of LO and the value of the C_{BS} capacitor, the drain-source (collector-emitter) drop of the external IGBT (or MOSFET), and the low-side free-wheeling diode drop.

The bootstrap MOSFET of each channel follows the state of the respective low-side output stage (i.e., the bootstrap MOSFET is ON when LO is high, it is OFF when LO is low), unless the V_B voltage is higher than approximately 110% of V_{CC}. In that case, the bootstrap MOSFET is designed to remain off until V_B returns below that threshold; this concept is illustrated in Figure 25.

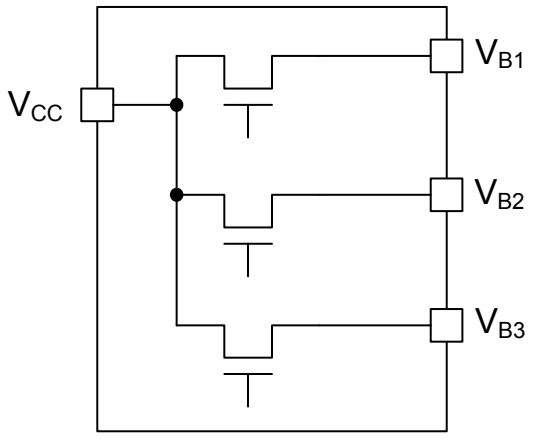


Figure 24: Internal bootstrap MOSFET connection

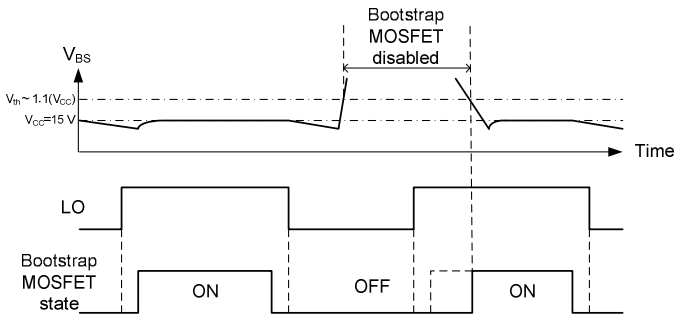


Figure 25: Bootstrap MOSFET state diagram

A bootstrap MOSFET is suitable for most of the PWM modulation schemes and can be used either in parallel with the external bootstrap network (i.e., diode and resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations. An example of this limitation may arise when this functionality is used in non-complementary PWM schemes (typically 6-step modulations) and at very high PWM duty cycle. In these cases, superior performances can be achieved by using an external bootstrap diode in parallel with the internal bootstrap network.

Bootstrap Power Supply Design

For information related to the design of the bootstrap power supply while using the integrated bootstrap functionality of the IRS26302DJ, please refer to Application Note 1123 (AN-1123) entitled "Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality." This application note is available at www.irf.com.

For information related to the design of a standard bootstrap power supply (i.e., using an external discrete diode) please refer to Design Tip 04-4 (DT04-4) entitled "Using Monolithic High Voltage Gate Drivers." This design tip is available at www.irf.com.

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Separate Logic and Power Grounds

The IRS26302DJ has separate logic and power ground pin (V_{SS} and COM respectively) to eliminate some of the noise problems that can occur in power conversion applications. Current sensing shunts are commonly used in many applications for power inverter protection (i.e., over-current protection), and in the case of motor drive applications, for motor current measurements. In these situations, it is often beneficial to separate the logic and power grounds.

Figure 26 shows a HVIC with separate V_{SS} and COM pins and how these two grounds are used in the system. The V_{SS} is used as the reference point for the logic and over-current circuitry; V_X in the figure is the voltage between the ITRIP pin and the V_{SS} pin. Alternatively, the COM pin is the reference point for the low-side gate drive circuitry. The output voltage used to drive the low-side gate is V_{LO}-COM; the gate-emitter voltage (V_{GE}) of the low-side switch is the output voltage of the driver minus the drop across $R_{G,LO}$.

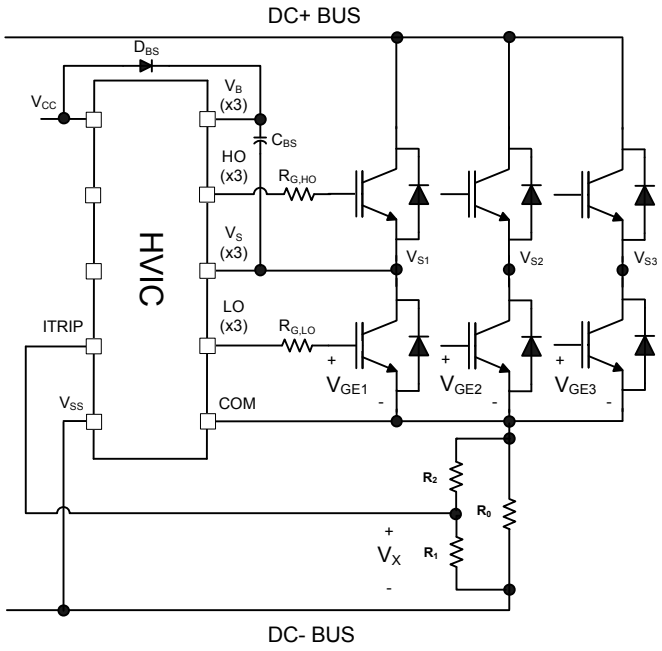


Figure 26: Separate V_{SS} and COM pins

Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 27; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 28 and 29) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

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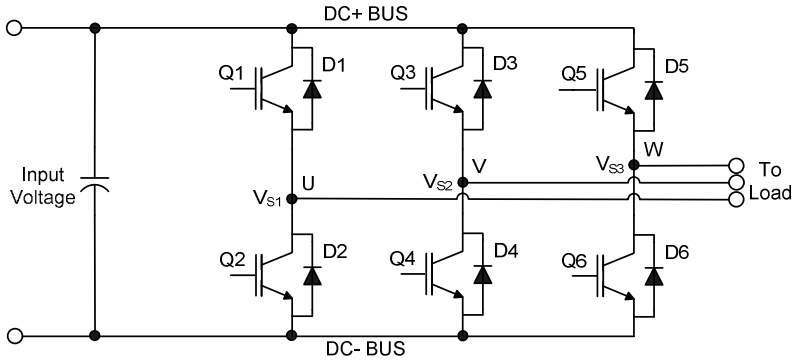


Figure 27: Three phase inverter

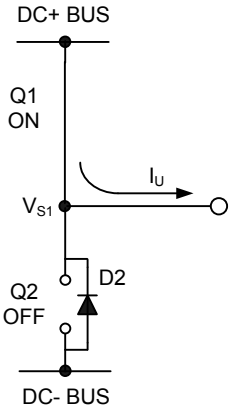


Figure 28: Q1 conducting

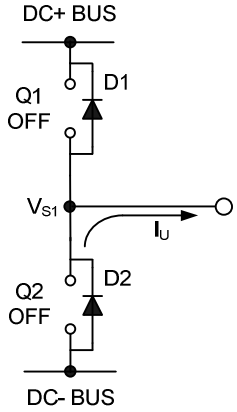


Figure 29: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 30 and 31), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

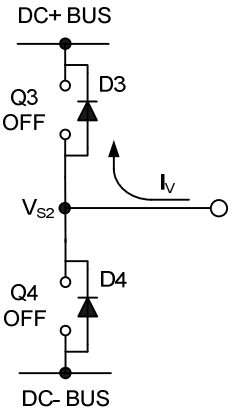


Figure 30: D3 conducting

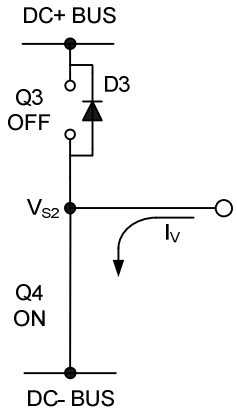


Figure 31: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”.

The circuit shown in Figure 32 depicts one leg of the three phase inverter; Figures 33 and 34 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on,

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V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

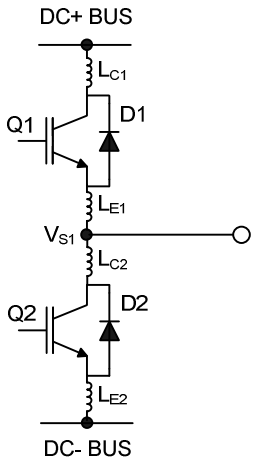


Figure 32: Parasitic Elements

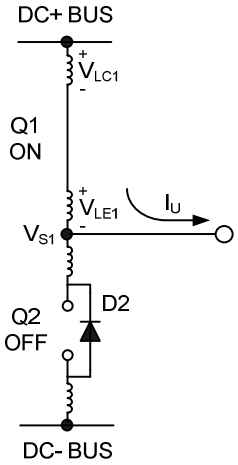


Figure 33: V_S positive

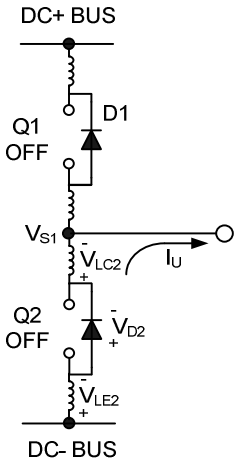


Figure 34: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. The IRS26302DJ has been seen to withstand large negative V_S transient conditions on the order of -50 V for a period of 50 ns. An illustration of the IRS26302DJ's performance can be seen in Figure 35. This experiment was conducted using various loads to create this condition; the curve shown in this figure illustrates the successful operation of the IRS26302DJ under these stressful conditions. In case of $-V_S$ transients greater then -20 V for a period of time greater than 100 ns; the HVIC is designed to hold the high-side outputs in the off state for 4.5 µs in order to ensure that the high- and low-side power switches are not on at the same time.

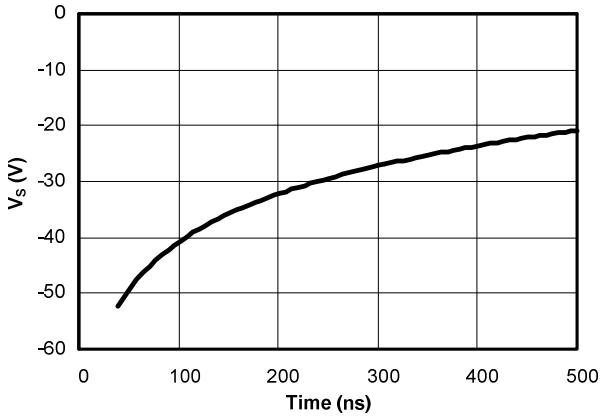


Figure 35: Negative V_S transient results for an International Rectifier HVIC

Even though the IRS26302DJ has been shown able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

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PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. The IRS26302DJ in the PLCC44 package has had some unused pins removed in order to maximize the distance between the high voltage and low voltage pins. Please see the Case Outline PLCC44 information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 36). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

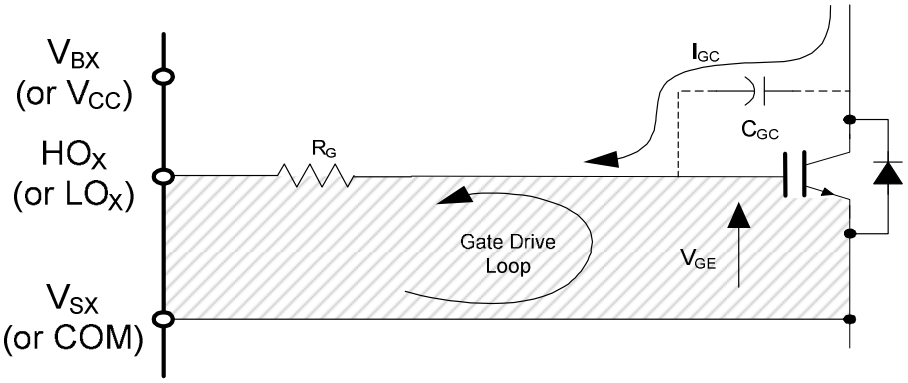


Figure 36: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and V_{SS} pins. This connection is shown in Figure 37. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

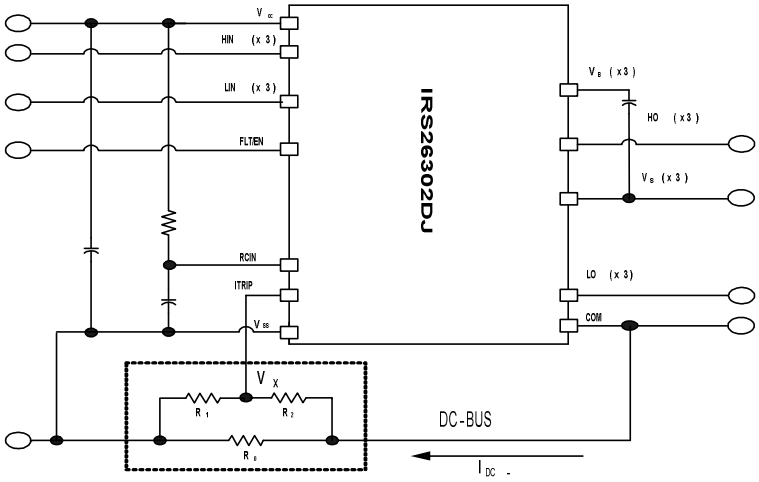


Figure 37: Supply capacitor

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Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 36), and in some cases using a clamping diode between V_{SS} and V_S (see Figure 39). See DT04-4 at www.irf.com for more detailed information.

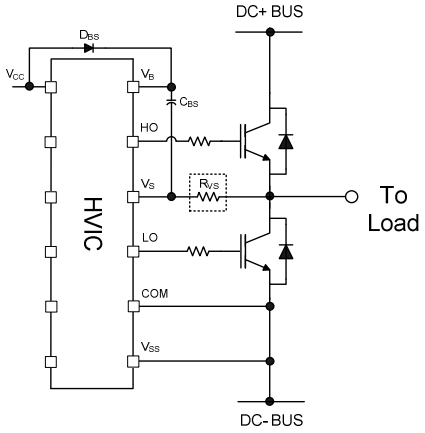


Figure 38: V_S resistor

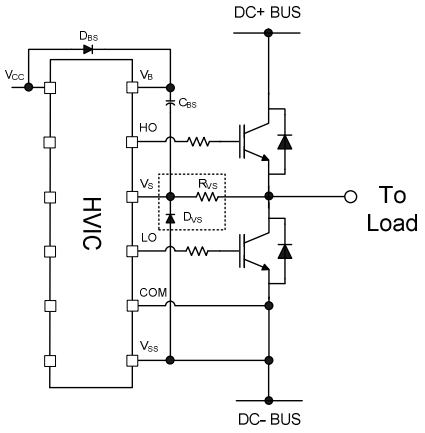


Figure 39: V_S clamping diode

Integrated Bootstrap FET limitation

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.40 below, resulting in power loss and possible damage to the HVIC.

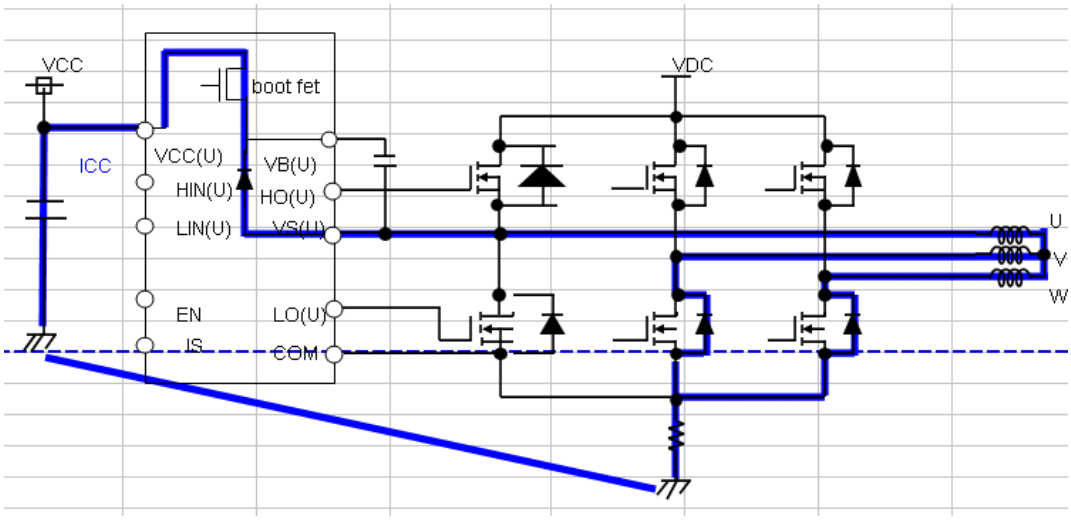


Figure 40: Current conduction path between VCC and VB pin

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Relevant Application Situations:

The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.
- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.41) prevents current conduction "out-of" VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.

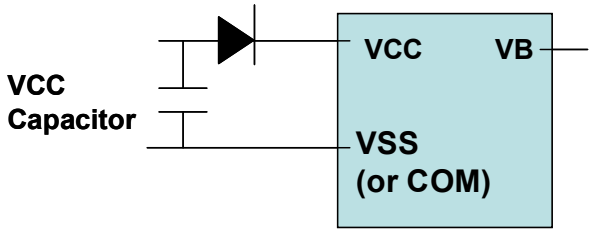


Figure 41: Diode insertion between VCC pin and VCC capacitor

Note that the forward voltage drop on the diode (V_F) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements. *VCC pin Bias = VCC Supply Voltage – V_F of Diode*.

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

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Parameter Temperature Trends

Figures 42-117 provide information on the experimental performance of the IRS26302DJ HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

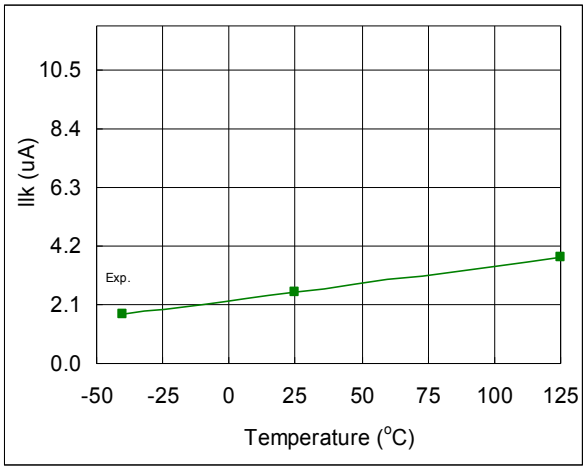


Fig. 42. Offset Supply Leakage Current vs. Temperature

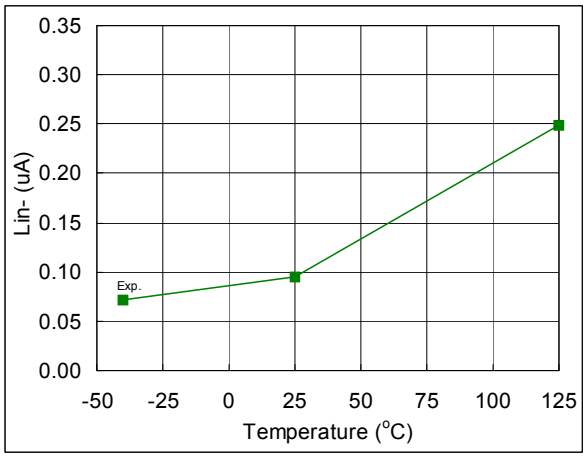


Fig. 43. Input Bias Current vs. Temperature

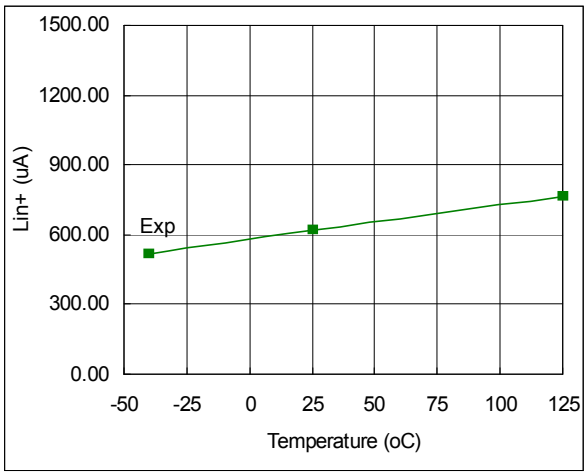


Fig. 44. Input Bias Current vs. Temperature

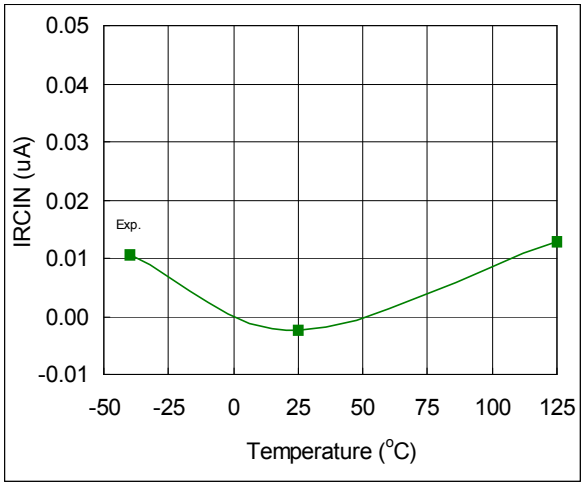


Fig. 45. RCIN Input Bias Current vs. Temperature

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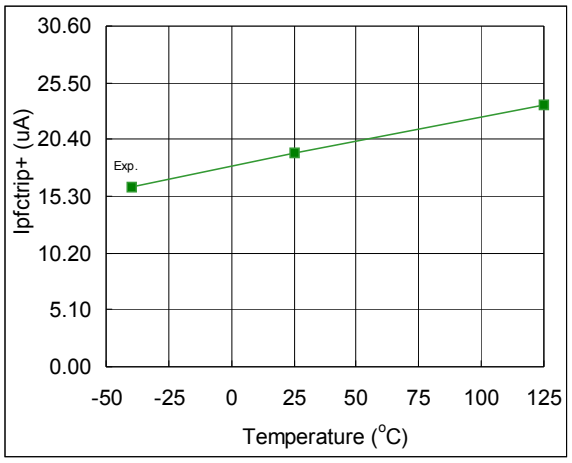


Fig. 46. PFC_{TRIP} Input Bias Current vs. Temperature

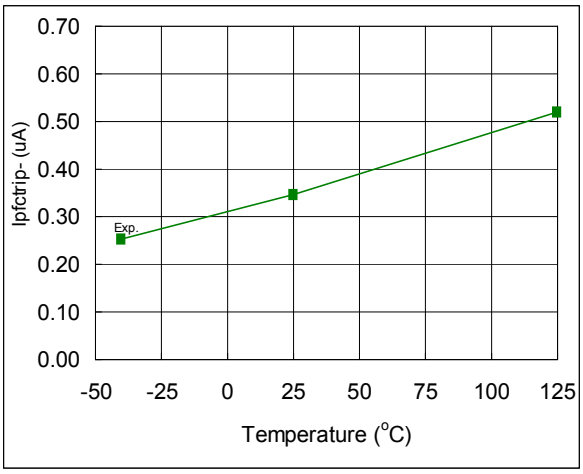


Fig. 47. PFC_{TRIP} Input Bias Current vs. Temperature

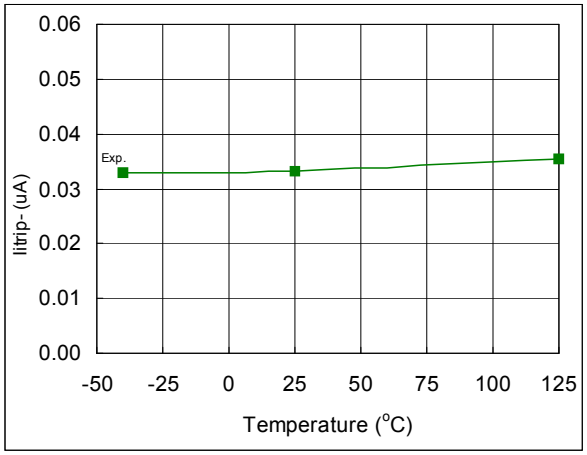


Fig. 48. ITRIP Input Bias Current vs. Temperature

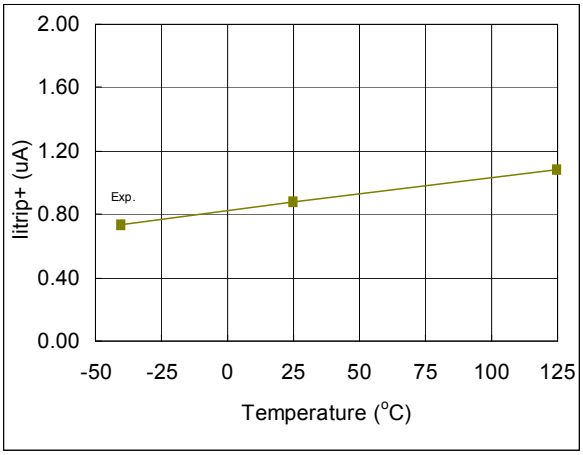


Fig. 49. ITRIP Input Bias Current vs. Temperature

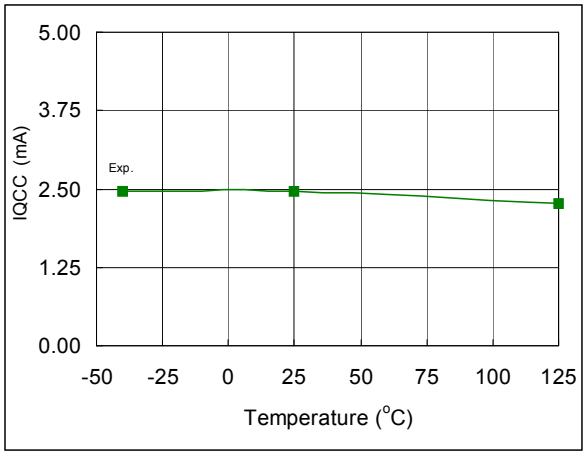


Fig. 50. Quiescent V_{CC} Supply Current vs. Temperature

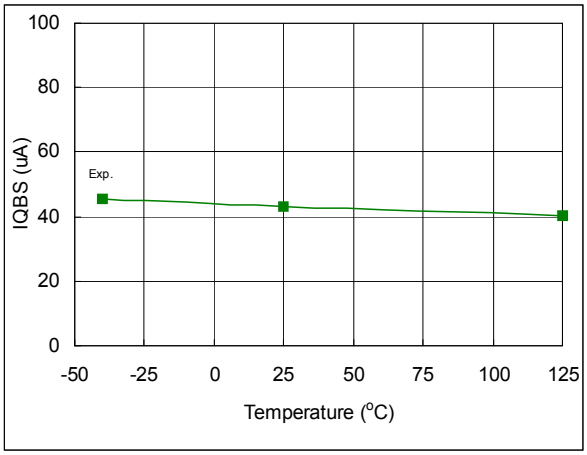


Fig. 51. Quiescent V_{BS} Supply Current vs. Temperature

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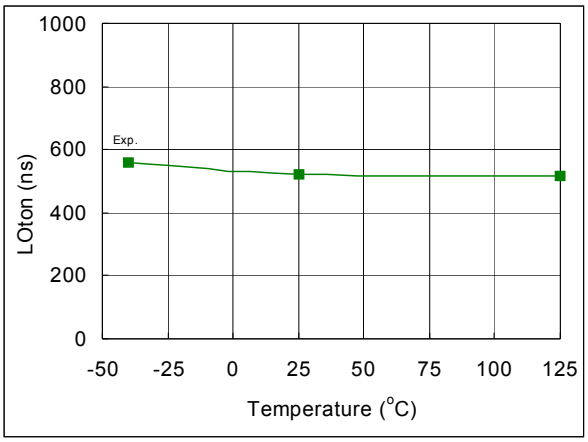


Fig. 52. Turn-On Propagation Delay vs. Temperature

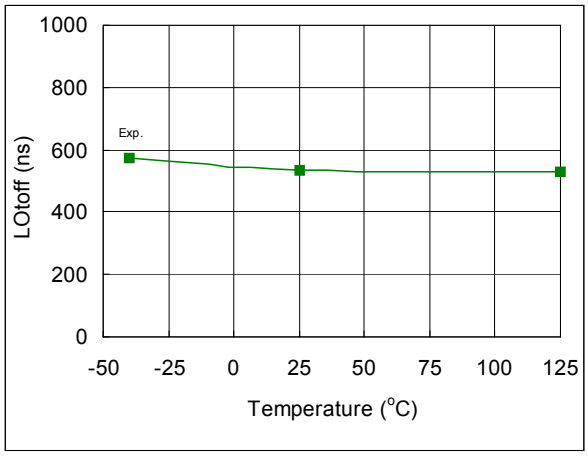


Fig. 53. Turn-Off Propagation Delay vs. Temperature

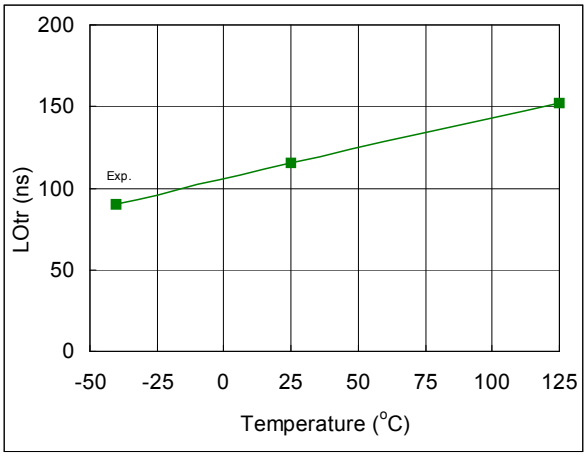


Fig. 54. Turn-On Rise Time vs. Temperature

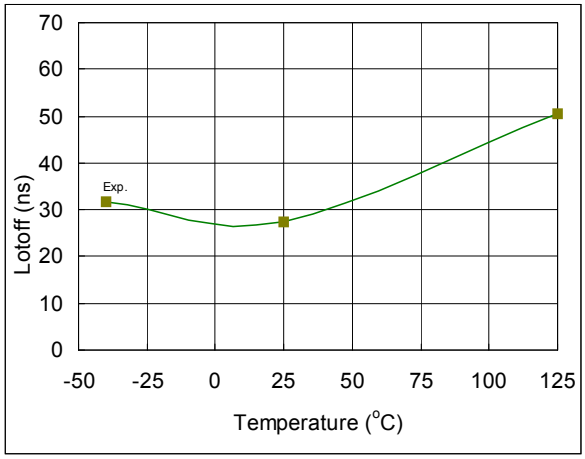


Fig. 55. Turn-Off Fall Time vs. Temperature

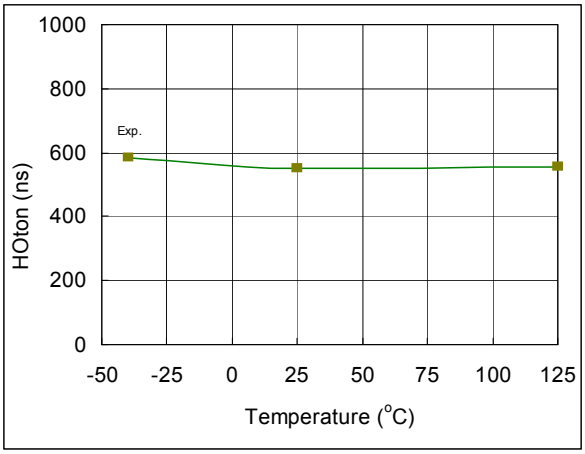


Fig. 56. Turn-On Propagation Delay vs. Temperature

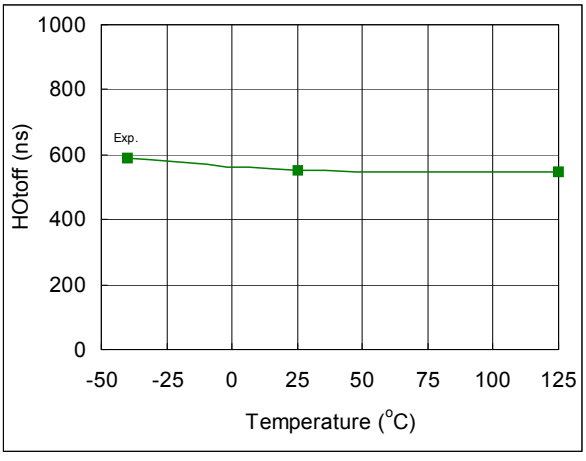


Fig. 57. Turn-Off Propagation Delay vs. Temperature

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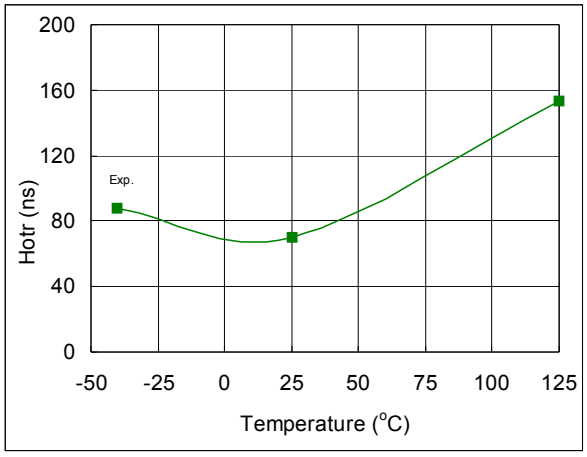


Fig. 58. Turn-On Rise Time vs. Temperature

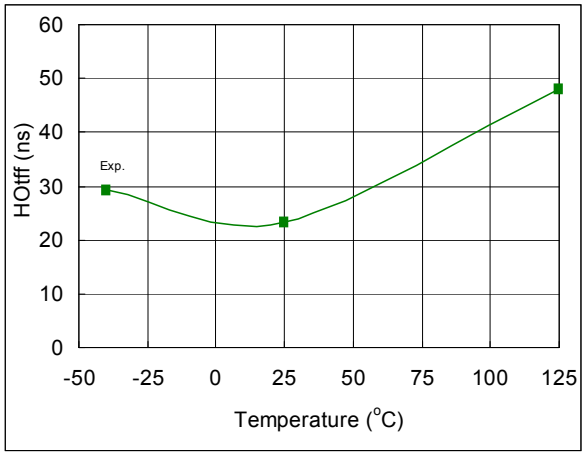


Fig. 59. Turn-Off Fall Time vs. Temperature

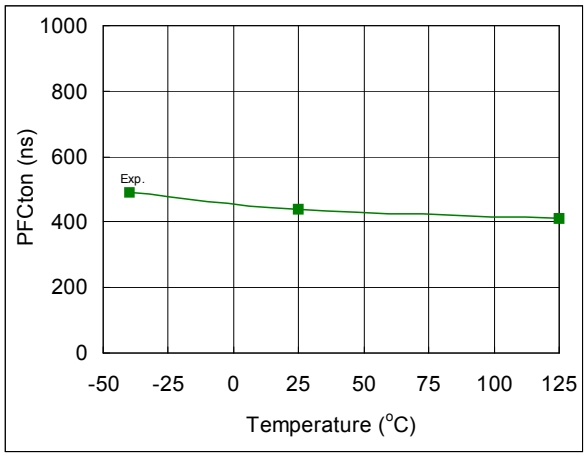


Fig. 60. Turn-On Propagation Delay vs. Temperature

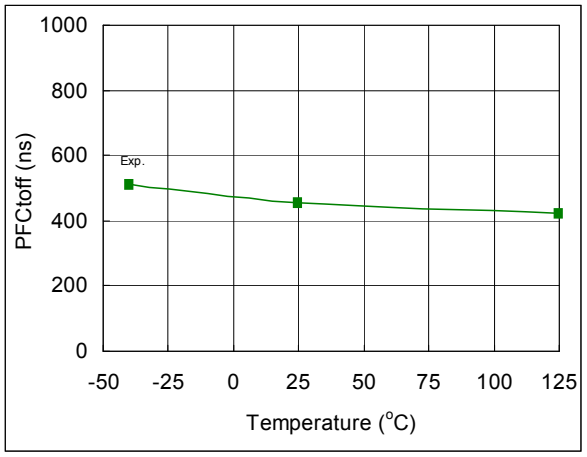


Fig. 61. Turn-Off Propagation Delay vs. Temperature

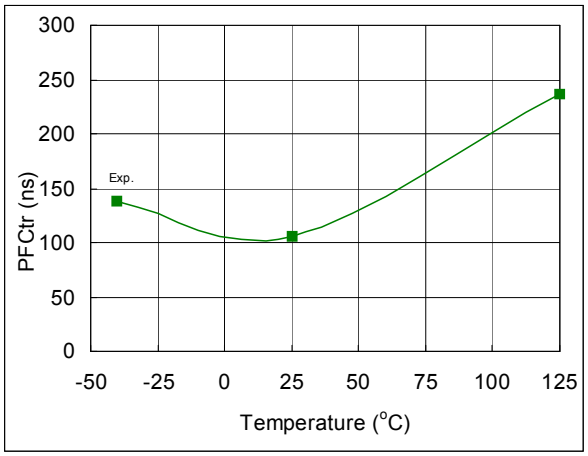


Fig. 62. Turn-On Rise Time vs. Temperature

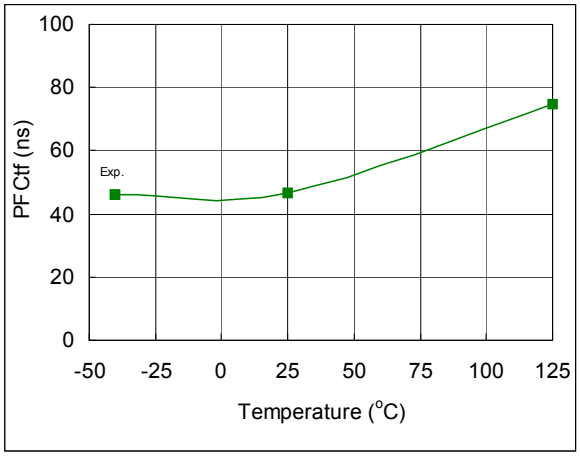


Fig. 63. Turn-Off Fall Time vs. Temperature

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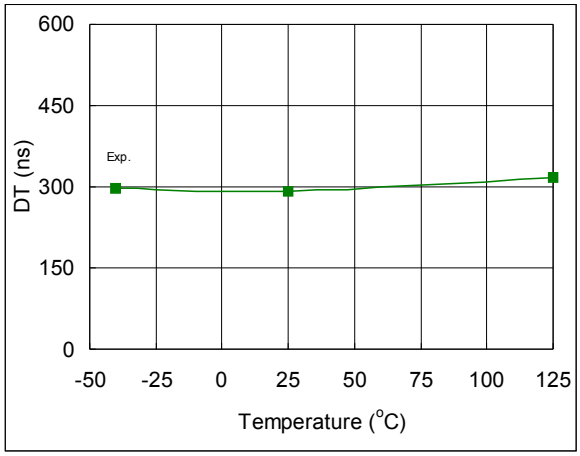


Fig. 64. Deadtime Rise Time vs. Temperature

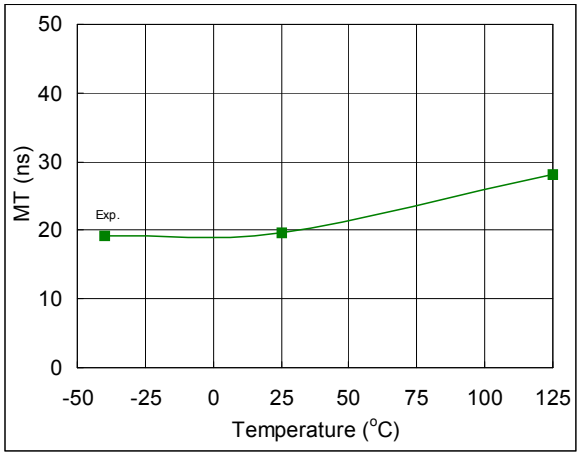


Fig. 65. Ton, Off Matching Time vs. Temperature

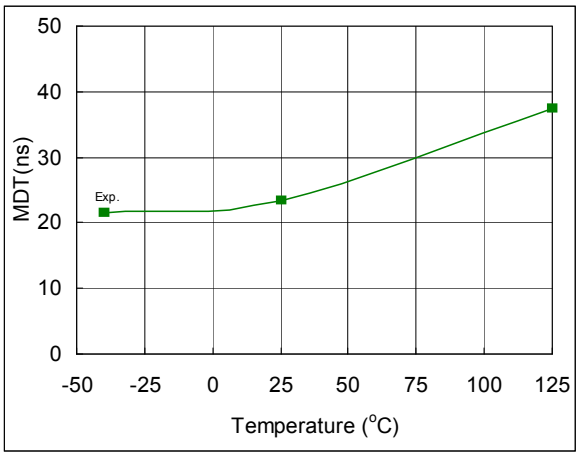


Fig. 66. Deadtime Matching vs. Temperature

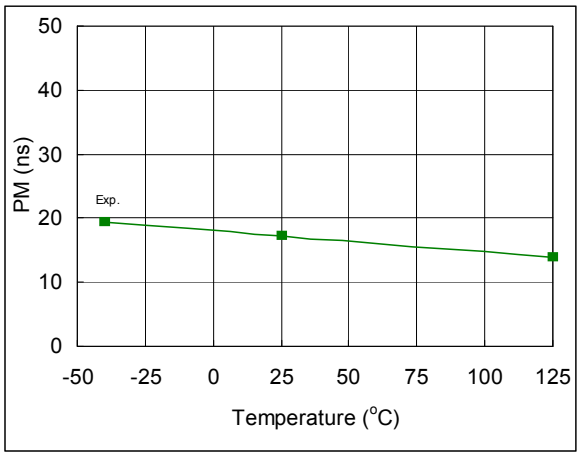


Fig. 67. Pulse Width Distortion vs. Temperature

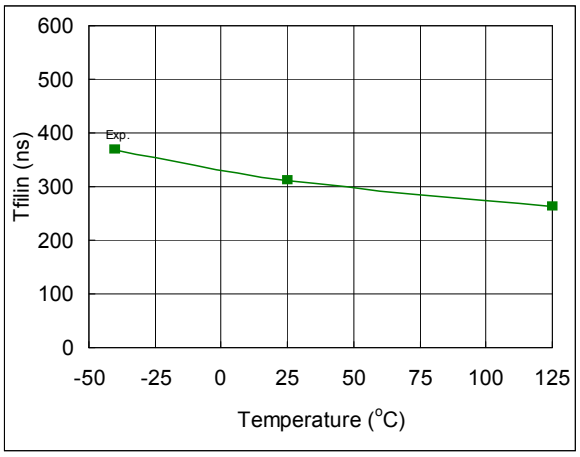


Fig. 68. Input Filter Time vs. Temperature

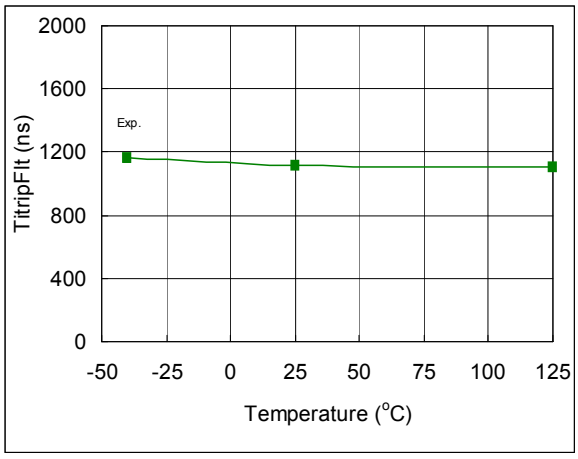


Fig. 69. ITRIP to Fault Time vs. Temperature

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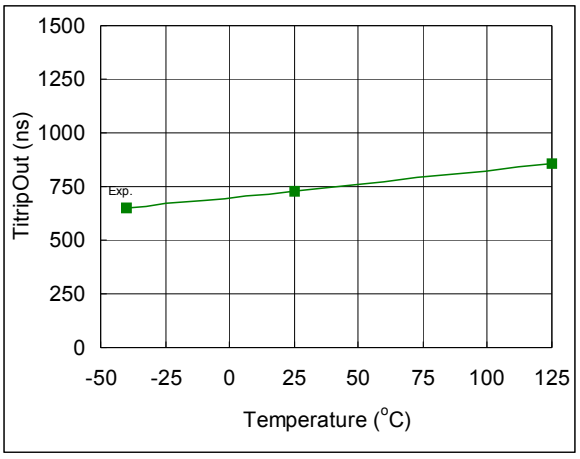


Fig. 70. ITRIP to Output Shutdown Propagation Delay vs. Temperature

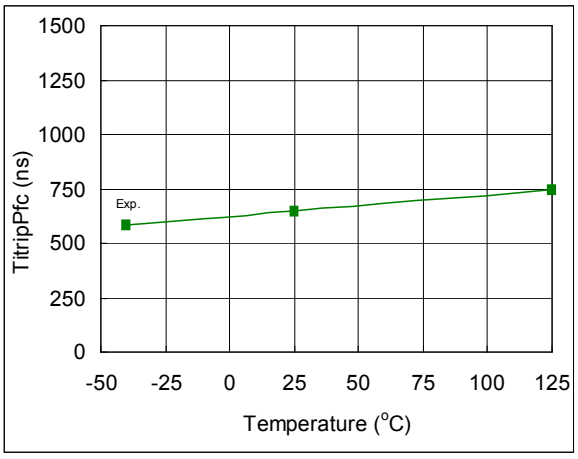


Fig. 71. ITRIP to PFC_{OUT} Shutdown Propagation Delay vs. Temperature

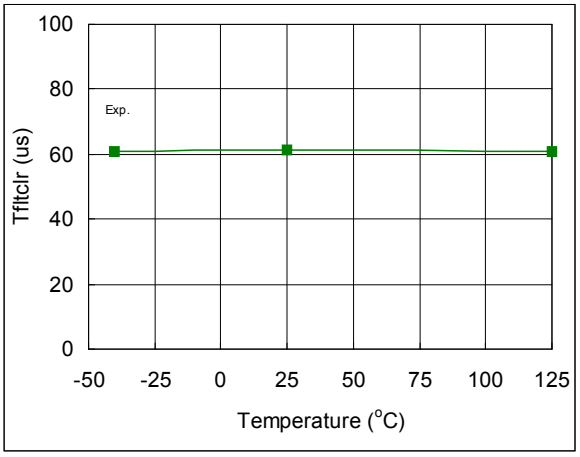


Fig. 72. FAULT Clear Time RCIN vs. Temperature

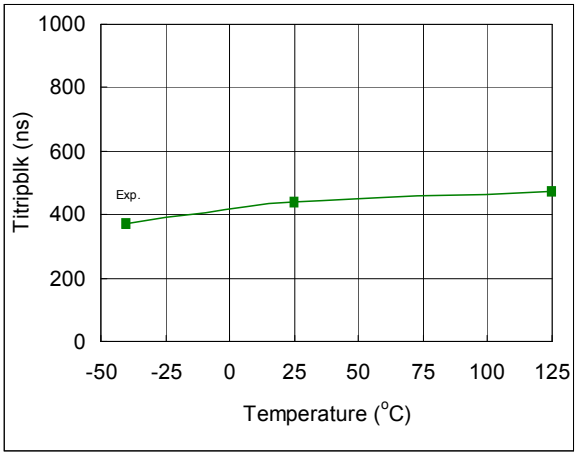


Fig. 73. ITRIP Blanking Time vs. Temperature

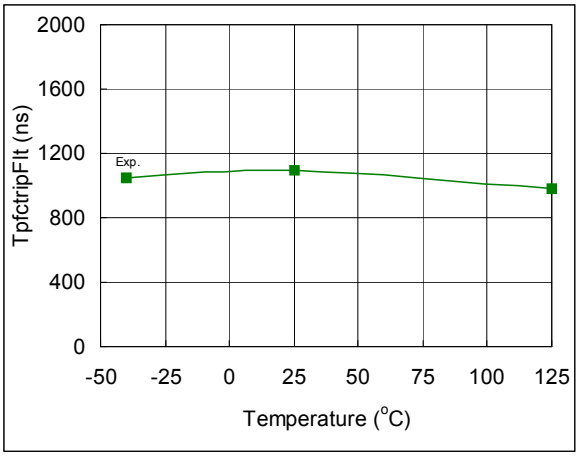


Fig. 74. PFC_{TRIP} to Fault Time vs. Temperature

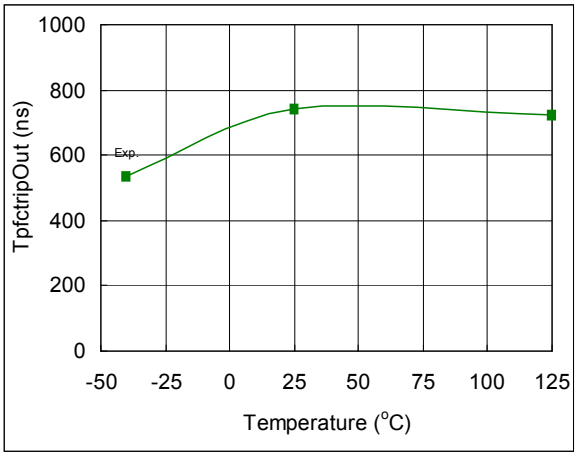


Fig. 75. PFC_{TRIP} to Output Shutdown Propagation Delay

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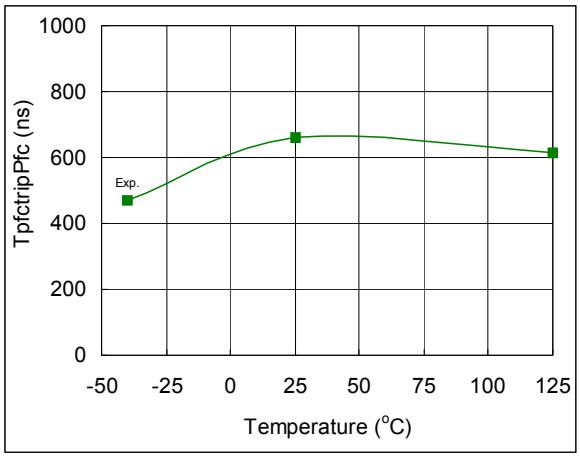


Fig. 76. PFC_{TRIP} to PFC Output Shutdown Propagation Delay vs. Temperature

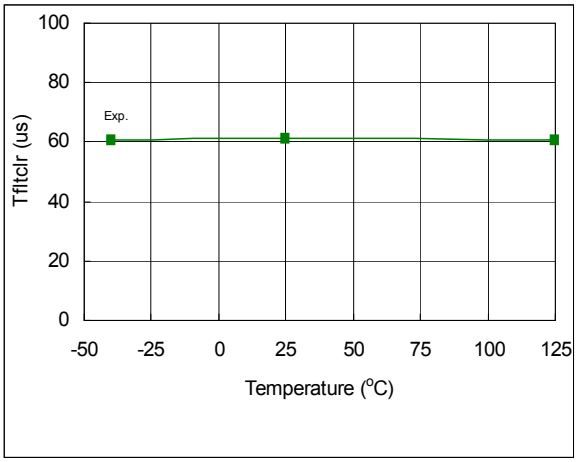


Fig. 77. FAULT Clear Time RCIN vs. Temperature

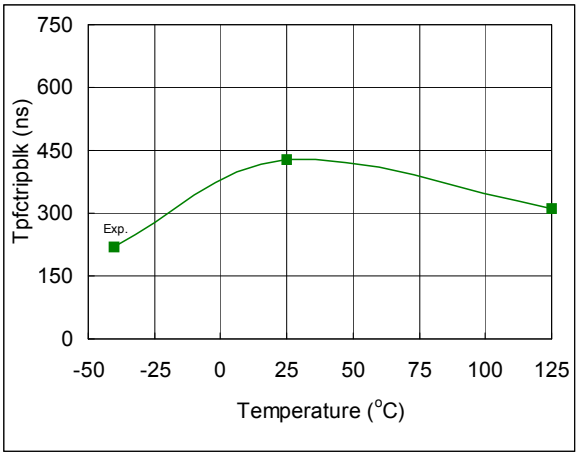


Fig. 78. PFC_{TRIP} Blanking Time vs. Temperature

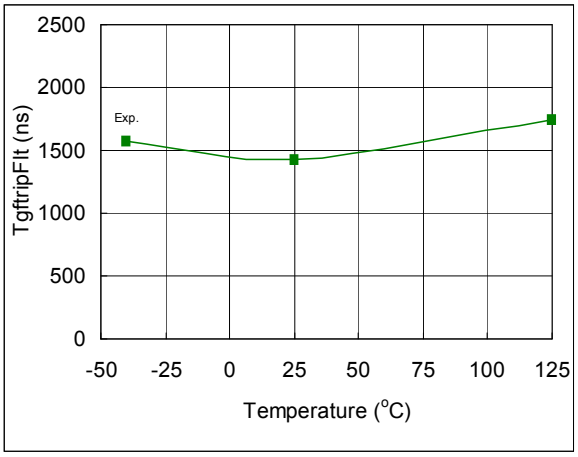


Fig. 79. GF_{TRIP} to Fault Time vs. Temperature

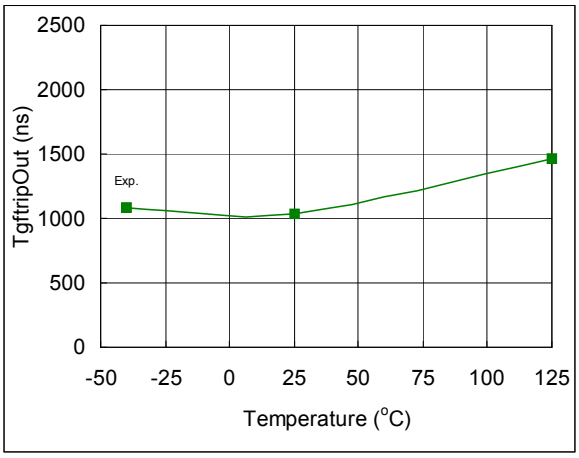


Fig. 80. GF_{TRIP} to Output Shutdown Propagation Delay vs. Temperature

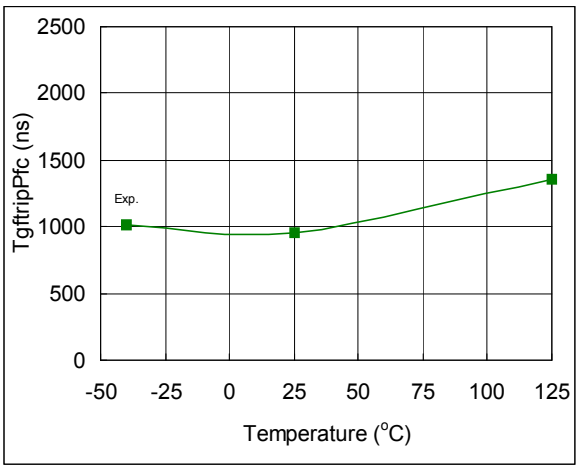


Fig. 81. GF_{TRIP} to PFC Output Shutdown Propagation Delay vs.

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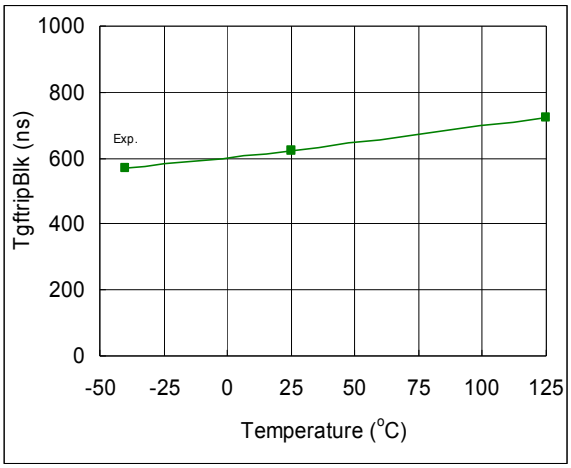


Fig. 82. GF_{TRIP} Blanking Time vs. Temperature

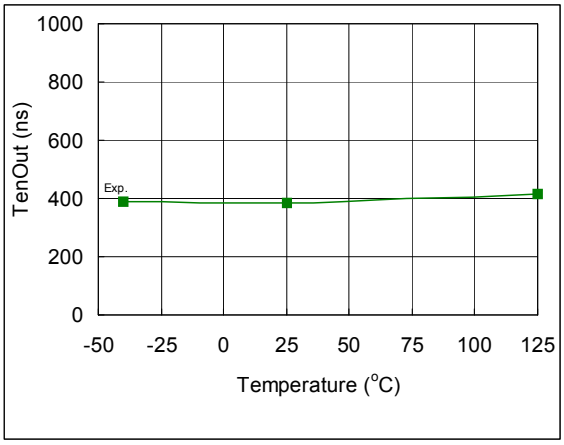


Fig. 83. EN On to Output Propagation Delay vs. Temperature

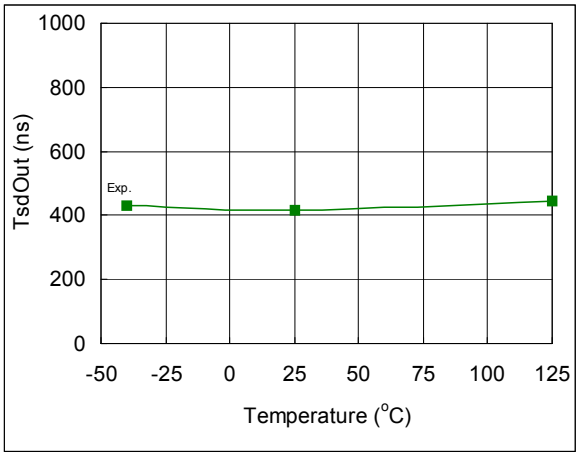


Fig. 84. EN Off to Output Shutdown Propagation Delay vs. Temperature

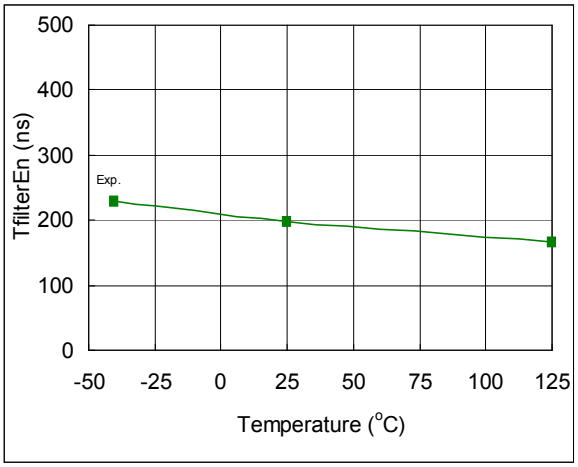


Fig. 85. Enable Input Filter Time vs. Temperature

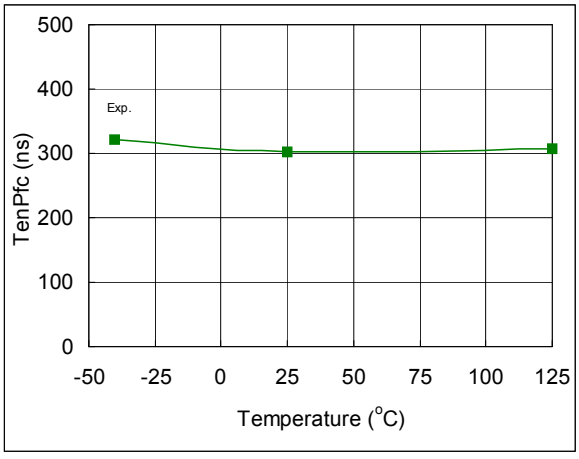


Fig. 86. EN On to PFC Output Propagation Delay vs. Temperature

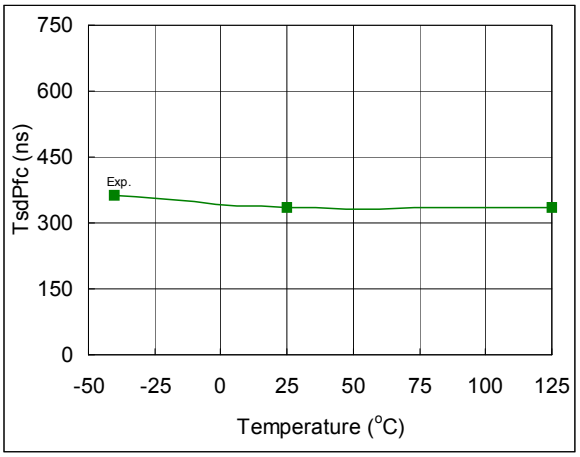


Fig. 87. EN off to Output Shutdown PFC Propagation Delay vs. Temperature

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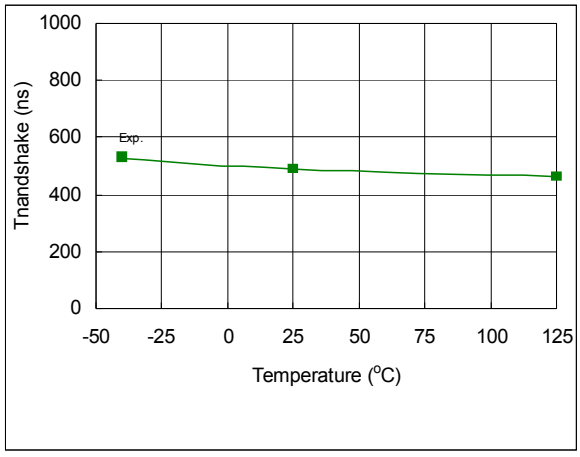


Fig. 88. Input to Hand Shake Mode Delay vs. Temperature

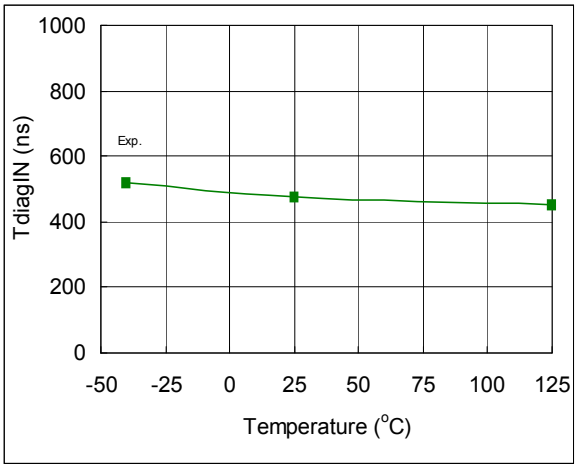


Fig. 89. Input to DIAG Mode in Delay vs. Temperature

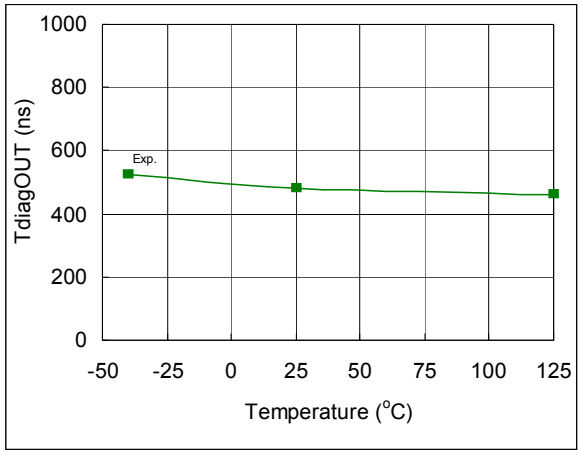


Fig. 90. Input to DIAG Mode Out Delay vs. Temperature

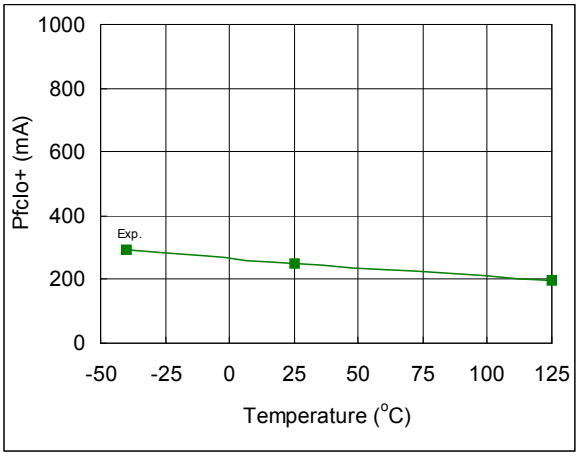


Fig. 91. Output High Short Circuit Pulsed Current PFC_{OUT} vs. Temperature

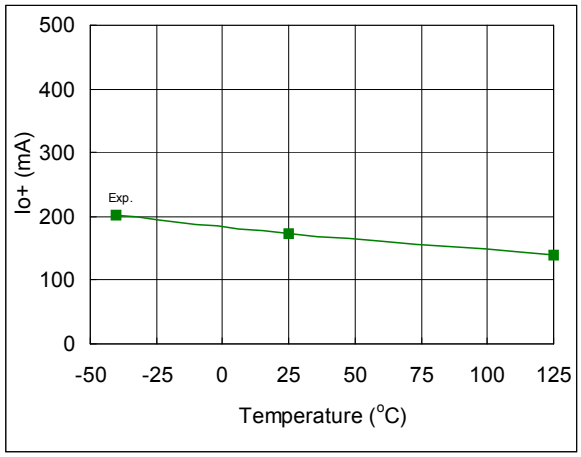


Fig. 92. Output High Short Circuit Pulsed Current, HO1,2,3 vs. Temperature

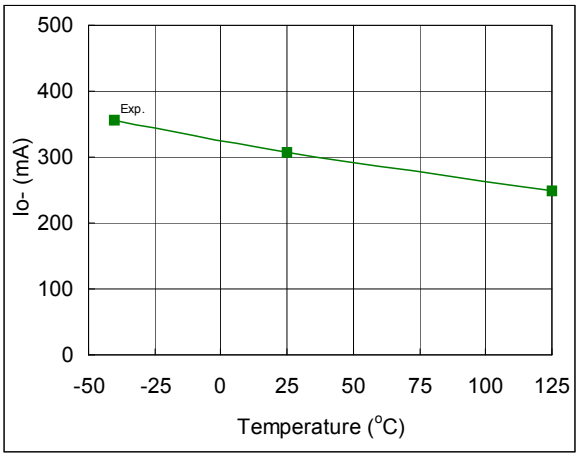


Fig. 93. Output Low Short Circuit Pulsed Current, HO1,2,3 vs. Temperature

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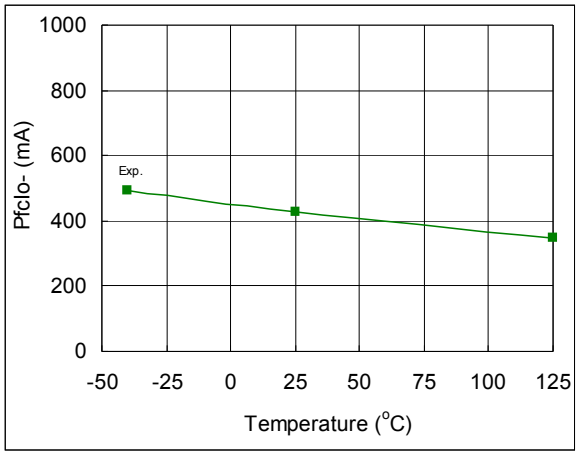


Fig. 94. Output Low Short Circuit Pulsed Current, PFC_{OUT} vs. Temperature

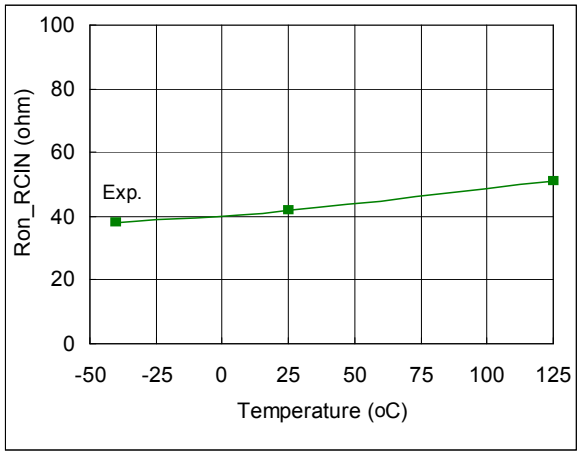


Fig. 95. RCIN Low On Resistance vs. Temperature

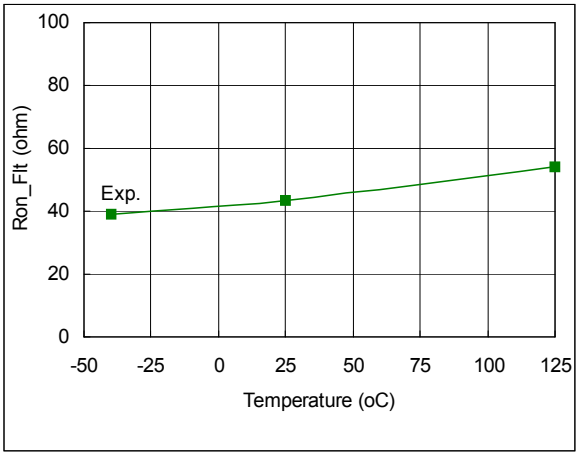


Fig. 96. FLT Low On Resistance vs. Temperature

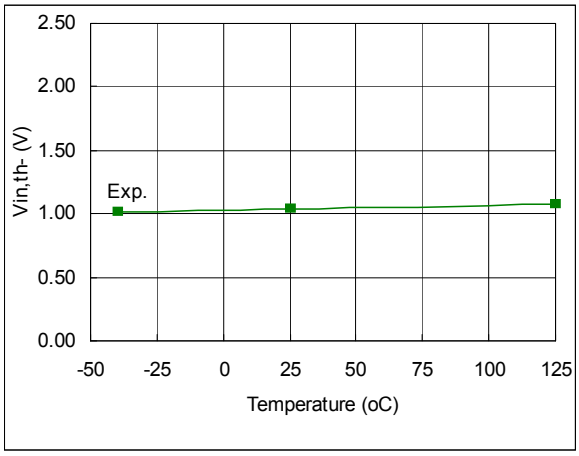


Fig. 97. Input Negative Going Threshold vs. Temperature

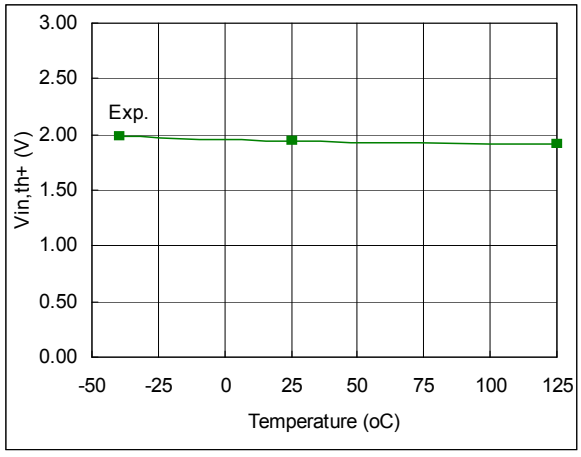


Fig. 98. Input Positive Going Threshold vs. Temperature

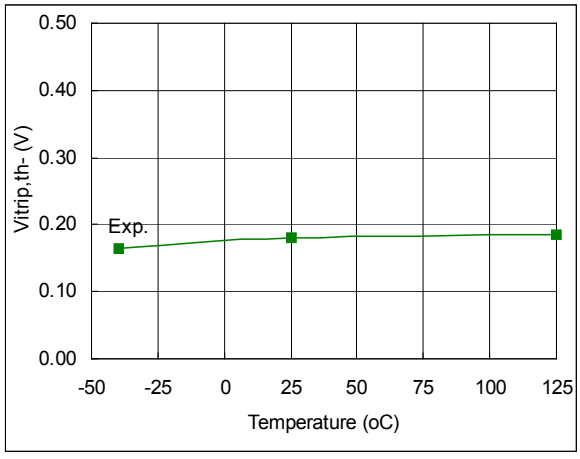


Fig. 99. Input Negative Going Threshold vs. Temperature

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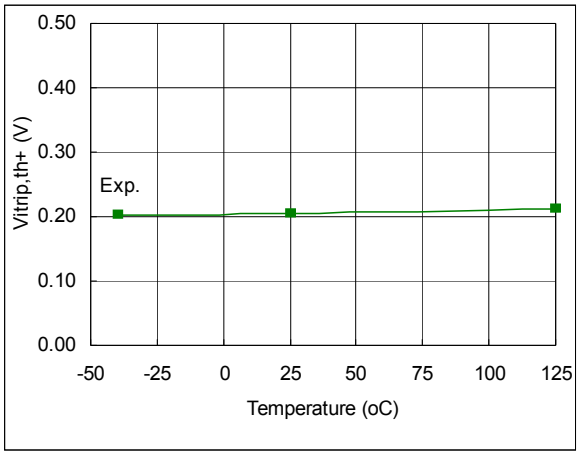


Fig. 100. Input Positive Going Threshold vs. Temperature

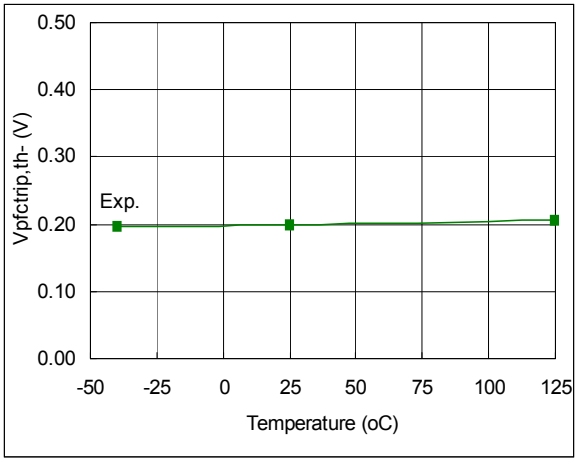


Fig. 101. PFC Negative Going Threshold vs. Temperature

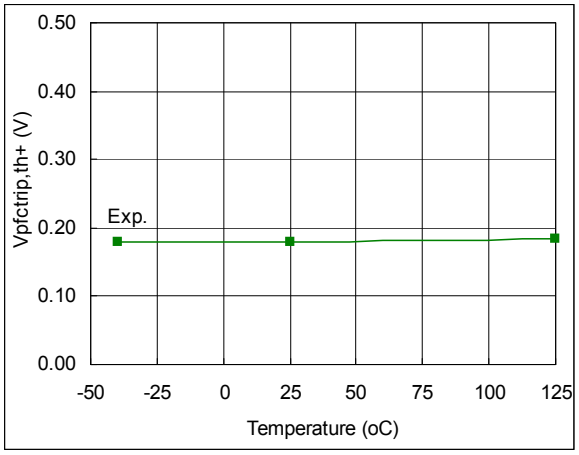


Fig. 102. PFC Positive Going Threshold vs. Temperature

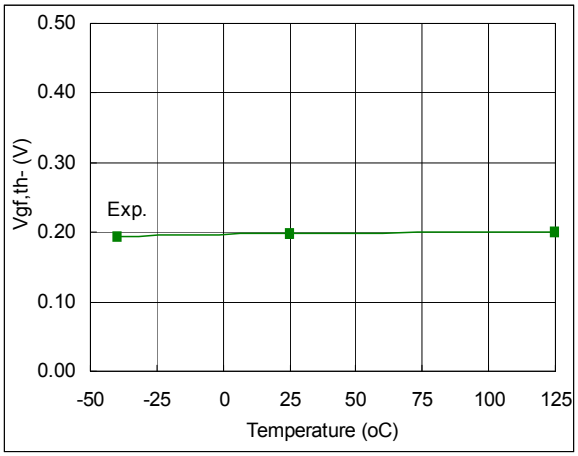


Fig. 103. GF Negative Going Threshold vs. Temperature

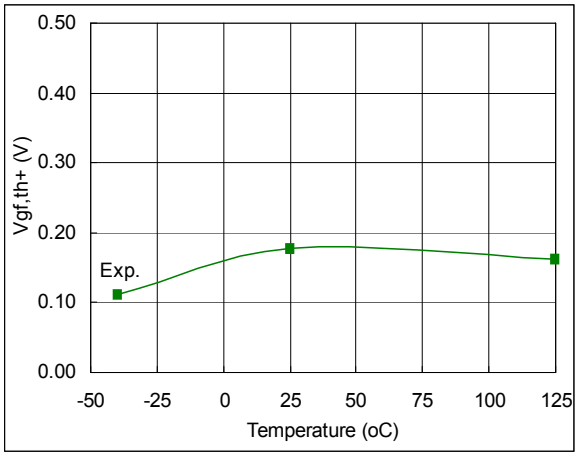


Fig. 104. GF Positive Going Threshold vs. Temperature

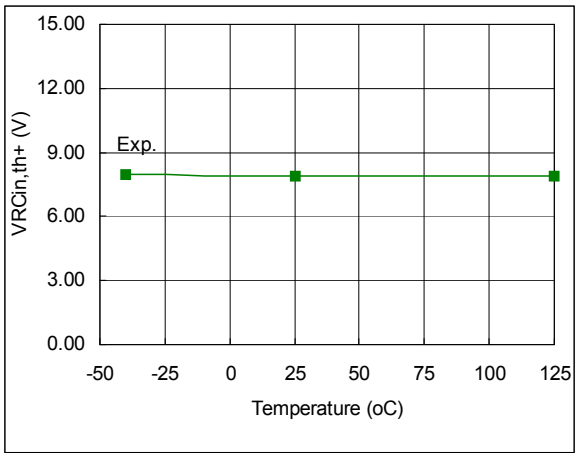


Fig. 105. RCIN Positive Going Threshold vs. Temperature

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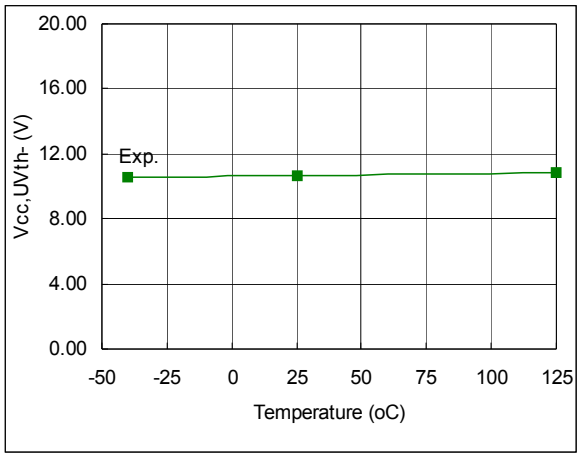


Fig. 106. V_{CC} Supply Undervoltage Negative Going Threshold vs. Temperature

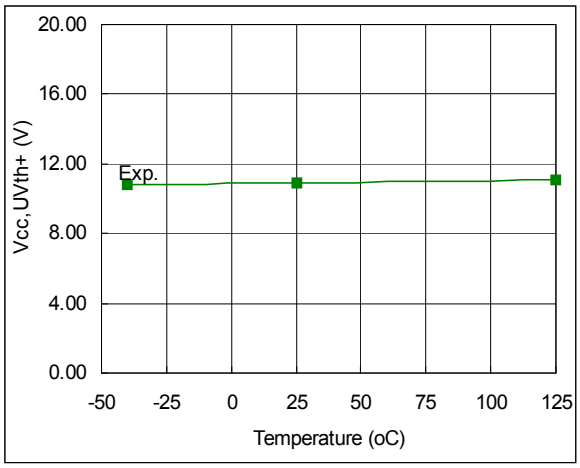


Fig. 107. V_{CC} Supply Undervoltage Positive Going Threshold vs. Temperature

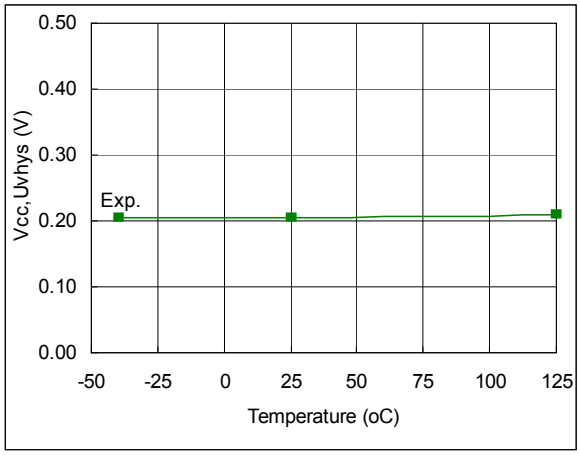


Fig. 108. V_{CC} Supply Undervoltage Hysteresis vs. Temperature

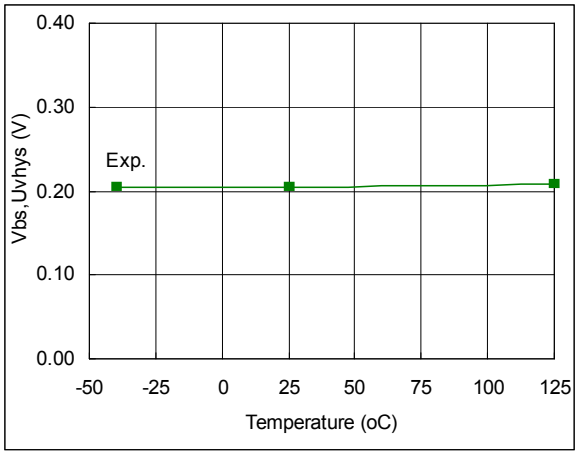


Fig. 109. V_{BS} Supply Undervoltage Hysteresis vs. Temperature

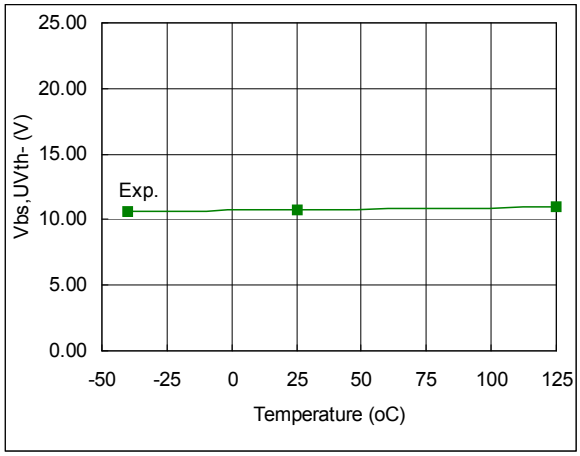


Fig. 110. V_{BS} Supply Undervoltage Negative Going Threshold vs. Temperature

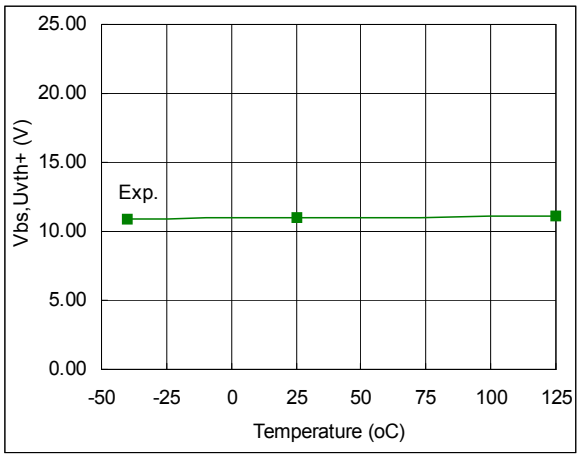


Fig. 111. V_{BS} Supply Undervoltage Positive Going Threshold vs. Temperature

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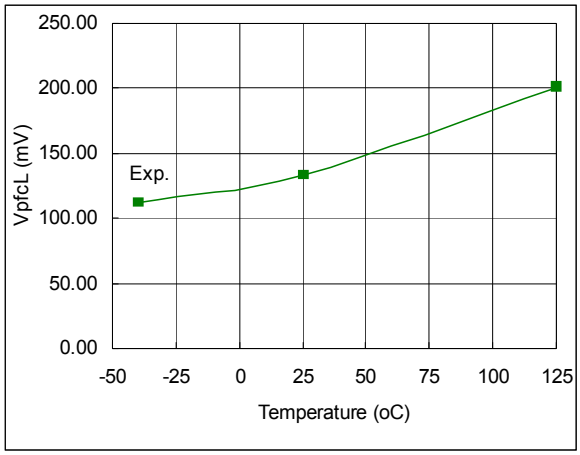


Fig. 112. Low Level Output Voltage, V_{BIAS} - V_O, PFC_{OUT} vs. Temperature

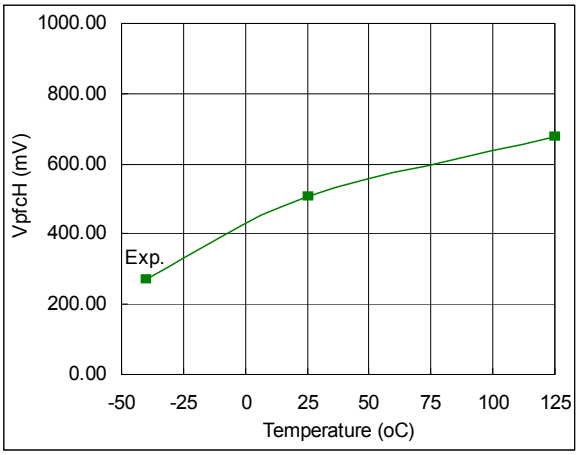


Fig. 113. High Level Output Voltage, V_{BIAS} - V_O, PFC_{OUT} vs. Temperature

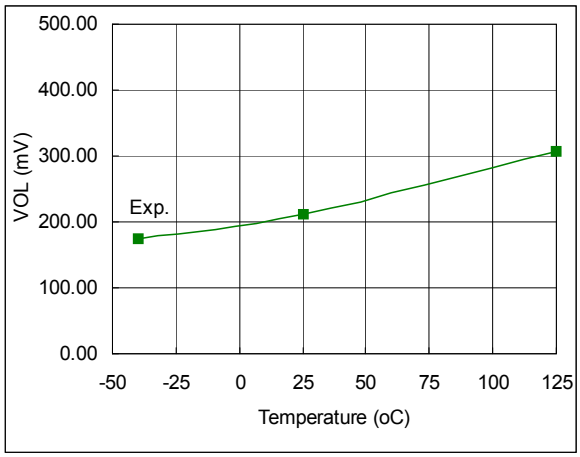


Fig. 114. Low Level Output Voltage, V_O, HO1,2,3 vs. Temperature

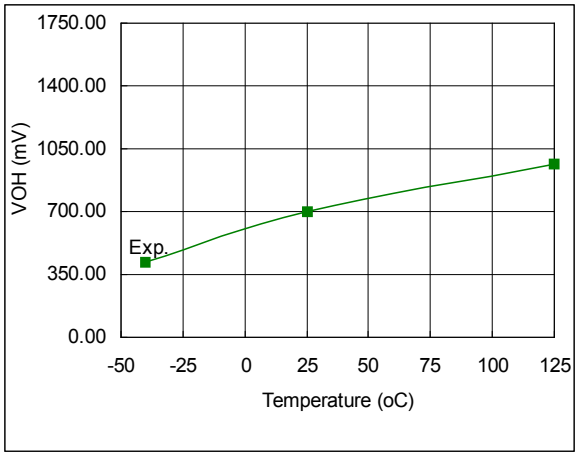


Fig. 115. High Level Output Voltage, V_{BIAS} - V_O, HO1,2,3 vs. Temperature

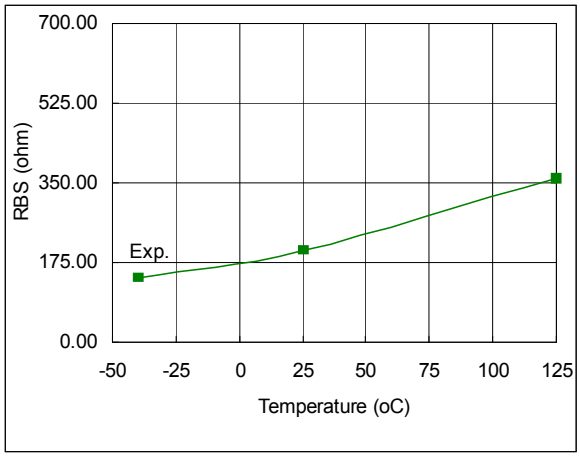


Fig. 116. Ron Internal Bootstrap Diode vs. Temperature

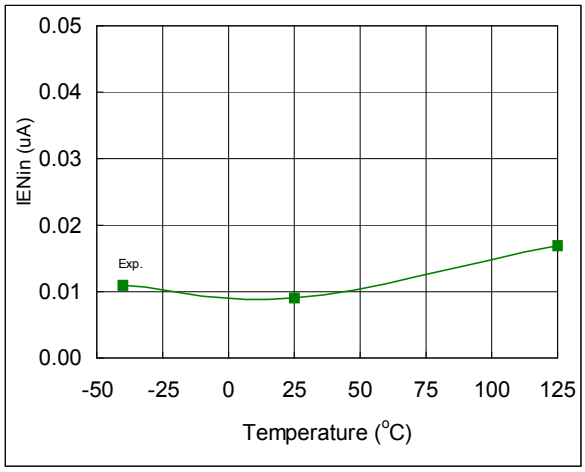
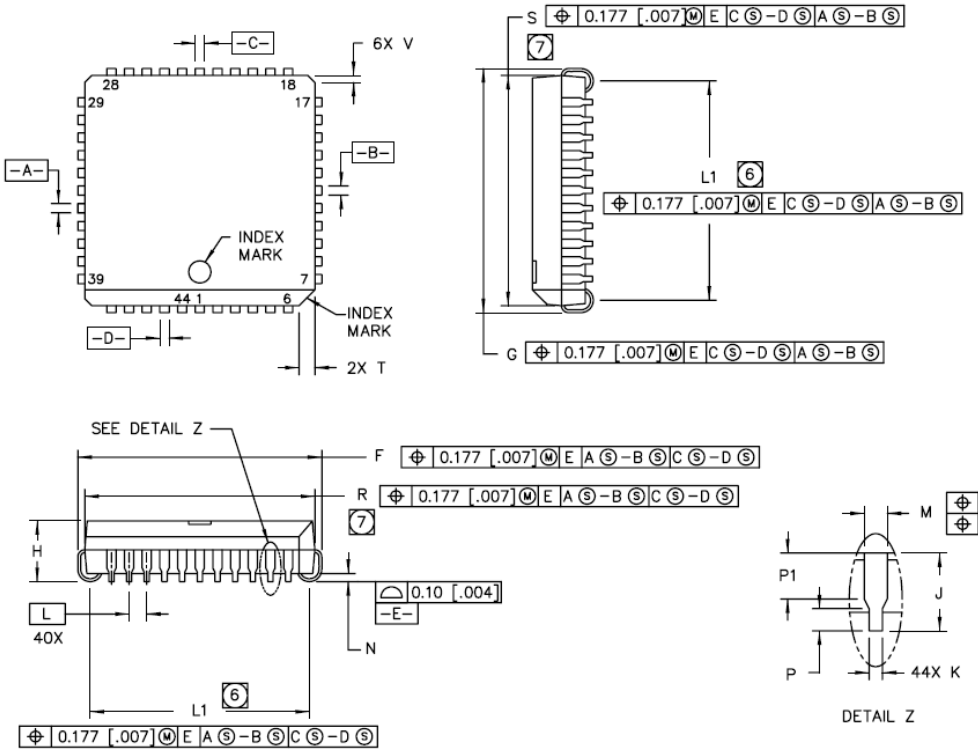


Fig. 117. En Input Bias Current vs. Temperature

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Package Details: PLCC44



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—
EXPOSED PINS	44		44	

NOTES:

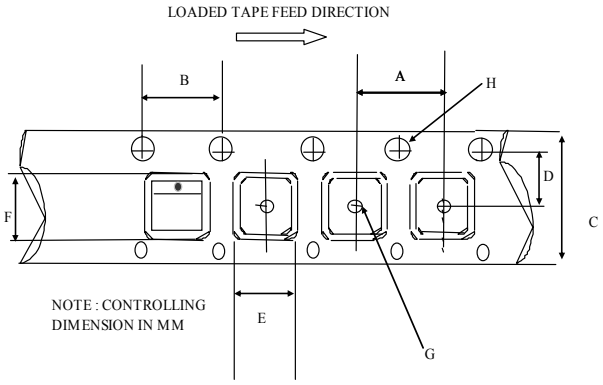
1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M–1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS–018.
6. TO BE MEASURED AT –E– SEATING PLANE.
   OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.

(5) DATUMS –A–, –B–, –C–, & –D– ARE DETERMINED BY WHERE THE TOP

(7) DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

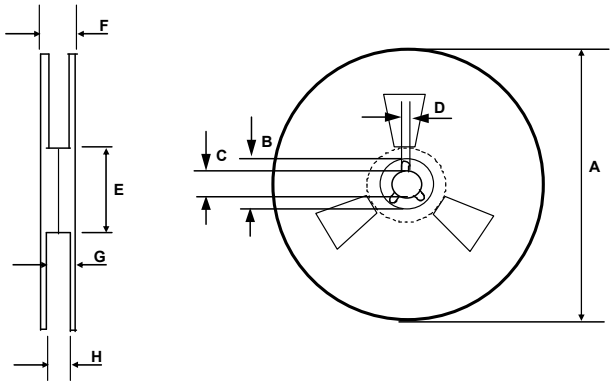
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Tape and Reel Details: PLCC44



CARRIER TAPE DIMENSION FOR 44PLCC

	Metric		Imperial	
Code	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062

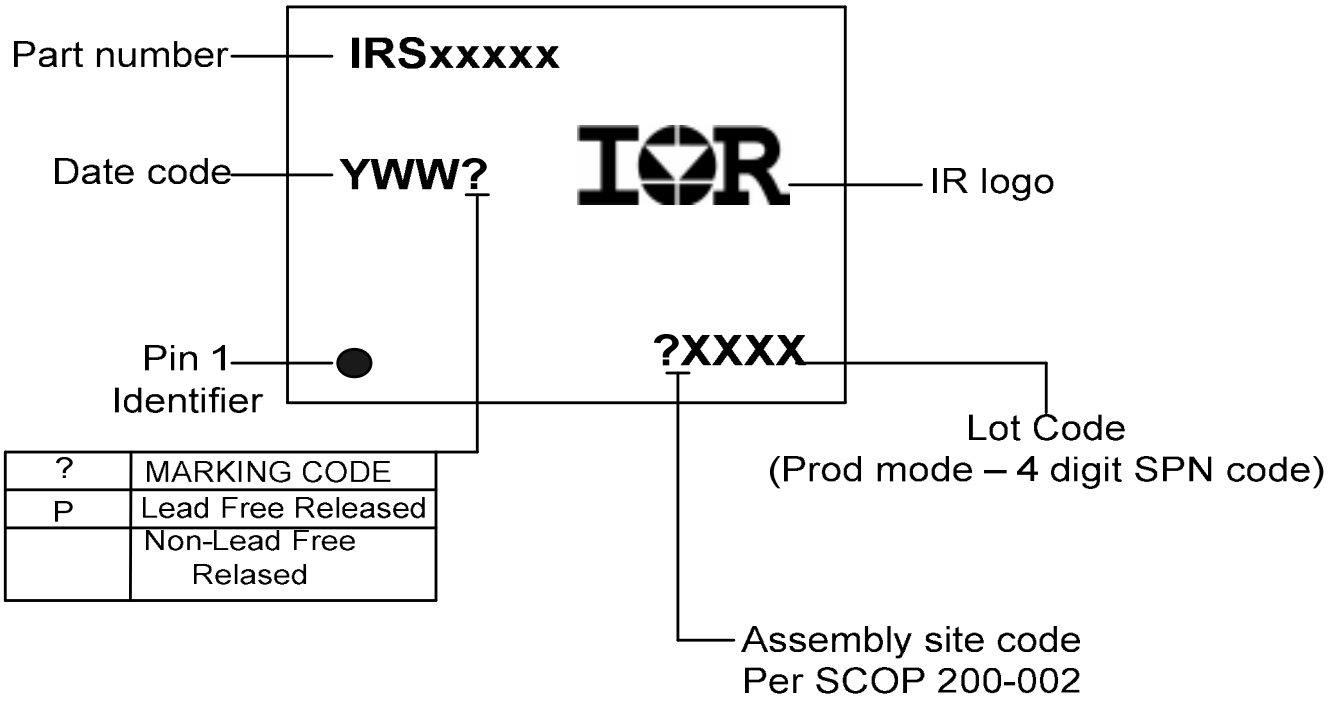


REEL DIMENSIONS FOR 44PLCC

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

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Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

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Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS26302DJ	PLCC44	Tube/Bulk	27	IRS26302DJPBF
		Tape and Reel	500	IRS26302DJTRPBF

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http://www.irf.com/technical-info/

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Tel: (310) 252-7105

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Revision History

Date	Comment
MM/DD/YY	Original document
Rev3.1	Started from rev3.0 of repository: header and footer updated, standard package PLCC44 specified, duplicate definition in dynamic electrical characteristic deleted
Rev3.3	Add application part related to bootstrap fet limitation

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