DATA SHEET



TDA9874A
Digital TV sound demodulator/decoder

Preliminary specification
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PHILIPS

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1 FEATURES

- Sound IF (SIF) input switch
- SIF AGC with 24 dB control range
- Switchable 10 dB SIF input attenuator
- SIF 8-bit Analog-to-Digital Converter (ADC)
- Easy TV standard programming option
- Differential Quadrature Phase Shift Keying (DQPSK) demodulation for different standards, simultaneously with 1-channel FM demodulation
- NICAM decoding (B/G, D/K, I and L standard)
- 2-carrier multi-standard FM demodulation (B/G, D/K and M standard)
- Single carrier high deviation FM mono demodulation mode
- Decoding for three analog multi-channel systems (A2) and satellite sound
- Adaptive de-emphasis for satellite
- Programmable identification (B/G, D/K and M standard) and different identification times
- FM pilot carrier presence detector
- Optional AM demodulation for system L, simultaneously with NICAM
- Monitor selection for FM/AM demodulator outputs and FM and NICAM signals with peak option
- Automatic FM dematrixing option
- Digital crossbar switch
- I^2S-bus serial audio output with matrix, level adjustment and mute
- Dual audio Digital-to-Analog Converter (DAC) from digital crossbar switch to analog crossbar switch, bandwidth = 15 kHz
- Automatic Volume Level (AVL) control
- Analog crossbar switch with inputs for mono and stereo
- Output selection of mono, stereo, dual, dual A or dual B
- Additional mono output with automatic select
- 20 kHz bandwidth for analog path
- Standby mode
- Automatic output selection for TV applications.

2 GENERAL DESCRIPTION

The TDA9874A is a single-chip Digital TV Sound Demodulator/Decoder (DTVSD) for analog and digital multi-channel sound systems in TV/VCR sets and satellite receivers.

2.1 Supported standards

The multi-standard/multi-stereo capability of the TDA9874A is of interest in Europe, Hong Kong/PR China and South East Asia. This includes B/G, D/K, I, M and L standard. In other application areas subsets of the standard combinations are available or, only single standards are transmitted.

All A2 (analog 2-carrier) and NICAM systems are supported. M standard (with mono or BTSC stereo sound) can be received and processed in mono sound mode.

The AM sound of L/L' standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9874A. A second possibility is to use the internal AM demodulator stage (with 6.5 MHz intercarrier), which gives limited performance.

Korea has a stereo sound system similar to Europe and is supported by the TDA9874A. The differences include deviation, modulation contents and identification. It is based on M standard.

For all FM standards a high deviation mode for a single carrier monaural sound demodulation is selectable.

An overview of the supported standards and sound systems and their key parameters is given in Tables 1 to 3.

The analog multi-channel systems are sometimes also called 2CS (2-carrier systems).

2.1.1 Analog 2-carrier systems

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz)			MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/μs)
			NOM.	MAX.	OVER.	SC1	SC2	
M	mono	4.5	15	25	50	mono	–	15/75
M	A2	4.5/4.724	15	25	50	½(L + R)	½(L – R)	15/75 (Korea)
B/G	A2	5.5/5.742	27	50	80	½(L + R)	R	15/50
I	mono	6.0	27	50	80	mono	–	15/50
D/K (2)	A2	6.5/6.742	27	50	80	½(L + R)	R	15/50
D/K (1)	A2	6.5/6.258	27	50	80	½(L + R)	R	15/50
D/K (3)	A2	6.5/5.742	27	50	80	½(L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2; A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 × line frequency	55.0699 kHz = 3.5 × line frequency
Stereo identification frequency	$117.5\ \text{Hz} = \frac{\text{line frequency}}{133}$	$149.9\ \text{Hz} = \frac{\text{line frequency}}{105}$
Dual identification frequency	$274.1\ \text{Hz} = \frac{\text{line frequency}}{57}$	$276.0\ \text{Hz} = \frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 2-carrier systems with NICAM

Table 3 NICAM

STANDARD	SC1						SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHz)	TYPE	MODULATION							
			INDEX (%)		DEVIATION (kHz)					
			NOM.	MAX.	NOM.	MAX.				
B/G	5.5	FM	–	–	27	50	5.85	J17	40	note 1
I	6.0	FM	–	–	27	50	6.552	J17	100	note 1
D/K	6.5	FM	–	–	27	50	5.85	J17	40	note 2
L	6.5	AM	54	100	–	–	5.85	J17	40	note 1

Notes

1. See *"EBU NICAM 728 specification"* or equivalent specification.
2. Not yet officially defined.

2.1.3 SATELLITE SYSTEMS

An important specification for satellite TV reception is the Astra specification. The TDA9874A is suitable for the reception of Astra and other satellite signals, with sound carrier frequencies from 4 to 9.2 MHz.

Table 4 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/μs)
Main	6.50[1]	0.26	85[2]	mono	15/50[1]
Sub	7.02/7.20	0.15	50	m/st/d[3]	15/adaptive[4]
	7.38/7.56				
	7.74/7.92				
	8.10/8.28				

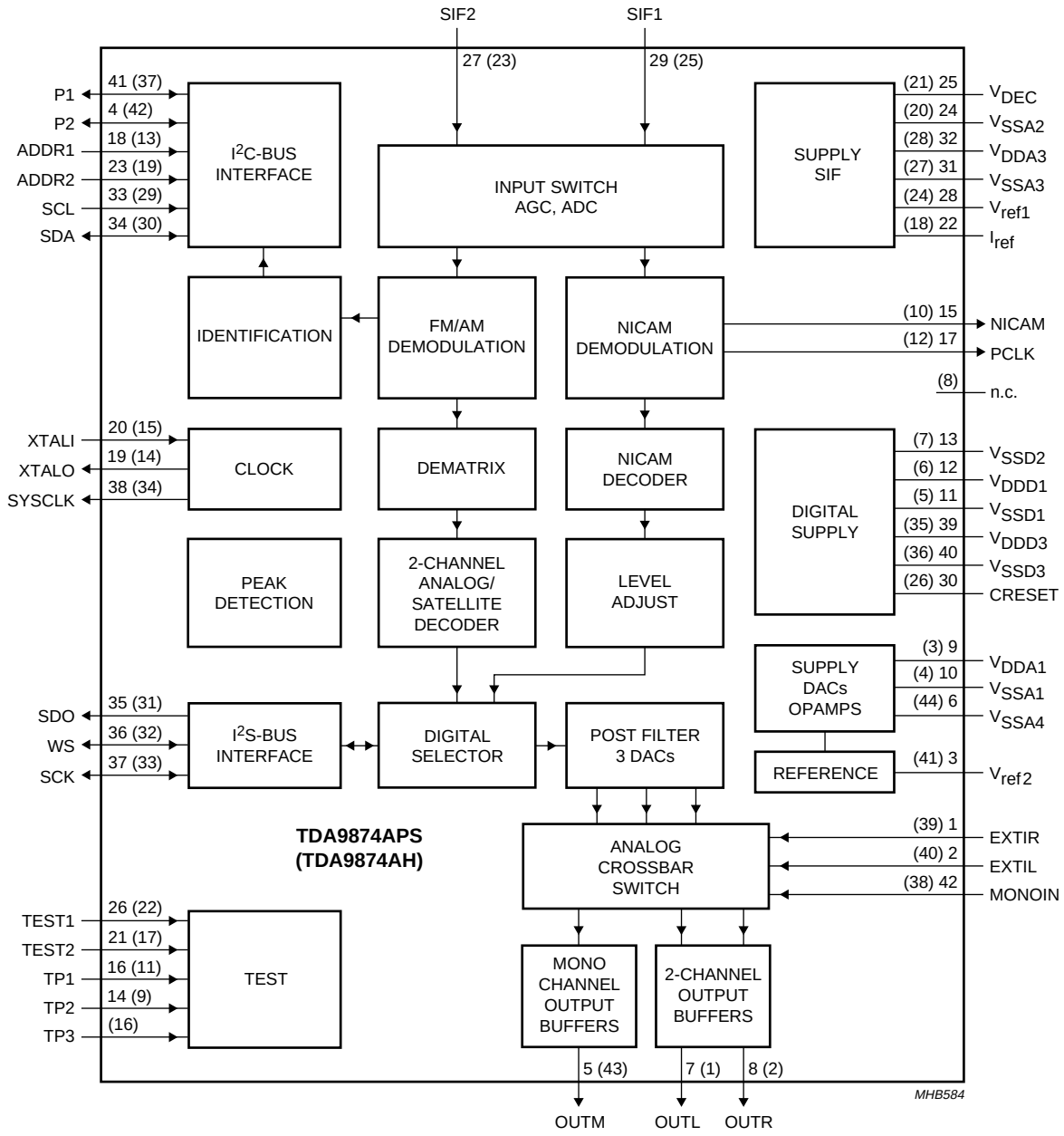
Notes

1. For other satellite systems, frequencies of e.g. 5.80, 6.60 or 6.65 MHz can also be received. A de-emphasis of 60 μs, or in accordance with J17, is available.
2. Main channels with high deviation can also be handled.
3. m/st/d = mono or stereo or dual language sound.
4. Adaptive de-emphasis is compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9874APS	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA9874AH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

4 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the TDA9874AH.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
EXTIR	1	39	external audio input right channel
EXTIL	2	40	external audio input left channel
V_{ref2}	3	41	analog reference voltage for DAC and operational amplifiers
P2	4	42	second general purpose I/O pin
OUTM	5	43	analog output right
V_{SSA4}	6	44	analog ground supply 4 for analog back-end circuitry
OUTL	7	1	analog output left
OUTR	8	2	analog output right
V_{DDA1}	9	3	analog supply voltage 1; back-end circuitry 5 V
V_{SSA1}	10	4	analog ground supply 1; back-end circuitry
V_{SSD1}	11	5	digital ground supply 1; core circuitry
V_{DDD1}	12	6	digital supply voltage 1; core voltage regulator circuitry
V_{SSD2}	13	7	digital ground supply 2; core circuitry
n.c.	–	8	not connected
TP2	14	9	additional test pin 2; connected to V_{SSD} for normal operation
NICAM	15	10	serial NICAM data output (at 728 kHz)
TP1	16	11	additional test pin 1; connected to V_{SSD} for normal operation
PCLK	17	12	NICAM clock output (at 728 kHz)
ADDR1	18	13	first I^2C-bus slave address modifier input
XTALO	19	14	crystal oscillator output
XTALI	20	15	crystal oscillator input
TP3	–	16	additional test pin 3; connected to V_{SSD} for normal operation
TEST2	21	17	test pin 2; connected to V_{SSD} for normal operation
I_{ref}	22	18	resistor for reference current generation; front-end circuitry
ADDR2	23	19	second I^2C-bus slave address modifier input
V_{SSA2}	24	20	analog ground supply 2; analog front-end circuitry
V_{DEC}	25	21	analog front-end circuitry supply voltage decoupling
TEST1	26	22	test pin 1; connected to V_{SSD} for normal operation
SIF2	27	23	sound IF input 2
V_{ref1}	28	24	reference voltage; for analog front-end circuitry
SIF1	29	25	sound IF input 1
CRESET	30	26	capacitor for Power-on reset
V_{SSA3}	31	27	digital ground supply 3; front-end circuitry
V_{DDA3}	32	28	analog front-end circuitry regulator supply voltage 3 (5 V)
SCL	33	29	I^2C-bus serial clock input
SDA	34	30	I^2C-bus serial data input/output
SDO	35	31	I^2S-bus serial data output
WS	36	32	I^2S-bus word select input/output

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
SCK	37	33	I^2S-bus clock input/output
SYSCLK	38	34	system clock output
V_{DDD3}	39	35	digital supply voltage 3; digital I/O pads
V_{SSD3}	40	36	digital ground supply 3; digital I/O pads
P1	41	37	first general purpose I/O pin
MONOIN	42	38	analog mono input

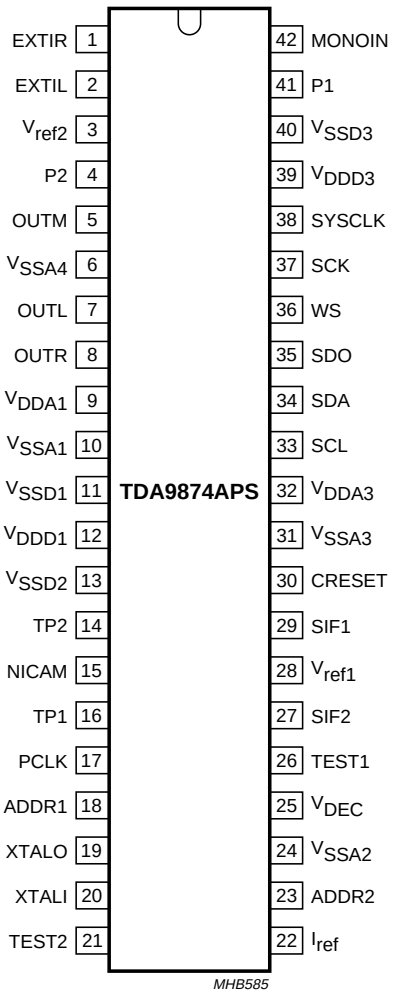


Fig.2 Pin configuration (SDIP42).

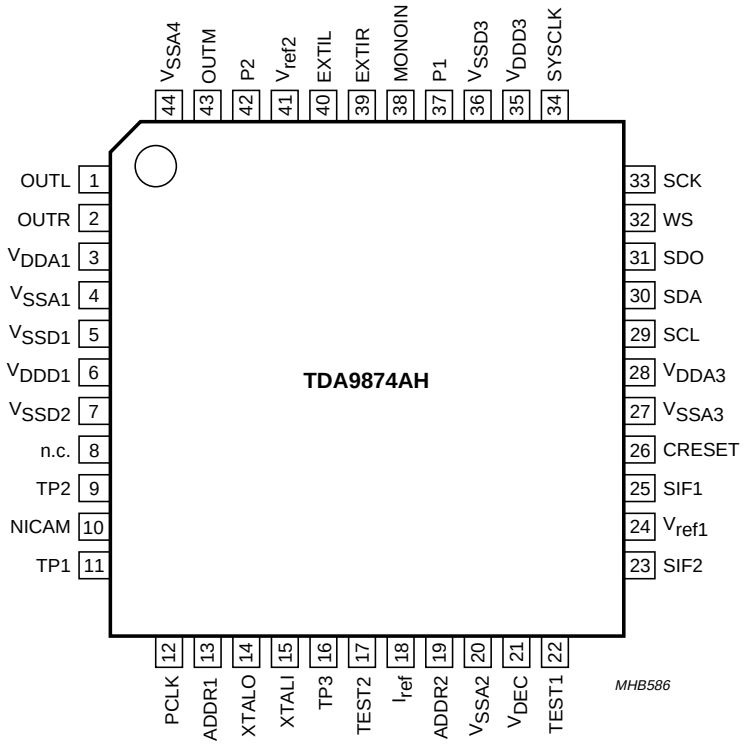


Fig.3 Pin configuration (QFP44).

6 FUNCTIONAL DESCRIPTION

6.1 Description of the demodulator and decoder section

6.1.1 SIF INPUT

Two input pins are provided, SIF1 and SIF2. For higher SIF signal levels the SIF input can be attenuated with an internal switchable −10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads, and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen; see Table 16.

The AGC can be controlled via the I^{2}C-bus; details are given in Sections 10.3.2, 10.3.3 and 10.4.6.

6.1.3 MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I^{2}C-bus (see Sections 10.3.5 and 10.3.6) or via Easy Standard Programming (ESP, see Section 10.3.23). When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is fed through a switchable band-limiting filter into a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

6.1.5 FM DECODING

A 2-carrier stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

Automatic FM dematrixing is also supported, which means that the FM sound mode identification (mono, stereo or dual) switches the FM dematrix directly. No loop via the microcontroller is needed.

For highly overmodulated signals, a high deviation mode for monaural audio sound single carrier demodulation can be selected.

NICAM decoding is still possible in high deviation mode.

6.1.6 FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot and narrow-band detection of the identification frequencies. The result is available via the I^2C-bus interface. A selection can be made via the I^2C-bus for B/G, D/K and M standards, and for three different time constants that represent different trade-offs between speed and reliability of identification. A pilot detector allows the control software to identify an analog 2-carrier (A2) transmission within approximately 0.1 s.

Automatic FM dematrixing, depending on the identification, is possible.

6.1.7 NICAM DEMODULATION

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbits/s. The NICAM demodulator performs DQPSK demodulation and passes the resulting bitstream and clock signal to the NICAM decoder and, for evaluation purposes, to various pins.

A timing loop controls the frequency of the crystal oscillator to lock the sampling instants to the symbol timing of the NICAM data.

6.1.8 NICAM DECODING

The device performs all decoding functions in accordance with the *"EBU NICAM 728 specification"*. After locking to the frame alignment word, the data is descrambled by applying the defined pseudo-random binary sequence. The device then synchronizes to the periodic frame flag bit C0.

The status of the NICAM decoder can be read out from the NICAM status register by the user (see Section 10.4.2). The OSB bit indicates that the decoder has locked to the NICAM data. The VDSP bit indicates that the decoder has locked to the NICAM data and that the data is valid sound data. The C4 bit indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel.

The error byte contains the number of sound sample errors (resulting from parity checking) that occurred in the past 128 ms period. The Bit Error Rate (BER) is approximately 0.0000174 times the contents of the error byte:

$$\mathrm{BER} = \frac{\text{bit errors}}{\text{total bits}} \approx \text{error byte} \times 1.74 \times 10^{-5}$$

6.1.9 NICAM AUTO-MUTE

This function is enabled by setting bit AMUTE LOW (see Section 10.3.12). Upper and lower error limits may be defined by writing appropriate values to two registers in the I^2C-bus section (see Sections 10.3.14 and 10.3.15). When the number of errors in a 128 ms period exceeds the upper error limit, the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM or AM) or to the analog mono input. When the error count is smaller than the lower error limit, the NICAM sound is restored.

The auto-mute function can be disabled by setting bit AMUTE HIGH. In this case clicks become audible when the error count increases. The user will hear a signal of degrading quality.

If no NICAM sound is received, the outputs are switched from the NICAM channel to the 1st sound carrier.

A decision to enable or disable the auto-mute is taken by the microprocessor based on an interpretation of the application control bits C1, C2, C3 and C4, and possibly any additional strategy implemented by the user in the microcontroller software.

When the AM sound in NICAM L systems is demodulated in the 1st sound IF and the audio signal connected to the mono input of the TDA9874A, the controlling microprocessor has to ensure switching from NICAM reception to mono input, if auto-muting is desired. This can be achieved by setting the AMSEL bit HIGH and the AMUTE bit LOW (see Section 10.3.12).

6.1.10 CRYSTAL OSCILLATOR

The digital controlled crystal oscillator (DCXO) is fully integrated. Only an external 24.576 MHz crystal is required.

6.1.11 TEST PINS

All test pins are active HIGH. In normal operation of the device they can be left open-circuit, as they have internal pull-down resistors. Test functions are for manufacturing tests only and are not available to customers.

6.1.12 POWER FAIL DETECTOR

The power fail detector monitors the internal power supply for the digital part of the device. If the supply has temporarily been lower than the specified lower limit, the power failure register bit PFR in subaddress 0 (see Section 10.4.1), will be set to HIGH. The CLRPFR bit, slave register subaddress 1 (see Section 10.3.3), resets the Power-on reset flip-flop to LOW. If this is detected, an initialization of the TDA9874A has to be performed to ensure reliable operation.

6.1.13 POWER-ON RESET

The reset is active LOW. In order to perform a reset at power-up, a simple RC circuit may be used which consists of an integrated passive pull-up resistor and an external capacitor connected to ground. The pull-up resistor has a nominal value of 50 kΩ, which can easily be measured between pins CRESET and V_{DDD3}. Before the supply voltage has reached a certain minimum level, the state of the circuit is completely undefined and remains in this undefined state until a reset is applied.

The reset is guaranteed to be active when:

- The power supply is within the specified limits (4.5 to 5.5 V)
- The crystal oscillator (DCXO) is functioning
- The voltage at pin CRESET is below $0.3V_{DDD}$ (1.5 V if V_{DDD} = 5.0 V, typically below 1.8 V).

The required capacitor value depends on the gradient of the rising power supply voltage. The time constant of the RC circuit should be clearly larger than the rise time of the power supply [to make sure that the reset condition is always satisfied (see Fig.4)], even when considering tolerance spreading. To avoid problems with a too slow discharging of the capacitor at power-down, it may be helpful to add a diode from the CRESET pin to V_{DDD}.

It should be noted that the internal ESD protection diode does not help here as it only conducts at higher voltages. Under difficult power supply conditions (e.g. very slow or non-monotonic ramp-up), it is recommended to drive the reset line from a microcontroller port or the like.

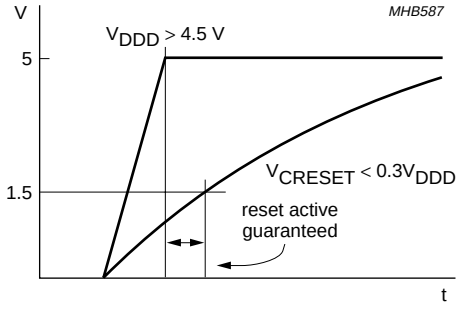


Fig.4 Reset at power-on.

6.2 Description of the DSP

6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch are equipped with a level adjustment facility to change the signal level in a range of ±15 dB. Adjusting the signal level is intended to compensate for the different modulation parameters of the various TV standards. Under nominal conditions it is recommended to scale all input channels to be 15 dB below full-scale [–15 dB (FS)]. This will create sufficient headroom to cope with overmodulation and avoids changes of the volume impression when switching from FM to NICAM or vice versa.

6.2.2 NICAM PATH

The NICAM path has a switchable J17 de-emphasis.

6.2.3 NICAM AUTO-MUTE

If NICAM is received, the auto-mute is enabled and the signal quality becomes poor. The digital crossbar switches automatically to FM, channel 1 or the analog mono input, as selected by bit AMSEL. This automatic switching depends on the NICAM bit error rate. The auto-mute function can be disabled via the I^2C-bus.

6.2.4 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator that may occur due to carrier frequency offsets, and supplies the FM monitor function with DC values, e.g. for the purpose of microprocessor controlled carrier search or fine tuning functions.

An adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

The de-emphasis stage offers a choice of settings for the supported TV standards.

The 2-channel decoder performs the dematrixing of $\frac{1}{2}$(L + R), R to L and R signals of $\frac{1}{2}$(L + R) and $\frac{1}{2}$(L – R) to L and R signals or of channel 1 and channel 2 to L and R signals, as demanded by the different TV standards or user preferences.

Automatic FM dematrixing is also supported.

Using the high deviation mode, only channel 1 (mono) can be demodulated. The scaling is –6 dB compared to 2-channel decoding.

6.2.5 MONITOR

This function provides data words from the FM demodulator outputs and FM and NICAM signals for external use, such as carrier search or fine tuning. The peak level of these signals can also be observed. Source selection and data read-out are performed via the I^{2}C-bus.

6.2.6 DIGITAL CROSSBAR SWITCH

The input channels are derived from the FM and NICAM paths, while the output channels comprise I^{2}S-bus and the audio DACs to the analog crossbar switch. It should be noted that there is no connection from the external analog audio inputs to the digital crossbar switch.

6.2.7 DIGITAL AUDIO OUTPUT

The digital audio output interface comprises an I^{2}S-bus output port and a system clock output. The I^{2}S-bus port is equipped with a level adjustment facility that can change the signal level in a ±15 dB range in 1 dB steps. Muting is possible, too, and outputs can be disabled to improve EMC performance.

The I^{2}S-bus output matrix provides the functions for forced mono, stereo, channel swap, channel 1 or channel 2.

Automatic selection for TV applications is possible. In this case the microcontroller program only has to provide a user controlled sound A or sound B selection.

6.2.8 STEREO CHANNEL TO THE ANALOG CROSSBAR PATH

A level adjustment function is provided with control positions of 0, 3, 6 and 9 dB in combination with the audio DACs. The Automatic Volume Level (AVL) function provides a constant output level of –20 dB (FS) for input levels between 0 and –26 dB (FS). There are some fixed decay time constants to choose from, i.e. 2, 4 or 8 s.

Automatic selection for TV applications is possible. In this case the microcontroller program only has to provide a user controlled sound A or sound B selection.

6.2.9 GENERAL

The level adjustment functions can provide signal gain at multiple locations. Great care has to be taken when using gain with large input signals, e.g., due to overmodulation, in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full-scale, i.e., –15 dB (FS).

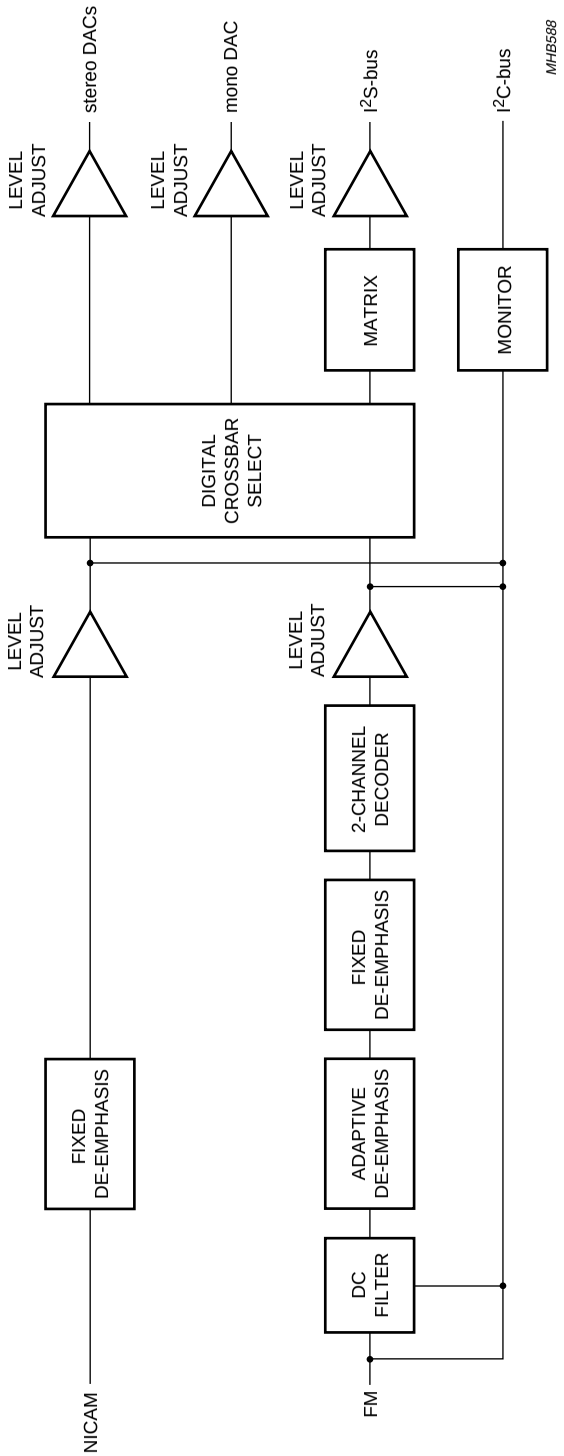


Fig.5 DSP data flow diagram.

6.3 Description of the analog audio section

6.3.1 Analog crossbar switch and analog matrix

The TDA9874A has one external analog stereo input, one mono input, one 2-channel and one single-channel output port. Analog source selector switches are employed to provide the desired analog signal routing capability, which is done by the analog crossbar switch section.

The basic signal routing philosophy of the TDA9874A is that each switch handles two signal channels at the same time (e.g. left and right, language A and B) directly at the source. For an overview of the signal flow see Fig.7.

Each source selector switch is followed by an analog matrix to perform further selection tasks, such as putting a signal from one input channel, say language A, to both output channels or for swapping left and right channels. The analog matrix provides the functions given in Table 5. Automatic matrixing for TV applications is also supported.

All switches and matrices are controlled via the I^2C-bus.

Table 5 Analog matrix functions

MODE	MATRIX OUTPUT	
	L OUTPUT	R OUTPUT
1	L input	R input
2	R input	L input
3	L input	L input
4	R input	R input

6.3.2 External and mono inputs

The external and mono inputs accept signal levels of up to 1.4 V (RMS). By adding external series resistors to provide suitable attenuation, the external input could be used as a SCART input. Whenever the external or mono input is selected, the output of the DAC is muted to improve the crosstalk performance.

6.3.3 Audio DACs

The TDA9874A comprises a 2-channel audio DAC and an additional single-channel audio DAC for feeding signals from the DSP section to the analog crossbar switch. These DACs have a resolution of 15 bits and employ four-times oversampling and noise shaping.

6.3.4 Audio output buffers

The output buffers provide a gain of 0 dB and offer a muting possibility. The post filter capacitors of the audio DACs are connected to the buffer outputs.

6.3.5 Standby mode

The standby mode (see Section 10.3.3) disables most functions and reduces power dissipation of the TDA9874A. It provides no other function.

Internal registers may lose their information in standby mode. Therefore, the device needs to be initialized on returning to normal operation. This can be accomplished in the same way as after a Power-on reset.

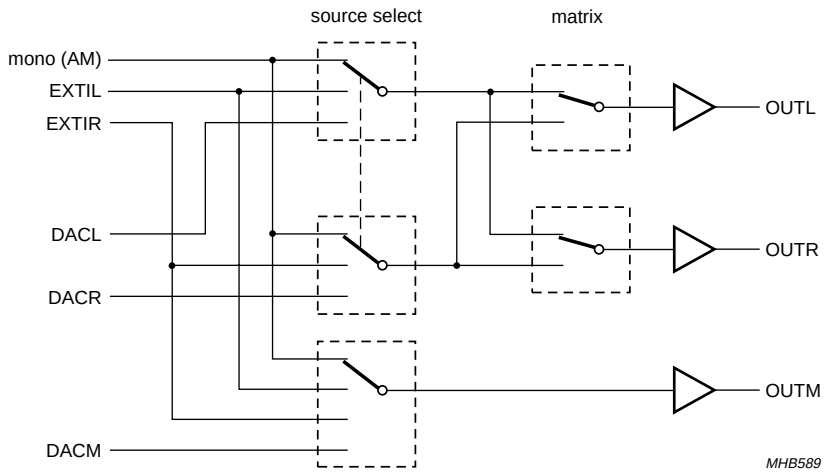


Fig.6 Switch diagram for the analog audio section.

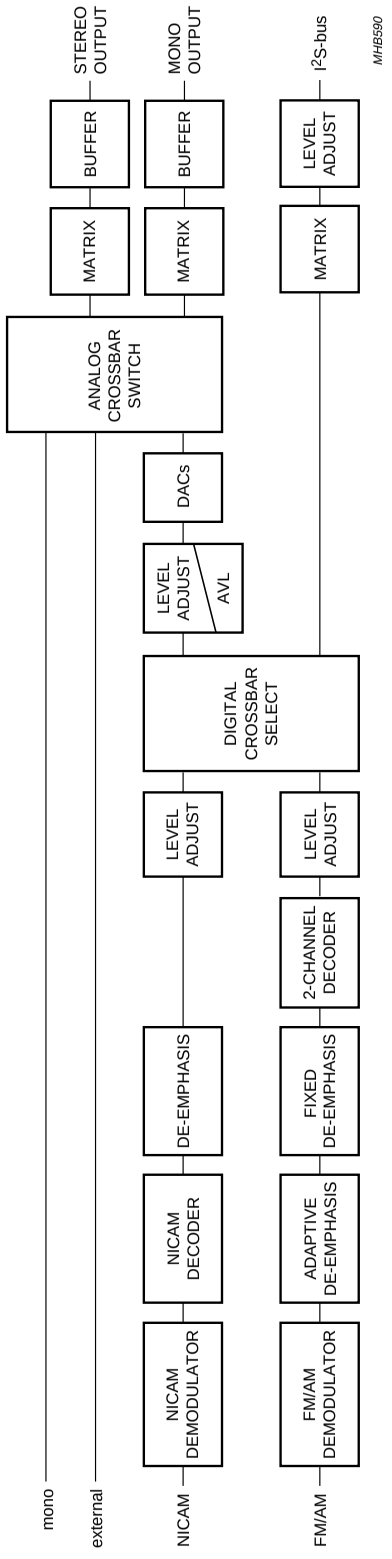


Fig.7 Audio signal flow.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDx}	DC supply voltage		–0.5	+6.5	V
ΔV_{DDx}	voltage differences between two V_{DDx} pins		–	550	mV
I_{IK}	DC input clamp diode current	$V_i < -0.5$ V or $V_i > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamp diode current output type 4 mA	$V_o < -0.5$ V or $V_o > V_{DD} + 0.5$ V	–	±20	mA
I_O	DC output source or sink current output type 4 mA	-0.5 V $< V_O < V_{DDx} + 0.5$ V	–	±20	mA
I_{DDD}, I_{SSD}	DC V_{DDD} or V_{SSD} current per digital supply pin		–	±96	mA
I_{DDA}, I_{SSA}	DC V_{DDA} or V_{SSA} current per analog supply pin		–	±50	mA
$I_{lu(prot)}$	latch-up protection current		100	–	mA
P/out	power dissipation per output		–	100	mW
P_{tot}	total power dissipation		–	0.75	W
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	note 1	2000	–	V
		note 2	200	–	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ.
2. Machine model: C = 200 pF; L = 0.75 μH; R = 0 Ω.

8 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

9 CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; settings in accordance with B/G standard; FM deviation ±50 kHz; f_{mod} = 1 kHz; FM sound parameters in accordance with system A2; NICAM in accordance with *"EBU NICAM 728 specification"*; 1 kΩ measurement source resistance for AF inputs; V_{SIF} = 300 mV (p-p); AGCOFF = 0; AGCSLOW = 1; level and gain settings according to note 1 with external components of Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital supplies						
V_{DDD1}	digital supply voltage 1		4.5	5.0	5.5	V
V_{SSD1}	digital ground supply 1		–	0.0	–	V
I_{DDD1}	digital supply current 1	V_{DDD1} = 5.5 V	40	59	74	mA
		V_{DDD1} = 5.0 V	42	59	75	mA
V_{SSD2}	digital ground supply 2		–	0.0	–	V
V_{DDD3}	digital supply voltage 3		4.5	5.0	5.5	V
V_{SSD3}	digital ground supply 3		–	0.0	–	V
I_{DDD3}	digital supply current 3	V_{DDD3} = 5.5 V; SYSCLK off	9	17	21	mA
		V_{DDD3} = 5.0 V; SYSCLK off	8	16	20	mA
Power failure register						
V_{pfr}	power failure response voltage		–	4.0	–	V
Demodulator supplies and references						
V_{DDA3}	analog supply voltage 3, demodulator part		4.5	5.0	5.5	V
V_{SSA3}	analog ground supply 3, demodulator part		–	0.0	–	V
I_{DDA3}	analog supply current 3, demodulator part	V_{DDA3} = 5.5 V	24	32	40	mA
		V_{DDA3} = 5.0 V	24	32	40	mA
V_{DEC1}	analog supply decoupling voltage for front-end		–	3.3	–	V
V_{SSA2}	analog ground supply 2		–	0.0	–	V
V_{ref1}	analog reference voltage, demodulator part		–	2	–	V
$I_{ref1(sink)}$	V_{ref1} sink current		–	200	–	µA
Audio supplies and references						
V_{DDA1}	analog supply voltage 1, operational amplifiers		4.5	5.0	5.5	V
V_{SSA1}	analog ground supply 1, operational amplifiers		–	0.0	–	V
I_{DDA1}	analog supply current 1, operational amplifiers	V_{DDA1} = 5.5 V	3	6	10	mA
		V_{DDA1} = 5.0 V	3	5	10	mA
V_{SSA4}	analog ground supply 4, audio DAC part		–	0.0	–	V
V_{ref2}	reference voltage 2, audio DACs and operational amplifiers	referenced to V_{DDA1} and V_{SSA1}	–	50	–	%
$Z_{(Vref2-VDDA3)}$	impedance V_{ref2} to V_{DDA3}		–	20	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{(Vref2-VSSA3)}$	impedance V_{ref2} to V_{SSA3}		–	20	–	kΩ
Digital inputs and outputs						
INPUTS						
CMOS level input, high drive, pull-down (pins TEST1, TEST2, TP1 and TP2)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
CMOS level input, hysteresis, high drive, pull-up (pin CRESET)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	1.3	–	V
C_i	input capacitance		–	–	10	pF
Z_i	input impedance		–	50	–	kΩ
INPUTS/OUTPUTS						
I^2C-bus level input with Schmitt trigger, open-drain output stage (pins SCL and SDA)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.05V_{DDD}$	–	V
I_{LI}	input leakage current		–	–	±10	µA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage		–	–	0.6	V
C_L	load capacitance		–	–	400	pF
TTL/CMOS level, high drive, 4 mA 3-state output stage, pull-up (pins PCLK, NICAM, ADDR1, ADDR2, P1, P2, SCK, WS and SDO)						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –3 mA	2.4	–	–	V
C_L	load capacitance	active pull-up	–	–	100	pF
Z_i	input impedance		–	50	–	kΩ
OUTPUTS						
4 mA 3-state output stage (pin SYSCLK)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	$0.3V_{DDD}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	$0.7V_{DDD}$	–	–	V
C_L	load capacitance		–	–	100	pF
$I_{LO(Z)}$	3-state leakage current	V_i = 0 to V_{DDD}	–	–	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIF1 and SIF2 analog inputs						
$V_{SIF(max)(p-p)}$	maximum composite SIF input voltage before clipping (peak-to-peak value)	SIF input level adjustment 0 dB	–	941	–	mV
		SIF input level adjustment −10 dB	–	2976	–	mV
$V_{SIF(min)(p-p)}$	minimum composite SIF input voltage for lower limit of AGC (peak-to-peak value)	SIF input level adjustment 0 dB	–	59	–	mV
		SIF input level adjustment −10 dB	–	188	–	mV
AGC	AGC range		–	24	–	dB
f_i	input frequency		4	–	9.2	MHz
R_i	input resistance	AGCLEV = 0	10	–	–	kΩ
C_i	input capacitance		–	7.5	11	pF
Δf_{FM}	FM deviation	B/G standard; THD < 1%	±100	–	–	kHz
$\Delta f_{FM(FS)}$	FM deviation full-scale level	terrestrial FM; level adjustment 0 dB; demodulator filter bandwidth set to narrow	±150	–	–	kHz
$\Delta f_{FM(max)}$	maximum FM deviation in high deviation mode	B/G standard; THD < 1%; demodulator filter bandwidth set to extra wide	±335	–	–	kHz
C/N_{FM}	FM carrier-to-noise ratio	N_{FM} bandwidth = 6 MHz; white noise for S/N = 40 dB; *"CCIR468-2"*; quasi peak	–	77	–	$\frac{dB}{Hz}$
C/N_N	NICAM carrier-to-noise ratio	N_N bandwidth = 6 MHz; bit error rate = 10^{-3}; white noise	–	66	–	$\frac{dB}{Hz}$
α_{ct}	crosstalk attenuation SIF1 to SIF2	f_i = 4 to 9.2 MHz	50	–	–	dB
Demodulator performance						
$V_{o(nom)(rms)}$	nominal level output voltage (RMS value)	note 1	400	500	600	mV
THD + N	total harmonic distortion plus noise	from FM source to any output; f_i = 1 kHz; bandwidth 20 Hz to 20 kHz; V_o = 1 V (RMS)	–	0.3	0.5	%
		from NICAM source to any output; f_i = 1 kHz; bandwidth 20 Hz to 20 kHz; V_o = 1 V (RMS)	–	0.1	0.3	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	V_o = 1 V (RMS); *"CCIR468-2"*; quasi peak				
		SC1 from FM source to any output	64	70	–	dB
		SC2 from FM source to any output	60	66	–	dB
		SC1 during use of high deviation mode from FM source to any output	62	68	–	dB
		NICAM source	NICAM in accordance with *"EBU specification"*; note 2			
$B_{(-3dB)}$	−3 dB bandwidth	from FM source to any output	14.5	15	–	kHz
		from NICAM source to any output	14.5	15	–	kHz
f_{resp}	frequency response 20 Hz to 14 kHz	from FM/NICAM to any output; reference 1 kHz	−2	–	+1	dB
$\alpha_{cd(dual)}$	dual signal channel separation	note 3	65	70	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	note 4	40	45	–	dB
α_{AM}	AM suppression for FM	AM: 1 kHz, 30% modulation; reference: f_i = 1 kHz; 50 kHz deviation	50	–	–	dB
dm_{AM}	AM demodulation	SIF level 100 mV (RMS); 54% AM; 1 kHz AF; *"CCIR468-2"*; quasi peak	36	45	–	dB
IDENTIFICATION FOR FM SYSTEMS						
$m_{pilot(ident)}$	pilot modulation for identification		25	50	75	%
$C/N_{pilot(ident)}$	pilot sideband C/N for identification start		–	27	–	$\frac{dB}{Hz}$
$hys_{(tun)}$	hysteresis		–	–	2	dB
f_{ident}	identification window	B/G stereo				
		slow mode	116.85	–	118.12	Hz
		medium mode	116.11	–	118.89	Hz
		fast mode	114.65	–	120.46	Hz
		B/G dual				
		slow mode	273.44	–	274.81	Hz
		medium mode	272.07	–	276.20	Hz
		fast mode	270.73	–	277.60	Hz
$t_{on(ident)}$	total identification time on	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{off(ident)}$	total identification time off	slow mode	–	–	2	s
		medium mode	–	–	1	s
		fast mode	–	–	0.5	s
Mono and external inputs						
$V_{i(nom)(rms)}$	nominal level input voltage (RMS value)	note 1	–	500	–	mV
$V_{i(cl)(rms)}$	clipping level input voltage (RMS value)	THD < 3%; note 5	1250	1400	–	mV
R_i	input resistance	note 5	28	35	42	kΩ
Analog audio outputs						
$V_{o(clip)(rms)}$	clipping level output voltage (RMS value)	THD < 3%	1400	–	–	mV
R_o	output resistance		150	250	375	Ω
$R_{L(AC)}$	AC load resistor		10	–	–	kΩ
$R_{L(DC)}$	DC load resistor		10	–	–	kΩ
$C_{o(L)}$	output load capacitor		–	10	12	nF
$V_{offset(DC)}$	static DC offset voltage		–	30	70	mV
α_{mute}	mute suppression	nominal input signal from any source; f_i = 1 kHz; note 1	80	–	–	dB
B_{line}	bandwidth	from external and mono source; –3 dB bandwidth	20	–	–	kHz
G_{ro}	roll-off gain at 14.5 kHz	from any source	–3	–2	–	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; V_{ripple} = 100 mV (peak); C_{Vref} = 47 µF; signal from I^2S-bus	40	45	–	dB
Audio performance						
THD + N	total harmonic distortion plus noise	$V_{in/out}$ = 1 V (RMS); f_i = 1 kHz; bandwidth 20 Hz to 20 kHz; from external/mono input to output copy	–	0.1	0.3	%
S/N	signal-to-noise ratio	reference voltage V_0 = 1.4 V (RMS); f_i = 1 kHz; *"CCIR468-2"*; quasi peak; from external or mono input to output copy	78	90	–	dB
α_{ct}	crosstalk attenuation	between any analog input pairs; f_i = 1 kHz	70	–	–	dB
α_{cs}	channel separation	between left and right of external input pair	65	–	–	dB
		between left and right of output pair	60	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal specification (fundamental mode)						
f_{xtal}	crystal frequency	note 6	–	24.576	–	MHz
C_L	load capacitance		–	20	–	pF
C_1	series capacitance		–	20	–	fF
C_0	parallel capacitance		–	–	7	pF
Φ_{pull}	pulling sensitivity	C_L changed from 18 to 16 pF	–	25	–	$\frac{10^{-6}}{pF}$
R_R	equivalent series resistance	at nominal frequency	–	–	30	Ω
R_N	equivalent series resistance of unwanted mode		$2R_R$	–	–	Ω
ΔT	temperature range		–20	+25	+70	°C
X_J	adjustment tolerance		–	–	±30	10^{-6}
X_D	drift	across temperature range	–	–	±30	10^{-6}
X_A	ageing		–	–	±5	$\frac{10^{-6}}{year}$

Notes

1. Definition of levels and level setting:
   a) The full-scale level for analog audio signals is V_{FS} = 1.4 V (RMS). The nominal level at the digital crossbar switch is defined at –15 dB (FS).
   b) Nominal audio input levels: external, mono: 500 mV; –9 dB (FS).
2. Audio performance is limited by the dynamic range of the NICAM 728 system. Due to companding, the quantization noise is never lower than –62 dB with respect to the input level.
3. FM source; in dual mode only A (respectively B) signal modulated; measured at B (respectively A) channel output; V_o = 1 V (RMS) of modulated channel.
4. FM source; in stereo mode only L (respectively R) signal modulated; measured at R (respectively L) channel output; V_o = 1 V (RMS) of modulated channel.
5. If the supply voltage for the TDA9874A is switched off, because of the ESD protection circuitry, all audio input pins are short-circuited.
6. The Philips crystal (order number 9922 520 20106) is suitable for this application.

Table 6 Level setting FM, AM and NICAM

0 dB (FS) = 1.4 V (RMS); FS = full-scale.

SOURCE	TRANSMITTER NOMINAL MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	LEVEL ADJUSTMENT SETTING	NOMINAL LEVEL AT CROSSBAR	DAC GAIN SETTING	NOMINAL OUTPUT VOLTAGE V_O
FM M standard	15 kHz deviation	–24 dB (FS)	+9 dB	–15 dB (FS) (spread of ±0.5 dB due to different transmitter references)	+6 dB	500 mV (RMS)
FM B/G, D/K, I standard	27 kHz deviation	–19 dB (FS)	+4 dB			
AM L/L accent standard	54%	–19 dB (FS)	+4 dB			
NICAM B/G, D/K, L standard	–11.2 dB (FS)	–18 dB (FS)	+3 dB			
NICAM I standard	–15.8 dB (FS)	–23 dB (FS)	+8 dB			

Table 7 Level setting SAT FM

0 dB (FS) = 1.4 V (RMS); FS = full-scale.

SOURCE	TRANSMITTER MAXIMUM MODULATION DEPTH	NOMINAL LEVEL AT DEMODULATOR OUTPUT	LEVEL ADJUSTMENT SETTING	MAXIMUM LEVEL AT CROSSBAR	DAC GAIN SETTING	MAXIMUM OUTPUT VOLTAGE V_O
SAT FM stereo	50 kHz deviation	–13 dB (FS)	+4 dB	–9 dB (FS)	+6 dB	1 V (RMS)
SAT FM mono	85 kHz deviation	–9 dB (FS)	0 dB			

10 I²C-BUS CONTROL

10.1 Introduction

The TDA9874A is controlled only via the I²C-bus. Control is exercised by writing data to one or more internal registers. Status information can be read from an array of registers to let the controlling microprocessor determine whether any action is required.

The device has an I²C-bus slave transceiver in accordance with the fast-mode specification with a maximum speed of 400 kbits/s. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011). To avoid conflicts in a real application with other ICs providing similar or complementing functions, there are four possible slave addresses available, which can be selected by pins ADDR1 and ADDR2 (see Table 8).

Table 8 Possible slave addresses

ADDR2	ADDR1	SLAVE ADDRESS						
		A6	A5	A4	A3	A2	A1	A0
0	0	1	0	1	1	0	0	0
0	1	1	0	1	1	0	0	1
1	0	1	0	1	1	0	1	0
1	1	1	0	1	1	0	1	1

The I²C-bus interface remains operational in the standby mode of the TDA9874A to allow the device to be reactivated via the I²C-bus.

The device will not respond to a 'general call' on the I²C-bus, i.e. when a slave address of 0000 000 is sent by a master.

10.2 Power-up state

After power-on reset respectively at power-up the device is in the following state:

- All outputs muted
- No sound carrier frequency loaded
- General purpose I/O pins ready for input (HIGH)
- Input SIF1 selected with:
  - AGC on
  - SIF 10 dB attenuator off
  - Small hysteresis.
- Demodulators for both sound carriers set to FM with:
  - Identification for B/G, D/K, identification mode 'slow'
  - Level adjustment set to 0 dB
  - De-emphasis 50 μs
  - Dematrix set to mono
  - Adaptive de-emphasis off.
- Analog outputs are muted and connected to DACs
- Digital audio interface all outputs off
- Monitor set to carrier 1 DC output.

After power-on reset/power-up a device initialization has to be performed via the I²C-bus to put the TDA9874A into the proper mode of operation, in accordance with the desired TV standard, etc. This can be done by writing to all registers with a single I²C-bus transmission (such as a refresh operation) or by writing selectively only to those registers, the contents of which need to be changed with regard to the power-up state. Easy Standard Programming (ESP) can also be used.

10.3 Slave receiver mode

As a slave receiver, the TDA9874A provides 26 registers for storing commands and data. Each register is accessed via a so-called subaddress. A subaddress can be thought of as a pointer to an internal memory location.

Detailed descriptions of the slave receiver registers are given in Sections 10.3.2 to 10.3.21.

It is allowed to send more than one data byte per transmission to the TDA9874A. In this event, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each byte that is properly stored, is acknowledged with A (acknowledge). If an attempt is made to write data to a non-existing subaddress, the device acknowledges with NA (not acknowledge), therefore telling the I^{2}C-bus master to abort the transmission. There is no ‘wrap-around’ of subaddresses.

Commands and data will be processed as soon as they have been received completely. Functions requiring more than one byte will thus be executed only after all bytes for that function have been received. If the transmission is terminated (STOP condition) before all bytes have been received, the incomplete data for that function is ignored.

Data patterns sent to the various subaddresses are not checked for being illegal or not at that address, except for the level adjustment functions.

Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. In this case, the last operation will not be executed.

Table 9 I^{2}C-bus; slave address/subaddress/data format

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA	A/NA	P

Table 10 Explanation of Table 9

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
A/NA	acknowledge or not acknowledge
P	STOP condition

Table 11 Format for a transmission employing auto-increment of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA BYTE A n data bytes with auto-increment of subaddresses	DATA	A/NA	P

10.3.1 Programming via the I^{2}C-bus

The TDA9874A can be programmed in the same way as its predecessor (TDA9874H) using the subaddresses 0 to 24 or by using ESP.

10.3.1.1 Programming via subaddresses 0 to 24

While programming the TDA9874A, by writing to subaddresses 0 to 24, it is not allowed to access subaddress 255. Writing data to subaddress 255 will overwrite the data previously written to subaddresses 3 to 10. This may cause unwanted effects.

10.3.1.2 Using Easy Standard Programming (ESP)

This facility simplifies programming by reducing the amount of data to be set-up and transferred via the I^2C-bus.

Subaddress 255 gives control of most standard dependent settings of the IC; see ESP register in Section 10.3.23.

When using ESP it is recommended not to write data to subaddresses 3 to 10.

A possible programming flow for using ESP and automatic FM dematrixing (TVSM = 1 and IDSWFM = 1) is shown in Table 12. It should be noted that the NICAM configuration register and the level adjustment registers for FM and NICAM are not affected by ESP.

Table 12 Programming the TDA9874A by using ESP and automatic FM dematrixing

REGISTER		CONTENT OF REGISTER
NUMBER	NAME	
0	AGCCGR	set AGCGR = 20H for using the −10 dB attenuator at the SIF input, otherwise write a 00H to this register
1	GCONR	select the chosen SIF input pin by writing data to bit SIFSEL (bit 0) and choose the AGC decay time corresponding to your application by writing the appropriate data to bit AGCSLOW (bit 2)
2	MSR	set this register according to your sound mode detection algorithm
3 to 10	–	do NOT write data to these registers while using ESP
11	FMMR	set FMMR = 80H to choose automatic FM dematrixing
12	C1OLAR	see Table 38
13	C2OLAR	see Table 39
14	NCONR	set NCONR = 04H to select FM source automatically if NICAM is not available
15	NOLAR	see Table 42
16	NLELR	set NLELR = 14H (default setting after Power-on reset) if no other value is chosen
17	NUELR	set NUELR = 50H (default setting after Power-on reset) if no other value is chosen
18	AMCONR	set AMCONR = F9H to enable all analog outputs
19	SDACOSR	Set SDACOSR = 81H to select +6 dB gain (see Table 48) and NICAM or FM output.
20	AOSR	To select an internal source set AOSR = 80H to select dual A or set AOSR = C0H to select dual B (if dual mode is transmitted) to all analog outputs. For selecting an external source see Section 10.3.18.
21	DAICONR	use only for I^2S-bus output, see detailed description in Section 10.3.19
22	I^2SOSR	use only for I^2S-bus output, see detailed description in Section 10.3.20
23	I^2SOLAR	use only for I^2S-bus output, see detailed description in Section 10.3.21
24	MDACOSR	Set MDACOSR = 82H to select dual A or set MDACOSR = 83H to select dual B (if dual mode is transmitted) to all analog outputs. For selecting an external source see Section 10.3.22.
255	ESP	see detailed description in Section 10.3.23

Table 13 Overview of the slave receiver registers

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
0	0	0	AGCLEV	B4	B3	B2	B1	B0	AGC gain selection (ignored, if AGC on)
1	P2OUT	P1OUT	STDBY	INIT	CLRPFR	AGCSLOW	AGCOFF	SIFSEL	general configuration
2	PEAK	0	0	MCSM1	MCSM0	0	MSS1	MSS0	monitor select
3	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; MS part
4	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency
5	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; LS part
6	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency; MS part
7	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency
8	B7	B5	B5	B4	B3	B2	B1	B0	carrier 2 frequency; LS part
9	IDMOD1	IDMOD0	IDAREA	FILTBW1	CH2MOD1	CH2MOD0	FILTBW0	CH1MODE	demodulator configuration
10	ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11	FM de-emphasis
11	IDSWFM	0	0	0	0	FDMS2	FDMS1	FDMS0	FM dematrix
12	0	0	0	B4	B3	B2	B1	B0	channel 1 output level adjustment
13	0	0	0	B4	B3	B2	B1	B0	channel 2 output level adjustment
14	DCXOPULL	DCXOTEST	0	DOUTEN	0	AMSEL	NDEEM	AMUTE	NICAM configuration
15	0	0	0	B4	B3	B2	B1	B0	NICAM output level adjustment
16	B7	B6	B5	B4	B3	B2	B1	B0	NICAM lower error limit

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
17	B7	B6	B5	B4	B3	B2	B1	B0	NICAM upper error limit
18	1	MUTI2S	1	1	1	MUTSOUT	MUTMOUT	1	audio mute control
19	SDGS1	0	AVL1	AVL0	SDGS0	0	SDOS1	SDOS0	stereo DAC output select
20	TVSM	CSM2	CSM1	CSM0	MOS1	MOS0	SSS1	SSS0	analog output select
21	0	0	0	SYSCL1	SYSCL0	SYSOUT	I2SFORM	IS2OUT	digital audio interface configuration
22	TVSMIIS	ICSM2	ICSM1	ICSM0	0	0	ISS1	ISS0	I^2S-bus output select
23	0	0	0	B3	B2	B1	B0	B0	I^2S-bus output level adjustment
24	MDGS1	0	0	0	MDGS0	0	MDOS1	MDOS0	mono DAC output select
25	0	0	0	0	0	0	0	0	reserved
255	FILTBW1	FILTBW0	IDMOD1	IDMOD0	EPB3	EPB2	EPB1	EPB0	ESP

10.3.2 AGC GAIN REGISTER (AGCGR)

If the Automatic Gain Control (AGC) function is switched off in the general configuration register (see Section 10.3.3) the contents of this register defines a fixed gain of the SIF input stage. The input voltages given are meant to generate a nearly full-scale output from the SIF ADC. If the AGC is on, the AGC gain setting is ignored. After switching off the AGC function, the latest gain control setting is copied to the AGC gain register. If the AGC input level shift bit (AGCLEV) is set to HIGH the input signal is scaled with −10 dB. The AGCLEV bit is also active if the AGC function is enabled.

The default setting after power-on reset is ‘0000 0000’.

In Table 16 the stated step number corresponds with the SIF level read from subaddress 7 (see Section 10.4.6); the input voltages should be considered as approximate target values.

Table 14 AGC gain register (subaddress 0)

7	6	5	4	3	2	1	0
0	0	AGCLEV	AGCB4	AGCB3	AGCB2	AGCB1	AGCB0

Table 15 Description of the AGCGR bits

BIT	NAME	DESCRIPTION
7	–	this bit is not used and should be set to a logic 0
6	–	this bit is not used and should be set to a logic 0
5	AGCLEV	If the AGC input level shift bit AGCLEV is set to HIGH the input signal is scaled with −10 dB. The AGCLEV bit is also active if the automatic gain function is enabled.
4	AGCB4	If the automatic gain control function is switched off in the general configuration register, the contents of this register will define a fixed gain of the AGC stage.
3	AGCB3	
2	AGCB2	
1	AGCB1	
0	AGCB0	

Table 16 AGC gain register

7	6	5	4	3	2	1	0	AGC GAIN (dB)	MAX. SIF INPUT VOLTAGE (mV; RMS)
–	–	AGCLEV	AGCB4	AGCB3	AGCB2	AGCB1	AGCB0		
0	0	0/1	1	1	1	1	1	0.0	333/1052
0	0	0/1	1	1	1	1	0	0.8	304/963
0	0	0/1	1	1	1	0	1	1.5	278/881
0	0	0/1	1	1	1	0	0	2.3	255/806
0	0	0/1	1	1	0	1	1	3.1	233/737
0	0	0/1	1	1	0	1	0	3.9	213/674
0	0	0/1	1	1	0	0	1	4.6	195/617
0	0	0/1	1	1	0	0	0	5.4	178/564
0	0	0/1	1	0	1	1	1	6.2	163/516
0	0	0/1	1	0	1	1	0	7.0	149/472
0	0	0/1	1	0	1	0	1	7.7	136/432
0	0	0/1	1	0	1	0	0	8.5	125/395
0	0	0/1	1	0	0	1	1	9.3	114/361
0	0	0/1	1	0	0	1	0	10.1	104/330
0	0	0/1	1	0	0	0	1	10.8	96/302
0	0	0/1	1	0	0	0	0	11.6	87/276
0	0	0/1	0	1	1	1	1	12.4	80/253
0	0	0/1	0	1	1	1	0	13.2	73/231
0	0	0/1	0	1	1	0	1	13.9	67/212
0	0	0/1	0	1	1	0	0	14.7	61/194
0	0	0/1	0	1	0	1	1	15.5	56/177
0	0	0/1	0	1	0	1	0	16.3	51/162
0	0	0/1	0	1	0	0	1	17.0	47/148
0	0	0/1	0	1	0	0	0	17.8	43/135
0	0	0/1	0	0	1	1	1	18.6	39/124
0	0	0/1	0	0	1	1	0	19.4	36/113
0	0	0/1	0	0	1	0	1	20.1	33/104
0	0	0/1	0	0	1	0	0	20.9	30/95
0	0	0/1	0	0	0	1	1	21.7	27/87
0	0	0/1	0	0	0	1	0	22.5	25/79
0	0	0/1	0	0	0	0	1	23.2	23/73
0	0	0/1	0	0	0	0	0	24.0	21/66

10.3.3 General Configuration Register (GCONR)

The default setting after power-on reset is ‘1100 0000’.

Table 17 General configuration register (subaddress 1)

7	6	5	4	3	2	1	0
P2OUT	P1OUT	STDBY	INIT	CLRPFR	AGCSLOW	AGCOFF	SIFSEL

Table 18 Description of the GCONR bits

BIT	SYMBOL	DESCRIPTION
7	P2OUT	**General purpose I/O pins 1 and 2:** these bits control the general purpose input/output pins. The contents of these bits is written directly to the corresponding pins. If an input is desired, the bits must be set HIGH to allow the pins to be pulled LOW externally. Input from the pins is reflected in the device status register (see Section 10.4.1). P1OUT is recommended to be used for switching an SIF trap for the adjacent picture carrier in designs that employ such a trap.
6	P1OUT	
5	STDBY	**Standby mode on/off:** when STDBY = 1 the TDA9874A is set to the standby mode. Most functions are disabled and power dissipation is somewhat reduced. When STDBY = 0, the TDA9874A is in its normal mode of operation. On return from standby mode, the device is in its Power-on reset mode and needs to be reinitialized with data defined by the user.
4	INIT	**Initialize to default settings:** when INIT = 1 it causes initialization of TDA9874A to its default settings. This has the same effect as a Power-on reset. In the event of a conflict between the default settings and any bit set HIGH in this register, the bits actually written to this register will overwrite the default settings. This bit is automatically reset to LOW after initialization has been completed. When set LOW, the TDA9874A is in its normal mode of operation.
3	CLRPFR	**Clear power failure register:** when CLRPFR = 1 it resets the clear power failure register. This bit is automatically reset to CLRPFR = 0 after bit PFR in the device status register has been read.
2	AGCSLOW	**AGC decay time:** when AGCSLOW = 1 a longer decay time and larger hysteresis are selected for input signals with strong video modulation (conventional intercarrier). This bit has only an effect, when bit AGCOFF = 0. When AGCSLOW = 0, it selects normal attack and decay times for the AGC and a small hysteresis.
1	AGCOFF	**AGC on/off:** when AGCOFF = 1 it forces the AGC block to a fixed gain as defined in the AGC gain register (see Section 10.3.2). When AGCOFF = 0, the AGC function is enabled and the contents of the AGC gain register are ignored.
0	SIFSEL	**SIF input select:** when SIFSEL = 1 it selects pin SIF2 for input (recommended for satellite tuner). When SIFSEL = 0, pin SIF1 (recommended for terrestrial TV) is selected.

10.3.4 Monitor Select Register (MSR)

This register is used to define the signal source (the level of which is to be monitored) and the signal channel. Data can be monitored e.g. before or after the DC filter at the FM/AM demodulator outputs. The peak level of signals can also be observed. The last available data sample can be read out in the I^2C-bus slave transmitter mode (see Section 10.4.5).

Phase means the differentiated phase output of the FM demodulator and is provided when the demodulator operates in FM mode. The magnitude is supplied in AM mode.

The default setting after power-on reset is ‘0000 0000’.

Table 19 Monitor select register (subaddress 2)

7	6	5	4	3	2	1	0
PEAK	0	0	MCSM1	MCSM0	0	MSS1	MSS0

Table 20 Description of the MSR bits

BIT	SYMBOL	DESCRIPTION
7	PEAK	**Peak level select:** when PEAK = 1 it selects the rectified peak level of a source to be monitored. Peak level value is reset to logic 0 after read-out (see read registers 5 and 6). After changing the monitor signal source for peak calculation it is advisable to ignore the first read-out value due to stored data from previous calculations.
6	–	these 2 bits are not used and should be set to logic 0
5	–	
4	MCSM1	**Signal channel select:** the state of these 2 bits determine which signal channel is selected; see Table 21.
3	MCSM0	
2	–	this bit is not used and should be set to logic 0
1	MSS1	**Signal source select:** the state of these 2 bits determine which signal source is selected; see Table 22.
0	MSS0	

Table 21 Signal channel selection

MCSM1	MCSM0	SIGNAL CHANNEL
0	0	$\frac{CH1 + CH2}{2}$
0	1	CH1
1	0	CH2

Table 22 Signal source selection

MSS1	MSS0	SIGNAL SOURCE
0	0	DC output of FM/AM demodulator
0	1	magnitude/phase output of FM/AM demodulator
1	0	FM/AM path output
1	1	NICAM path output

10.3.5 Carrier 1 Frequency Register (C1FR)

This register should not be used when applying ESP. Three bytes are required to define a 24-bit frequency control word to represent the sound carrier (i.e. mixer) frequency. These three bytes are stored at subaddresses 3 to 5; subaddress 3 being the high byte. Execution of the command starts only after all bytes have been received. If an error occurs, e.g. a premature STOP condition, partial data for this function is ignored. The sound carrier frequency can be calculated in accordance with the following formula:

$$data = \frac{f_{mix}}{f_{clk}} \times 2^{24}$$

where:

data = 24-bit frequency control word

f_{mix} = desired sound carrier frequency

f_{clk} = 12.288 MHz (clock frequency of mixer)

2^{24} = 16777216 (number of steps in a 24-bit word size).

Example: A 5.5 MHz sound carrier frequency will be generated by sending the following sequence of data bytes to the TDA9874A (data = 7509333 in decimal notation or 729555 in hexadecimal notation): 01110010 10010101 01010101.

The default setting after power-on reset is ‘0000 0000’ for all three bytes.

Table 23 Carrier 1 frequency register high byte (subaddress 3)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Table 24 Carrier 1 frequency register middle byte (subaddress 4)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Table 25 Carrier 1 frequency register low byte (subaddress 5)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.3.6 Carrier 2 Frequency Register (C2FR)

This register should not be used when applying ESP. The format is the same as for sound carrier 1, except subaddresses 6 to 8 are used. Subaddress 6 holds the high byte.

If the C2FR is used, it will be for either the second FM sound carrier of a terrestrial or satellite FM program or the NICAM sound carrier.

10.3.7 Demodulator Configuration Register (DCONR)

This register should not be used when applying ESP. The default setting after power-on reset is ‘0000 0000’.

Table 26 Demodulator configuration register (subaddress 9)

7	6	5	4	3	2	1	0
IDMOD1	IDMOD0	IDAREA	FILTBW1	CH2MOD1	CH2MOD0	FILTBW0	CH1MODE

Table 27 Description of the DCONR bits

BIT	SYMBOL	DESCRIPTION
7	IDMOD1	**Identification mode for FM sound:** these bits define the integrator time of the FM identification. A valid result may be expected after twice this time has expired, at the latest. The longer the time, the more reliable the identification; see Table 28.
6	IDMOD0	
5	IDAREA	**Application area for FM identification:** when IDAREA = 1 it selects the FM identification frequencies in accordance with the specification for Korea. When IDAREA = 0, frequencies for Europe are selected (B/G and D/K standard).
4	FILTBW1	selects filter bandwidth in accordance with Table 30
3	CH2MOD1	**Channel 2 receive mode:** these bits control the hardware for the second sound carrier in accordance with Table 29. The NICAM mode employs a wider bandwidth of the decimation filters than the FM mode.
2	CH2MOD0	
1	FILTBW0	selects filter bandwidth in accordance with Table 30
0	CH1MODE	**Channel 1 receive mode:** when CH1MODE = 1 it selects the hardware for the first sound carrier to operate in AM mode. When CH1MODE = 0 the FM mode is assumed. This applies to both terrestrial and satellite FM reception.

Table 28 Identification mode

IDMOD1	IDMOD0	IDENTIFICATION MODE
0	0	slow
0	1	medium
1	0	fast
1	1	off/reset, recommended during use of high deviation mode

Table 29 Channel 2 receive mode

CH2MOD1	CH2MOD0	CHANNEL 2
0	0	FM
0	1	AM
1	0	NICAM

Table 30 Filter bandwidth for channel 1 and channel 2; note 1

FILTBW1	FILTBW0	FILTER BANDWIDTH		FILTER MODES
		CHANNEL 1	CHANNEL 2	
0	0	narrow	narrow	Recommended for nominal terrestrial broadcast conditions and SAT with 2 carriers
0	1	extra wide	narrow	Recommended for highly overmodulated single FM carriers. Only channel 1 is available for FM demodulation in this mode. NICAM can still be processed on channel 2.
1	0	medium	medium	Recommended for moderately overmodulated broadcast conditions
1	1	wide	wide	Recommended for strongly overmodulated broadcast conditions

Note

1. It is recommended to switch the FM sound mode identification off whenever the received program is not a terrestrial 2-carrier sound. Switching the identification off will reset the associated hardware to a defined state.

10.3.8 FM De-emphasis Register (FMDR)

This register should not be used when applying ESP. This register is used to select the proper de-emphasis characteristics as appropriate for the standard of the received carrier. Bits 3 to 0 apply to sound carrier 1, bits 7 to 4 apply to sound carrier 2. In the event of A2 reception, both groups must be set to the same characteristics.

The default setting after power-on reset is ‘0000 0000’.

Table 31 FM De-emphasis register (subaddress 10)

7	6	5	4	3	2	1	0
ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11

Table 32 Description of the FMDR bits

BIT	SYMBOL	DESCRIPTION
7	ADEEM2	**Adaptive de-emphasis on/off sound carrier 2:** when ADEEM2 = 1 it activates the adaptive de-emphasis function (for Wegener-Panda 1 encoded programs), which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 µs. When ADEEM2 = 0, the adaptive de-emphasis is off.
6	FMDSC23	**FM de-emphasis:** the state of these 3 bits determines the FM de-emphasis for sound carrier 2; see Table 33.
5	FMDSC22	
4	FMDSC21	
3	ADEEM1	**Adaptive de-emphasis on/off sound carrier 1:** when ADEEM1 = 1 it activates the adaptive de-emphasis function (for Wegener-Panda 1 encoded programs), which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 µs. When ADEEM1 = 0, the adaptive de-emphasis is off.
2	FMDSC13	**FM de-emphasis:** the state of these 3 bits determines the FM de-emphasis for sound carrier 1; see Table 33.
1	FMDSC12	
0	FMDSC11	

Table 33 De-emphasis

FMDSC23; FMDSC13	FMDSC22; FMDSC12	FMDSC21;FMDSC11	DE-EMPHASIS[1]
0	0	0	50 μs
0	0	1	60 μs
0	1	0	75 μs
0	1	1	J17[2]
1	0	0	off

Notes

1. The FM de-emphasis gain is 0 dB at 40 Hz.
2. Not used in any known terrestrial TV sound standard. NICAM de-emphasis is selected in the NICAM configuration register; see Table 41.

10.3.9 FM DEMATRIX REGISTER (FMMR)

This register is used to select the proper dematrixing characteristics as appropriate for the standard of the received carrier and the related sound mode identification. For the dematrixing, it is assumed that the output from sound carrier 1 is on channel 1 input. Bits 3 to 6 are not used.

The default setting after power-on reset is ‘0000 0000’.

Table 34 FM dematrix register (subaddress 11)

7	6	5	4	3	2	1	0
IDSWFM	0	0	0	0	FDMS2	FDMS1	FDMS0

Table 35 Description of the FMMR bits

BIT	SYMBOL	DESCRIPTION
7	IDSWFM	**Automatic FM-dematrix switching:** if set to logic 1, the FM dematrix is switched automatically in dependence on the current FM identification result. In case of stereo, the type of stereo dematrixing (Europe or Korea) is determined by bit IDAREA in subaddress 9. Bits FDMS2, FDMS1 and FDMS0 are ignored and the dematrix output is set according to Table 37. With channel 2 in NICAM mode, mono (channel 1) is always selected.
6	–	these 4 bits are not used and should be set to logic 0
5	–	
4	–	
3	–	
2	FDMS2	**Dematrixing characteristics select:** the state of these 3 bits select the dematrixing characteristics; see Table 36
1	FDMS1	
0	FDMS0	

Table 36 Selection of the dematrixing characteristics (manual mode)

FDMS2	FDMS1	FDMS0	L OUTPUT	R OUTPUT	MODE
0	0	0	CH1	CH1	mono 1
0	0	1	CH2	CH2	mono 2
0	1	0	CH1	CH2	dual
0	1	1	CH2	CH1	dual swapped
1	0	0	2CH1 – CH2	CH2	stereo Europe
1	0	1	$\frac{CH1 + CH2}{2}$	$\frac{CH1 - CH2}{2}$	stereo Korea –6 dB
1	1	0	CH1 + CH2	CH1 – CH2	stereo Korea

Table 37 Setting of the dematrixing characteristics (automatic mode)

IDENTIFICATION MODE		L OUTPUT	R OUTPUT
Mono		CH1	CH1
Stereo	Europe	2CH1 – CH2	CH2
	Korea	CH1 + CH2	CH1 – CH2
Dual		CH1	CH2

10.3.10 Channel 1 Output Level Adjustment Register (C1OLAR)

This register is used to correct for standard and station-dependent differences of signal levels. Table 38 applies to the FM dematrix output channel 1.

The default setting after power-on reset is ‘0000 0000’.

Table 38 Channel 1 output level adjustment register (subaddress 12)
The selected gain is also applied to the FM signal channel 1 for input to the mono channel.

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	−1
0	0	0	1	1	1	0	1	−2
0	0	0	1	1	1	0	0	−3
0	0	0	1	1	0	1	1	−4
0	0	0	1	1	0	1	0	−5
0	0	0	1	1	0	0	1	−6
0	0	0	1	1	0	0	0	−7
0	0	0	1	0	1	1	1	−8
0	0	0	1	0	1	1	0	−9
0	0	0	1	0	1	0	1	−10
0	0	0	1	0	1	0	0	−11
0	0	0	1	0	0	1	1	−12
0	0	0	1	0	0	1	0	−13
0	0	0	1	0	0	0	1	−14
0	0	0	1	0	0	0	0	−15

10.3.11 Channel 2 Output Level Adjustment Register (C2OLAR)

This register is used to correct for standard and station-dependent differences of signal levels. Table 39 applies to the FM dematrix output channel 2 in its FM and AM modes. In the event of FM stereo or FM dual language reception, channels 1 and 2 should be adjusted to the same level. The default setting after power-on reset is '0000 0000'.

Table 39 Channel 2 output level adjustment register (subaddress 13)

The gain chosen is also applied to the FM signal channel 1 for input to the mono channel.

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	–1
0	0	0	1	1	1	0	1	–2
0	0	0	1	1	1	0	0	–3
0	0	0	1	1	0	1	1	–4
0	0	0	1	1	0	1	0	–5
0	0	0	1	1	0	0	1	–6
0	0	0	1	1	0	0	0	–7
0	0	0	1	0	1	1	1	–8
0	0	0	1	0	1	1	0	–9
0	0	0	1	0	1	0	1	–10
0	0	0	1	0	1	0	0	–11
0	0	0	1	0	0	1	1	–12
0	0	0	1	0	0	1	0	–13
0	0	0	1	0	0	0	1	–14
0	0	0	1	0	0	0	0	–15

10.3.12 NICAM CONFIGURATION REGISTER (NCONR)

The default setting after power-on reset is ‘0000 0000’.

Table 40 NICAM configuration register (subaddress 14)

7	6	5	4	3	2	1	0
DCXOPULL	DCXOTEST	0	DOUTEN	0	AMSEL	NDEEM	AMUTE

Table 41 Description of the NCONR bits; see notes 1 to 4

BIT	SYMBOL	DESCRIPTION
7	DCXOPULL	**DCXO frequency select:** selects DCXO lower or upper test frequency during DCXO test mode. When DCXOPULL = 1 it sets the DCXO to the lower DCXO frequency. When DCXOPULL = 0 it sets the DCXO to its higher frequency.
6	DCXOTEST	**DCXO test mode enable:** when DCXOTEST = 1 it enables the DCXO test mode (available only during FM mode). In this mode frequency pulling via DCXOPULL is enabled. When DCXOTEST = 0 it enables normal operation.
5	–	this bit is not used and should be set to logic 0
4	DOUTEN	**Data output enable:** when DOUTEN = 1 it enables the output of the NICAM serial data stream from the DQPSK demodulator and of the associated clock, PCLK. When DOUTEN = 0, both outputs will be 3-stated.
3	–	this bit is not used and should be set to logic 0
2	AMSEL	**Auto-mute select:** when AMSEL = 1 the auto-mute will switch between NICAM sound and the analog mono input. This bit only has an effect when the auto-mute function is enabled and when the DAC has been selected in the analog output select register (see Section 10.3.18). When AMSEL = 0, the auto-mute will switch between NICAM sound and the sound on the first sound carrier (i.e. FM mono or AM).
1	NDEEM	**De-emphasis on/off:** when NDEEM = 1 it switches the NICAM J17 de-emphasis off. When NDEEM = 0 it switches the NICAM J17 de-emphasis on.
0	AMUTE	**Auto-muting on/off:** when AMUTE = 1 automatic muting is disabled. This bit only has an effect when the second sound carrier is set to NICAM. When AMUTE = 0 it enables the automatic switching between NICAM and the program on the first sound carrier (i.e. FM mono or AM), depending on the NICAM bit error rate. The FM dematrix should be set to the mono position or IDSWFM (subaddress 11) should be set.

Notes

1. The decision of whether auto-muting is permitted will be taken by the controlling microprocessor based on information contained in the TDA9874A’s status registers. Thus, it depends on the strategy implemented in the software whether the auto-mute function is in accordance with *“NICAM 728 ETS Revised for Data Applications”* or any other preference.
2. The NICAM de-emphasis gain is 0 dB at 40 Hz.
3. The AMSEL bit has only an effect on the analog sound outputs (OUTL, OUTR and OUTM). With regard to the digital sound output (I^2S-bus), the auto-mute will only switch between NICAM and the first sound carrier.
4. The DCXO test mode is intended for checking the DCXO control range with the actually used PCB layout and crystal type. During normal operation, the DCXO test mode should not be used.

10.3.13 NICAM Output Level Adjustment Register (NOLAR)

This register is used to correct for standard and station-dependent differences of signal levels. Table 42 applies to both NICAM sound outputs. The default setting after power-on reset is '0000 0000'.

Table 42 NICAM output level adjustment register (subaddress 15)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	–1
0	0	0	1	1	1	0	1	–2
0	0	0	1	1	1	0	0	–3
0	0	0	1	1	0	1	1	–4
0	0	0	1	1	0	1	0	–5
0	0	0	1	1	0	0	1	–6
0	0	0	1	1	0	0	0	–7
0	0	0	1	0	1	1	1	–8
0	0	0	1	0	1	1	0	–9
0	0	0	1	0	1	0	1	–10
0	0	0	1	0	1	0	0	–11
0	0	0	1	0	0	1	1	–12
0	0	0	1	0	0	1	0	–13
0	0	0	1	0	0	0	1	–14
0	0	0	1	0	0	0	0	–15

10.3.14 NICAM Lower Error Limit Register (NLELR)

When the auto-mute function is enabled (see Section 10.3.12) and the NICAM bit error count is lower than the value contained in this register, the NICAM signal is selected (again) for reproduction; see also Section 10.3.15.

The default setting after power-on reset is ‘0001 0100’.

Table 43 NICAM lower error limit register (subaddress 16)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.3.15 NICAM Upper Error Limit Register (NUELR)

When the auto-mute function is enabled (see Section 10.3.12) and the NICAM bit error count is higher than the value contained in this register, the signal of the first sound carrier (i.e. FM mono or AM sound) or the analog mono input is selected for reproduction.

The difference between the upper and lower error limit constitutes a hysteresis to avoid frequent switching between NICAM and the program on the 1st sound carrier.

The default setting after power-on reset is ‘0101 0000’.

Table 44 NICAM upper error limit register (subaddress 17)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.3.16 Audio Mute Control Register (AMCONR)

Only bits 6, 2 and 1 are used. The state of the **unused bits should be set to logic 1**. When any of these bits is set HIGH, the corresponding pair of output channels will be muted. A LOW bit allows normal signal output.

The default setting after power-on reset is ‘1111 1111’.

Table 45 Audio mute control register (subaddress 18)

7	6	5	4	3	2	1	0
1	MUTI^{2}S	1	1	1	MUTSOUT	MUTMOUT	1

Table 46 Description of the AMCONR bits

BIT	SYMBOL	DESCRIPTION
7	–	this bit is not used and should be set to logic 1
6	MUTI^{2}S	**Mute I^{2}S-bus output:** when MUTI^{2}S = 1 it mutes the I^{2}S-bus output
5	–	these 3 bits are not used and should be set to logic 1
4	–	
3	–	
2	MUTSOUT	**Mute Stereo Output:** if MUTSOUT = 1 the analog stereo output is muted
1	MUTMOUT	**Mute Mono Output:** if MUTMOUT = 1 the analog mono output is muted
0	–	this bit is not used and should be set to logic 1

10.3.17 Stereo DAC Output Select Register (SDACOSR)

This register is used to define the signal source to be entered into the DAC. The stereo DAC output can be routed to the analog stereo output pins, depending on the setting in the AOSR; see Section 10.3.18.

A simplified setting is possible, if automatic FM dematrix switching (see Section 10.3.9) and auto-select (see Section 10.3.18) is applied.

The two combinations of FM and NICAM shown in Table 50 apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for special applications. It should be noted that the controlling microprocessor has to assure that the FM dematrix is set to the mono position or that IDSWFM is set HIGH.

An additional Automatic Volume Level (AVL) control function is implemented, which provides a constant output level of −23 dB (FS) for input levels between 0 and −29 dB (FS). There are some fixed decay time constants to choose from, i.e. 2, 4 or 8 s.

The automatic stereo DAC switching, operating similar to the mono DAC switching, is shown in Table 56.

The default setting after power-on reset is ‘0000 0000’.

Bits 2 and 6 are not used and should be set to logic 0.

Table 47 Stereo DAC output select register (subaddress 19)

7	6	5	4	3	2	1	0
SDGS1	0	AVL 1	AVL 0	SDGS0	0	SDOS1	SDOS0

Table 48 Selection of stereo DAC gain

SDGS1	SDGS0	DAC GAIN (dB)
0	0	0
0	1	3
1	0	6
1	1	9

Table 49 AVL control mode

The AVL attack time is always 10 ms.

AVL1	AVL0	AVL MODE
0	0	off or reset
0	1	short decay (2 s)
1	0	medium decay (4 s)
1	1	long decay (8 s)

Table 50 Signal source left and right

SDOS1	SDOS0	SIGNAL SOURCE STEREO DAC	
		LEFT	RIGHT
0	0	FM/AM	FM/AM
0	1	NICAM left	NICAM right
1	0	FM/AM	NICAM M1
1	1	FM/AM	NICAM M2

The auto-select function is available only if SDOS1 and SDOS0 are set to ‘00’ or ‘01’. Matrixing can be set in the analog output select register.

10.3.18 Analog Output Select Register (AOSR)

This register is used to define both the signal source to be output at the analog outputs and the output channel selector mode.

The DAC outputs are automatically muted in the event that one of the analog inputs is selected for output.

The $\frac{L+R}{2}$ position of the matrix applies only to the DAC outputs, it is not available for analog input signals.

The default setting after power-on reset is ‘0000 0000’.

Table 51 Analog output select register (subaddress 20)

7	6	5	4	3	2	1	0
TVSM	CSM2	CSM1	CSM0	MOS1	MOS0	SSS1	SSS0

Table 52 Description of the AOSR bits

BIT	SYMBOL	DESCRIPTION
7	TVSM	**Auto-select function:** for TV applications, only in combination with IDSWFM set HIGH. If set HIGH switches the matrix automatically depending on the IDSTE, IDDUA bits for FM and the S/MB, D/SB bits for NICAM (see Sections 10.4.1 and 10.4.2).
6	CSM2	**Output channel selection mode, stereo output:** these 3 bits select the output channel selection mode; see Table 53
5	CSM1	
4	CSM0	
3	MOS1	**Signal source for mono output:** these 2 bits select the signal source for the mono output; see Table 54
2	MOS0	
1	SSS1	**Signal source for stereo output:** these 2 bits select the signal source for the stereo output; see Table 55
0	SSS0	

Table 53 Output channel selection mode for stereo output (TVSM = LOW)

CSM2	CSM1	CSM0	L OUTPUT	R OUTPUT	REMARK
0	0	0	L input	R input	–
0	0	1	L input	L input	–
0	1	0	R input	R input	–
0	1	1	R input	L input	–
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$	not allowed during use of high deviation mode

Table 54 Signal source selection analog mono output

MOS1	MOS0	SIGNAL SOURCE
0	0	mono DAC
0	1	external input L
1	0	external input R
1	1	mono input

Table 55 Signal source selection stereo output

SSS1	SSS0	SIGNAL SOURCE
0	0	DAC
0	1	reserved
1	0	external input
1	1	mono input

Table 56 Auto-select function (TVSM = HIGH and IDSWFM = HIGH): FM mode/NICAM mode for stereo DAC

OUTPUT CHANNEL SELECTION MODE			FM IDENT/NICAM SOUND MODE			AUTO-MUTE = HIGH AND CH2MOD = 10
CSM2	CSM1	CSM0	MONO	STEREO	DUAL	
0	0	X[1]	M/M	L/R	A/A	FM/AM: M/M
0	1	0	M/M	L/R	B/B	FM/AM: M/M

Note

1. X = don't care.

Signal source selection bits SDOS1 and SDOS0 must be set to 0X for FM mode (including FM mode by switching if auto-mute select is set LOW) or 01 for NICAM mode, when using the auto-select function.

10.3.19 DIGITAL AUDIO INTERFACE CONFIGURATION REGISTER (DAICONR)

The default setting after Power-on reset is 00000000.

Table 57 Digital Audio Interface Configuration Register (subaddress 21)

7	6	5	4	3	2	1	0
0	0	0	SYSCL1	SYSCL0	SYSOUT	I^2SFORM	I^2SOUT

Table 58 Description of the DAICONR bits

BIT	SYMBOL	DESCRIPTION
7	–	these 3 bits are not used and should be set to logic 0
6	–	
5	–	
4	SYSCL1	**System clock frequency select:** these 2 bits select the frequency of the system clock; see Table 59
3	SYSCL0	
2	SYSOUT	**System clock output on/off:** when SYSOUT = 1 it enables the output of a system (or master) clock signal at pin SYSCLK. When SYSOUT = 0, the output will be off, thereby improving EMC performance.
1	I^2SFORM	**Serial output format:** when I^2SFORM = 1 it selects an MSB-aligned, MSB-first output format, i.e. a level change at the word select pin indicates the beginning of a new audio sample. When I^2SFORM = 0, it selects the standard I^2S-bus output format.
0	I^2SOUT	**I^2S-bus output on/off:** when I^2SOUT = 1 it enables the output of serial audio data (2 pins) plus serial bit clock and word select in a format determined by the I^2SFORM bit. The TDA9874A then is an I^2S-bus master. When I^2SOUT = 0, the outputs mentioned will be 3-stated, thereby improving EMC performance.

Table 59 System clock frequency select

SYSCL1	SYSCL0	SYSCLK OUTPUT	FREQUENCY (MHz)
0	0	$256f_s$	8.192
0	1	$384f_s$	12.288
1	0	$512f_s$	16.384
1	1	$768f_s$	24.576

10.3.20 I²S-BUS OUTPUT SELECT REGISTER (I²SOSR)

This register is used to define both the signal source to be output at the I²S-bus port and the mode of the digital matrix for signal selection.

The two combinations of FM and NICAM shown in Table 62 apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for special applications. It should be noted that the controlling microprocessor has to assure that the FM dematrix is set to the mono position or IDSWFM is set HIGH. If the I²S-bus signal source is set to FM left or FM right it is influenced by the automatic FM dematrix switching (see subaddress 11).

The default setting after power-on reset is ‘0000 0000’.

Table 60 I²S-bus output select register (subaddress 22)

7	6	5	4	3	2	1	0
TVSMIIS	ICSM2	ICSM1	ICSM0	0	0	ISS1	ISS0

Table 61 Description of the I²SOSR bits

BIT	SYMBOL	DESCRIPTION
7	TVSMIIS	**Auto-select function:** for TV applications, only in combination with IDSWFM set HIGH. If set HIGH switches the matrix automatically depending on the IDSTE, IDDUA bits for FM and the S/MB, D/SB bits for NICAM in transmitters subaddresses 0 and 1 (see Sections 10.4.1 and 10.4.2).
6	ICSM2	**Output channel selection mode:** these 3 bits select the output channel selection mode; see Table 62
5	ICSM1	
4	ICSM0	
3	–	these 2 bits are not used and should be set to logic 0
2	–	
1	ISS1	**Signal source:** these 2 bits select the signal source; see Table 62
0	ISS0	

Table 62 Mode of the digital matrix for signal selection (TVSMIIS = LOW)

ICSM2	ICSM1	ICSM0	L OUTPUT	R OUTPUT	REMARK
0	0	0	L input	R input	–
0	0	1	L input	L input	–
0	1	0	R input	R input	–
0	1	1	R input	L input	–
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$	not allowed during use of high deviation mode

Table 63 Signal source left and right; note 1

ISS1	ISS0	SIGNAL SOURCE I²S-BUS OUTPUT	
		LEFT	RIGHT
0	0	FM/AM left	FM/AM right
0	1	NICAM left	NICAM right
1	0	FM/AM	NICAM M1
1	1	FM/AM	NICAM M2

Note

1. The auto-select function is available only if ISS1 and ISS0 are set to ‘00’ or ‘01’.

Table 64 Auto-select function (TVSMIIS = HIGH and IDSWFM = HIGH): FM mode/NICAM mode for I²S-bus output

I²S-BUS OUTPUT			FM IDENT/NICAM SOUND MODE			AUTO-MUTE = HIGH AND CH2MOD = 10
ICSM2	ICSM1	ICSM0	MONO	STEREO	DUAL	
0	0	X[1]	M/M	L/R	A/A	FM/AM: M/M
0	1	0	M/M	L/R	B/B	FM/AM: M/M

Note

1. X = don’t care.

10.3.21 I²S-BUS OUTPUT LEVEL ADJUSTMENT REGISTER (I²SOLAR)

This register is used to adjust the output level at the I²S-bus port. Left and right signal channels are treated identically.

The default setting after power-on reset is ‘0000 0000’.

Table 65 I²S-bus output level adjustment register (subaddress 23)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	−1
0	0	0	1	1	1	0	1	−2
0	0	0	1	1	1	0	0	−3
0	0	0	1	1	0	1	1	−4
0	0	0	1	1	0	1	0	−5
0	0	0	1	1	0	0	1	−6
0	0	0	1	1	0	0	0	−7
0	0	0	1	0	1	1	1	−8
0	0	0	1	0	1	1	0	−9
0	0	0	1	0	1	0	1	−10
0	0	0	1	0	1	0	0	−11
0	0	0	1	0	0	1	1	−12
0	0	0	1	0	0	1	0	−13
0	0	0	1	0	0	0	1	−14
0	0	0	1	0	0	0	0	−15

10.3.22 MONO DAC OUTPUT SELECT REGISTER (MDACOSR)

This register is used to define the signal source to be entered into the mono DAC. The mono DAC is used for signal output from digital sources.

For the mono DAC output auto-matrix switching is always active.

In stereo mode $\frac{L+R}{2}$ is chosen automatically. Selecting Language B (MDOS1, MDOS0 = 01 or 11) will only show effect, while a dual transmission via FM A2 or NICAM is being received.

Settings in the FM dematrix register have no effect on the source selection for the mono DAC.

The level adjustment for an FM source is determined by the Channel 1 output level adjustment register (subaddress 12) for mono/dual A, or by the Channel 2 output level adjustment register (subaddress 13) for dual B, or by the NICAM output level adjustment register (subaddress 15) if a NICAM source is selected.

Some extra gain can be introduced at the input to the DAC to provide a coarse level adjustment function.

The default setting after power-on reset is ‘0000 0000’.

Bits 2, 4, 5 and 6 are don’t care and should be set to logic 0.

Table 66 Mono DAC output select register (subaddress 24)

7	6	5	4	3	2	1	0
MDGS1	0	0	0	MDGS0	0	MDOS1	MDOS0

Table 67 Selection of DAC gain

MDGS1	MDGS0	DAC GAIN (dB)
0	0	0
0	1	3
1	0	6
1	1	9

Table 68 Signal source

MDOS1	MDOS0	MONO DAC OUTPUT
0	0	FM/AM $\frac{L+R}{2}$ or mono/dual A
0	1	FM/AM dual B if dual mode transmission, otherwise mono
1	0	NICAM $\frac{L+R}{2}$ or mono/dual A
1	1	NICAM mono 2 if dual mode transmission, otherwise mono

10.3.23 Easy Standard Programming (ESP) register

This register is used to simplify the setting of different TV sound standards via the I²C-bus. Writing to this register will overwrite the contents of registers 3 to 10 with the settings needed to demodulate one of the standards shown in Table 70. After power-up, the default setting has no effect on the settings of registers 3 to 10. Old values of registers 3 to 10 are not stored. Demodulators filter the bandwidth and identification time constants are also set independently from the chosen standard selected in this register.

This means for I²C-bus refreshing: using the ESP option, registers 3 to 10 should not be overwritten during a refresh.

If ESP is not used, the ESP register should not be accessed in the refresh routine.

Demodulators filter bandwidth and identification time constants are also set independently in this register.

The default setting after power-on reset is ‘0000 0000’.

For a description of bits IDMOD0 and IDMOD1 (FM identification mode), FILTBW0 and FILTBW1 (demodulator filter bandwidth) refer to Section 10.3.7. Bits IDMOD0 and IDMOD1 (FM identification mode), FILTBW0 and FILTBW1 (demodulator filter bandwidth) are identical in registers 255 and 9.

Table 69 Easy standard programming register (subaddress 255)

7	6	5	4	3	2	1	0
FILTBW1	FILTBW0	IDMOD1	IDMOD0	EPB3	EPB2	EPB1	EPB0

Table 70 Available standards for easy standard programming

EPB3	EPB2	EPB1	EPB0	STANDARD	
				NUMBER	NAME
0	0	0	0	0	A2, B/G
0	0	0	1	1	A2, M (Korea)
0	0	1	0	2	A2, D/K (1)
0	0	1	1	3	A2, D/K (2)
0	1	0	0	4	A2, D/K (3)
0	1	0	1	5	NICAM, I
0	1	1	0	6	NICAM, B/G
0	1	1	1	7	NICAM, D/K
1	0	0	0	8	NICAM, L
1	0	0	1	9	reserved
1	0	1	0	10	reserved
1	0	1	1	11	reserved
1	1	0	0	12	Astra satellite stereo (7.02/7.20 MHz)
1	1	0	1	13	reserved
1	1	1	0	14	reserved
1	1	1	1	15	reserved

10.4 Slave transmitter mode

As a slave transmitter, the TDA9874A provides 12 registers with status information and data, a part of which is for Philips internal purposes only. Each register is accessed by means of a subaddress.

Detailed descriptions of the slave transmitter registers are given in Sections 10.4.1 to 10.4.9.

Reading of data can start at any valid subaddress. It is allowed to read more than 1 data byte per transmission from the TDA9874A. In this case, the subaddress is automatically incremented after each data byte, resulting in reading the sequence of data bytes from successive register locations, starting at SUBADDRESS.

Each data byte in a read sequence, except for the last one, is acknowledged with Am. The subaddresses ‘wrap around’ from decimal 255 to 0. If an attempt is made to read from a non-existing subaddress, the device will send a data pattern of all ones, i.e. FF in hexadecimal notation.

Table 71 General format for reading data from the TDA9874A

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	Sr	SLAVE ADDRESS	1	A	DATA	NAm	P

Table 72 Explanation of Tables 71 and 73

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge (by the slave)
SUBADDRESS	address of register to read from
Sr	repeated START condition
1	data direction bit (read from device)
DATA	data byte read from register
NAm	not acknowledge (by the master)
Am	acknowledge (by the master)
P	STOP condition

Table 73 Format of a transmission using automatic incrementing of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	Sr	SLAVE ADDRESS	1	A	DATA BYTE Am n data bytes with auto-increment of subaddresses	DATA	NAm	P

Table 74 Overview of the slave transmitter registers

SUBADDRESS (DECIMAL)(1)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
0	P2IN	P1IN	RSSF	AMSTAT	VDSP	IDDUA	IDSTE	PFR	device status (identification, etc.)
1	C4	C3	C2	C1	OSB	CFC	S/MB	D/SB	NICAM status
2	B7	B6	B5	B4	B3	B2	B1	B0	NICAM error count
3	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	additional data (LSB)
4	OVW	SAD	–	CI1	CI2	AD10	AD9	AD8	additional data (MSB)
5	B7	B6	B5	B4	B3	B2	B1	B0	level read-out (MSB)
6	B7	B6	B5	B4	B3	B2	B1	B0	level read-out (LSB)
7	IDPILOT	–	–	B4	B3	B2	B1	B0	SIF level
252	B7	B6	B5	B4	B3	B2	B1	B0	test register 2
253	B7	B6	B5	B4	B3	B2	B1	B0	test register 1
254	B7	B6	B5	B4	B3	B2	B1	B0	device identification code
255	B7	B6	B5	B4	B3	B2	B1	B0	software identification code

Note

1. Registers from subaddress 252 to 255 are for Philips internal purposes only. They are considered as a set of registers for the identification of individual members and some key parameters in a family of devices.

10.4.1 Device Status Register (DSR)

Table 75 Device status register (subaddress 0)

7	6	5	4	3	2	1	0
P2IN	P1IN	RSSF	AMSTAT	VDSP	IDDUA	IDSTE	PFR

Table 76 Description of the DSR bits

BIT	SYMBOL	DESCRIPTION
7	P2IN	**Input from Port 2:** this bit reflects the status of the P2 general purpose port pin; see Section 10.3.3. If P2IN = 1, then the P2 general purpose port pin is HIGH. If P2IN = 0, then the P2 general purpose port pin is LOW.
6	P1IN	**Input from Port 1:** this bit reflects the status of the P1 general purpose port pin; see Section 10.3.3. If P1IN = 1, then the P1 general purpose port pin is HIGH. If P1IN = 0, then the P1 general purpose port pin is LOW.
5	RSSF	**Reserve Sound Switching Flag:** when RSSF = 1, this bit is a copy of the C4 bit in the NICAM status register (see Section 10.4.2). It indicates that the FM (or AM for standard L) sound matches the digital transmission and auto-muting should be enabled. When RSSF = 0, auto-muting should be disabled, as analog and digital sound are different.
4	AMSTAT	**Auto-mute Status:** if this bit is HIGH, it indicates that the auto-muting function has switched from NICAM to the program of the first sound carrier (i.e. FM mono or AM in NICAM L systems)
3	VDSP	**Identification of NICAM sound:** when VDSP = 1, it indicates that digital transmission is a sound source. When VDSP = 0, it indicates that the transmission is either data or a currently undefined format.
2	IDDUA	**Identification of FM dual sound; A2 systems:** if IDDUA = 1, an FM dual-language signal has been identified. When neither IDSTE nor IDDUA = 1, the received signal is assumed to be FM mono (A2 systems only).
1	IDSTE	**Identification of FM stereo; A2 systems:** if IDSTE = 1, an FM stereo signal has been identified (A2 systems only)
0	PFR	**Power failure register:** the power supply for the digital part of the device (V_{DDD1}) has temporarily been lower than the specified lower limit. If this is detected an initialization of the device has to be carried out to ensure reliable operation.

10.4.2 NICAM Status Register (NISR)

Table 77 NICAM status register (subaddress 1)

7	6	5	4	3	2	1	0
C4	C3	C2	C1	OSB	CFC	S/MB	D/SB

Table 78 Description of the NISR bits; notes 1 and 2

BIT	SYMBOL	DESCRIPTION
7	C4	**NICAM application control bits:** these bits correspond to the control bits C1 to C4 in the NICAM transmission.
6	C3	
5	C2	
4	C1	
3	OSB	**Synchronization bit:** when OSB = 1, it indicates that the device has both frame and C0 (16 frame) synchronization. When OSB = 0, it indicates that the audio output from the NICAM part is digital silence.
2	CFC	**Configuration change:** when CFC = 1, it indicates a configuration change at the 16 frame (C0) boundary
1	S/MB	**Identification of NICAM stereo:** when S/MB = 1, it indicates stereo mode
0	D/SB	**Identification of NICAM dual mono:** when D/SB = 1, it indicates dual mono mode.

Notes

1. The TDA9874A does not support the extended control modes. Therefore, the program of the first sound carrier (i.e. FM mono or AM) is selected for reproduction in case bit C3 is set HIGH, independent of bit AMUTE in the NICAM configuration register being set or not.
2. When a NICAM transmitter is switched off, the device will lose synchronization. In that case the program of the first sound carrier is selected for reproduction, independent of bit AMUTE being set or not.

10.4.3 NICAM Error Count Register (NIECR)

Bits B7 to B0 contain the number of errors occurring in the previous 128 ms period. The register is updated every 128 ms.

Table 79 NICAM error count register (subaddress 2)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.4.4 Data Registers (DR1 and DR2)

The contents of these two registers provide information on the additional data bits. AD byte 0 is stored at subaddress 3.

Table 80 Data register 1 (subaddress 3)

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 81 Description of the DR1 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	AD7 to AD0	The lower 8 bits of the additional data word.

Table 82 Data register 2 (subaddress 4)

7	6	5	4	3	2	1	0
OVW	SAD	–	CI1	CI2	AD10	AD9	AD8

Table 83 Description of the DR2 bits

BIT	SYMBOL	DESCRIPTION
7	OVW	If this bit is HIGH, new additional data bits are written to the IC without the previous bits being read.
6	SAD	When SAD = 1, new additional data is written into the IC. This bit is reset when the additional data bits are read.
5	–	this bit is undefined
4	CI1	These 2 bits are CI bits decoded by majority logic from the parity checks of the last ten samples in a frame.
3	CI2	
2	AD10	the upper 3 bits of the additional data word
1	AD9	
0	AD8	

10.4.5 Level Read-out Registers (LRRA and LRRB)

These two bytes constitute a word that provides data from a location that has been specified with the monitor select register (see Section 10.3.4). The most significant byte of the data is stored at subaddress 5.

Table 84 Level read-out register A (subaddress 5)

7	6	5	4	3	2	1	0
B7(1)	B6	B5	B4	B3	B2	B1	B0

Note

1. B7 is the most significant bit or sign bit of the word.

Table 85 Level read-out register B (subaddress 6)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0(1)

Note

1. B0 is the least significant bit of the word.

10.4.6 SIF Level Register (SIFLR)

When the SIF AGC is on, bits B4 to B0 of this register contain a number that gives an indication of the SIF input level. That number can be interpreted in the same way as the AGC gain register setting (see Section 10.3.2), i.e. if the SIF AGC were set to a fixed gain and the same number loaded into the AGC gain register, the current SIF input signal level would generate a SIF ADC output close to full-scale.

When the SIF AGC is off, this register returns the contents of the AGC gain register.

Bits B5 and B6 are don't care.

Table 86 SIF level register (subaddress 7)

7	6	5	4	3	2	1	0
IDPILOT	–	–	B4	B3	B2	B1	B0

Table 87 Description of the SIF level bits

BIT	SYMBOL	DESCRIPTION
7	IDPILOT	**IDPILOT bit:** when IDPILOT = 1 it indicates that an FM pilot carrier in the 2nd channel is detected; note 1
6	–	this bit is undefined
5	–	this bit is undefined
4	B4	**SIF level data bits:** these bits correspond to the input level at the selected SIF input
3	B3	
2	B2	
1	B1	
0	B0	

Note

1. The pilot detector is faster than the stereo/dual identification, but not as reliable and slightly less sensitive. By means of the pilot detector bit, the control software is able to identify an analog 2-carrier (A2) standard transmission within approximately 0.1 s and even in the event of a mono transmission (second sound carrier with pilot). Certain NICAM test signals may trigger a wrong pilot indication, therefore the pilot detector bit should not be evaluated at channel 2 mixer frequencies that correspond to NICAM carriers (5.85 and 6.552 MHz). For detailed information, please contact a Philips representative.

10.4.7 Test Register 2 (TR2)

This register contains, as a binary number, the highest subaddress used for slave receiver registers.

The first version will have the identification '0010 1101'.

Table 88 Test register 2 (subaddress 252)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.4.8 Test Register 1 (TR1)

This register contains, as a binary number, the highest subaddress used for slave transmitter (status) registers.

The first version will have the identification '0000 0111'.

Table 89 Test register 1 (subaddress 253)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.4.9 Device Identification Code (DIC)

There will be several devices in the digital TV sound processor family, with TDA9874A being the second member. This byte is used to identify the individual family members.

The first version will have the identification '0001 0001'.

Table 90 Device identification code (subaddress 254)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

10.4.10 Software Identification Code (SIC)

It is likely that during the life time of this family of devices several versions of the DSP software will be made, e.g. to incorporate new application concepts, respond to customer wishes, etc. This byte is used to identify the different releases.

The first version will have the identification '0000 0010'.

Table 91 Software identification code (subaddress 255)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

11 I²S-BUS DESCRIPTION

The digital audio interface of the TDA9874A consists of a serial audio output and associated clock signals. It can be used to supply digital audio signals from received TV programs to a suitable output device, e.g. a DAC or an AES/EBU transmitter.

Two serial audio formats are supported at the digital audio interface, the I²S-bus format and a very similar MSB-aligned format. The difference is illustrated in Fig.8.

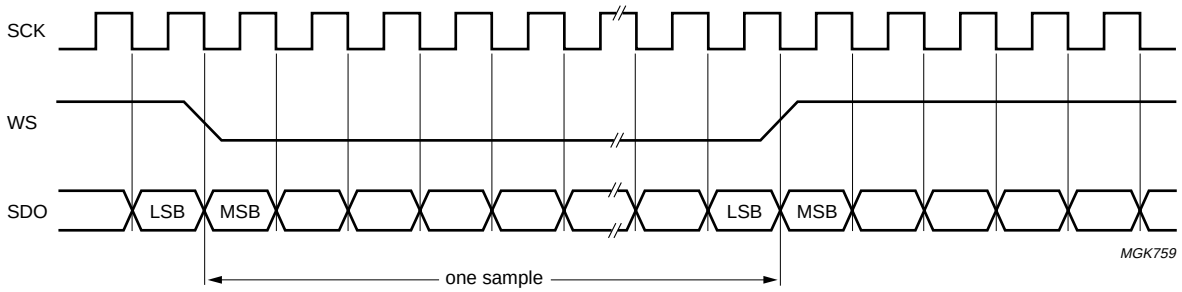
In both formats the left audio channel of a stereo sample pair is output first, and is on the Serial Data line (SDO) when the Word Select line (WS) is LOW. Data is written on the trailing edge of SCK and read on the leading edge of SCK. The most significant bit is sent first.

After power-on reset, the outputs of the digital audio interface are 3-stated to reduce EMC and allow for combinations with other ICs. If an output is desired, it has to be activated by means of an I²C-bus command.

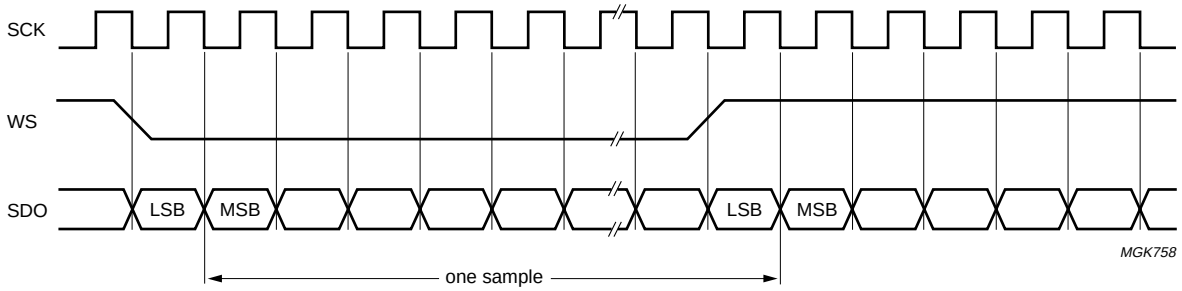
When the output is enabled, serial audio data can be taken from pin SDO. Depending on the signal source, switch and matrix positions, the output can be either mono, stereo or dual language.

The Word Select output (WS) is clocked with the audio sample frequency of 32 kHz. The Serial Clock output (SCK) is clocked at a frequency of 2.048 MHz. This means that there are 64 clock pulses per pair of stereo output samples, or 32 clock pulses per sample. There are 18 significant bits used on the Serial Data Output (SDO).

A symmetrical system clock output (SYSCLK) is available from the TDA9874A as a master clock for external digital audio devices. After Power-on reset, the clock is off. It can be enabled and the output frequency set via an I²C-bus command. Available output frequencies are 8.192, 12.288, 16.384 and 24.576 MHz.



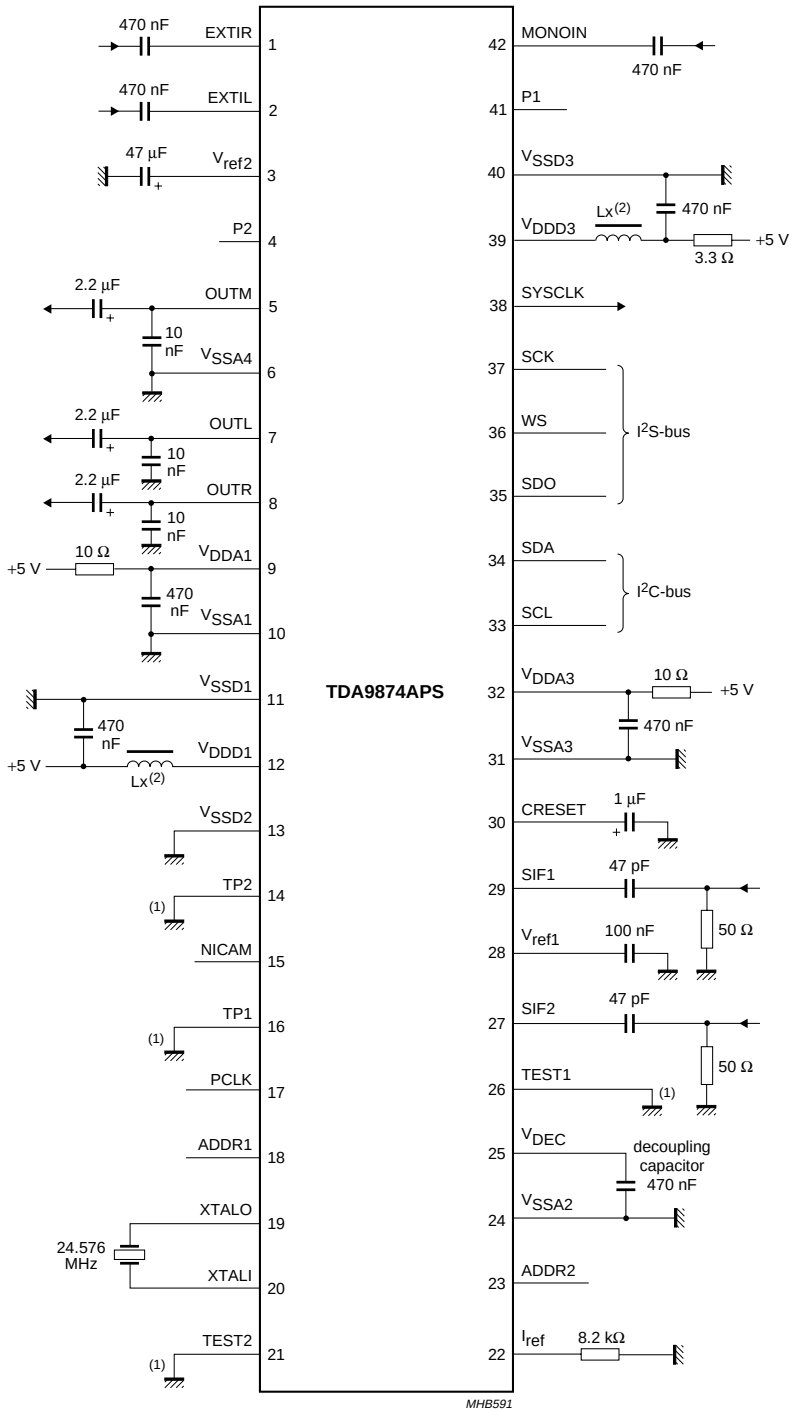
a. MSB-aligned format.



b. I^2S-bus format.

Fig.8 Serial audio interface formats.

12 EXTERNAL COMPONENTS

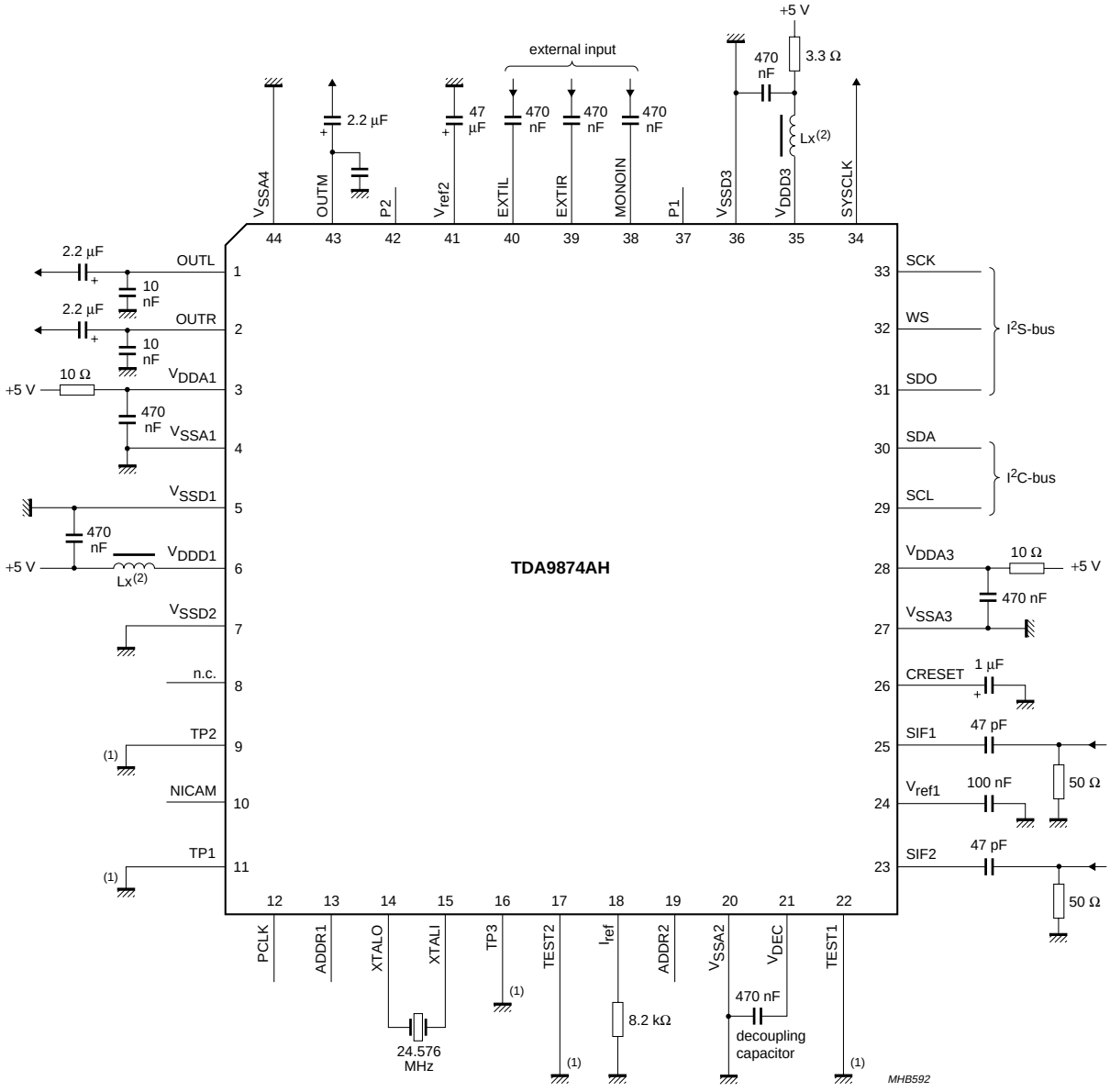


All analog and digital supply ground pins are connected internally and should be connected via a massive external ground plate.

(1) TP1, TP2, TEST1 and TEST2 should be connected to V_{SSD} during normal operation.

(2) Lx: ferrite bead, e.g. BLM 31A601S (Murata).

Fig.9 External components (SDIP42 version).



All analog and digital supply ground pins are connected internally and should be connected via a massive external ground plate.

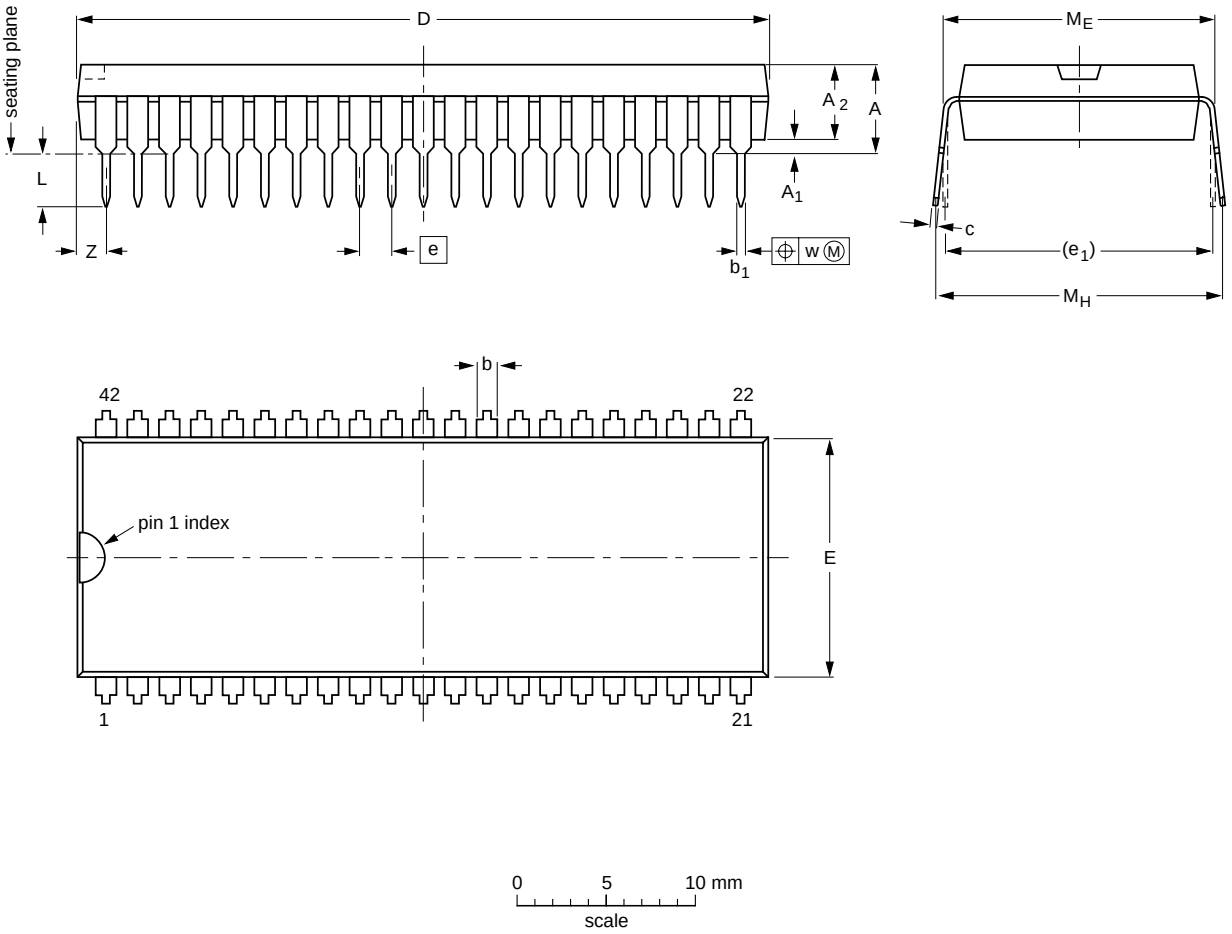
(1) TP1, TP2, TP3, TEST1 and TEST2 should be connected to V_{SSD} during normal operation.

(2) Lx: ferrite bead, e.g. BLM 31A601S (Murata).

Fig.10 External components (QFP44 version).

13 PACKAGE OUTLINES

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

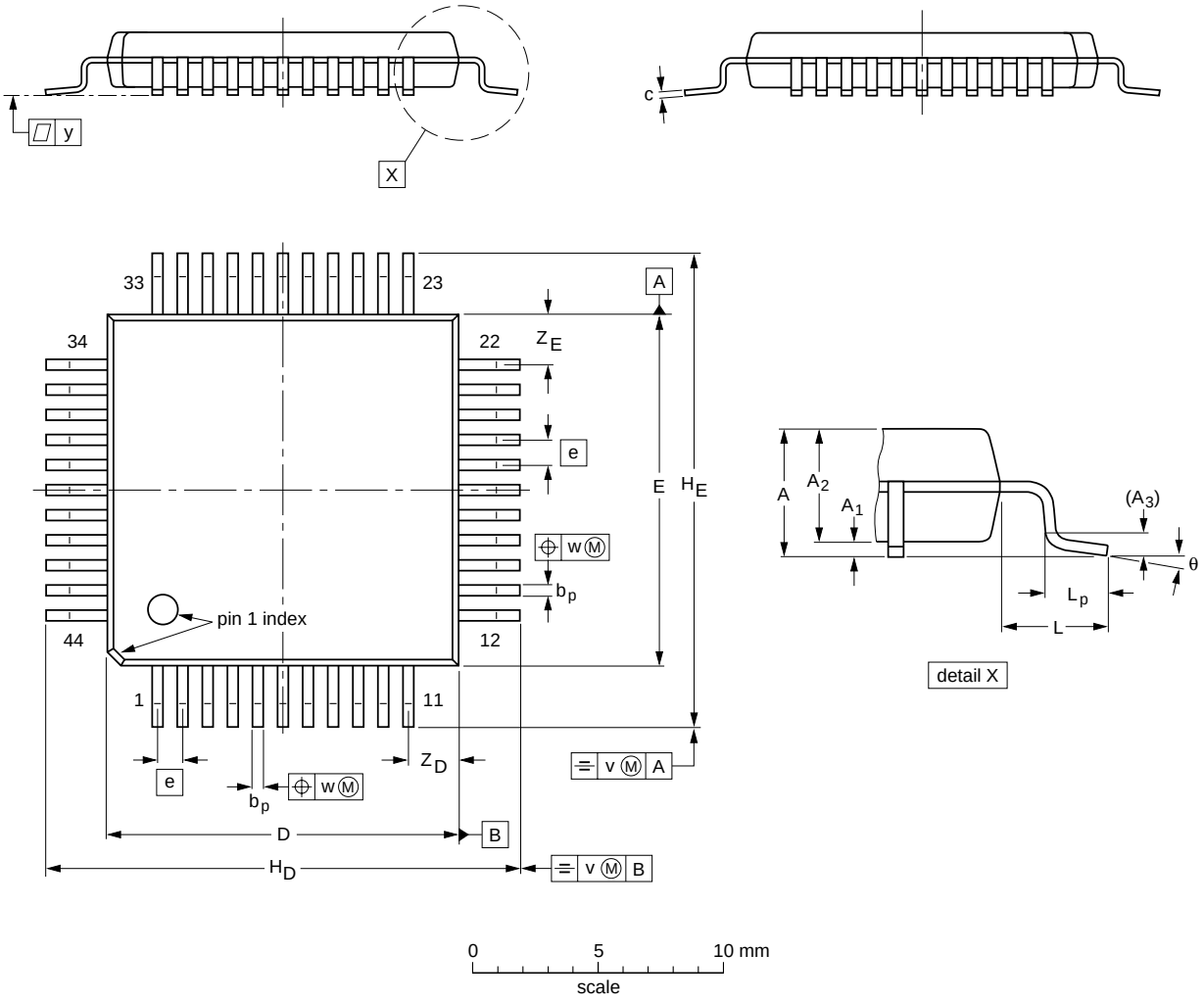
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

14 SOLDERING

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Through-hole mount packages

14.2.1 SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 Surface mount packages

14.3.1 REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3.2 WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

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