LM124-N/LM224-N/LM324-N/LM2902-N Low Power Quad Operational Amplifiers

Check for Samples: LM124-N, LM224-N, LM2902-N, LM324-N

FEATURES

- **Internally Frequency Compensated for Unity Gain**
- **Large DC Voltage Gain 100 dB**
- **Wide Bandwidth (Unity Gain) 1 MHz (Temperature Compensated)**
- **Wide Power Supply Range:**
  - **Single Supply 3V to 32V**
  - **or Dual Supplies ±1.5V to ±16V**
- **Very Low Supply Current Drain (700 µA)—Essentially Independent of Supply Voltage**
- **Low Input Biasing Current 45 nA (Temperature Compensated)**
- **Low Input Offset Voltage 2 mV**
  - **and Offset Current: 5 nA**
- **Input Common-Mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **Large Output Voltage Swing 0V to V^+ − 1.5V**

UNIQUE CHARACTERISTICS

- **In the Linear Mode the Input Common-Mode Voltage Range Includes Ground and the Output Voltage can also Swing to Ground, Even Though Operated from Only a Single Power Supply Voltage**
- **The Unity Gain Cross Frequency is Temperature Compensated**
- **The Input Bias Current is also Temperature Compensated**

ADVANTAGES

- **Eliminates Need for Dual Supplies**
- **Four Internally Compensated Op Amps in a Single Package**
- **Allows Directly Sensing Near GND and V_{OUT} also Goes to GND**
- **Compatible with All Forms of Logic**
- **Power Drain Suitable for Battery Operation**

DESCRIPTION

The LM124-N series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124-N series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

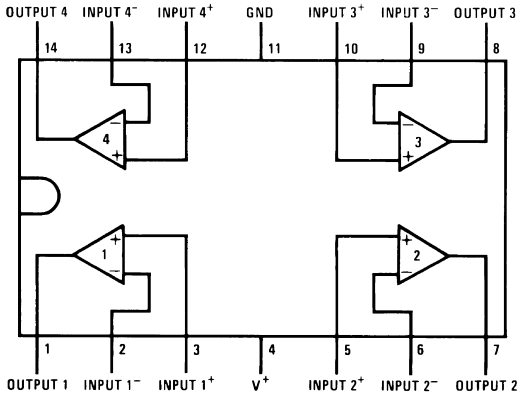
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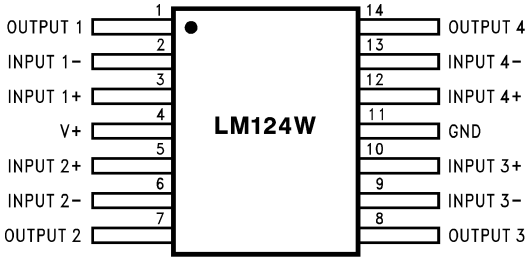
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Connection Diagrams



Note 1: LM124A available per JM38510/11006
Note 2: LM124-N available per JM38510/11005
Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device

Figure 1. Dual-In-Line Package - Top View
See Package Number J0014A D0014A or NFF0014A

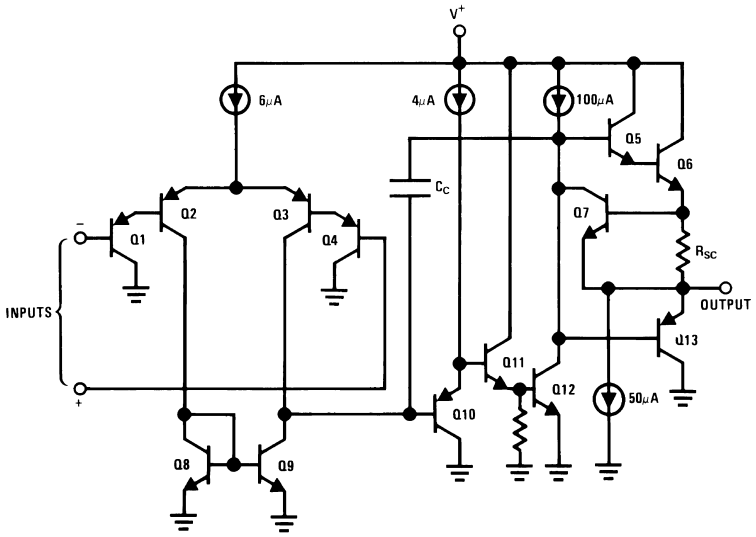


Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device

Figure 2. See Package Number NAD0014B
See Package Number NAC0014A

Schematic Diagram

(Each Amplifier)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

			LM124-N/LM224-N/LM324-N LM124A/LM224A/LM324A	LM2902-N
Supply Voltage, V^+			32V	26V
Differential Input Voltage			32V	26V
Input Voltage			−0.3V to +32V	−0.3V to +26V
Input Current (V_{IN} < −0.3V)(3)			50 mA	50 mA
Power Dissipation(4)	PDIP		1130 mW	1130 mW
	CDIP		1260 mW	1260 mW
	SOIC Package		800 mW	800 mW
Output Short-Circuit to GND (One Amplifier)(5)				
V^+ ≤ 15V and T_A = 25°C			Continuous	Continuous
Operating Temperature Range				−40°C to +85°C
LM324-N/LM324A			0°C to +70°C	
LM224-N/LM224A			−25°C to +85°C	
LM124-N/LM124A			−55°C to +125°C	
Storage Temperature Range			−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)			260°C	260°C
Soldering Information	Dual-In-Line Package	Soldering (10 seconds)	260°C	260°C
	Small Outline Package	Vapor Phase (60 seconds)	215°C	215°C
		Infrared (15 seconds)	220°C	220°C
ESD Tolerance(6)			250V	250V

(1) Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124-N military specifications.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/
(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).
(4) For operating at high temperatures, the LM324-N/LM324A/LM2902-N must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224-N/LM224A and LM124-N/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.
(5) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
(6) Human body model, 1.5 kΩ in series with 100 pF.

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ELECTRICAL CHARACTERISTICS

V^+ = +5.0V, (1), unless otherwise stated

Parameter		Conditions	LM124A			LM224A			LM324A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		T_A = 25°C (2)		1	2		1	3		2	3	mV
Input Bias Current (3)		$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		20	50		40	80		45	100	nA
Input Offset Current		$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range (4)		V^+ = 30V, (LM2902-N, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current		Over Full Temperature Range R_L = ∞ On All Op Amps V^+ = 30V (LM2902-N V^+ = 26V) V^+ = 5V		 1.5 0.7	 3 1.2		 1.5 0.7	 3 1.2		 1.5 0.7	 3 1.2	mA
Large Signal Voltage Gain		V^+ = 15V, R_L ≥ 2kΩ, (V_O = 1V to 11V), T_A = 25°C	50	100		50	100		25	100		V/mV
Common-Mode Rejection Ratio		DC, V_{CM} = 0V to V^+ − 1.5V, T_A = 25°C	70	85		70	85		65	85		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2902-N, V^+ = 5V to 26V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling (5)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)		−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C	12	50		12	50		12	50		µA
Short Circuit to Ground		V^+ = 15V, T_A = 25°C (6)		40	60		40	60		40	60	mA
Input Offset Voltage		See (2)			4			4			5	mV
V_{OS} Drift		R_S = 0Ω		7	20		7	20		7	30	µV/°C
Input Offset Current		$I_{IN(+)}$ − $I_{IN(-)}$, V_{CM} = 0V			30			30			75	nA
I_{OS} Drift		R_S = 0Ω		10	200		10	200		10	300	pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200	nA
Input Common-Mode Voltage Range (4)		V^+ = +30V (LM2902-N, V^+ = 26V)	0		V^+−2	0		V^+−2	0		V^+−2	V

(1) These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124-N/LM124A. With the LM224-N/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324-N/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902-N specifications are limited to −40°C ≤ T_A ≤ +85°C.

(2) V_O ≅ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V) for LM2902-N, V^+ from 5V to 26V.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

(4) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902-N), independent of the magnitude of V^+.

(5) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

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ELECTRICAL CHARACTERISTICS (continued)

V^+ = +5.0V, (1), unless otherwise stated

Parameter		Conditions		LM124A			LM224A			LM324A			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			25			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V	R_L = 2 kΩ	26			26			26			V
		(LM2902-N, V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		27	28		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	10	15		5	8		5	8		

ELECTRICAL CHARACTERISTICS

V^+ = +5.0V, (1), unless otherwise stated

Parameter	Conditions	LM124-N/LM224-N			LM324-N			LM2902-N			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C (2)		2	5		2	7		2	7	mV
Input Bias Current (3)	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (4)	V^+ = 30V, (LM2902-N, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range										mA
	R_L = ∞ On All Op Amps										
	V^+ = 30V (LM2902-N V^+ = 26V)		1.5	3		1.5	3		1.5	3	
	V^+ = 5V		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	V^+ = 15V, $R_L \geq$ 2kΩ, (V_O = 1V to 11V), T_A = 25°C	50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, V_{CM} = 0V to V^+ − 1.5V, T_A = 25°C	70	85		65	85		50	70		dB
Power Supply Rejection Ratio	V^+ = 5V to 30V (LM2902-N, V^+ = 5V to 26V), T_A = 25°C	65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (5)	f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)		−120			−120			−120		dB

(1) These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124-N/LM124A. With the LM224-N/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324-N/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902-N specifications are limited to −40°C ≤ T_A ≤ +85°C.

(2) $V_O \cong$ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V) for LM2902-N, V^+ from 5V to 26V.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

(4) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902-N), independent of the magnitude of V^+.

(5) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

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ELECTRICAL CHARACTERISTICS (continued)

V^+ = +5.0V, (1), unless otherwise stated

Parameter		Conditions		LM124-N/LM224-N			LM324-N			LM2902-N			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		V^+ = 15V, T_A = 25°C (6)			40	60		40	60		40	60	mA
Input Offset Voltage		See (2)				7			9			10	mV
V_{OS} Drift		R_S = 0Ω			7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				100			150		45	200	nA
I_{OS} Drift		R_S = 0Ω			10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (4)		V^+ = +30V (LM2902-N, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal		V^+ = +15V (V_OSwing = 1V to 11V)											
Voltage Gain		R_L ≥ 2 kΩ		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V	R_L = 2 kΩ	26			26			22			V
		(LM2902-N, V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		23	24		V
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	100	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	5	8		5	8		5	8		mA

(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

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TYPICAL PERFORMANCE CHARACTERISTICS

Input Voltage Range

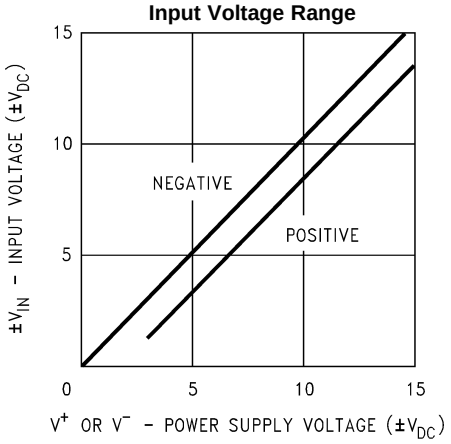


Figure 3.

Input Current

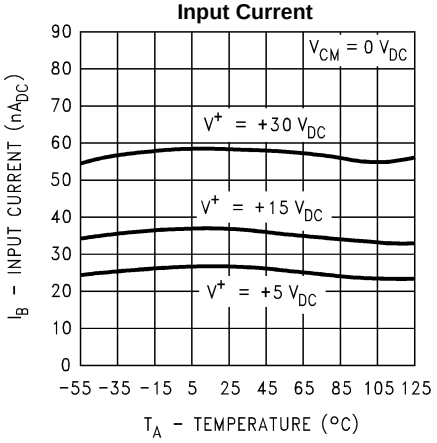


Figure 4.

Supply Current

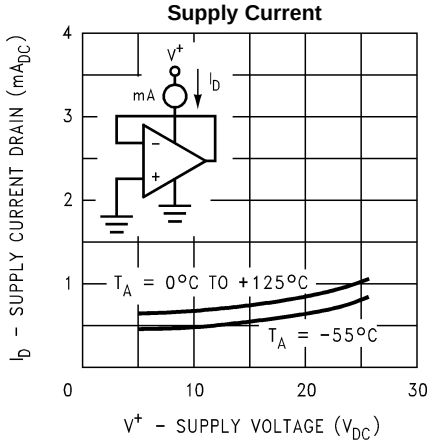


Figure 5.

Voltage Gain

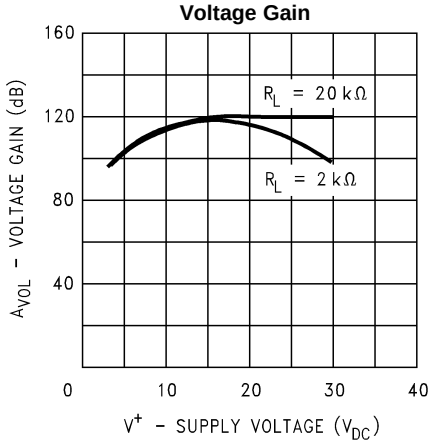


Figure 6.

Open Loop Frequency Response

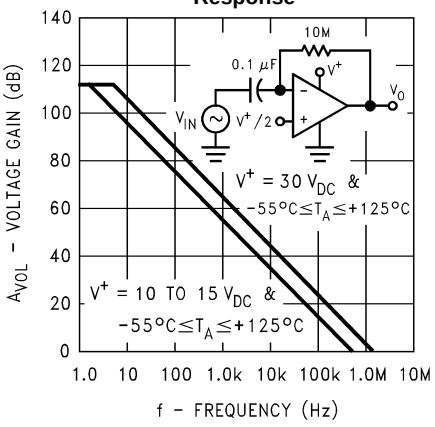


Figure 7.

Common Mode Rejection Ratio

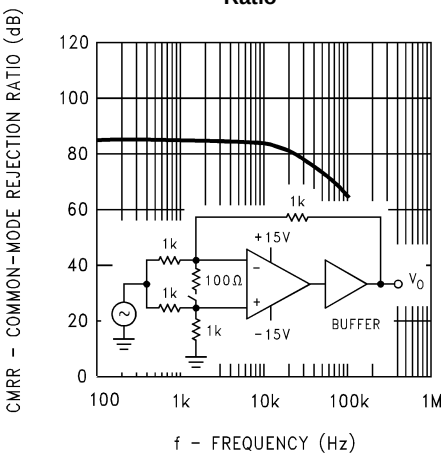


Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Voltage Follower Pulse Response

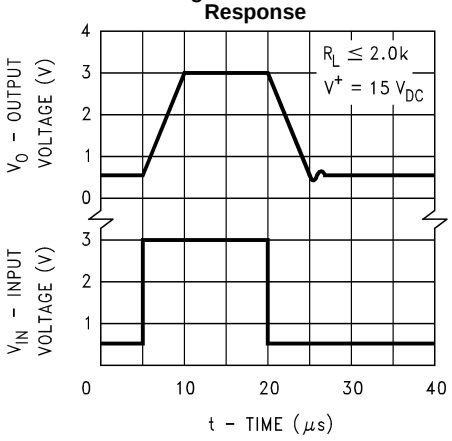


Figure 9.

Voltage Follower Pulse Response (Small Signal)

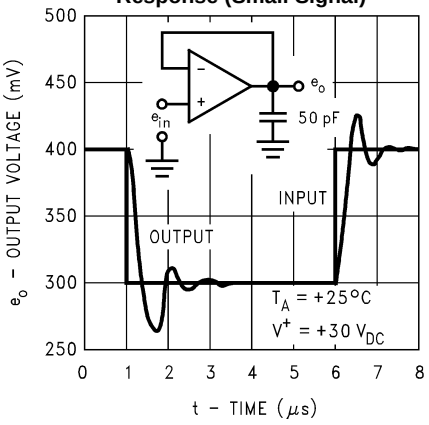


Figure 10.

Large Signal Frequency Response

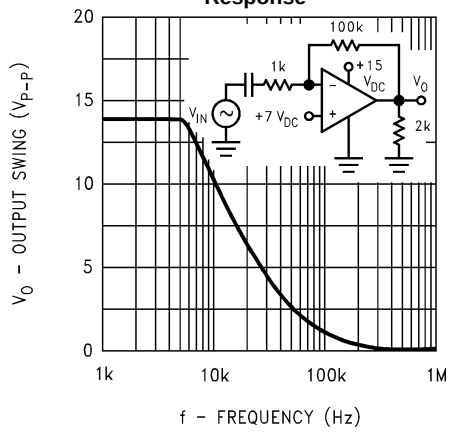


Figure 11.

Output Characteristics Current Sourcing

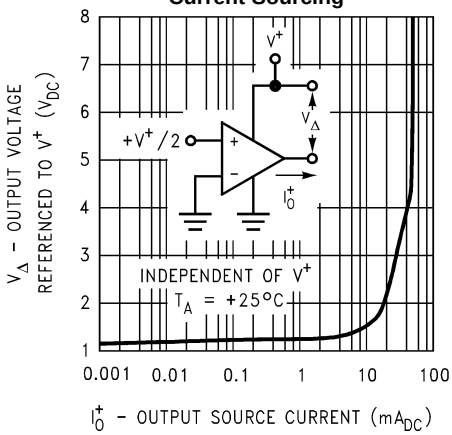


Figure 12.

Output Characteristics Current Sinking

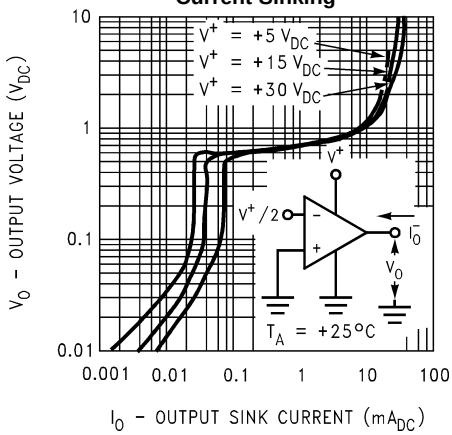


Figure 13.

Current Limiting

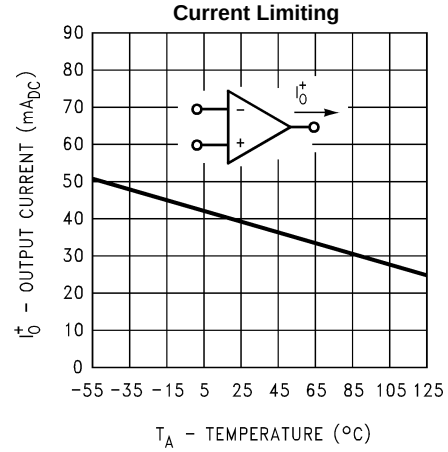


Figure 14.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Input Current (LM2902-N only)

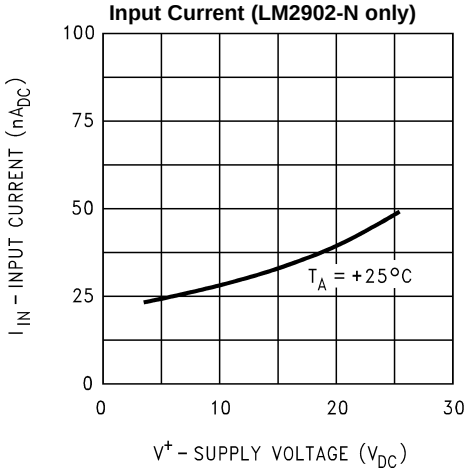


Figure 15.

Voltage Gain (LM2902-N only)

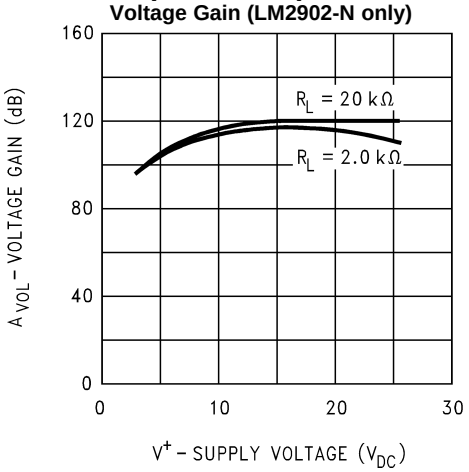


Figure 16.

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APPLICATION HINTS

The LM124-N series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM124-N establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

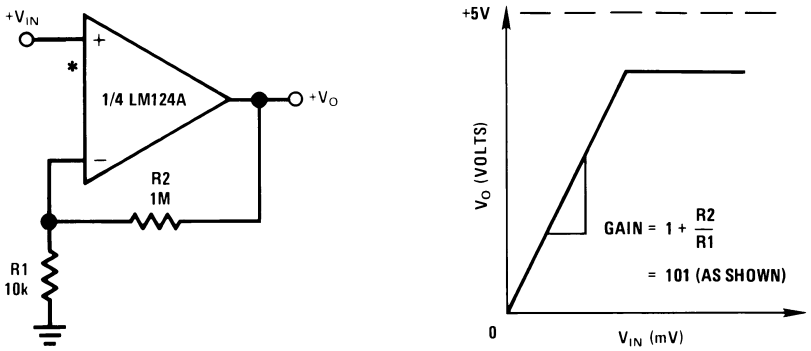
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see TYPICAL PERFORMANCE CHARACTERISTICS) than a standard IC op amp.

The circuits presented in the section on Typical Single-Supply Applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

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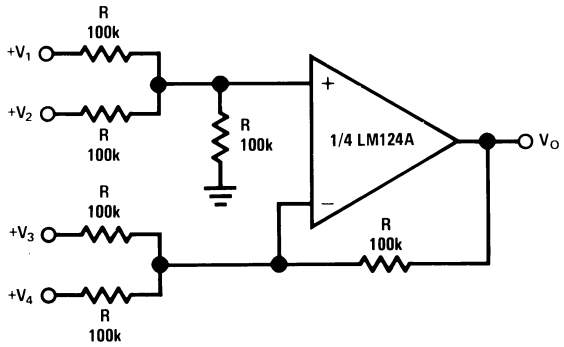
Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})



*R not needed due to temperature independent I_{IN}

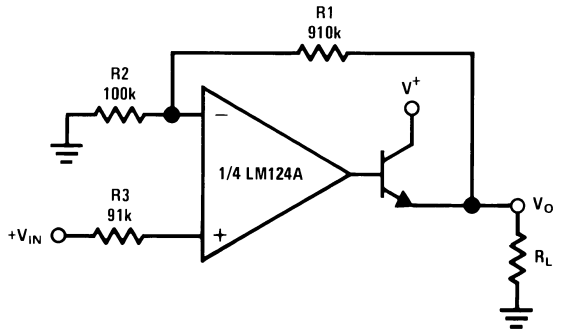
Figure 17. Non-Inverting DC Gain (0V Input = 0V Output)



Where: $V_0 = V_1 + V_2 - V_3 - V_4$

$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

Figure 18. DC Summing Amplifier ($V_{IN'S} \geq 0$ V_{DC} and $V_O \geq V_{DC}$)



$V_0 = 0$ V_{DC} for $V_{IN} = 0$ V_{DC}

$A_V = 10$

Figure 19. Power Amplifier

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(V^+ = 5.0 V_{DC})

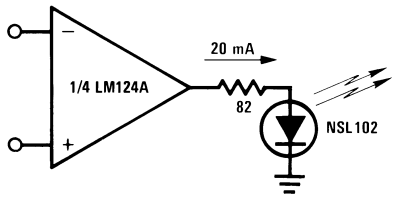
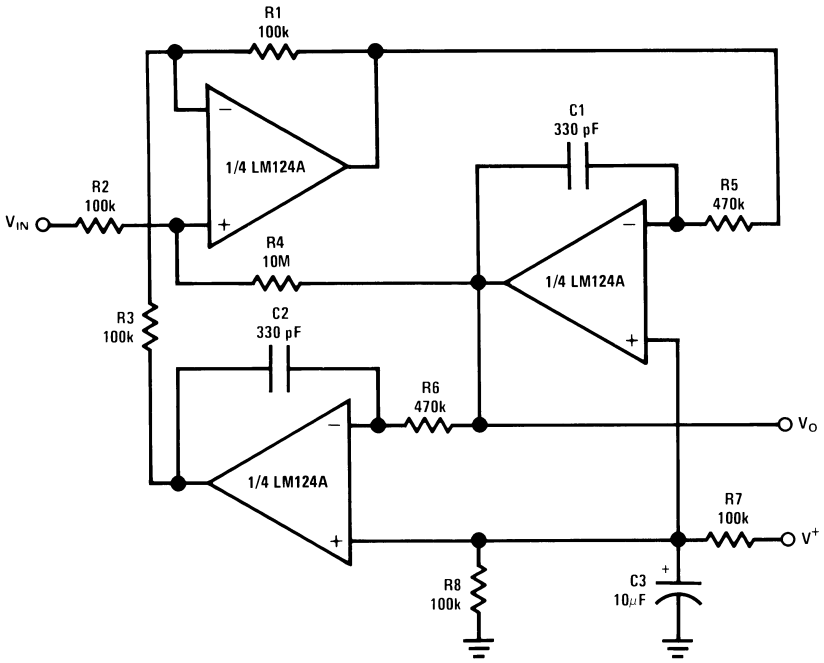


Figure 20. LED Driver

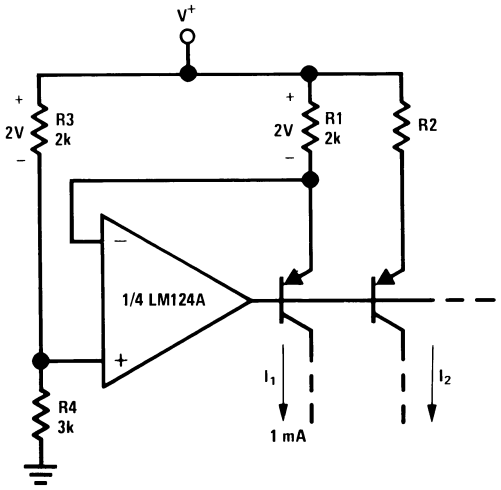


f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

Figure 21. "BI-QUAD" RC Active Bandpass Filter

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(V^+ = 5.0 V_{DC})



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Figure 22. Fixed Current Sources

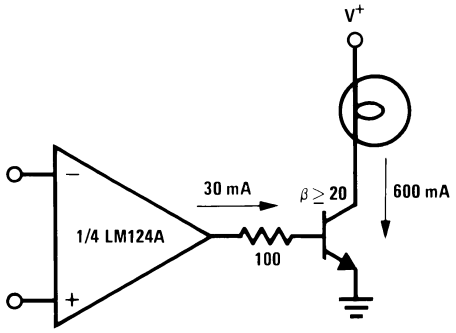
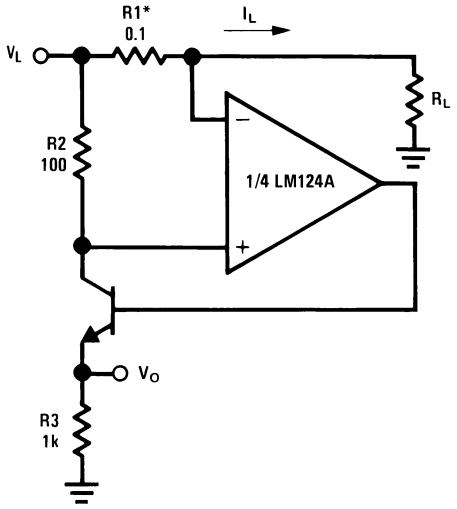


Figure 23. Lamp Driver

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($V^+ = 5.0\ V_{DC}$)



$$V_O = \frac{1V(I_L)}{1A}$$

$$V_L \leq V^+ - 2V$$

*(Increase R1 for I_L small)

Figure 24. Current Monitor

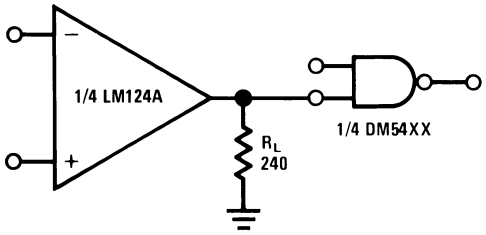


Figure 25. Driving TTL

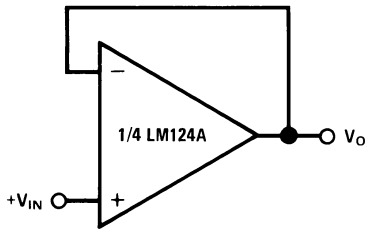


Figure 26. Voltage Follower

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($V^+ = 5.0\ V_{DC}$)

Figure 27.

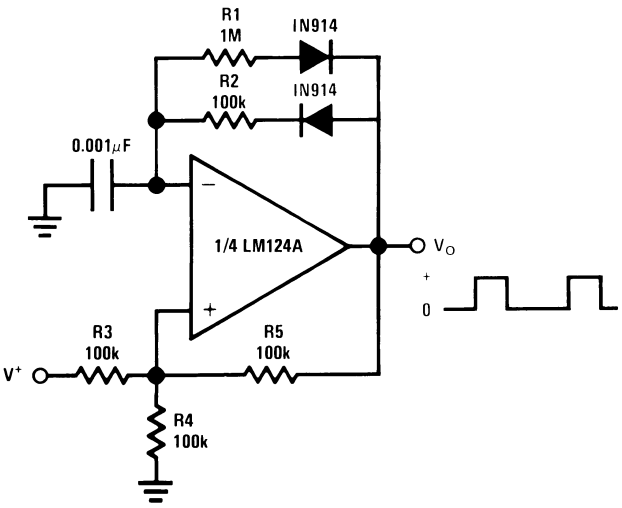


Figure 28. Pulse Generator

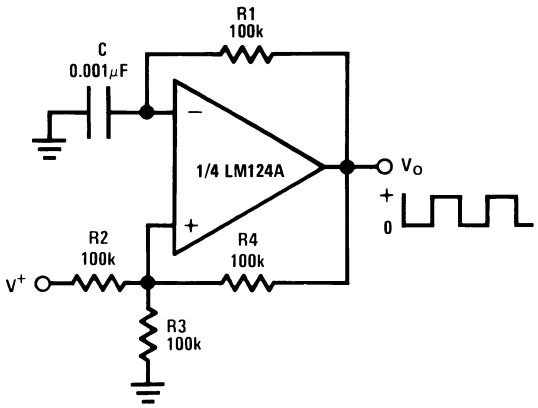


Figure 29. Squarewave Oscillator

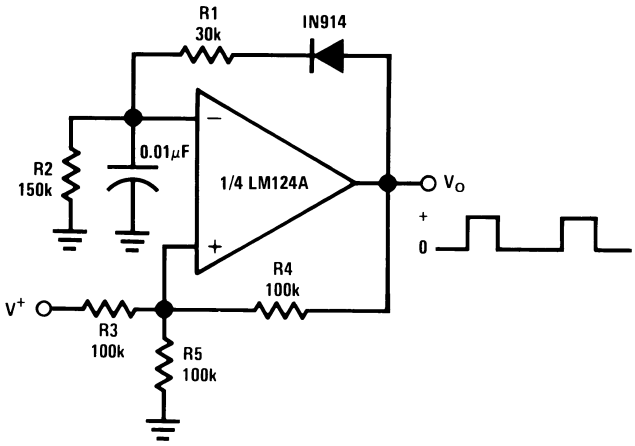
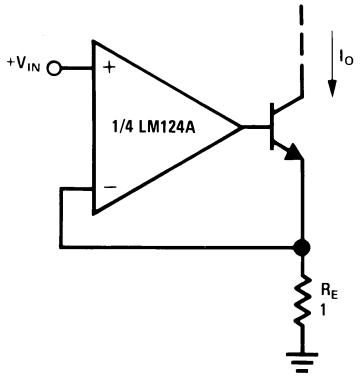


Figure 30. Pulse Generator

(V^+ = 5.0 V_{DC})



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

Figure 31. High Compliance Current Sink

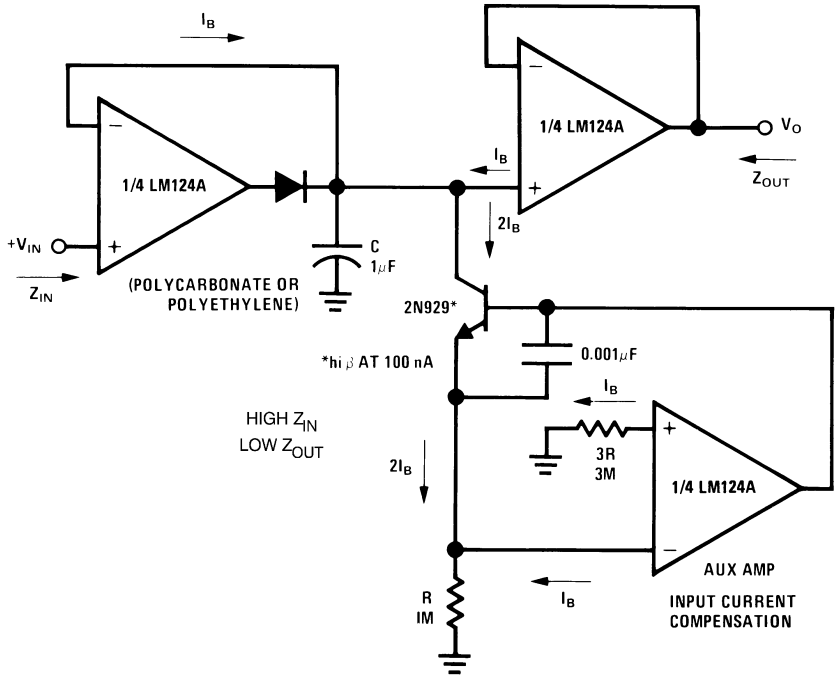


Figure 32. Low Drift Peak Detector

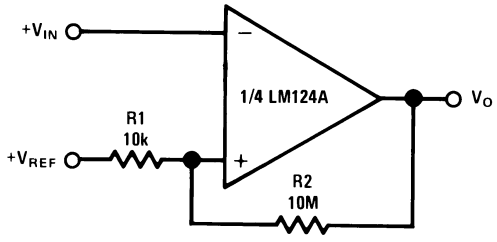
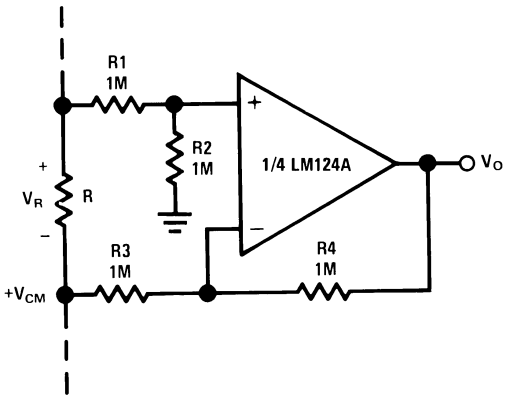


Figure 33. Comparator with Hysteresis

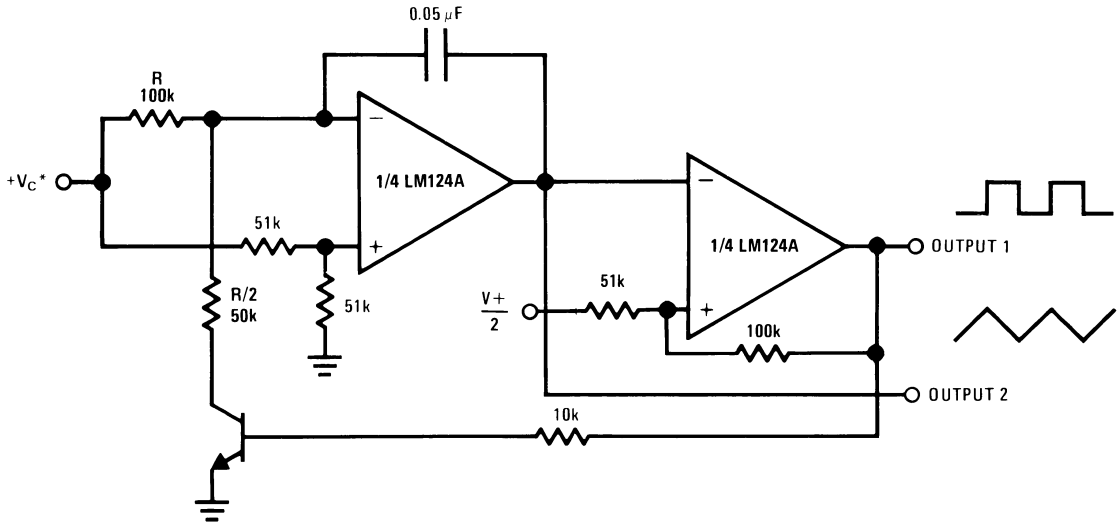
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(V^+ = 5.0 V_{DC})



$V_O = V_R$

Figure 34. Ground Referencing a Differential Input Signal



*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2$ ($V^+ - 1.5$ V_{DC})

Figure 35. Voltage Controlled Oscillator Circuit

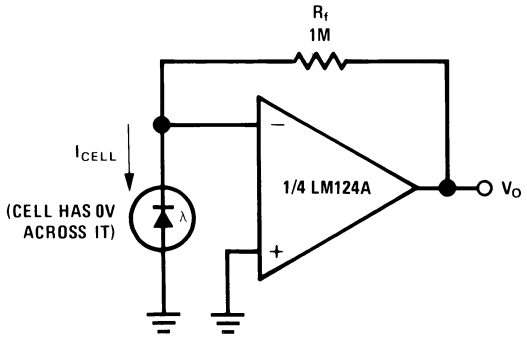
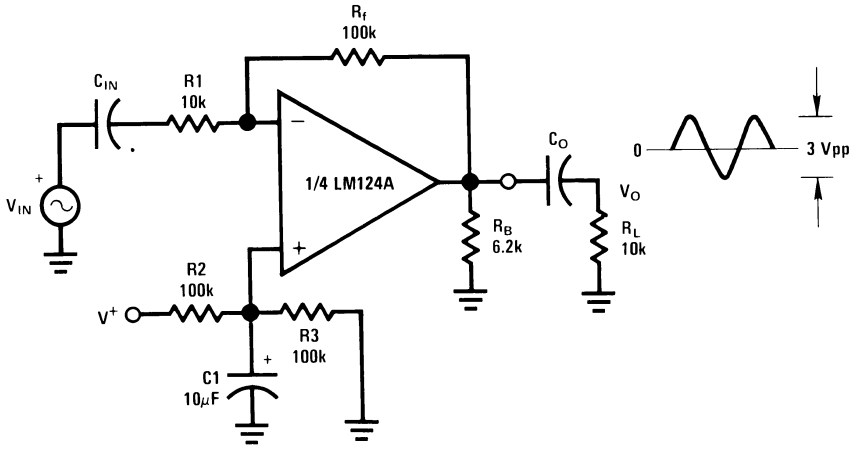


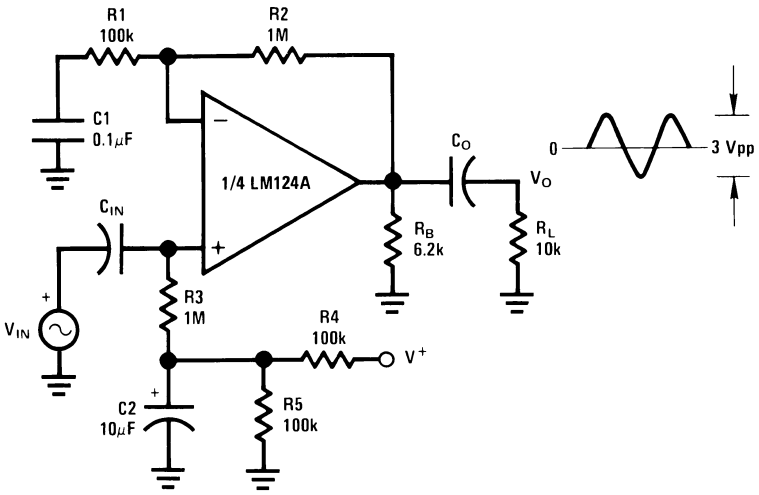
Figure 36. Photo Voltaic-Cell Amplifier

(V^+ = 5.0 V_{DC})



$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

Figure 37. AC Coupled Inverting Amplifier



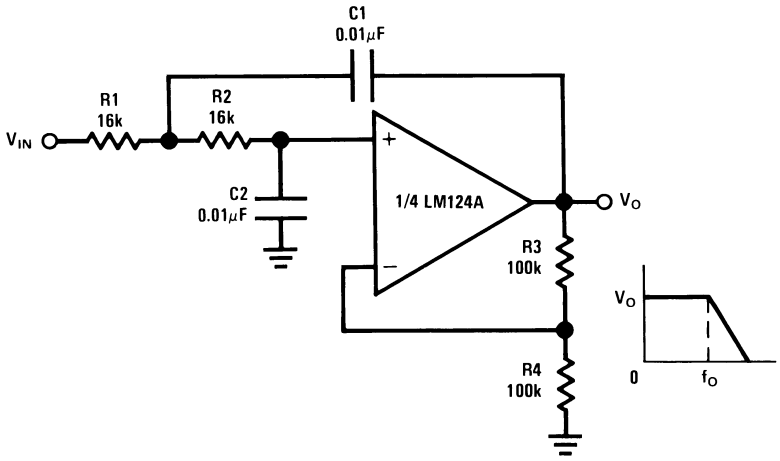
$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As shown)

Figure 38. AC Coupled Non-Inverting Amplifier

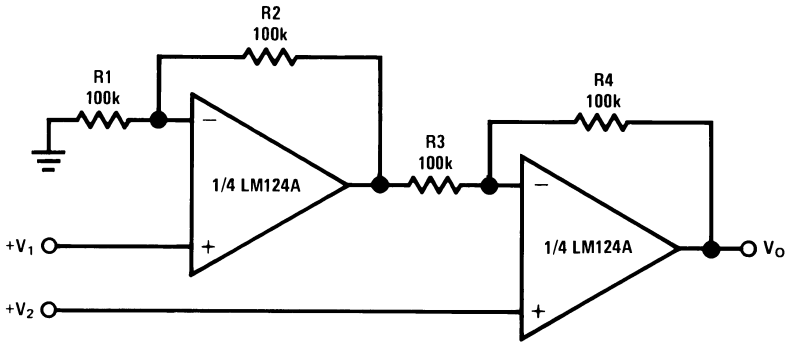
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(V^+ = 5.0 V_{DC})



f_O = 1 kHz
Q = 1
A_V = 2

Figure 39. DC Coupled Low-Pass RC Active Filter



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

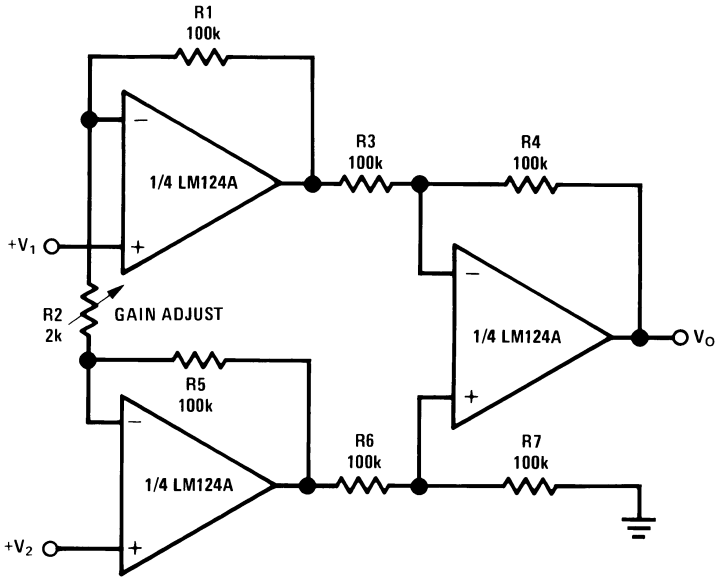
$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

Figure 40. High Input Z, DC Differential Amplifier

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(V^+ = 5.0 V_{DC})



If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\,(V_2 - V_1)$

Figure 41. High Input Z Adjustable-Gain DC Instrumentation Amplifier

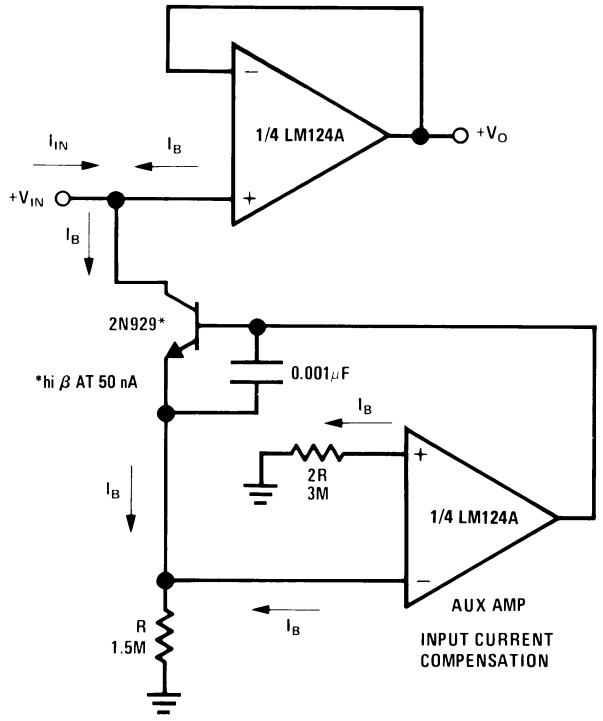
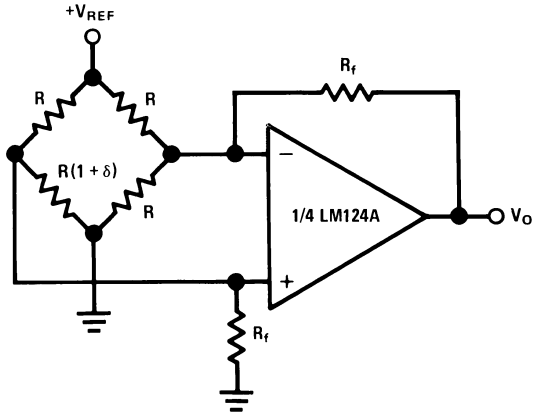


Figure 42. Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

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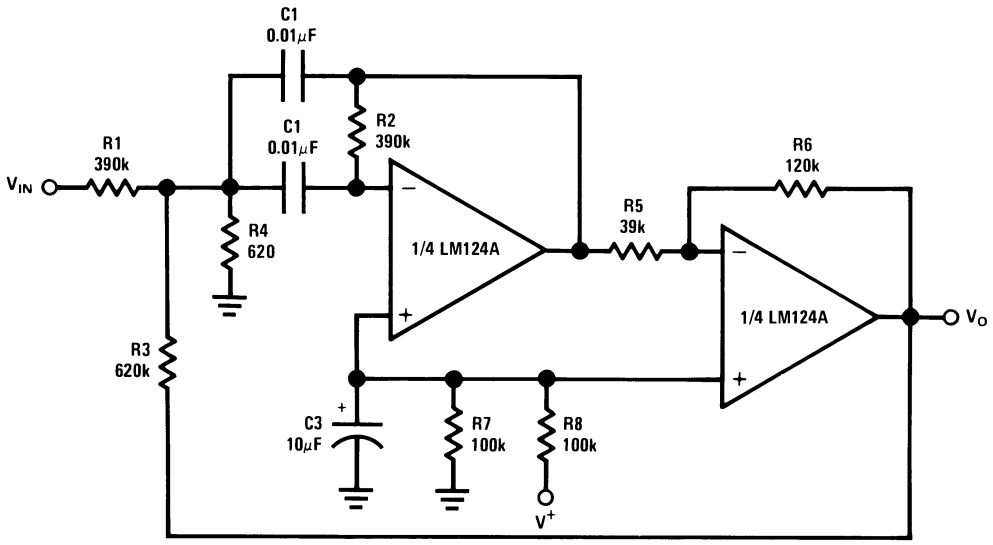
(V^+ = 5.0 V_{DC})



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Figure 43. Bridge Current Amplifier



f_O = 1 kHz
Q = 25

Figure 44. Bandpass Active Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM124AJ/PB	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI		LM124AJ	Samples
LM124J/PB	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI		LM124J	Samples
LM224J	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-25 to 85	LM224J	Samples
LM2902M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM2902M	
LM2902M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LM2902M	Samples
LM2902MT	NRND	TSSOP	PW	14	94	TBD	Call TI	Call TI	-40 to 85	LM290 2MT	
LM2902MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM290 2MT	Samples
LM2902MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM290 2MT	Samples
LM2902MX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LM2902M	
LM2902MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LM2902M	Samples
LM2902N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-NA-UNLIM	-40 to 85	LM2902N	Samples
LM2902N/PB	LIFEBUY	PDIP	NFF	14	25	TBD	Call TI	Call TI		LM2902N	
LM324AM	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM324AM	
LM324AM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM324AM	Samples
LM324AMX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70	LM324AM	
LM324AMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM324AM	Samples
LM324AN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-NA-UNLIM	0 to 70	LM324AN	Samples
LM324AN/PB	LIFEBUY	PDIP	NFF	14	25	TBD	Call TI	Call TI		LM324AN	
LM324J	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	0 to 70	LM324J	Samples
LM324M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM324M	
LM324M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM324M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM324MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM324 MT	Samples
LM324MTX	NRND	TSSOP	PW	14	2500	TBD	Call TI	Call TI	0 to 70	LM324 MT	
LM324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM324 MT	Samples
LM324MX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70	LM324M	
LM324MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM324M	Samples
LM324N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 70	LM324N	Samples
LM324N/PB	LIFEBUY	PDIP	NFF	14	25	TBD	Call TI	Call TI		LM324N	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

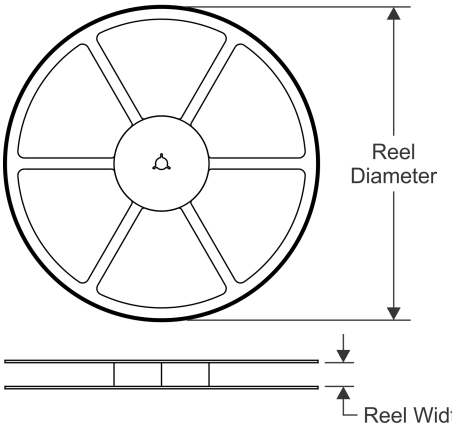
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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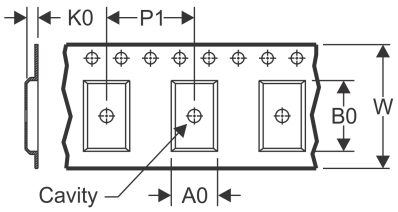
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

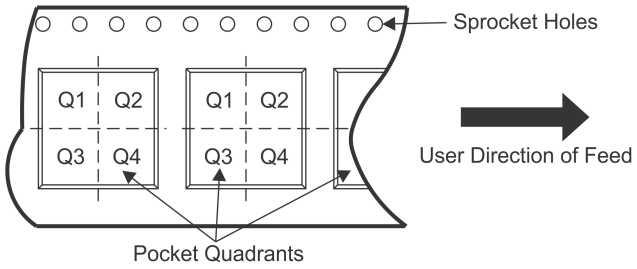


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

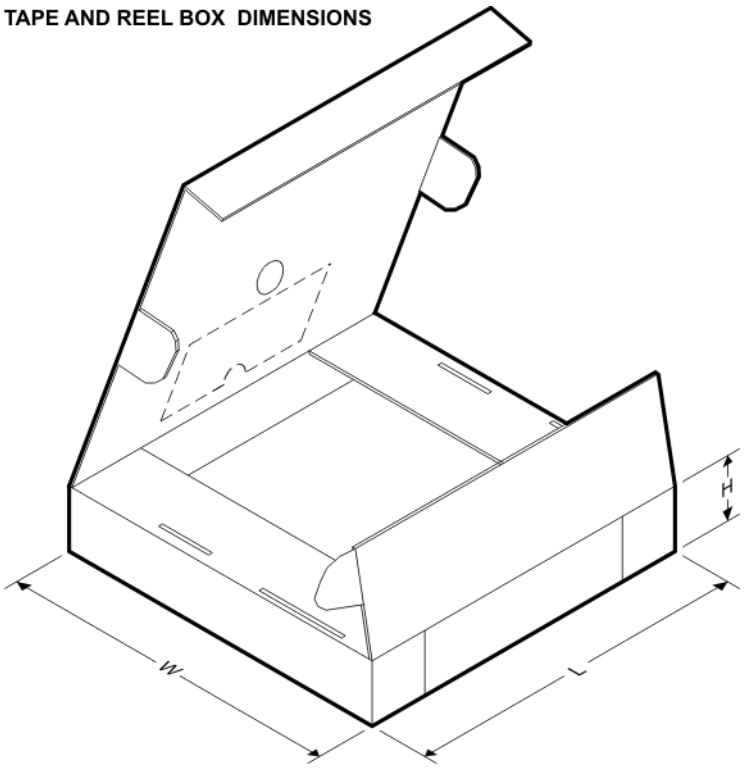
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM2902MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM2902MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM324AMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM324AMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM324MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM324MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



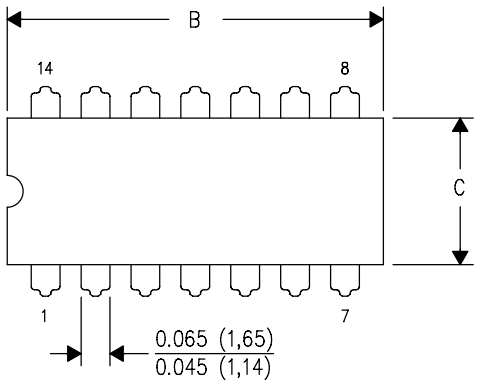
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LM2902MX	SOIC	D	14	2500	367.0	367.0	35.0
LM2902MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM324AMX	SOIC	D	14	2500	367.0	367.0	35.0
LM324AMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM324MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LM324MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LM324MX	SOIC	D	14	2500	367.0	367.0	35.0
LM324MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

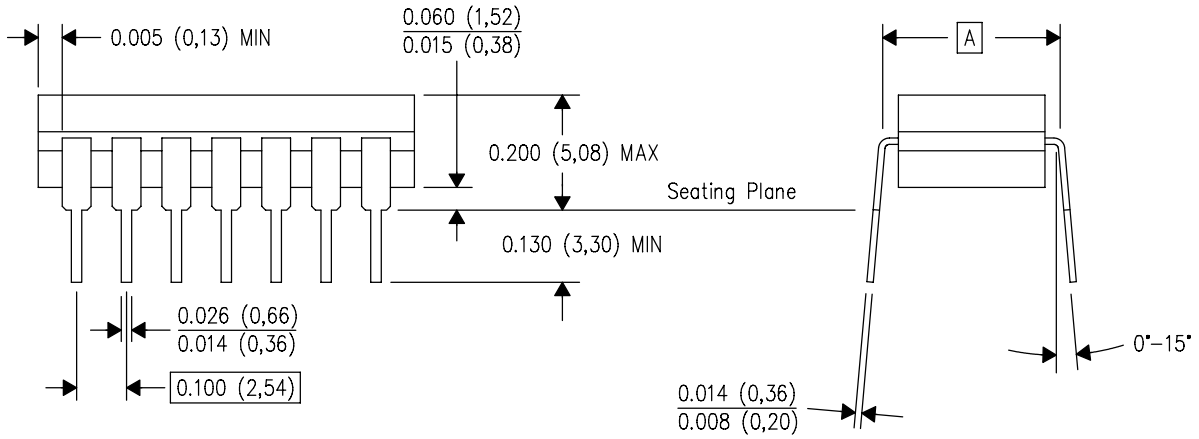
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



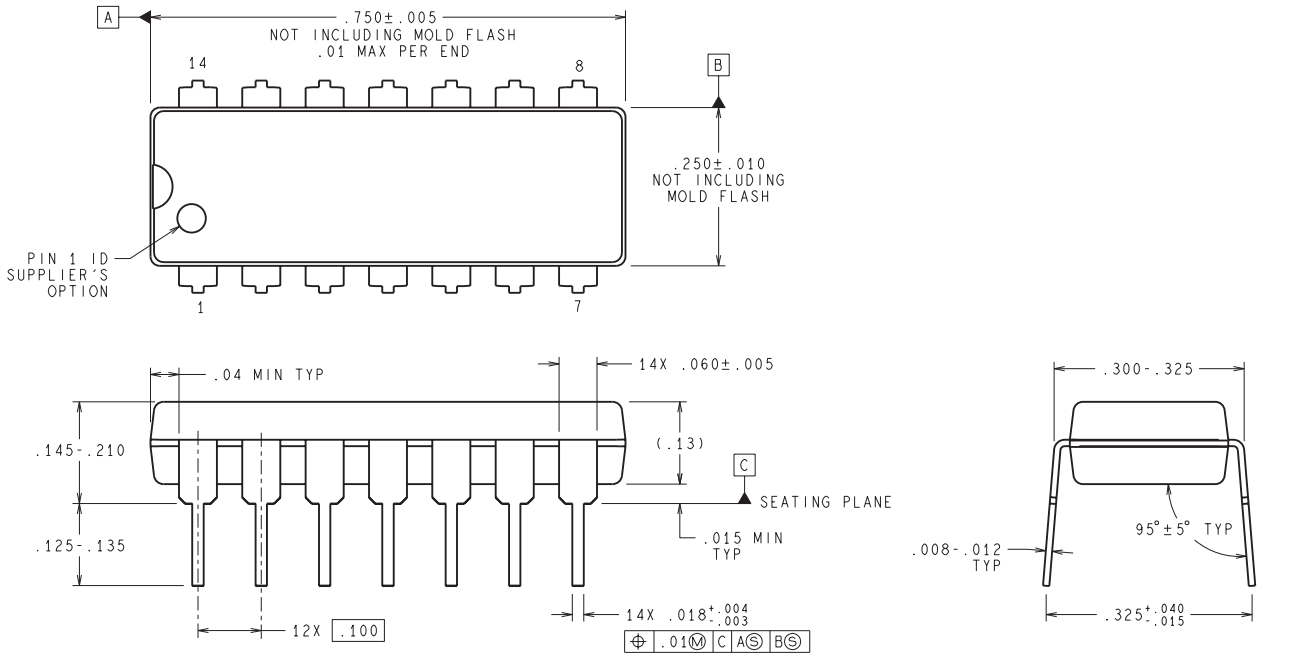
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

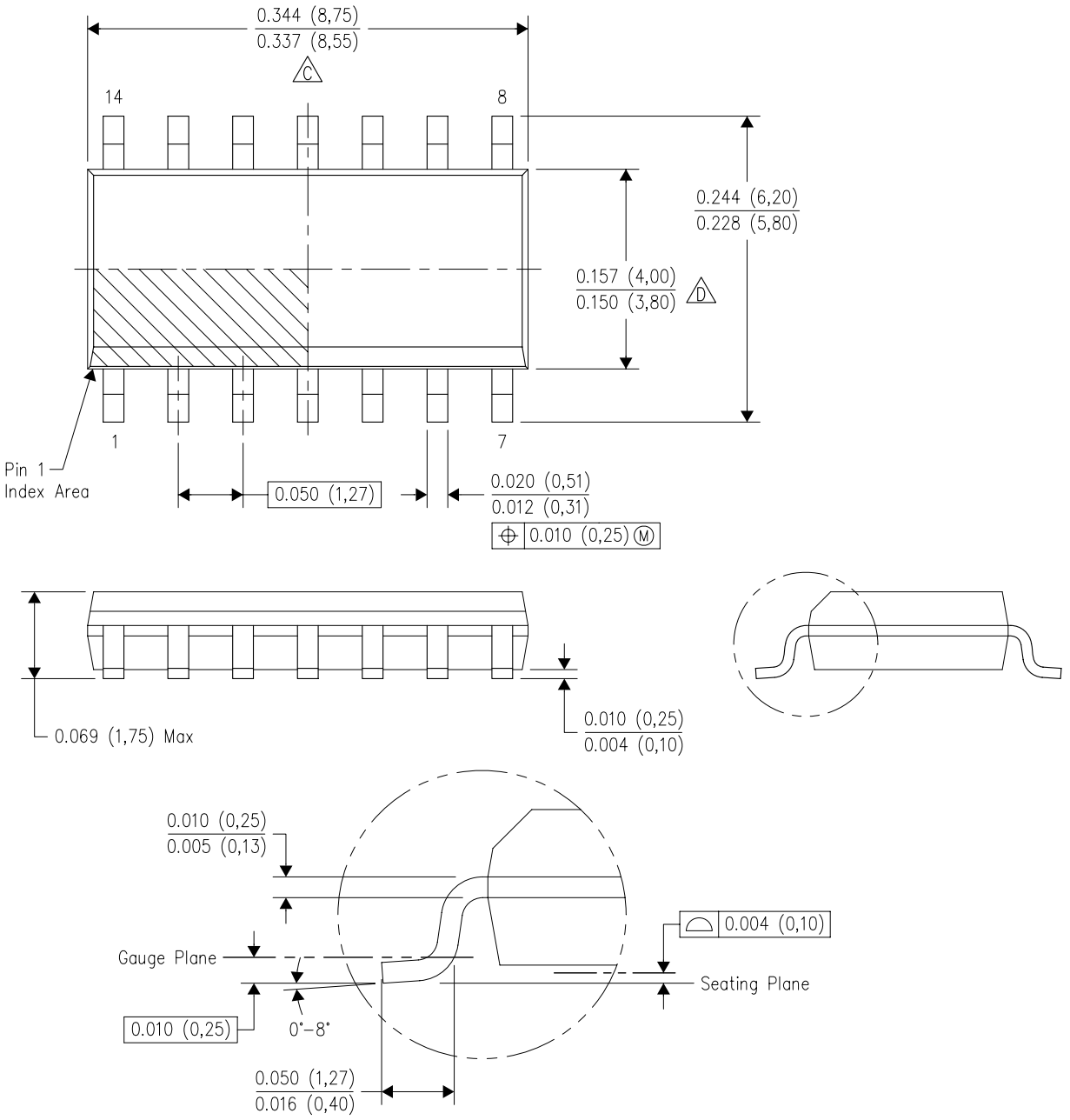
NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

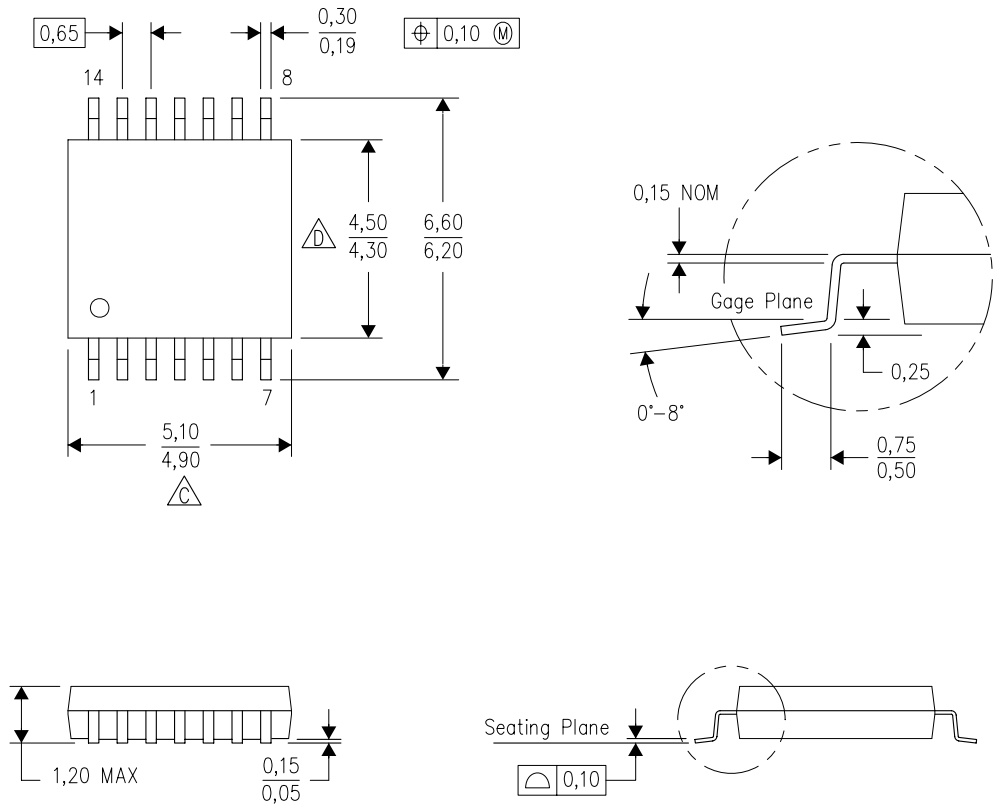
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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