24-Bit, 192-kHz Sampling, Enhanced Multilevel, Delta-Sigma, Audio Digital-to-Analog Converter

FEATURES

- **24-Bit Resolution**
- **Analog Performance (V_{CC} = 5 V):**
  - **Dynamic Range: 106 dB**
  - **SNR: 106 dB, Typical**
  - **THD+N: 0.002%, Typical**
  - **Full-Scale Output: 3.9 Vp-p, Typical**
- **4×/8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: –50 dB**
  - **Pass-Band Ripple: ±0.04 dB**
- **Sampling Frequency: 5 kHz to 200 kHz**
- **System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S With Autodetect**
- **Software Control (PCM1780, PCM1782):**
  - **Accepts 16-, 18-, 20-, and 24-Bit Audio Data**
  - **Formats: Right-Justified, I^2S, and Left-Justified**
  - **Digital Attenuation: Mode Selectable**
    - **0 dB to –63 dB, 0.5 dB/step**
    - **0 dB to –100 dB, 1 dB/step**
  - **Digital De-Emphasis**
  - **Digital Filter Rolloff: Sharp or Slow**
  - **Soft Mute**
  - **Zero Flags for Each Output**
  - **Open-Drain Output Zero Flag (PCM1782)**
- **Hardware Control (PCM1781):**
  - **I^2S and 16-Bit Word, Right-Justified**
  - **Digital De-Emphasis**
  - **Soft Mute**
  - **Zero Flag for L-, R-Channel Common Output**
- **Power Supply: 5-V Single Supply**
- **Small, 16-Lead SSOP Package (150 mil)**
- **Pin-Compatible with PCM1680**

APPLICATIONS

- **A/V Receivers**
- **DVD Movie Players**
- **DVD Add-On Cards For High-End PCs**
- **DVD Audio Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **Other Applications Requiring 24-Bit Audio**

DESCRIPTION

The PCM1780/81/82 is a CMOS, monolithic, integrated circuit, which includes stereo digital-to-analog converters and support circuitry in a small 16-lead SSOP package. The data converters use TI's enhanced multilevel delta-sigma architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1780/81/82 accepts industry standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 200 kHz are supported. The PCM1780/82 provides a full set of user-programmable functions through a three-wire serial control port, which supports register write functions. The PCM1781 provides a subset of user-programmable functions through four control pins.

The PCM1780 is pin-compatible with the PCM1680 (8-channel DAC).

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		PCM1780, PCM1781, PCM1782
Supply voltage	V_{CC}	–0.3 V to 6.5 V
Input voltage		–0.3 V to V_{CC} + 0.3 V, < 6.5 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		– 40°C to 125°C
Storage temperature		– 55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Digital and analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		36.864	MHz
	Sampling clock	32		192	kHz
Analog output load resistance		5			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution				24		Bits
DATA FORMAT							
	Audio data interface format	PCM1780, PCM1782			Right-justified, I^2S, left-justified		
		PCM1781			I^2S, right-justified		
	Audio data bit length	PCM1780, PCM1782			16-, 18-, 20-, 24-bit selectable		
		PCM1781			16–24-bit I^2S, 16-bit right-justified		
	Audio data format				MSB-first, 2s complement		
f_S	Sampling frequency			5		200	kHz
	System clock frequency				128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S		

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2			Vdc
V_{IL}					0.8	
I_{IH} (1)	Input logic current	$V_{IN} = V_{CC}$			10	µA
I_{IL} (1)		V_{IN} = 0 V			–10	
I_{IH} (2)		$V_{IN} = V_{CC}$		65	100	
I_{IL} (2)		V_{IN} = 0 V			–10	
V_{OH} (3)	Output logic level	I_{OH} = –1 mA	2.4			Vdc
V_{OL} (4)		I_{OL} = 1 mA			0.4	
DYNAMIC PERFORMANCE (5)						
THD+N	Total harmonic distortion + noise	V_{OUT} = 0 dB, f_S = 48 kHz		0.002%	0.006%	
		V_{OUT} = 0 dB, f_S = 96 kHz, system clock = 256 f_S		0.003%		
		V_{OUT} = 0 dB, f_S = 192 kHz, system clock = 128 f_S		0.004%		
	Dynamic range	EIAJ, A-weighted, f_S = 48 kHz	100	106		dB
		A-weighted, f_S = 96 kHz, system clock = 256 f_S		104		
		A-weighted, f_S = 192 kHz, system clock = 128 f_S		102		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 48 kHz	100	106		dB
		A-weighted, f_S = 96 kHz, system clock = 256 f_S		104		
		A-weighted, f_S = 192 kHz, system clock = 128 f_S		102		
	Channel separation	f_S = 48 kHz	97	103		dB
		f_S = 96 kHz, system clock = 256 f_S		101		
		f_S = 192 kHz, system clock = 128 f_S		100		
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±6	% of FSR
	Bipolar zero error	V_{OUT} = 49% of V_{CC} at BPZ input		±30	±80	mV
ANALOG OUTPUT						
	Output voltage	Full scale (–0 dB)		0.78 V_{CC}		Vp-p
	Bipolar zero voltage			0.49 V_{CC}		Vdc
	Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE						
Filter Characteristics (Sharp Rolloff)						
	Pass band	±0.04 dB			0.454 f_S	
	Stop band		0.546 f_S			
	Pass-band ripple				0.04	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–50			dB

(1) Pins 5, 6, 7, 8: SCK, DATA, BCK, LRCK
(2) Pins 2, 3, 4: $\overline{MS}$, MC, MD (PCM1780/PCM1782). Pins 1, 2, 3, 4: FMT, DEMP0, DEMP1, MUTE (PCM1781)
(3) Pins 1, 16: ZEROL, ZEROR (PCM1780). Pin 16: ZEROA (PCM1781)
(4) Pins 1, 16: ZEROL, ZEROR (PCM1780/PCM1782). Pin 16: ZEROA (PCM1781)
(5) Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™.

ELECTRICAL CHARACTERISTICS (continued)

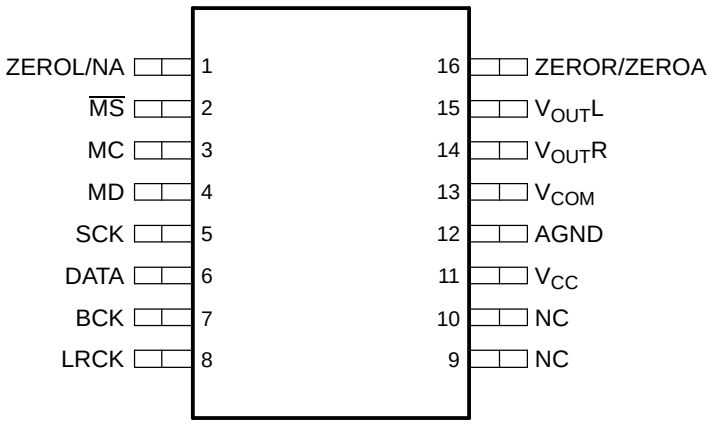
All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter Characteristics (Slow Rolloff, PCM1780/PCM1782)						
	Pass band	±0.5 dB			0.198 f_S	
	Stop band		0.884 f_S			
	Pass-band ripple				±0.5	dB
	Stop-band attenuation	Stop band = 0.884 f_S	–35			dB
	Delay time			20/f_S		s
	De-emphasis error			±0.1		dB
ANALOG FILTER PERFORMANCE						
	Frequency response	at 20 kHz		–0.02		dB
		at 44 kHz		–0.07		
POWER SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	Vdc
I_{CC}	Supply current	f_S = 48 kHz		25	40	mA
		f_S = 96 kHz, system clock = 256 f_S		30		
		f_S = 192 kHz, system clock = 128 f_S		30		
	Power dissipation	f_S = 48 kHz		125	200	mW
		f_S = 96 kHz, system clock = 256 f_S		150		
		f_S = 192 kHz, system clock = 128 f_S		150		
TEMPERATURE RANGE						
T_A	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance			115		°C/W

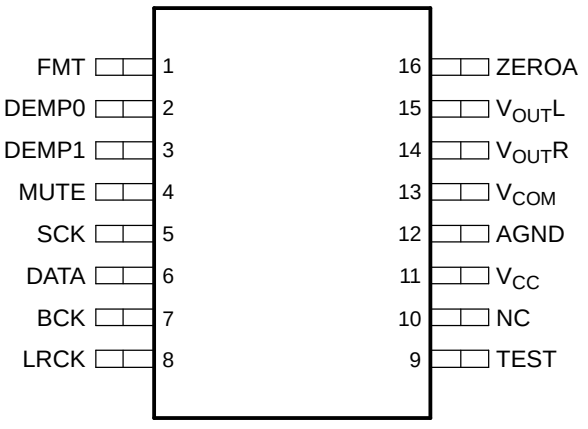
DEVICE INFORMATION

PIN ASSIGNMENTS

PCM1780/PCM1782 (TOP VIEW)



PCM1781 (TOP VIEW)



P0014-01

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS—PCM1780/PCM1782

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	12	–	Ground
BCK	7	I	Audio data bit clock input(1)
DATA	6	I	Audio data digital input(1)
LRCK	8	I	Audio data left and right clock input(1)
MC	3	I	Mode control clock input(1)(2)
MD	4	I	Mode control data input (1)(2)
$\overline{MS}$	2	I	Mode control select input(1)(2)
NC	9, 10	–	No connection
SCK	5	I	System clock input(1)
V_{CC}	11	–	Power supply, 5-V
V_{COM}	13	–	Common voltage decoupling
$V_{OUT}L$	15	O	Analog output for L-channel
$V_{OUT}R$	14	O	Analog output for R-channel
ZEROL/NA	1	O	Zero flag output for L-channel / No assign(3)
ZEROR/ZEROA	16	O	Zero flag output for R-channel / Zero flag output for L- and R-channels(3)

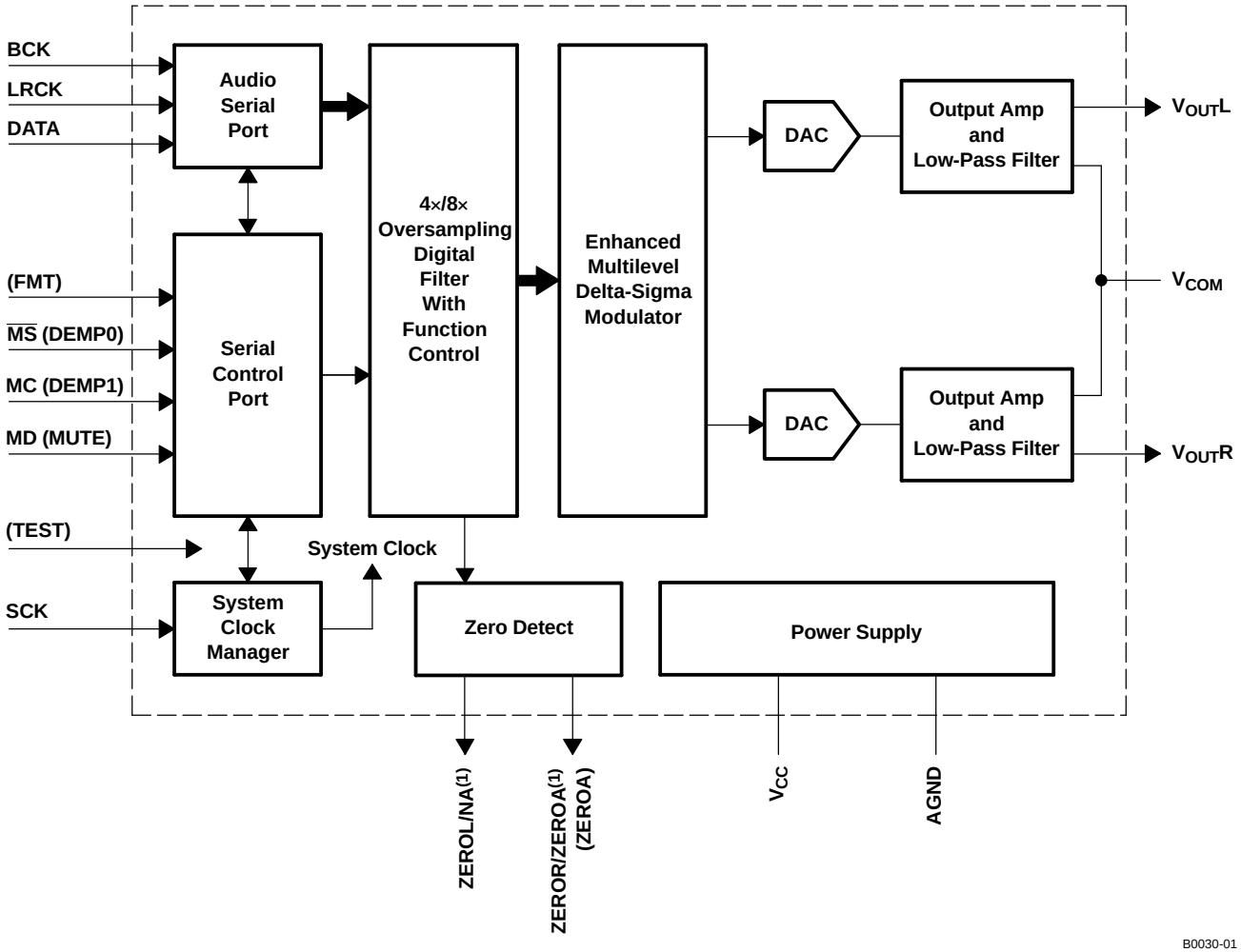
(1) Schmitt-trigger input
(2) Pulldown
(3) Open-drain output (PCM1782)

TERMINAL FUNCTIONS—PCM1781

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	12	–	Ground
BCK	7	I	Audio data bit clock input(1)
DATA	6	I	Audio data digital input(1)
DEMP0	2	I	De-emphasis control(1)(2)
DEMP1	3	I	De-emphasis control(1)(2)
FMT	1	I	Data format select(1)(2)
LRCK	8	I	Audio data left and right clock input(1)
MUTE	4	I	Soft mute control(1)(2)
NC	10	–	No connection
SCK	5	I	System clock input(1)
TEST	9	–	Test pin for factory use. Must be LOW or open(1)(2)
V_{CC}	11	–	Power supply, 5-V
V_{COM}	13	–	Common voltage decoupling
$V_{OUT}L$	15	O	Analog output for L-channel
$V_{OUT}R$	14	O	Analog output for R-channel
ZEROA	16	O	Zero flag output for L- and R-channels

(1) Schmitt-trigger input
(2) Pulldown

Functional Block Diagram



(1) Open-drain output for the PCM1782

NOTE: Signal names in parentheses ( ) are for the PCM1781.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

Digital Filter (De-Emphasis Off)

FREQUENCY RESPONSE
(SHARP ROLLOFF)

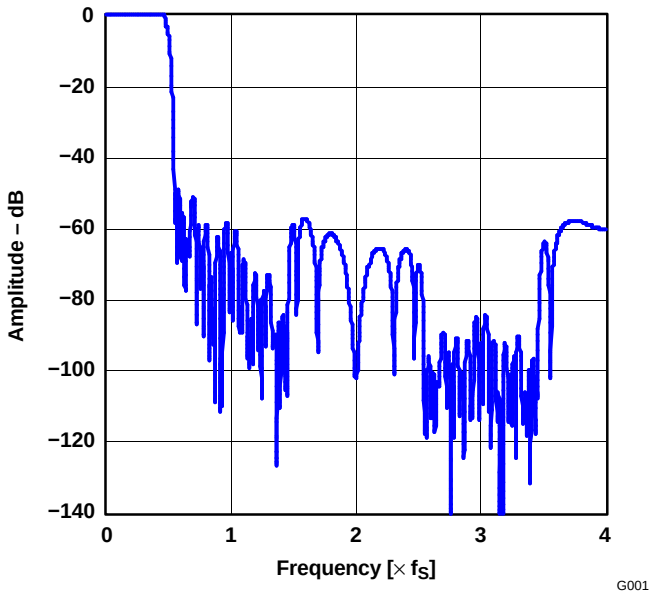


Figure 1.

PASS-BAND FREQUENCY RESPONSE
(SHARP ROLLOFF)

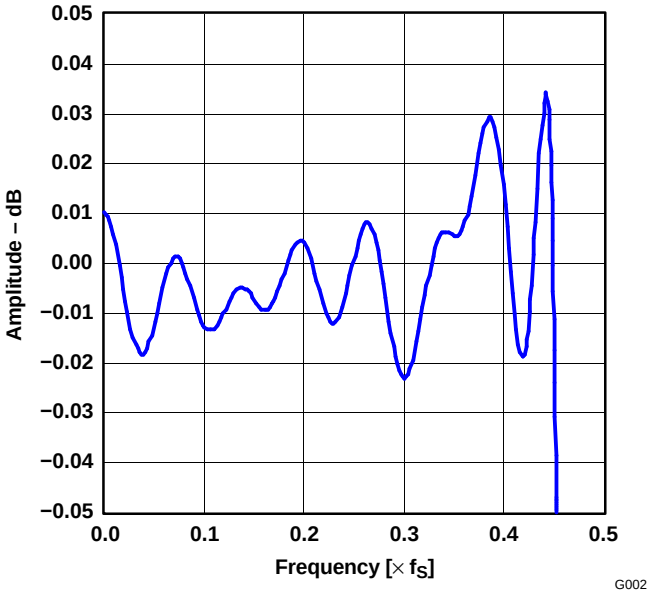


Figure 2.

FREQUENCY RESPONSE
(SLOW ROLLOFF)

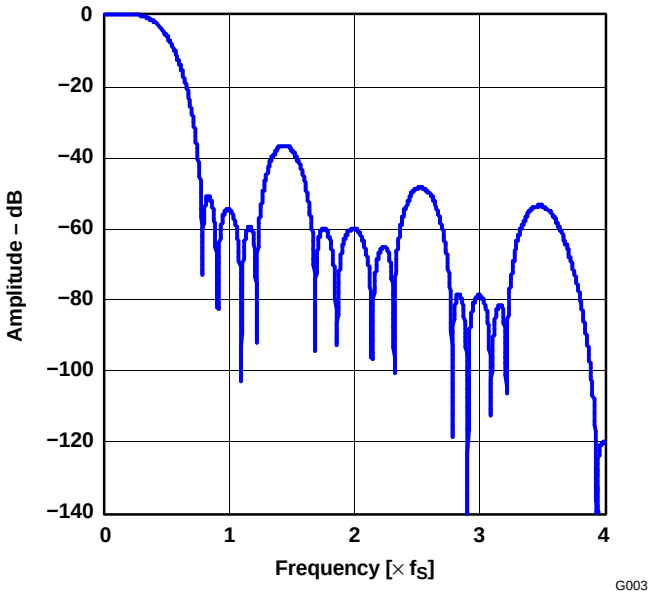


Figure 3.

TRANSITION CHARACTERISTICS
(SLOW ROLLOFF)

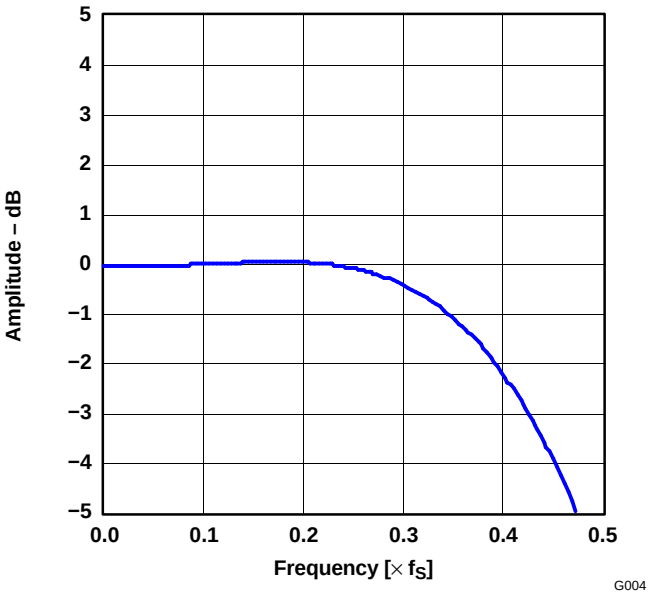


Figure 4.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

De-Emphasis Filter

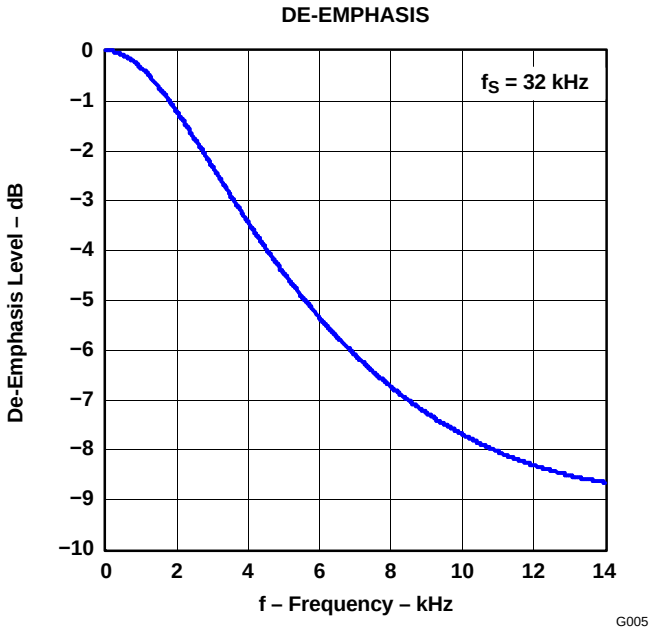


Figure 5.

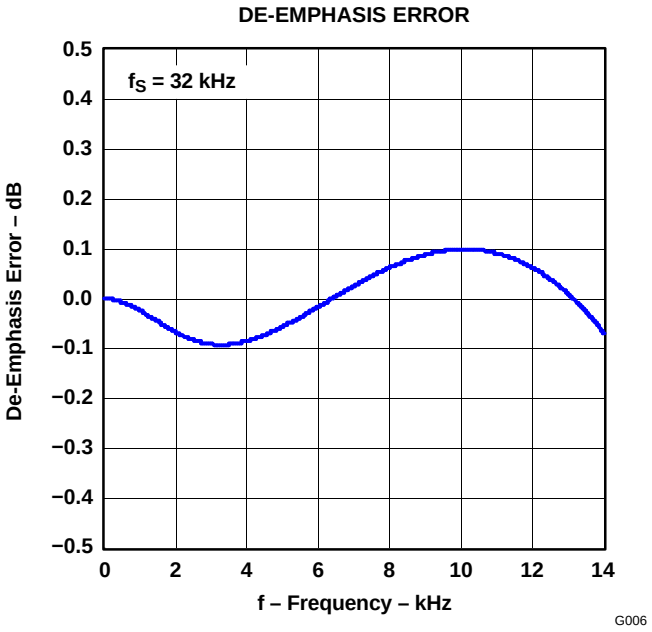


Figure 6.

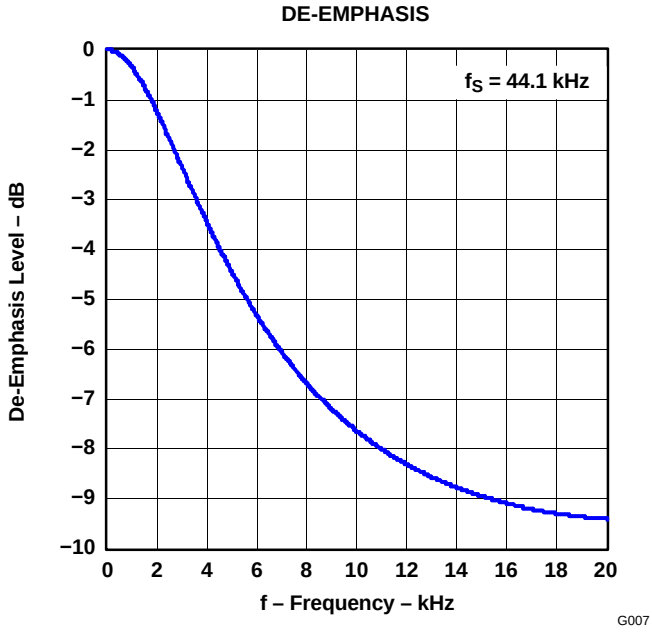


Figure 7.

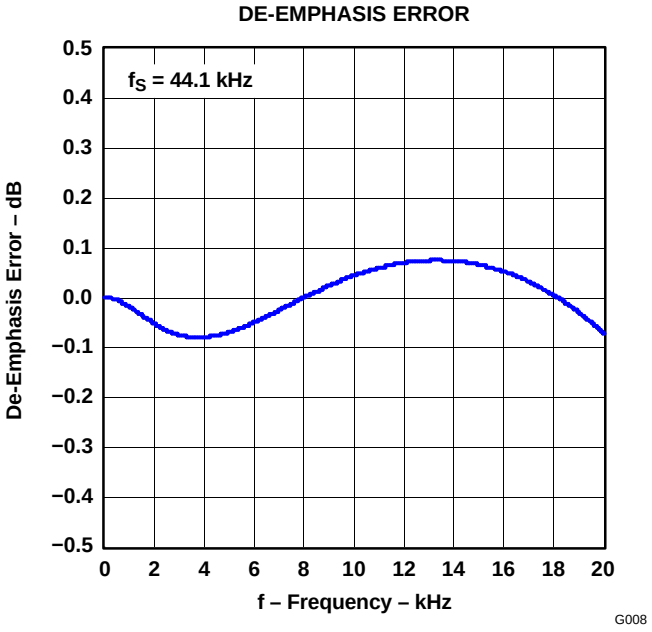


Figure 8.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

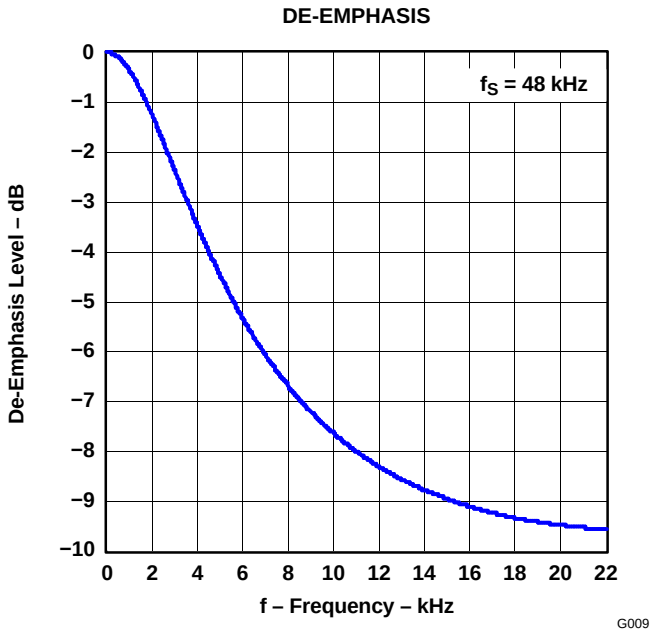


Figure 9.

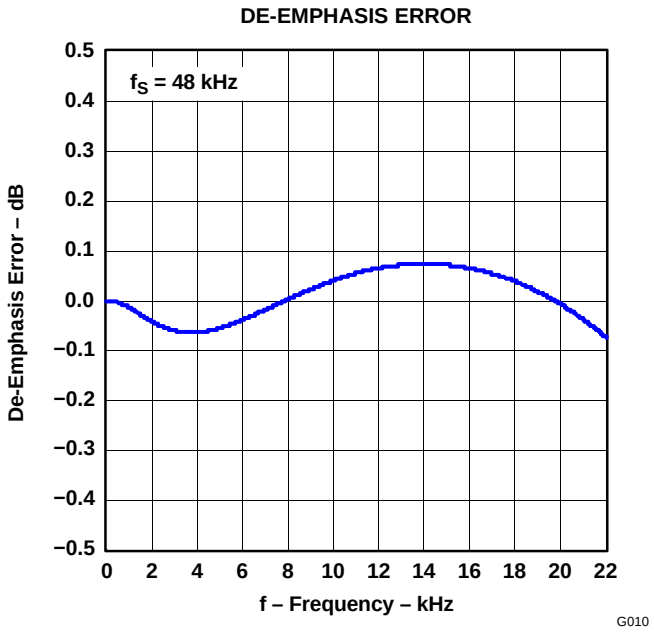


Figure 10.

Analog Filter

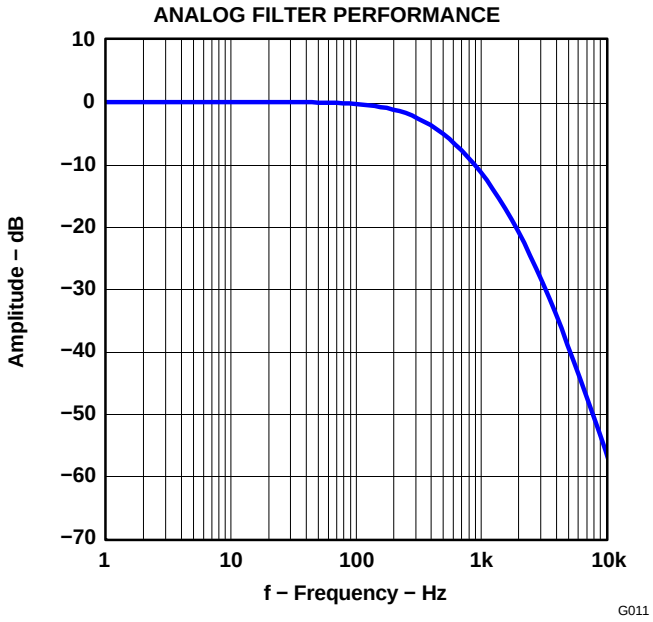


Figure 11.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

Analog Dynamic Performance

Supply Voltage Characteristics

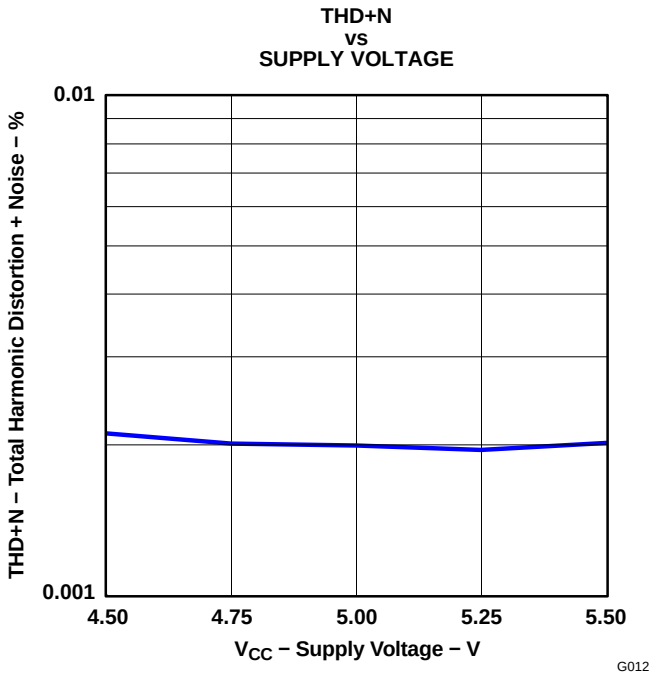


Figure 12.

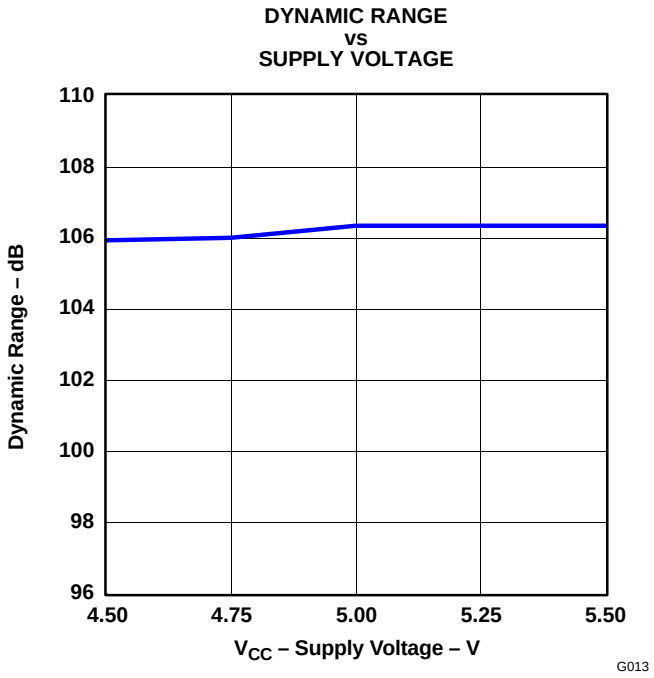


Figure 13.

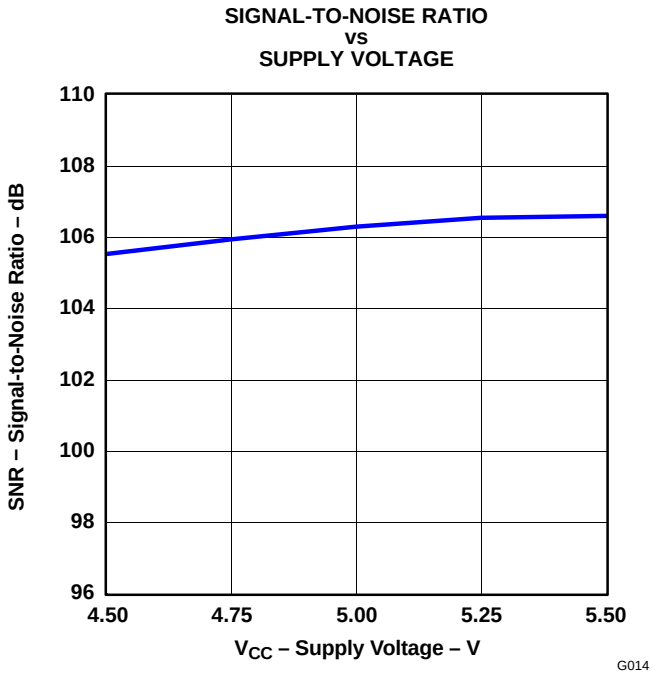


Figure 14.

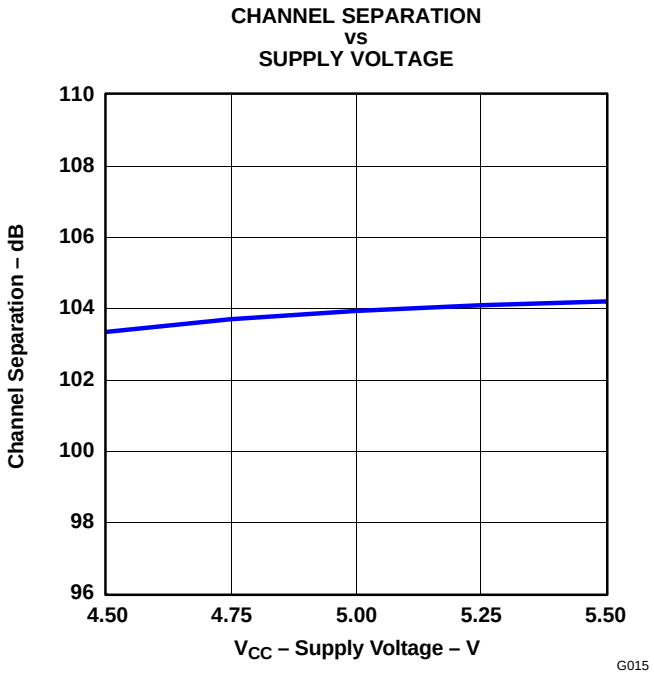


Figure 15.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted

Temperature Characteristics

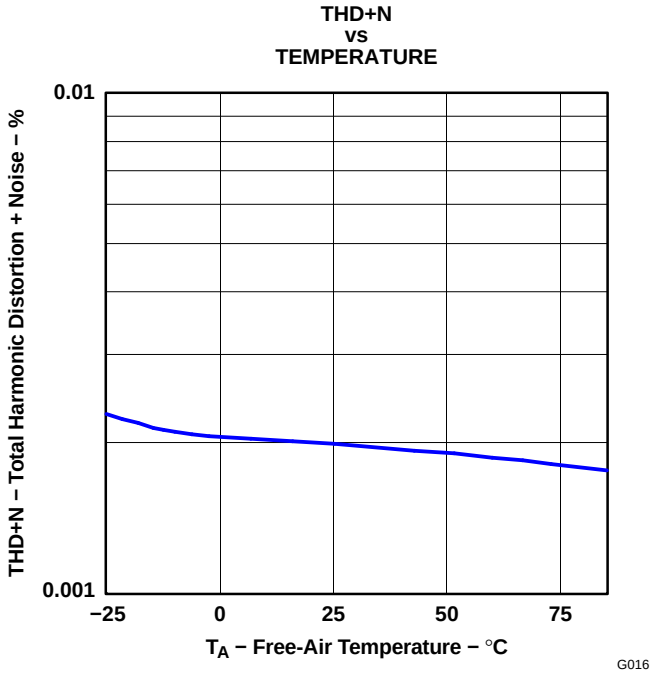


Figure 16.

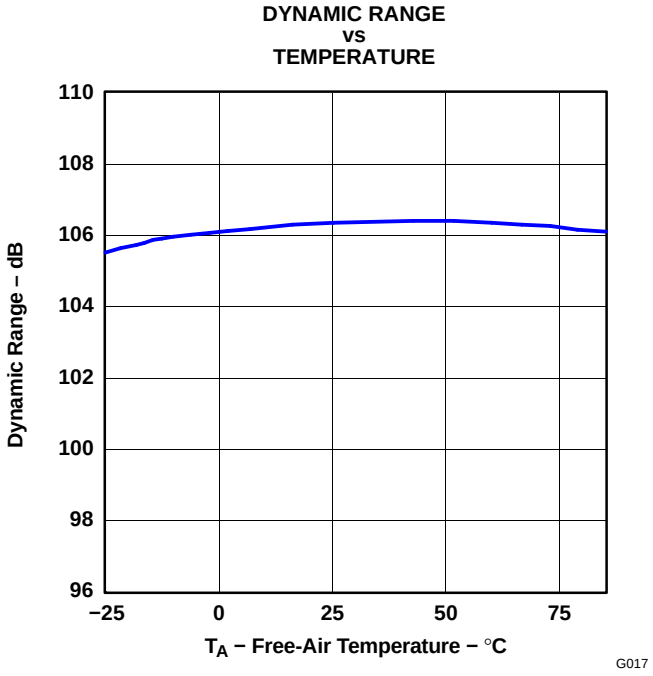


Figure 17.

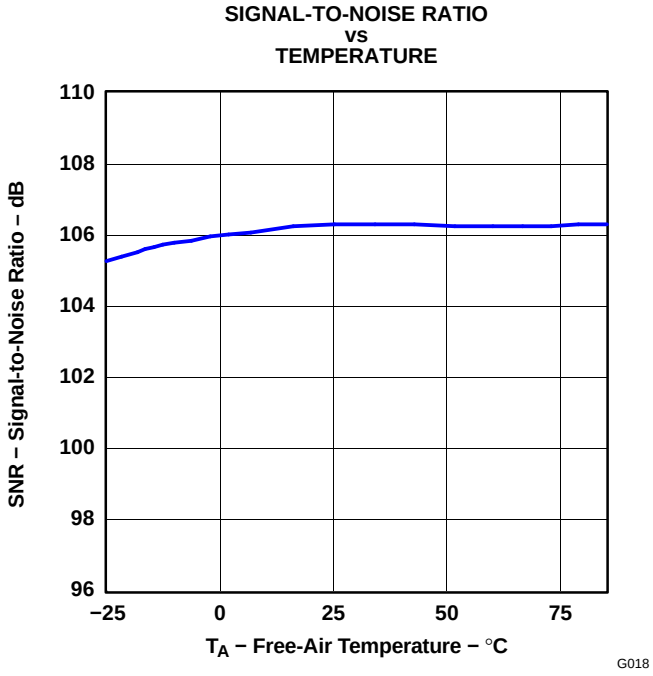


Figure 18.

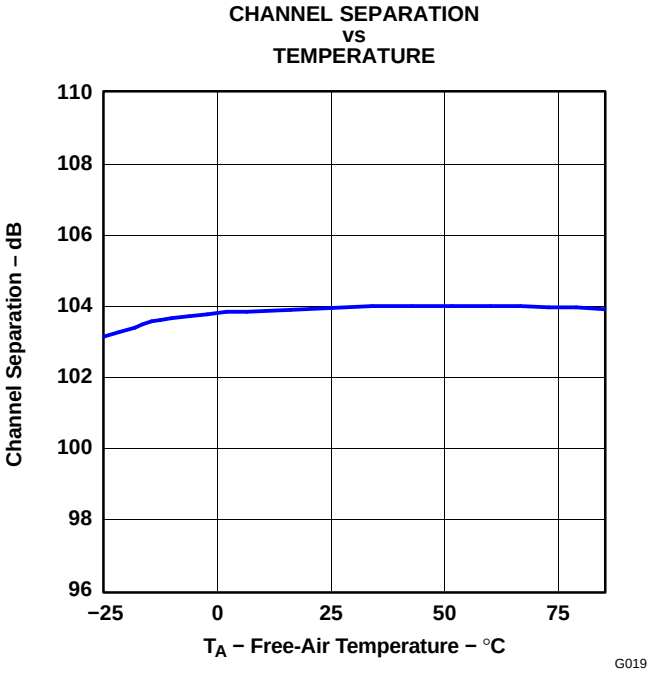


Figure 19.

SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

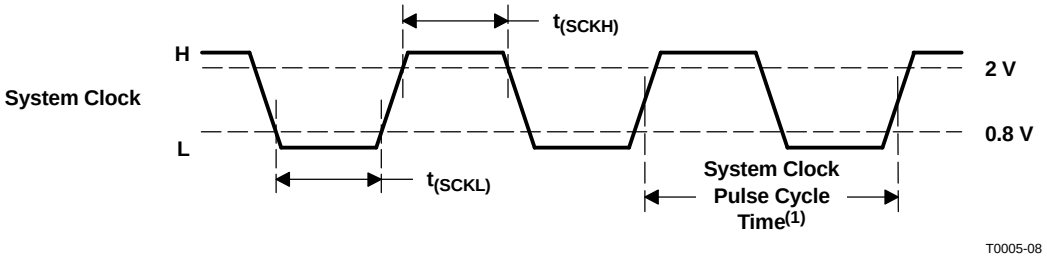
The PCM1780/81/82 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 5). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 20 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. TI's PLL170x family of multiclock generators is an excellent choice for providing the PCM1780/81/82 system clock.

Table 1. System Clock Frequencies for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCK}), MHz						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	–(1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	–(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	–(1)	–(1)	–(1)
96 kHz	12.288	18.432	24.576	36.864	–(1)	–(1)	–(1)
192 kHz	24.576	36.864	–(1)	–(1)	–(1)	–(1)	–(1)

(1) This system clock frequency is not supported for the given sampling frequency.



(1) 1/128 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(SCKH)}$	System clock pulse duration, HIGH	7			ns
$t_{(SCKL)}$	System clock pulse duration, LOW	7			ns

Figure 20. System Clock Input Timing

Power-On-Reset Functions

The PCM1780/81/82 includes a power-on-reset function. Figure 21 shows the operation of this function. With the system clock active and V_{CC} > 3 V (typical, 2.2 V to 3.7 V), the power-on-reset function is enabled. The initialization sequence requires 3072 system clocks from the time V_{CC} > 3 V (typical, 2.2 V to 3.7 V). After the initialization period, the PCM1780/82 is set to its reset default state, as described in the *Mode Control Register* section of this data sheet.

During the reset period (3072 system clocks), the analog output is forced to the common voltage (V_{COM}), or V_{CC}/2. After the reset period, the internal register is initialized in the next $1/f_S$ period and if SCK, BCK, and LRCK are provided continuously, the PCM1780/81/82 provides the proper analog output with a group delay corresponding to the input data.

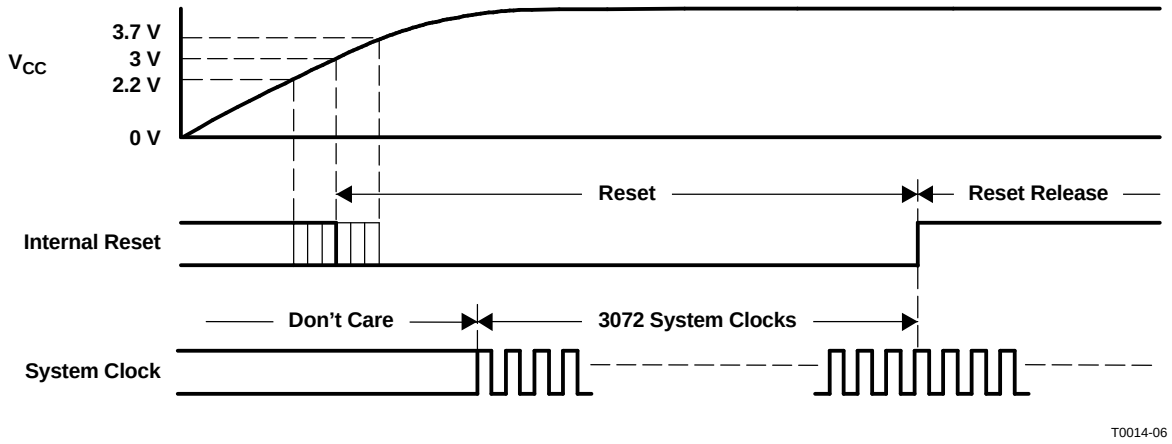


Figure 21. Power-On-Reset Timing

Audio Serial Interface

The audio serial interface for the PCM1780/81/82 consists of a three-wire synchronous serial port. It includes LRCK (pin 8), BCK (pin 7), and DATA (pin 6). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1780/81/82 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface.

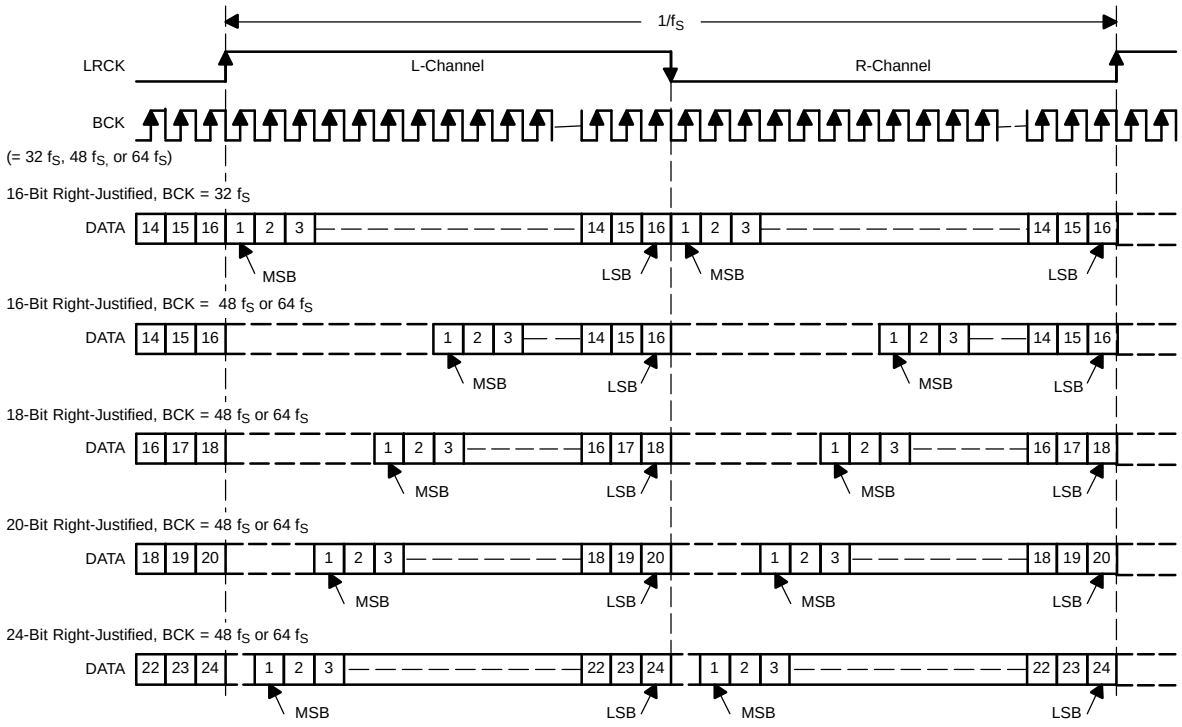
Both LRCK and BCK should be synchronous with the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, or 64 times the sampling frequency.

Internal operation of the PCM1780/81/82 is synchronized with LRCK. Accordingly, internal operation of the device is suspended when the sampling rate clock, LRCK, is changed or SCK and/or BCK is interrupted at least for three bit-clock cycles. If SCK, BCK, and LRCK are provided continuously after this suspended condition, the internal operation is resynchronized automatically within a period of less than $3/f_S$. External resetting is not required.

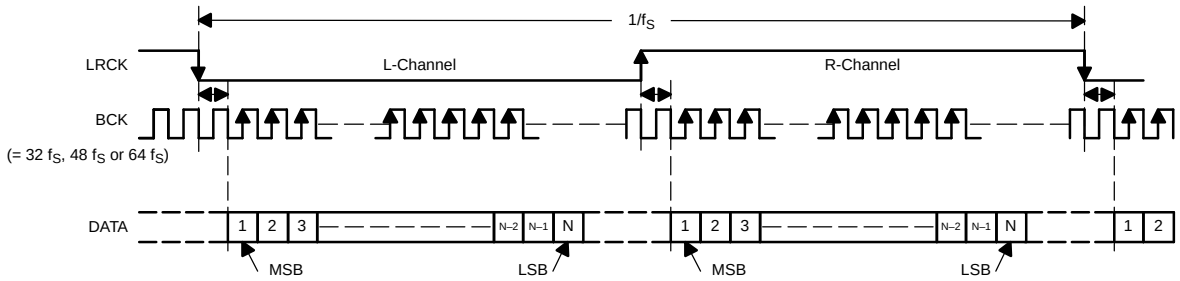
Audio Data Formats and Timing

The PCM1780/82 supports industry-standard audio data formats, including right-justified, I^2S, and left-justified. The PCM1781 supports I^2S and 16-bit-word, right-justified. The data formats are shown in Figure 22. Data formats are selected for the PCM1780/82 using the format bits, FMT[2:0], located in control register 20, and are selected for the PCM1781 using the FMT pin. The default data format is 24-bit, left-justified. All formats require binary 2s complement, MSB-first audio data. Figure 23 shows a detailed timing diagram for the serial audio interface.

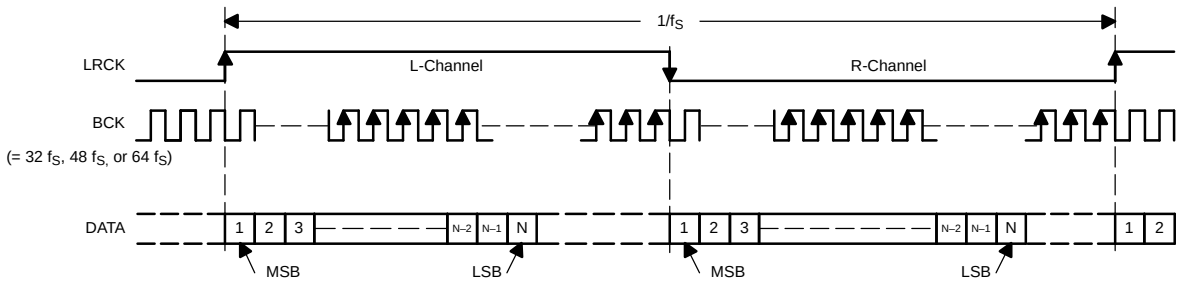
(1) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH

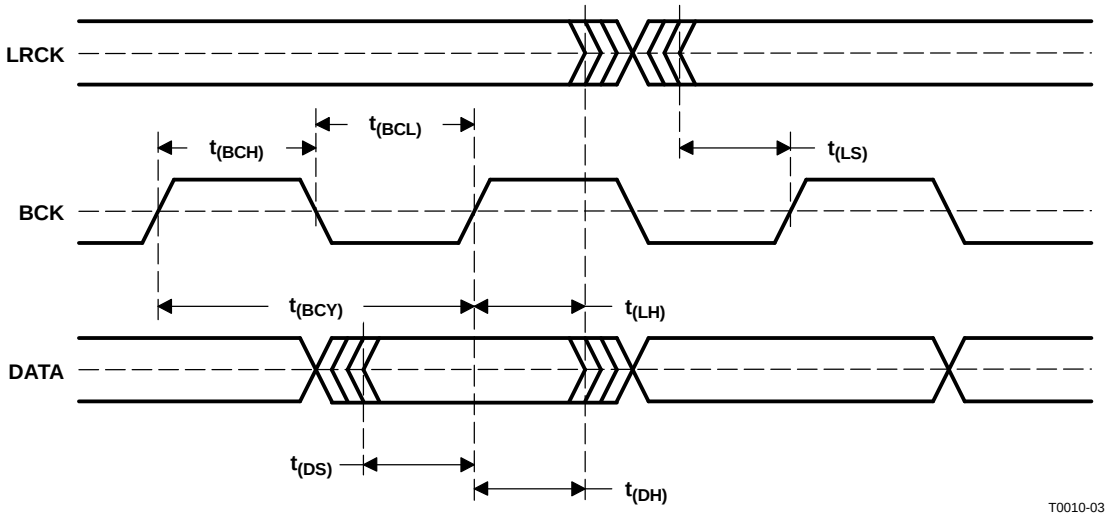


(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



T0009-02

Figure 22. Audio Data Input Formats



PARAMETER		MIN	UNIT
$t_{(BCY)}$	BCK pulse cycle time	1/(32 f_S), 1/(48 f_S), 1/(64 f_S)(1)	
$t_{(BCH)}$	BCK pulse duration, HIGH	35	ns
$t_{(BCL)}$	BCK pulse duration, LOW	35	ns
$t_{(LS)}$	LRCK setup time to BCK rising edge	10	ns
$t_{(LH)}$	LRCK hold time to BCK rising edge	10	ns
$t_{(DS)}$	DATA setup time	10	ns
$t_{(DH)}$	DATA hold time	10	ns

(1) f_S is the sampling frequency (e.g., 44.1 kHz, 48 kHz, 96 kHz, etc.).

Figure 23. Audio Interface Timing

OVERSAMPLING RATE CONTROL

The PCM1780/81/82 automatically controls the oversampling rate of the delta-sigma D/A converters with the system clock frequency. The oversampling rate is set to 64× oversampling with an 1152-f_S, 768-f_S, or 512-f_S system clock, to 32× oversampling with a 384-f_S or 256-f_S system clock, or to 16× oversampling with a 192-f_S or 128-f_S system clock.

ZERO FLAGS (PCM1780/82)

Zero-Detect Condition

Zero detection for each output channel is independent from the other. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero-detect condition exists for that channel.

Zero-Flag Outputs

Each channel has a corresponding zero-flag pin, ZEROL (pin 1) or ZEROR (pin 16). Given that a zero-detect condition exists for one or more channels, the zero-flag pins for those channels are set to a logic-1 state. The zero-flag pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled function.

The active polarity of the zero-flag outputs can be inverted by setting the ZREV bit of control register 22 to 1. The reset default is active-high output, or ZREV = 0.

The L-channel and R-channel common zero flag can be selected by setting the AZRO bit of control register 22 to 1. The reset default is for independent L-channel and R-channel zero flags, or AZRO = 0.

On the PCM1782, ZEROL and ZEROR are open-drain outputs.

ZERO FLAG (PCM1781)

The PCM1781 has a zero-flag pin, ZEROA (pin 16). ZEROA is the L-channel and R-channel common zero-flag pin. If the data for L-channel and R-channel remains at a 0 level for 1024 sampling periods (or LRCK clock periods), ZEROA is set to a logic-1 state.

HARDWARE CONTROL (PCM1781)

The digital functions of the PCM1781 are capable of hardware control. Table 2 shows selectable formats, Table 3 shows de-emphasis control, and Table 4 shows muting control.

Table 2. Data Format Selection

FMT (PIN 1)	DATA FORMAT
LOW	16- to 24-bit, I^2S format
HIGH	16-bit right-justified

Table 3. De-Emphasis Control

DEMP1 (PIN 3)	DEMP0 (PIN 2)	DE-EMPHASIS FUNCTION
LOW	LOW	OFF
LOW	HIGH	48-kHz de-emphasis ON
HIGH	LOW	44.1-kHz de-emphasis ON
HIGH	HIGH	32-kHz de-emphasis ON

Table 4. Mute Control

MUTE (PIN 4)	MUTE STATUS
LOW	Mute OFF
HIGH	Mute ON

SOFTWARE CONTROL (PCM1780/82)

The PCM1780/82 has many programmable functions that can be controlled in the software control mode; the functions are controlled by programming the internal registers using $\overline{MS}$, MC, and MD.

The serial control interface is a 3-wire serial port which operates asynchronously to the audio serial interface. The serial control interface is used to program the on-chip mode registers. The control interface includes MD (pin 4), MC (pin 3), and $\overline{MS}$ (pin 2). MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. $\overline{MS}$ is the select input, used to enable the mode control port.

Register Write Operation

All write operations for the serial control port use 16-bit data words. Figure 24 shows the control data word format. The most significant bit must be a 0. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 25 shows the functional timing diagram for writing to the serial control port. $\overline{MS}$ is held at a logic-1 state until a register needs to be written. To start the register write cycle, $\overline{MS}$ is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, $\overline{MS}$ is set to logic 1 to latch the data into the indexed mode control register.

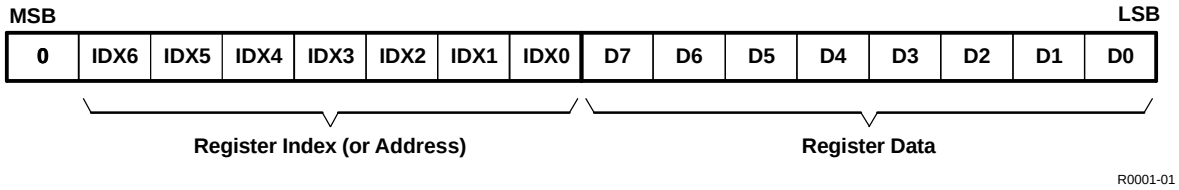


Figure 24. Control Data Word Format for MD

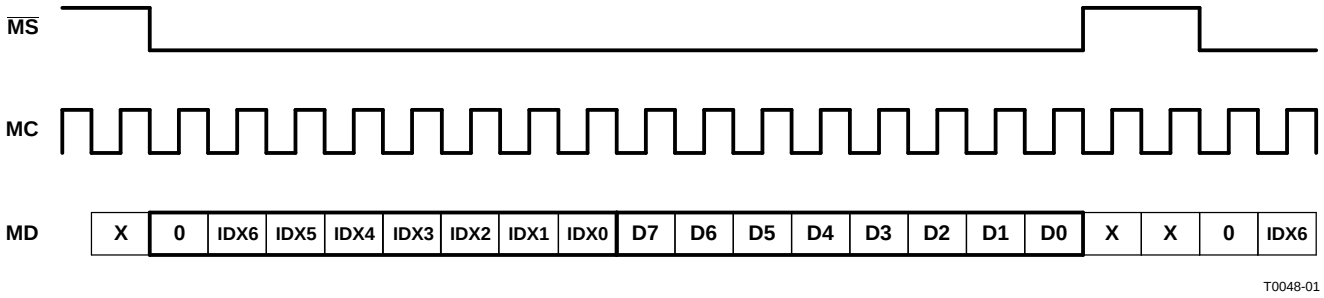
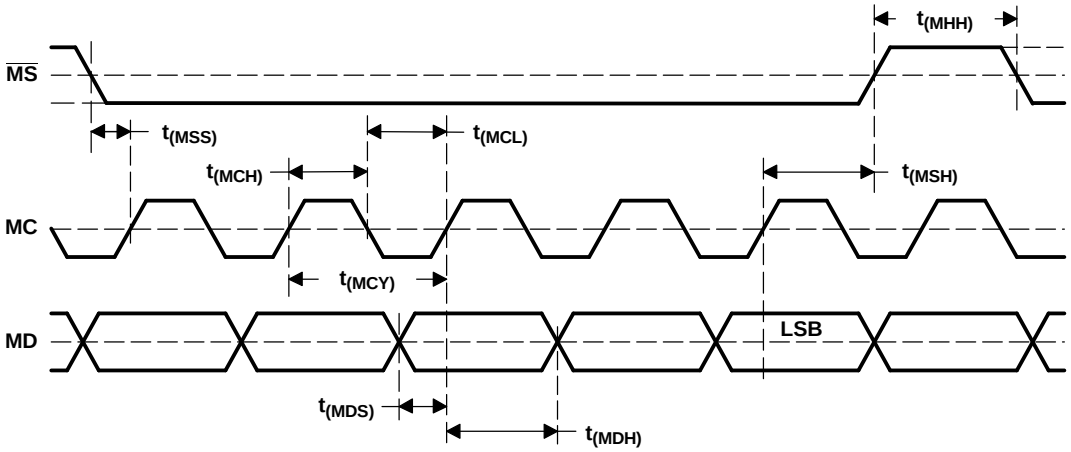


Figure 25. Register Write Operation

Control Interface Timing Requirements

Figure 26 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



PARAMETER		MIN	UNIT
$t_{(MCY)}$	MC pulse cycle time	100	ns
$t_{(MCL)}$	MC low-level time	50	ns
$t_{(MCH)}$	MC high-level time	50	ns
$t_{(MHH)}$	$\overline{MS}$ high-level time	$3/(256 \times f_S)$(2)	ns
$t_{(MSS)}$	$\overline{MS}$ falling edge to MC rising edge	20	ns
$t_{(MSH)}$	$\overline{MS}$ hold time(1)	20	ns
$t_{(MDH)}$	MD hold time	15	ns
$t_{(MDS)}$	MD setup time	20	ns

(1) MC rising edge for LSB to $\overline{MS}$ rising edge

(2) f_S: sampling rate

Figure 26. Control Interface Timing

MODE CONTROL REGISTERS (PCM1780/82)

User-Programmable Mode Controls

The PCM1780/82 includes a number of user-programmable functions, which are accessed via control registers. The registers are programmed using the serial control interface, which was previously discussed in the *Software Control* section of this data sheet. Table 5 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 5. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(S)
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	16 and 17	AT1[7:0], AT2[7:0]
Soft mute control	Mute disabled	18	MUT[2:0]
Oversampling rate control	×64, ×32, ×16	18	OVER
Soft reset control	Reset disabled	18	SRST
DAC operation control	DAC1 and DAC2 enabled	19	DAC[2:1]
De-emphasis function control	De-emphasis disabled	19	DM12
De-emphasis sample rate selection	44.1 kHz	19	DMF[1:0]
Audio data format control	24-bit, left-justified	20	FMT[2:0]
Digital filter rolloff control	Sharp rolloff	20	FLT
Digital attenuation mode select	0 to –63 dB, 0.5 dB/step	21	DAMS
Output phase select	Normal Phase	22	DREV
Zero-flag polarity select	High	22	ZREV
Zero-flag function select	L-, R-channels independent	22	AZRO

Table 6. Mode Control Register Map

IDX (B8–B14)	REGIS-TER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
10h	16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
11h	17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
12h	18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1
13h	19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1
14h	20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0
15h	21	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DAMS
16h	22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	0	AZRO	ZREV	DREV

Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

ATx[7:0]: Digital Attenuation Level Setting

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2)

Default value: 1111 1111b

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING	
		DAMS = 0	DAMS = 1
1111 1111b	255	0 dB, no attenuation (default)	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB	–1 dB
1111 1101b	253	–1 dB	–2 dB
:	:	:	:
1001 1100b	156	–49.5 dB	–99 dB
1001 1011b	155	–50 dB	–100 dB
1001 1010b	154	–50.5 dB	Mute
:	:		:
1000 0010b	130	–62.5 dB	Mute
1000 0001b	129	–63 dB	Mute
1000 0000b	128	Mute	Mute
:	:	:	:
0000 0000b	0	Mute	Mute

Each DAC channel ($V_{OUT}L$ or $V_{OUT}R$) includes a digital attenuation function. The attenuation level can be set from 0 dB to R dB, in S-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (S dB) every $8/f_S$ time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

R (range) and S (step) are –63 and 0.5 for DAMS = 0 and –100 and 1 for DAMS = 1, respectively. The DAMS bit is defined in register 21.

The attenuation data for each channel can be set individually. The attenuation level can be calculated using the following formula:

$$\text{Attenuation level (dB)} = S \bullet (ATx[7:0]_{DEC} - 255)$$

where $ATx[7:0]_{DEC}$ = 0 through 255. For $ATx[7:0]_{DEC}$ = 0 through 128 with DAMS = 0, or for $ATx[7:0]_{DEC}$ = 0 through 154 with DAMS = 1, the attenuation level is set to infinite attenuation (mute).

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1

NOTE: RSV indicates a reserved bit that should be set to 0.

MUTx: Soft Mute Control

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (S dB) for every 8/fS seconds. This provides pop-free muting of the DAC output. The step size, S, is 0.5 dB for DAMS = 0 and 1 dB for DAMS = 1.

By setting MUTx = 0, the attenuator is increased one step for every $8/f_S$ seconds to the previously programmed attenuation level.

OVER: Oversampling Rate Control

Default value: 0

System clock frequency = 512 f_S, 768 f_S, or 1152 f_S

OVER = 0	×64 oversampling (default)
OVER = 1	×128 oversampling (applicable only if sampling clock frequency ≤ 24 kHz)

System clock frequency = 256 f_S or 384 f_S

OVER = 0	×32 oversampling (default)
OVER = 1	×64 oversampling (applicable only if sampling clock frequency ≤ 48 kHz)

System clock frequency = 128 f_S, 192 f_S

OVER = 0	×16 oversampling (default)
OVER = 1	×32 oversampling (applicable only if sampling clock frequency ≤ 96 kHz)

The OVER bit is used to control the oversampling rate of the delta-sigma D/A converters.

Setting OVER = 1 is recommended under the following conditions:

- System clock frequency = 512 f_S, 768 f_S, or 1152 f_S, and sampling clock frequency = 24 kHz
- System clock frequency = 256 f_S or 384 f_S and sampling clock frequency = 48 kHz
- System clock frequency = 128 f_S or 192 f_S and sampling clock frequency = 96 kHz

SRST: Reset

Default value: 0

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

The SRST bit is used to enable or disable the soft reset function. The operation is the same as for the power-on-reset function with the exception of the reset period, which is 1024 system clocks for the SRST function. All registers are initialized.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1

NOTE: RSV indicates a reserved bit that should be set to 0.

DACx: DAC Operation Control

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2).

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output generates the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output is set to the dc common voltage (V_{COM}), equal to $V_{CC}/2$.

DM12: Digital De-Emphasis Function Control

Default value: 0

DM12 = 0	De-emphasis disabled (default)
DM12 = 1	De-emphasis enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. Refer to the plots shown in the *Typical Performance Curves* section of this data sheet.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

Default value: 00

DMF[1:0]	De-Emphasis Sample Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

NOTE: RSV indicates a reserved bit that should be set to 0.

FMT[2:0]: Audio Interface Data Format

Default value: 101

FMT[2:0]	Audio Data Format Selection
000	24-bit right-justified format, standard data
001	20-bit right-justified format, standard data
010	18-bit right-justified format, standard data
011	16-bit right-justified format, standard data
100	I^2S format, 16 to 24 bits
101	Left-justified format, 16 to 24 bits (default)
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface. The preceding table shows the available format options.

FLT: Digital Filter Rolloff Control

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows users to select the digital filter rolloff that is best suited to their application. Two filter rolloff selections are available: sharp and slow. The filter responses for these selections are shown in the *Typical Performance Curves* section of this data sheet

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 21	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DAMS

NOTE: RSV indicates a reserved bit that should be set to 0.

DAMS: Digital Attenuation Mode Select

Default value: 0

DAMS = 0	Fine step, 0.5 dB/step for 0 to –63 dB range (default)
DAMS = 1	Wide range, 1 dB/step for 0 to –100 dB range

The DAMS bit is used to select the digital attenuation mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	0	AZRO	ZREV	DREV

NOTE: RSV indicates a reserved bit that should be set to 0.

DREV: Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit allows the user to control the phase of the analog output signal.

ZREV: Zero-Flag Polarity Select

Default value: 0

ZREV = 0	Zero-flag pins HIGH at a zero detect (default)
ZREV = 1	Zero-flag pins LOW at a zero detect

The ZREV bit allows the user to select the polarity of the zero-flag pins.

AZRO: Zero Flag Function Select

Default value: 0

AZRO = 0	Pin 1: ZEROL; zero-flag output for L-channel
	Pin 16: ZEROR; zero-flag output for R-channel
AZRO = 1	Pin 1: NA; not assigned
	Pin 16: ZEROA; zero-flag output for L-/R-channel

The AZRO bit allows the user to select the function of zero-flag pins.

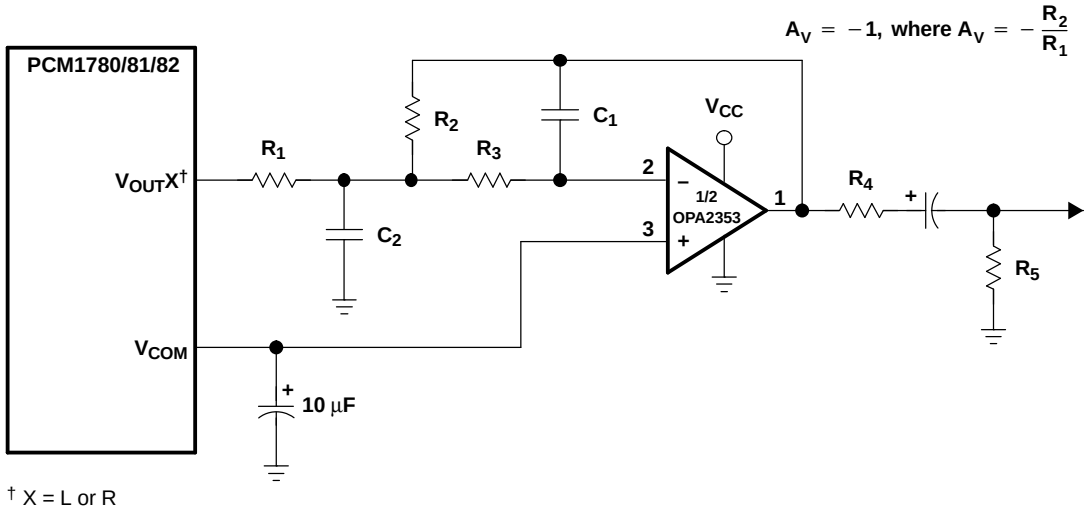
ANALOG OUTPUTS

The PCM1780/81/82 includes two independent output channels, $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 3.9 Vp-p typical into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common voltage, equal to 0.5 V_{CC}.

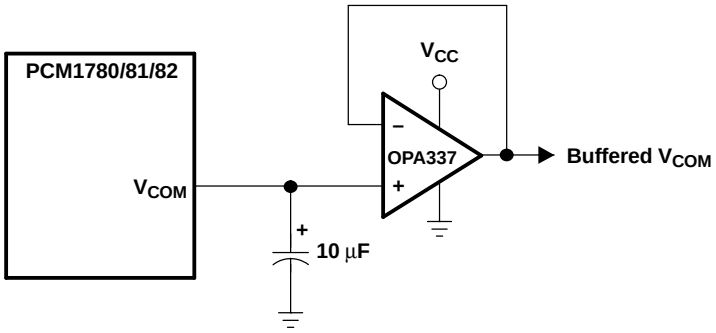
The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise-shaping characteristics of the PCM1780/81/82 delta-sigma D/A converters. The frequency response of this filter is shown as ANALOG FILTER in the *Typical Performance Curves* section. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application Information* section of this data sheet.

V_{COM} Output

One unbuffered common voltage output pin, V_{COM} (pin 13), is brought out for decoupling purposes. This pin is nominally biased to the dc common voltage, equal to $V_{CC}/2$. This pin can be used to bias external circuits. Figure 27 shows an example of using the V_{COM} pin for external biasing applications.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} When Biasing Multiple Nodes

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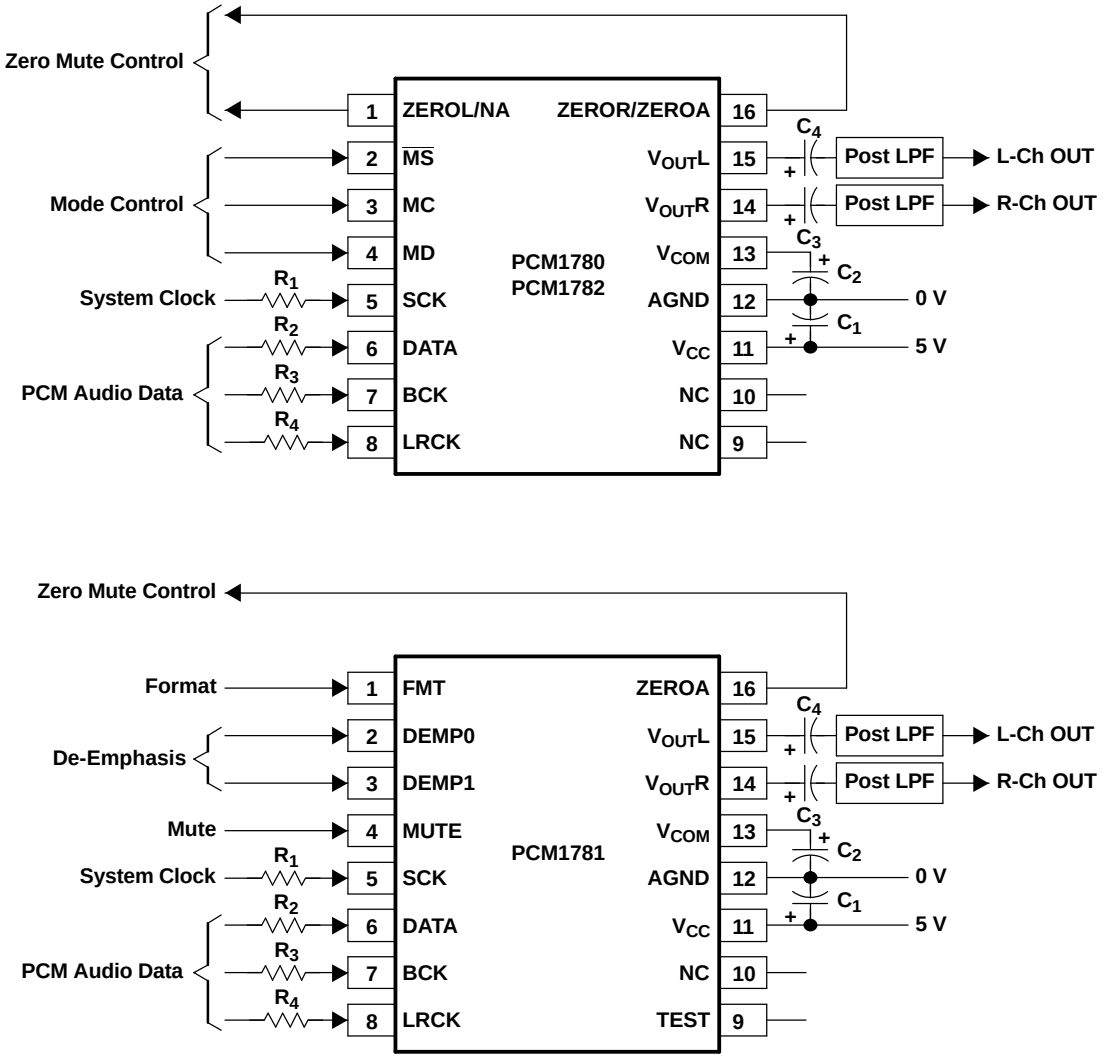
Figure 27. Biasing External Circuits Using the V_{COM} Pin

APPLICATION INFORMATION

Connection Diagrams

A basic connection diagram is shown in Figure 28, with the necessary power supply bypassing and decoupling components. TI recommends using the component values shown in Figure 28 for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter which reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.



C_1: 0.1 μF Ceramic and 10 μF Electrolytic
C_2: 10 μF Electrolytic
C_3, C_4: 4.7 μF – 10 μF Electrolytic
R_1 – R_4: 22 Ω – 100 Ω

S0055-01

Figure 28. Basic Connection Diagram

APPLICATION INFORMATION (continued)

Power Supplies and Grounding

The PCM1780/81/82 requires a 5-V supply for V_{CC}.

Proper power supply bypassing is shown in Figure 28. The 0.1-µF ceramic capacitor and the 10-µF electrolytic capacitor are recommended.

D/A Output Filter Circuits

Delta-sigma D/A converters use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 27(a) and Figure 29 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are second-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see *Dynamic Performance Testing of Digital Audio D/A Converters* (SBAA055), available from the TI Web site at http://www.ti.com.

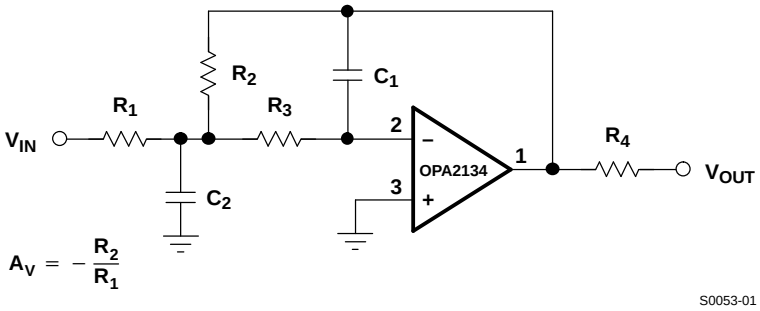


Figure 29. Dual-Supply Filter Circuit

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1780/81/82 is shown in Figure 30. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1780/81/82 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1780/81/82. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 31 shows the recommended approach for single-supply applications.

APPLICATION INFORMATION (continued)

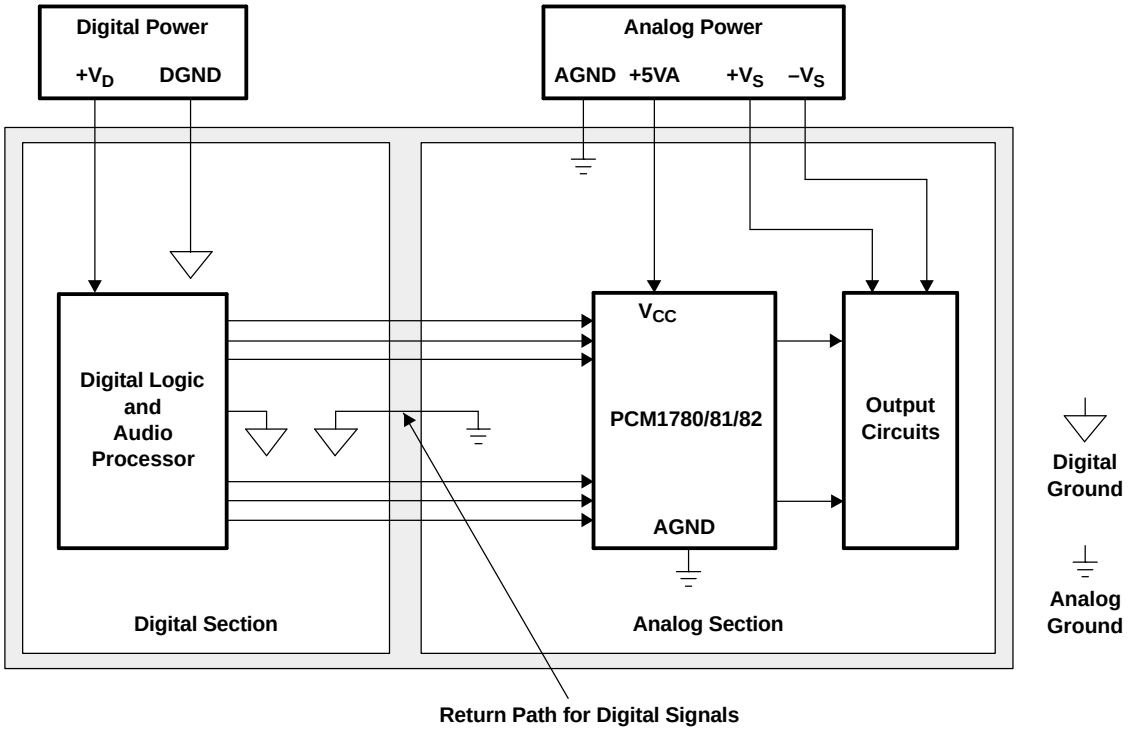


Figure 30. Recommended PCB Layout

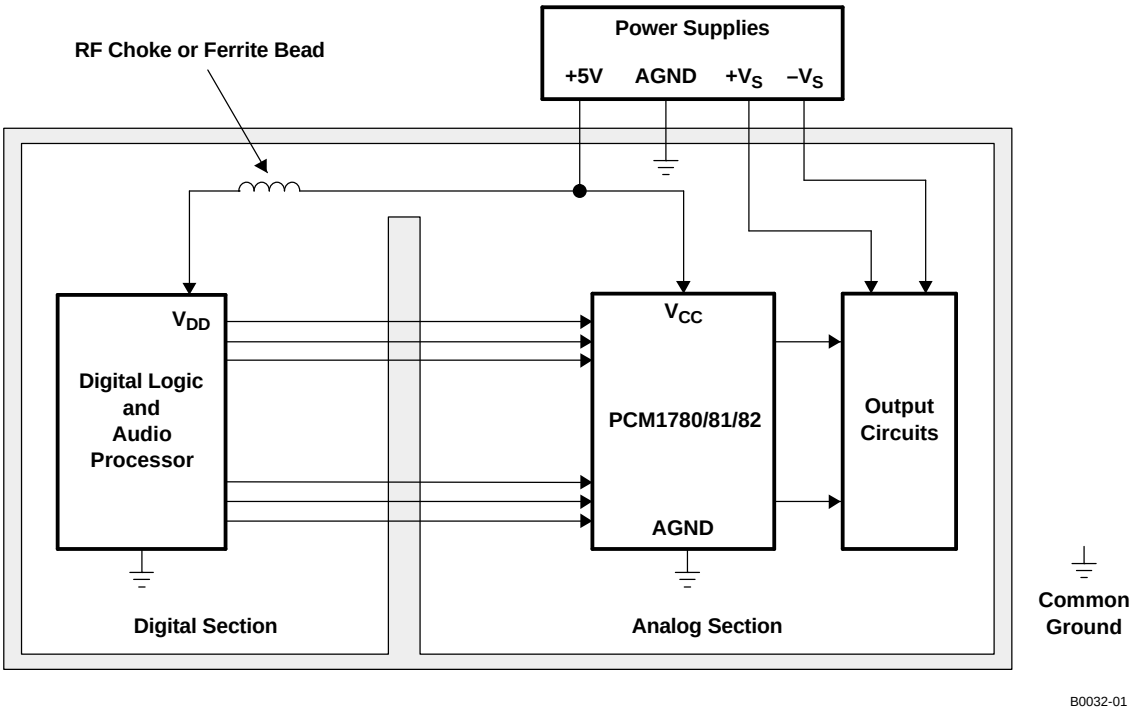


Figure 31. Single-Supply PCB Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM1780DBQ	ACTIVE	SSOP/ QSOP	DBQ	16	98	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1780DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1781DBQ	ACTIVE	SSOP/ QSOP	DBQ	16	98	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM1781DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM1782DBQ	ACTIVE	SSOP/ QSOP	DBQ	16	98	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1782DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

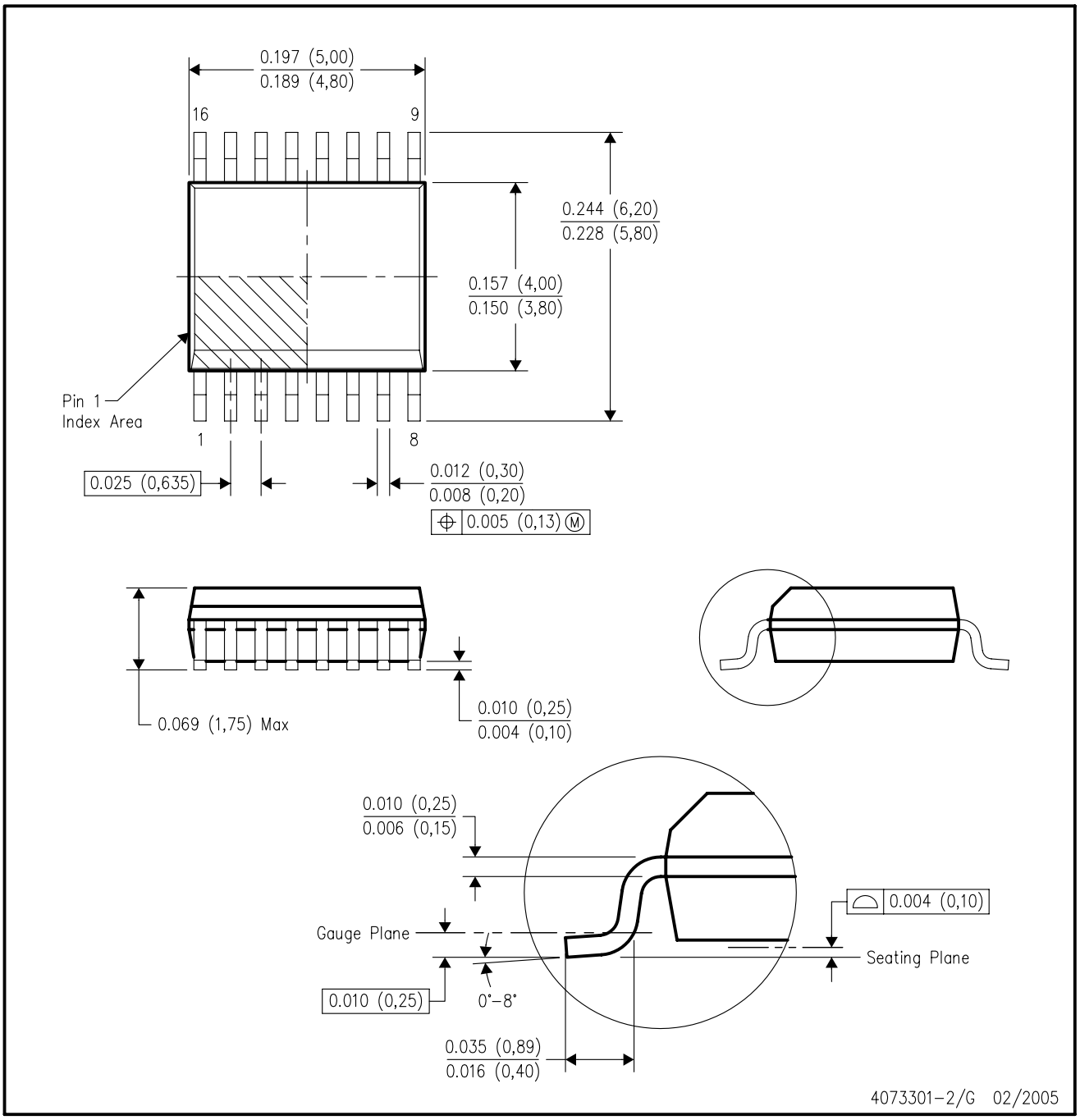
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

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