Preliminary TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

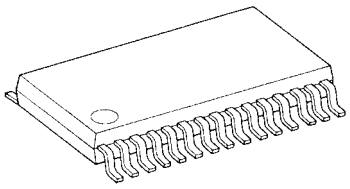
TA1296FN

Down-Converter IC with PLL for Satellite Tuner

The TA1296FN is a wideband down-converter which can operate at input frequency ranging from 850 MHz to 2200 MHz. Intended primarily for use in satellite tuners, this IC includes an oscillator, a mixer, an IF amplifier and a PLL.

The I^2C bus data format is used as the data control format.

The supply voltage of 5.0 V helps minimize the tuner's power dissipation, while the compact 30-pin SSOP package allows the tuner to be kept small.



SSOP30-P-300-0.65

Weight: 0.17 g (typ.)

Features

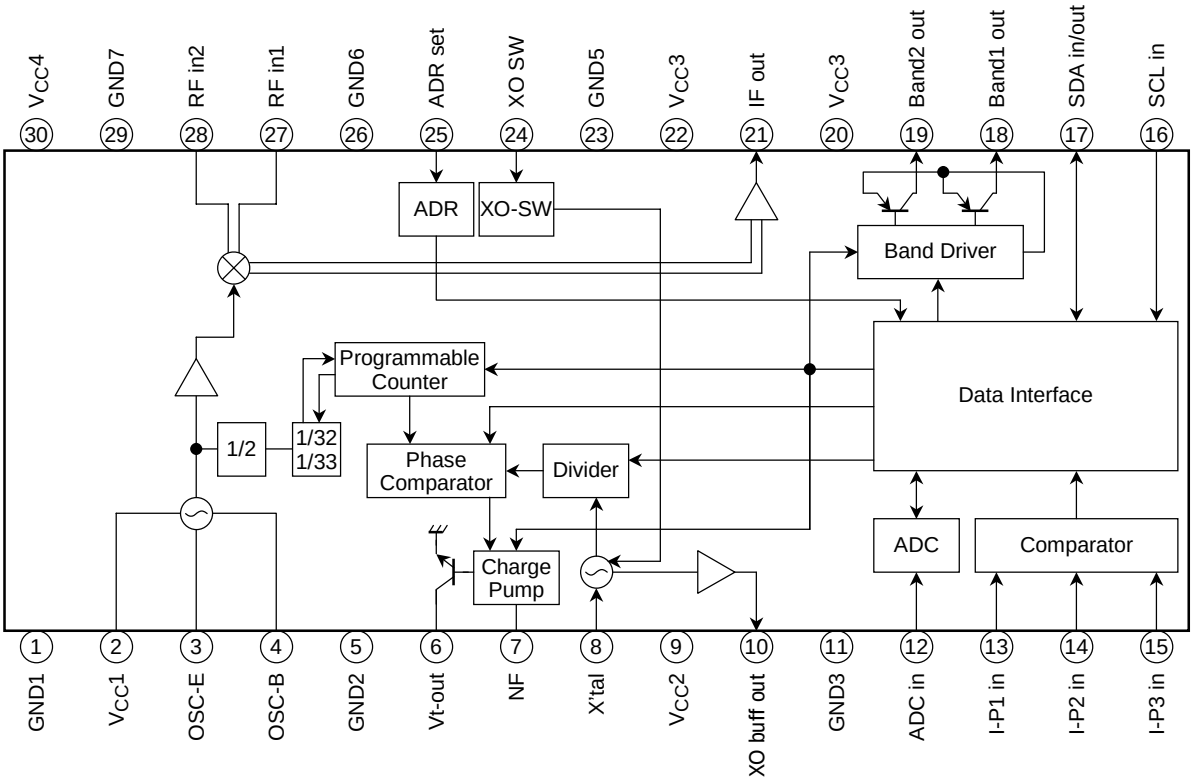
- Supply voltage: 5.0 V (typ.)
- Wide input frequency range
- Low phase noise oscillator
- Standard I^2C bus format control
- 4-MHz (X'tal) buffer output pin
- Reference oscillator input change-over switch [X'tal or external input]
- 33-V high-voltage tuning amplifier built-in
- 3-bit input port (for read mode)
- 2-bit band switch drive transistor (for write mode)
- 5-level AD converter
- Frequency step: 62.5 kHz or 125 kHz (for 4-MHz X'tal)
- 4-address setting via address selector
- Power-on reset circuit
- ×1/2 prescaler
- Flat compact package: SSOP30-P-300-0.65 (0.65-mm pitch)

Power-On Reset Operation Conditions

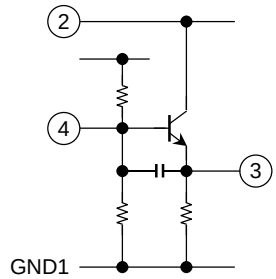
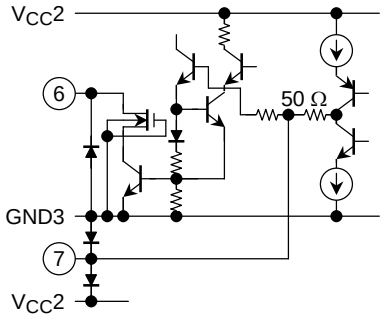
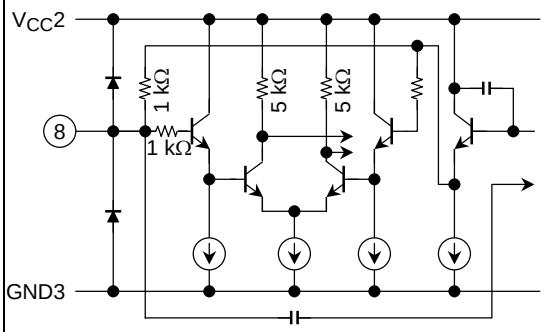
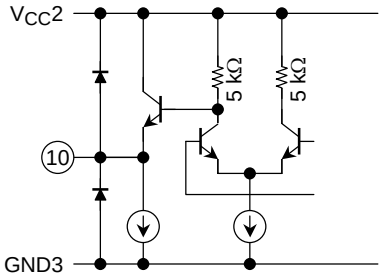
- Frequency step: 125 kHz
- Charge pump output current: ±50 μA
- Counter data: all [0]
- Band driver: OFF
- Tuning amplifier: OFF

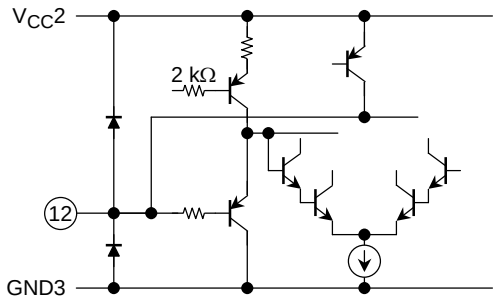
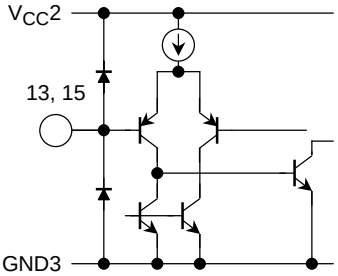
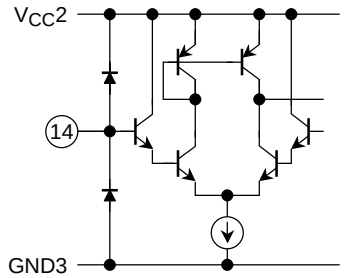
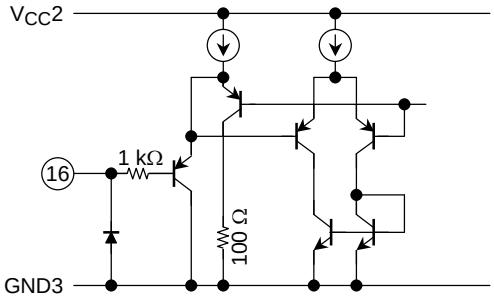
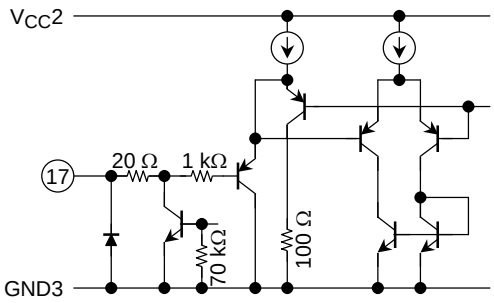
Note 1: This device can easily be damaged by high voltages or electrical fields. For this reason, please handle it with care.

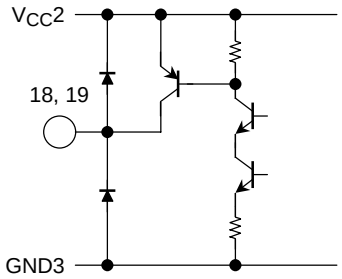
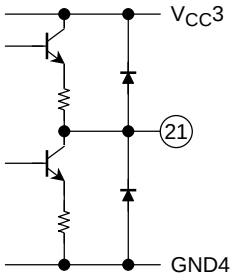
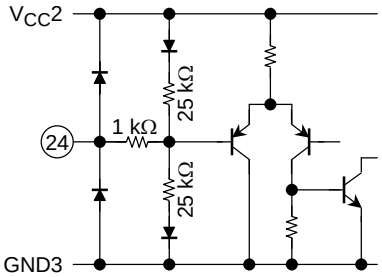
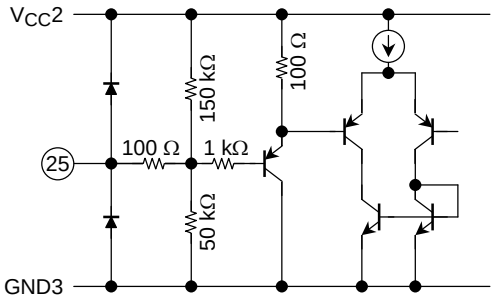
Block Diagram

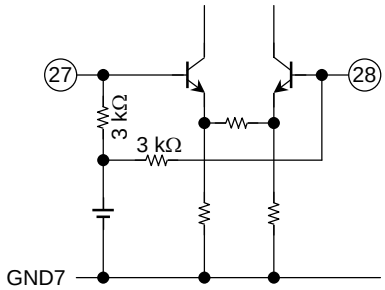


Pin Functions

Pin No.	Pin Name	Function	Interface
1	GND1	Ground pin for oscillator circuit block	—
2	$V_{CC}1$	Power supply pin for local oscillator circuit block	
3 4	Oscillator	Local oscillator circuit	
5	GND2	Ground pin for oscillator circuit block	—
6	Vt Output	Tuning voltage output pin with built-in tuning amplifier	
7	NF		
8	Reference Input (4-MHz input)	Crystal oscillator input Can be switched between X'tal oscillator and external input using pin 24 (XO switch).	
9	$V_{CC}2$	Power supply pin for PLL circuit block	—
10	Reference signal buffer output	Buffer output pin for reference signal	
11	GND3	Ground pin for PLL circuit block	—

Pin No.	Pin Name	Function	Interface
12	ADC	AD converter pin Converts input voltage into digital data.	
13	I-P1	Comparator status can be checked in Read Mode.	
15	I-P3		
14	I-P2		
16	SCL Input	Input pin for I^2C bus serial clock data	
17	SDA Input/Output	Input/output pin for I^2C bus serial clock data	

Pin No.	Pin Name	Function	Interface
18	Band 1 Output	Output can be controlled by setting band switch data.	
19	Band 2 Output		
20	GND4	Ground pin for IF amplifier circuit block	—
21	IF Output	IF output pin	
22	$V_{CC}3$	Power supply pin for IF amplifier circuit block	—
23	GND5	Ground pin for IF amplifier circuit block	—
24	XO Switch	Determines reference signal input. If connected to ground: X'tal oscillator. If open or connected to $V_{CC}2$: external input	
25	ADR Set	The address for hardware bit setting can be selected by applying voltage to this pin. 4 programmable address can be programmed.	
26	GND6	Ground pin for mixer circuit block	—

Pin No.	Pin Name	Function	Interface
27	RF Input1	RF signal input pin Input can be either balanced or unbalanced.	
28	RF Input2		
29	GND7	Ground pin for mixer circuit block	—
30	$V_{CC}4$	Power supply pin for mixer circuit block	—

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Pin No.	Symbol	Rating	Unit
Supply voltage	2	$V_{CC}1$	6	V
	9	$V_{CC}2$	6	
	22	$V_{CC}3$	6	
	30	$V_{CC}4$	6	
Tuning amplifier voltage	6	VBT	38	V
Power dissipation	—	P_D	1130 (Note 2)	mW
Operating temperature	—	T_{opr}	−20 to 85	°C
Storage temperature	—	T_{stg}	−55 to 150	°C

Note 2: 50 mm × 50 mm × 1.6 mm, 40% Cu board
If Ta > 25°C, derate this value by 9.1 mW/°C.

Recommended Operating Conditions

Pin No.	Symbol		Min	Typ.	Max	Unit
2	Local oscillator block	$V_{CC}1$	4.5	5.0	5.5	V
9	PLL block	$V_{CC}2$	4.5	5.0	5.5	V
22	IF amplifier block	$V_{CC}3$	4.5	5.0	5.5	V
30	Mixer block	$V_{CC}4$	4.5	5.0	5.5	V

Electrical Characteristics

DC Characteristics (unless otherwise specified, $V_{CC}1 = V_{CC}2 = V_{CC}3 = V_{CC}4 = 5$ V, Ta = 25°C)

When power on, counter data = all [0], VBT = OFF, CP1 = CP0 = 0 and band = all [0]

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Power supply current	$I_{CC}1$	1	—	5.0	7.5	10.0	mA
	$I_{CC}2$		—	16.0	20.0	25.5	
	$I_{CC}3$		—	16.5	20.0	24.5	
	$I_{CC}4$		—	9.5	12.5	16.0	
Total	I_{CC}-total	—	—	47.0	60.0	76.0	mA

Down-Converter Block

AC Characteristics (unless otherwise specified, $V_{CC}1 = V_{CC}2 = V_{CC}3 = V_{CC}4 = 5$ V, Ta = 25°C)

Parameter	Symbol	Test Circuit	Test Condition (Note 4)	Min	Typ.	Max	Unit
RF input frequency	Mfin	—	—	850	—	2200	MHz
RF input level	MPin	—	—	—	—	−35	dBmW
IF output frequency	Afin	—	—	350	—	550	MHz
IF output impedance (Note 3)	AZout	—	Single-end	—	75	—	Ω
Local oscillator frequency	LO	—	—	1300	—	2700	MHz
Conversion gain (Note 3)	CG	2	fRF = 898 MHz	27.5	31	34	dB
			fRF = 1598 MHz	27.5	31	34.5	
			fRF = 2198 MHz	25	29	32.5	
Noise figure (Note 3)	NF	3	fRF = 898 MHz	—	9	10.5	dB
			fRF = 1598 MHz	—	9	11	
			fRF = 2198 MHz	—	11	13	
IF output power level (Note 3)	Apsat	2	fRF = 898 MHz	6.5	8.5	—	dBmW
			fRF = 1598 MHz	6.5	8.5	—	
			fRF = 2198 MHz	6.5	8.5	—	
3^{rd} inter modulation (IF output intercept point) (Note 3)	IP3	4	fd = 898 MHz, fud = 903 MHz	15	18.5	—	dBmW
			fd = 1598 MHz, fud = 1603 MHz	15	17	—	
			fd = 2198 MHz, fud = 2203 MHz	15	17	—	
Conversion gain shift (Note 3)	CGs	2	fRF = 898 MHz	—	—	±2	dB
			fRF = 1598 MHz	—	—	±2	
			fRF = 2198 MHz	—	—	±2	
Frequency shift (PLL OFF)	ΔfB	2	fosc = 1300 MHz	—	—	±4.5	MHz
			fosc = 2000 MHz	—	—	±3.5	
			fosc = 2600 MHz	—	—	±3.5	
Phase noise (with 10-kHz offset)	PN	2	fosc = 1300 MHz	—	−74	−70	dBc/Hz
			fosc = 2000 MHz	—	−75	−71	
			fosc = 2600 MHz	—	−74	−70	
RF pin LO leak level	LORF	2	fosc = 1300 MHz		−40	−37	dBmW
			fosc = 2000 MHz		−32	−29	
			fosc = 2600 MHz		−32	−29	
IF pin LO leak level	LOIF	2	fosc = 1300 MHz		−28	−20	dBmW
			fosc = 2000 MHz		−32	−24	
			fosc = 2600 MHz		−32.5	−27	

Note 3: IF output frequency = 402 MHz

Note 4: IF output load = 75 Ω

PLL Block (unless otherwise specified, $V_{CC}1 = V_{CC}2 = V_{CC}3 = V_{CC}4 = 5$ V, Ta = 25°C)

Parameter	Symbol	Test Circuit	Test Condition (Note 4)	Min	Typ.	Max	Unit
Tuning amplifier output voltage (close)	Vt out	1	VBT = 33 V, RL = 33 kΩ	0.3	—	33	V
Tuning amplifier maximum current	Ivt	1	VBT = 33 V	—	—	3	mA
X'tal negative resistance	XtR	1	XO-SW:GND (X'tal oscillator mode)	1	2.5	—	kΩ
X'tal operating range	OSCin	1	[NDK (AT-51), 4 MHz used]	3.2	—	4.5	MHz
X'tal external input level	Xo extl	1	XO-SW: $V_{CC}2$ or open	100	—	1000	mV_{p-p}
X'tal external input frequency	X-ext	1		2	—	6	MHz
Ratio setting range	N	—	16-bit counter	1024	—	65,535	
Logic input low voltage	V_{IL}	1	SDA and SCL pins	−0.3	—	1.5	V
Logic input high voltage	V_{IH}	1		2.4	—	$V_{CC}2$ + 0.3	V
Logic input current (low)	I BsL	1	SDA and SCL pins	−20	—	10	μA
Logic input current (high)	I BsH	1		−10	—	20	μA
ACK output voltage	VACK	1	ISINK = 3 mA	—	—	0.4	V
Charge pump output current	Ichg	1	CP1 = [0], CP0 = [0]	±35	±50	±75	μA
			CP1 = [0], CP0 = [1]	±75	±100	±145	
			CP1 = [1], CP0 = [0]	±180	±240	±345	
			CP1 = [1], CP0 = [1]	±375	±490	±700	
Band driver drive current	IBD	1	B1, B2	—	—	10	mA
Band driver voltage drop	VBDsat	1	B1, B2: IBD = 10-mA drive	—	—	0.2	V
Comparator pin input voltage	VCMP	1	IP-1, IP-2, IP-3	0	—	6	V
Comparator pin low voltage	VLCMP	1	IP-1, IP-2, IP-3	0	—	1.5	V
Comparator pin high voltage	VHCMP	1	IP-1, IP-2, IP-3	2.7	—	6	V
Xo buffer output level	Xo out	1	1-kΩ, 10-pF load X'tal: NDK (AT-51), 4 MHz used. 4-MHz level monitored on oscilloscope using FET probe (1 MΩ, 1.9 pF).	350	500	—	mV_{p-p}

Bus Line Characteristics

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
SCL clock frequency	fSCL	—	Please refer to data timing chart.	0	—	100	kHz
Bus free time between a STOP and START conditions	t_{BUF}			4.7	—	—	μs
Hold time for repeated START condition	t_{HD}; STA			4	—	—	μs
SCL clock low period	t_{LOW}			4.7	—	—	μs
SCL clock high period	t_{HIGH}			4	—	—	μs
Set-up time for repeated START condition	f_{SU}; STA			4.7	—	—	μs
Data hold time	t_{HD}; DAT			0	—	—	μs
Data set-up time	t_{SU}; DAT			250	—	—	ns
Rise time for SDA and SCL signals	tR			—	—	1000	ns
Fall time for SDA and SCL signals	tF			—	—	300	ns
Set-up time for STOP condition	tsU; STO			4	—	—	μs

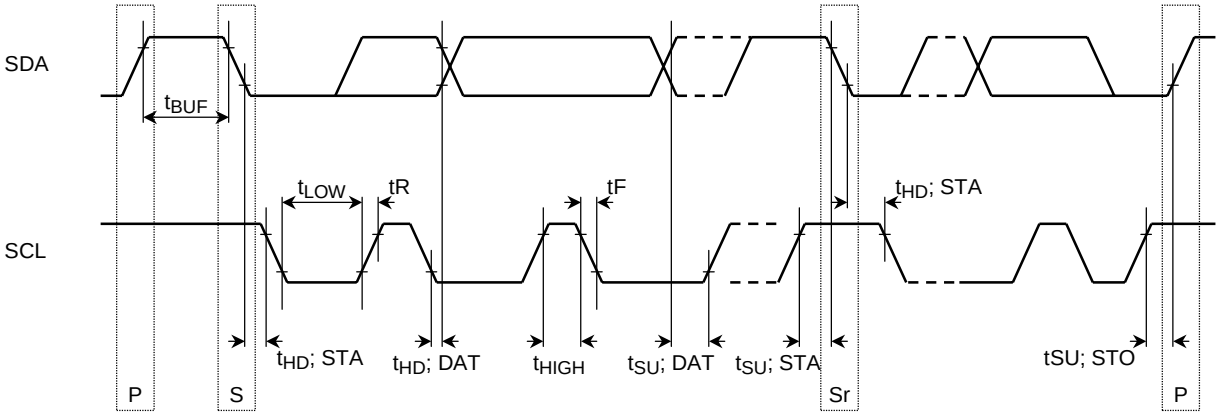


Figure 1 I^2C Bus Data Timing Chart (rising-edge timing)

Test Conditions

(1) Conversion gain
RF input level = −40dBmW

(2) Noise figure
NF meter direct-reading value (DSB measurement)

(3) IF output power level
Measure maximum IF output level.

(4) 3rd inter modulation
- fd (fd input level = −40dBmW)
- fud = fd + 5 MHz (fud input level = −40dBmW)

Calculate IF output intercept point as follows:
IP3 = S/(N − 1) + P [dBmW]
S: suppression level N: 3 P: IF output level

(5) Conversion gain shift
Conversion gain shift is defined as change in conversion gain when supply voltage exceeds ranges V_{CC} = 5 V to 4.5 V or V_{CC} = 5 V to 5.5 V.

(6) Frequency shift (PLL OFF)
Frequency shift is defined as change in oscillator frequency when supply voltage exceeds ranges $V_{CC}1$ = 5 V to 4.5 V or $V_{CC}1$ = 5 V to 5.5 V.

(7) Phase noise (offset = 10 kHz)
Measure phase noise at 10-kHz offset.

(8) RF pin local-leak level
Measure worst-case local-leak level for RF pin (with IF output pin open).

(9) IF pin local-leak level
Measure worst-case local-leak level for IF pin (with RF input pins shorted using 50-Ω resistor).

PLL Block

--I^{2}C Bus Communications Control--

The TA1296FN conforms to Standard Mode I^{2}C bus format.

I^{2}C Bus Mode allows two-way bus communication using Write Mode (for receiving data) and Read Mode (for processing status data).

Write Mode or Read Mode can be selected by setting the least significant bit (R/W bit) of the address byte.

If the least significant address bit is set to 0, Write Mode is selected; if it is set to 1, Read Mode is selected.

Address can be set using the hardware bits. 4 programmable address can be programmed.

Using this setting, multiple frequency synthesizers can be used on the same I^{2}C bus line.

The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR-pin 25). The address is selected according to the setting of these bits.

During acknowledgment of receipt of a valid address byte, the serial data (SDA) line is Low.

If Write Mode is currently selected, when the data byte is programmed, the serial data (SDA) line will be Low during the next acknowledgment.

A) Write mode (setting command)

When Write Mode is selected, byte 1 holds address data; byte 2 and byte 3 hold frequency data; byte 4 holds frequency data, the divider ratio setting and function setting data; and byte 5 holds output port data.

Data is latched and transferred at the end of byte 3, byte 4 and byte 5.

Byte 2 and byte 3 are latched and transferred as a byte pair.

Once a valid address has been received and acknowledged, the data type can be determined by reading the first bit of the next byte. That is, if the first bit is 0, the data is frequency data; if it is 1, the data is function-setting or band output data.

Additional data can be input without the need to transmit the address data again until the I^{2}C bus STOP condition is detected (e.g. a frequency sweep using additional frequency data is possible).

If a data transmission is aborted, data programmed before the abort remains valid.

[[BYTE 1]]

The address data for byte 1 can be set using the hardware bit.

The hardware bit can be set by applying a voltage to the address-setting pin (ADR: pin 25).

[[BYTE 2, BYTE 3, (N15) in BYTE 4]]

Byte 2 , byte 3 and N15 of byte 4 control the 16-bit programmable counter ratio and are stored in the 16-bit shift register together with frequency setting counter data.

The program frequency can be calculated using the following formula:

$$fosc = 2 \times fr \times N$$

fosc: Program frequency
fr: Phase comparator reference frequency
N: Counter total divider ratio

fr is calculated from the crystal oscillator frequency and the reference frequency divider ratio set in byte 4 (the control byte).

(fr = X'tal oscillator frequency/reference divider ratio)

The reference frequency divider ratio can be set to 1/64 or 1/128.

When a 4-MHz crystal oscillator is used, fr = 62.5 kHz or 31.25 kHz. The respective step frequencies are 125 kHz and 62.5 kHz.

[[BYTE 4]]

Byte 4 is a control byte used for selecting functions. Bit 4 (CP1) and bit 5 (CP0) determine the output current of the charge pump circuit.

If bit 4 and bit 5 are set to [CP1]:[CP0] = 00, the output current is set to ±50 μA.

If bit 4 and bit 5 are set to [CP1]:[CP0] = 01, the output current is set to ±100 μA.

If bit 4 and bit 5 are set to [CP1]:[CP0] = 10, the output current is set to ±240 μA.

If bit 4 and bit 5 are set to [CP1]:[CP0] = 11, the output current is set to ±490 μA.

Bit 7 (Rs) can be used to set the X'tal reference frequency divider ratio. If bit 7 is set to 0, the X'tal divider ratio is 1/128 (with a frequency step of 62.5 kHz). If it is set to 1, the X'tal divider ratio is 1/64 (with a frequency step of 125 kHz).

Bit 8 (OS) can be used to set the charge pump driver amplifier output setting. If bit 8 is set to 0, the output is ON (the normal setting). If it is set to 1, the output is OFF.

[[BYTE 5]]

Byte 5 can be used to select Test Mode and to control the output ports (band 1 and band 2).

Bit 1, bit 2 and bit 3 (T2, T1 and T0) can be used to set up Test Mode. These bits determine the phase comparator reference signal output and the counter divider output.

Bit 5 (for B2) and bit 8 (for B1) can be used to control the output ports. When either of these bits is set to 0, the corresponding port is turned OFF. When either of these bits is set to 1, the corresponding port is turned ON. Each output port can be driven at less than 10 mA.

B) Read mode (status request)

When Read Mode is selected, the power-on reset operation status, phase comparator lock detector output status, comparator input port status and 5-level AD converter pin input voltage status are output to the master device.

Bit 1 (POR) indicates the power-on reset operation status. When the power supply voltage $V_{CC}2$ is cut off, this bit is set to 1. Bit 1 is reset to 0 when a voltage of 3 V or higher is applied to $V_{CC}2$ and transmission is requested in Read Mode. At this point the new status is output. (bit 1 is also set to 1 when $V_{CC}2$ is turned ON.)

Bit 2 (FL) indicates the phase comparator lock status. When the phase comparator is locked, 1 is output. When the phase comparator is unlocked, 0 is output.

Bit 3, bit 4 and bit 5 (I-P3, I-P2, I-P1) indicate the input comparator status. I-P3, I-P2 and I-P1 indicate the status of input ports I-P3, I-P2 and I-P1 (pins 13, 14 and 15) respectively. The input voltage status for each comparator input port pin is output to the master device. High is indicated by 1. Low is indicated by 0. High represents a voltage of above 2.7 V applied to the corresponding pin. Low represents an applied voltage of below 1.5 V.

Bit 6, bit 7 and bit 8 (A2, A1 and A0) indicate the status of the five-level AD converter. The voltage applied to the AD converter input pin (pin 3) is output after being resolved to one of five levels.

To see the bit values output for the five resolution levels and to see how these levels correspond to the voltage applied to the AD converter input pin (ADCin-pin 12), please refer to the table entitled A2, A1 and A0: Five-level AD converter status (e.g. the AFT output voltage data can be given to the master device).

Data Format

A) Write mode

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W = 0	ACK
2	Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	ACK
3	Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	ACK (L)
4	Control Byte	1	×	N15	CP1	CP0	×	Rs	OS	ACK (L)
5	Band SW Byte	T2	T1	T0	×	B2	×	×	B1	ACK (L)

×: Don't care

ACK: Acknowledged

(L): Latch and transfer timing

B) Read mode

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W = 1	ACK
2	Status Byte	POR	FL	I-P3	I-P2	I-P1	A2	A1	A0	—

ACK: Acknowledged

Data Specifications

- MA1 and MA0: programmable hardware address bits

MA1	MA0	Voltage Applied to Address Pin
0	0	0 to 0.1$V_{CC}2$
0	1	OPEN or 0.2$V_{CC}2$ to 0.3$V_{CC}2$
1	0	0.4$V_{CC}2$ to 0.6$V_{CC}2$
1	1	0.9$V_{CC}2$ to $V_{CC}2$

- N15-N0: programmable counter data

- CP1 and CP0: charge pump output current setting

CP1	CP0	Output Current (μA)
0	0	±50 (typ.)
0	1	±100 (typ.)
1	0	±240 (typ.)
1	1	±490 (typ.)

- Rs: reference frequency divider ratio selection bit.

Rsa	Divider Ratio	Step Frequency	Phase Comparator Reference Frequency
0	1/128	62.5 kHz	31.25 kHz
1	1/64	125 kHz	62.5 kHz

- OS: tuning amplifier control bit
  0: Tuning amplifier ON (normal operation)
  1: Tuning amplifier OFF

- T2, T1 and T0: test mode setting bits

Parameter		T2	T1	T0	Notes
Normal operation		0	0	×	—
Charge pump	OFF	0	1	×	Charge pump is OFF.
	SINK	1	1	0	Only charge pump sink current is ON.
	SOURCE	1	1	1	Only charge pump source current is ON.
Reference signal output		1	0	0	Reference signal output (check output: ADC)
1/2 counter divider output		1	0	1	1/2 counter output (check output: ADC)
Phase comparator test		0	0	1	Comparative signal input: SDA Reference signal input: SCL

×: DON'T CARE

Note 5: When Test Mode is used, the tuning amplifier control bit OS is 0, signifying normal operation.
To test the counter divider output, programmable counter data input is required.

- B1 and B2: band output
  0: OFF
  1: ON

- POR: power-on reset flag
  0: Normal operation
  1: Reset

- FL: lock detect flag
  0: Unlocked
  1: Locked

- I-P1, I-P2 and I-P3: comparator input status
  0: Input voltage is below 1.5 V.
  1: Input voltage is above 2.7 V.

- A2, A1 and A0: five-level AD converter status

Voltage Applied to ADC Pin	A2	A1	A0
$0.60V_{CC}2$ to $V_{CC}2$	1	0	0
$0.45V_{CC}2$ to $0.60V_{CC}2$	0	1	1
$0.30V_{CC}2$ to $0.45V_{CC}2$	0	1	0
$0.15V_{CC}2$ to $0.30V_{CC}2$	0	0	1
0 V to $0.15V_{CC}2$	0	0	0

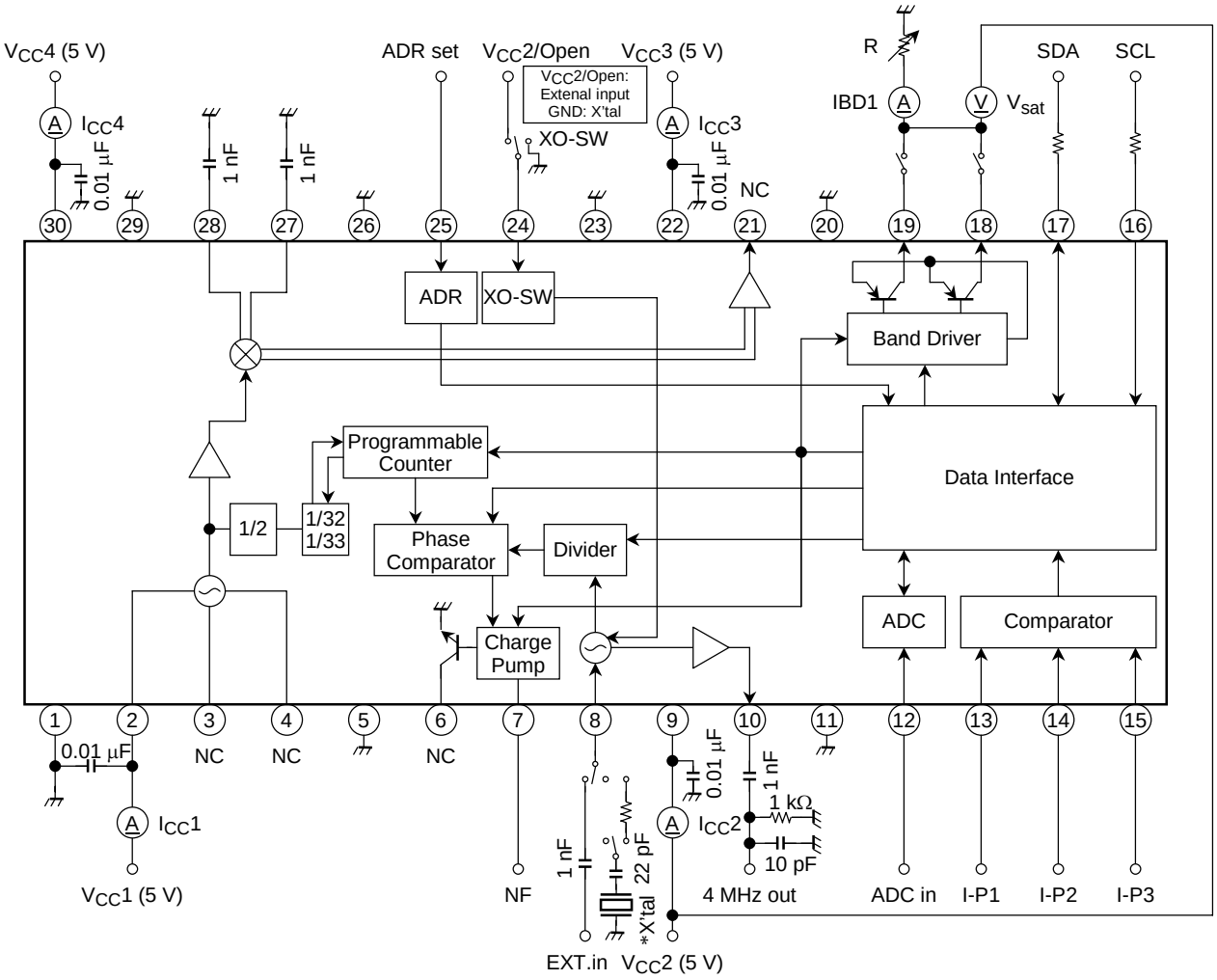
Accuracy is $\pm(0.03 \times V_{CC}2)$

- XO-SW: reference signal changeover switch

Pin 24 Status	Input Method
GND	X'tal input
$V_{CC}2$ or open	External input

Test Circuit 1

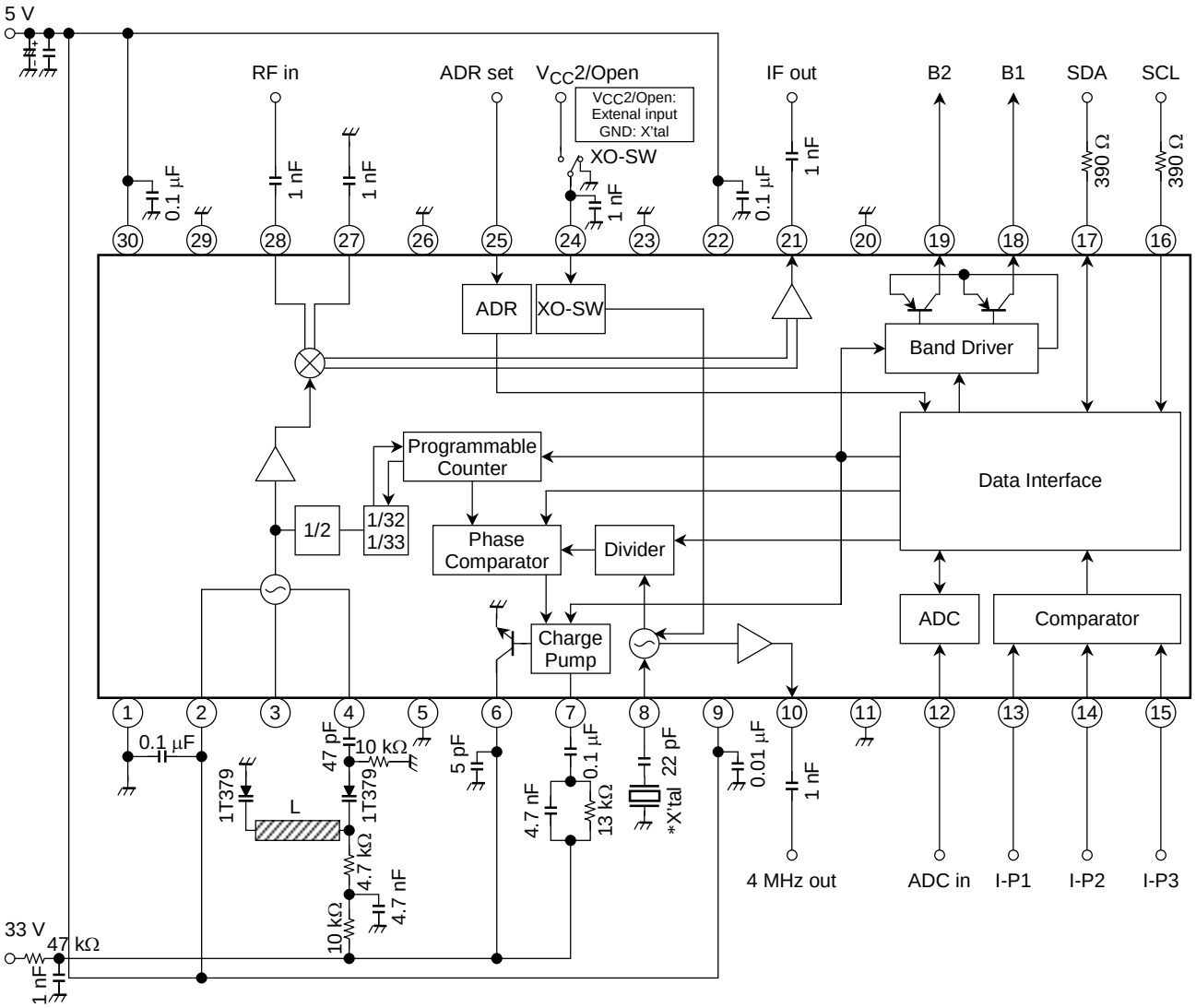
DC Characteristics



X'tal: NDK (AT-51), 4 MHz

Test Circuit 2

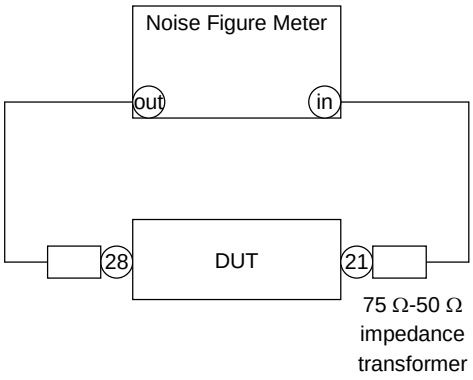
AC Characteristics



X'tal: NDK (AT-51), 4 MHz

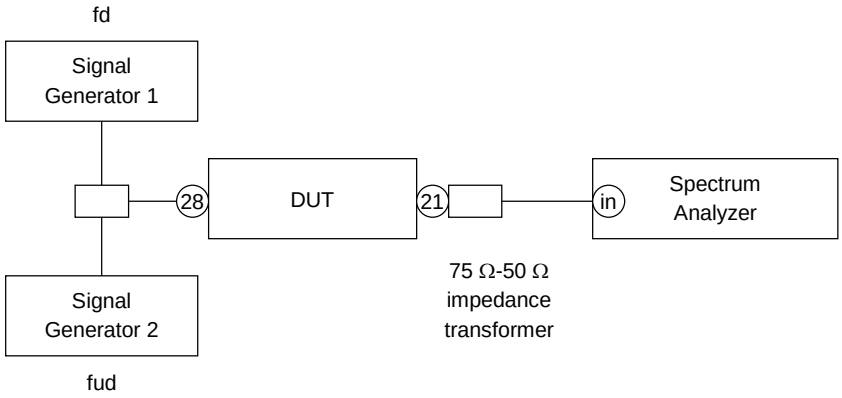
Test Circuit 3

Measuring Noise Figure



Test Circuit 4

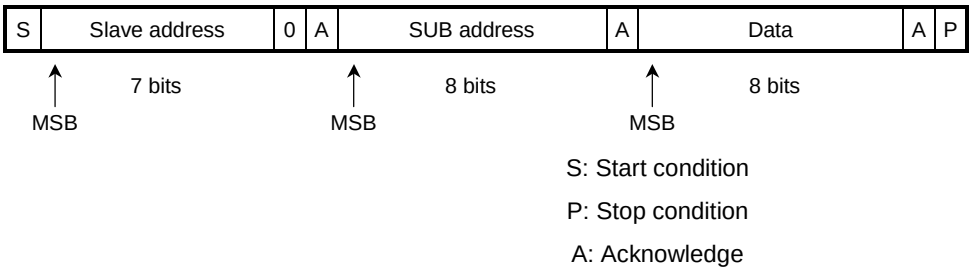
Measuring 3rd Inter Modulation



I^2C-Bus Control Summary

The bus control format of TA1296FN conforms to the Philips I^2C-bus control format.

Data Transmission Format

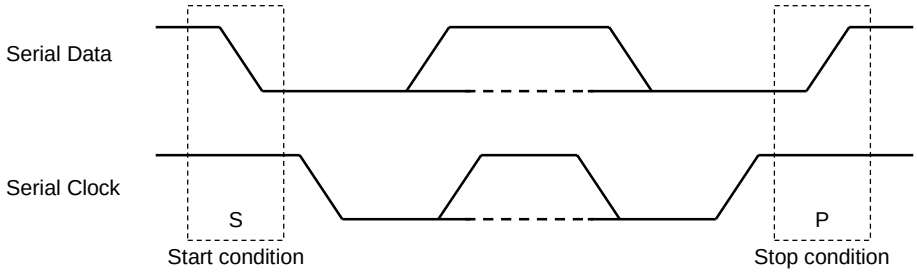


S: Start condition

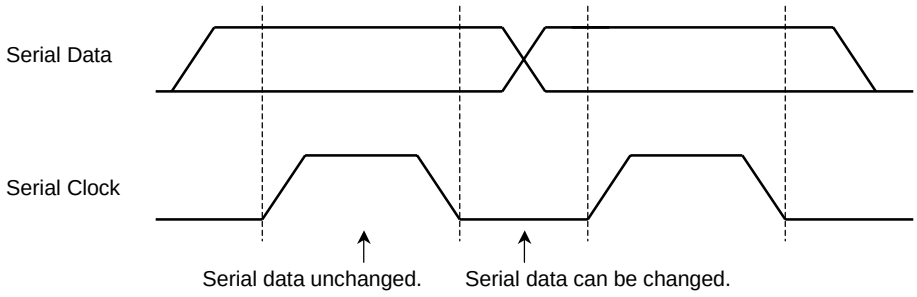
P: Stop condition

A: Acknowledge

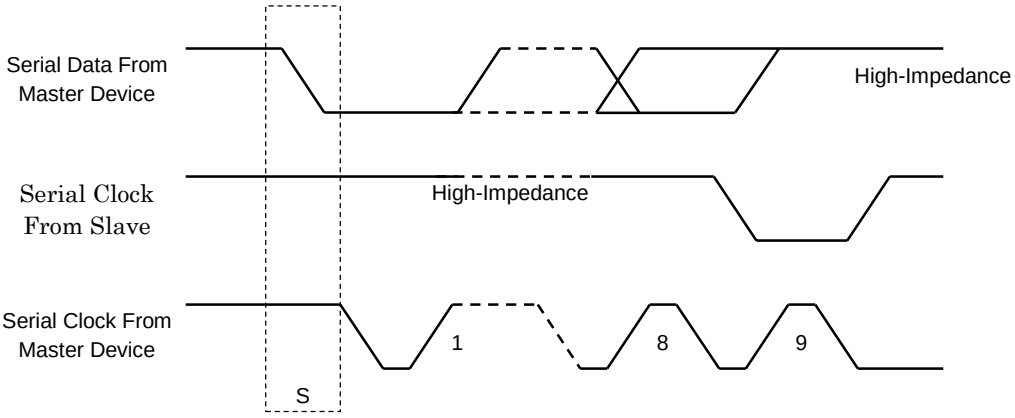
(1) Start/stop condition



(2) Bit transfer



(3) Acknowledge



(4) Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	0	*	*	0

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Tights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Handling Precautions

1. The device should not be inserted into or removed from the test jig while a voltage is being applied to it: otherwise the device may be degraded or break down.
   Also, do not abruptly increase or decrease the power supply to the device (see figure 1).
   Overshoot or chattering in the power supply may cause the IC to be degraded.
   To avoid this, filters should be placed on the power supply line.

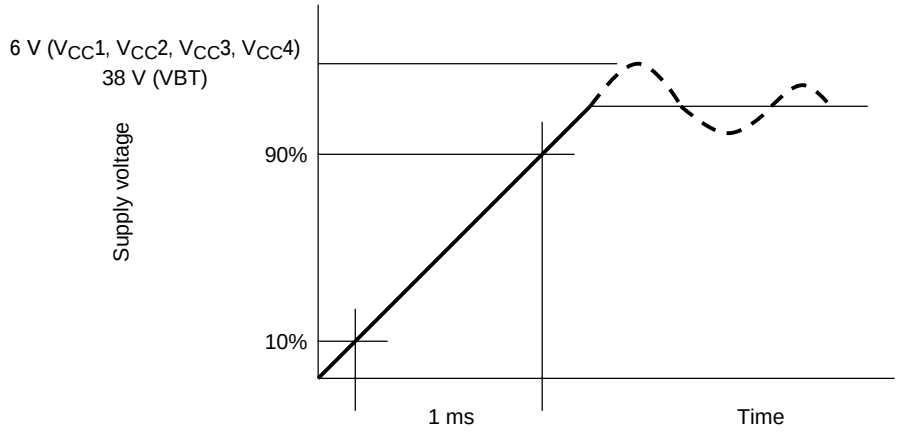


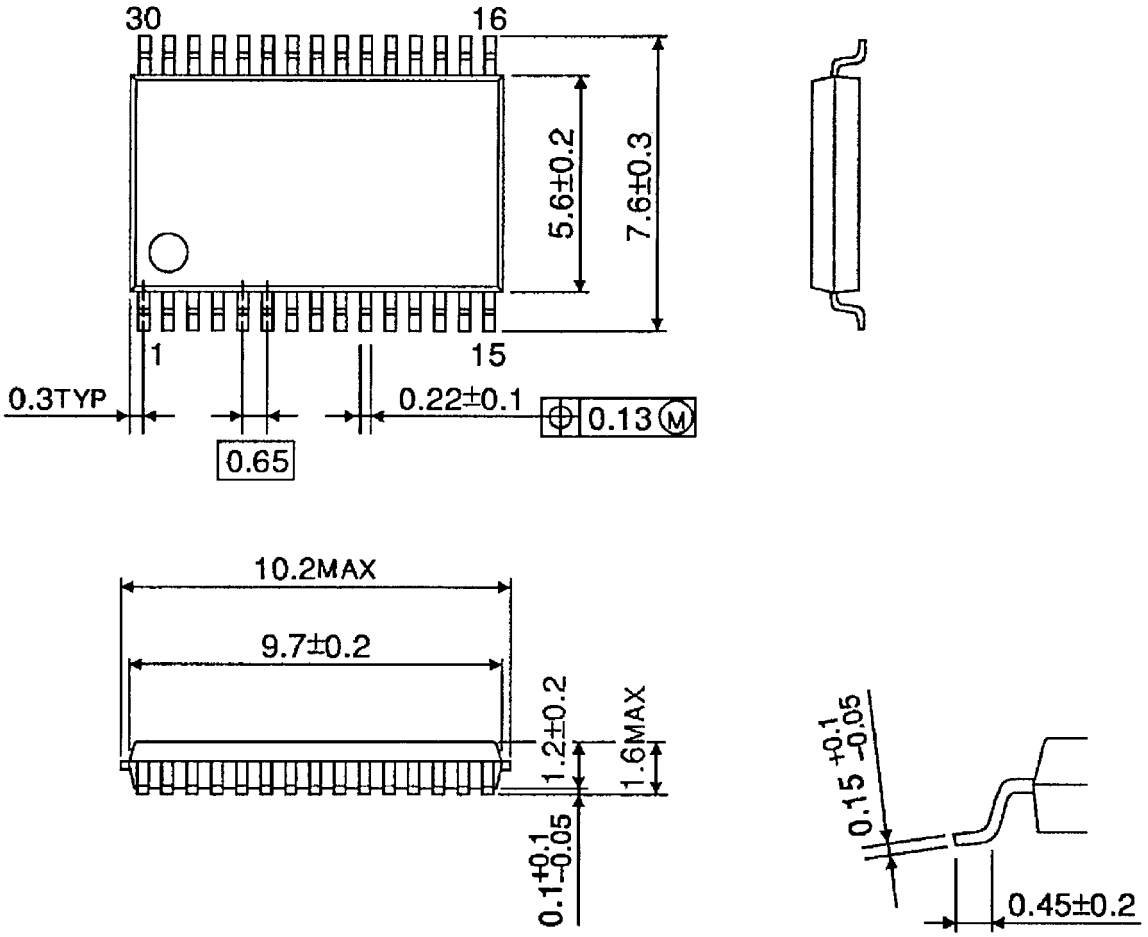
Figure 1

2. The peripheral circuits described in this datasheet are given only as system examples for evaluating the device's performance. TOSHIBA intend neither to recommend the configuration or related values of the peripheral circuits nor to manufacture such application systems in large quantities.
   Please note that the high-frequency characteristics of the device may vary depending on the external components, the mounting method and other factors relating to the application design. Therefore, the evaluation of the characteristics of application circuits is the responsibility of the designer.
   TOSHIBA only guarantee the quality and characteristics of the device as described in this datasheet and do not assume any responsibility for the customer's application design.

3. In order to better understand the quality and reliability of TOSHIBA semiconductor products and to incorporate them into designs in an appropriate manner, please refer to the latest Semiconductor Reliability Handbook (integrated circuits) published by TOSHIBA Semiconductor Company.
   This handbook can also be viewed on-line at the following URL:
   <http://www.semicon.toshiba.co.jp/noseek/us/sinrai/sinraifm.htm>.

Package Dimensions

SSOP30-P-300-0.65 Unit : mm



Weight: 0.17 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
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