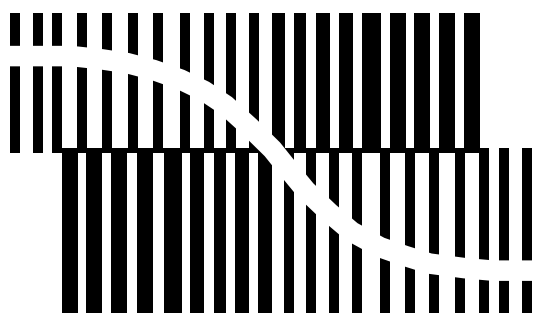


DATA SHEET



BITSTREAM CONVERSION

TDA1309H

Low-voltage low-power stereo
bitstream ADC/DAC

Product specification
Supersedes data of 1996 Jun 04
File under Integrated Circuits, IC01

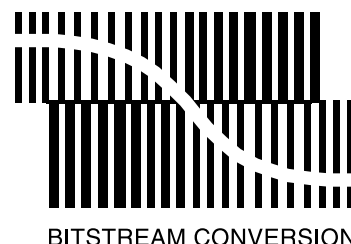
1996 Oct 21

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

FEATURES

- Low power
- Low supply voltage (2.7 V)
- Integrated high-pass filter to cancel DC offset (ADC)
- Analog loop-through function
- Multiple digital input/output formats possible
- 256f_s system clock frequency
- Several power-down modes
- Digital de-emphasis (DAC)
- Overload detector to enable automatic recording level adjustment (ADC)
- Input pads suitable for 5.5 V; low supply voltage interfacing
- High dynamic range
- DAC requires only one capacitor for post-filtering
- Small 44-pin quad flat pack with 0.8 mm pitch
- 256f_s system clock frequency in Analog-to-Digital (AD) and Digital-to-Analog (DA) mode
- Choice of three system clock frequencies (192f_s, 256f_s or 384f_s) in DA mode.



APPLICATION

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1309H is a single chip stereo analog-to-digital and digital-to-analog converter employing bitstream conversion techniques. The low voltage requirement makes the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1309H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 3\text{ V}$; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; full scale sine wave input; mode 1; $f_i = 1\text{ kHz}$; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	4.0	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	4.0	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	4.0	V
V_{DDD}	ADC and DAC digital supply voltage (pin 28)		2.7	3.0	4.0	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	4.0	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
I_{DDD}	ADC and DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
$I_{PD(DA)}$	DAC power-down current		–	15	20	mA
$I_{PD(AD)}$	ADC power-down current		–	7	10	mA
T_{amb}	operating ambient temperature		–20	–	+75	°C
Analog-to-digital converter						
$V_{I(\text{rms})}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_I = 0\text{ V}$; A-weighted	90	95	–	dB
α_{CS}	channel separation		–	90	–	dB
Digital-to-analog converter						
$V_{O(\text{rms})}$	output voltage (RMS value)	note 2	0.43	0.5	0.57	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 3	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{CS}	channel separation		90	100	–	dB

Notes

1. The input voltage for full scale digital output is a function of $V_{DDA(AD)}$.
2. At full scale digital input; no de-emphasis; $V_{O(\text{rms})}$ is a function of $V_{DDA(DA)}$.
3. 18-bit input data.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

BLOCK DIAGRAM

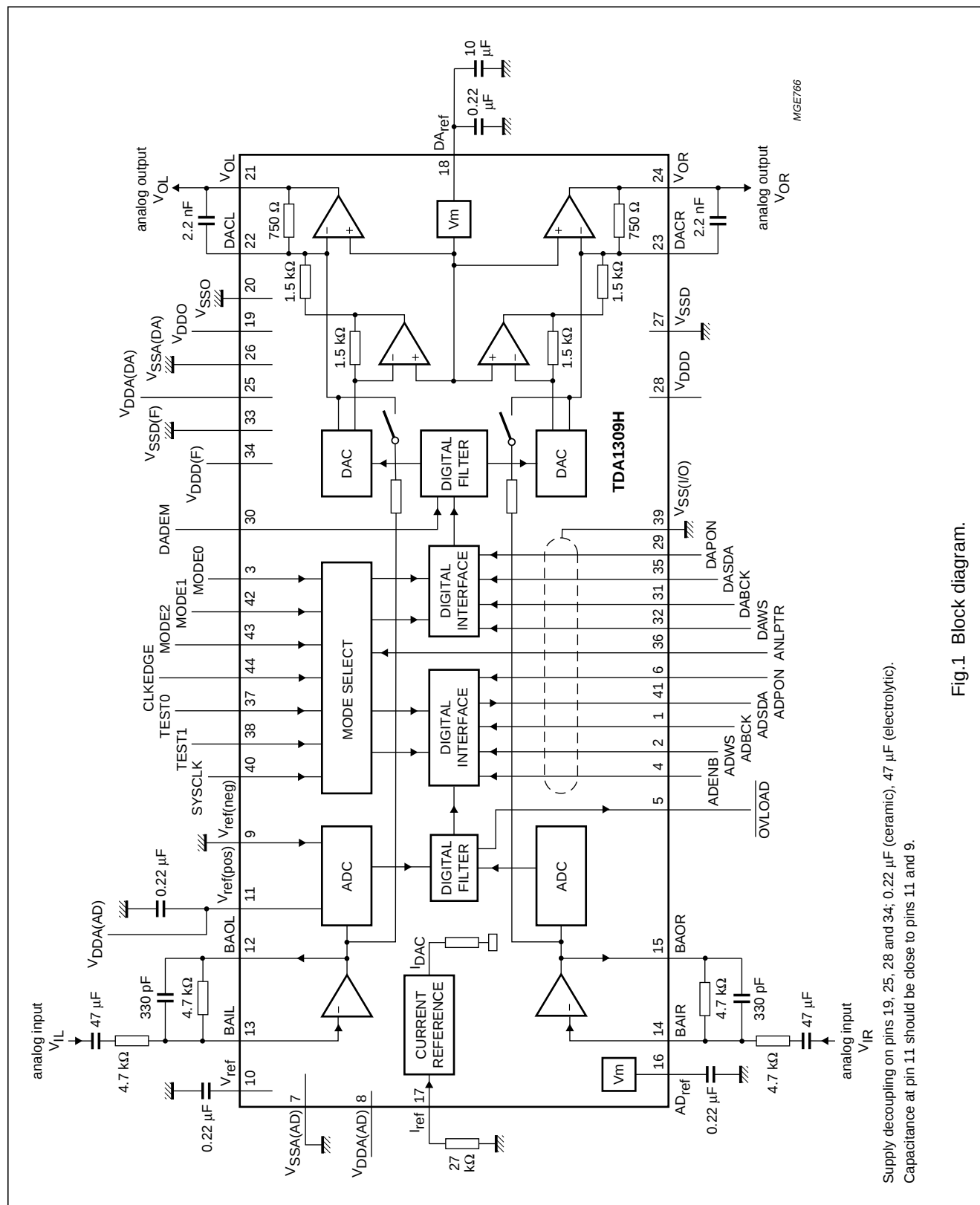


Fig.1 Block diagram.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

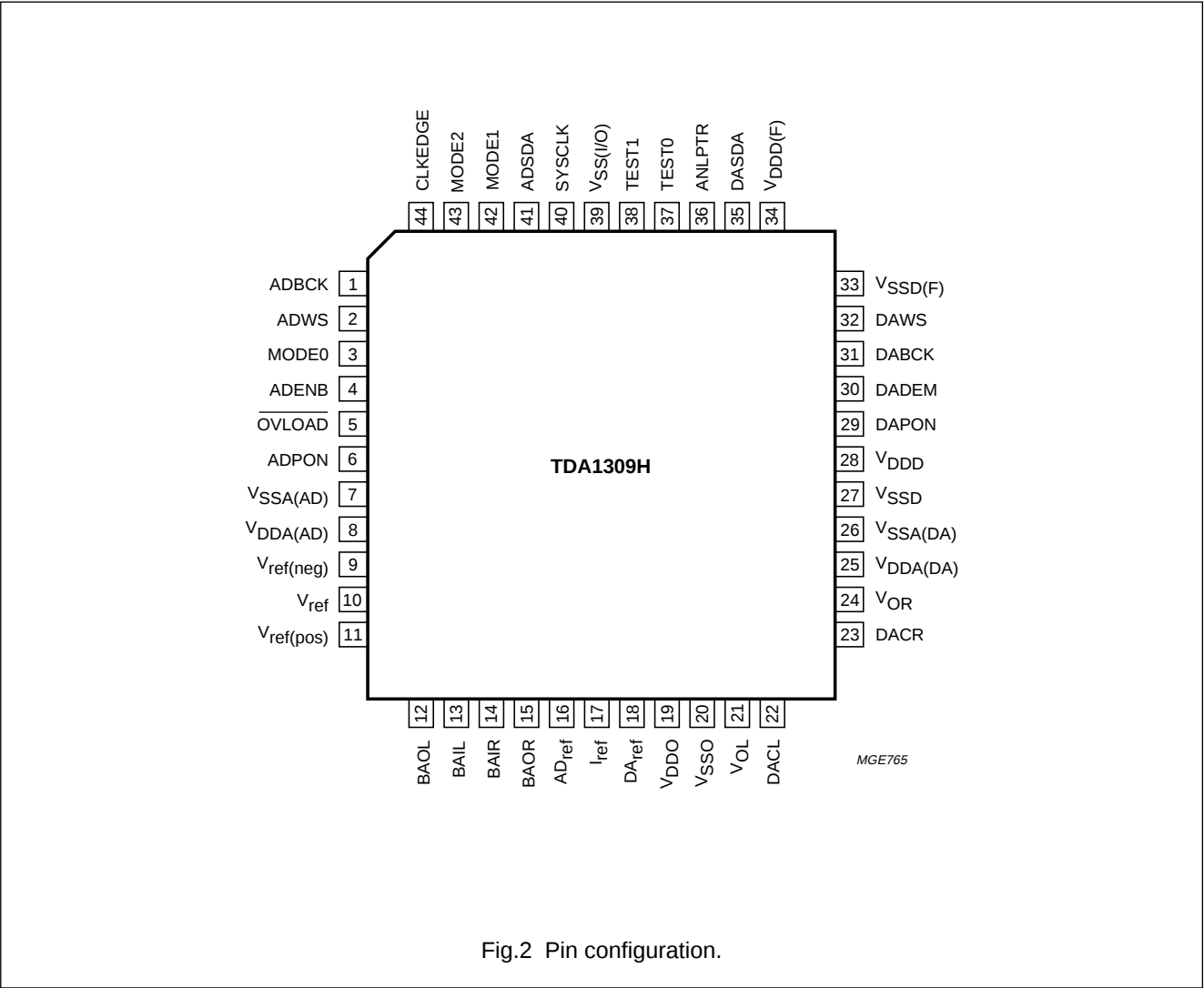
PINNING

SYMBOL	PIN	DESCRIPTION
ADBCK	1	ADC input bit clock; $32f_s$ or $64f_s$
ADWS	2	ADC word select input at f_s
MODE0	3	ADC/DAC mode select input
ADENB	4	ADC serial data enable input (active HIGH)
OVLOAD	5	ADC output overload flag (active LOW)
ADPON	6	ADC power-on-mode input (active HIGH)
$V_{SSA(AD)}$	7	ADC analog ground supply voltage
$V_{DDA(AD)}$	8	ADC analog supply voltage
$V_{ref(neg)}$	9	ADC negative reference voltage input (ground)
V_{ref}	10	ADC decoupling capacitor
$V_{ref(pos)}$	11	ADC positive reference voltage decoupling capacitor
BAOL	12	ADC input amplifier output left
BAIL	13	ADC input amplifier virtual ground left
BAIR	14	ADC input amplifier virtual ground right
BAOR	15	ADC input amplifier output right
AD_{ref}	16	ADC decoupling capacitor
I_{ref}	17	ADC/DAC reference current resistor input
DA_{ref}	18	DAC decoupling capacitor
V_{DDO}	19	ADC/DAC operational amplifier supply voltage
V_{SSO}	20	ADC/DAC operational amplifier ground supply voltage
V_{OL}	21	DAC output voltage left
DACL	22	DAC output current left
DACR	23	DAC output current right
V_{OR}	24	DAC output voltage right
$V_{DDA(DA)}$	25	DAC analog supply voltage
$V_{SSA(DA)}$	26	DAC analog ground supply voltage
V_{SSD}	27	ADC/DAC digital ground supply voltage
V_{DDD}	28	ADC/DAC digital supply voltage
DAPON	29	DAC power-on-mode input (active HIGH)
DADEM	30	DAC digital de-emphasis input (active HIGH)
DABCK	31	DAC input bit clock; $32f_s$, $48f_s$ or $64f_s$
DAWS	32	DAC word select input at f_s
$V_{SSD(F)}$	33	ADC/DAC digital filters ground supply voltage
$V_{DDD(F)}$	34	ADC/DAC digital filters supply voltage
DASDA	35	DAC serial data input
ANLPTR	36	ADC/DAC analog loop-through input (active HIGH)
TEST0	37	ADC/DAC enable test mode 0 input (LOW is normal mode)
TEST1	38	ADC/DAC enable test mode 1 input (LOW is normal mode)
$V_{SS(I/O)}$	39	ADC/DAC digital input/output ground supply voltage
SYSCLK	40	ADC/DAC system clock input ($f_{sys} = 256f_s$; DAC also $192f_s$ and $384f_s$)

Low-voltage low-power stereo bitstream
ADC/DAC

TDA1309H

SYMBOL	PIN	DESCRIPTION
ADSDA	41	ADC serial data output
MODE1	42	ADC/DAC mode 1 select input
MODE2	43	ADC/DAC mode 2 select input
CLKEDGE	44	ADC/DAC input bit clock rising/falling edge



Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

FUNCTIONAL DESCRIPTION

Figure 1 illustrates the various components of the TDA1309H.

The analog-to-digital converter is a bitstream type converter, both channels are sampled simultaneously. The digital-to-analog converter is a BCC (Bitstream Continuous Calibration) type converter. The digital filter for the ADC is a bit serial IIR filter that produces a fairly linear phase response up to 15 kHz. A high-pass filter is incorporated in the down-sampling path to remove DC offsets. An overload detection circuit is incorporated to facilitate automatic recording level adjustment.

The digital up-sample filter for the DAC is partly IIR, with virtual linear phase response up to 15 kHz, and partly FIR. A switchable digital de-emphasis circuit is also incorporated. Due to the BCC principle used, the DAC needs only single pole post-filtering (one external capacitor) to meet the out-of-band suppression requirement.

The ADC and DAC channels have separate power-down modes, to reduce power if one of them is not in use. An analog loop-through function enables analog-input analog-output mode without using the ADC and DAC converters or filters, thereby switching them off to reduce power consumption.

The digital interfaces accommodates, 16 and 18-bit, I²S-bus and LSB justified formats. The ADC digital output can be made 3-state by means of the ADENB signal, this enables the use of a digital bus.

The TDA1309H interface accommodates slave mode only, therefore, the system ICs must provide the system clock, bit clock and word clock signals. For the DAC, the TDA1309H accepts the data together with these clocks, for the ADC it delivers the data in response to these clocks. Within one stereo frame, the first sample always represents the left channel. When sending data the unused bit positions are set to zero, when receiving data these bit positions are don't cares.

To accommodate the various interface formats and system clock frequencies four control pins are provided, MODE0 to MODE2 for mode selection and CLKEDGE which selects the active edge of the BCK signal. Table 1 gives the interface mode selection, Fig.3 illustrates the ADC/DAC data formats and Fig.5 the operating modes.

The section of the TDA1309H is designed to accommodate two main modes:

1. The 256f_s mode in which analog-to-digital and digital-to-analog can be used
2. The 192f_s or 384f_s mode (digital-to-analog only).

Table 1 Interface mode selection

DEVICE PIN			ADC/DAC FORMATS				
MODE 2	MODE 1	MODE 0	TYPE	BITS	BCK	SYS; f _{sys}	FIGURE
0	0	0	LSB justified	16	32f _s	256f _s	3(a)
0	0	1	LSB justified	16	64f _s	256f _s	3(b)
0	1	0	LSB justified	16	48f _s	192f _s ⁽¹⁾	4(a)
0	1	1	LSB justified	18	64f _s	256f _s	3(c)
1	0	0	I ² S-bus	16	32f _s	256f _s	3(d)
1	0	1	I ² S-bus	16	64f _s	256f _s	3(e)
1	1	0	I ² S-bus	16	48f _s	384f _s ⁽¹⁾	4(b)
1	1	1	I ² S-bus	18	64f _s	256f _s	3(f)

Note

1. Only digital-to-analog.

Table 2 Clock edge mode

CLKEDGE	VALID EDGE OF BCK	
	ADC	DAC
0	falling	rising
1	rising	falling

Low-voltage low-power stereo bitstream
ADC/DAC

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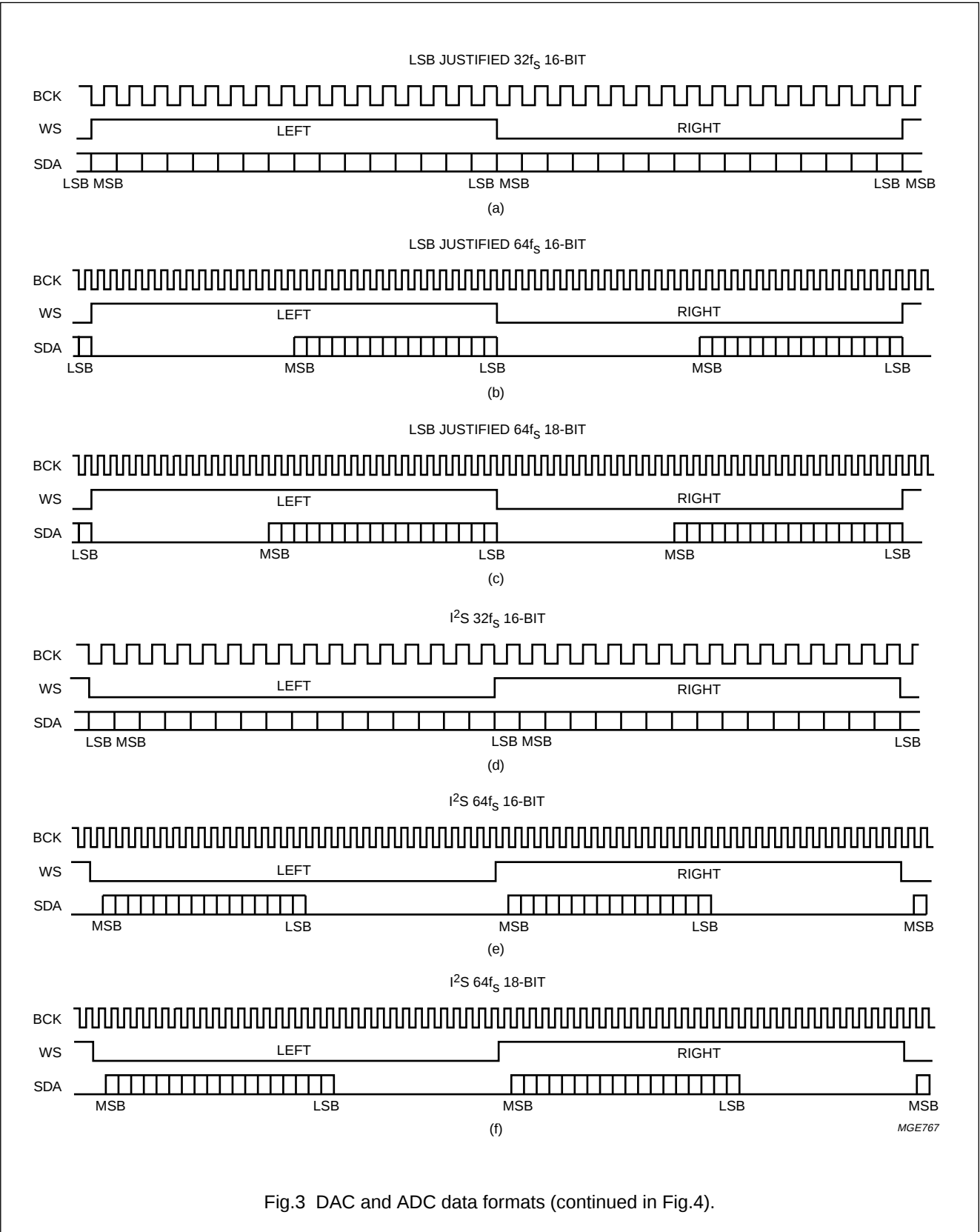
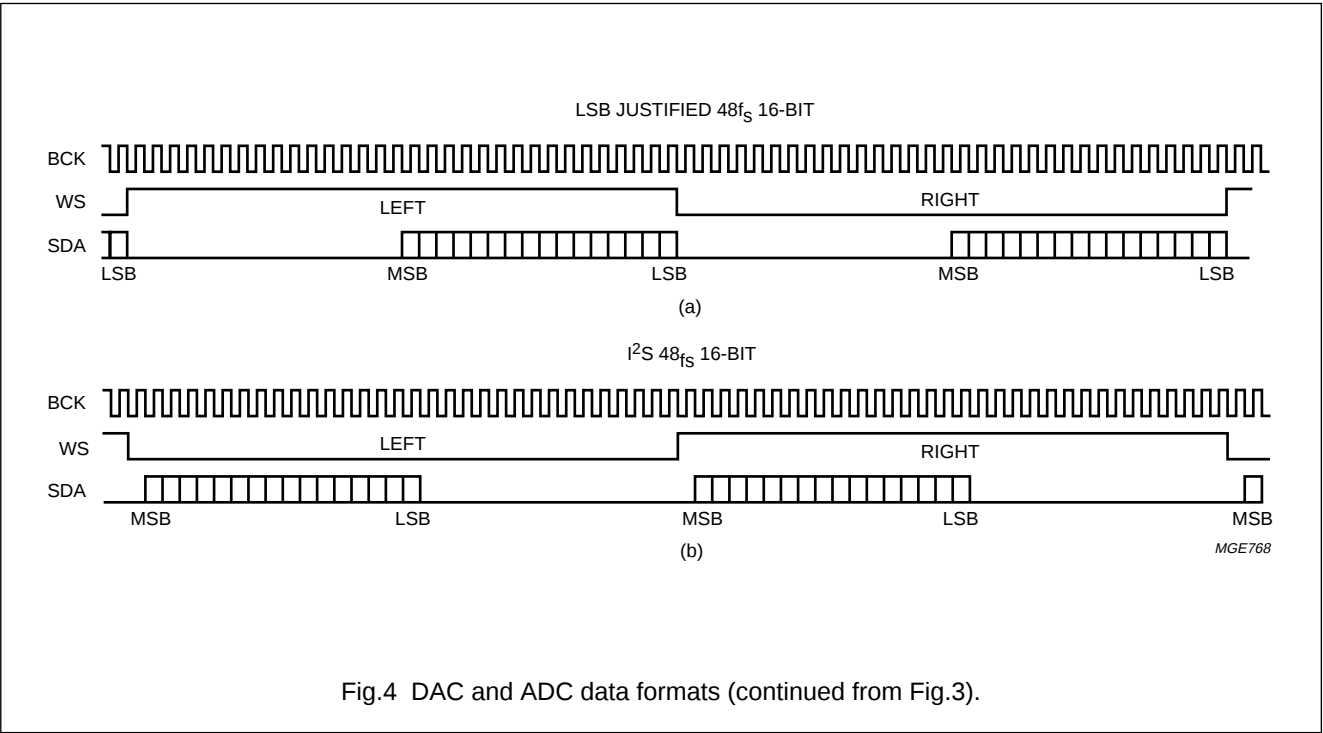


Fig.3 DAC and ADC data formats (continued in Fig.4).

Low-voltage low-power stereo bitstream
ADC/DAC

TDA1309H



There are different modes in which the TDA1309H can operate. These modes can be selected as shown in Table 3 and Fig.5. In mode a, the digital filters clock is switched off. Switching over to one of the ADC active modes (b, c or d) initiates a reset sequence of the digital filters. This mode should be activated immediately after power-on for at least 2 clock periods.

Table 3 Operating mode selection

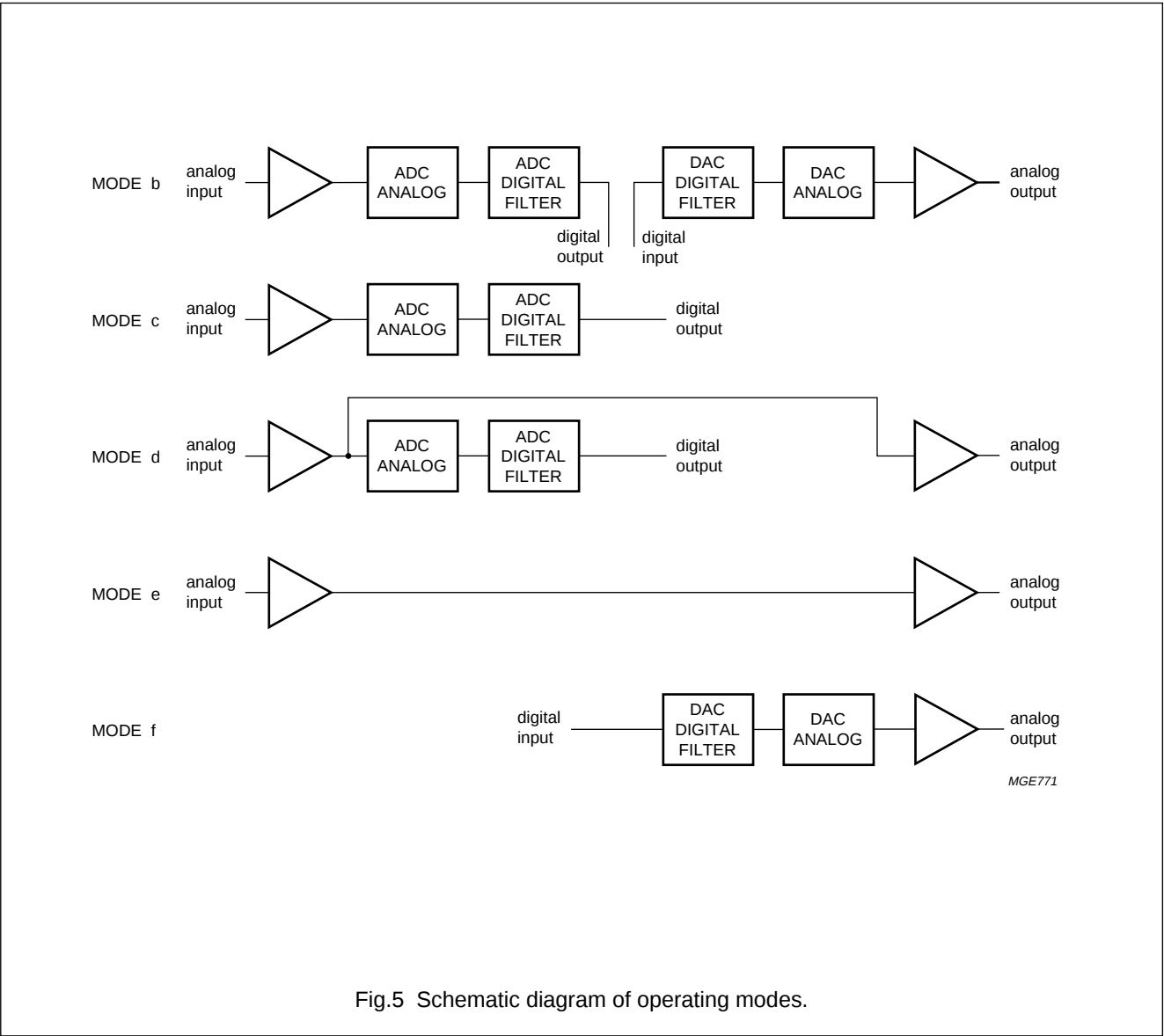
MODE	DESCRIPTION	DEVICE PIN LOGIC		
		ANLPTR	ADPON	DAPON
a	not used	0	0	0
b	record and playback	0	1	1
c	record only	0	1	0
d	record and analog loop-through	1	1	0
e	analog loop-through	1	0	0
f	playback only	0	0	1
g and h	reserved	1	X ⁽¹⁾	1

Note

1. X = don't care.

Low-voltage low-power stereo bitstream
ADC/DAC

TDA1309H



Low-voltage low-power stereo bitstream ADC/DAC

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDA(AD)}$	analog supply voltage (pin 8)		–	4.5	V
$V_{DDA(DA)}$	analog supply voltage (pin 25)		–	4.5	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		–	4.5	V
V_{DDD}	digital supply voltage (pin 28)		–	4.5	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		–	4.5	V
ΔV_{DD}	maximum supply voltage difference		–	100	mV
ΔV_{SS}	maximum ground supply voltage difference		–	100	mV
V_I	maximum input voltage		–0.5	$V_{DD} + 0.5$	V
I_{IK}	DC clamp input diode current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	–	± 10	mA
I_{OK}	DC output clamp diode current; (output type 2 mA)	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	–	± 10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
V_{es}	electrostatic handling	note 1	–1500	+1500	V
		note 2	–300	+300	V

Notes

- Human body model: $C = 100$ pF; $R = 1.5$ k Ω ; 3 zaps positive and 3 zaps negative.
- Machine model: $C = 200$ pF; $L = 0.5$ μ H; $R = 10$ Ω ; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	60	K/W

QUALITY SPECIFICATION

In accordance with “SNW-FQ-611E”. The number of this quality specification can be found in the “Quality Reference Handbook”. The handbook can be ordered using the code 9397 750 00192.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 3\text{ V}$; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; full scale sine wave input; mode 1; $f_i = 1\text{ kHz}$; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	4.0	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	4.0	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	4.0	V
V_{DDD}	ADC/DAC digital supply voltage (pin 28)		2.7	3.0	4.0	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	4.0	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
		ADC power-down	–	0.3	1	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
		DAC power-down	–	1.4	2	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
		DAC power-down	–	5.5	9	mA
		ADC power-down	–	7	11	mA
		ADC/DAC power-down	–	0	–	mA
I_{DDD}	ADC/DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
		DAC power-down	–	15	20	mA
		ADC power-down	–	7	10	mA
$I_{DDD(F)q}$	digital filters quiescent current		–	–	100	μA

Low-voltage low-power stereo bitstream ADC/DAC

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
I_I	input current (pins 13 and 14)		–	–	10	nA
ΔV_O	unbalance between channels		–	–	0.3	dB
RES	resolution	16-bit format	–	16	–	bits
		18-bit format	–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –20 dB	–	–75	–	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_i = 0$ V; A-weighted	90	95	–	dB
α_{CS}	channel separation		–	90	–	dB
PSRR	power supply rejection ratio	note 2	–	–30	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 3	0.43	0.5	0.57	V
ΔV_O	unbalance between channels		–	0.1	–	dB
R_L	load resistance		5	–	–	k Ω
C_L	load capacitance	note 4	–	–	200	pF
RES	resolution	16-bit format	–	16	–	bits
		18-bit format	–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –20 dB	–	–75	–	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 5	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{CS}	channel separation		90	100	–	dB
PSRR	power supply rejection ratio	note 2	–	–30	–	dB
Analog loop-through (mode e)						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–	dB
S/N	idle channel signal-to-noise ratio	$V_i = 0$ V; A-weighted	–	95	–	dB
G_{ltr}	loop-through gain	note 1	–	–1.1	–	dB
E_{OS}	DC offset error		–	1.0	–	mV

Low-voltage low-power stereo bitstream ADC/DAC

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital decimation filter						
$f_{s(o)}$	output sample frequency		28	44.1	54	kHz
$f_{s(i)}$	input sample frequency		–	$128f_s$	–	
f_{sys}	system clock frequency		$256f_s$	–	$256f_s$	
B	signal bandwidth	$f_{s(o)} = 44.1$ kHz	0.02	–	20	kHz
A_{sup}	aliasing suppression	$f_{s(o)} - B < f_i < 2f_{s(o)} - B$; note 6	60	–	–	dB
		$f_i > 2f_{s(o)} - B$; note 6	80	–	–	dB
α	frequency response	$f_i = 20$ Hz to 20 kHz	–0.2	–	+0.2	dB
OL_{det}	overload detection level	note 7	–	0.11	–	dB
Digital-to-analog interpolation filter						
$f_{s(o)}$	output sample frequency		–	$64f_s$	–	
$f_{s(i)}$	input sample frequency		28	44.1	54	kHz
f_{sys}	system clock frequency		$256f_s$	–	$256f_s$	
B	signal bandwidth	$f_{s(i)} = 44.1$ kHz	0.02	–	20	kHz
α	frequency response	$f_i = 20$ Hz to 20 kHz	–0.2	–	+0.2	dB
SUP	out-of-band suppression		40	50	–	dB
Digital part; note 8						
INPUTS (PINS 1 TO 4, 6, 29 TO 32, 35 TO 38, 40 AND 42 TO 44)						
V_{IL}	LOW level input voltage		–0.5	–	$0.3V_{DDD}$	V
$ I_{IL} $	LOW level input current	$V_I = V_{SSD}$	–	–	10	μA
$ I_{IH} $	HIGH level input current	$V_I = V_{DDD}$	–	–	10	μA
$C_{I(max)}$	maximum input capacitance		–	–	10	pF
INPUTS (PINS 1 TO 4, 6, 29 TO 32, 35 TO 38, 40 AND 42)						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	5.5	V
INPUTS (PINS 43 AND 44)						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	$V_{DDD} + 0.5$	V
OUTPUTS (PINS 5 AND 41)						
V_{OL}	LOW level output voltage	$I_{OL} = 2$ mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	$I_{OH} = -2$ mA	$V_{DDD} - 0.5$	–	–	V
$ I_{OZ} $	3-state leakage current	$V_O = V_{DDD}$ or V_{SSD}	–	–	10	μA

Low-voltage low-power stereo bitstream ADC/DAC

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
BIT CLOCK (BCK) RELATED SIGNALS (see Fig.6); CLKEDGE = 0						
T_{cy}	clock period		300	–	–	ns
t_{HC}	clock HIGH time		100	–	–	ns
t_{LC}	clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_{suWS}	set-up time WS to rising edge of BCK		20	–	–	ns
t_{hWS}	hold time WS to rising edge of BCK		0	–	–	ns
t_{suDA}	set-up time SDA (DAC) to rising edge of BCK		20	–	–	ns
t_{hDA}	hold time SDA (DAC) to rising edge of BCK		0	–	–	ns
t_{hAD}	hold time SDA (ADC) to falling edge of BCK		0	–	–	ns
t_{dAD}	delay time SDA (ADC) to falling edge of BCK		–	–	80	ns
SYSTEM CLOCK (SYSCLK) RELATED SIGNALS (see Fig.7)						
T_{cy}	clock period		72	–	–	ns
t_{HC}	clock HIGH time		22	–	–	ns
t_{LC}	clock LOW time		22	–	–	ns
t_r	rise time		–	–	10	ns
t_f	fall time		–	–	10	ns

Notes

1. V_I for full scale digital output is a function of $V_{DDA(AD)}$, 0.5 V (RMS) (at 3 V the digital voltages are equivalent to –1.1 dB in the digital domain).
2. $V_{ripple} = 1\%$ of the supply voltage and $f_{ripple} = 100$ Hz.
3. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
4. For a load capacitance greater than 33 pF a series resistor of 200 Ω is recommended.
5. 18 bits input data.
6. The aliasing suppression frequency is mirrored around $128f_s$.
7. $V_{DDA} = 3$ V; indicated digital level is with respect to –1.1 dB (no overload).
8. All digital voltages = 2.7 to 4.0 V; all ground supply voltages = 0 V; $T_{amb} = -20$ to $+75$ °C.

Low-voltage low-power stereo bitstream
ADC/DAC

TDA1309H

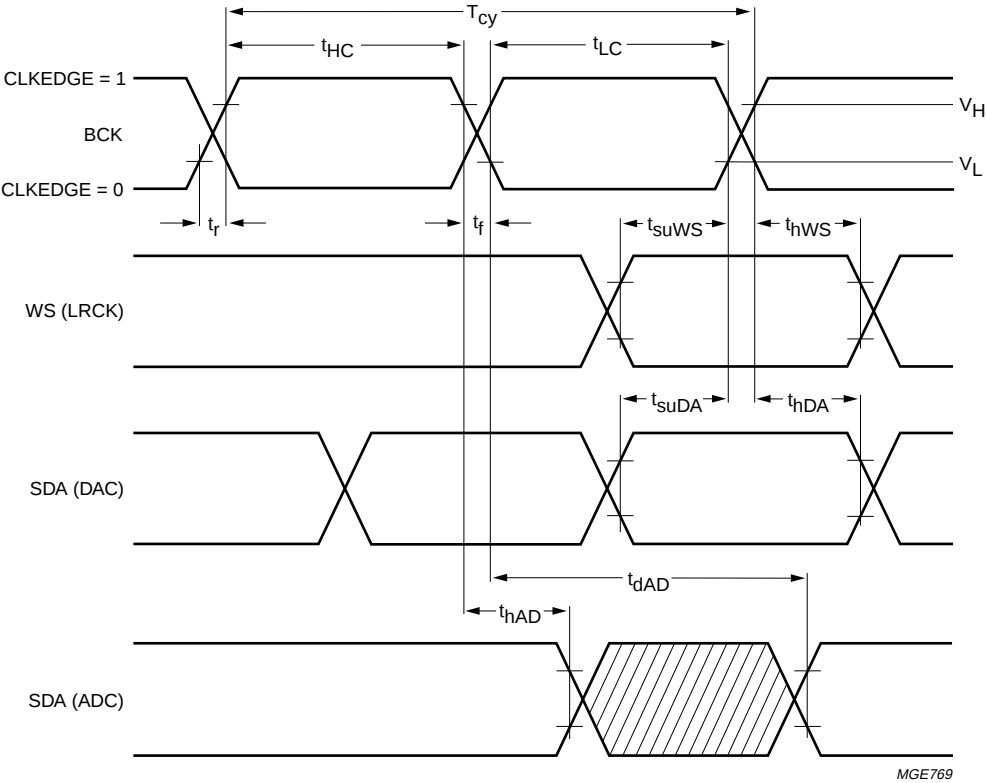


Fig.6 Serial timing of BCK related signals.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

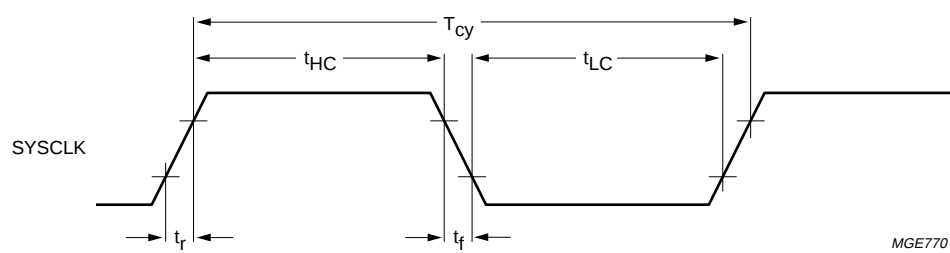


Fig.7 Serial timing of SYSCLK related signals.

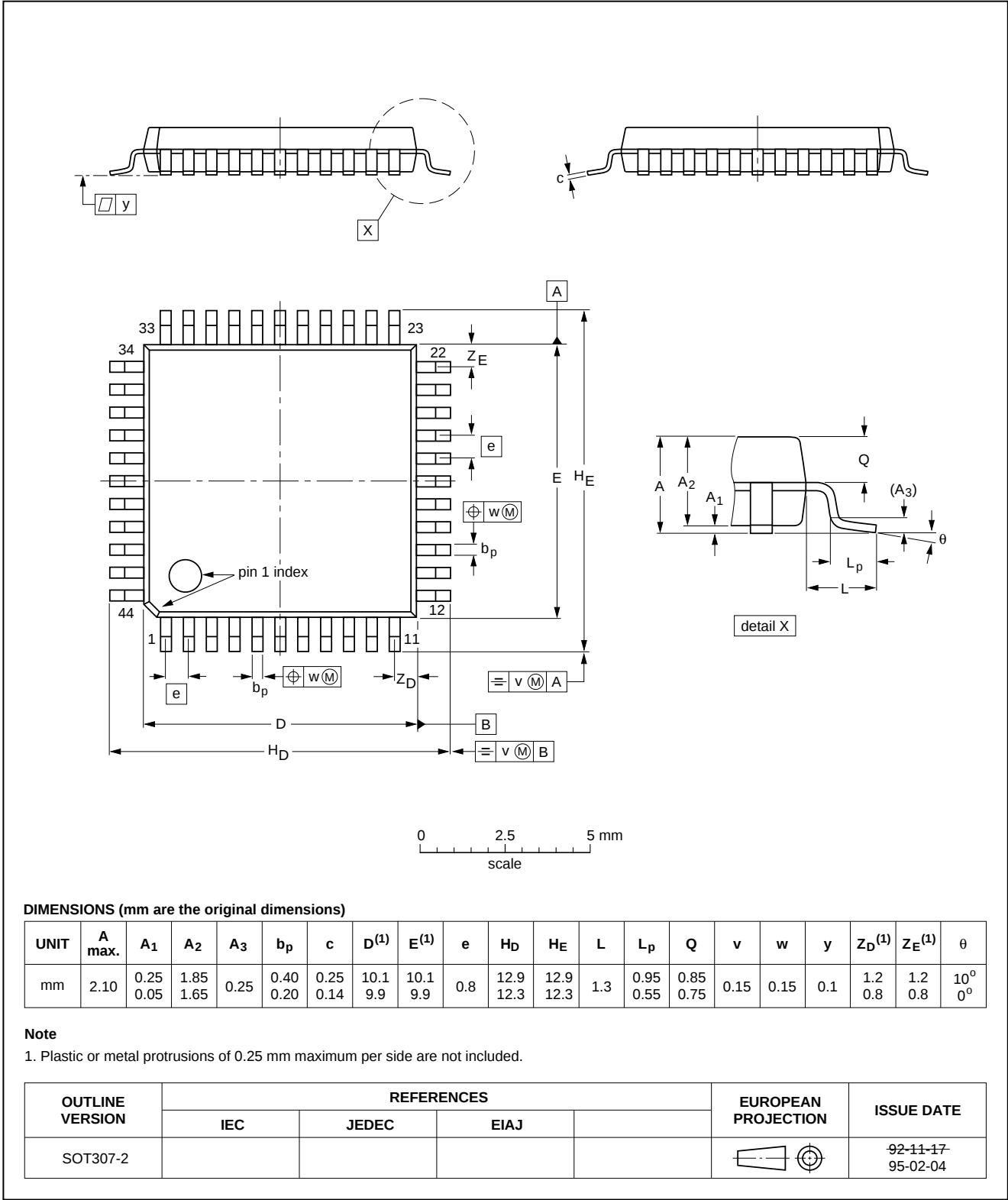
Low-voltage low-power stereo bitstream
ADC/DAC

TDA1309H

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages:

QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
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Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoprojekt, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 247 9145, Fax. +7 095 247 9144

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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