BSS138L, BVSS138L

Power MOSFET 200 mA, 50 V

N−Channel SOT−23

Typical applications are DC−DC converters, power management in portable and battery−powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

Features

- Low Threshold Voltage ($V_{GS(th)}$: 0.5 V−1.5 V) Makes it Ideal for Low Voltage Applications
- Miniature SOT−23 Surface Mount Package Saves Board Space
- BVSS Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

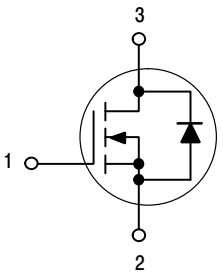
ON Semiconductor®

http://onsemi.com

200 mA, 50 V

$R_{DS(on)}$ = 3.5 Ω

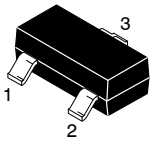
N−Channel



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

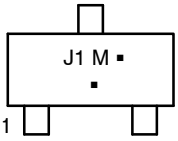
Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	50	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	± 20	Vdc
Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current ($t_p \le 10$ μs)	 I_D I_{DM}	 200 800	mA
Total Power Dissipation @ T_A = 25°C	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



SOT−23
CASE 318
STYLE 21

MARKING DIAGRAM



J1 = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
BSS138LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
BVSS138LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
BSS138LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	50	–	–	Vdc
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, 25°C)			–	–	0.1	
(V_{DS} = 50 Vdc, V_{GS} = 0 Vdc, 25°C)			–	–	0.5	
(V_{DS} = 50 Vdc, V_{GS} = 0 Vdc, 150°C)			–	–	5.0	
Gate−Source Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±0.1	μAdc
ON CHARACTERISTICS (Note 1)						
Gate−Source Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc)		$V_{GS(th)}$	0.5	–	1.5	Vdc
Static Drain−to−Source On−Resistance		$r_{DS(on)}$				Ω
(V_{GS} = 2.75 Vdc, I_D < 200 mAdc, T_A = −40°C to +85°C)			–	5.6	10	
(V_{GS} = 5.0 Vdc, I_D = 200 mAdc)			–	–	3.5	
Forward Transconductance (V_{DS} = 25 Vdc, I_D = 200 mAdc, f = 1.0 kHz)		g_{fs}	100	–	–	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	40	50	pF
Output Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	12	25	
Transfer Capacitance	(V_{DG} = 25 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	3.5	5.0	
SWITCHING CHARACTERISTICS (Note 2)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 0.2 Adc,)	$t_{d(on)}$	–	–	20	ns
Turn−Off Delay Time		$t_{d(off)}$	–	–	20	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

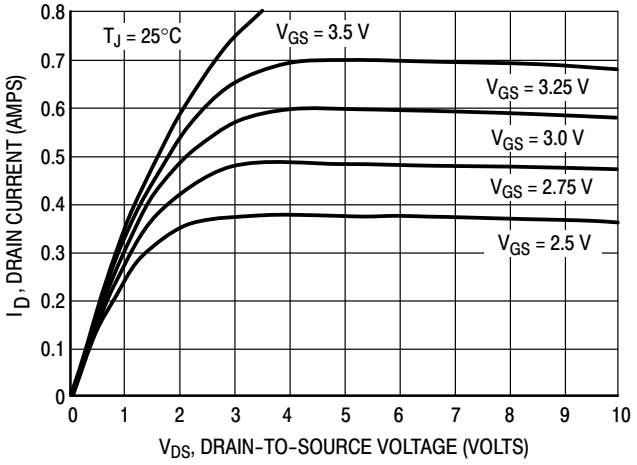


Figure 1. On−Region Characteristics

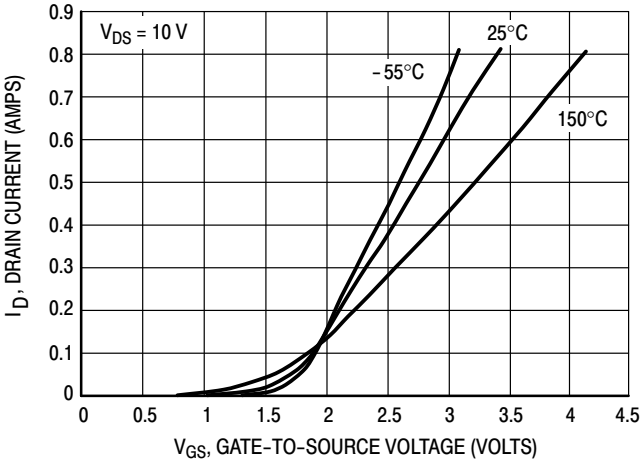


Figure 2. Transfer Characteristics

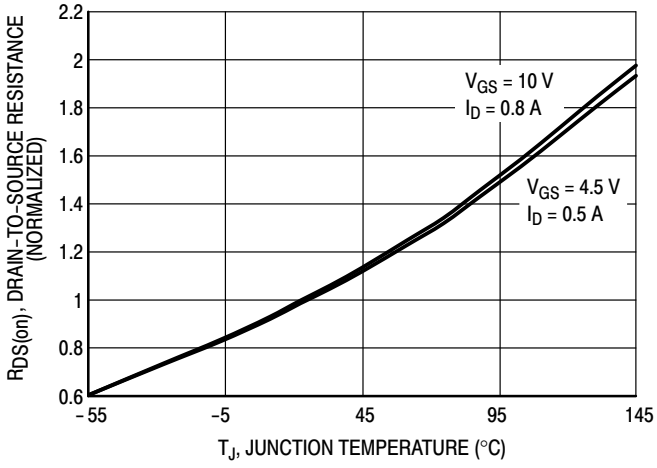


Figure 3. On−Resistance Variation with Temperature

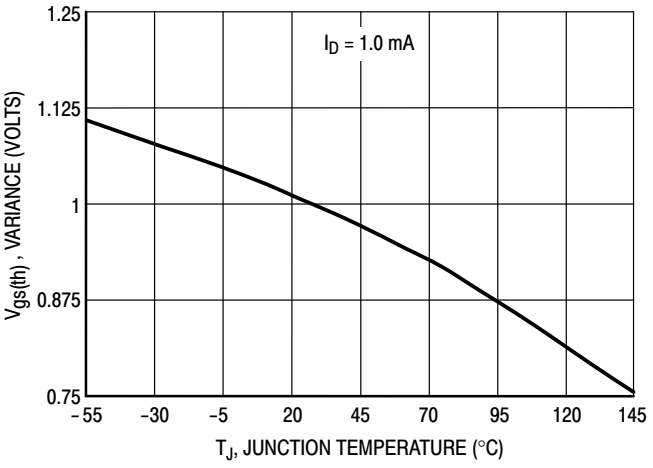


Figure 4. Threshold Voltage Variation with Temperature

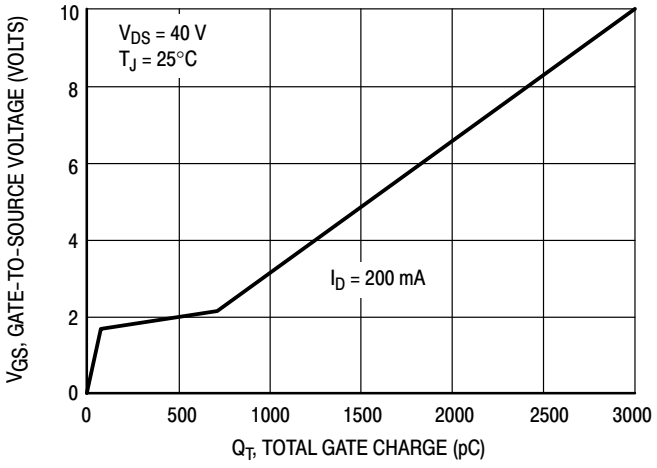


Figure 5. Gate Charge

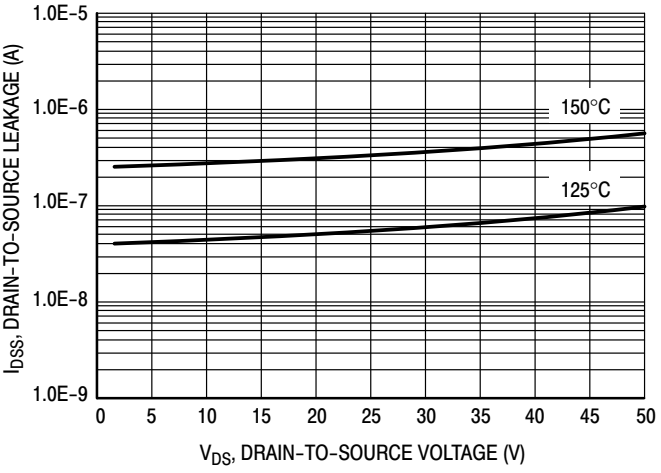


Figure 6. IDSS

TYPICAL ELECTRICAL CHARACTERISTICS

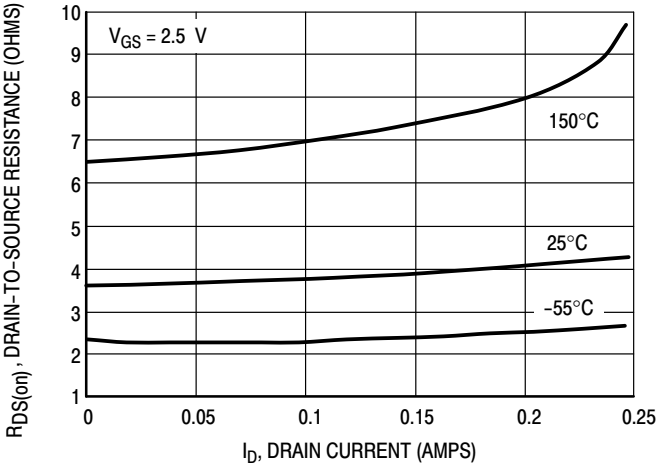


Figure 7. On−Resistance versus Drain Current

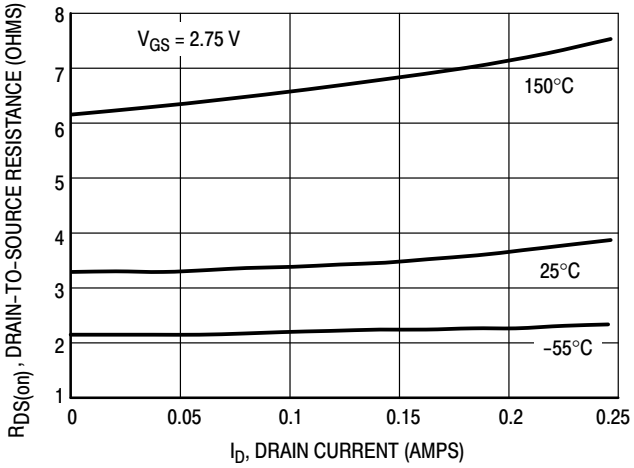


Figure 8. On−Resistance versus Drain Current

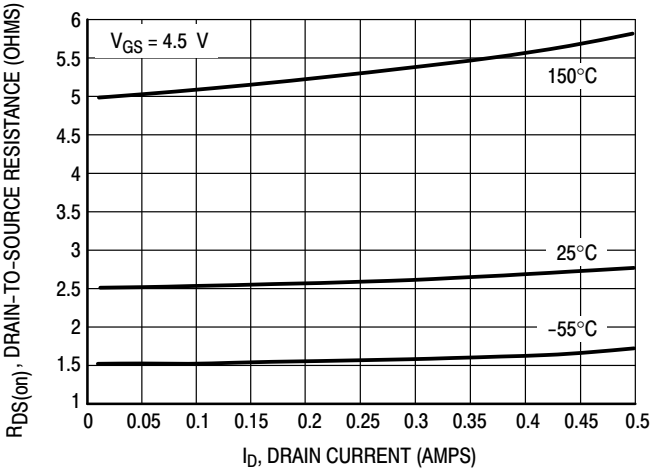


Figure 9. On−Resistance versus Drain Current

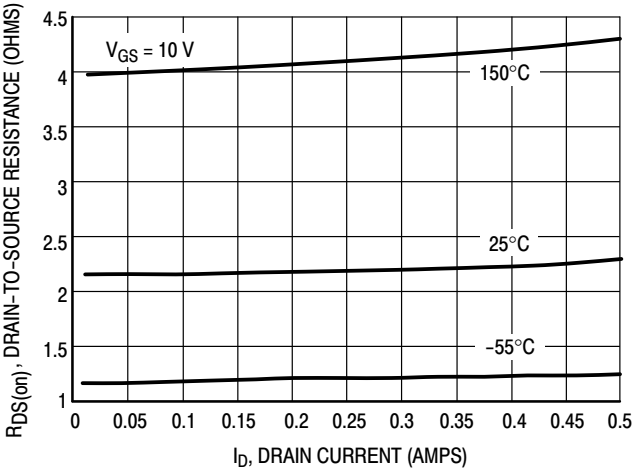


Figure 10. On−Resistance versus Drain Current

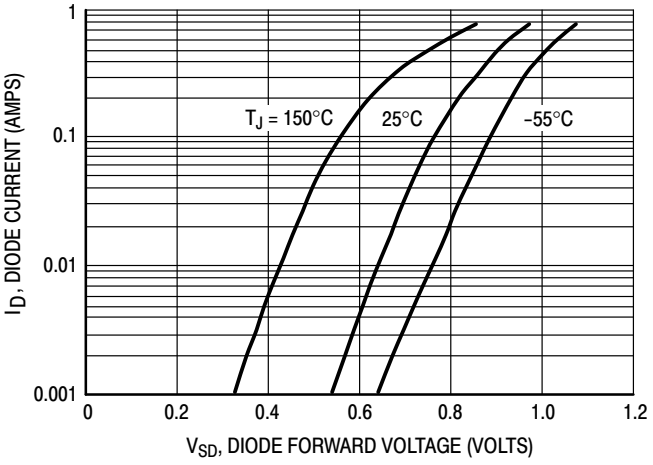


Figure 11. Body Diode Forward Voltage

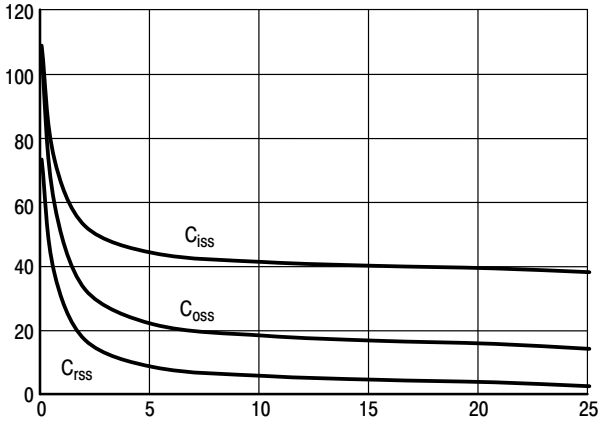
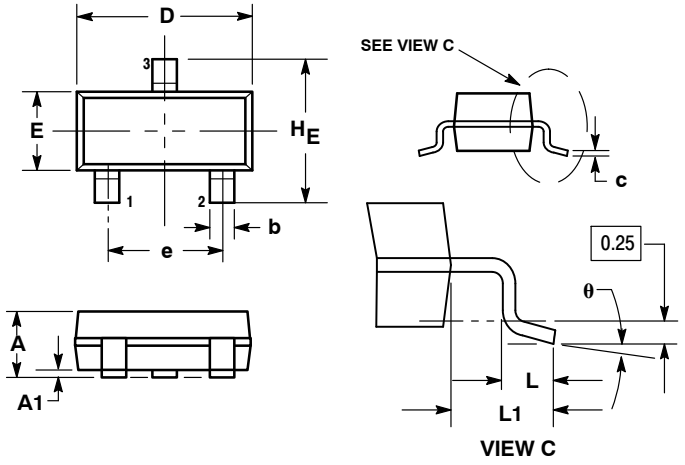


Figure 12. Capacitance

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

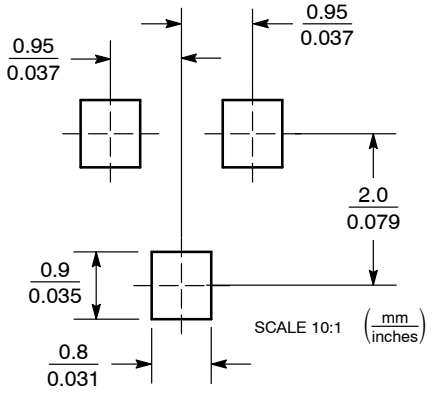


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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