THVD14x9 3.3-V to 5-V RS-485 Transceivers With Surge Protection

1 Features

- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- 3 V to 5.5 V Supply Voltage
- Bus I/O Protection
  - ± 16 kV HBM ESD
  - ± 8 kV IEC 61000-4-2 Contact Discharge
  - ± 15 kV IEC 61000-4-2 Air-Gap Discharge
  - ± 4 kV IEC 61000-4-4 Electrical Fast Transient
  - ± 3 kV IEC 61000-4-5 1.2/50-µs Surge
- Available in Two Speed Grades
  - THVD1419: 250 kbps
  - THVD1429: 20 Mbps
- Extended Ambient Temperature Range: -40°C to 125°C
- Extended Operational Common-Mode Range: ± 12 V
- Receiver Hysteresis for Noise Rejection: 30 mV
- Low Power Consumption
  - Standby Supply Current: < 1 µA
  - Current During Operation: < 3 mA
- Glitch-Free Power-Up/Down for Hot Plug-in Capability
- Open, Short, and Idle Bus Failsafe
- 1/8 Unit Load (Up to 256 Bus Nodes)
- Industry Standard 8-Pin SOIC for Drop-in Compatibility

2 Applications

- Building Automation
- HVAC Systems
- Factory Automation & Control
- Grid Infrastructure
- Smart Meters
- Process Analytics
- Video Surveillance

3 Description

THVD1419 and THVD1429 are half-duplex RS-485 transceivers with integrated surge protection. Surge protection is achieved by integrating transient voltage suppressor (TVS) diodes in the standard 8-pin SOIC (D) package. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable, eliminating the need for external protection components.

Each of these devices operates from a single 3.3 V or 5 V supply. The devices in this family feature a wide common-mode voltage range which makes them suitable for multi-point applications over long cable runs.

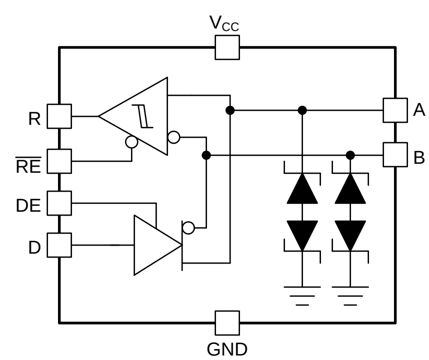
The THVD1419 and THVD1429 devices are available in the industry standard SOIC package for easy drop-in without any PCB changes. These devices are characterized over ambient free-air temperatures from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THVD1419 THVD1429	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available devices, see the orderable addendum at the end of the data sheet.

THVD1419 and THVD1429 Block Diagram



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4 Revision History

DATE	REVISION	NOTES
November 2018	*	Initial release.

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5 Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1419	Half	DE, $\overline{RE}$	up to 250 kbps	256
THVD1429			up to 20 Mbps	

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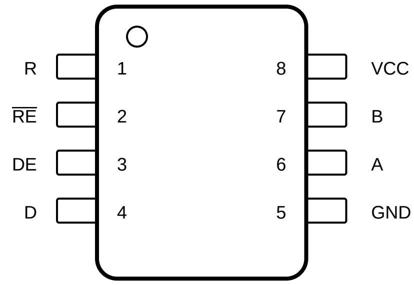
6 Pin Configuration and Functions

THVD1419, THVD1429 Devices
8-Pin D Package (SOIC)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	5	Ground	Device ground
R	1	Digital output	Receive data output
V_{CC}	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	V_{CC}	-0.5	7	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-15	15	V
Input voltage	Range at any logic pin (D, DE, or /RE)	-0.3	5.7	V
Receiver output current	I_O	-24	24	mA
Storage temperature range		-65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, 2010	Bus terminals and GND	±16	kV
			All other pins	±8	kV
		Charged device model (CDM), per JEDEC JESD22-C101E	All pins	±1.5	kV
		Machine model (MM), per JEDEC JESD22-A115-A	All pins	±200	V

7.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact Discharge, per IEC 61000-4-2	Bus pins and GND	±8	kV
		Air-Gap Discharge, per IEC 61000-4-2	Bus pins and GND	±15	kV
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus pins and GND	±4	kV
$V_{(surge)}$	Surge	Per IEC 61000-4-5, 1.2/50 μs	Bus pins and GND	±3	kV

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7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode) [1]	-12		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	-12		12	V
I_O	Output current, driver	-60		60	mA
I_{OR}	Output current, receiver	-8		8	mA
R_L	Differential load resistance	54			Ω
$1/t_{UI}$	Signaling rate: THVD1419			250	kbps
$1/t_{UI}$	Signaling rate: THVD1429			20	Mbps
T_A	Operating ambient temperature	-40		125	℃
T_J	Junction temperature	-40		150	℃

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.5 Thermal Information

THERMAL METRIC[1]		THVD14x9 D (SOIC) 8-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.6 Power Dissipation

PARAMETER	Description	TEST CONDITIONS	VALUE	UNIT
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 ^{0}C, 50% duty cycle square wave at maximum signaling rate, THVD1419	Unterminated: R_L = 300 Ω, C_L = 50 pF	210	mW
		RS-422 load: R_L = 100 Ω, C_L = 50 pF	220	mW
		RS-485 load: R_L = 54 Ω, C_L = 50 pF	250	mW
	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 ^{0}C, 50% duty cycle square wave at maximum signaling rate, THVD1429	Unterminated: R_L = 300 Ω, C_L = 50 pF	360	mW
		RS-422 load: R_L = 100 Ω, C_L = 50 pF	320	mW
		RS-485 load: R_L = 54 Ω, C_L = 50 pF	330	mW

7.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -12 V ≤ V_{test} ≤ 12 V, see Figure 1		1.5	3.5		V
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -12 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5V, see Figure 1		2.1			V
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 100 Ω, see Figure 2		2	4		V
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 54 Ω, see Figure 2		1.5	3.5		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω, see Figure 2		-200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC} / 2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -7 V ≤ V_O ≤ 12 V		-250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		50	125	µA
			V_I = -7 V	-100	-65		µA
			V_I = -12 V	-150	-100		µA
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of ±12 V		See (1)	-100	-20	mV
V_{TH-}	Negative-going input threshold voltage			-200	-130	See (1)	mV
V_{HYS}	Input hysteresis				30		mV
V_{OH}	Output high voltage	I_{OH} = -8 mA		V_{CC} – 0.4	V_{CC} – 0.3		V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}		-1		1	µA
Logic							
I_{IN}	Input current (D, DE, $\overline{RE}$)	4.5 V ≤ V_{CC} ≤ 5.5 V		-6.2		6.2	µA
Device							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{CC}, No load		2.4	3	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2	2.5	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0V, No load		700	960	µA
		Driver and receiver disabled	$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1	µA
T_{SD}	Thermal shutdown temperature				170		℃

(1) Under any specific conditions, VIT+ is assured to be at least Vhys higher than VIT–.

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7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: THVD1419						
t_r, t_f	Differential output rise / fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 3	300	700	1200	ns
t_{PHL}, t_{PLH}	Propagation delay			450	650	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$				40	ns
t_{PHZ}, t_{PLZ}	Disable time			50	200	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V, see Figure 4 and Figure 5		300	600	ns
		$\overline{RE}$ = V_{CC}, see Figure 4 and Figure 5		4	11	µs
Receiver: THVD1419						
t_r, t_f	Output rise / fall time	C_L = 15 pF, see Figure 6		13	25	ns
t_{PHL}, t_{PLH}	Propagation delay			70	110	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time			45	60	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$,	Enable time	DE = V_{CC}, see Figure 7		20	115	ns
		DE = 0 V, see Figure 8		4	14	µs
Driver: THVD1429						
t_r, t_f	Differential output rise / fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 3	2	7	14	ns
t_{PHL}, t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$				3.5	ns
t_{PHZ}, t_{PLZ}	Disable time			15	25	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V, see Figure 4 and Figure 5		20	50	ns
		$\overline{RE}$ = V_{CC}, see Figure 4 and Figure 5		4	11	µs
Receiver: THVD1429						
t_r, t_f	Output rise / fall time	C_L = 15 pF, see Figure 6		2	6	ns
t_{PHL}, t_{PLH}	Propagation delay			25	40	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$				3.5	ns
t_{PHZ}, t_{PLZ}	Disable time			14	28	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$,	Enable time	DE = V_{CC}, see Figure 7		50	110	ns
		DE = 0 V, see Figure 8		4	14	µs

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8 Parameter Measurement Information

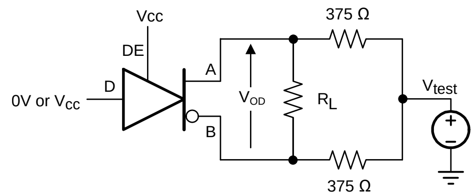

Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

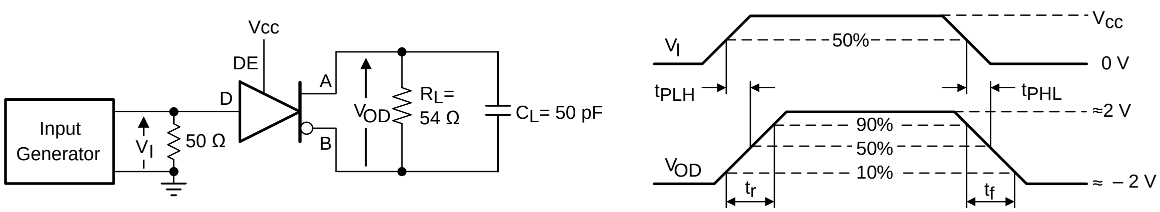

Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

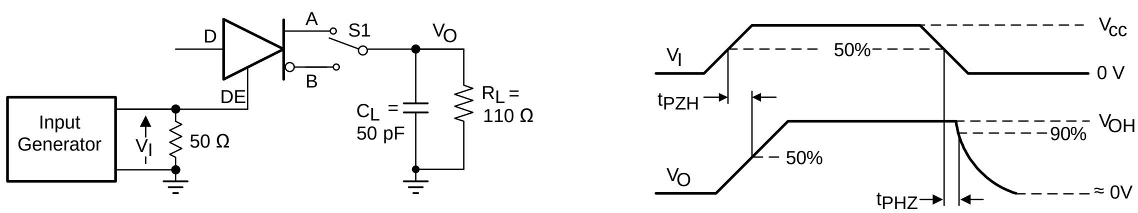

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

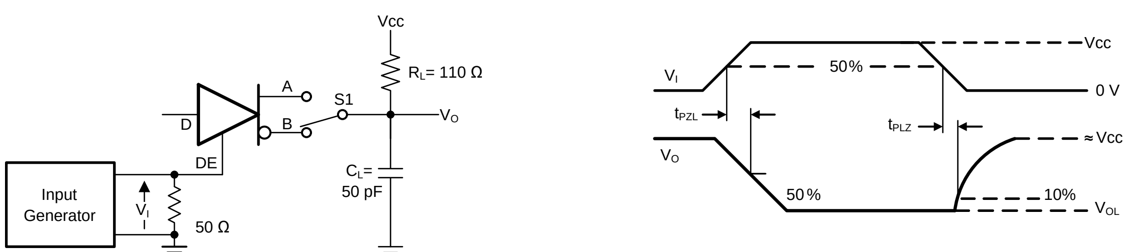

Figure 5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (continued)

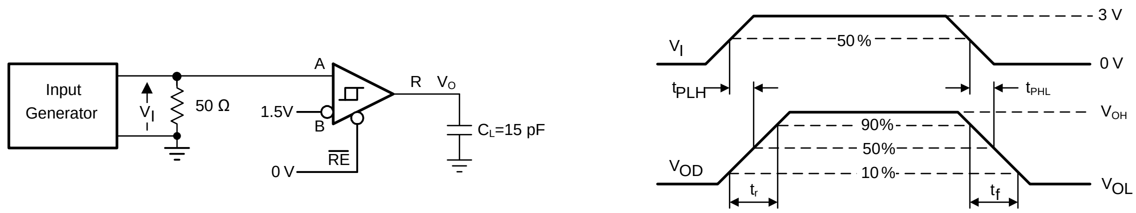

Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

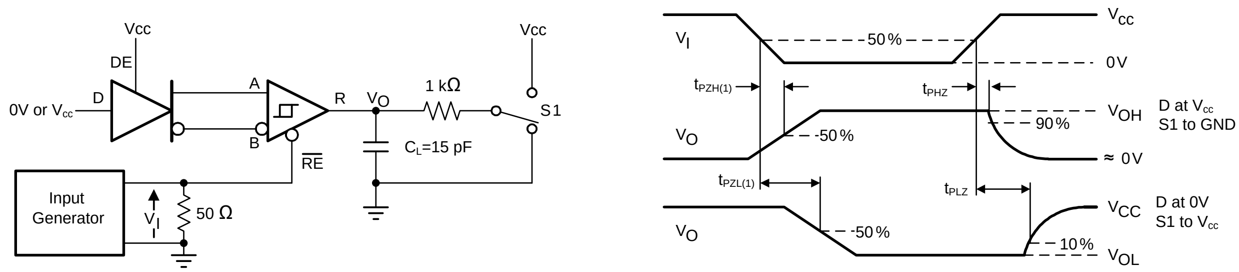

Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

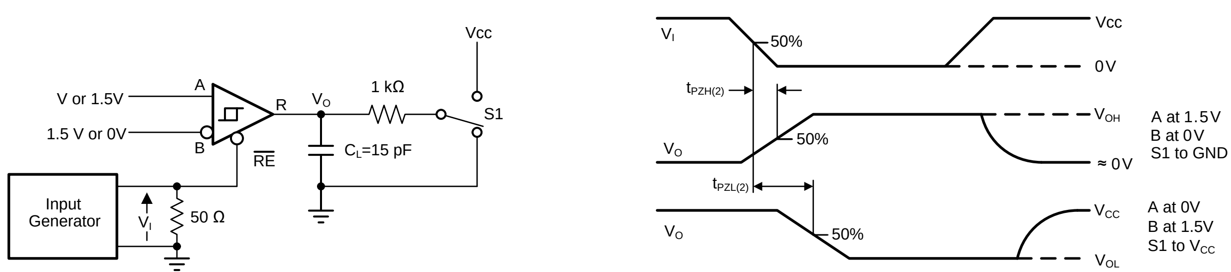

Figure 8. Measurement of Receiver Enable Times With Driver Disabled

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9 Detailed Description

9.1 Overview

THVD1419 and THVD1429 are surge-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 250 kbps and 20 Mbps respectively. Surge protection is achieved by integrating transient voltage suppresser (TVS) diodes in the standard 8-pin SOIC (D) package.

These devices have active-high driver enables and active-low receiver enables. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagrams

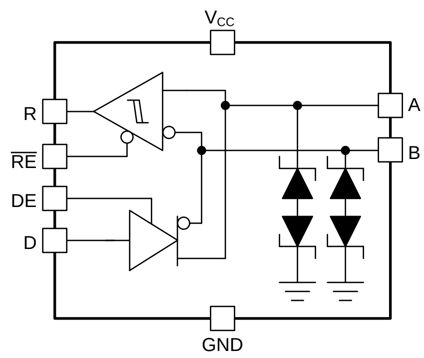

Figure 9. THVD1419 and THVD1429 Block Diagram

9.3 Feature Description

9.3.1 Electrostatic Discharge (ESD) Protection

The bus pins of the THVD14x9 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

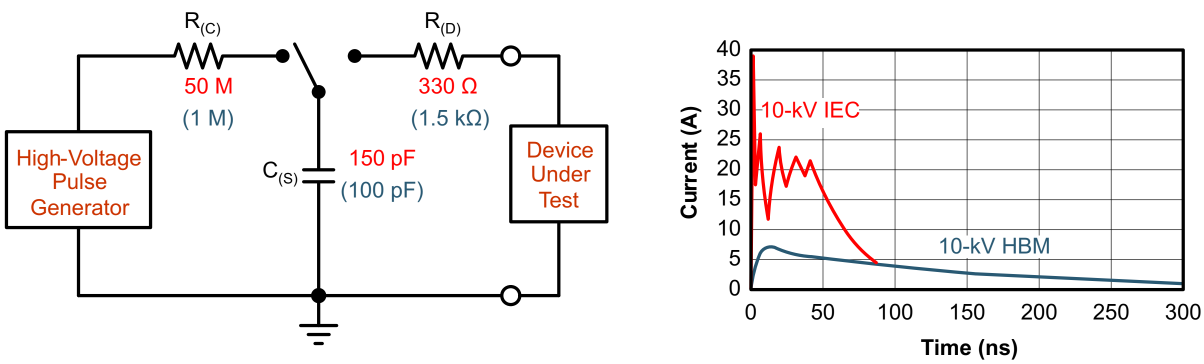

Figure 10. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables.

Feature Description (continued)

9.3.2 Electrical Fast Transient (EFT) Protection

Inductive loads such as relays, switch contactors, or heavy-duty motors can create high-frequency bursts during transition. The IEC 61000-4-4 test is intended to simulate the transients created by such switching of inductive loads on AC power lines. Figure 11 shows the voltage waveforms in to 50-Ω termination as defined by the IEC standard.

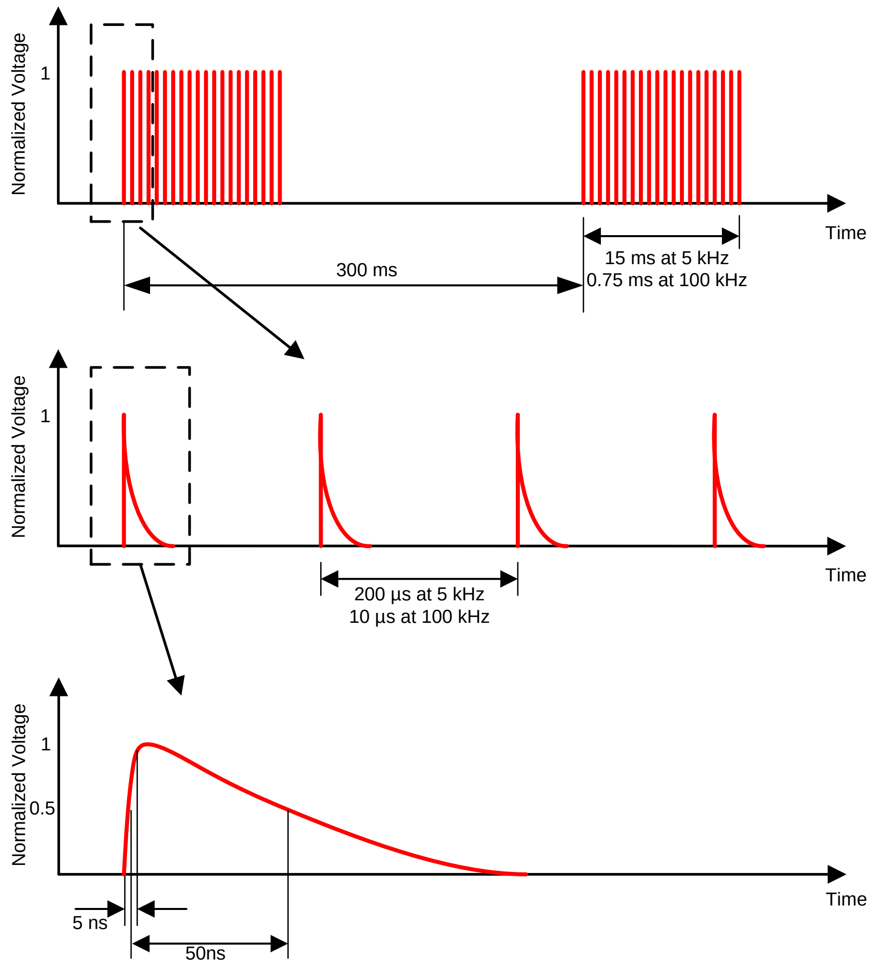

Figure 11. EFT Voltage Waveforms

Internal ESD protection circuits of the THVD14x9 protect the transceivers against EFT ±4 kV.

9.3.3 Surge Protection

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 12 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

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Feature Description (continued)

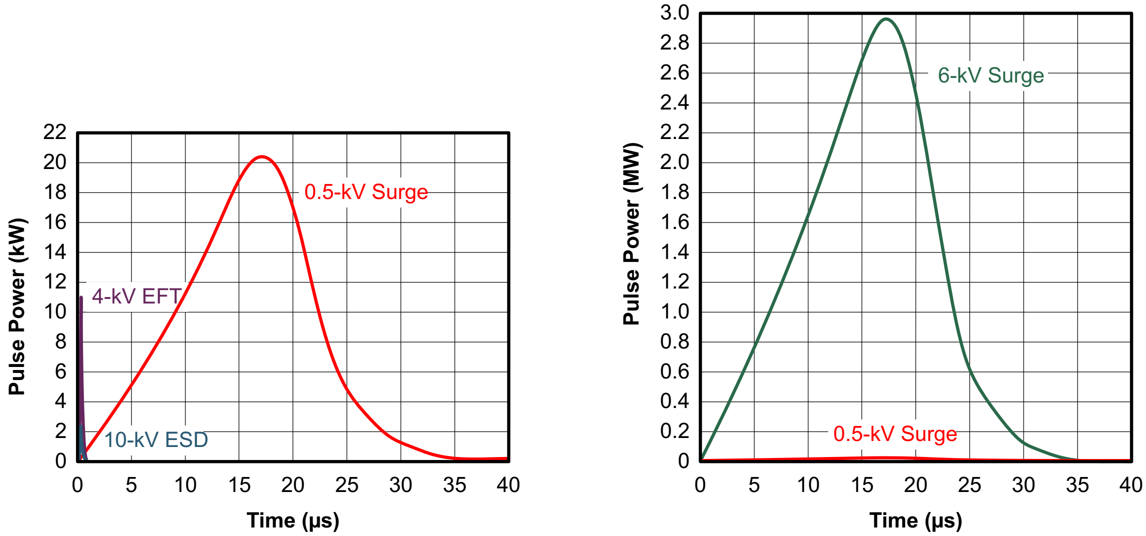

Figure 12. Power Comparison of ESD, EFT, and Surge Transients

Figure 13 shows the test setup used to validate THVD14x9 surge performance according to the IEC 61000-4-5 1.2/50-µs surge pulse.

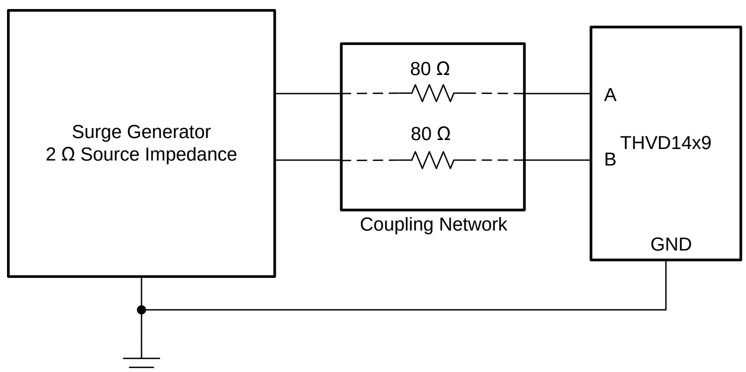

Figure 13. THVD14x9 Surge Test Setup

THVD14x9 product family is robust to ±3-kV surge transients without the need for any external components.

9.3.4 Failsafe Receiver

The differential receivers of the THVD14x9 family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

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9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

THVD14x9 are half-duplex RS-485 transceivers with integrated system-level surge protection. Standard 8-pin SOIC (D) package allows drop-in replacement into existing systems and eliminate system-level protection components.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

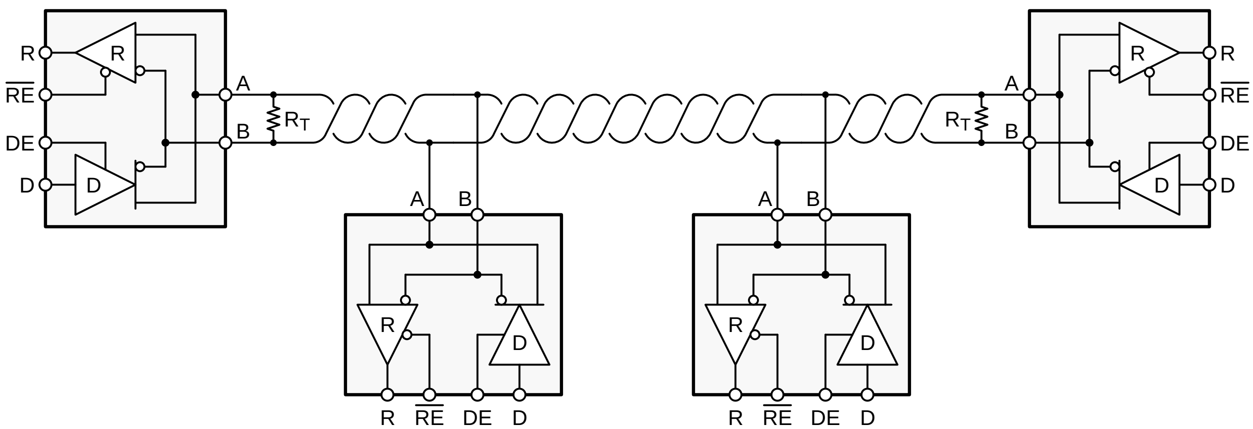

Figure 14. Typical RS-485 Network With Half-Duplex Transceivers

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

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Typical Application (continued)

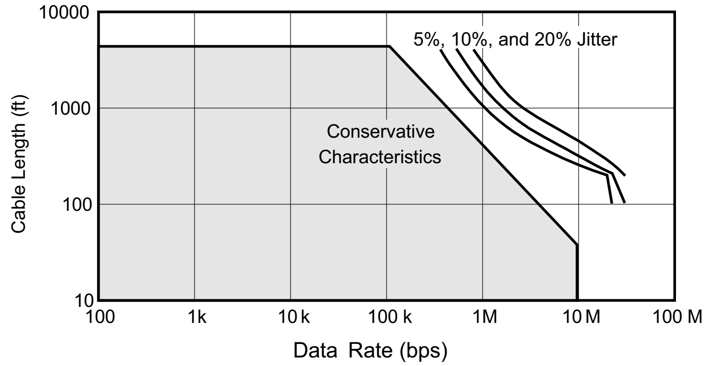

Figure 15. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 20 Mbps for the THVD1429) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD14x9 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

Typical Application (continued)

10.2.2 Detailed Design Procedure

RS-485 transceivers operate in noisy industrial environments typically require surge protection at the bus pins. Figure 16 compares 1-kV surge protection implementation with a regular RS-485 transceiver (such as THVD14x0) against with the THVD14x9. The internal TVS protection of the THVD14x9 achieves ±3 kV IEC 61000-4-5 surge protection without any additional external components, reducing system level bill of materials.

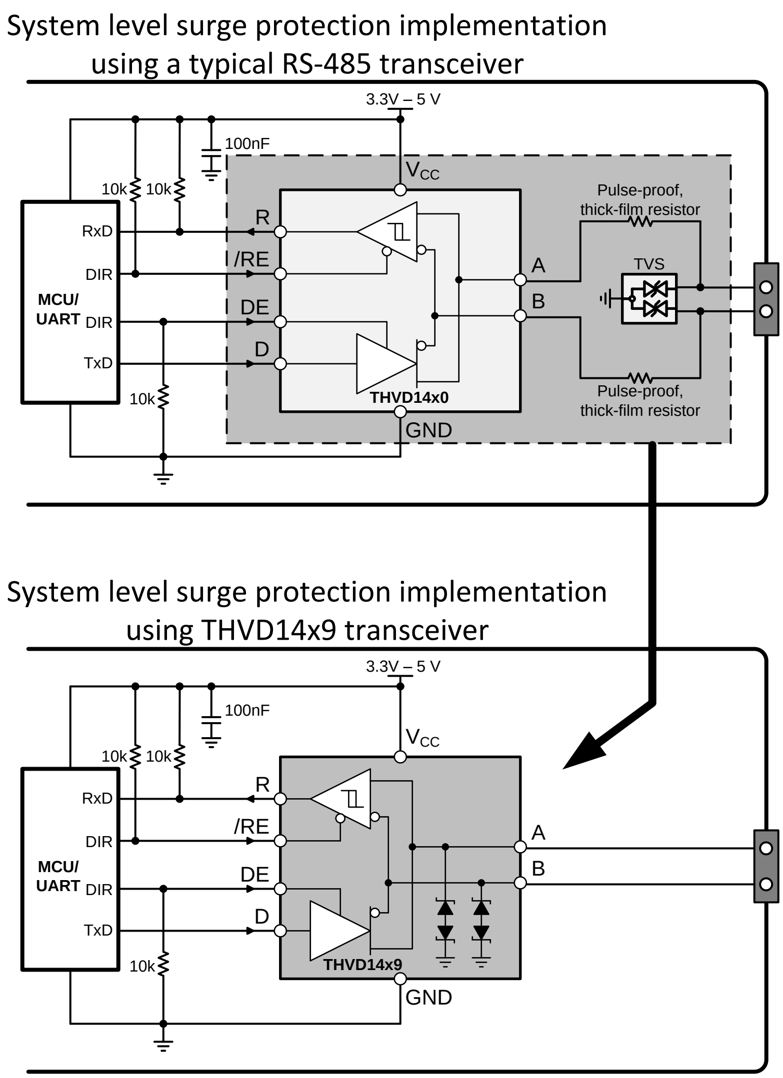

Figure 16. Implementation of System-Level Surge Protection Using THVD14x9

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

ADVANCE INFORMATION

12 Layout

12.1 Layout Guidelines

Additional external protection components generally are not needed when using THVD14x9 transceivers.

1. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
2. Use at least two vias for V_{CC} and ground connections of decoupling capacitors to minimize effective via-inductance.
3. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.

12.2 Layout Example

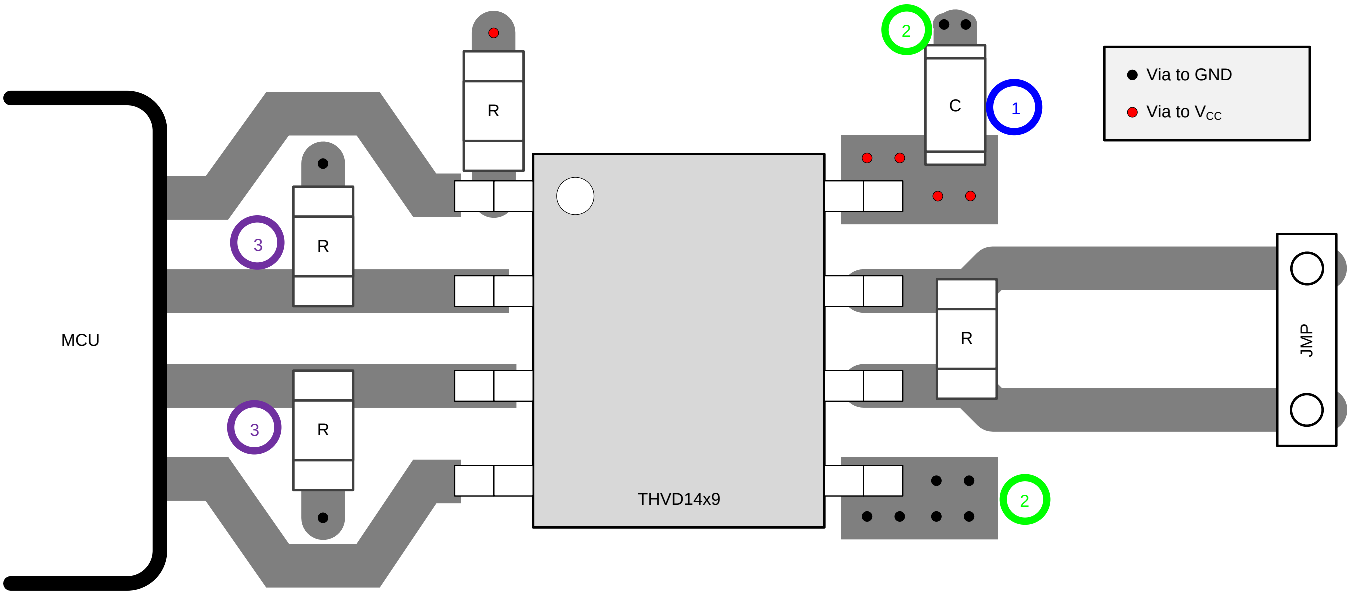

Figure 17. Half-Duplex Layout Example

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Device Support

13.2 Third-Party Products Disclaimer

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13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THVD1419	Click here	Click here	Click here	Click here	Click here
THVD1429	Click here	Click here	Click here	Click here	Click here

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document..

13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

E2E is a trademark of Texas Instruments.

13.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTHVD1419DR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
PTHVD1429DR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
THVD1419D	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		
THVD1419DR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
THVD1429D	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		
THVD1429DR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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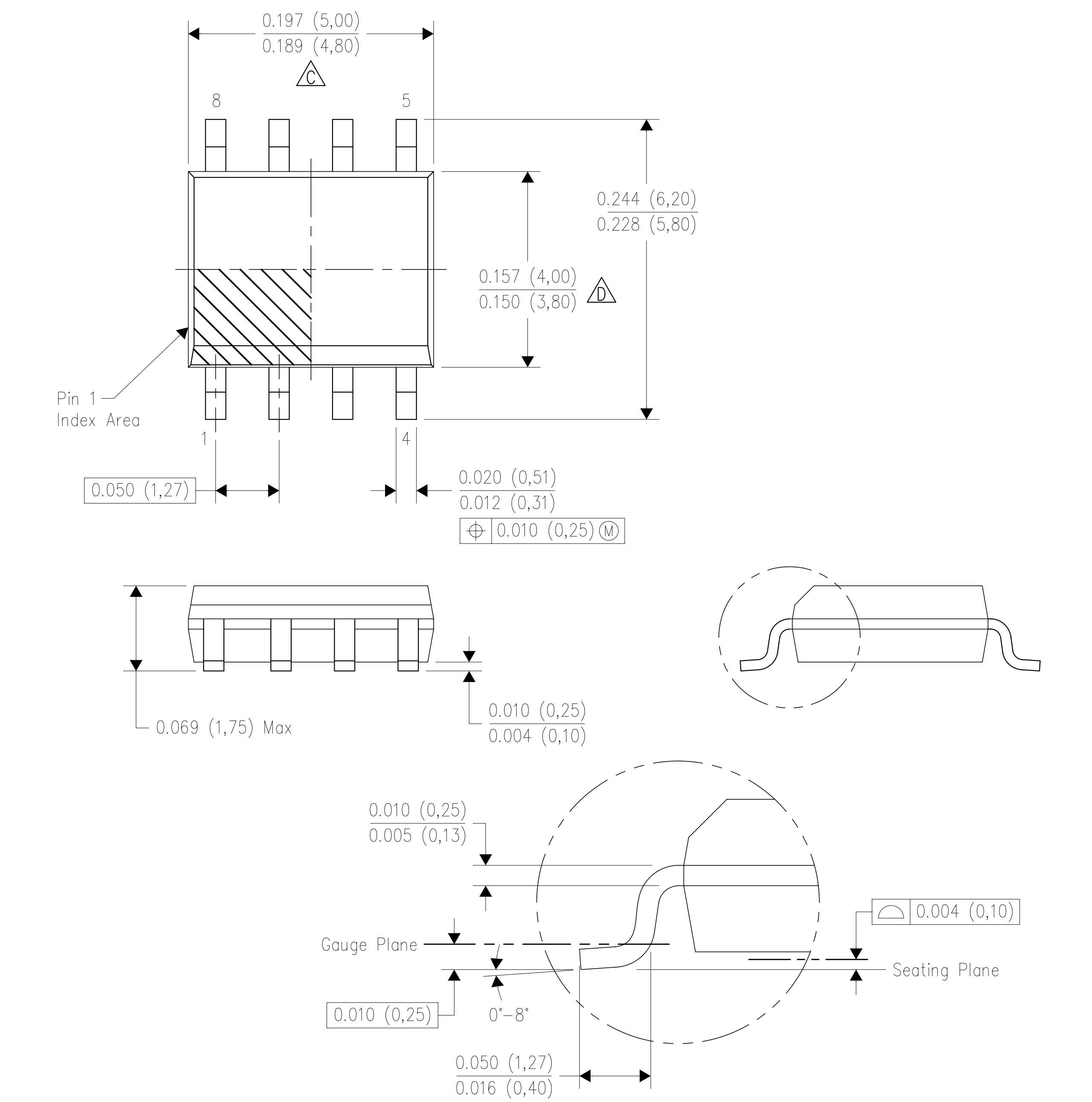
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



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NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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