

## 10-BIT 1.25-MSPS MICRO-POWER MINIATURE SAR ANALOG-TO-DIGITAL CONVERTER

Check for Samples: [ADS7887M](#)

### FEATURES

- 1.25-MHz Sample Rate Serial Device
- 10-Bit Resolution
- Zero Latency
- 25-MHz Serial Interface
- Supply Range: 2.35 V to 5.25 V
- Typical Power Dissipation at 1.25 MSPS:
  - 3.8 mW at 3-V  $V_{DD}$
  - 8 mW at 5-V  $V_{DD}$
- $\pm 0.35$  LSB INL, DNL
- 61-dB SINAD,  $-84$ -dB THD
- Unipolar Input Range: 0 V to  $V_{DD}$
- Power Down Current: 10  $\mu$ A Max
- Wide Input Bandwidth: 15 MHz at 3 dB
- 6-Pin SOT23 Package

### APPLICATIONS

- Base Band Converters in Radio Communication
- Motor Current/Bus Voltage Sensors in Digital Drives
- Optical Networking (DWDM, MEMS Based Switching)
- Optical Sensors
- Battery Powered Systems
- Medical Instrumentations
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

### DESCRIPTION

The ADS7887 is a 10-bit 1.25-MSPS analog-to-digital converter (ADC). The device includes a capacitor-based SAR A/D converter with inherent sample and hold. The serial interface is controlled by the  $\overline{CS}$  and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of  $\overline{CS}$ , and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power-saving powerdown feature for when the device is operated at lower conversion speeds.

The high level of the digital input to the device is not limited to device  $V_{DD}$ . This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuits with different supply levels. Also, this relaxes restriction on power-up sequencing.

The ADS7887 is available in a 6-pin SOT23 package and is specified for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



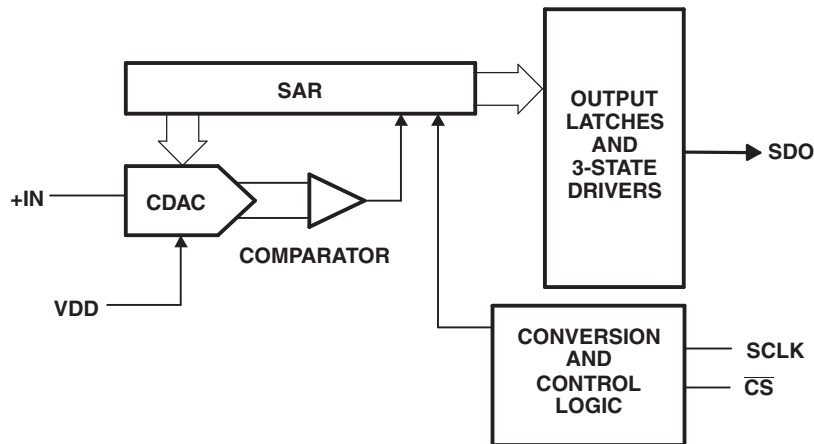
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOT-23 – DBV	Reel of 250	ADS7887MDBVT	BCNM

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

+IN to AGND	-0.3 V to +V <sub>DD</sub> +0.3 V	
+V <sub>DD</sub> to AGND	-0.3 V to 7.0 V	
Digital input voltage to GND	-0.3V to (7.0 V)	
Digital output to GND	-0.3 V to (+V <sub>DD</sub> + 0.3 V)	
Operating temperature range	-55°C to 125°C	
Storage temperature range	-65°C to 150°C	
Junction temperature (T <sub>J</sub> Max)	150°C	
Power dissipation	(T <sub>J</sub> Max – T <sub>A</sub> )/θ <sub>JA</sub>	
θ <sub>JA</sub> Thermal impedance <sup>(2)</sup>	295.2°C/W	
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

- (1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7, except for through-hole packages, which use a trace length of zero.

## ELECTRICAL SPECIFICATIONS

 $+V_{DD} = 2.35 \text{ V to } 5.25 \text{ V}$ ,  $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ ,  $f_{\text{sample}} = 1.25 \text{ MHz}$ 

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>					
Full-scale input voltage span <sup>(1)</sup>		0		$V_{DD}$	V
Absolute input voltage range	+IN	-0.20		$V_{DD}+0.20$	V
$C_i$ Input capacitance <sup>(2)</sup>			21		pF
$I_{ilk}$ Input leakage current	$T_A = 125^\circ\text{C}$		40		nA
<b>SYSTEM PERFORMANCE</b>					
Resolution			10		Bits
No missing codes		10			Bits
INL Integral nonlinearity		-1.2	$\pm 0.35$	1.2	LSB <sup>(3)</sup>
DNL Differential nonlinearity		-1 <sup>(4)</sup>	$\pm 0.35$	1.35	LSB
$E_O$ Offset error <sup>(5) (6) (7)</sup>		-2.5	$\pm 0.5$	2.5	LSB
$E_G$ Gain error <sup>(6)</sup>		-2	$\pm 0.5$	2	LSB
<b>SAMPLING DYNAMICS</b>					
Conversion time	25-MHz SCLK	530	560		ns
Acquisition time		260			ns
Maximum throughput rate	25-MHz SCLK			1.25	MHz
Aperture delay			5		ns
Step response			160		ns
Overvoltage recovery			160		ns
<b>DYNAMIC CHARACTERISTICS</b>					
THD Total harmonic distortion <sup>(8)</sup>	100 kHz		-84	-67	dB
SINAD Signal-to-noise and distortion	100 kHz	59	61		dB
SFDR Spurious free dynamic range	100 kHz	70	81		dB
Full power bandwidth	At -3 dB		15		MHz
<b>DIGITAL INPUT/OUTPUT</b>					
Logic family — CMOS					
$V_{IH}$ High-level input voltage	$V_{DD} = 2.35 \text{ V to } 5.25 \text{ V}$	$V_{DD} - 0.4$		5.25	V
$V_{IL}$ Low-level input voltage	$V_{DD} = 5 \text{ V}$			0.8	V
	$V_{DD} = 3 \text{ V}$			0.4	
$V_{OH}$ High-level output voltage	At $I_{\text{source}} = 200 \mu\text{A}$	$V_{DD}-0.2$			V
$V_{OL}$ Low-level output voltage	At $I_{\text{sink}} = 200 \mu\text{A}$			0.4	
<b>POWER SUPPLY REQUIREMENTS</b>					
$+V_{DD}$ Supply voltage		2.35	3.3	5.25	V
Supply current (normal mode)	At $V_{DD} = 2.35 \text{ V to } 5.25 \text{ V}$ , 1.25-MHz throughput			2	mA
	At $V_{DD} = 2.35 \text{ V to } 5.25 \text{ V}$ , static state			1.5	
Power-down state supply current	SCLK off			10	$\mu\text{A}$
	SCLK on (25 MHz)			200	
Power dissipation at 1.25 MHz throughput	$V_{DD} = 5 \text{ V}$		8	10	mW
	$V_{DD} = 3 \text{ V}$		3.8	6	

- (1) Ideal input span; does not include gain or offset error.
- (2) Refer [Figure 21](#) for details on sampling circuit
- (3) LSB means least significant bit
- (4) Exclusive
- (5) Measured relative to an ideal full-scale input
- (6) Offset error and gain error ensured by characterization.
- (7) First transition of 000H to 001H at  $0.5 \times (V_{\text{ref}}/2^{10})$
- (8) Calculated on the first nine harmonics of the input frequency

**ELECTRICAL SPECIFICATIONS (continued)**

+V<sub>DD</sub> = 2.35 V to 5.25 V, T<sub>A</sub> = -55°C to 125°C, f<sub>sample</sub> = 1.25 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation in static state	V <sub>DD</sub> = 5 V		5.5	7.5	mW
	V <sub>DD</sub> = 3 V		3	4.5	
Power down time				0.1	μs
Power up time				0.8	μs
Invalid conversions after power up				1	
<b>TEMPERATURE RANGE</b>					
Specified performance		-55		125	°C

**TIMING REQUIREMENTS (see Figure 1)**

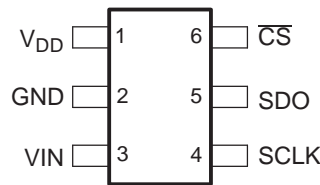
All specifications typical at T<sub>A</sub> = -55°C to 125°C, V<sub>DD</sub> = 2.35 V to 5.25 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
t <sub>conv</sub> Conversion time	V <sub>DD</sub> = 3 V			14 × t <sub>SCLK</sub>	ns
	V <sub>DD</sub> = 5 V			14 × t <sub>SCLK</sub>	
t <sub>q</sub> Minimum quiet time needed from bus 3-state to start of next conversion	V <sub>DD</sub> = 3 V	40			ns
	V <sub>DD</sub> = 5 V	40			
t <sub>d1</sub> Delay time, $\overline{CS}$ low to first data (0) out	V <sub>DD</sub> = 3 V		15	25	ns
	V <sub>DD</sub> = 5 V		13	25	
t <sub>su1</sub> Setup time, $\overline{CS}$ low to SCLK low	V <sub>DD</sub> = 3 V	10			ns
	V <sub>DD</sub> = 5 V	10			
t <sub>d2</sub> Delay time, SCLK falling to SDO	V <sub>DD</sub> = 3 V		15	25	ns
	V <sub>DD</sub> = 5 V		13	25	
t <sub>h1</sub> Hold time, SCLK falling to data valid <sup>(2)</sup>	V <sub>DD</sub> < 3 V	7			ns
	V <sub>DD</sub> > 5 V	5.5			
t <sub>d3</sub> Delay time, 16th SCLK falling edge to SDO 3-state	V <sub>DD</sub> = 3 V		10	25	ns
	V <sub>DD</sub> = 5 V		8	20	
t <sub>w1</sub> Pulse duration, $\overline{CS}$	V <sub>DD</sub> = 3 V	25	40		ns
	V <sub>DD</sub> = 5 V	25	40		
t <sub>d4</sub> Delay time, $\overline{CS}$ high to SDO 3-state	V <sub>DD</sub> = 3 V		17	30	ns
	V <sub>DD</sub> = 5 V		15	25	
t <sub>wH</sub> Pulse duration, SCLK high	V <sub>DD</sub> = 3 V	0.4 × t <sub>SCLK</sub>			ns
	V <sub>DD</sub> = 5 V	0.4 × t <sub>SCLK</sub>			
t <sub>wL</sub> Pulse duration, SCLK low	V <sub>DD</sub> = 3 V	0.4 × t <sub>SCLK</sub>			ns
	V <sub>DD</sub> = 5 V	0.4 × t <sub>SCLK</sub>			
Frequency, SCLK	V <sub>DD</sub> = 3 V			25	MHz
	V <sub>DD</sub> = 5 V			25	
t <sub>d5</sub> Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use minimum specification to avoid accidentally entering powerdown) <a href="#">Figure 2</a>	V <sub>DD</sub> = 3 V	-2		5	ns
	V <sub>DD</sub> = 5 V	-2		5	
t <sub>d6</sub> Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in powerdown (use maximum specification to avoid accidentally entering powerdown) <a href="#">Figure 2</a>	V <sub>DD</sub> = 3 V	2		-5	ns
	V <sub>DD</sub> = 5 V	2		-5	

(1) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.  
 (2) With 50-pf load.

DEVICE INFORMATION

SOT23 PACKAGE  
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V <sub>DD</sub>	1	–	Power supply input also acts like a reference voltage to ADC.
GND	2	–	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	I	Analog signal input
SCLK	4	I	Serial clock
SDO	5	O	Serial data out
$\overline{\text{CS}}$	6	I	Chip select signal, active low

NORMAL OPERATION

The cycle begins with the falling edge of  $\overline{\text{CS}}$ . This point is indicated as **a** in Figure 1. With the falling edge of  $\overline{\text{CS}}$ , the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 10-bit data in MSB first format and padded by 2 lagging zeros.

The falling edge of  $\overline{\text{CS}}$  clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. Data is padded with two lagging zeros as shown in Figure 1. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 14th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by **b** in Figure 1.

$\overline{\text{CS}}$  can be asserted (pulled high) after 16 clocks have elapsed. Do not start the next conversion by pulling  $\overline{\text{CS}}$  low until the end of the quiet time ( $t_q$ ) after SDO goes to 3-state. To continue normal operation, do not pull  $\overline{\text{CS}}$  high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.)  $\overline{\text{CS}}$  going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V<sub>DD</sub>. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels (V<sub>OH</sub> and V<sub>OL</sub>) are governed by V<sub>DD</sub> as listed in the SPECIFICATIONS table.

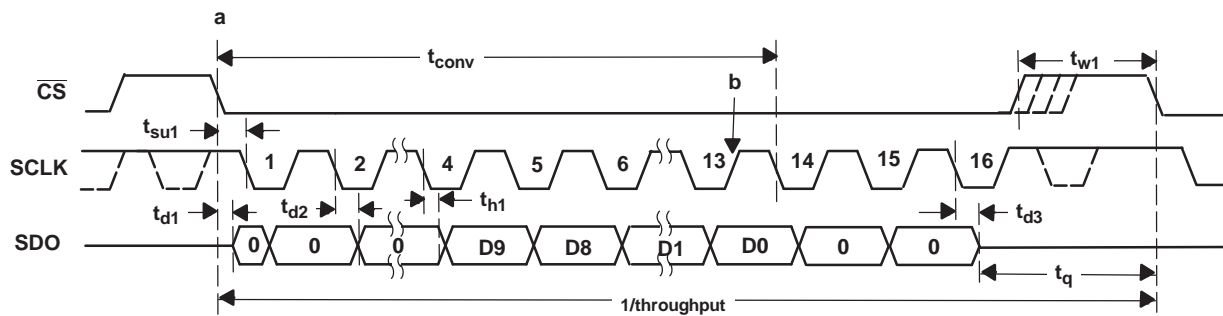


Figure 1. Interface Timing Diagram

### POWER-DOWN MODE

The device enters power down mode if  $\overline{CS}$  goes high anytime after the second SCLK falling edge to before the tenth SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power-down condition as shown in Figure 2.

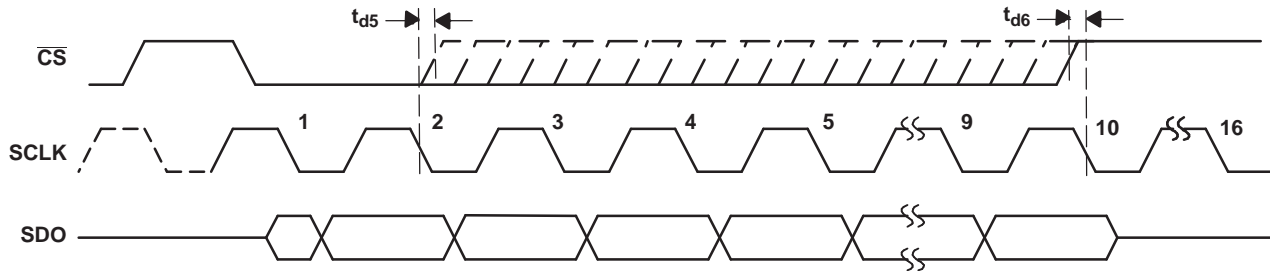


Figure 2. Entering Power Down Mode

A dummy cycle with  $\overline{CS}$  low for more than ten SCLK falling edges brings the device out of power-down mode. For the device to come to the fully powered up condition it takes 0.8  $\mu$ s.  $\overline{CS}$  can be pulled high any time after the 10th falling edge as shown in Figure 3. It is not necessary to continue until the 16th clock if the next conversion starts 0.8  $\mu$ s after  $\overline{CS}$  going low of the dummy cycle and the quiet time ( $t_q$ ) condition is met.

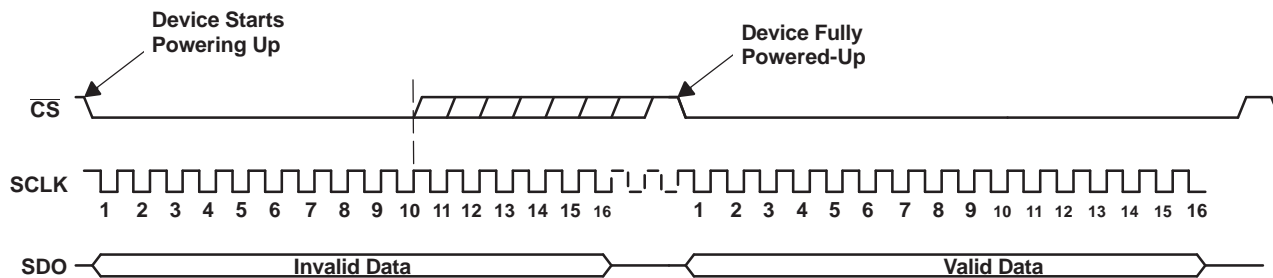


Figure 3. Exiting Power Down Mode

TYPICAL CHARACTERISTICS

SUPPLY CURRENT  
VS  
SUPPLY VOLTAGE

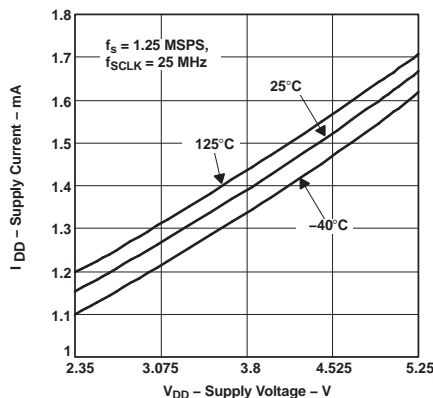


Figure 4.

SUPPLY CURRENT  
VS  
SCLK FREQUENCY

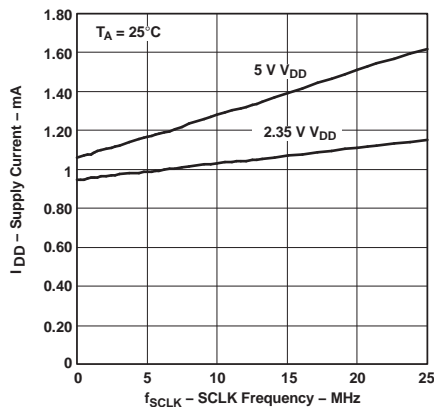


Figure 5.

SUPPLY CURRENT  
VS  
SAMPLE RATE

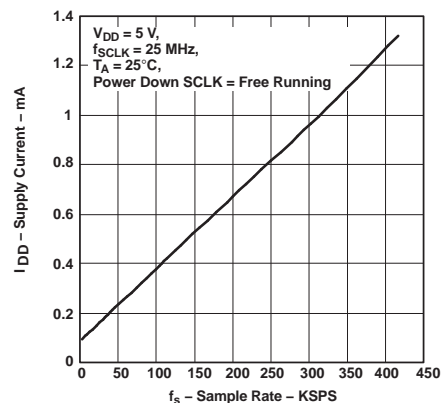


Figure 6.

ANALOG INPUT  
LEAKAGE CURRENT  
VS  
FREE-AIR TEMPERATURE

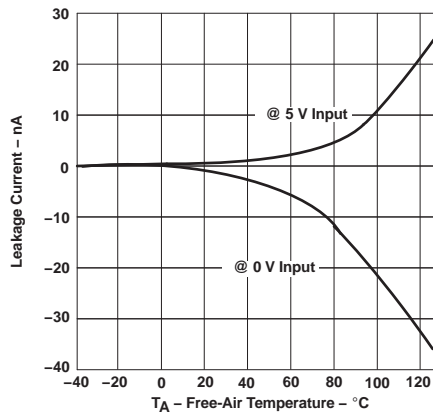


Figure 7.

SIGNAL-TO-NOISE  
AND DISTORTION  
VS  
INPUT FREQUENCY

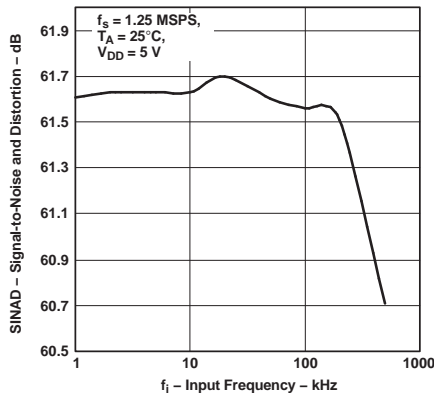


Figure 8.

SIGNAL-TO-NOISE  
AND DISTORTION  
VS  
SUPPLY VOLTAGE

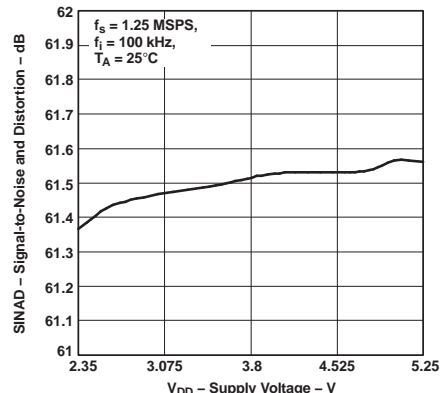


Figure 9.

TOTAL HARMONIC DISTORTION  
VS  
INPUT FREQUENCY

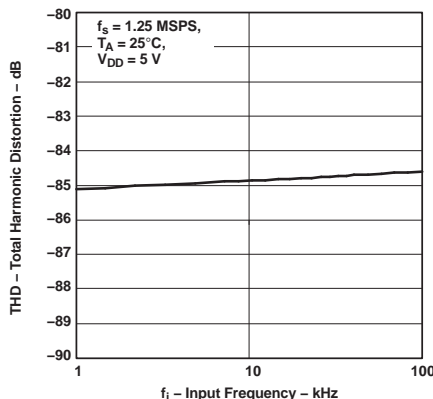


Figure 10.

TOTAL HARMONIC DISTORTION  
VS  
SUPPLY VOLTAGE

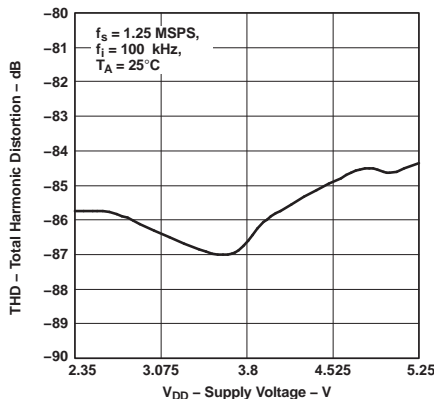


Figure 11.

SPURIOUS FREE DYNAMIC RANGE  
VS  
INPUT FREQUENCY

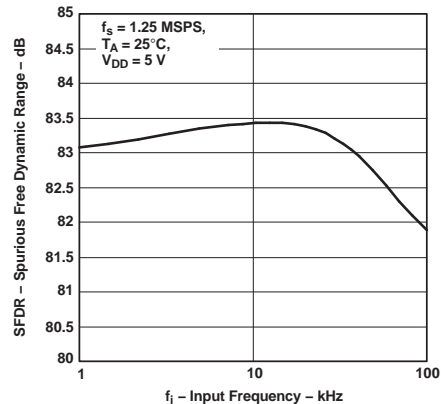


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

**SPURIOUS FREE DYNAMIC RANGE  
vs  
SUPPLY VOLTAGE**

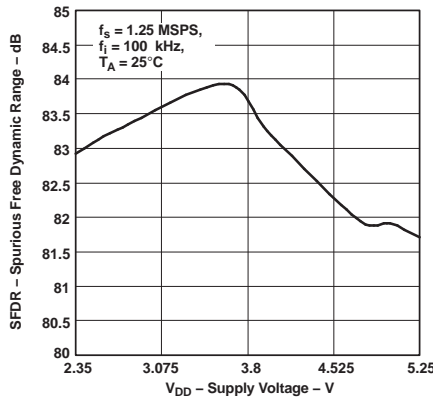


Figure 13.

**OFFSET ERROR  
vs  
SUPPLY VOLTAGE**

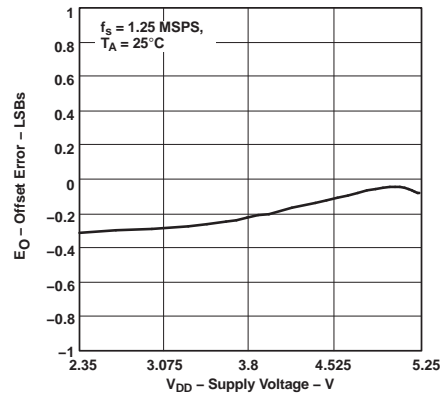


Figure 14.

**OFFSET ERROR  
vs  
FREE-AIR TEMPERATURE**

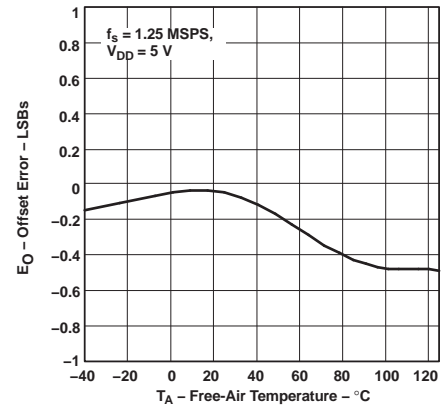


Figure 15.

**GAIN ERROR  
vs  
SUPPLY VOLTAGE**

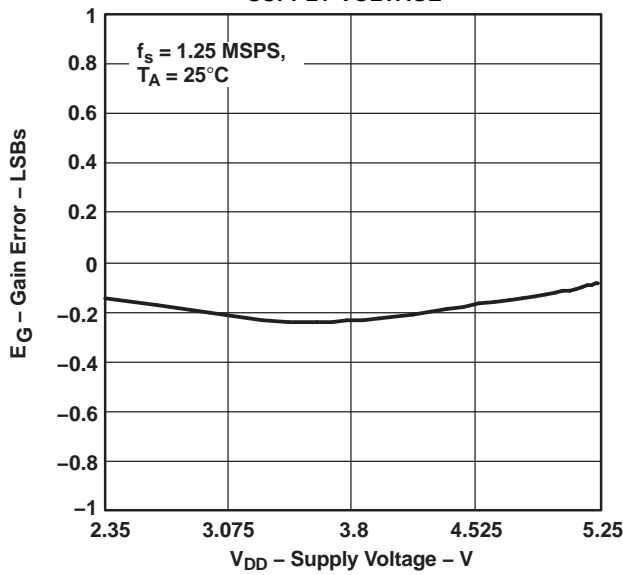


Figure 16.

**GAIN ERROR  
vs  
FREE-AIR TEMPERATURE**

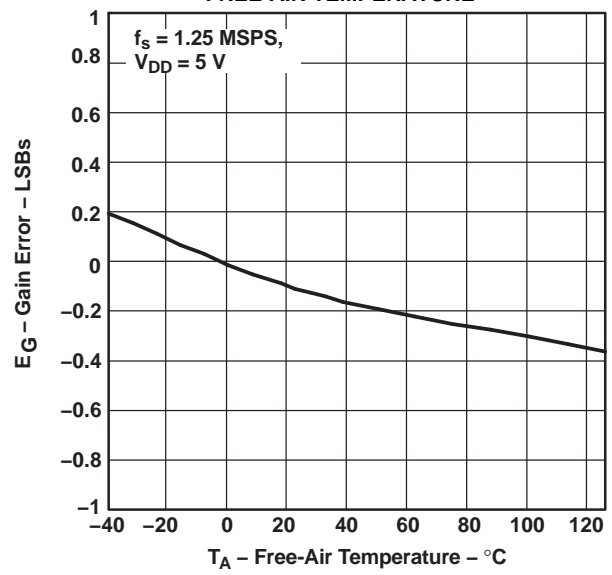


Figure 17.

TYPICAL CHARACTERISTICS (continued)

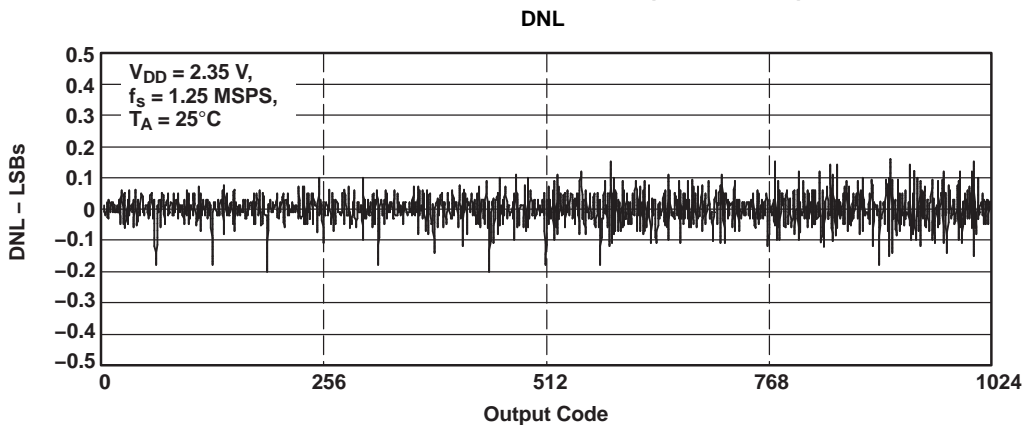


Figure 18.

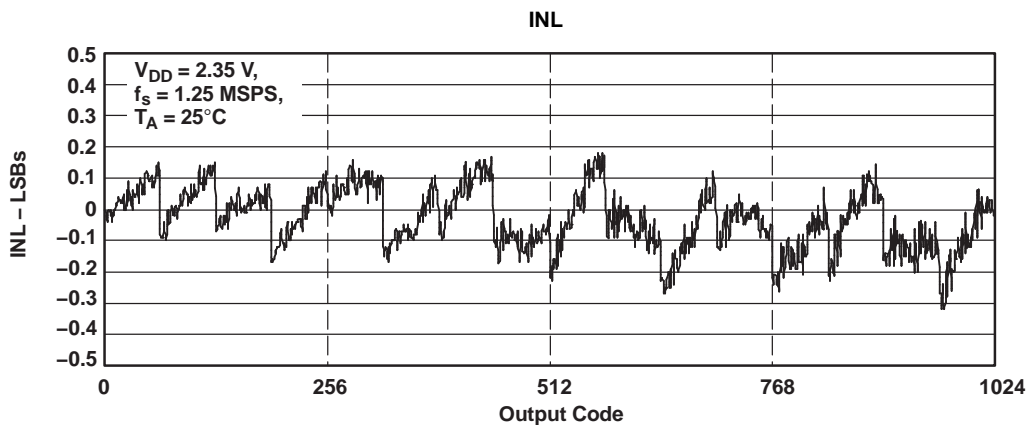


Figure 19.

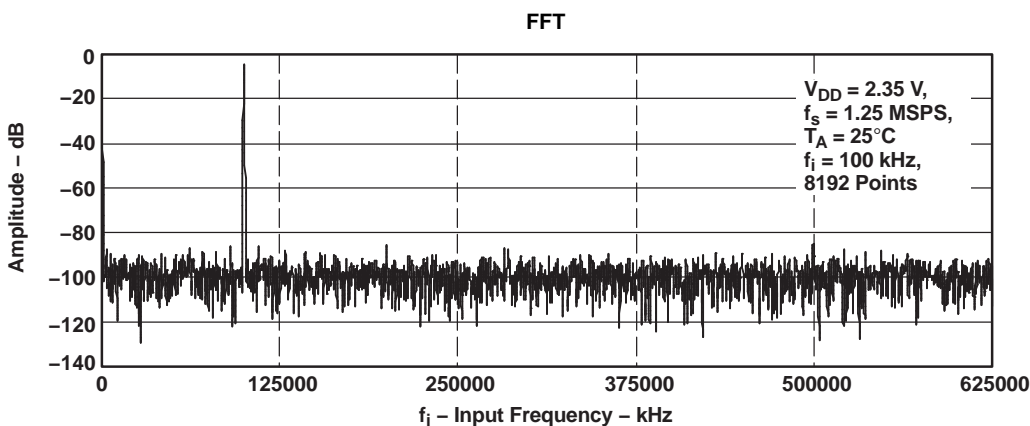
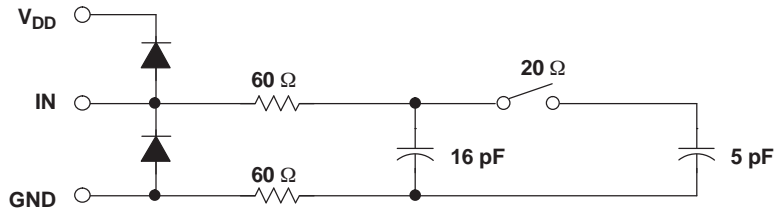


Figure 20.

**APPLICATION INFORMATION**



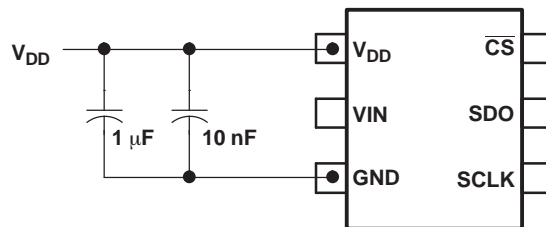
**Figure 21. Typical Equivalent Sampling Circuit**

**Driving the VIN and V<sub>DD</sub> Pins**

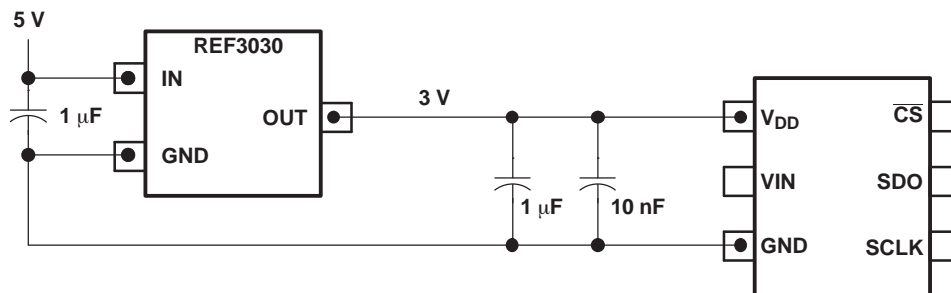
The VIN input to the ADS7887 should be driven with a low-impedance source. In most cases, additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer helps achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7887 A/D converter is derived internally from the supply voltage. The device offer limited low-pass filtering functionality on-chip. The supply to the converter should be driven with a low-impedance source and should be decoupled to ground. A 1-μF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide low-impedance traces should be used to connect the capacitor to the pins of the device. The ADS7887 draws very little current from the supply lines. The supply line can be driven:

- Directly from the system supply.
- From a reference output from a low-drift and low-dropout reference voltage generator like REF3030 or REF3130. The ADS7887 can operate off a wide range of supply voltages. The actual choice of the reference voltage generator depends upon the system. [Figure 23](#) shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer such as the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the V<sub>DD</sub> input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. [Figure 24](#) shows one possible application circuit.



**Figure 22. Supply/Reference Decoupling Capacitors**



**Figure 23. Using the REF3030 Reference**

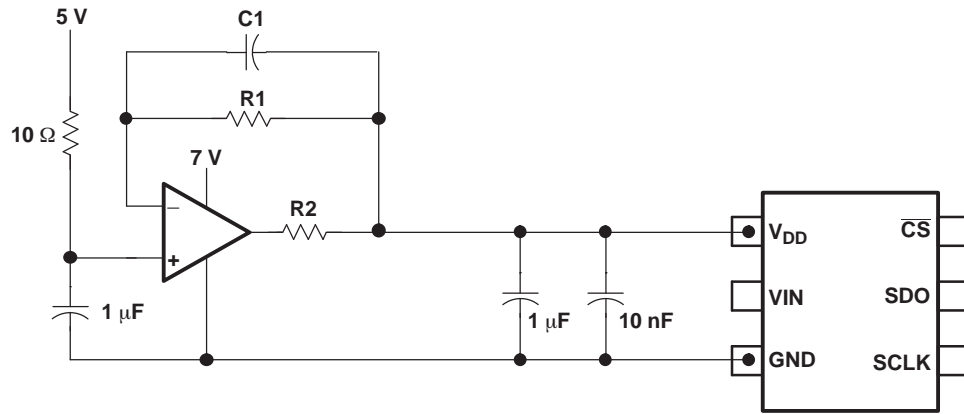


Figure 24. Buffering with the OPA735

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7887MDBVT	ACTIVE	SOT-23	DBV	6	250	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	-55 to 125	BCNM	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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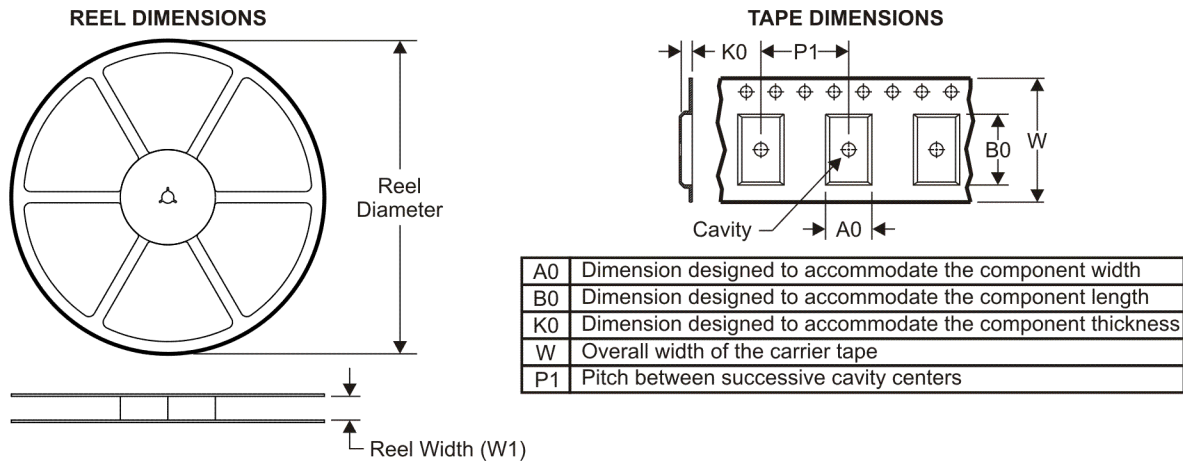
**OTHER QUALIFIED VERSIONS OF ADS7887M :**

- Catalog: [ADS7887](#)

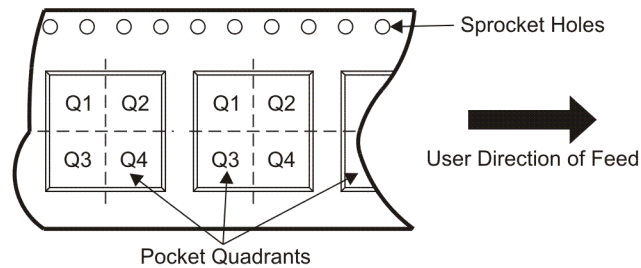
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



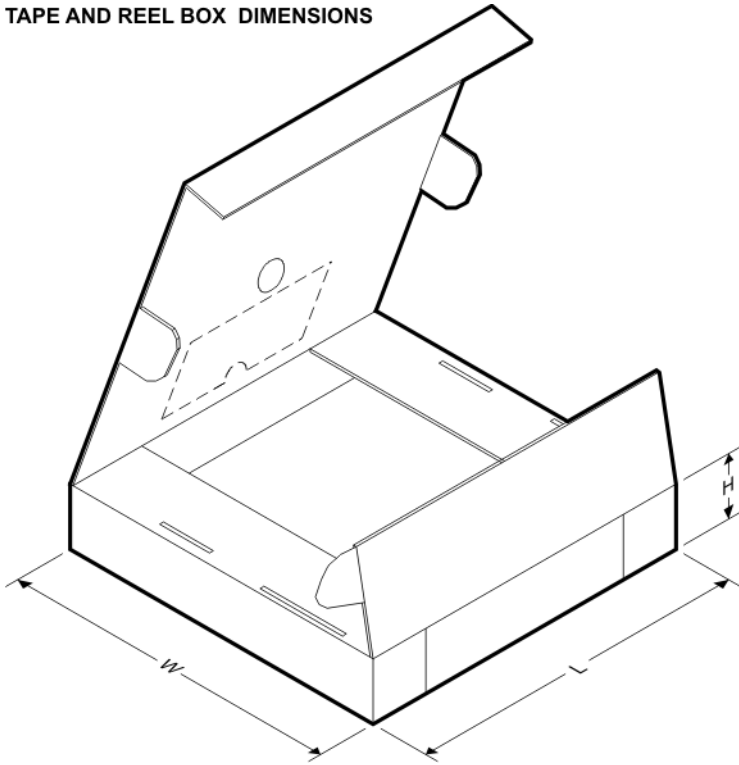
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7887MDBVT	SOT-23	DBV	6	250	177.8	9.7	3.2	3.1	1.39	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



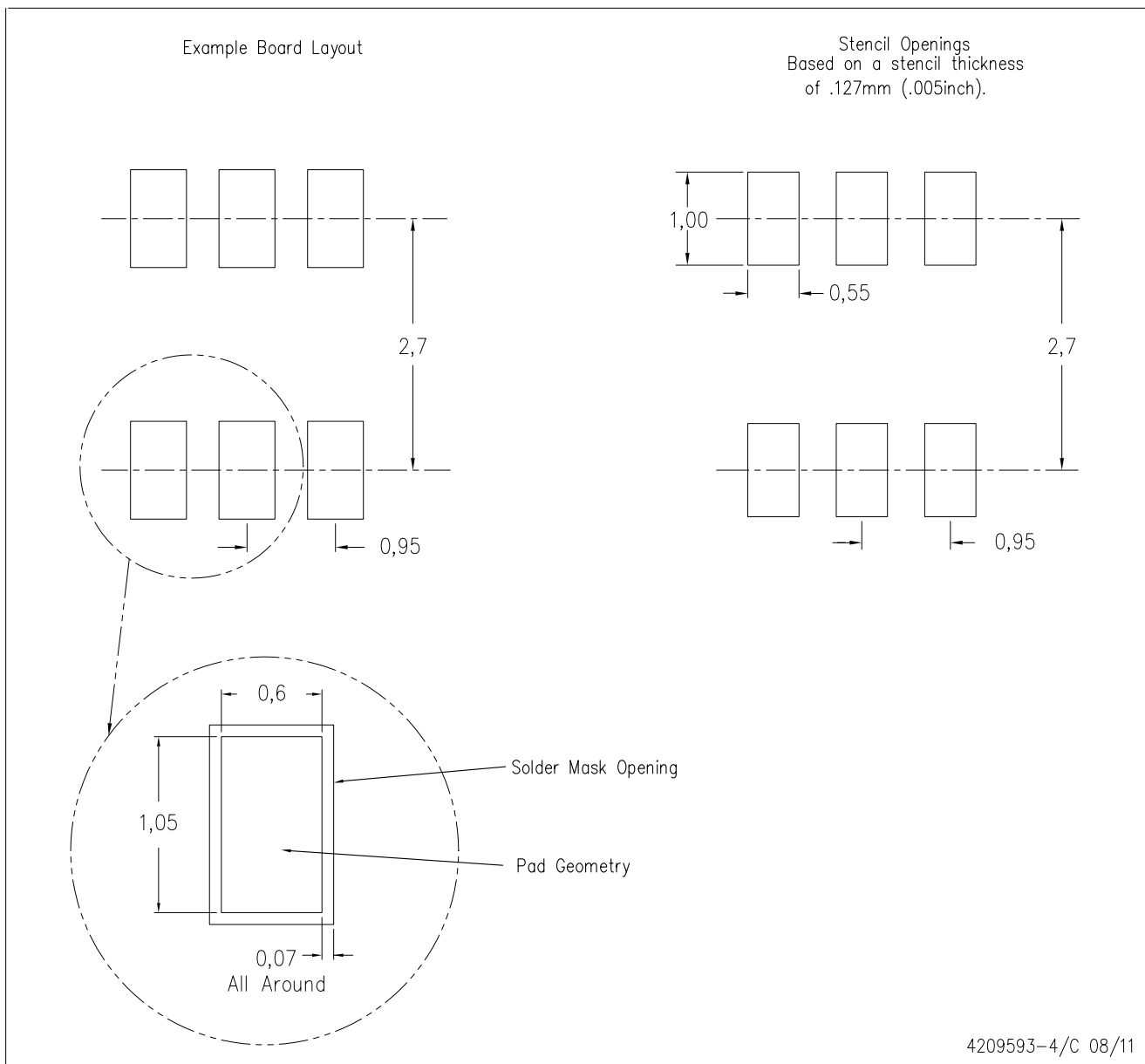
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7887MDBVT	SOT-23	DBV	6	250	184.0	184.0	50.0



DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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