TEXAS INSTRUMENTS

LMT01-SP

SNIS205 – JANUARY 2019

LMT01-SP radiation hardened 2-pin precision digital output temperature sensor

1 Features

- 5962R18211301VXC
  - Radiation Hardness Assured (RHA) to 100-krad(Si) Total Ionizing Dose (TID)
  - Single Event Latchup (SEL) immune to LET = 93 MeV-cm^2/mg
  - 2-lead HTA ceramic package
- 1.5°C accuracy over –50°C to 150°C wide temperature range and radiation
- Pulse count current loop easily read by processor
  - Number of output pulses is proportional to temperature with 0.0625°C resolution
- Communication frequency: 88 kHz
- Conversion current: 34 µA
- Continuous conversion plus data-transmission period: 100 ms
- Floating 2-V to 5.5-V (VP – VN) supply operation with integrated EMI immunity

2 Applications

- Thermistor signal chain upgrade
- Space analog temp sensor upgrade
- Space satellite telemetry
- High-speed signal chain monitoring
- Power supply monitoring
- Digital output wired probes

3 Description

The LMT01-SP device is a radiation hardened, high-accuracy, 2-pin temperature sensor with an easy-to-use pulse count current loop interface. The pulsed output is designed to easily interface directly with a comparator or GPIO input, thereby simplifying the hardware implementation. For space applications looking to minimize board area, the LMT01-SP is an ideal replacement for traditional thermistor signal chains and is inherently robust against single event effects. Integrated EMI suppression and a simple 2-pin architecture makes the device suitable for sensing in a noisy environment. The LMT01-SP can be mounted directly to a board or converted into a two-wire temperature probe with a wire length up to two meters. It can also be used to replace thermistors or analog temperature sensors in space applications with the added benefit of connecting directly to an MCU or FPGA without the need for amplifiers or ADCs for signal conditioning, reducing board space and power consumption.

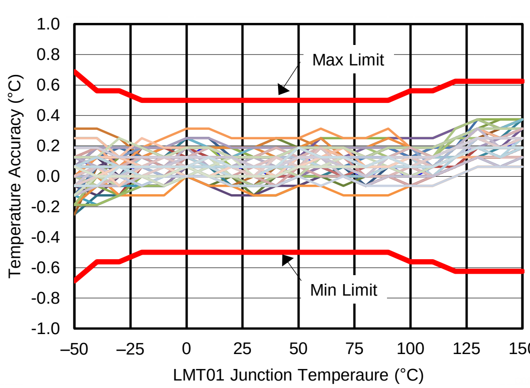
Device Information(1)

PART NUMBER	GRADE	PACKAGE
5962R18211301VXC	RHA - 100 krad(Si)	HTA (2) 5.57 mm × 3.00 mm
LMT01SPHTA/EM	Engineering Evaluation(2)	
PLMT01SPHTA/EM	Prototype Engineering Evaluation(2)	
LMT01CVAL-EVM	Evaluation Module(2)	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

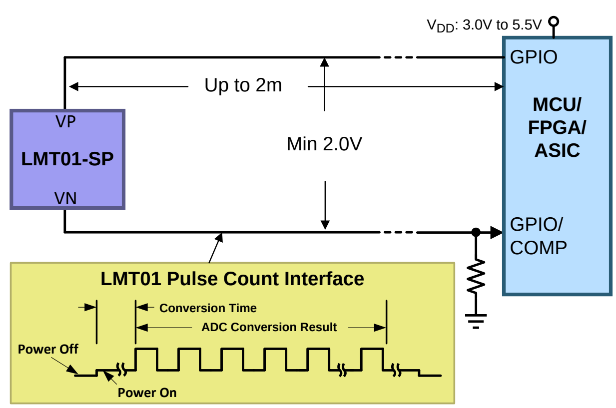
(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

LMT01-SP Accuracy



Typical units plotted in center of curve.

2-Pin IC Temperature Sensor



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2019	*	Initial release.

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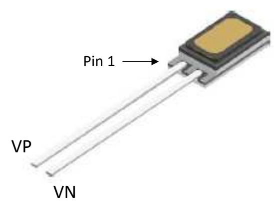
5 Pin Configuration and Functions

HTA Package
2-Pin CTO-92
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VP	1	Input	Positive voltage pin; may be connected to system power supply or bias resistor.
VN	2	Output	Negative voltage pin; may be connected to system ground or a bias resistor.
LID	—	Floating	The HTA package used for the LMT01-SP does not have an internal connection to the metal lid. If necessary, this lid can be connected to ground with no impact to device operation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1).

	MIN	MAX	UNIT
Voltage drop (VP – VN)	−0.3	6	V
Storage temperature, T_{stg}	−65	175	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Free-air temperature	−55	125	°C
Voltage drop (VP – VN)	2(1)	5.5	V

(1) During transmission of pulses at a high level.

6.4 Thermal Information

THERMAL METRIC(1)		LMT01-SP HTA (CTO-92) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Over operating free-air temperature range and operating VP-VN range (unless otherwise noted).

PARAMETER		SUBGROUPS	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY								
	Temperature accuracy[(1)(2)]	1, 2, 3	VP – VN of 2.15 V to 5.5 V	150°C		±0.4		°C
				125°C	–0.7	±0.3	1.5	
				120°C		±0.3		
				110°C		±0.3		
				100°C		±0.3		
				90°C		±0.125		
				25°C	–0.7	±0.125	1.5	
				–20°C		±0.125		
				–30°C		±0.3		
				–40°C		±0.4		
				–50°C	–0.7	±0.4	1.5	
				–55°C	–5		5	
PULSE COUNT TRANSFER FUNCTION								
	Number of pulses at 25°C	1			1195	1201	1207	
	Output pulse range				15		3228	
			Theoretical max (exceeds device rating)		1		4095	
	Resolution of one pulse					0.0625		°C
OUTPUT CURRENT								
I_{OL}	Output current variation	1, 2, 3	Low level		28	34	40	µA
I_{OH}			High level		112.5	125	143	µA
	High-to-low level output current ratio				3.1	3.7	4.5	
POWER SUPPLY								
	Accuracy sensitivity to change in VP – VN	1	2.15 V ≤ VP – VN ≤ 5 V[(3)]			40	133	m°C/V
	Leakage current VP – VN	1, 2, 3	VDD ≤ 0.4 V			0.002	3.5	µA
THERMAL RESPONSE								
	Still air thermal response time to 63% of final value (package only)					40		ms

(1) Calculated using Pulse Count to Temperature LUT and 0.0625°C resolution per pulse, see *Electrical Characteristics - Pulse Count to Temperature LUT* section.
(2) Error can be linearly interpolated between temperatures given in table as shown in the Accuracy vs Temperature curves in *Typical Characteristics* section.
(3) Limit is using end point calculation.

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6.6 Electrical Characteristics - Pulse Count to Temperature LUT

Over operating free-air temperature range and 2.15 V ≤ VP – VN ≤ 5 V power supply operating range (unless otherwise noted). LUT is short for Look-up Table.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	–50°C	15	26	37	
	–40°C	172	181	190	
	–30°C	329	338	347	
	–20°C	486	494	502	
	–10°C	643	651	659	
	0°C	800	808	816	
	10°C	958	966	974	
	20°C	1117	1125	1133	
	30°C	1276	1284	1292	
	40°C	1435	1443	1451	
Digital output code	50°C	1594	1602	1610	pulses
	60°C	1754	1762	1770	
	70°C	1915	1923	1931	
	80°C	2076	2084	2092	
	90°C	2237	2245	2253	
	100°C	2398	2407	2416	
	110°C	2560	2569	2578	
	120°C	2721	2731	2741	
	130°C	2883	2893	2903	
	140°C	3047	3057	3067	
	150°C	3208	3218	3228	

6.7 Switching Characteristics

Over operating free-air temperature range and operating VP – VN range (unless otherwise noted).

PARAMETER		SUBGROUPS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R, t_F	Output current rise and fall time		C_L = 10 pF, R_L = 8 k		1.45		µs
f_P	Output current pulse frequency	8, 9, 10		82	88	94	kHz
	Output current duty cycle			40%	50%	60%	
t_{CONV}	Temperature conversion time(1)	8, 9, 10	2.15 V to 5.5 V	46	50	54	ms
t_{DATA}	Data transmission time	8, 9, 10		44	47	50	ms
	Minimum time required between power cycles			50			ms

(1) Conversion time includes power up time or device turn on time that is typically 3 ms after POR threshold of 1.2 V is exceeded.

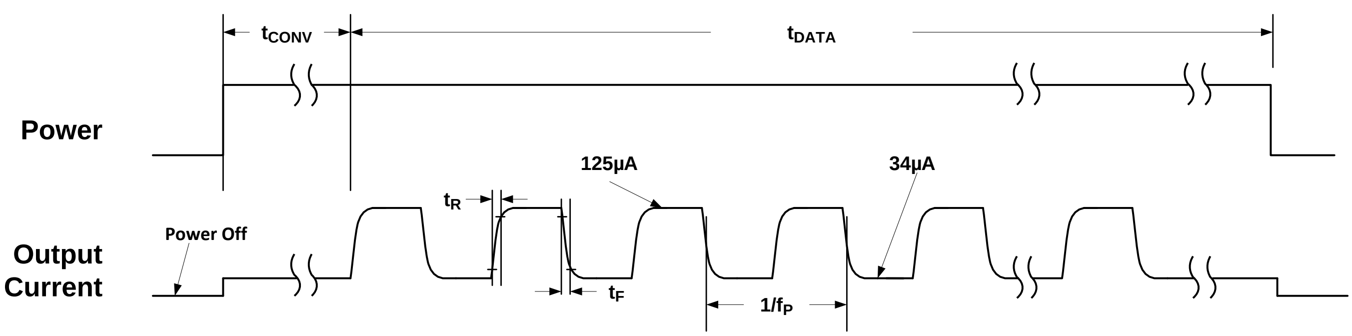
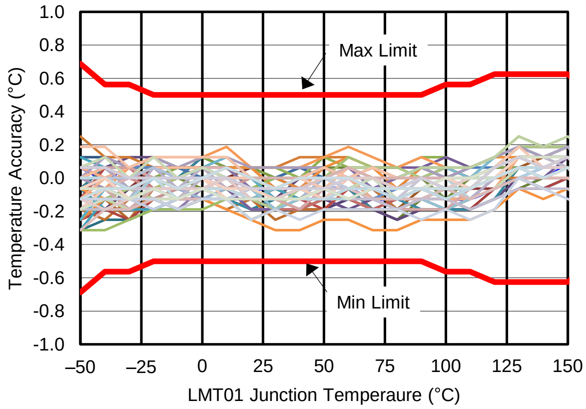


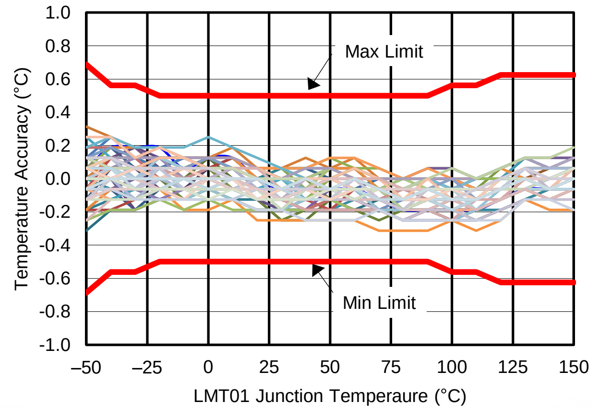
Figure 1. Timing Specification Waveform

6.8 Typical Characteristics



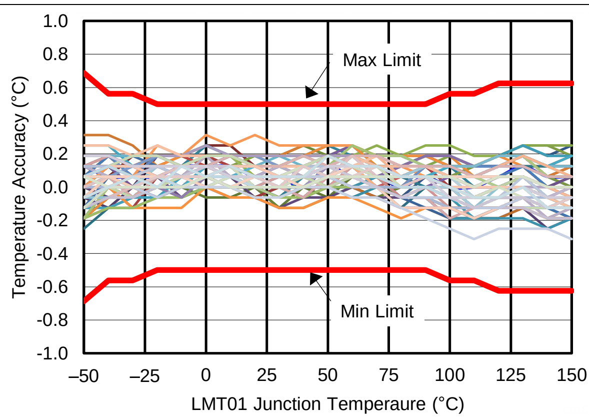
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.15 V

Figure 2. Accuracy vs LMT01-SP Junction Temperature



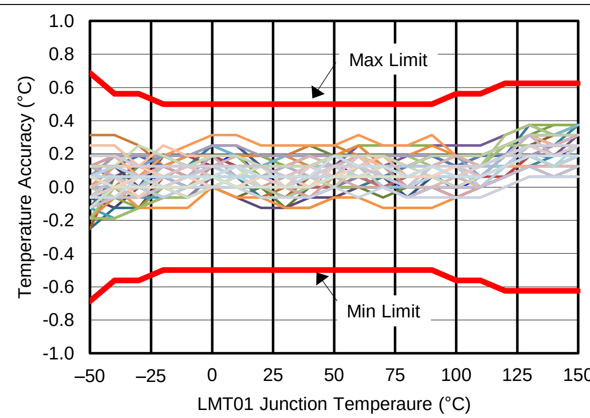
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.4 V

Figure 3. Accuracy vs LMT01-SP Junction Temperature



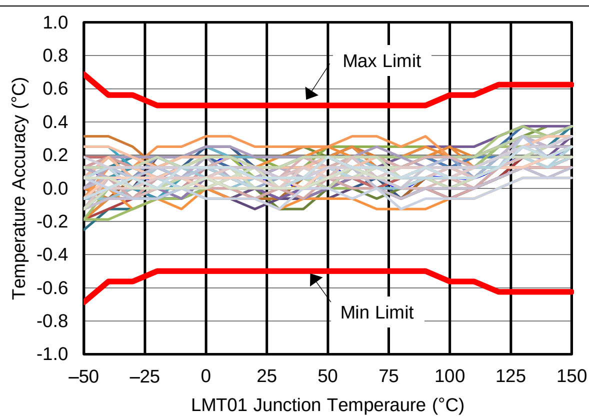
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.7 V

Figure 4. Accuracy vs LMT01-SP Junction Temperature



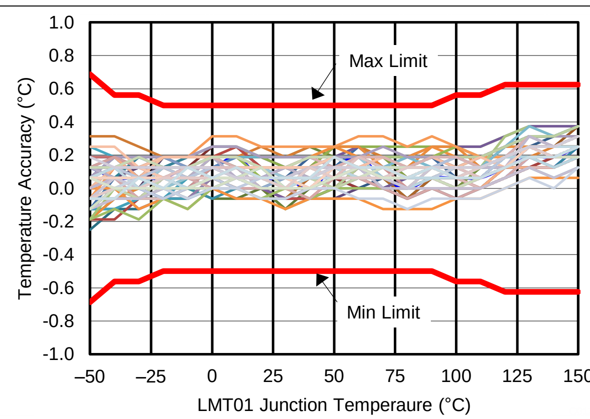
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 3 V

Figure 5. Accuracy vs LMT01-SP Junction Temperature



Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 4 V

Figure 6. Accuracy vs LMT01-SP Junction Temperature



Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 5 V

Figure 7. Accuracy vs LMT01-SP Junction Temperature

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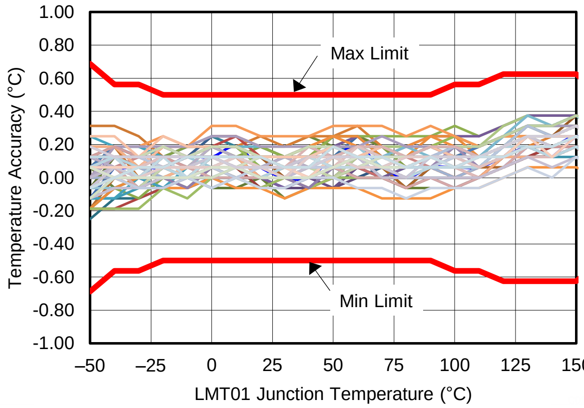
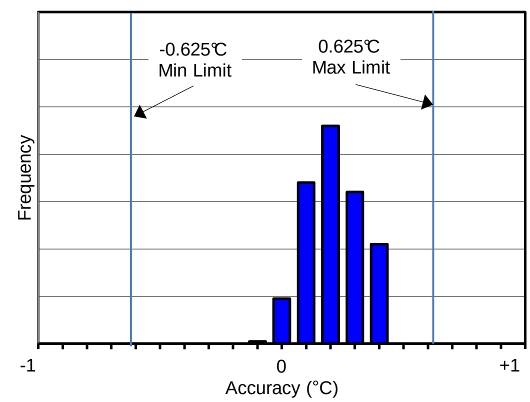
Typical Characteristics (continued)



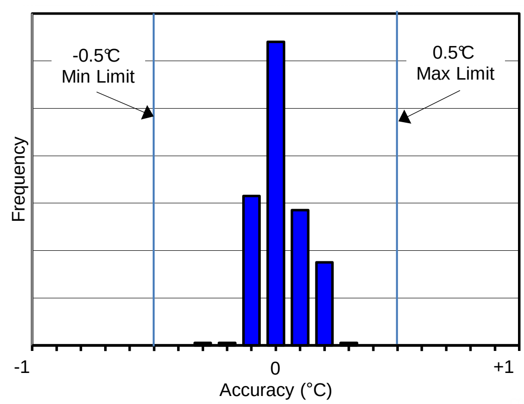
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 5.5 V

Figure 8. Accuracy vs LMT01-SP Junction Temperature



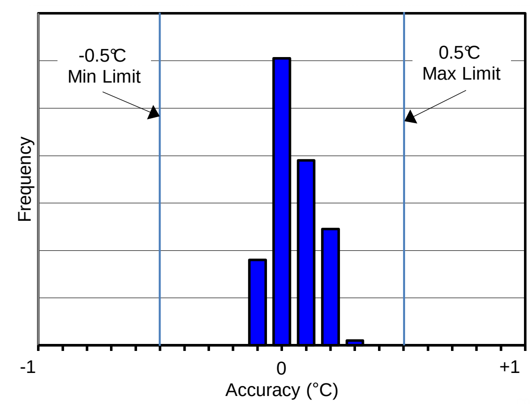
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.15 V to 5.5 V

Figure 9. Accuracy Histogram at 150°C



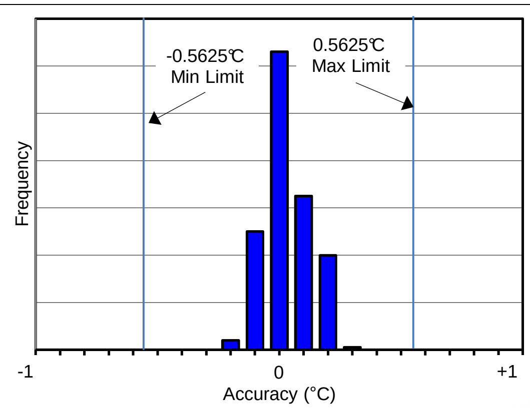
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.15 V to 5.5 V

Figure 10. Accuracy Histogram at 30°C



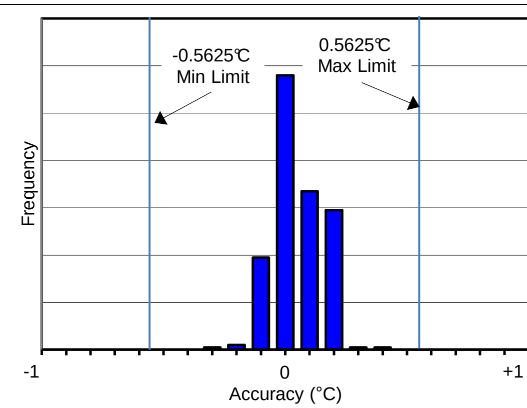
Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.15 V to 5.5 V

Figure 11. Accuracy Histogram at –20°C



Using LUT *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.15 V to 5.5 V

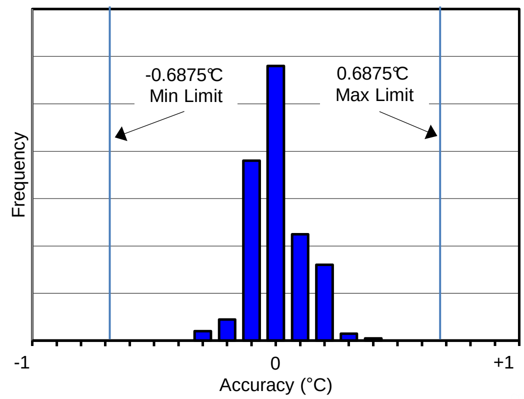
Figure 12. Accuracy Histogram at –30°C



Using *Electrical Characteristics - Pulse Count to Temperature LUT*
VP – VN = 2.15 V to 5.5 V

Figure 13. Accuracy Histogram at –40°C

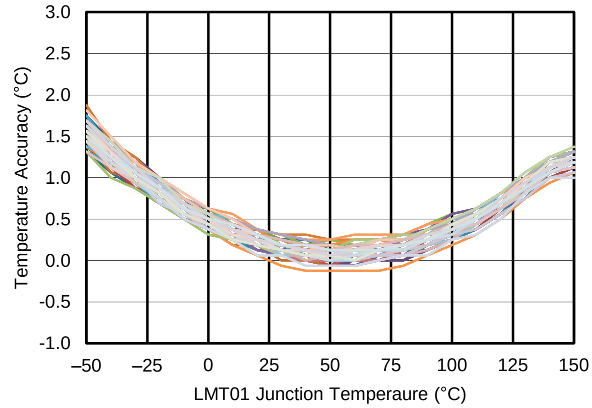
Typical Characteristics (continued)



Using LUT *Electrical Characteristics - Pulse Count to Temperature LUT*

VP – VN = 2.15 V to 5.5 V

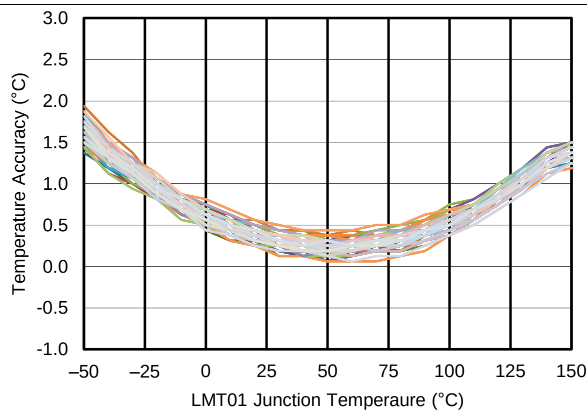
Figure 14. Accuracy Histogram at –50°C



Using Temp = (PC/4096 × 256°C) – 50°C

VP – VN = 2.15 V

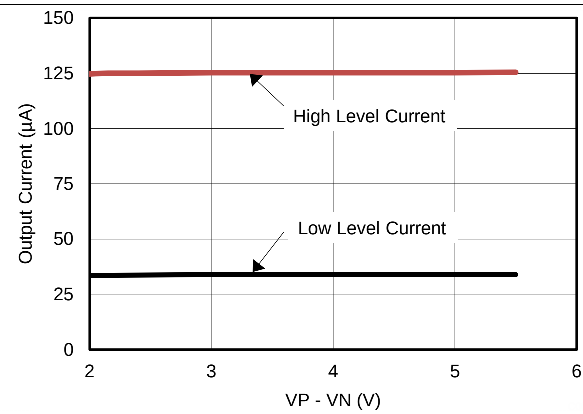
Figure 15. Accuracy Using Linear Transfer Function



Using Temp = (PC/4096 × 256°C) – 50°C

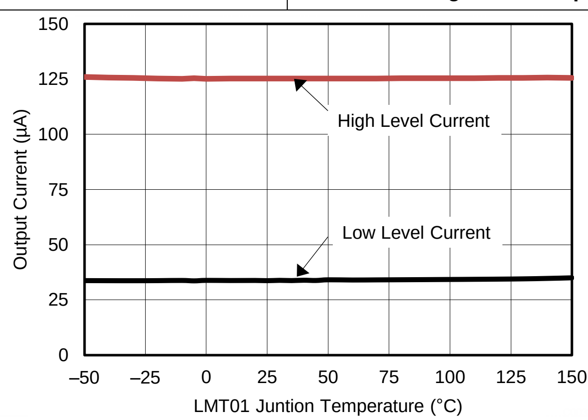
VP – VN = 5.5 V

Figure 16. Accuracy Using Linear Transfer Function



T_A = 30°C

Figure 17. Output Current vs VP-VN Voltage



VP – VN = 3.3 V

Figure 18. Output Current vs Temperature

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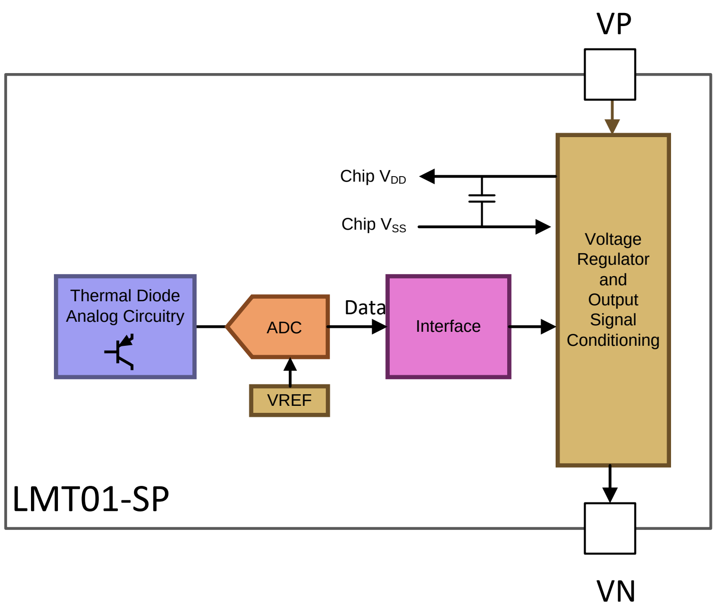
7 Detailed Description

7.1 Overview

The LMT01-SP uses thermal diode analog circuitry to detect the temperature. The temperature signal is then amplified and applied to the input of a ΣΔ ADC that is driven by an internal reference voltage. The ΣΔ ADC output is then processed through the interface circuitry into a digital pulse train. The digital pulse train is then converted to a current pulse train by the output signal conditioning circuitry that includes high and low current regulators. The voltage applied across the pins of the LMT01-SP is regulated by an internal voltage regulator to provide a consistent Chip V_{DD} used by the ADC and its associated circuitry.

The current pulse train output can be converted into a voltage with a single resistor. A simple microcontroller comparator or external transistor can be used convert this signal to valid logic levels the microcontroller can process properly through a GPIO pin. The temperature can be determined by gating a simple counter on for a specific time interval to count the total number of output pulses. After power is first applied the device will remain in a low output state while the LMT01-SP determines the temperature. Once the conversion cycle completes, the pulse train begins with a pulse frequency of approximately 88 kHz. The LMT01-SP will continuously convert and transmit data when the power is applied approximately every 104 ms.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Interface

The LMT01-SP provides a digital output in the form of a pulse count that is transmitted by a train of current pulses. After the LMT01-SP is powered up, it transmits a very low current of 34 µA for less than 54 ms while the part executes a temperature to digital conversion, as shown in *Figure 19*. When the temperature-to-digital conversion is complete, the LMT01-SP starts to transmit a pulse train that toggles from the low current of 34 µA to a high current level of 125 µA. The pulse train total time interval is at maximum 50 ms. The LMT01-SP transmits a series of pulses equivalent to the pulse count at a given temperature as described in *Electrical Characteristics - Pulse Count to Temperature LUT*. After the pulse count has been transmitted the LMT01-SP current level will remain low for the remainder of the 50 ms. The total time for the temperature to digital conversion and the pulse train time interval is 104 ms (maximum). If power is continuously applied, the pulse train output will repeat start every 104 ms (maximum). The LMT01-SP can be powered down at any time to conserve system power. To avoid invalid data it is recommended that a minimum power-down wait time of 50 ms is used before the device is turned on again.

Feature Description (continued)

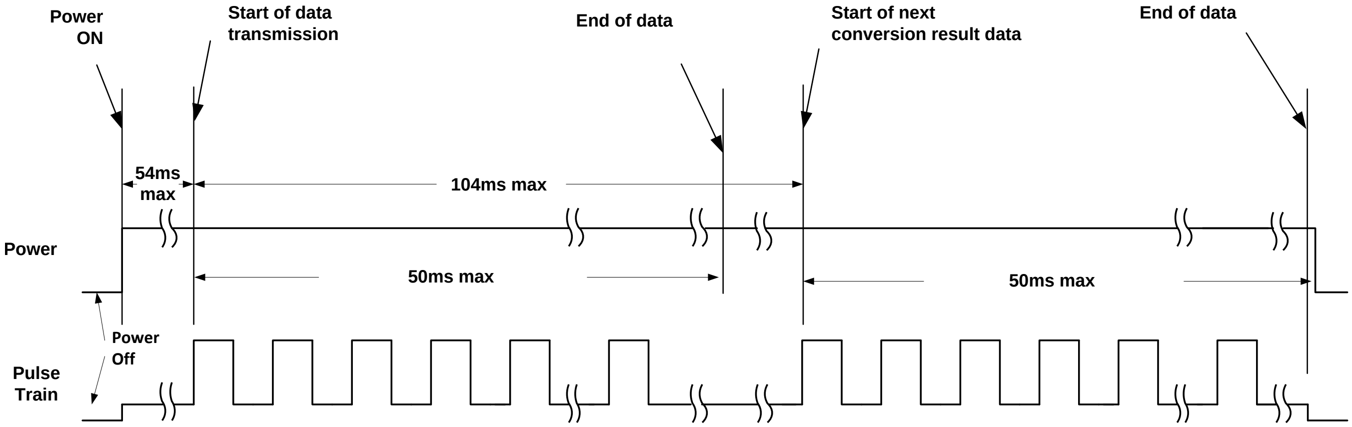


Figure 19. Temperature to Digital Pulse Train Timing Cycle

7.3.2 Output Transfer Function

The LMT01-SP outputs at minimum 1 pulse and a theoretical maximum 4095 pulses. Each pulse has a weight of 0.0625°C. One pulse corresponds to a temperature less than –50°C while a pulse count of 4096 corresponds to a temperature greater than 200°C. Note that the LMT01-SP is only ensured to operate up to 125°C, but is functional up to 150°C. Exceeding this temperature by more than 5°C may damage the device. The accuracy of the device degrades as well when 125°C is exceeded.

Two different methods of converting the pulse count to a temperature value are discussed in this section. The first method is the least accurate and uses a first order equation, and the second method is the most accurate and uses linear interpolation of the values found in the look-up table (LUT) as described in *Electrical Characteristics - Pulse Count to Temperature LUT*.

The output transfer function appears to be linear and can be approximated by Equation 1:

$$\text{Temp} = \left(\frac{PC}{4096} \times 256°C\right) - 50°C \quad (1)$$

where

- PC is the Pulse Count
- Temp is the temperature reading

Table 1 shows some sample calculations using Equation 1.

Table 1. Sample Calculations Using Equation 1

TEMPERATURE (°C)	NUMBER OF PULSES
–49.9375	1
–49.875	2
–40	160
–20	480
0	800
30	1280
50	1600
100	2400
150	3200

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The curve shown in Figure 20 shows the output transfer function using equation Equation 1 (blue line) and the look-up table (LUT) found in *Electrical Characteristics - Pulse Count to Temperature LUT* (red line). The LMT01-SP output transfer function as described by the LUT appears to be linear, but upon close inspection, it can be seen as truly not linear. To actually see the difference, the accuracy obtained by the two methods must be compared.

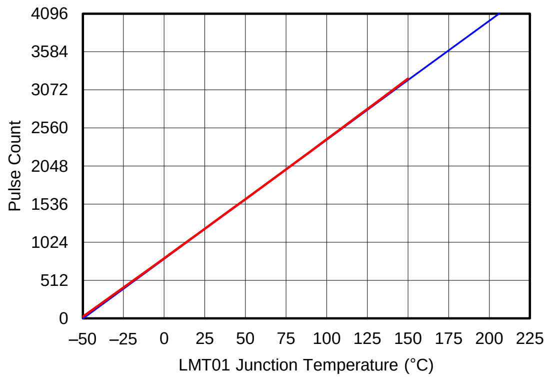

Figure 20. LMT01-SP Output Transfer Function

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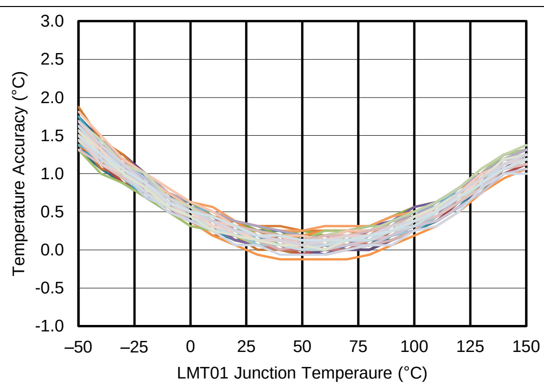
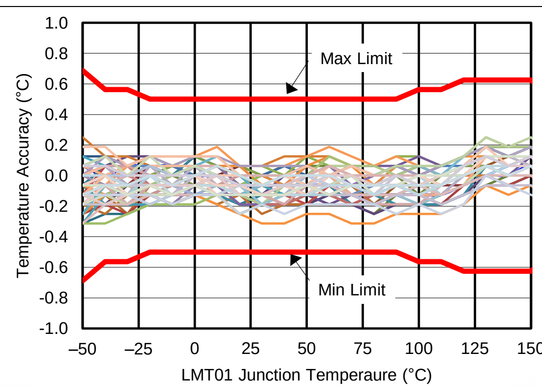
For more exact temperature readings the output pulse count can be converted to temperature using linear interpolation of the values found in *Electrical Characteristics - Pulse Count to Temperature LUT.*

The curves in Figure 21 and Figure 22 show the accuracy of typical units when using the Equation 1 and linear interpolation using *Electrical Characteristics - Pulse Count to Temperature LUT*, respectively. When compared, the improved performance when using the LUT linear interpolation method can clearly be seen. For a limited temperature range of 25°C to 80°C, the error shown in Figure 21 is flat, so the linear equation will provide good results. For a wide temperature range, TI recommends that linear interpolation and the LUT be used.



92 Typical Units Plotted at (VP – VN) = 2.15 V

Figure 21. LMT01-SP Typical Accuracy When Using First Order Equation, Equation 1



92 typical units plotted at (VP – VN) = 2.15 V

Figure 22. LMT01-SP Accuracy Using Linear Interpolation of LUT Found In *Electrical Characteristics - Pulse Count to Temperature LUT*

7.3.3 Current Output Conversion to Voltage

The minimum voltage drop across the LMT01-SP must be maintained at 2.15 V during the conversion cycle. After the conversion cycle, the minimum voltage drop can decrease to 2 V. Thus the LMT01-SP can be used for low voltage applications. See *Application Information* section for more information on low voltage operation and other information on picking the actual resistor value for different applications conditions. The resistor value is dependent on the power supply level and the variation and the threshold level requirements of the circuitry the resistor is driving (that is, MCU, GPIO, or Comparator).

Stray capacitance can be introduced when connecting the LMT01-SP through a long wire. This stray capacitance influences the signal rise and fall times. The wire inductance has negligible effect on the AC signal integrity. A simple RC time constant model as shown in Figure 23 can be used to determine the rise and fall times.

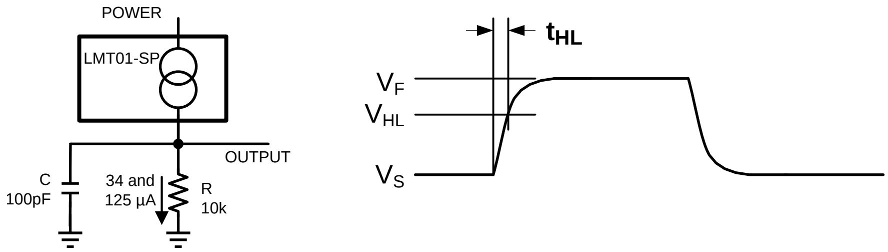


Figure 23. Simple RC Model for Rise and Fall Times

$$t_{HL} = R \times C \times \ln\left(\frac{V_F - V_S}{V_F - V_{HL}}\right)$$

where

- RC as shown in Figure 23
- V_{HL} is the target high level
- the final voltage V_F = 125 µA × R
- the start voltage V_S = 34 µA × R (2)

For the 10% to 90% level rise time (t_r), Equation 2 simplifies to:

$$t_r = R \times C \times 2.197 \quad (3)$$

Take care to ensure that the LMT01-SP voltage drop does not exceed 300 mV under reverse bias conditions, as given in the *Absolute Maximum Ratings*.

7.4 Device Functional Modes

The only functional mode the LMT01-SP has is that it provides a pulse count output that is directly proportional to temperature.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Mounting, Temperature Conductivity, and Self-Heating

The LMT01-SP can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface to ensure good temperature conductivity. The temperatures of the lands and traces to the leads of the LMT01-SP also affect the temperature reading, so they must be a thin as possible.

The LMT01-SP comes in a hermetically sealed ceramic package and as such the IC is not susceptible to moisture or corrosion. Accompanying wiring and circuits should be kept insulated and dry to avoid excessive leakage and corrosion. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The junction temperature of the LMT01-SP is the actual temperature being measured by the device. The thermal resistance junction-to-ambient ($R_{\theta JA}$) is the parameter (from *Thermal Information*) used to calculate the rise of a device junction temperature (self-heating) due to its average power dissipation. The average power dissipation of the LMT01-SP is dependent on the temperature it is transmitting as it effects the output pulse count and the voltage across the device. Equation 4 is used to calculate the self-heating in the die temperature of the LMT01-SP (T_{SH}).

$$T_{SH} = \left[\left(I_{OL} \times \frac{t_{CONV}}{(t_{CONV} + t_{DATA})} \times V_{CONV}\right) + \left(\left[\left(\frac{PC}{4096} \times \frac{(I_{OL} + I_{OH})}{2}\right) + \left(\frac{(4096 - PC)}{4096} \times I_{OL}\right)\right] \times \frac{t_{DATA}}{(t_{CONV} + t_{DATA})}\right) \times V_{DATA}\right] \times R_{\theta JA}$$

where

- T_{SH} is the ambient temperature
- I_{OL} and I_{OH} are the output low and high current level, respectively
- V_{CONV} is the voltage across the LMT01-SP during conversion
- V_{DATA} is the voltage across the LMT01-SP during data transmission
- t_{CONV} is the conversion time
- t_{DATA} is the data transmission time
- PC is the output pulse count
- $R_{\theta JA}$ is the junction to ambient package thermal resistance (4)

Plotted in the curve Figure 24 are the typical average supply current (black line using left y-axis) and the resulting self-heating (red and violet lines using right y-axis) during continuous conversions. A temperature range of –50°C to 150°C, a V_{CONV} of 5 V (red line) and 2.15 V (violet line) were used for the self-heating calculation. As can be seen in the curve, the average power supply current and thus the average self-heating changes linearly over temperature because the number of pulses increases with temperature. A negligible self-heating of about 45 m°C is observed at 150°C with continuous conversions. If temperature readings are not required as frequently as every 100 ms, self-heating can be minimized by shutting down power to the part periodically thus lowering the average power dissipation.

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Application Information (continued)

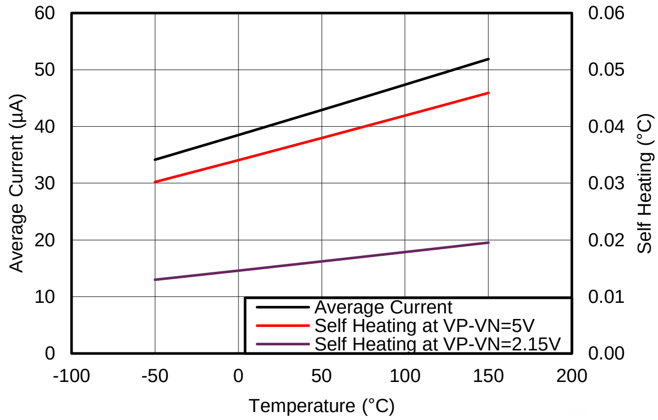

Figure 24. Average Current Draw and Self-Heating Over Temperature

8.2 Typical Application

8.2.1 3.3-V System VDD MSP430 Interface - Using Comparator Input

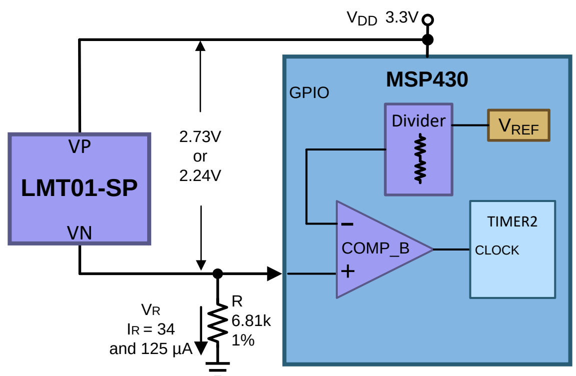

Figure 25. MSP430 Comparator Input Implementation

8.2.1.1 Design Requirements

The design requirements listed in Table 2 are used in the detailed design procedure.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3 V
VDD minimum	3 V
LMT01-SP VP – VN minimum during conversion	2.15 V
LMT01-SP VP – VN minimum during data transmission	2 V
Noise margin	50-mV minimum
Comparator input current over temperature range of interest	< 1 uA
Resistor tolerance	1%

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8.2.1.2 Detailed Design Procedure

First, select the R and determine the maximum logic low voltage and the minimum logic high voltage while ensuring that when the LMT01-SP is converting, the minimum (VP – VN) requirement of 2.15 V is met.

1. Select R using minimum VP – VN during data transmission (2 V) and maximum output current of the LMT01-SP (143.75 µA)
   - R = (3.0 V – 2 V) / 143.75 µA = 6.993 k the closest 1% resistor is 6.980 k
   - 6.993 k is the maximum resistance so if using 1% tolerance resistor the actual resistor value needs to be 1% less than 6.993 k and 6.98 k is 0.2% less than 6.993 k thus 6.81 k must be used.
2. Check to see if the 2.15-V minimum voltage during conversion requirement for the LMT01-SP is met with the maximum I_{OL} of 39 µA and maximum R of 6.81 k + 1%:
   - $V_{LMT01\text{-}SP}$ = 3 V – (6.81 k × 1.01) × 39 µA = 2.73 V
3. Find the maximum low level voltage range using the maximum R of 6.81 k and maximum I_{OL} of 39 µA:
   - V_{RLmax} = (6.81 k × 1.01) × 39 µA = 268 mV
4. Find the minimum high level voltage using the minimum R of 6.81 k and minimum I_{OH} of 112.5 µA:
   - V_{RHmin} = (6.81 k × 0.99) × 112.5 µA = 758 mV

Now select the MSP430 comparator threshold voltage that enables the LMT01-SP to communicate to the MSP430 properly.

1. The MSP430 voltage is selected by selecting the internal V_{REF} and then choosing the appropriate 1 of n/32 settings for n of 1 to 31.
   - V_{MID}= (V_{RLmax} – V_{RHmin}) / 2 + V_{RHmin} = (758 mV – 268 mV) / 2 + 268 mV = 513 mV
   - n = (V_{MID} / V_{REF}) × 32 = (0.513 / 2.5) × 32 = 7
2. To prevent oscillation of the comparator, output hysteresis must be implemented. The MSP430 allows this by enabling different n for the rising edge and falling edge of the comparator output. For a falling comparator output transition, N must be set to 6.
3. Determine the noise margin caused by variation in comparator threshold level. Even though the comparator threshold level theoretically is set to V_{MID}, the actual level varies from device to device due to V_{REF} tolerance, resistor divider tolerance, and comparator offset. For proper operation, the COMP_B worst case input threshold levels must be within the minimum high and maximum low voltage levels presented across R, V_{RHmin} and V_{RLmax}, respectively

$$V_{CHmax} = V_{REF} \times (1 + V\_REF\_TOL) \times \frac{(N + N\_TOL)}{32} + COMP\_OFFSET$$

where
- VREF is the MSP430 COMP_B reference voltage for this example at 2.5 V
- V_REF_TOL is the tolerance of the VREF of 1% or 0.01
- N is the divisor for the MSP430 or 7
- N_TOL is the tolerance of the divisor or 0.5
- COMP_OFFSET is the comparator offset specification or 10 mV (5)

$$V_{CLmin} = V_{REF} \times (1 - V\_REF\_TOL) \times \frac{(N - N\_TOL)}{32} - COMP\_OFFSET$$

where
- VREF is the MSP430 COMP_B reference voltage for this example at 2.5 V
- V_REF_TOL is the tolerance of the VREF of 1% or 0.01
- N is the divisor for the MSP430 for the hysteresis setting or 6
- N_TOL is the tolerance of the divisor or 0.5
- COMP_OFFSET is the comparator offset specification or 10 mV (6)

The noise margin is the minimum of the two differences:

$$(V_{RHmin} – V_{CHmax}) \text{ or } (V_{CHmin} – V_{RLmax}) \quad (7)$$

which works out to be 145 mV.

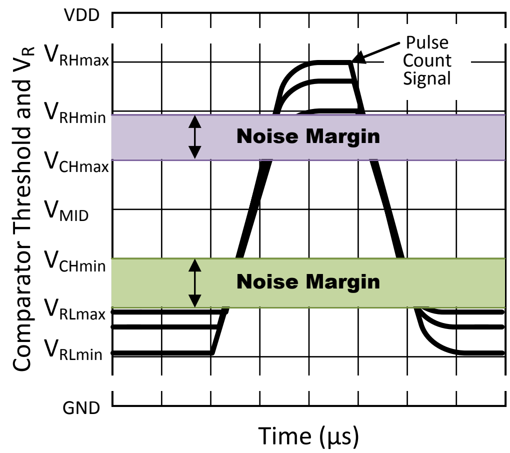
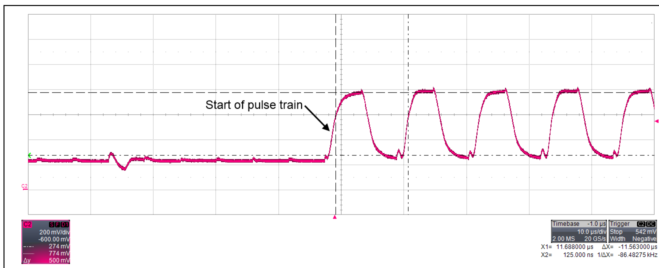


Figure 26. Pulse Count Signal Amplitude Variation

8.2.1.2.1 Setting the MSP430 Threshold and Hysteresis

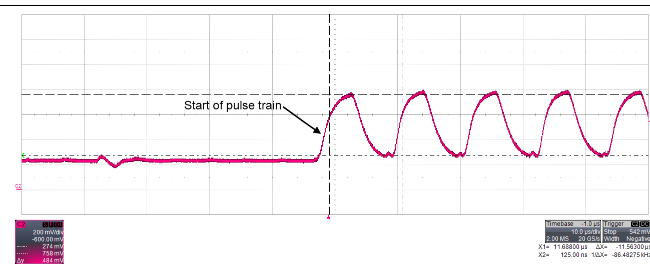
The comparator hysteresis determines the noise level that the signal can support without causing the comparator to trip falsely and resulting in an inaccurate pulse count. The comparator hysteresis is set by the precision of the MSP430 and what thresholds it is capable of. For this case, as the input signal transitions high, the comparator threshold is dropped by 77 mV. If the noise on the signal is kept below this level as it transitions, the comparator will not trip falsely. In addition, the MSP430 has a digital filter on the COMP_B output that can be used to further filter output transitions that occur too quickly.

8.2.1.3 Application Curves



Amplitude = 200 mV/div
Time Base = 10 µs/div
∆y at cursors = 500 mV
∆x at cursors = 11.7 µs

Figure 27. MSP430 COMP_B Input Signal No Capacitance Load



Amplitude = 200 mV/div
Time Base = 10 µs/div
∆y at cursors = 484 mV
∆x at cursors = 11.7 µs

Figure 28. MSP430 COMP_B Input Signal 100-pF Capacitance Load

8.3 System Examples

The LMT01-SP device can be configured in a number of ways. Transistor level shifting can be used so that the output pulse of the device can be read with a GPIO (see Figure 29). Multiple LMT01-SP devices can be controlled with GPIOs and read by a single comparator input as shown in Figure 30. Lastly, the LMT01-SP device can be configured to have a common ground with a high side signal (see Figure 31).

ADVANCE INFORMATION

System Examples (continued)

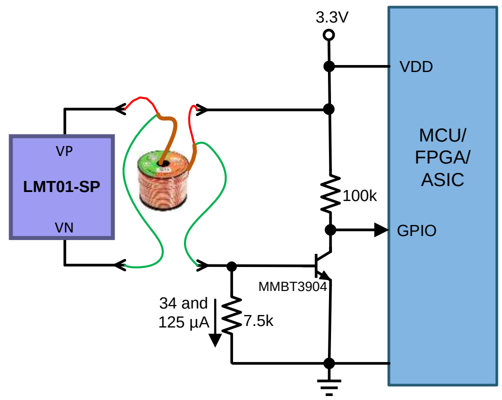
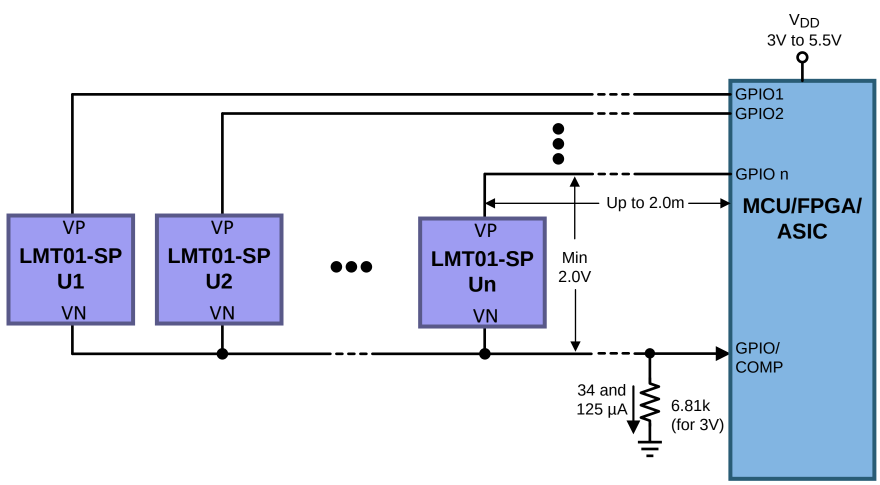
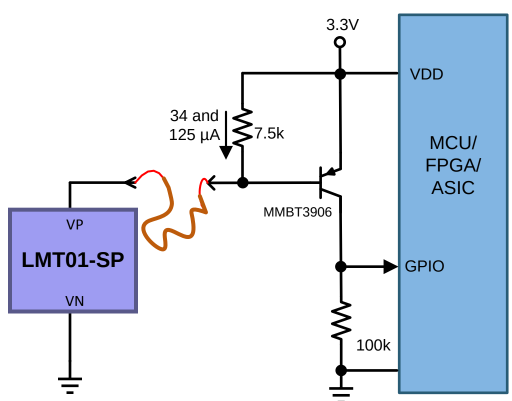


Figure 29. Transistor Level Shifting



Note: to turn off an LMT01-SP set the GPIO pin connected to VP to high impedance state as setting it low would cause the off LMT01-SP to be reverse biased. Comparator input of MCU must be used.

Figure 30. Connecting Multiple Devices to One MCU Input Pin



Note: the VN of the LMT01-SP must be connected to the MCU GND.

Figure 31. Common Ground With High-Side Signal

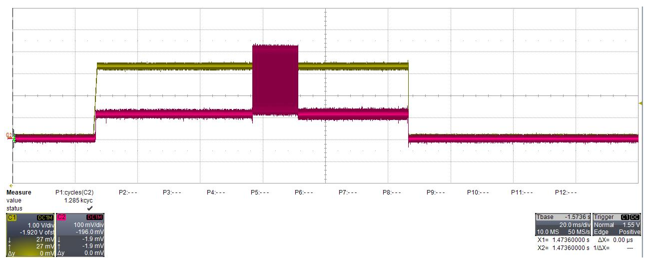
ADVANCE INFORMATION

9 Power Supply Recommendations

Because the LMT01-SP is only a 2-pin device the power pins are common with the signal pins, thus the LMT01-SP has a floating supply that can vary greatly. The LMT01-SP has an internal regulator that provides a stable voltage to internal circuitry.

Take care to prevent reverse biasing of the LMT01-SP as exceeding the absolute maximum ratings may cause damage to the device.

Power supply ramp rate can effect the accuracy of the first result transmitted by the LMT01-SP. As shown in Figure 32 with a 1-ms rise time, the LMT01-SP output code is at 1286, which converts to 30.125°C. The scope photo shown in Figure 33 reflects what happens when the rise time is too slow. In Figure 33, the power supply (yellow trace) is still ramping up to final value while the LMT01-SP (red trace) has already started a conversion. This causes the output pulse count to decrease from the previously shown 1286, to 1282 (or 29.875°C). Thus, for slow ramp rates, TI recommends that the first conversion be discarded. For even slower ramp rates, more than one conversion may have to be discarded as TI recommends that either the power supply be within final value before a conversion is used or that ramp rates be faster than 2.5 ms.

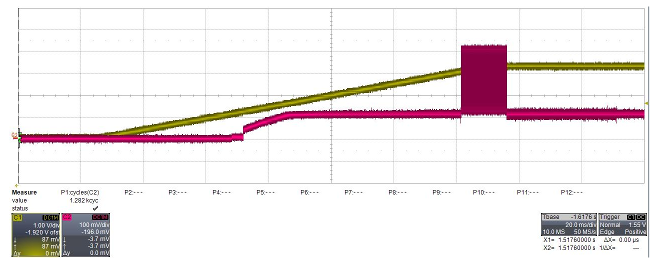


Yellow trace = 1 V/div, Red trace = 100 mV/div, Time Base = 20 ms/div

T_A = 30°C LMT01-SP Pulse Count = 1286

VP – VN = 3.3 V Rise Time = 1 ms

Figure 32. Output Pulse Count With Appropriate Power Supply Rise Time



Yellow trace = 1 V/div, Red trace = 100 mV/div, Time base = 20 ms/div

T_A = 30°C LMT01-SP Pulse Count = 1282

VP – VN = 3.3 V Rise Time = 100 ms

Figure 33. Output Pulse Count With Slow Power Supply Rise Time

10 Layout

10.1 Layout Guidelines

The LMT01-SP can be mounted as a through-hole component for ambient sensing or cemented to a surface using a thermally conductive paste. The traces leading to the pads of the LMT01-SP should be kept as small as possible to minimize their effect on the temperature the LMT01-SP is measuring. The metal lid of the device has no internal connections to the die and is thus floating. If desired, a wire can be soldered from the lid to ground.

10.2 Layout Example

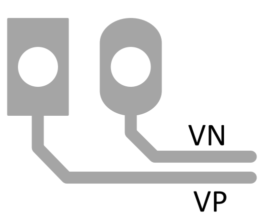


Figure 34. Layout Example (CTO-92/HTA Package)

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLMT01HTA/EM	ACTIVE	CTO	HTA	2	1	TBD	Call TI	Call TI	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMT01-SP :

- Catalog: LMT01
- Automotive: LMT01-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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