2.5 Ω CMOS Low Power Dual 2:1 Mux/Demux USB 1.1 Switch

ADG787

FEATURES

- **USB 1.1 signal switching compliant**
- **−3 dB bandwidth, 150 MHz**
- **Tiny 10-lead LFCSP and MSOP packages, 10-ball WLCSP package**
- **Single-supply 1.8 V to 5.5 V operation**
- **Low on resistance**
  - **2.5 Ω typical**
  - **3.45 Ω maximum at 85°C**
- **Typical power consumption: <0.1 µW**

APPLICATIONS

- **USB 1.1 signal switching circuits**
- **Cellular phones**
- **PDAs**
- **MP3 players**
- **Battery-powered systems**
- **Headphone switching**
- **Audio and video signal routing**
- **Communications systems**

FUNCTIONAL BLOCK DIAGRAM

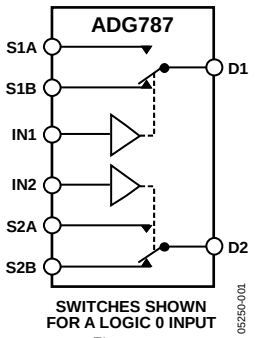


Figure 1.

GENERAL DESCRIPTION

The ADG787 is a low voltage, CMOS device that contains two independently selectable single-pole, double-throw (SPDT) switches. It is designed as a general analog-to-digital switch and can also be used for routing USB 1.1 signals.

This device offers low on resistance of typically 2.5 Ω, making the part an attractive solution for applications that require low distortion through the switch.

The ADG787 comes in a 10-ball WLCSP, a tiny 10-lead LFCSP, and a tiny 10-lead MSOP. These packages make the ADG787 the ideal solution for space-constrained applications.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG787 exhibits break-before-make switching action.

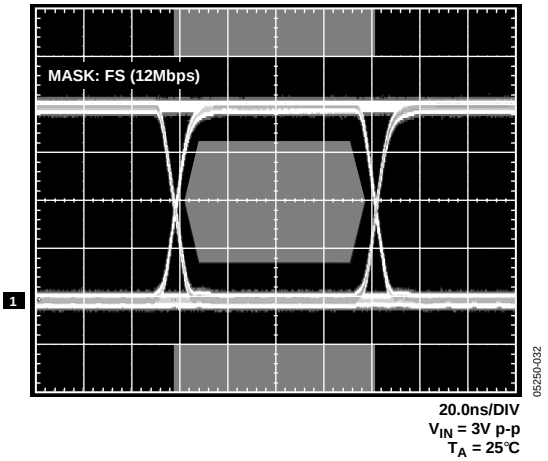


Figure 2. Eye Pattern; 12 Mbps, V_{DD} = 4.2 V, PRBS 31

Rev. A

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REVISION HISTORY

5/06—Rev. 0 to Rev. A

Updated Formatting ..... Universal
Changes to Table 1 3
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Changes to Ordering Guide 15

1/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.2 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	B Version[1]	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_{DD} = 4.2 V, V_S = 0 V to V_{DD}, I_S = 10 mA
	3	3.45	Ω max	See Figure 28
On Resistance Match Between Channels (ΔR_{ON})	0.02		Ω typ	V_{DD} = 4.2 V, V_S = 3.5 V, I_S = 10 mA
		0.1	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.65		Ω typ	V_{DD} = 4.2 V, V_S = 0 V to V_{DD}
	0.8	0.95	Ω max	I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage, I_S (OFF)	±0.05		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 29
Channel On Leakage, I_D, I_S (ON)	±0.05		nA typ	V_S = V_D = 1 V or 4.5 V; see Figure 30
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	2.5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	13		ns typ	R_L = 50 Ω, C_L = 35 pF
	19	22	ns max	V_S = 3 V; see Figure 31
t_{OFF}	3		ns typ	R_L = 50 Ω, C_L = 35 pF
	5	6	ns max	V_S = 3 V; see Figure 31
Propagation Delay Skew, t_{SKEW}	0.06		ns typ	C_L = 50 pF; V_S = 3 V
		0.15	ns max	
Break-Before-Make Time Delay (t_{BBM})	10		ns typ	R_L = 50 Ω, C_L = 35 pF
		5	ns min	V_{S1} = V_{S2} = 3 V; see Figure 32
Charge Injection	14		pC typ	V_D = 1 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−63		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Channel-to-Channel Crosstalk	−110		dB typ	S1A to S2A/S1B to S2B; R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
	−63		dB typ	S1A to S1B/S2A to S2B; R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 36
Total Harmonic Distortion (THD + N)	0.03		%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p
Insertion Loss	−0.2		dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
−3 dB Bandwidth	145		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
C_S (OFF)	16		pF typ	
C_D, C_S (ON)	40		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.005		μA typ	Digital inputs = 0 V or 5.5 V
		1	μA max	

[1] Temperature ranges: B version: −40°C to +85°C for the MSOP and LFCSP packages, and −25°C to +85°C for the WLCSP package.
[2] Guaranteed by design, not production tested.

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	B Version[1]	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range			V	
On Resistance (R_{ON})	4		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}
	5.75	6	Ω max	I_S = 10 mA; see Figure 28
On Resistance Match Between Channels (ΔR_{ON})	0.07		Ω typ	V_{DD} = 2.7 V, V_S = 1.5 V
	0.3	0.35	Ω max	I_S = 10 mA
On Resistance Flatness ($R_{FLAT (ON)}$)	1.6		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}
	2.3	2.6	Ω max	I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.6 V
Source Off Leakage, I_S (OFF)	±0.01		nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V; see Figure 29
Channel On Leakage, I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 0.6 V or 3.3 V; see Figure 30
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.3	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	18		ns typ	R_L = 50 Ω, C_L = 35 pF
	30	35	ns max	V_S = 1.5 V; see Figure 31
t_{OFF}	4		ns typ	R_L = 50 Ω, C_L = 35 pF
	6	7	ns max	V_S = 1.5 V; see Figure 31
Propagation Delay Skew, t_{SKEW}	0.04		ns typ	C_L = 50 pF; V_S = 1.5 V
		0.12	ns max	
Break-Before-Make Time Delay (t_{BBM})	15		ns typ	R_L = 50 Ω, C_L = 35 pF
		5	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 32
Charge Injection	10		pC typ	V_D = 1.25 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−63		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Channel-to-Channel Crosstalk	−110		dB typ	S1A to S2A/S1B to S2B; R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
	−63		dB typ	S1A to S1B/S2A to S2B; R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
Total Harmonic Distortion (THD + N)	0.07		%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1.5 V p-p
Insertion Loss	−0.24		dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
−3 dB Bandwidth	145		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
C_S (OFF)	16		pF typ	
C_D, C_S (ON)	40		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.6 V
I_{DD}	0.005		μA typ	Digital inputs = 0 V or 3.6 V
		1	μA max	

[1] Temperature range: B version: −40°C to +85°C for the MSOP and LFCSP packages, and −25°C to +85°C for the WLCSP package.
[2] Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +6 V
Analog Inputs[1], Digital Inputs	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Peak Current, S or D	
5 V Operation	300 mA
3.3 V Operation	200 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	
5 V Operation	100 mA
3.3 V Operation	80 mA
Operating Temperature Range	
Extended Industrial (B Version)	
MSOP and LFCSP packages	−40°C to +85°C
Industrial (B version)	
WLCSP package	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
WLCSP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	120°C/W
LFCSP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	61°C/W
MSOP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	142°C/W
θ_{JC} Thermal Impedance	43.7°C/W
Lead-Free Temperature Soldering	
IR Reflow, Peak Temperature	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at the IN, S, or D pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

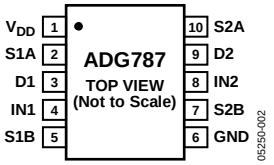


Figure 3. 10-Lead LFCSP and 10-lead MSOP Pin Configuration

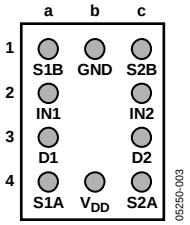


Figure 4. 10-Ball WLCSP Pin Configuration

Table 4. 10-Lead LFCSP/MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	S1A	Source Terminal. May be an input or output.
3	D1	Drain Terminal. May be an input or output.
4	IN1	Logic Control Input.
5	S1B	Source Terminal. May be an input or output.
6	GND	Ground (0 V) Reference.
7	S2B	Source Terminal. May be an input or output.
8	IN2	Logic Control Input.
9	D2	Drain Terminal. May be an input or output.
10	S2A	Source Terminal. May be an input or output.

Table 5. 10-Lead WLCSP Pin Function Descriptions

Ball Location	Mnemonic	Description
1a	S1B	Source Terminal. May be an input or output.
1b	GND	Ground (0 V) Reference.
1c	S2B	Source Terminal. May be an input or output.
2a	IN1	Source Terminal. May be an input or output.
2c	IN2	Logic Control Input.
3a	D1	Drain Terminal. May be an input or output.
3c	D2	Drain Terminal. May be an input or output.
4a	S1A	Logic Control Input.
4b	V_{DD}	Most Positive Power Supply Potential.
4c	S2A	Source Terminal. May be an input or output.

TRUTH TABLE

Table 6.

Logic (IN1/IN2)	Switch 1A/2A	Switch 1B/2B
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

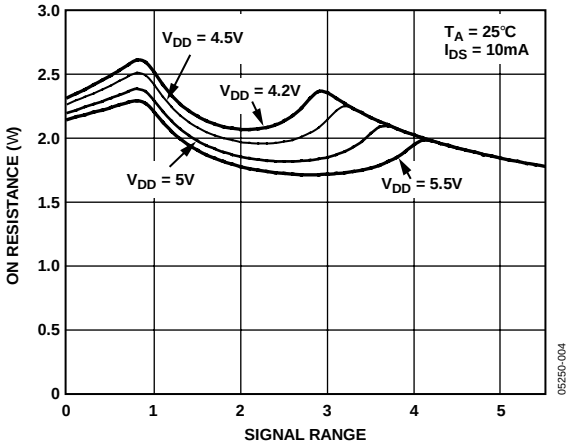


Figure 5. On Resistance vs. V_D (V_S), V_{DD} = 4.2 V to 5.5 V

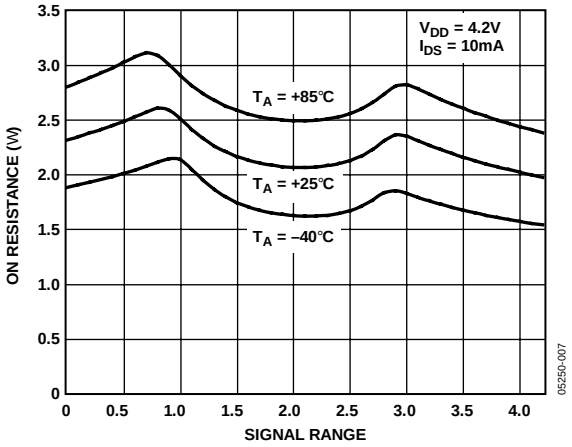


Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 4.2 V

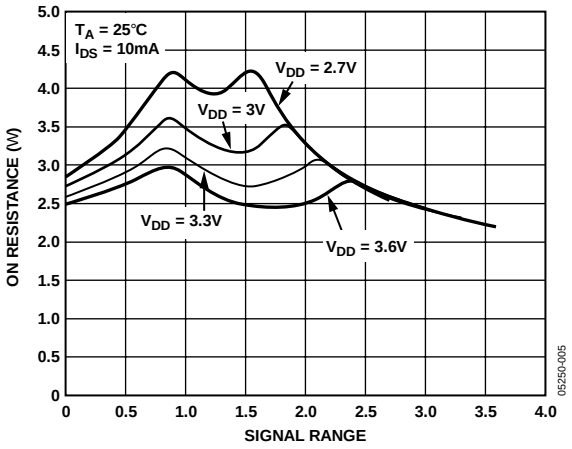


Figure 6. On Resistance vs. V_D (V_S), V_{DD} = 2.7 V to 3.6 V

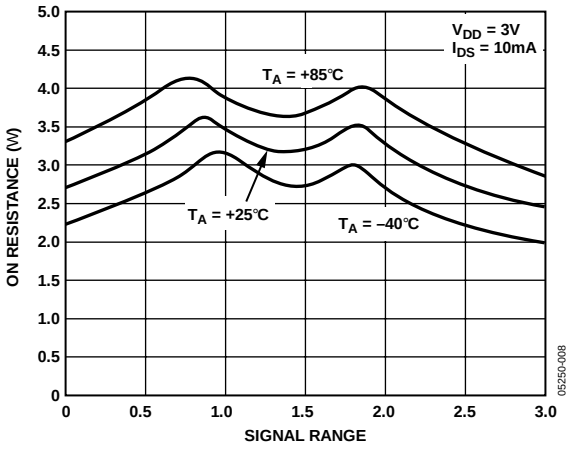


Figure 9. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 3 V

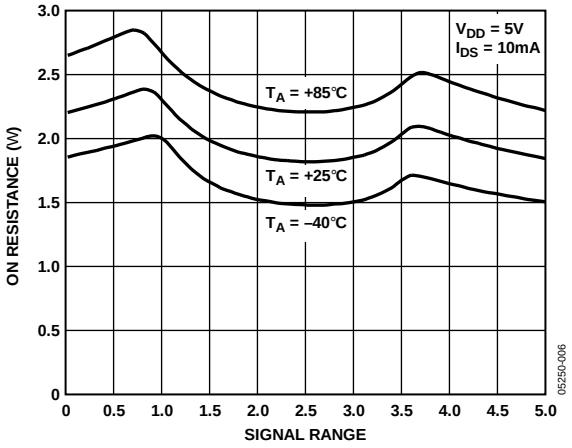


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 5 V

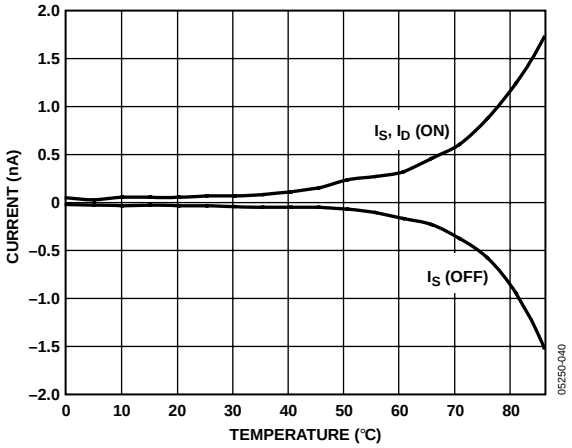


Figure 10. Leakage Current vs. Temperature, V_{DD} = 5.5 V

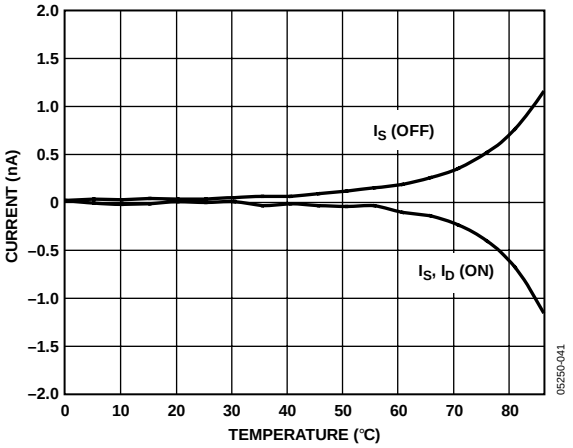


Figure 11. Leakage Current vs. Temperature, V_{DD} = 3.3 V

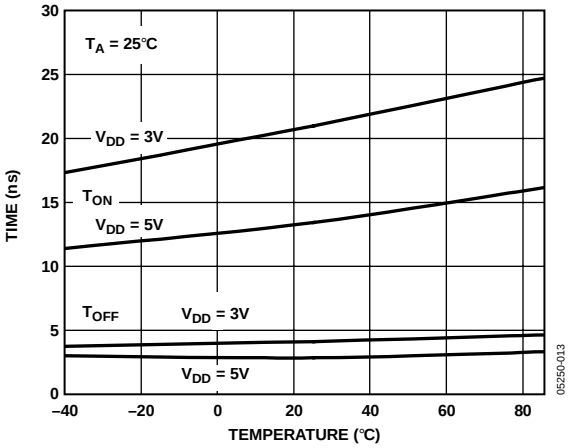


Figure 14. t_{ON}/t_{OFF} Time vs. Temperature

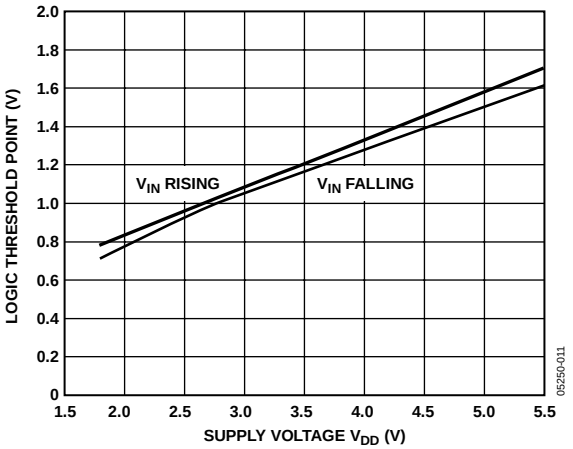


Figure 12. Threshold Voltage vs. Supply

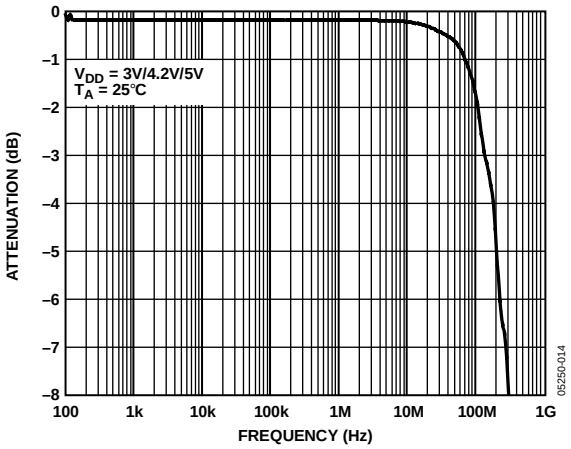


Figure 15. Bandwidth

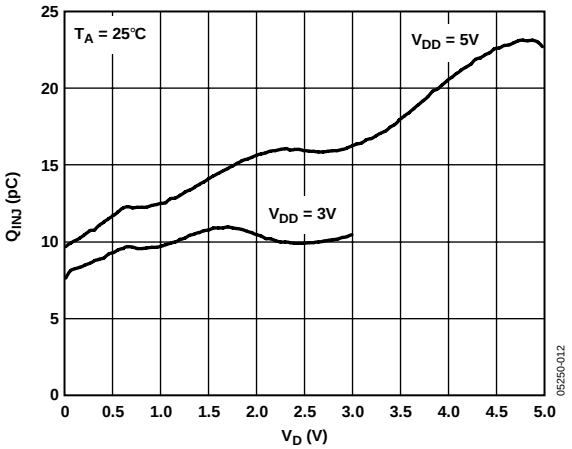


Figure 13. Charge Injection vs. Source Voltage

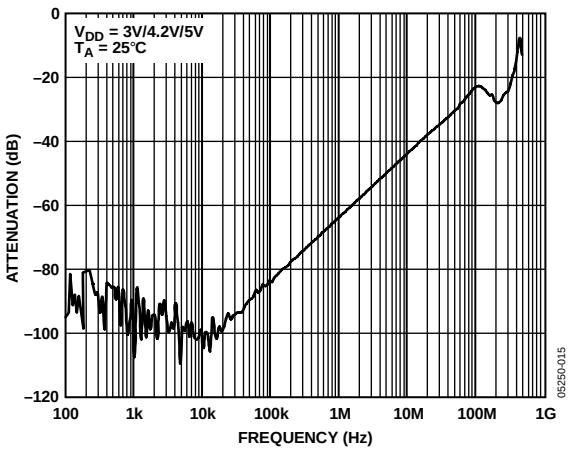


Figure 16. Off Isolation vs. Frequency

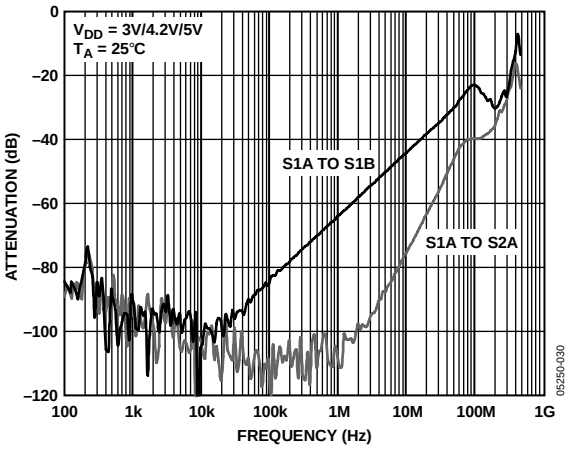


Figure 17. Crosstalk vs. Frequency

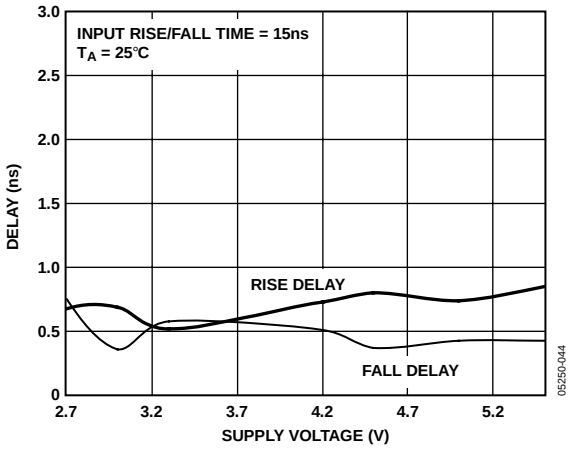


Figure 20. Rise/Fall Time Delay vs. Supply Voltage

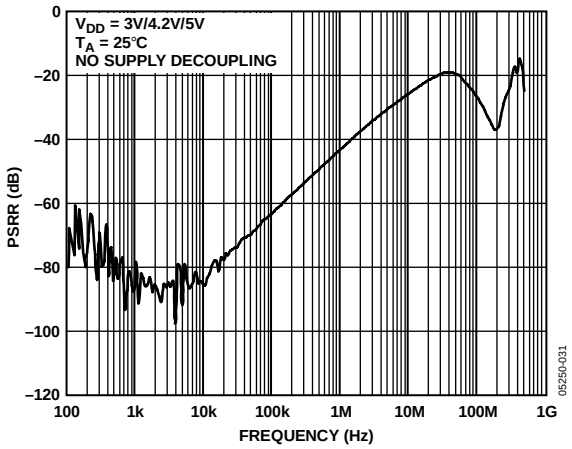


Figure 18. AC Power Supply Rejection Ratio (PSRR)

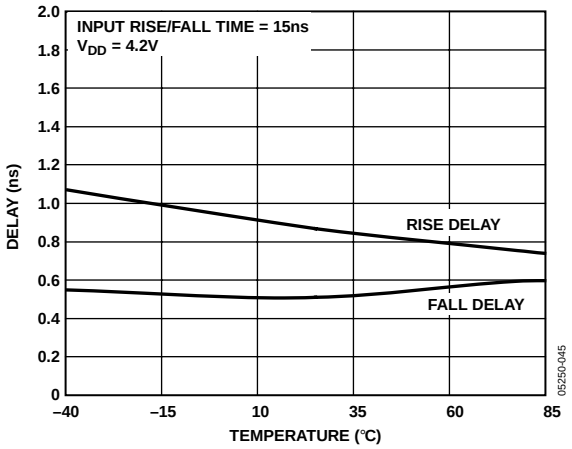


Figure 21. Rise/Fall Time Delay vs. Temperature

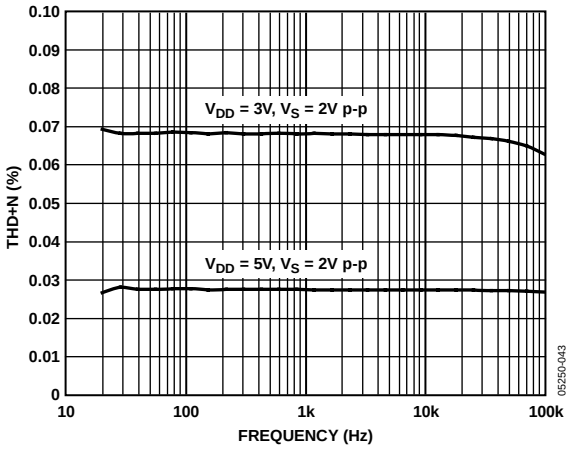


Figure 19. Total Harmonic Distortion + Noise

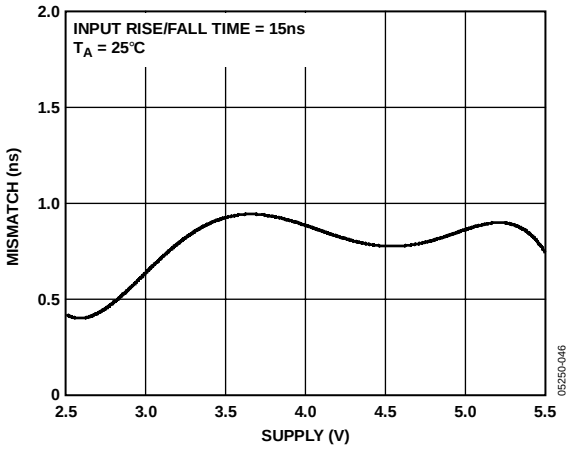


Figure 22. Rise-Time-to-Fall-Time Mismatch vs. Supply Voltage

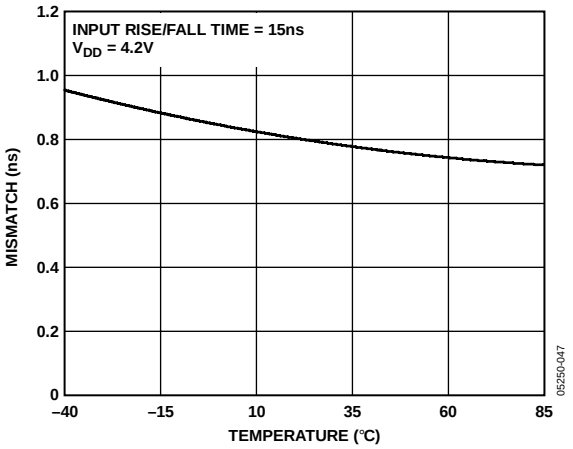


Figure 23. Rise-Time-to-Fall-Time Mismatch vs. Temperature

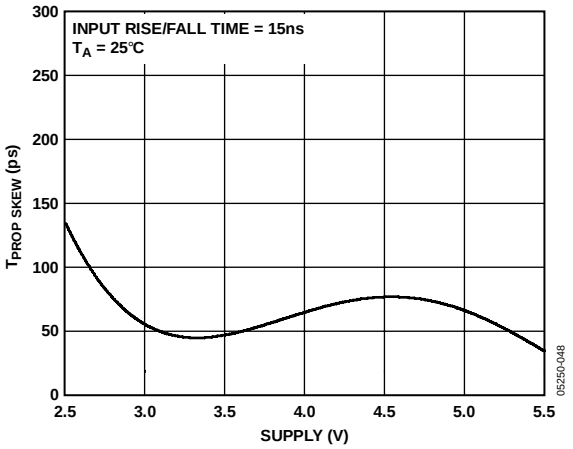


Figure 24. Propagation Delay Skew (t_{SKEW}) vs. Supply Voltage

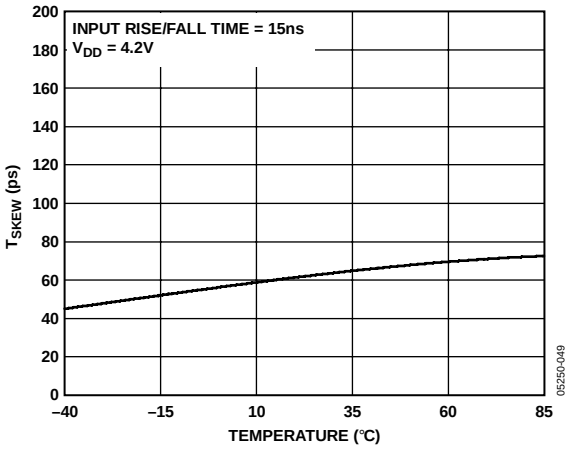


Figure 25. Propagation Delay Skew (t_{SKEW}) vs. Temperature

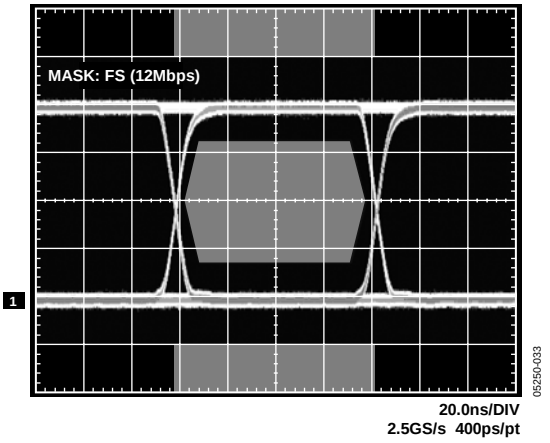


Figure 26. Eye Pattern, 12 Mbps, V_{DD} = 4.2 V, T_A = 85°C, PRBS 31

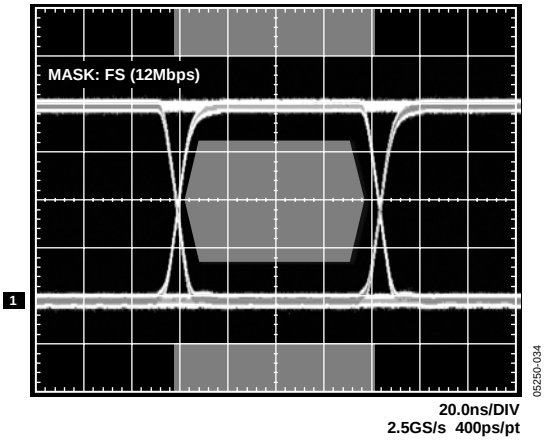


Figure 27. Eye Pattern, 12 Mbps, V_{DD} = 4.2 V, T_A = −40°C, PRBS 31

TEST CIRCUITS

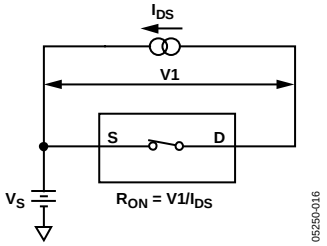


Figure 28. On Resistance

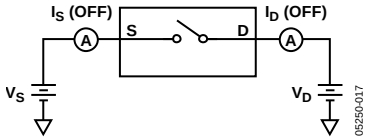


Figure 29. Off Leakage

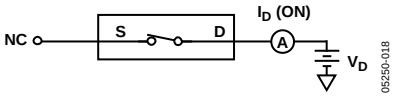


Figure 30. On Leakage

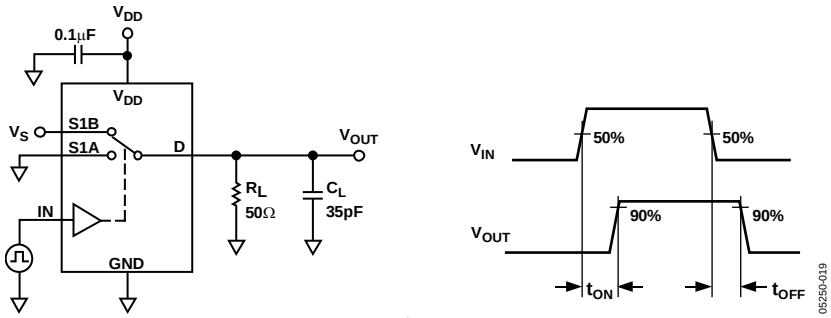


Figure 31. Switching Times, t_{ON}, t_{OFF}

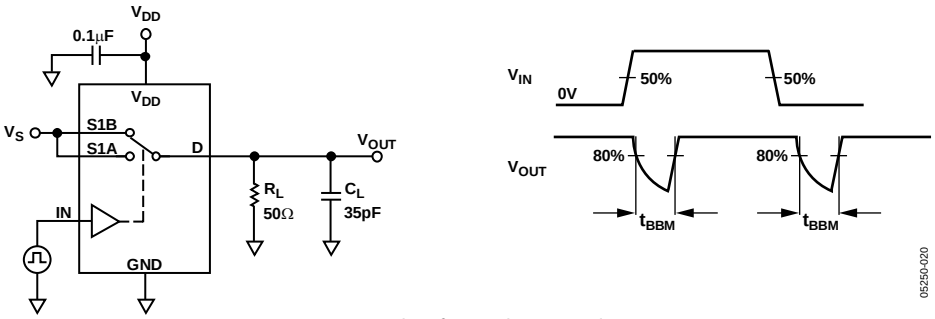


Figure 32. Break-Before-Make Time Delay, t_{BBM}

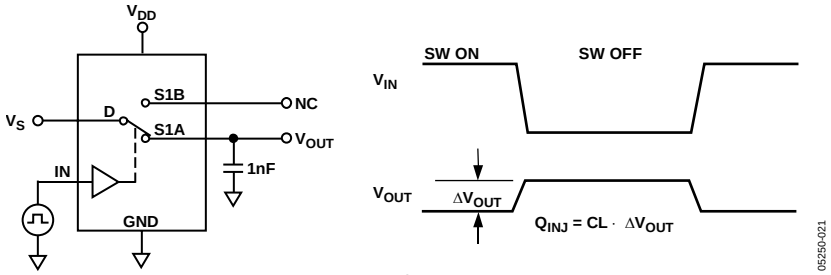
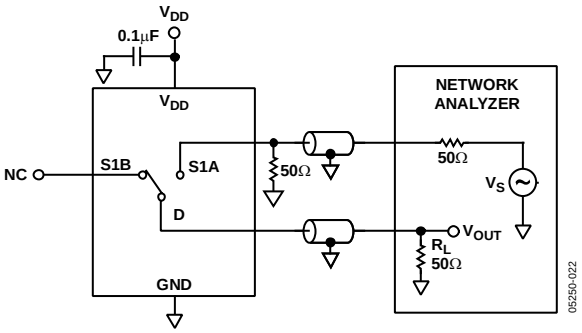
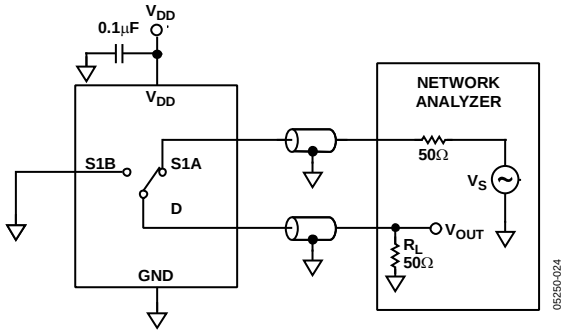


Figure 33. Charge Injection



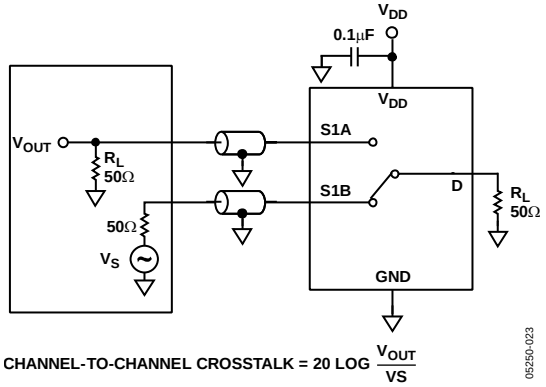
$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 34. Off Isolation



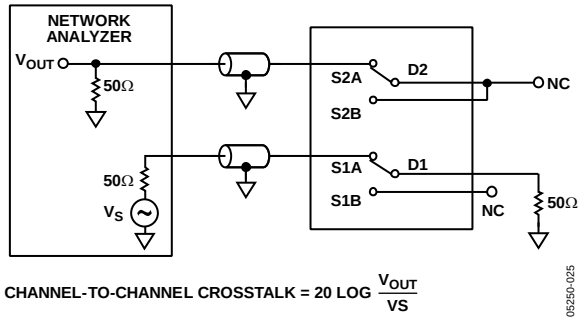
$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}$$

Figure 36. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 35. Channel-to-Channel Crosstalk (S1A to S1B)



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 37. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD}
Positive supply current.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

R_{ON}
Ohmic resistance between D and S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}
On resistance match between any two channels.

I_S (OFF)
Source leakage current with the switch off.

I_D (OFF)
Drain leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (OFF)
Off switch source capacitance. Measured with reference to ground.

C_D (OFF)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (ON)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitudes plus noise of a signal, to the fundamental.

T_{SKEW}
The measure of the variation in propagation delay between each channel.

Rise Time Delay
The rise time of a signal is a measure of the time for the signal to rise from 10% of the ON level to 90% of the ON level. Rise time delay is the difference between the rise time, measured at the input, and the rise time, measured at the output.

Fall Time Delay
The fall time of a signal is a measure of the time for the signal to fall from 90% of the ON level to 10% of the ON level. Fall time delay is the difference between the fall time, measured at the input, and the fall time, measured at the output.

Rise-Time-to-Fall-Time Mismatch
This is the absolute value between the variation in the fall time and the rise time, measured at the output.

OUTLINE DIMENSIONS

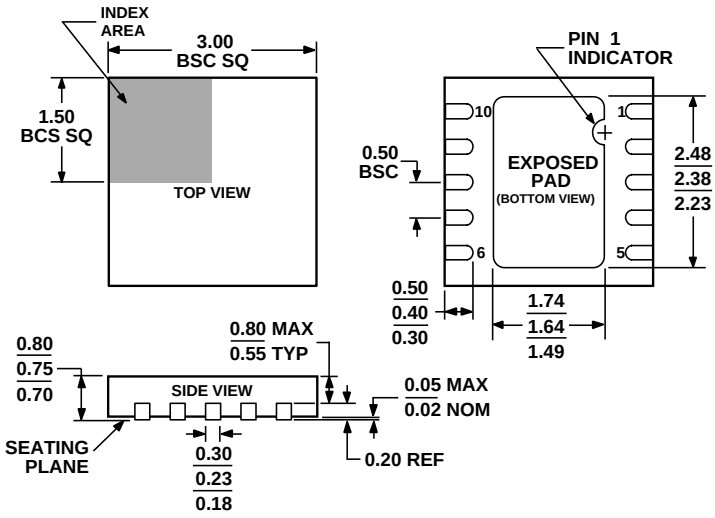
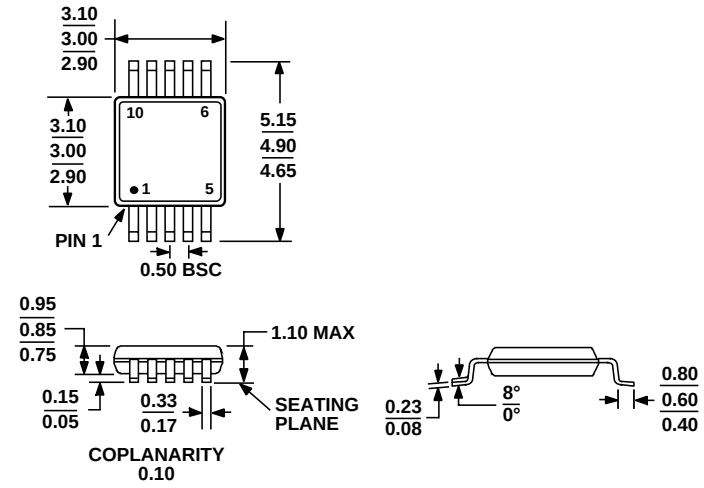


Figure 38. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very, Very Thin, Dual Lead (CP-10-9)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 39. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

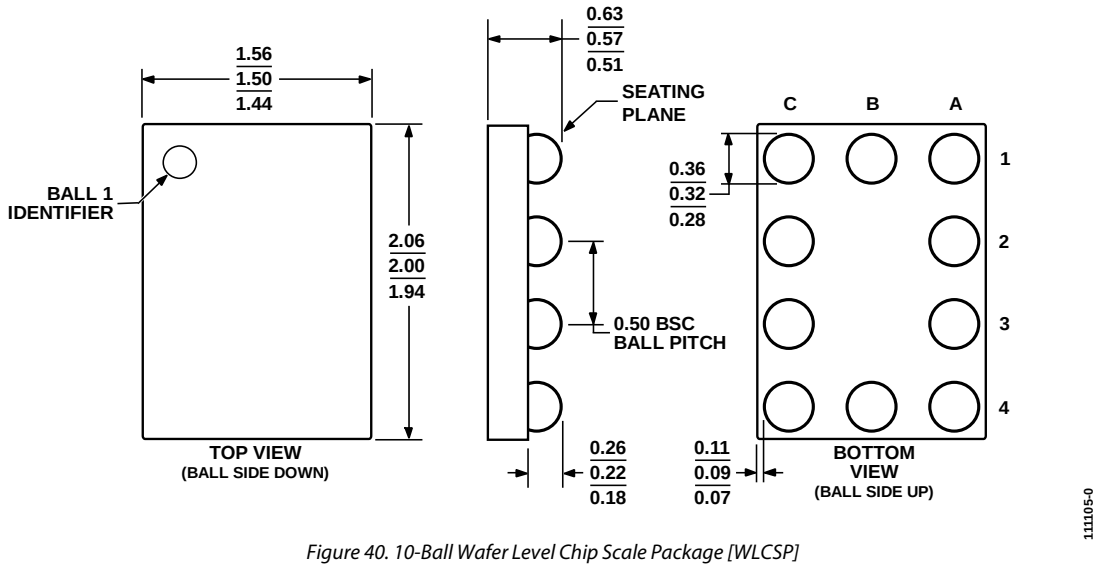


Figure 40. 10-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG787BRMZ[2]	–40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SM1
ADG787BRMZ-500RL7[2]	–40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SM1
ADG787BRMZ-REEL[2]	–40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SM1
ADG787BCBZ-500RL7[2]	–25°C to +85°C	10-Ball Wafer Level Chip Scale Package (WLCSP)	CB-10	S04
ADG787BCBZ-REEL[2]	–25°C to +85°C	10-Ball Wafer Level Chip Scale Package (WLCSP)	CB-10	S04
ADG787BCPZ-500RL7[2]	–40°C to +85°C	10-Lead Lead Frame Chip Scale Package (LFCSP_WD)	CP-10-9	SM1
ADG787BCPZ-REEL[2]	–40°C to +85°C	10-Lead Lead Frame Chip Scale Package (LFCSP_WD)	CP-10-9	SM1

[1] Due to space constraints, branding on this package is limited to three characters.
[2] Z = Pb-free part.

NOTES

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D05250-0-5/06(A)