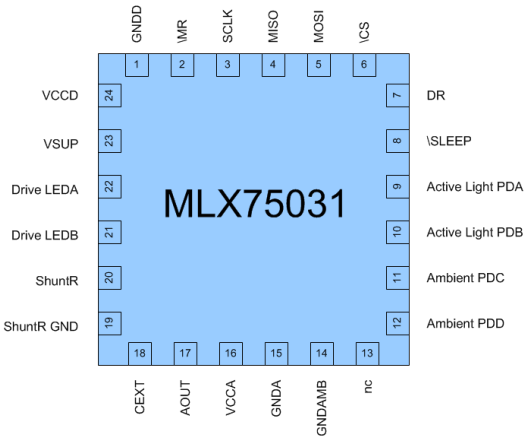
Features & Benefits

- Two independent Active Light measurement channels for proximity sensing and/or gesture recognition
- Integrated DC light cancellation circuitry
- Two logarithmic ambient light channels with two different sensitivities
- Minimum amount of external components
- Stand-by and sleep modes for low power consumption
- Integrated LED drivers
- Integrated battery voltage monitor
- Integrated LED temperature sensing circuitry
- Integrated 16bit ADC for high resolution A2D conversion
- Integrated temperature sensor
- Integrated watchdog timer
- Easy digital communication interface via SPI
- High input capacitance tolerant input current terminals
- High safety design by several diagnostic and monitoring functions

Applications

- Robust Proximity Sensing
- Smart Touch Displays & Panels
- Simple Gesture Detection
- Driver-Passenger Discrimination
- Ambient Light Sensing & Display Dimming

Functional Diagram



Ordering Information

Product Code	Temperature Code	Package Code	Option Code
MLX75031	R (-40°C to 105°C)	LQ (QFN24 4x4)	B
MLX75031	C (0°C to 70°C)	LQ (QFN24 4x4)	B

General Description

The MLX75031 Optical Gesture & Proximity Sensing IC actively controls up to 2 independent Active Light measurement channels. Each channel consists out of one or multiple LEDs, of any type, combined with one or more photodiodes, of any type. Additional Active Light channels can be added through multiplexing. Integrated DC light suppression makes the sensors highly tolerant to background light interference. Primary function is complemented with two integrated ambient light channels. Internal control logic, configurable user registers and SPI communication enable intuitive & programmable operation. Extra features include a watchdog timer, on-board temperature sensor and self-diagnostics are built-in to facilitate robust product design.

The digital output from the Active Light and ambient light channels can be used for proximity and ambient light detection. Gestures such as swipe, zoom, scroll can be recognized by software algorithms that can run on the customer's microcontroller. Reliable communication is assured via an SPI interface.

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1. Functional Block Diagram

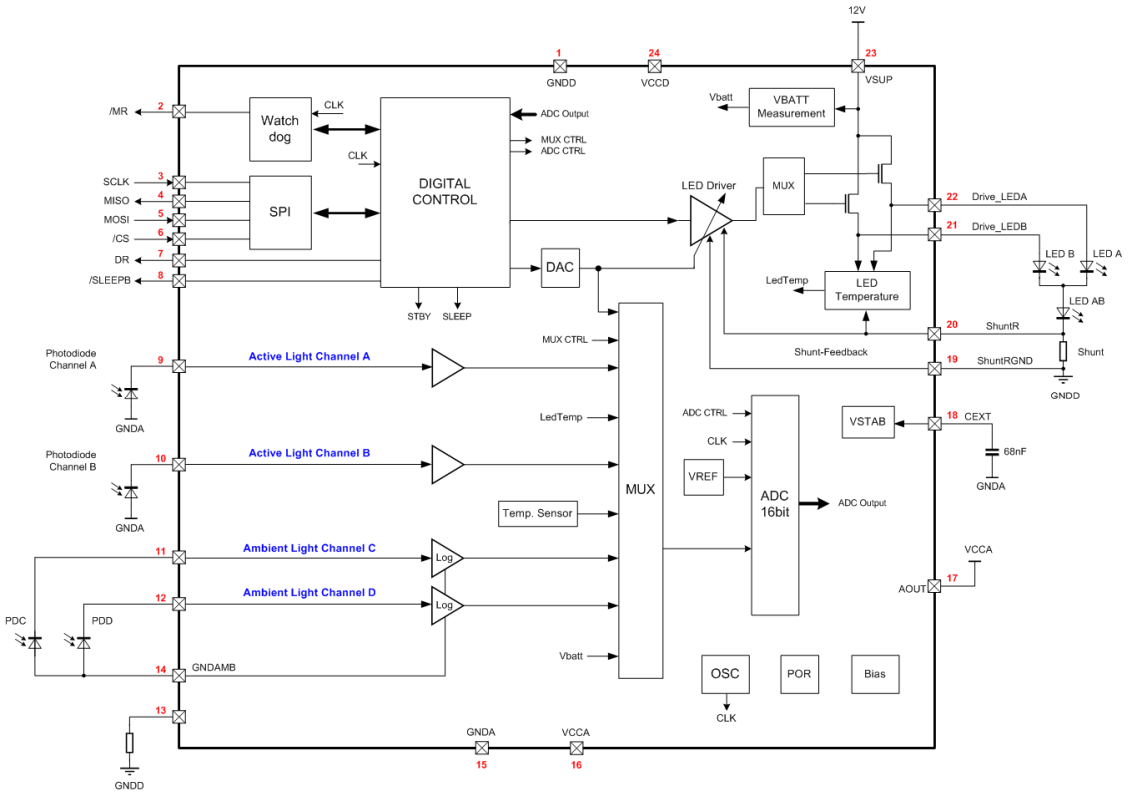


Figure 1 : MLX75031 Functional Block Diagram

2. Device Overview

The MLX75031 Optical Gesture & Proximity Sensing IC independently controls up to 2 Active Light channels. Both channels, A and B, have externally connected photodiodes. External LEDs can be driven up to 150 mA by the built-in LED driver. This current drive capability can also be used to drive a low cost bipolar transistor to increase the peak LED current. The chip synchronizes the pulsing of the LEDs and the exposure time of the Active Light channel photodiodes whereby ambient light and reflected LED light are detected separately. Any spurious light source is subtracted from the Active Light signal. See Section 8.1.

The two logarithmic current sensing channels C and D can be used to measure ambient light over a very wide intensity range. See Section 8.2 for more details.

As auxiliary features, the sensor integrates a watchdog timer, can measure its own temperature, the LED temperature, monitor voltage supply level and perform self diagnostics.
All of this information is available via the SPI interface.
See Section 8.14, 8.3, 8.5.3, 8.5.4 or 8.11.8 for detailed information.

The sensor features sleep and standby modes to save on current consumption. (Section 8.11.2)
The SPI interface is used for data transfer and control of the IC. The timing characteristics are explained in Section 8.11.1 and the interface commands and programmable options in Section 8.11.3 & 8.13.
The sensor is available in both consumer and automotive temperature grades.

3. Glossary of Terms

CR	Chip Reset
CRC	Cyclic Redundancy Check
CS	Chip Select
CSLP	Confirm Sleep
CSTBY	Confirm Standby
DAC	Digital to Analog Converter
DC	Direct Current
DR	Device Ready
EMC	Electromagnetic Compatibility
GNDA	Ground for analog blocks of MLX75031
GNDD	Ground for digital blocks of MLX75031
IR	Infrared
LPF	Low-pass filter
LSB	Least Significant Bit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MR	Master Reset
MSB	Most Significant Bit
MUX	Multiplexer
NOP	No Operation
NRM	Normal Running Mode
OSC	Oscillator
OTR	Optical transfer ratio
POR	Power on reset
RCO	RC-Oscillator
RO	Read-Out
RR	Read Register
RSLP	Request Sleep
RSTBY	Request Standby
SCLK	SPI Shift Clock
SM	Start Measurement
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TIA	Transimpedance Amplifier
VCCA	Supply Voltage for the analog blocks
VCCD	Supply Voltage for the digital blocks
VSENSE	Voltage across the shunt resistor
WDT	Watchdog Timer
WR	Write Register
uC	Microcontroller

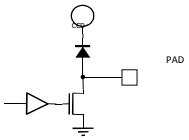
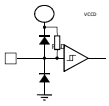
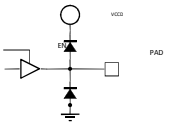
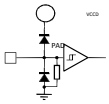
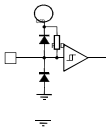
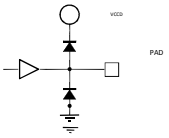
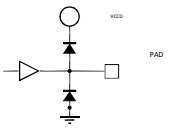
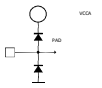
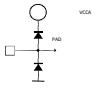
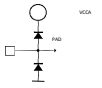
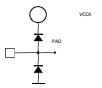
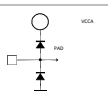
4. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Units
Supply Voltage range	VCCD, VCCA		-0.3	5.0	V
Battery Supply Voltage range	VSUP	t<400ms, no functionality, only during load dump t<2min, functional, not guaranteed to be within specifications	-0.3 -0.3	40 28	V V
Voltage range Drive_LEDA and Drive_LEDB			-0.3	5.5	V
Voltage range on all pins except VCCD, VCCA, VSUP, Drive_LEDA, Drive_LEDB			-0.3	V(VCCD)+0.3 V(VCCA)+0.3	V
Terminal current	Iterminal ILED	per bondpad Battery connection	-20 -20	+20 +155	mA mA
Storage temperature	Tstg		-40	+150	°C
Junction temperature	Tj			+150	°C
ESD capability of any pin (Human Body Model)	ESDHBM	Human body model, acc. to AEC-Q100-002 Rev D	-2	+2	kV
ESD capability of any pin (Charge device model)	ESDCDM	Charge device model acc. to AEC- Q100-011 Rev B	-500	+500	V
Maximum latch–up free current at any pin	ILATCH	JEDEC- Standard EIA / JESD78	-100	+100	mA

Table 1 : Absolute maximum ratings

Note : Exceeding the absolute maximum ratings may cause permanent damage.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5. Pin Definitions & Descriptions

Pin №	Name	Functional Schematic	Type	Function
1	GNDD		Ground	Ground
2	\MR		Digital Open DActive Light Output	Master Reset
3	SCLK		Digital Input with pull-up	SPI Shift Clock
4	MISO		Digital push-pull Output with Tri-state	SPI Data Output
5	MOSI		Digital Input with pull-down	SPI Data Input
6	\CS		Digital Input with pull-up	Chip Select
7	DR		Digital push-pull Output	Device Ready
8	\SLEEPB		Digital push-pull Output	Sleep Detect
9	Active Light PDA		Analog Input	IR Photo Diode A
10	Active Light PDB		Analog Input	IR Photo Diode B
11	Ambient Light PDC		Analog Input	Ambient Light Photo Diode C
12	Ambient Light PDD		Analog Input	Ambient Light Photo Diode D
13	n.c		Analog Input	Test Pin, connect to ground via a resistor

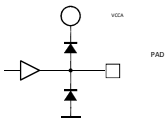
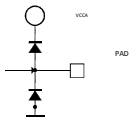
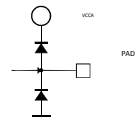
14	GNDAMB		Analog I/O	Ground Ambient Light Channels
15	GNDA		Ground	Ground
16	VCCA		Supply	Regulated Power Supply
17	AOUT		Analog I/O	Test Pin, connect to VCCA
18	CEXT		Analog Input	External blocking Cap, connected to GNDA
19	ShuntRGND		Analog Input	Shunt resistor feedback to Ground
20	ShuntR		Analog Input	Shunt resistor feedback
21	Drive_LEDB		Analog Output	IR LED Emitter B
22	Drive_LEDA		Analog Output	IR LED Emitter A
23	VSUP		Supply	LED driver supply
24	VCCD		Supply	Regulated Power Supply

Table 2 : Pin definitions and descriptions

Note : Pins of measurement channels that are not used, can be left unconnected.
However, this can lead to an error indicated by the corresponding error flags in the Error register.

6. General Electrical Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage range	VDD	VCCD and VCCA pin	3.135	3.3	3.465	V
Supply current (active mode)	IDD	I(VCCD)+I(VCCA) without photodiode DC current			6	mA
Supply current (standby mode)	IDD_STBY	I(VCCD)+I(VCCA)			350	uA
Supply current (sleep mode)	IDD_SLP	I(VCCD)+I(VCCA) without SPI communication			30	uA
Battery supply voltage range	VSUP	VSUP pin	6		18	V
Battery supply current (active mode)	IVSUP	I(VSUP) with Active Light pulses I(VSUP) without Active Light pulses	0 0		155 0.1	mA mA
Battery supply current (standby mode)	IVSUP_STBY	I(VSUP)	0		10	uA
Battery supply current (sleep mode)	IVSUP_SLP	I(VSUP)	0		10	uA
Operation Temperature	TA		-40		105	°C

Table 3 : Electrical specifications

7. Sensor Interface Specific Specifications

The following characteristics are valid over the full temperature range of T_A = -40°C to +105°C and a supply range of VSUP = 6.18V and VCCD = VCCA = 3.135..3.465V unless otherwise noted.

Active Light Channels (Photodiode A & B)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Optical transfer ratio	$OTR = \frac{I_{LED}}{I_{PD}}$		30		12000	
DC sunlight current in the photodiode	I_{sun}		0		900	µA
Fast full scale transition at I_{sunmax}	$t_{sunrise}$		3.5			ms
Min. relative active light modulation (referred to received IR signal)	$\frac{\Delta I_{PD_min}}{I_{PD}}$	- 20 µs LED pulse - PD pulsed current ≥ 20µA, - 25°C - DC sun constant - response per channel 2.5ms		1	5 (*)	%
Dynamic range of active light events (referred to received IR signal)	$\Delta I_{ActiveLight}$				80	%
Active light repetition time Acive light measurement channel A, channel B	$t_{rep_activelight}$			2.5 2.5		ms ms
LED pulse duration range	t_0	selectable via register	15-8%		30+8%	µs
Max. input capacitance PDA & PDB	C_{PDA}, C_{PDB}				80	pF
DC light measurement range	I_{DC} range		0		900	µA
DC light measurement offset	I_{DC} offset	I_{DC} = 0uA & VDD=3.3V	1360	1960	2460	LSB
DC light measurement slope	I_{DC} sens		28	35	44	LSB/µA
DC light measurement inearity error		I_{DC} range: 0uA -> 900uA		5	8	%
DC light measurement word length				16		Bit
DC light measurement noise		for averaging of 8 measurements		3		Bit
Error condition Err_TIA						
Critical error detected on TIA output, if TIA output outside 1.1V+/- (0.65 … 0.75V)						

Table 4 : Active Light Channels Specification

(*) The 5% is really worst case condition, i.e. with OTR = 30 and Rshunt = 1Ohm, this condition is not realistic and should be avoided in a the application

Table 5 : Ambient Light Channels Specifications

Ambient Light Channels (Photodiode C & D)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Input current range for detector C	Iambc	Detector C	0.01		1040	uA
Input current threshold level	Iambc_detect	Detector C	333			nA
Input capacity on ambient PDC	Cambc	at 1V, Detector C			1	nF
Input current range for detector D	Iambd	Detector D	0.002		20	uA
Input current threshold level	Iambd_detect	Detector D	22			nA
Input capacity on ambient PDD	Cambd	at 1V, Detector D			100	pF
Transfer function logarithmic	Vamb	See Section 8.2.2				
Output Ambient Channel C		At VDD=3.3V, Iin=100uA	30464	32768	37376	LSB
Output Ambient Channel D		At VDD=3.3V, Iin=10uA	30464	32768	37376	LSB
Slope Ambient Channel C		At VDD=3.3V and 105°C	5300	5900	6500	LSB/dec
Slope Ambient Channel D		At VDD=3.3V and 105°C	5300	5900	6500	LSB/dec
Ambient Channels Linearity Error		for Iin ≥ Iambx_detect		3	5	%
Ambient light word length				16		bits
Ambient light channel accuracy		for averaging of 16 measurements		13		bits
Ambient light response time		See Section 8.2.4 for a detailed explanation of this parameter. for Iin ≥ Iambx_detect			3	ms
Ambient light measurement repetition rate			10			ms
Error condition Err_Amb						
Err_Amb it is set if the output common mode of one ambient channel SC filter is out of range (meaning > 55% of VCCA for each of the differential outputs).						

Table 6 : Temperature Sensor Specification

Die Temperature Sensor						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Temp. sensor range	ϑ		-40		105	°C
Temp. sensor transfer function (*)	Vϑ	At VDD=3.3V	-82	-67	-51	LSB/K
Temp. sensor output	V@85°C	At VDD=3.3V and full Calib 1/2 ranges	5990	8096	10203	LSB
Temp. sensor error	ϑerror@30°C	At VDD=3.3V			±3	°C
Temp. response time	tresp_ϑ				1	s
Temp. sensor word length				16		bits
Temp. sensor noise		for averaging of 16 measurements		3		bits

(*) This value will be stored in the Calib1 Register.

LED Driver						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
LED pulse current		Shunt=1 Ω	1		150	mA
Shunt resistor values		The minimum VSUP voltage is affected by the drop across the shunt resistor	1		6.6	Ohm
Shunt voltage			1		993	mV
Rising and falling time		1tau settling time, programmable via Rise<1:0>		1..7		us
DC offset level		Shunt bias voltage before transmitting the current pulse		1		mV
Time before pulse	Tdc_pulse	Biasing time of the LED driver (Shunt voltage = DC offset level) before pulse transmission. See Section 8.13.0 for details.		200		us
Error condition Err_Drv						
Err_Drv difference between Vdac and Vsense. Detection level larger 200mV						

Table 7 : LED Driver specification

Table 8 : Power on Reset specification

POR						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
POR off threshold voltage	VPOR-ON		1.8		2.85	V
POR on threshold voltage	VPOR-OFF		1.7		2.75	V
POR hysteresis voltage	VHYS			150		mV

VSup Voltage Monitor						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
VSUP Measurement Range			5		20	V
VSup Low threshold voltage	VTSUPL	Default VSUPLOW<1:0>		6		V
VSup Low hysteresis	VTSUPL_hys			1		V
VSup High threshold voltage	VTSUPH			20		V
VSup High hysteresis	VTSUPH_hys			1.8		V
Gain error	VTgain_err				+/-2	%
Offset error	VToffset_err				+/-50	LSB
Voltage Monitor Noise		for averaging of 16 measurements		3		bits

Table 9 : VSup Voltage Monitor specification

SPI						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
SPI word length					8	bit
High-level input voltage	VIH		0.7VDD		VDD	V
Low-level input voltage	VIL		0		0.3VDD	V
Hysteresis on digital inputs	VHYST			0.28		V
High output voltage (not on pin MR)	VOH	CL=30pF	0.8VDD		VDD	V
Low output voltage (not on pin MR)	VOL	CL=30pF	0		0.2VDD	V
Input leakage	ILK		-10		10	µA
Tri-state output leakage current	IOZ		-10		10	µA
Input capacitance, per pin	CIN			10		pF
Pull up resistance of SCLK and \CS Pin	RPU	PD -> leakage to VCCD (causing a voltage drop across the PD resistor)		50k		Ohm

Pull Down Resistance of MOSI Pin	RPD	PU -> leakage to GNDD (causing a voltage drop across the PU resistor)		50k		Ohm
Output voltage Low, Pin MR	VOutL	IODC = 2mA			0.1	V
Start-up time after power-on	tstartup		-8%	20	+8%	ms
Start-up time after power-on only for SPI	tstartupSPI				10	µs
Start-up time after wake-up from sleep	twakeup_slp		-8%	20	+8%	ms
Start-up time after wake-up from standby	twakeup_stby		-8%	20	+8%	ms
SPI Clock Frequency	fSCLK = 1/tSCLK		0.5	1	5	MHz
Frequency of Internal RC Oscillator	fRCO = 1/TRCO		-8%	2.5	+8%	MHz
CS low prior to first SCLK edge	tcs_sclk		50			ns
CS high after last SCLK edge	tsclk_cs		50			ns
CS high time between transmissions	tcs_inter		50			ns
Time between CS high and DR low (*)	tcs_dr		0		22.47 (239us)	µs
WDT initial active window time	twdt_init	After POR, Watchdog Reset and Wake-Up	-8%	140	+8%	ms
WDT open window time	twdt_open		-8%	70	+8%	ms
WDT closed window time	twdt_closed		-8%	70	+8%	ms
MR low time during reset	tMR	After Watchdog Reset	-8%	2	+8%	ms
SLEEPB low after CS high	tsleepb	After CSBTY/CSLP command	0	1.2		µs
Error condition Err_RCO						
RCO stuck at High or Low						
Error condition Err_Vref						
Internal voltage regulator : Err_Vref is set if the regulator does not start (detection threshold in the range [1V;2V])						

Table 10 : SPI specification

(*) with random measurement start, the max time can be up to 239us, if an auto-zeroing phase of the IC is executed.

8. Detailed General Description

8.1. Active Light Channels A & B

The MLX75031 has two separate Active Light channels. Both channels work synchronously & independently. These channels are able to detect the amplitude/intensity of a reflected signal whilst subtracting the DC variation of the background light or sunlight illumination.

The LEDs transmit one single light pulse (pulse duration is programmable via TP<2:0>) which is detected by the channel receiver. The pulse amplitude is sampled and amplified by a S&H stage synchronized with the LED pulse.

In addition to the LED pulse amplitude programming, the effective trans-impedance can be adjusted in order to maximize the dynamic range of the system.

The calibration to find the best working point should be calculated and set by means of the µController over the SPI interface.

8.1.1. Transimpedance Amplifier (TIA)

The transimpedance amplifier converts the photocurrent of the connected photodiode into a voltage signal.

The overall transfer function for the Active Light channels is defined by following formula :

$$I_{pd} = \frac{\left(\frac{ADC_ActiveLight}{65535} - \frac{1}{2}\right) \times 3.3 + 1.45 \times GAIN_BUF}{0.02 \times GAIN_ADJ \times GAIN_BUF \times k}$$

- I_{pd} : the current through the photo diode (in µA)
- ADC_ActiveLight : the decimal value of the Active Light measurement (see Output Data Frame of read-out)
- GAIN_BUF : the gain value selected by the GainBuf register
- GAIN_ADJ : the gain value selected by the SetAL or SetBL register
- k : Factor causing by signal attenuation from TIA. Range from 50% - 90%.

The TIA's DC-light cancellation circuitry delivers a 16bit value of the received (external) DC light.

8.1.2. Active Light Channel DC Light Measurement

The DC current compensation circuitry of the transimpedance amplifier is able to supply and measure the DC current supplied to the photodetector. Both Active Light channels are identical in structure.
In order to reach a feasible resolution in the current range of interest (low currents in the range up to 900uA), the measurement characteristics will saturate for currents above the IDC current range, however the compensation circuit is nevertheless able to supply the specified current levels to the detector (up to 900uA). The given ADC word length for the Active Light channel DC light data is 16bit.

The typical transfer function of DC measurement is defined by formula:

$$I_{pd_DC} = \frac{ADC_DC - 1760}{35}$$

I_{pd_DC} : The DC current through photo diode (in uA).
ADC_DC : the decimal value of the DC measurement (see Output Data Frame of read-out).

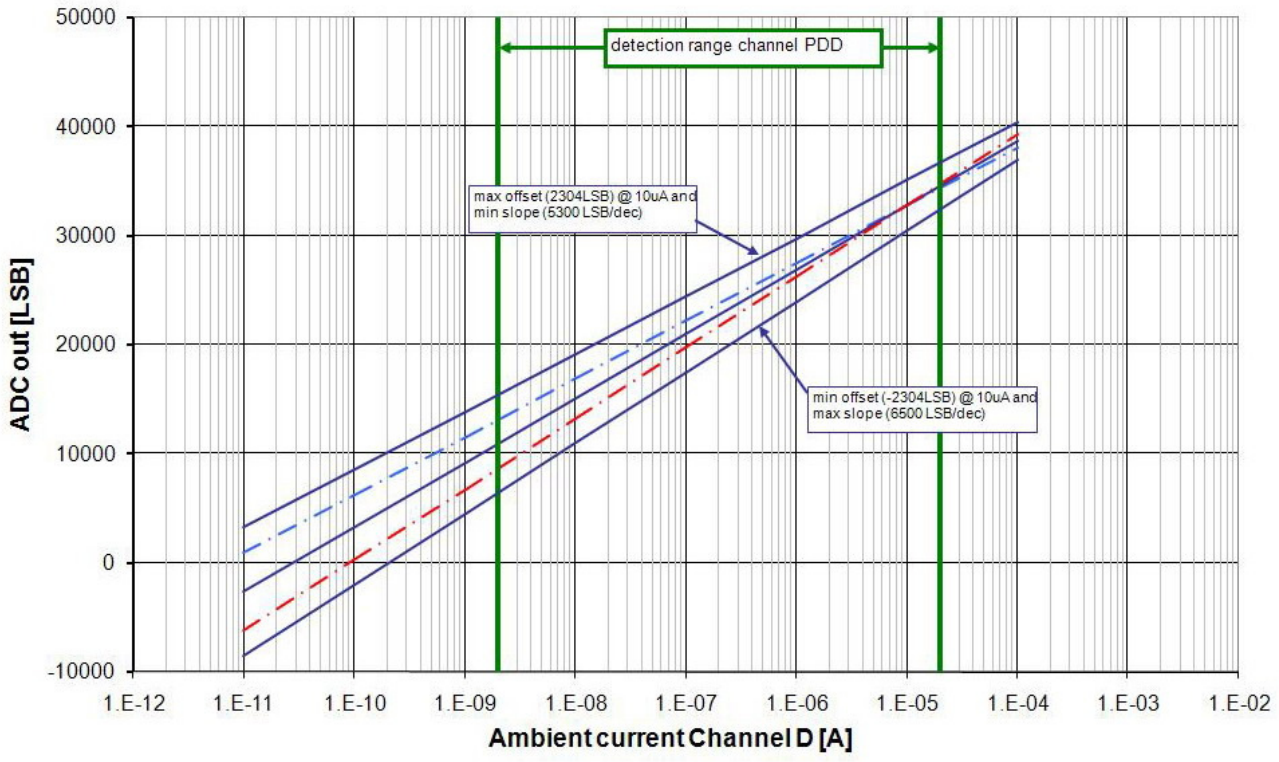
8.2. Ambient Light Sensor

8.2.1. Normal Operation

The ambient light detection system of the MLX75031 consists of two independent channels C & D and an on-chip controllable dedicated ground pin GNDAMB. GNDAMB is internally set to GNDA in normal operation. An external photodiode is connected in between each channel and GNDAMB. The Base-Emitter diode of a bipolar transistor generates a logarithmic transfer function from the incoming photocurrent to an internal voltage. Please refer to the MLX75031 EMC guidelines to improve the EMC resistance of the ambient channels

8.2.2. Logarithmic Transfer Function

Following graphs show the input current to output ADC value characteristic of each ambient channel.



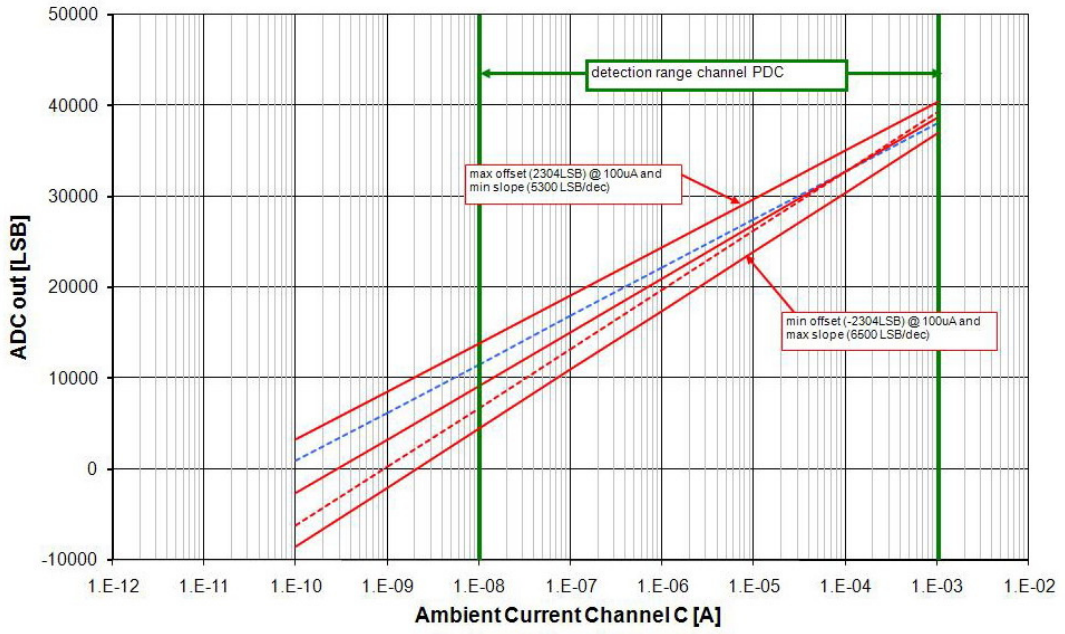


Figure 2: Input-to-output characteristic of each ambient channel at 3 different temperatures

8.2.3. Calibration & Temperaure Compensaion

The output of each ambient channel has a strong temperature dependence and a slight process dependence that can be compensated at run time. This is shown in following equation (channel x, x = C, D) :

$$I_x = \left(1 + TC_{Iref}\,\Delta T\right)\left(1 + \alpha\frac{O_x}{300^2}\Delta T\right)\mathrm{e}^{\alpha\left(\frac{ambout_x - 2^{15}}{T}\right) + \beta} \qquad (1)$$

- I_x: calculated input light value
- $ambout_x$: 16-bit ADC converted value of the ambient channel
- TC_{Iref}: temperature coefficient of the reference current (typ. Value = +1230ppm/K)
- O_x: offset of the internal amplifiers (digital value)
- α_x, β_x: calibration values for channel x (see below)

During calibration at least 2 light levels (I_{x1} and I_{x2}) have to be supplied to the target ambient channel (x) with its photodiode at the same known temperature T. The closer these values are chosen to the range used in application, the more accurate the final result will be. During the setting of these two light levels, the output of ambient channel x: $ambout_{x1}$ and $ambout_{x2}$ are measured. This results in 2 equations and 2 unknowns: α_x and β_x. Both unknowns can be calculated from following formulas :

$$\alpha = \frac{T \ln\left(\frac{I_1}{I_2}\right)}{ambout_1 - ambout_2} \quad \text{and} \quad \beta = \ln\left(\frac{I_1}{1}\right) - \alpha\left(\frac{ambout_1 - 2^{15}}{T}\right) \qquad (2)$$

Note : these 2 values automatically correct any gain error of the connected photodiode and used lens system.

After the calibration step, some error remains when the temperature deviates from the calibration temperature. The error depends on the temperature drift of the reference current ($TC_{Iref}\Delta T$) and on the offset Ox. In second order, it also depends on the temperature drift of gain G and of the offset Ox.

With TC_{Iref} = + 1230 ppm/K, the ambient current calculation error because of the temperature drift of I_{ref} is from -10% at low temperature to +10% at high temperature.

The offset of the ambient signal conditioning chain is between 0 and -20mV (400 LSB). The corresponding temperature coefficient would be between 0 and -670 ppm/°C. The corresponding error in the ambient light calculation would be from 0 to -5.3%.

To reduce the MCU load a simple lookup table can be implemented instead of the complete formula.

8.2.4. Response Time

During operation, each ambient channel constantly shows a logarithmic output response towards the input current that is applied. As a result, the time for the output to respond on a changing input current is defined by a strongly non-linear function (similar but not equal to an RC-curve). Therefore a threshold crossing criterion is used to define the time response.

The light threshold level is defined as a border between light and dark. This threshold can be defined as a light level of a voltage level at the output of the ambient light channel. If the light suddenly crosses the defined light threshold, the output of the ambient light channel will cross the corresponding voltage threshold with a delay. This delay is the response time.

Figure 3 shows an example of such a threshold crossing. An input current step is used as this represents the worst case condition. Note that starting from an input current level that is close to the threshold, the end requirement of 20% below or 80% above can be heavily relaxed.

The ambient light response time is valid for any threshold level equal to or above the defined input threshold level I_{ambx_detect} of any input channel.

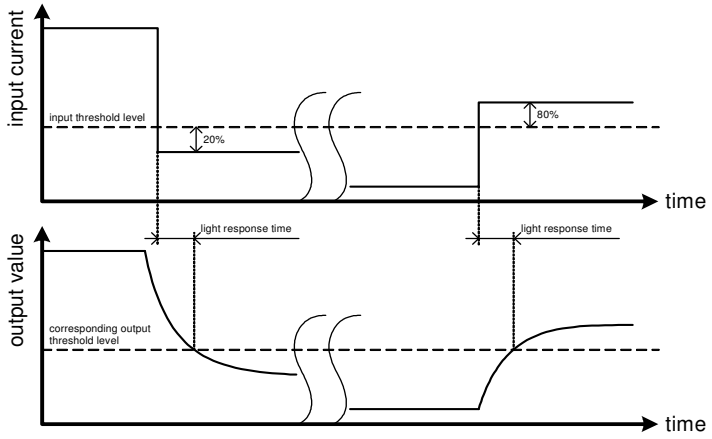


Figure 3 : Ambient response time explanation

8.2.5. Diagnostics Mode Operation

In diagnostics mode, the status of the external photodiodes is checked.
A set of switches controls the different possible error conditions by running through the different tests. At the end of this check, all switches go back into the initial position to allow normal ambient light detection.

Table 11 lists the possible error modes for detector C and pin GNDAMB.
The error modes for detectors D are equivalent.

Failure	Detected	How
detC disconnected	Diagnostics	If checkC == 0: error!
GNDAMB disconnected	Diagnostics	Identical test as detC disconnected.
detC shorted to GNDA/GNDD/GNDAMB	normal mode	• Ambient detector shows incredible high light input • ADC response is much likely saturated, anyway the output is far beyond the allowed operation range
	Diagnostics	If checkC == 0: error!
detC shorted to VCCA/VCCD	Diagnostics	If checkC == 1: error!
GNDAMB shorted to GNDA/GNDD	Various	• This is no problem for normal operation • This CAN be a problem in testmode if short is strong and pin GNDAMB pulled to VDDA: a maximum current of 50mA can be pulled during 10µs • If so, test for detC disconnected will show an error
GNDAMB shorted to VCCA/VCCD	normal mode	A maximum current of 800mA can be pulled from this driver
	Diagnostics	If the current can be supplied by the module, an error will be flagged similar to detC shorted to VCCA/VCCD
detC shorted to detD	Diagnostics	• If checkC == 0: error! • If checkD == 1: error!

Table 11 : List of possible failures on the ambient pins – projected on channel C.

Note that in spite of the ability to detect any error by the ambient diagnostics, an error on an ambient pin might still have other unwanted effects.

-

- Shorting any channel to GNDA/GNDD/GNDAMB will make the readout of the whole ambient block useless. At this time a maximum current of 14mA might be constantly pulled from the supply, independent of the amount of channels that is shorted to GNDA/GNDD/GNDAMB.
- During normal operation, node GNDAMB should be considered a ground pin. Shorting this pin to any other voltage might result in a shortcurrent of max 800mA!
- Because of such unwanted effects, a detection of an error in diagnostics mode should be followed by a disabling of the ambient channels in order to avoid disturbing the operation of other blocks in the system.
- Note that unused channels should be connected with an external resistance (~60kOhm) to GNDAMB. Doing so will avoid disturbing the other channels, but will give a constant error on the channel connected to GNDAMB.

8.3. Temperature Sensor

The on-chip temperature sensor measures the IC temperature. The output voltage of the sensor is converted by the 16-bit ADC. The sensor will be trimmed for the best result during the production. This trimming value is not applied to the temperature sensor internally, but is available to the customer through two on-chip registers Calib1 and Calib2, see 0. The Calib1 register contains the slope of the temperature curve in LSB/K. The Calib2 register contains the offset of the curve at a defined temperature at which the chip is tested in production. An exemplary plot for the temperature sensor is given in
Figure **4** : Temperature sensor exemplary graph.

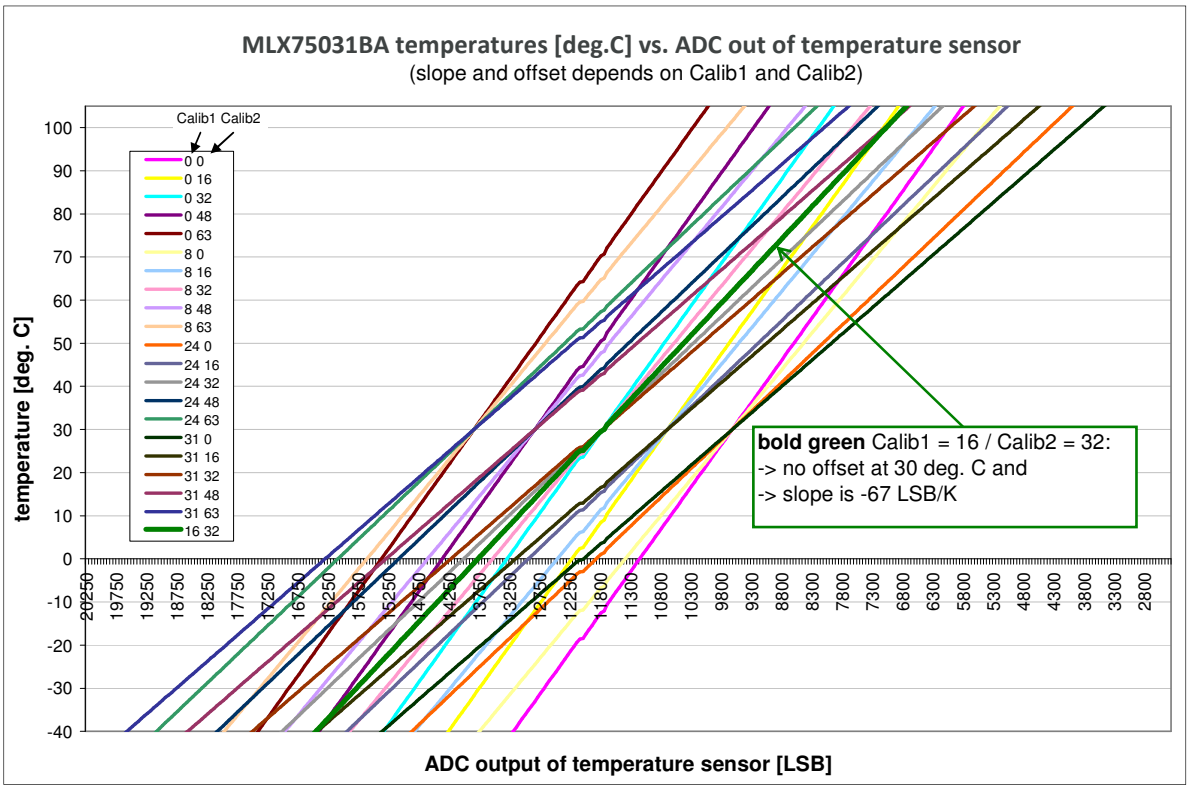


Figure 4 : Temperature sensor exemplary graph

The temperature is calculated from the temperature readout (*tempout*) and the gain and offset calibration data (calibration data measured at 30°C) according to the formula :

$$T_K = 303.15K + \frac{(11781 + 67(calib2 - 32)) - tempout}{67 + (calib1 - 16)} \text{ K}$$

or in °C:

$$T = 30°\text{C} + \frac{(11781 + 67(calib2 - 32)) - tempout}{67 + (calib1 - 16)} \text{ °C}$$

- tempout : digital temperature readout (16Bit)
- calib1 : contents of calib1 register (5Bit)
- calib2 : contents of calib2 register (6Bit)

8.4. Analog to Digital Conversion

The ADC converts all MUX signals in a 16 bit word which is passed in a register in the digital block and can be read out through the SPI interface.

8.5. Output Stage

8.5.1. DAC

For the MLX75031 Active Light application, the DAC has been designed to generate a pulse voltage signal from 1mV to 1V, so that LED current driven by the LED driver can be 1mA to 150mA, if a 6.6Ω external resistor is used.

A logarithmic DAC was used.
A piece-wise linear DAC with four zones is implemented as approximation for the logarithmic DAC.

DAC piece (DACx[7:6])	Steps in each piece (6LSBs DACx[5:0])	Step size for 1 bit (V)	Trasfer function Vdac (V) =	Range start (V)	Range end (V)
00	64	1.00E-04	1.00E-04*DACx[7:0] + 1.03E-3	1.03E-03	7.43E-03
01	64	5.10E-04	5.10E-04*DACx[7:0] - 2.491E-2	7.56E-03	3.952E-02
10	64	2.52E-03	2.52E-03*DACx[7:0] - 2.820E-01	4.022E-02	1.988E-01
11	64	1.224E-02	1.224E-02*DACx[7:0] - 2.145	2.057E-01	9.769E-01

Table 12 : The DAC voltage values based on the DAC codes (DACx[7:0], x=A or B) at VDD=3.3V

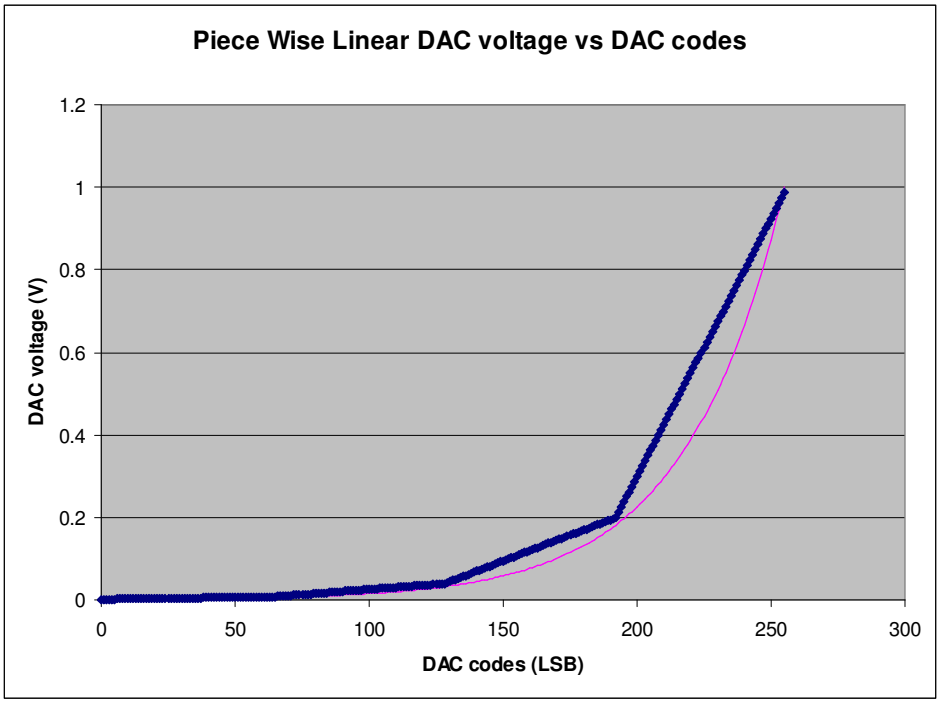


Figure 5 : Piece Wise Linear DAC voltage vs DAC codes

8.5.2. LED Driver

The LED driver mainly contains one operational amplifier and transistors able to drive the external LEDs.
Its task is to set the voltage over the external Rshunt equal to the voltage generated by DAC, so the corresponded current (Vdac/ Rshunt) is flowing through LED.

The error flag Err_Drv is set high if the LED current regulation loop is broken (disconnected LED or shunt resistor).

8.5.3. LED Forward Voltage Measurement

When the current pulse is flowing through the LED, the voltage drop across the LED (between pin Drive_LEDA/B and pin ShuntR) is sampled and then held for later ADC conversion.
This value can be used to estimate the LED temperature.
The sampling occurs synchronously with the Active Light signal sampling.

The overall transfer function for the LED temperature sensing is defined by following formula:

$$V_{LED} = \frac{(ADC_LEDTEMP - 32768) \times 6.64}{65535 \times G_ADJ_LED} + 2 \times OS_ADJ_LED$$

- V_{LED} : the voltage between pin Drive_LEDA/B and pin ShuntR (in V)
- ADC_LEDTEMP : the decimal value of the LED temperature measurement (see Output Data Frame of read-out)
- G_ADJ_LED: the gain value selected by the SetPLS register
- OS_ADJ_LED: the offset value selected by the SetPLS register (in V)

Due to different LED types and LED connections, the gain G_ADJ_LED and OS_ADJ_LED shall be set such that the measurement range fits the application the best way.

Minimum V_{LED} measurement resolution is typical 0.5mV.

8.5.4. Battery Supply Voltage Measurement & Monitoring

The voltage on the *VSUP* pin is continuously monitored. In case the voltage on the pin goes above 20V typical, the error flag Err_VsupH will be set and the LED driver will be shut off. Active Light measurements can still be executed but the LED driver will be disabled as long as VSUP > 20V typical, protecting the LED's from being damaged.

The error flag Err_VsupL will be set when the voltage on *VSUP* goes below the threshold defined by the two bits VSUPLOW<1:0>. The LED driver will remain active. Active Light measurements are still possible.

In Figure 6 the definition of the thresholds is shown. It is indicated when the certain error conditions are present and when the error flags are set.

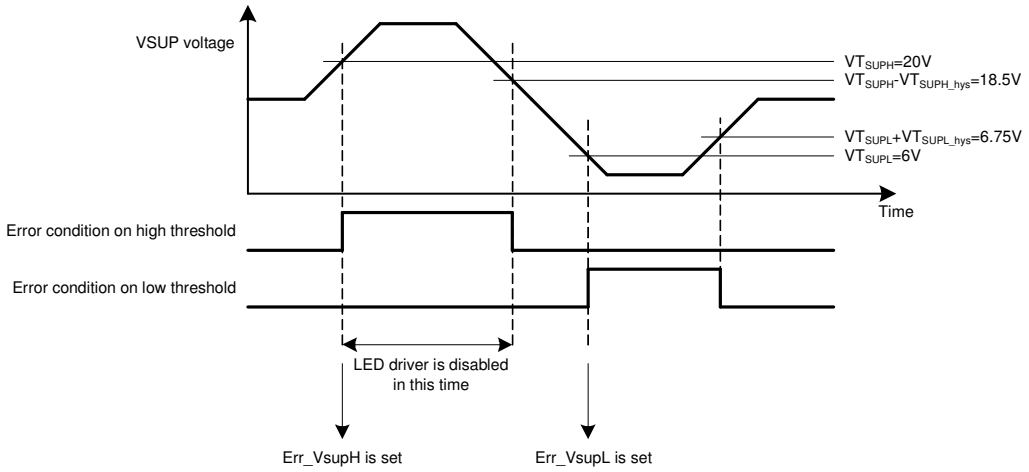


Figure 6 : Threshold definitions of VSUP monitoring block

Besides this continuous monitoring, it is possible to do a VSUP voltage measurement on request.
This is included in the Measurement Sequence 1 of the Start Measurement command.
Please refer to Section 8.11.4 for more information.

The overall transfer function for the VSUP measurement is defined by following formula :

$$V_{SUP} = \frac{16.6 \times ADC_VSUP}{13107}$$

- V_{SUP}: the voltage on the pin VSUP (in V)
- ADC_VSUP: the decimal value of the VSUP measurement (see Output Data Frame of read-out)

8.6. Power-On Reset

The Power On Reset (POR) is connected to voltage supply.
At power-on the POR cell generates a reset signal before the supply voltage exceeds a level of V_{POR-ON}.
The cell contains a hysteresis of 100mV.

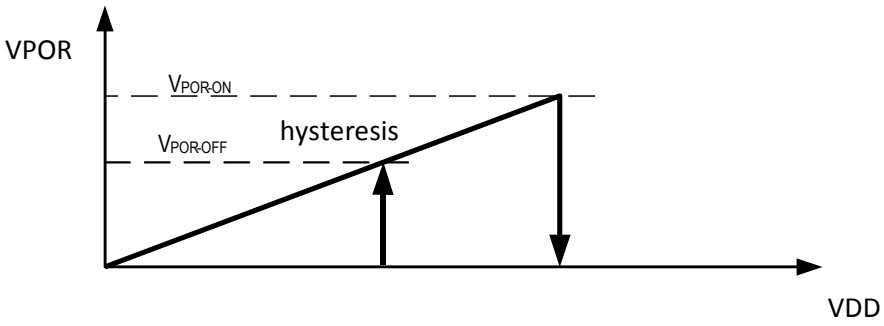


Figure 7 : POR sequence

8.7. Oscillator (RC)

The integrated oscillator has to provide a clock signal to the digital control logic, the watchdog timer and the ADC. The oscillator will run with a frequency at 2.5MHz, all other components with 1.25MHz.
The drift of f_{osc} over temperature and supply voltage is smaller than 8%.
The oscillator can be enabled and disabled when changing the modes (NRM/STBY –SLP). It is active in normal mode and in standby mode. In sleep mode, it is disabled.

8.8. ADC MUX

The ADC multiplexer transfers the various voltages of interest to the AD converter.

8.9. Vstab Analog +Bandgap

This block generates all reference voltages and current sources for the analogue blocks.
These sources work as far as possible independent from the temperature.
The block is also switched off in standby and sleep mode and has a wake up functionality with the smallest possible time.

8.10. Digital Control

The digital control is responsible for all clock and gating signals used within the IC. These signals control the LED drive sequence, the sampling and conversion of the photo-diode inputs, and so on.
The digital control is also responsible for channeling data to and from the SPI interface.

8.11. SPI

8.11.1. General Description of the SPI Interface

After power-on, the sensor enters a reset state (invoked by the internal power-on-reset circuit). A start-up time tstartup after power-on, the internal reference voltages have become stable and a first measurement cycle can start. To indicate that the start-up phase is complete, the DR pin will go high (DR is low during the start-up phase).

The control of this sensor is completely SPI driven. For each task to be executed, the proper command must be uploaded via the SPI. The SPI uses a four-wire communication protocol. The following pins are used:

- **CS** : when CS pin is low, transmission and reception are enabled and the MISO pin is driven. When the CS pin goes high, the MISO pin is no longer driven and becomes a floating output. This makes it possible that one micro-processor takes control over multiple sensors by setting the CS pin of the appropriate sensor low while sending commands. The idle state of the chip select is high.
- **SCLK** : clock input for the sensor. The clock input must be running only during the upload of a new command or during a read-out cycle. The idle state of the clock input is high.
- **MOSI** : data input for uploading the different commands and the data that needs to be written into some registers. The idle state of the data input is low.
- **MISO** : data output of the sensor.

A SPI timing diagram is given in Figure 8. This is the general format for sending a command. First the CS pin must be set low so that the sensor can accept data. The low level on the CS pin in combination with the first rising clock edge is used to start an internal synchronization counter that counts the incoming bits. Data on the MOSI pin is clocked in at the rising clock edge. Data on the MISO pin is shifted out during the falling clock edge. Note that the tri-state of the MISO pin is controlled by the state of CS.
After uploading a command, the CS pin must be set high for a minimum time of tcs_inter in order to reset the internal synchronization counter and to allow new commands to be interpreted.

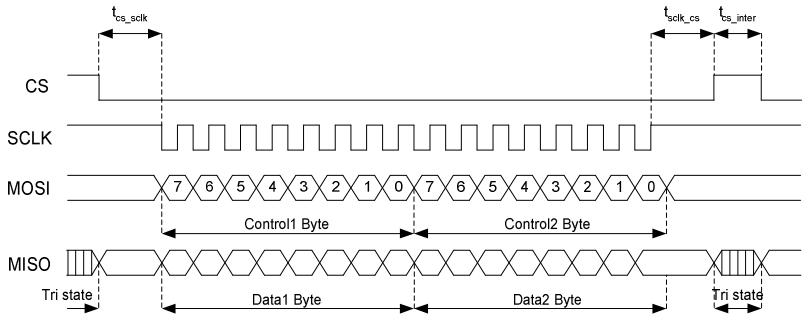


Figure 8 : SPI Timing Diagram for 2 byte instructions

The basic structure of a command consists of 2 bytes: the Control1 Byte and the Control2 Byte that are uploaded to the device and the Data1 Byte and the Data2 Byte that are downloaded to the micro-controller. Exceptions are the commands needed to read and write the user registers (WR/RR). These commands need 3 bytes. The timing diagram is given in Figure 9.

All data transfer happens with MSB first, LSB last. Referring to Figure 8 and Figure 9 within a byte, bit 7 is always defined as the MSB, bit 0 is the LSB. This applies to all data transfers from master to slave and vice versa.

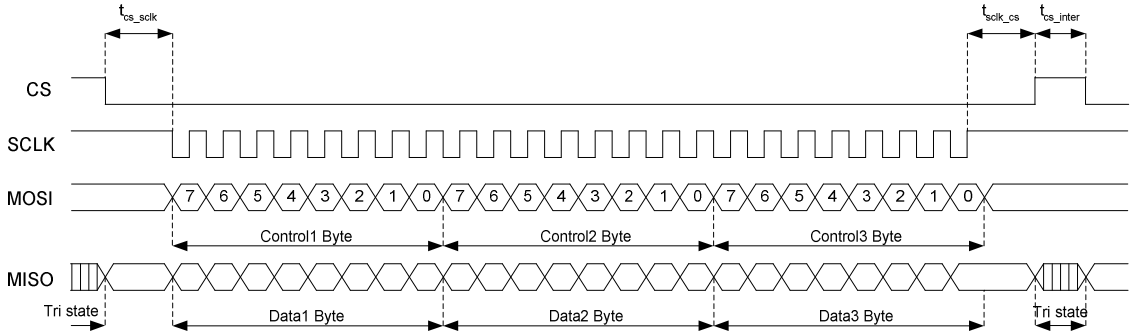


Figure 9 : SPI Timing Diagram for 3 byte instructions

The MSB of the Control1 Byte (bit 7) is a command token: setting this bit to 1 means that the Control1 Byte will be interpreted as a new command. If the MSB is 0, the next bits are ignored and no command will be accepted. The idle command has a Control1 Byte of 0x00.
The command type (chip reset, watchdog trigger, power mode change, start measurements, start read-out, read/write register) is selected with the next bits 6..0 of the Control1 Byte.
The Control2 Byte consists of 0x00, to allow clocking out the Data2 Byte. The Data2 Byte contains always the Ctrl1 Byte that was uploaded. Thus the micro-controller can check that the Data2 Byte is an exact replica of the Ctrl1 Byte, to verify that the right command is uploaded to the device.

The Data1 Byte contains some internal status flags to allow checking the internal state of the device.
The internal status flags are defined in the table below (Table 13). See section 0 for more information concerning the operation of the status flags.

Status flag	Status when bit is set	Status when bit is clear
Bit 7 (MSB)	Previous Command was invalid	Previous Command was valid
Bit 6..5	Power State: 11 = (reserved) 10 = Normal Running Mode 01 = Stand-by State 00 = Sleep State	
Bit 4	Sleep Request was sent	No Sleep Request available
Bit 3	Standby Request was sent	No Standby Request available
Bit 2	Device is in TestMode	Device is not in TestMode
Bit 1	Internal Oscillator is enabled (Standby Mode or Normal Running Mode)	Internal Oscillator is shut down (Sleep Mode)
Bit 0 (LSB)	Critical Error occurred	No Error is detected

Table 13 : Internal Status Flags as given in the Data1 Byte

Table 14 summarizes the instruction set of the sensor.
A detailed explanation of these different commands is given in Section 8.11.3.

Symbol	Command Description	Control1 Byte	Control2 Byte	Control3 Byte
NOP	Idle Command	0000 0000	0000 0000	N/A
CR	Chip Reset	1111 0000	0000 0000	N/A
WDT	Watchdog Trigger	1001 0011	0000 0000	N/A
RSLP	Request Sleep	1110 0001	0000 0000	N/A
CSLP	Confirm Sleep	1010 0011	0000 0000	N/A
RSTBY	Request Standby	1110 0010	0000 0000	N/A
CSTBY	Confirm Standby	1010 0110	0000 0000	N/A
NRM	Normal Running Mode	1110 0100	0000 0000	N/A
SM	Start Measurement	1101 00R0T	M6..M3 M2M1M0P	N/A
SD	Start Diagnostics	1011 0000	0000 0000	N/A
RO	Start Read-Out	1100 0011	0000 0000	N/A
WR	Write Register	1000 0111	D7..D0	A3..A0 P1P000
RR	Read Register	1000 1110	A3..A0 0000	0000 0000

Table 14 : Instruction set of the Active Light sensor

Besides the above instruction set, there are some test commands available for production test purposes. To prevent unintentional access into these test modes, it requires multiple commands before the actual test mode is entered.

8.11.2. Operation Modes

The MLX75031 can work in three operation modes :

1. <u>Normal mode</u> :
Normal operation is the state during which all internal blocks are powered on (default state after power-on). Measurement sequences and their conversion to digital values are regularly ongoing.
The pin SLEEPB is set high when the device is in Normal mode.

2. <u>Standby mode</u> :
Standby mode is defined as the state in which only the Watchdog and oscillator is active.
The pin SLEEPB is set low when the device is in Standby mode.

3. <u>Sleep mode</u> :
In Sleep mode the complete system is switched off. Only the SPI can work.
The Optical Gesture & Proximity Sensing IC can switch in the normal mode via SPI.
The pin SLEEPB is set low when the device is in Sleep mode.

An overview of modes in which the device can operate is shown in Figure 10 below. It is also indicates which commands are available in the different operation modes and it shows the state of the different flags in the Status Flags byte.

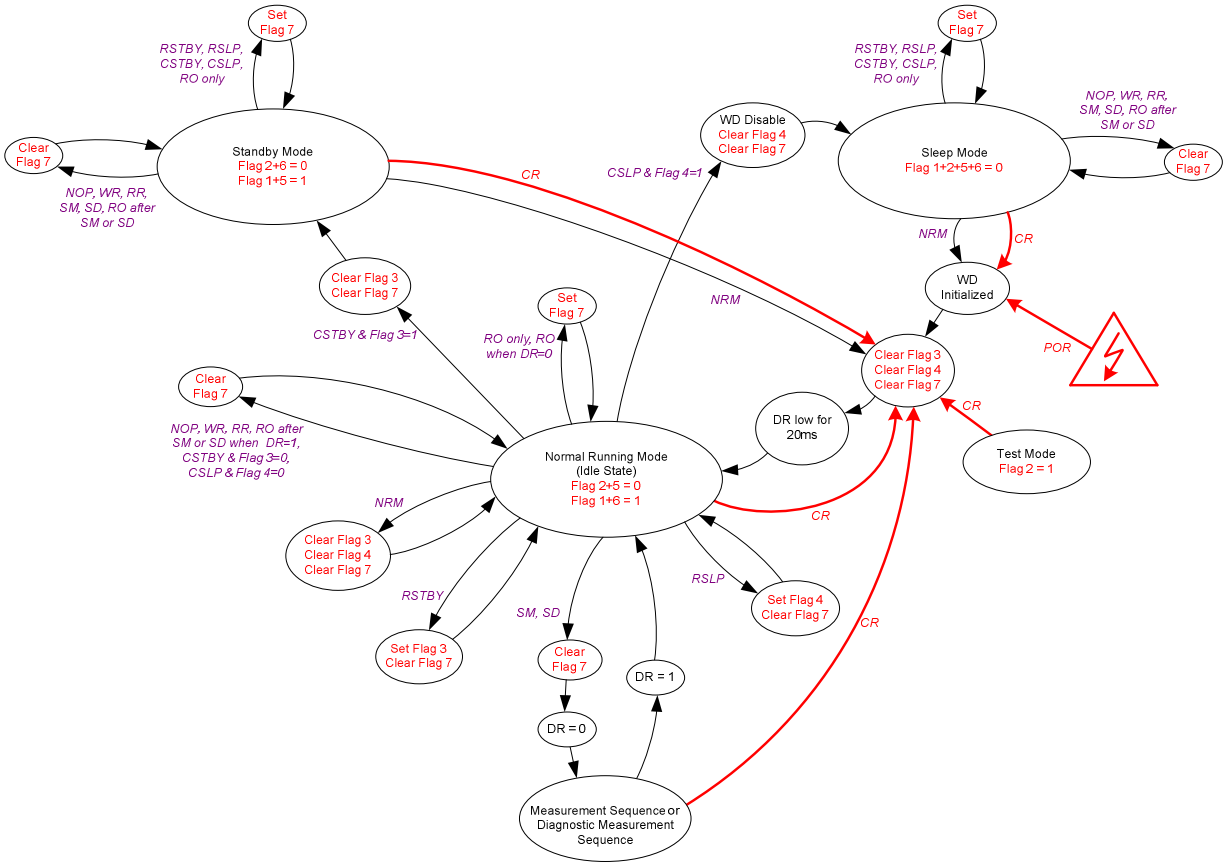


Figure 10 : State Diagram of the MLX75031

8.11.3. Detailed Explanation of SPI Instruction Words

8.11.3.1. NOP – Idle Command

The Idle Command can be used to read back the internal status flags that appear in the Data1 Byte.
The state of the device is not changed after the NOP command is uploaded.

8.11.3.2. CR – Chip Reset Command

After upload of a Chip Reset command, the sensor returns to a state as it is after power-up (Normal Running Mode) except for the watchdog counter, the state of the *MR* line and the contents of the 'Rst' register. The watchdog counter, the 'Rst' register and the state of the *MR* line will not be influenced by a CR command.

The CR command can be uploaded at any time, even during a measurement or a read-out cycle, provided that the internal synchronization counter is reset. This is done by setting the *CS* pin high for at least a time t_{cs_inter}.

When a CR command is uploaded during sleep mode resp. standby mode, the device goes automatically into normal running mode. Note that this requires a time t_{wakeup_slp} resp. t_{wakeup_stby} before the internal analog circuitry is fully set up again.

Right after upload of a CR command, the *DR* pin will go low during a time $t_{startup}$. Once the wake-up/reset phase is complete, the *DR* pin will go high.

8.11.3.3. RSLP/CSLP – Request Sleep/Confirm Sleep

To avoid that the slave device goes unintentionally into sleep mode, the master has to upload two commands. First a RSLP (Request Sleep) shall be uploaded, then the slave sets bit 4 of the internal status flag byte high. The master has to confirm the sleep request by uploading a CSLP (Confirm Sleep). Afterwards the slave will go into Sleep Mode, hereby reducing the current consumption, and the pin *SLEEPB* will switch to low indicating that the device state changed into Sleep mode.
The pin *SLEEPB* will change state a time t_{sleepb} after the pin *CS* is set high at the end of the CSLP command.

The status flag can be cleared by uploading a CR command or a NRM command.
Note that uploading a Chip Reset makes the device switching into normal running mode.

The state of the DR pin will not be changed when going into Sleep Mode. However, after a wake-up event the DR pin is set low during a time t_{wakeup_slp}.

8.11.3.4. RSTBY/CSTBY - Request Standby/Confirm Standby

To put the device in Standby Mode, a similar system is used: the master shall send the RSTBY command, requesting the slave to go into Standby Mode. The slave device sets bit 3 of the internal status flag byte high, indicating that it wants to go into standby. The master has to confirm this by sending the CSTBY byte. The pin *SLEEPB* will be set low a time t_{sleepb} after the pin *CS* is set high at the end of the CSTBY command.

The status flag can be cleared by uploading a CR command or a NRM command.
Note that uploading a Chip Reset makes the device switching into normal running mode.

The state of the DR pin will not be changed when going into Standby Mode. However, after a wake-up event the DR pin is set low during a time t_{wakeup_stby}.

8.11.3.5. NRM – Normal Running Mode

The NRM command shall be used to wake up the device from Sleep Mode, or to go from Standby into Normal Running Mode. This requires a time t_{wakeup_slp} resp. t_{wakeup_stby} before the internal analog circuitry is fully set up again. The NRM will also clear the Sleep Request or Standby Request flag.
When the device wakes up from Standby or Sleep mode, the pin *SLEEPB* will go high, to indicate that the device state changed into Normal Running Mode. The t_{sleepb} time is not applicable in case of wake-up.

When the NRM command is uploaded during normal running mode, the state of the device will not be influenced, except when the Sleep Request or Standby Request flag was set high due to a RSLP or RSTBY command. In this case, the Sleep Request or Standby Request flag will be cleared; the state of the DR pin will not change.

8.11.4. SM – Start Measurement

The SM command is used to start up measurement cycles.
Two different Measurement Sequences can be selected with option bit M_6:

- setting M_6 high enables the Measurement Sequence 1, wherein the two Ambient Light Channels, the die temperature and the voltage on the *VSUP* pin are measured
- setting M_6 low enables the Measurement Sequence 2, wherein the DC Light, the Active Light, the LED Temperature and the voltage on the *VSUP* pin during the Active Light pulse are measured. When M_6 is set low, 4 other option bits are available in order to select the LED that needs to be fired and to select the Active Light channel that needs to be read out:
  - M_3: setting this bit high fires LED A and measures the temperature of LED A
  - M_2: setting this bit high fires LED B and measures the temperature of LED B
  - M_1: setting this bit high enables the Active Light measurement in channel A
  - M_0: setting this bit high enables the Active Light measurement in channel B

The table below gives the overview of available options bits in the SM command.

Control2 Bits	Measurement Sequence 1	Measurement Sequence 2
M6	Set to 1	Set to 0
M5	Set to 0	Set to 0
M4	Set to 0	Set to 0
M3	Set to 0	1 = Fire + Measure Temperature of LED A 0 = Don't fire + Measure Temperature of LED A
M2	Set to 0	1 = Fire + Measure Temperature of LED B 0 = Don't fire + Measure Temperature of LED B
M1	Set to 0	1 = Measure Active Light on Channel A 0 = Don’t measure Active Light on Channel A
M0	Set to 0	1 = Measure Active Light on Channel B 0 = Don’t measure Active Light on Channel B
Available Measurements	Die temperature Ambient light channel C Ambient light channel D Battery voltage	DC light before Active Light pulse Battery voltage during Active Light pulse Active Light measurements Temperature of LED

Table 15 : Available option bits in SM Command

A typical timing diagram is given in Figure 11. After uploading the SM command, the measurement cycle is started as soon as the *CS* pin is set high. The ADC starts converting all the needed analog voltages and stores the digital values in registers.
A time t_{cs_dr} after *CS* is set high, the state of the *DR* pin goes low. A time t_{dr} after *DR* was set low, the state of the *DR* pin becomes high, indicating that all measurements are completed and that the resulted data is available for read-out (read-back of the stored data in the registers). This time can be up to 239us, if an internal auto-zeroing process is under execution and needs to be finished.

Table 16 : Basic Measurement Execution Times tdr

Measurement Type	Min. tdr (µs)	Max. tdr (µs)
Measurement Sequence 1	520	611
Measurement Sequence 2: measure one Active Light channel with typical Tdc_pulse<1:0> and typical TP<2:0> settings	786	924
Measurement Sequence 2: measure one Active Light channel with maximum Tdc_pulse<1:0> and maximum TP<2:0> settings	1024	1203
Measurement Sequence 2: measure two Active Light channels with typical Tdc_pulse<1:0> and typical TP<2:0> settings	921	1082
Measurement Sequence 2: measure two Active Light channels with maximum Tdc_pulse<1:0> and maximum TP<2:0> settings	1159	1361

Note : the *DR* pin can be used as an interrupt for the master device as it indicates when a read-out cycle can be started.

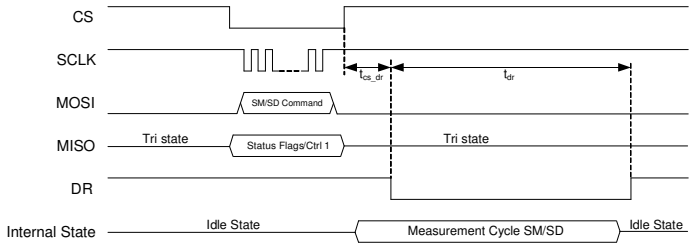


Figure 11 : Timing Diagram of a Measurement Cycle

The SM command contains 2 option bits: R0 & T. The bit R0 sets the polarity of the ADC input buffer in Active Light channels A & B. The bit T provides test pulses during the Active Light measurements.

- R0: Inversion of the offset of the ADC_buffer. The output will change from (Signal + Offset_opamp_buf) to (Signal - offset_opamp_buf). In this way, by processing 2 measurements with inverted R0 bits, the offset of the ADC buffer filter can be cancelled.
- T: This bit replaces the light pulses by internal current pulses during the Active Light measurements. The LED driver will not be activated when this option bit is selected.

The SM command contains an option bit T. If this bit is set to 0, normal Active Light measurements are performed (i.e. the external LED's are fired and the Active Light channels A and/or B are measured). If this bit is set to 1, no LED's are fired, but an internal test pulse is applied to channels A and/or B. The internal test pulse can be influenced in amplitude by the bits DACA7 and DACA6 (when LED A is fired) or by the bits DACB7 and DACB6 (when LED B is fired).

DACA7/ DACB7	DACA6/ DACB6	I_Testpulse [uA]	Typical ADC value [LSB] at default TP & Gain settings
0	0	5	8466
0	1	13	14737
1	0	21	20967
1	1	29	27195

Table 17 : Current levels for Active Light testmode.

In the Control2 byte an even parity bit P is foreseen. The parity bits calculation is based on the measurement selection bits $M_6..M_0$. If the number of ones in the given data set $[M_6..M_0]$ is odd, the even parity bit P shall be set to 1, making the total number of ones in the set $[M_6..M_0, P]$ even.
The SPI invalid flag will be set when the parity bit does not correspond to the calculated parity bit.

After upload of a SM/SD command, no other commands will be accepted till *DR* is high. This is done to avoid too much disturbances in the analog part. Once *DR* is high, the next command will be accepted. An exception however is the Chip Reset command. This will always be accepted.

Note : none of the SM/SD commands are available in Standby and Sleep Mode.

8.11.5. RO – Start Read-Out

When the state of the *DR* pin changed into a high state, the measurement data is available for read-out.
The RO command shall be uploaded to start a read-out cycle and to start reading out the data that was stored in the internal registers.

To make sure that no memory effects can occur,
all data registers are cleared at the end of each read-out cycle.

A typical timing diagram is given in Figure 12 below:

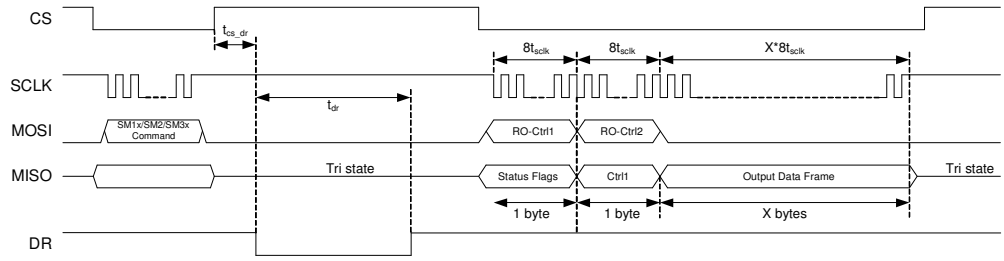


Figure 12 : Timing diagram for Read-Out

Note : the RO command is not available in Standby and Sleep Mode.

The data that appears on the *MISO* pin depends on the type of measurement that was done (i.e. it depends on the command that was uploaded: SM/SD and the selected option bits $M_6..M_0$).

The table below shows the Output Data Frame when Measurement Sequence 1 is selected :

Data Byte Number	Output Data Frame Contents - Measurement Sequence 1	Comments
Byte 3	Die Temperature Measurement (8 MSB)	Depends on EN_TEMP
Byte 4	Die Temperature Measurement (8 LSB)	Depends on EN_TEMP
Byte 5	Ambient light \ channel C measurement (8 MSB)	Depends on EN_CH_C
Byte 6	Ambient light channel C measurement (8 LSB)	Depends on EN_CH_C
Byte 7	Ambient light channel D measurement (8 MSB)	Depends on EN_CH_D
Byte 8	Ambient light channel D measurement (8 LSB)	Depends on EN_CH_D
Byte 9	Internally Reserved Register	Reserved
Byte 10	Internally Reserved Register	Reserved
Byte 11	Battery Voltage Measurement (8 MSB)	Depends on EN_VSUPMON
Byte 12	Battery Voltage Measurement (8 LSB)	Depends on EN_VSUPMON
Byte 13	CRC (8 bit)	Output always

Table 18 : SM Output Data Frame - Measurement Sequence 1

The table below shows the Output Data Frame when Measurement Sequence 2 is selected :

Data Byte Number	Output Data Frame Contents - Measurement Sequence 2	Comments
Byte 3	DC measurement of IR channel A (8 MSB)	Depends on M1 + on EN_CH_A
Byte 4	DC measurement of IR channel A (8 LSB)	Depends on M1 + on EN_CH_A
Byte 5	DC measurement of IR channel B (8 MSB)	Depends on M0 + on EN_CH_B
Byte 6	DC measurement of IR channel B (8 LSB)	Depends on M0 + on EN_CH_B
Byte 7	Battery voltage measurement during Active Light pulse (8 MSB)	Depends on EN_VSUPMON
Byte 8	Battery voltage measurement during Active Light pulse (8 LSB)	Depends on EN_VSUPMON
Byte 9	Active Light measurement of IR channel A (8 MSB)	Depends on M1 + on EN_CH_A + LED selection depends on M3/M2
Byte 10	Active Light measurement of IR channel A (8 LSB)	Depends on M1 + on EN_CH_A + LED selection depends on M3/M2
Byte 11	Active Light measurement of IR channel B (8 MSB)	Depends on M0 + on EN_CH_B + LED selection depends on M3/M2
Byte 12	Active Light measurement of IR channel B (8 LSB)	Depends on M0 + on EN_CH_B + LED selection depends on M3/M2

Byte 13	Temperature of LED that was fired (8 MSB)	Depends on EN_LEDSENS + LED selection depends on M3/M2
Byte 14	Temperature of LED that was fired (8 LSB)	Depends on EN_LEDSENS + LED selection depends on M3/M2
Byte 15	CRC (8 bit)	Output always

Table 19 : SM Output Data Frame - Measurement Sequence 2

When certain measurement blocks are disabled, the corresponding data bytes are omitted from the Output Data Frame.

Cyclic Redundancy Check Calculation

In all Output Data Frames, a CRC byte is included as last byte. This byte provides a way to detect transmission errors between slave and master. An easy method to check if there were no transmission errors is to calculate the CRC of the whole read-out frame as defined in previous tables. When the calculated CRC results in 0x00, the transmission was error free. If the resulting CRC is not equal to zero, then an error occurred in the transmission and all the data should be ignored.
For more information regarding the CRC calculation, please refer to Section 8.18.

8.11.6. DM+RO - Start Measurement combined with Read-Out

If after upload of the SM command, extra clocks are given (without putting CS high!), the data stored in the internal registers will appear on the MISO pin. At the end of the read-out phase the internal registers will be cleared to avoid memory effects in the next read-outs.
The newly uploaded SM command will be executed after the read-out, when the CS pin goes high.

The two figures below show the difference between the two modes of operation:
- Figure 13 shows the operation with separate SM and RO commands. After upload of a SM command, the measurement cycle will start and the internal registers will be filled. Once the DR pin is high, the RO command can be uploaded to start the read-out cycle. All data of the internal registers will be transferred and at the end of the read-out the registers will be cleared.
- Figure 14 shows the operation with the combined SM and RO. First one has to upload a SM command to start a measurement. The data is available for read-out when the DR pin goes high. Instead of uploading a RO command, a SM command can be uploaded again to combine read-out and the start of the next measurement cycle. If extra clocks are given after upload of the SM command, the data of the internal registers becomes available on the MISO pin. Note that the CS pin shall not be set high until the read-out is finished. Once CS pin goes high, the DR pin is set low and a new measurement cycle will be started. A time tdr later the DR pin goes high to indicate that the data is available.

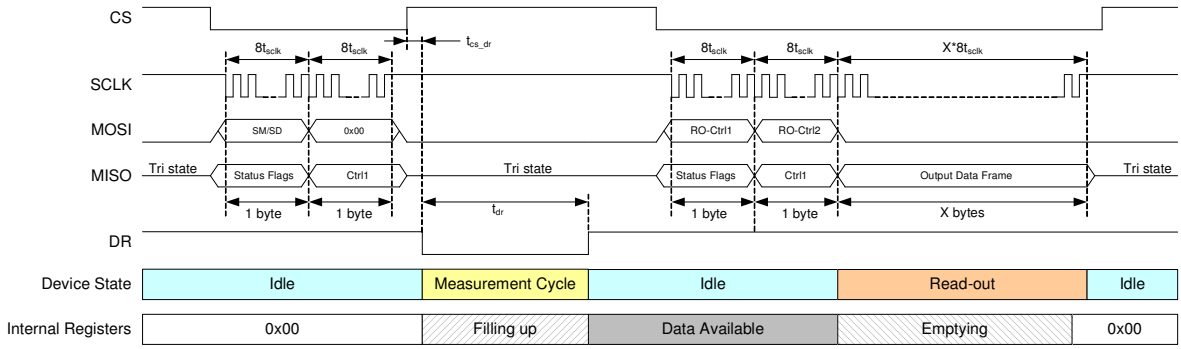


Figure 13 : Separated SM - RO (X value is defined in Figure 12)

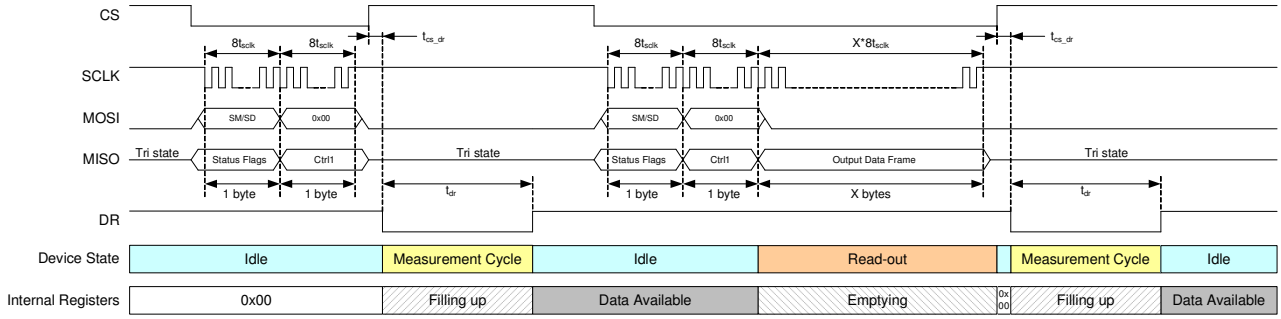


Figure 14 : Combined SM - RO (X value is defined in Figure 12)

8.11.7. WR/RR - Write/Read Register

The slave contains several user registers that can be read and written by the master.
The WR and RR commands are used for that.

The WR command writes the contents of an 8-bit register addressed by bits $A_{3..0}$ with data $D_{7..0}$. Data is sent to the device over the *MOSI* pin. Control2 Byte contains the 8 bit data that shall be written into the target register. Control3 Byte contains the address of the target register.
The WR command is defined in the table below:

Control1 Byte	Control2 Byte	Control3 Byte
1000 0111	D7D6D5D4 D3D2D1D0	A3A2A1A0 P1P000
D7D6D5D4 D3D2D1D0 A3A2A1A0 P1P0	Data contents of register to be written Address of target register Parity bits (P1 = odd parity bit, P0 = even parity bit)	
Data1 Byte	**Data2 Byte**	**Data3 Byte**
Status Flag Byte	1000 0111	0000 0000

Table 20 : Write Register command

In order to detect some transmission errors while writing data towards the slave device, the micro-controller has to compute an odd and an even parity bit of the Control2 and the 4 MSB's of the Control3 byte and send these parity bits to the slave. The slave will check if the parity bits are valid. The data will only be written into the registers if the parity bits are correct. If the parity bits are not correct, bit 7 of the internal Status Flag Byte will be set high, indicating that the command was invalid. This can be seen when uploading a NOP command (when one is only interested in reading back the internal status flags) or during upload of the next command.
In case the parity bits were not correct, the data of the registers will not be changed.

The parity bits calculation is based on the data $D_7..D_0$ and $A_3..A_0$. If the number of ones in the given data set [$D_7..D_0$, $A_3..A_0$] is odd, the even parity bit P_0 shall be set to 1, making the total number of ones in the set [D7..D0, A3..A0, P0] even.
Similar: if the number of ones in the given data set [D7..D0, A3..A0] is even, the odd parity bit P1 shall be set to 1, making the total number of ones in the set [D7..D0, A3..A0, P1] odd.

Note that the parity bits can be generated with XOR instructions: P1 = XNOR(D7..D0, A3..A0) and P0 = XOR(D7..D0, A3..A0). The odd parity bit P1 should always be the inverse of the even parity bit P0.

The RR command returns the contents of an 8-bit register addressed by bits A3..0. Data is read back over the MISO pin. The Data1 Byte contains the Internal Status Flag byte. Data2 Byte contains the copy of the Control1 Byte. Data3 Byte contains the 8 bits of the target register.
The RR command is defined in the table below:

Control1 Byte	Control2 Byte	Control3 Byte
1000 1110	A3A2A1A0 0000	0000 0000
A3A2A1A0	Address of target register	
Data1 Byte	**Data2 Byte**	**Data3 Byte**
Status Flag Byte	1000 1110	D7D6D5D4 D3D2D1D0
D7..0	Data contents of register read	

Table 21 : Read Register command

Note : WR and RR commands are commands that require 3 bytes instead of 2 bytes.

More information concerning the user registers can be found in Section 0.

8.11.8. SD – Start Diagnostics

The SD command will start a measurement cycle in which internal signals will be measured and converted. With this command it is possible to test some circuits in the chip and check if they are functioning as expected.

The SD command behaves in much the same way as the SM commands: instead of uploading a SM command, a SD command can be uploaded. This starts the measurement cycle and conversion of some internal signals. The pin DR goes high when the cycle is completed, indicating that a read-out can be started. With the RO command it is possible to read out the data and check if all the data values are within certain ranges.

After upload of a SD command, no other commands will be accepted till DR is high. This is done to avoid too much disturbances in the analog part. Once DR is high, the next command will be accepted. An exception however is the Chip Reset command. This will always be accepted.
The SD command is not available in Standby Mode.

The execution time tdr for the diagnostics measurements is between 605µs and 712µs.

The Output Data Frame is defined in the table below :

Data Byte Number	Data Byte Contents after SD command
Byte 3	ADCtest0 (8 MSB)
Byte 4	ADCtest0 (8 LSB)
Byte 5	ADCtest1 (8 MSB)
Byte 6	ADCtest1 (8 LSB)
Byte 7	ADCtest2 (8 MSB)
Byte 8	ADCtest2 (8 LSB)
Byte 9	ADCtest3 (8 MSB)
Byte 10	ADCtest3 (8 LSB)
Byte 11	DAC-ADC Test (8 MSB)
Byte 12	DAC-ADC Test (8 LSB)
Byte 13	00000 + CDE Ambient Diodes Detection (3 bit)
Byte 14	CRC (8 bit)

Table 22 : SD Output Data Frame

ADCtest0/1/2/3
These measurements are AD conversions of some internal reference voltages:

- ADCtest0 is typically at 1/16 of the ADC range: ADCtest0 = 0x0E00 .. 0x1200.
- ADCtest1 is typically at 1/4=4/16 of the ADC range: ADCtest1 = 0x3E00 .. 0x4200.
- ADCtest2 is typically at 15/16 of the ADC range: ADCtest2 = 0xEE00 .. 0xF200.

ADCtest3 is similar to ADCtest0/1/2: an AD conversion of an internal reference voltage is made. However, an independent voltage reference is used as input for the ADC in case of ADCtest3. In the case of ADCtest0/1/2, the reference voltages are generated from the references used for the ADC.
The typical output for ADCtest3 will be at half of the ADC range: ADCtest3 = 0x7888 .. 0x89D0. These values are valid for VDD=3.3V +/-2%.

DAC-ADC test
A DAC-ADC test measurement is performed in the following way: the DAC output is connected to the ADC input. The DAC input will be DACA<7:0> from register 'SetAH'. This DAC-input will be converted to an analog output voltage that will be converted again by the ADC to give a digital value. This digital value is given in the bytes DAC-ADC Test. Note that the values written to DACA<7:0> should be limited to the range 0x80..0xFF during the DAC-ADC test.

In section Section 8.5.1 the typical DAC output voltage is given for a certain code, call this voltage Vdac (in V). Then the following formula applies: ADC_out = 19721*Vdac + 32768, where ADC_out is the decimal value of the DAC-ADC Test word in the Output Data Frame.

Ambient Diodes Detection
During the Diagnostics measurement, the status of the external photo diodes connected to the ambient light channel inputs is checked.
Three bits b'CDE are output: when the bit C is set high, an error on the photodiode channel C is present. In a similar way, bits D and E indicate if errors on ambient light channels D and E are present or not.

8.12. Internal Status Flags

Bit 7: Previous Command invalid/valid
When an uploaded command is considered invalid, bit 7 will be set high. This bit can be read out when the next command will be uploaded. If the next command is valid, bit 7 will be cleared again.

A command is considered invalid in case :

- a command is unknown (i.e. all commands that are not mentioned in Table 14)
- the parity bit in the SM or SD command is not correct
- the parity bits in a WR command are not correct
- when a command (except the CR command) was sent during a measurement cycle (i.e. after uploading a SM/SD command, when *DR* is still low)
- when a RO command was sent when *DR* is low (at any time, i.e. not only after uploading a SM/SD command)
- if a '1' is written into one of the bits of the 'Err' register
- if a WDT command is uploaded while the device is in Sleep Mode

Bit 6..5: Power State, Bit 4: Sleep request, Bit 3: Standby request
The behaviour of the power state and the sleep request bits is explained in Figure 15.
First a RSLP command is uploaded to the sensor. As a result of that, the sensor will put the status flag bit 4 (sleep request flag) high. The master can read out that flag by uploading a NOP command, or when uploading other commands.
The master can confirm to go into sleep mode by uploading a CSLP command. The request flag will be reset and the sensor will switch into sleep state. The status flag bits 6 and 5 will be set accordingly.

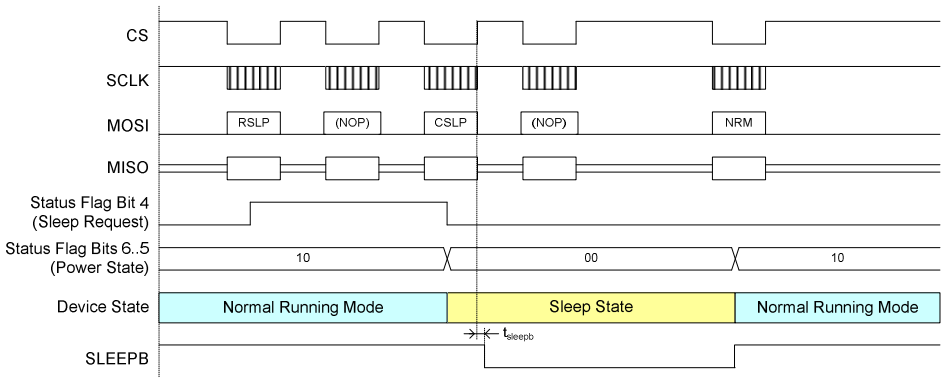


Figure 15 : Power State and Sleep Request bits

To go into standby mode, the same procedure shall be applied: uploading a RSTBY command makes the request standby flag going high. Uploading a CSTBY will make the device going into standby mode, whereby the request standby flag will be cleared and the power state bits will be set accordingly.

Bit 2: Device in TestMode/Normal Mode

To make the sensor efficiently testable in production, several test modes are foreseen to get easy access to different blocks. The status flag bit 2 indicates if the device is operating in Test Mode or Normal Mode.
If the device enters test mode by accident, the application will still work like normal. However, the status flag bit 2 will be set high. The master can take actions to get out of test mode by uploading a CR command.

Bit 1: Internal Oscillator is enabled/disabled

This bit is high when the internal oscillator is enabled. Once the RCO is shut down the bit will be set low.

Bit 0: Critical Error is detected/not detected

During each measurement cycle there is a monitoring of the voltage on critical nodes along the analog paths. When the voltage of one of these controlled nodes goes out of its normal operating range, the Critical Error Flag will be set high.

Following nodes are monitored :

- TIA output: when the output is clipped (either high or low), the Critical Error Flag will be set high
- Difference between DAC output and shunt-feedback
- An internal reference voltage
- Output of the common mode SC-amplifiers of the Ambient Light/Temperature Channels
- Frequency on RCO output
- Voltage on the *VSUP* pin

In case the Critical Error Flag was set high, the 'Err' register indicates which node voltages got out of their normal operating range. More info about the 'Err' register can be found in Section 8.13.6.

The Critical Error Flag remains high as long as the 'Err' register is not cleared. Once the 'Err' register is cleared, the Critical Error Flag will be cleared as well.

Note : after POR, or after wake-up from Sleep/Standby, some bits in the 'Err' register might be set.
As such the Critical Error Flag might be set as well.

8.13. User Registers Overview

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SetAna	0x0	VSUPLOW1	VSUPLOW0	-	-	-	Tdc_pulse1	Tdc_pulse0	Unity_Gain
SetAH	0x1	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
SetAL	0x2	GAIN_ADJ _A2	GAIN_ADJ _A1	GAIN_ADJ _A0	-	BW_ADJ _A1	BW_ADJ _A0	-	-
SetBH	0x3	DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
SetBL	0x4	GAIN_ADJ _B2	GAIN_ADJ _B1	GAIN_ADJ _B0	-	BW_ADJ _B1	BW_ADJ _B0	-	-
SetTP	0x5	-	-	EN_ LEDSENS	EN_ VSUPMON	-	TP2	TP1	TP0
Err	0x6	Err_ VsupH	Err_ TIA	Err_ Drv	Err_ Vref	Err_ Amb	Err_ RCO	-	Err_ VsupL
Rst	0x7	-	-	-	-	TrimOk	DieChip	TO	POR
Version	0x8	Ver3	Ver2	Ver1	Ver0	-	-	-	-
Reserved	0x9	-	-	-	-	-	-	-	-
GainBuf	0xA	-	-	-	GAIN_BUF4	GAIN_BUF3	GAIN_BUF2	GAIN_BUF1	GAIN_BUF0
Calib1	0xB	TRIM_ T_SLOPE4	TRIM_ T_SLOPE3	TRIM_ T_SLOPE2	TRIM_ T_SLOPE1	TRIM_ T_SLOPE0	-	-	-
Calib2	0xC	-	-	TRIM_ TEMP5	TRIM_ TEMP4	TRIM_ TEMP3	TRIM_ TEMP2	TRIM_ TEMP1	TRIM_ TEMP0
EnChan	0xD	EN_TEMP	EN_DIAG_A	EN_DIAG_B	EN_CH_A	EN_CH_B	EN_CH_C	EN_CH_D	-
Tamb	0xE	-	-	-	-	-	-	Tamb1	Tamb0
SetPLS	0xF	OS_ADJ_ LED1	OS_ADJ_ LED0	G_ADJ_ LED1	G_ADJ_ LED0	-	-	Rise1	Rise0

In the next sections, all the bits of these registers are described. The value of the register at Power-On is indicated in the line 'Init' (0 or 1 or x=unknown) and the read/write access ability is indicated in the line 'Read/Write' (R indicates Read access, W indicates Write access).

8.13.0. SetAna register

This register contains some settings of the analog chain.

	Bit	7	6	5	4	3	2	1	0
SetAna		VSUP LOW1	VSUP LOW0	-	-	-	Tdc_ pulse1	Tdc_ pulse0	Unity_ Gain
0x0	Read/Write	R/W	R/W	R	R	R	R/W	R/W	R/W
	Init	1	0	0	0	0	1	0	1

- VSUPLOW<1:0>: defines the threshold voltage at which the critical error flag Err_VSupL is set

VSUPLOW1	VSUPLOW0	VSUP Threshold (V)
0	0	5
0	1	5.5
1	0	6
1	1	6.5

- SetAna<5:3>: not implemented, read as '0'
- Tdc_pulse<1:0>: defines the time that the DC component in the Active Light pulse signal is enabled before the actual Active Light pulses start. The time mentioned in the table below is the delay time as generated by the digital logic.

Tdc_ pulse1	Tdc_ pulse0	Delay time (in µs, +/-8%)
0	0	50
0	1	100
1	0	200
1	1	400

- Unity_Gain: only during Active Light measurements: 1=ADC buffer is bypassed, 0=ADC gain stage is used (gain is set with bits GAIN_BUF<4:0> in register 'GainBuf')

8.13.1. SetAH register

This register defines the DAC level for IR channel A.

	Bit	7	6	5	4	3	2	1	0
SetAH		DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
0x1	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	0	0	0	0

- DACA<7:0>: the 8 bits of the DAC level for IR channel A

8.13.2. SetAL register

This register defines the gain and cut-off frequency adjustments for IR channel A.

	Bit	7	6	5	4	3	2	1	0
SetAL		GAIN_ ADJ _A2	GAIN_ ADJ _A1	GAIN_ ADJ _A0	-	BW_ ADJ _A1	BW_ ADJ _A0	-	-
0x2	Read/Write	R/W	R/W	R/W	R	R/W	R/W	R	R
	Init	0	0	0	0	0	1	0	0

- GAIN_ADJ_A<2:0>: gain adjustment of channel A

GAIN_ADJ_ _A2	GAIN_ADJ_ _A1	GAIN_ADJ_ _A0	Gain
0	0	0	3
0	0	1	5.8
0	1	0	8.7
0	1	1	11.5
1	0	0	14.4
1	0	1	17.1
1	1	0	20.3
1	1	1	22.5

- SetAL<4>: not implemented, read as '0'
- BW_ADJ_A<1:0>: cut-off frequency adjustment of channel A

BW_ADJ_ _A1	BW_ADJ_ _A0	3dB Cut-off Frequency (kHz)
0	0	15
0	1	30
1	0	45
1	1	70

- SetAL<1:0>: not implemented, read as '0'

8.13.3. SetBH register

This register defines the DAC level for IR channel B.

	Bit	7	6	5	4	3	2	1	0
SetBH		DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
0x3	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	0	0	0	0

- DACB<7:0>: the 8 bits of the DAC level for IR channel B

8.13.4. SetBL register

This register defines the gain and cut-off frequency adjustments for IR channel B.

	Bit	7	6	5	4	3	2	1	0
SetBL		GAIN_ADJ_B2	GAIN_ADJ_B1	GAIN_ADJ_B0	-	BW_ADJ_B1	BW_ADJ_B0	-	-
0x4	Read/Write	R/W	R/W	R/W	R	R/W	R/W	R	R
	Init	0	0	0	0	0	1	0	0

- GAIN_ADJ_B<2:0>: gain adjustment of channel B

GAIN_ADJ_B2	GAIN_ADJ_B1	GAIN_ADJ_B0	Gain
0	0	0	3
0	0	1	5.8
0	1	0	8.7
0	1	1	11.5
1	0	0	14.4
1	0	1	17.1
1	1	0	20.3
1	1	1	22.5

- SetBL<4>: not implemented, read as '0'
- BW_ADJ_B<1:0>: cut-off frequency adjustment of channel B

BW_ADJ_B1	BW_ADJ_B0	3dB Cut-off Frequency (kHz)
0	0	15
0	1	30
1	0	45
1	1	70

- SetBL<1:0>: not implemented, read as '0'

8.13.5. SetTP register

This register contains some enable signals and defines the pulse duration setting for the Active Light measurements.

	Bit	7	6	5	4	3	2	1	0
SetTP		-	-	EN_LEDSENS	EN_VSUPMON	-	TP2	TP1	TP0
0x5	Read/Write	R	R	R/W	R/W	R	R/W	R/W	R/W
	Init	0	0	1	1	0	0	1	1

- SetTP<7:6>: not implemented, read as '0'
- EN_LEDSENS: 1 = enables LED temperature sensing, 0 = disables LED temperature sensing
- EN_VSUPMON: 1 = enables voltage monitoring on VSUP, 0 = disables voltage monitoring on VSUP
- TP<2:0>: pulse duration selection for the Active Light measurements, as defined below :

Bit 2 - TP2	Bit 1 - TP1	Bit 0 - TP0	Pulse width (+/- 8%)
0	0	0	4 µs
0	0	1	9.6 µs
0	1	0	14.4 µs
0	1	1	19.2 µs
1	0	0	24µs
1	0	1	29.6µs
1	1	0	49.6µs
1	1	1	79.2µs

Note : the target pulse width's to be used are: 14.4, 19.2, 24 and 29.6µs.
The smaller and the larger pulse width's are available for engineering purposes only. For the smaller pulse width's the settling of the LED driver is not guaranteed. For the larger pulse width's the thermal behaviour is not guaranteed.

8.13.6. Err register

As described in Section 0 (under section 'Bit 0: Critical Error is detected/not detected'), the voltages on critical nodes are monitored continuously. When a voltage on such a critical node goes outside its operating range, the Critical Error Flag and the appropriate error bit in the 'Err' register will be set high. As such, the source of the error can be found in the 'Err' register.
The error bit remains high as long as the error condition is present, or as long as the error bit is not cleared (in case the error condition is not present anymore).

	Bit	7	6	5	4	3	2	1	0
Err		Err_ VsupH	Err_ TIA	Err_ Drv	Err_ Vref	Err_ Amb	Err_ RCO	-	Err_ VsupL
0x6	Read/Write	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R	R/W*
	Init	x**	0	0	x**	x**	x**	0	x**

The following bits are defined (0= no error detected; 1=error is detected) :

- Err_VsupH: critcal error detected on battery supply voltage: VSUP > 20V typical. As long as VSUP > 20V typical, the LED driver will be shut off to avoid damaging the LED's. Measurement data should be discarded in this situation.
- Err_TIA: critical error detected on TIA output
- Err_Drv: critical error detected on the difference between DAC output and shunt-feedback
- Err_Vref: critical error detected on internal voltage reference: when the internal voltage reference is below 1V.
- Err_Amb: critical error detected on one of the common mode SC-filters of the ambient light/temperature channels
- Err_RCO: critical error detected on RCO: either a stuck-at-high or a stuck-at-low condition occurred at the output of the RCO. Note that in SLP, the error flag on the RCO will be set high.
- Err<1>: not implemented, read as '0'
- Err_VsupL: critical error detected on battery supply voltage: VSUP < 6V typical (default). Note that this threshold is programmable with 2 bits VSUPLOW<1:0>).

* : only writing '0' is allowed. If a '1' is written, the bit value in the register will not be changed, but Bit 7 of the Internal Status Flags will be set high (Previous Command Invalid).
** : 'x' indicates that the value after POR is unknown. If the voltages of the nodes are out of range right after POR, it will be immediately reflected in the 'Err' register and the Critical Error Flag will be set. The same is valid after wake-up from Sleep/Standby.

8.13.7. Rst register

This register allows differentiation of either a POR or a reset due to a watchdog time-out + settings for the PD compensation circuitry.

	Bit	7	6	5	4	3	2	1	0
Rst		-	-	-	-	TrimOK	DieChip	TO	POR
0x7	Read/Write	R-	R-	R-	R-	R	R	R	R/W
	Init	0	0	0	0	1	0	0	1

- TrimOK: 1 if device passed both 105degC and m40degC test successfully, 0 if one of the tests is not passed successfully
- DieChip: 1 if die chipping is present, 0 is not die chipping is present. Note that DieChip will only be valid during NRM.
- TO: 1=a Watchdog time-out and a master reset occurred. 0=no Watchdog time-out occurred, or after Power-On, or after a WDT command
- POR: 1=a POR occurred, 0=a POR has not occurred. To detect subsequent Power-On-Resets, the POR-bit shall be cleared right after Power-On.

8.13.8. Version register

This register contains the actual device version + settings for the PD compensation circuitry.

	Bit	7	6	5	4	3	2	1	0
Version		Ver3	Ver2	Ver1	Ver0	-	-	-	-
0x8	Read/Write	R	R	R	R	R	R	R	R
	Init	0	0	0	1	0	0	0	0

- Ver<3:0>: indicates the device version (will be incremented at every design iteration)
  - A-version: Ver<3:0> = 4'b0001

8.10.9. Reserved register

This register is used for internal evaluation purposes.

8.10.10. GainBuf register

This register contains the gain settings of the ADC input buffer. The use of this buffer is depending on bit 'Unity_Gain' in the register 'SetAna'. It is recommended to keep the GainBuf register to its default value. Please contact Melexis before changing it.

	Bit	7	6	5	4	3	2	1	0
GainBuf		-	-	-	GAIN_ BUF4	GAIN_ BUF3	GAIN_ BUF2	GAIN_ BUF1	GAIN_ BUF0
0xA	Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	1	1	0	1	0

- GainBuf<7:5>: not implemented, read as '0'
- GAIN_BUF<4:0>: defines the gain setting of the ADC input buffer

GAIN_ BUF4	GAIN_ BUF3	GAIN_ BUF2	GAIN_ BUF1	GAIN_ BUF0	Gain
0	0	0	0	1	2
0	0	0	1	0	1
0	0	0	1	1	0.67
0	0	1	0	0	0.5
0	0	1	0	1	0.4
0	0	1	1	0	0.33
0	0	1	1	1	0.29
0	1	0	0	0	0.25
0	1	0	0	1	0.22
0	1	0	1	0	0.2
1	0	0	0	1	10
1	0	0	1	0	5
1	0	0	1	1	3.33
1	0	1	0	0	2.5
1	0	1	0	1	2
1	0	1	1	0	1.67
1	0	1	1	1	1.43
1	1	0	0	0	1.25
1	1	0	0	1	1.11
1	1	0	1	0	1

8.13.11/12 Calib1/Calib2 register

These registers contain the calibration settings for the temperature sensor.

	Bit	7	6	5	4	3	2	1	0
Calib1		TRIM_ T_SLOPE4	TRIM_ T_SLOPE3	TRIM_ T_SLOPE2	TRIM_ T_SLOPE1	TRIM_ T_SLOPE0	-	-	-
0xB	Read/Write	R	R	R	R	R	R	R	R
	Init	x	x	x	x	x	0	0	0

- TRIM_T_SLOPE<4:0>: defines the slope of the temperature sensor
- Calib1<2:0>: not implemented, read as '0'

The Calib1 register is used to indicate the slope of the temperature sensor curve in LSB/Kelvin. The slope is calculated out of a 2-point measurement of the temperature curve and is permanently programmed in the OTP by means of a 5 Bit word and accessible via the Calib1 register, see Table 23.

Calib1 - TRIM_T_SLOPE<4:0>					
Dec	Bin	Slope (LSB/Kelvin)	Dec	Bin	Slope (LSB/Kelvin)
0	0	-51	16	10000	-67
1	1	-52	17	10001	-68
2	10	-53	18	10010	-69
3	11	-54	19	10011	-70
4	100	-55	20	10100	-71
5	101	-56	21	10101	-72
6	110	-57	22	10110	-73
7	111	-58	23	10111	-74
8	1000	-59	24	11000	-75
9	1001	-60	25	11001	-76
10	1010	-61	26	11010	-77
11	1011	-62	27	11011	-78
12	1100	-63	28	11100	-79
13	1101	-64	29	11101	-80
14	1110	-65	30	11110	-81
15	1111	-66	31	11111	-82

Table 23 : 5-Bit temperature sensor slope information as it is stored in the calib1 register.

	Bit	7	6	5	4	3	2	1	0
Calib2		-	-	TRIM_ TEMP5	TRIM_ TEMP4	TRIM_ TEMP3	TRIM_ TEMP2	TRIM_ TEMP1	TRIM_ TEMP0
0xC	Read/Write	R	R	R	R	R	R	R	R
	Init	0	0	x	x	x	x	x	x

- Calib2<7:6>: not implemented, read as '0'
- TRIM_TEMP<5:0>: defines the calibration settings of the temperature sensor

The offset of the temperature curve is measured at one temperature (preferably 30degC) and permanently stored in the zenerzap OTP with 6 bit word length. This information is accessible via the Calib2 register, see Table 24.

Calib2 - TRIM_TEMP<5:0>			Slope: -67LSB/K					
			25degC			30degC		
Dec	Bin	Offset (degC)	LSL	expected	USL	LSL	expected	USL
1	1	-31	10005.5	10039	10072.5	9670.5	9704	9737.5
2	10	-30	10072.5	10106	10139.5	9737.5	9771	9804.5
3	11	-29	10139.5	10173	10206.5	9804.5	9838	9871.5
4	100	-28	10206.5	10240	10273.5	9871.5	9905	9938.5
5	101	-27	10273.5	10307	10340.5	9938.5	9972	10005.5
6	110	-26	10340.5	10374	10407.5	10005.5	10039	10072.5
7	111	-25	10407.5	10441	10474.5	10072.5	10106	10139.5
8	1000	-24	10474.5	10508	10541.5	10139.5	10173	10206.5
9	1001	-23	10541.5	10575	10608.5	10206.5	10240	10273.5
10	1010	-22	10608.5	10642	10675.5	10273.5	10307	10340.5
11	1011	-21	10675.5	10709	10742.5	10340.5	10374	10407.5
12	1100	-20	10742.5	10776	10809.5	10407.5	10441	10474.5
13	1101	-19	10809.5	10843	10876.5	10474.5	10508	10541.5
14	1110	-18	10876.5	10910	10943.5	10541.5	10575	10608.5
15	1111	-17	10943.5	10977	11010.5	10608.5	10642	10675.5
16	10000	-16	11010.5	11044	11077.5	10675.5	10709	10742.5
17	10001	-15	11077.5	11111	11144.5	10742.5	10776	10809.5
18	10010	-14	11144.5	11178	11211.5	10809.5	10843	10876.5
19	10011	-13	11211.5	11245	11278.5	10876.5	10910	10943.5
20	10100	-12	11278.5	11312	11345.5	10943.5	10977	11010.5
21	10101	-11	11345.5	11379	11412.5	11010.5	11044	11077.5
22	10110	-10	11412.5	11446	11479.5	11077.5	11111	11144.5
23	10111	-9	11479.5	11513	11546.5	11144.5	11178	11211.5
24	11000	-8	11546.5	11580	11613.5	11211.5	11245	11278.5
25	11001	-7	11613.5	11647	11680.5	11278.5	11312	11345.5
26	11010	-6	11680.5	11714	11747.5	11345.5	11379	11412.5
27	11011	-5	11747.5	11781	11814.5	11412.5	11446	11479.5
28	11100	-4	11814.5	11848	11881.5	11479.5	11513	11546.5
29	11101	-3	11881.5	11915	11948.5	11546.5	11580	11613.5
30	11110	-2	11948.5	11982	12015.5	11613.5	11647	11680.5
31	11111	-1	12015.5	12049	12082.5	11680.5	11714	11747.5
32	100000	0	12082.5	12116	12149.5	11747.5	11781	11814.5
33	100001	1	12149.5	12183	12216.5	11814.5	11848	11881.5
34	100010	2	12216.5	12250	12283.5	11881.5	11915	11948.5
35	100011	3	12283.5	12317	12350.5	11948.5	11982	12015.5
36	100100	4	12350.5	12384	12417.5	12015.5	12049	12082.5
37	100101	5	12417.5	12451	12484.5	12082.5	12116	12149.5
38	100110	6	12484.5	12518	12551.5	12149.5	12183	12216.5
39	100111	7	12551.5	12585	12618.5	12216.5	12250	12283.5
40	101000	8	12618.5	12652	12685.5	12283.5	12317	12350.5
41	101001	9	12685.5	12719	12752.5	12350.5	12384	12417.5

42	101010	10	12752.5	12786	12819.5	12417.5	12451	12484.5
43	101011	11	12819.5	12853	12886.5	12484.5	12518	12551.5
44	101100	12	12886.5	12920	12953.5	12551.5	12585	12618.5
45	101101	13	12953.5	12987	13020.5	12618.5	12652	12685.5
46	101110	14	13020.5	13054	13087.5	12685.5	12719	12752.5
47	101111	15	13087.5	13121	13154.5	12752.5	12786	12819.5
48	110000	16	13154.5	13188	13221.5	12819.5	12853	12886.5
49	110001	17	13221.5	13255	13288.5	12886.5	12920	12953.5
50	110010	18	13288.5	13322	13355.5	12953.5	12987	13020.5
51	110011	19	13355.5	13389	13422.5	13020.5	13054	13087.5
52	110100	20	13422.5	13456	13489.5	13087.5	13121	13154.5
53	110101	21	13489.5	13523	13556.5	13154.5	13188	13221.5
54	110110	22	13556.5	13590	13623.5	13221.5	13255	13288.5
55	110111	23	13623.5	13657	13690.5	13288.5	13322	13355.5
56	111000	24	13690.5	13724	13757.5	13355.5	13389	13422.5
57	111001	25	13757.5	13791	13824.5	13422.5	13456	13489.5
58	111010	26	13824.5	13858	13891.5	13489.5	13523	13556.5
59	111011	27	13891.5	13925	13958.5	13556.5	13590	13623.5
60	111100	28	13958.5	13992	14025.5	13623.5	13657	13690.5
61	111101	29	14025.5	14059	14092.5	13690.5	13724	13757.5
62	111110	30	14092.5	14126	14159.5	13757.5	13791	13824.5
63	111111	31	14159.5	14193	14226.5	13824.5	13858	13891.5

Calib2 - TRIM_TEMP			Slope: -67LSB/K					
			85degC			105degC		
Dec	Bin	Offset (degC)	LSL	expected	USL	LSL	expected	USL
1	1	-31	5985.5	6019	6052.5	4645.5	4679	4712.5
2	10	-30	6052.5	6086	6119.5	4712.5	4746	4779.5
3	11	-29	6119.5	6153	6186.5	4779.5	4813	4846.5
4	100	-28	6186.5	6220	6253.5	4846.5	4880	4913.5
5	101	-27	6253.5	6287	6320.5	4913.5	4947	4980.5
6	110	-26	6320.5	6354	6387.5	4980.5	5014	5047.5
7	111	-25	6387.5	6421	6454.5	5047.5	5081	5114.5
8	1000	-24	6454.5	6488	6521.5	5114.5	5148	5181.5
9	1001	-23	6521.5	6555	6588.5	5181.5	5215	5248.5
10	1010	-22	6588.5	6622	6655.5	5248.5	5282	5315.5
11	1011	-21	6655.5	6689	6722.5	5315.5	5349	5382.5
12	1100	-20	6722.5	6756	6789.5	5382.5	5416	5449.5
13	1101	-19	6789.5	6823	6856.5	5449.5	5483	5516.5
14	1110	-18	6856.5	6890	6923.5	5516.5	5550	5583.5
15	1111	-17	6923.5	6957	6990.5	5583.5	5617	5650.5
16	10000	-16	6990.5	7024	7057.5	5650.5	5684	5717.5
17	10001	-15	7057.5	7091	7124.5	5717.5	5751	5784.5
18	10010	-14	7124.5	7158	7191.5	5784.5	5818	5851.5
19	10011	-13	7191.5	7225	7258.5	5851.5	5885	5918.5
20	10100	-12	7258.5	7292	7325.5	5918.5	5952	5985.5
21	10101	-11	7325.5	7359	7392.5	5985.5	6019	6052.5

22	10110	-10	7392.5	7426	7459.5	6052.5	6086	6119.5
23	10111	-9	7459.5	7493	7526.5	6119.5	6153	6186.5
24	11000	-8	7526.5	7560	7593.5	6186.5	6220	6253.5
25	11001	-7	7593.5	7627	7660.5	6253.5	6287	6320.5
26	11010	-6	7660.5	7694	7727.5	6320.5	6354	6387.5
27	11011	-5	7727.5	7761	7794.5	6387.5	6421	6454.5
28	11100	-4	7794.5	7828	7861.5	6454.5	6488	6521.5
29	11101	-3	7861.5	7895	7928.5	6521.5	6555	6588.5
30	11110	-2	7928.5	7962	7995.5	6588.5	6622	6655.5
31	11111	-1	7995.5	8029	8062.5	6655.5	6689	6722.5
32	100000	0	8062.5	8096	8129.5	6722.5	6756	6789.5
33	100001	1	8129.5	8163	8196.5	6789.5	6823	6856.5
34	100010	2	8196.5	8230	8263.5	6856.5	6890	6923.5
35	100011	3	8263.5	8297	8330.5	6923.5	6957	6990.5
36	100100	4	8330.5	8364	8397.5	6990.5	7024	7057.5
37	100101	5	8397.5	8431	8464.5	7057.5	7091	7124.5
38	100110	6	8464.5	8498	8531.5	7124.5	7158	7191.5
39	100111	7	8531.5	8565	8598.5	7191.5	7225	7258.5
40	101000	8	8598.5	8632	8665.5	7258.5	7292	7325.5
41	101001	9	8665.5	8699	8732.5	7325.5	7359	7392.5
42	101010	10	8732.5	8766	8799.5	7392.5	7426	7459.5
43	101011	11	8799.5	8833	8866.5	7459.5	7493	7526.5
44	101100	12	8866.5	8900	8933.5	7526.5	7560	7593.5
45	101101	13	8933.5	8967	9000.5	7593.5	7627	7660.5
46	101110	14	9000.5	9034	9067.5	7660.5	7694	7727.5
47	101111	15	9067.5	9101	9134.5	7727.5	7761	7794.5
48	110000	16	9134.5	9168	9201.5	7794.5	7828	7861.5
49	110001	17	9201.5	9235	9268.5	7861.5	7895	7928.5
50	110010	18	9268.5	9302	9335.5	7928.5	7962	7995.5
51	110011	19	9335.5	9369	9402.5	7995.5	8029	8062.5
52	110100	20	9402.5	9436	9469.5	8062.5	8096	8129.5
53	110101	21	9469.5	9503	9536.5	8129.5	8163	8196.5
54	110110	22	9536.5	9570	9603.5	8196.5	8230	8263.5
55	110111	23	9603.5	9637	9670.5	8263.5	8297	8330.5
56	111000	24	9670.5	9704	9737.5	8330.5	8364	8397.5
57	111001	25	9737.5	9771	9804.5	8397.5	8431	8464.5
58	111010	26	9804.5	9838	9871.5	8464.5	8498	8531.5
59	111011	27	9871.5	9905	9938.5	8531.5	8565	8598.5
60	111100	28	9938.5	9972	10005.5	8598.5	8632	8665.5
61	111101	29	10005.5	10039	10072.5	8665.5	8699	8732.5
62	111110	30	10072.5	10106	10139.5	8732.5	8766	8799.5
63	111111	31	10139.5	10173	10206.5	8799.5	8833	8866.5

Table 24 : 6-Bit Temperature curve offset information for a typical slope of 67LSB/K.

8.13.13. EnChan register

This register contains bit to enable/disable Active Light and ambient light channels.

	Bit	7	6	5	4	3	2	1	0
EnChan		EN_ TEMP	EN_ DIAG_A	EN_ DIAG_B	EN_ CH_A	EN_ CH_B	EN_ CH_C	EN_ CH_D	-
0xD	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
	Init	1	1	1	1	1	1	1	1

- EN_TEMP: 1 = temperature channel is in use, 0 = temperature channel is not in use
- EN_DIAG_A: 1 = enables diagnostics on Active Light channel A, 0 = disables the diagnostics
- EN_DIAG_B: 1 = enables diagnostics on Active Light channel B, 0 = disables the diagnostics
- EN_CH_A: 1 = Active Light channel A is enabled (TIA + Filter), 0 = Active Light channel A is completely switched off to reduce current consumption
- EN_CH_B: 1 = Active Light channel B is enabled (TIA + Filter), 0 = Active Light channel B is completely switched off to reduce current consumption
- EN_CH_C: 1 = ambient light channel C is in use, 0 = ambient light channel C is not in use
- EN_CH_D: 1 = ambient light channel D is in use, 0 = ambient light channel D is not in use

The bits EN_CH_A/EN_CH_B can be used to switch off channels that are not needed, and thus reducing the current consumption. When going into Sleep or Standby the setting of these bits is ignored, all channels will be switched off independently of EN_CH_A/EN_CH_B.

The bits EN_TEMP/EN_CH_C/EN_CH_D/EN_CH_E are used to indicate which channels are in use and which channels are not in use.

In case all EN_CH_C/D/E bits are set to zero, but an ambient measurement is requested, then the Command Invalid status flag will be set high. The measurement itself will not be executed.

8.13.14. Tamb register

This register contains settings for the PD compensation circuitry + controls the repetition rate of the auto-zero timer.

	Bit	7	6	5	4	3	2	1	0
Tamb		-	-	-	-	-	-	Tamb1	Tamb0
0xE	Read/Write	R	R	R	R	R	R	R/W	R/W
	Init	0	0	0	0	0	0	1	0

- Tamb<3:2>: not implemented, read as '0'
- Tamb<1:0>: controls the repetition rate of the auto-zero timer

Tamb1	Tamb0	Repetition Rate (ms +/-8%)
0	0	1.25
0	1	2.5
1	0	5
1	1	10

8.13.15. SetPLS register

This register provides parameters to set up the LED temperature sensing circuit and it defines the shape of the Active Light pulses.

	Bit	7	6	5	4	3	2	1	0
SetPLS		OS_ ADJ_ LED1	OS_ ADJ_ LED0	G_ ADJ_ LED1	G_ ADJ_ LED0	-	-	Rise1	Rise0
0xF	Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
	Init	0	1	0	0	0	0	1	0

- OS_ADJ_LED<1:0>: input offset selection for LED temperature sensing circuit

OS_ADJ_LED1	OS_ADJ_LED0	Reference Input
0	0	0.03 V
0	1	0.85 V
1	0	1.65 V
1	1	2.47 V

- G_ADJ_LED<1:0>: amplifier gain selection for LED temperature sensing circuit

G_ADJ_LED1	G_ADJ_LED0	Gain
0	0	0.99
0	1	1.98
1	0	2.98
1	1	3.99

- SetPLS<3:2>: not implemented, read as '0'
- Rise<1:0>: controls the shape of the Active Light pulses

Rise1	Rise0	Rise time of Active Light pulses (1tau - µs)
0	0	7
0	1	5
1	0	3
1	1	1

8.14. Window Watchdog Timer

The internal watchdog timer is a watchdog based on two different windows: an open and a closed window. During the open window the master can restart the watchdog timer. During the closed window, no restarts are accepted.

The restart (re-initialisation) of the watchdog timer happens via WatchDog Trigger Command: when a WDT command is sent, the watchdog will be restarted.

After a POR or a reset issued by the watchdog and after a wake-up from Sleep Mode (by uploading the NRM command), the window watchdog will open an active window of a time twdt_init, during which a watchdog restart must be issued by the µC. If no watchdog restart is received by the end of the open window, the µC will be reset.
After this initial period, the window watchdog is programmed to wait a time twdt_closed during which no watchdog restarts are allowed. If a watchdog restart is sent during the closed window time, the watchdog will reset the master via the MR (Master Reset) pin.
After a closed window, an open window of a time twdt_open will follow during which a watchdog restart is expected. If no watchdog restart is received till the end of the open window, the µC will be reset via the MR pin.

Changing mode between Normal Running Mode and Standby Mode will not influence the watchdog timing or state. Also a CR command will not change the used window times. The watchdog counter will not be influenced when changing mode between NRM and STBY or when uploading a CR command.

The Watch Dog Timer is disabled in Sleep Mode. Sending a WDT command in the Sleep Mode will set the Previous Command Invalid flag high. Coming back from Sleep Mode to Normal Running Mode always restarts the watchdog with the initial timing window.
This figure shows what timing windows are used in the different operating modes :

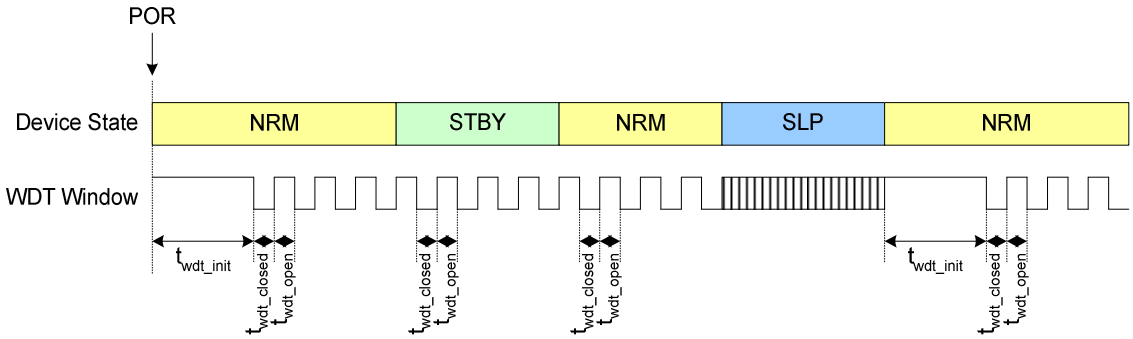


Figure 16 : Window times during different operating modes

The two figures below show the functionality of the watchdog timer :



Figure 17 : Functionality of the window watchdog timer

A reset of the µC due to time-out of the watchdog is achieved by setting the *MR* pin low during a time t_{MR} (default state of the *MR* pin is high).

8.15. Reset Behaviour

Power-On Reset
After a Power-On Reset, the device is operating in Normal Running Mode.
All internal data registers are set to their initial state :

- the device state is Normal Running Mode
- the Watchdog counter is initialized to generate the initial window time
- all registers containing (diagnostic) measurement data are initialized to 0x00
- bits 7, 4, 3 of the Internal Status Flags are cleared
- the user settings registers are set to their initial values (see Section 0)
- the 'Err' register will initialize to 0x00. However, as some voltages are continuously measured, it will reflect immediately if an error is detected or not.

The *MR* pin will be initialized to '1'. The *DR* pin will be initialized to '0', but after the time $t_{startup}$ it will switch to '1' to indicate that the device is ready to accept the first command (see also Section 0).

The output of the *MISO* pin is depending on the *CS* state: if *CS* is high, the *MISO* pin is in tri-state. If *CS* is low, the output of the *MISO* pin is undefined, but either logic high or logic low.

CR Command
At every upload of the CR command, the device returns to the state like it is after a Power-On-Reset, except for the Watchdog counter and the state of the *MR* line. The Watchdog counter and the state of the *MR* line will not be influenced by uploading a CR command. Also, the CR command will not change the contents of bits 1 and 0 of the register 'Rst'.

After a CR command the DR pin will be kept low during a time $t_{startup}$.

Read-out
At the end of each read-out, all registers containing (diagnostic) measurement data are cleared to 0x00.

Watchdog time-out
When a reset occurs due to a watchdog time-out, the *MR* pin will go low for a time t_{MR}. The Watchdog counter will be initialized with the window time t_{wdt_init}. All other states, lines and registers of the ASIC will not be affected.

Changing operation mode
When changing operation mode (RSLP, CSLP, RSTBY, CSTBY, NRM) the right status flags are set.
Changing operation mode will not affect the user settings registers and the (diagnostic) measurement data registers.

The *DR* pin will be set to '0' and after the time t_{wakeup_slp} resp. t_{wakeup_stby} it will be set to '1', when waking up from Sleep resp. Standby Mode.

8.16. Supply Voltage Behaviour

The next figure gives an overview of the behaviour of the POR, the MR/Watchdog and the under/overvoltage error flags for changing power supply voltage.

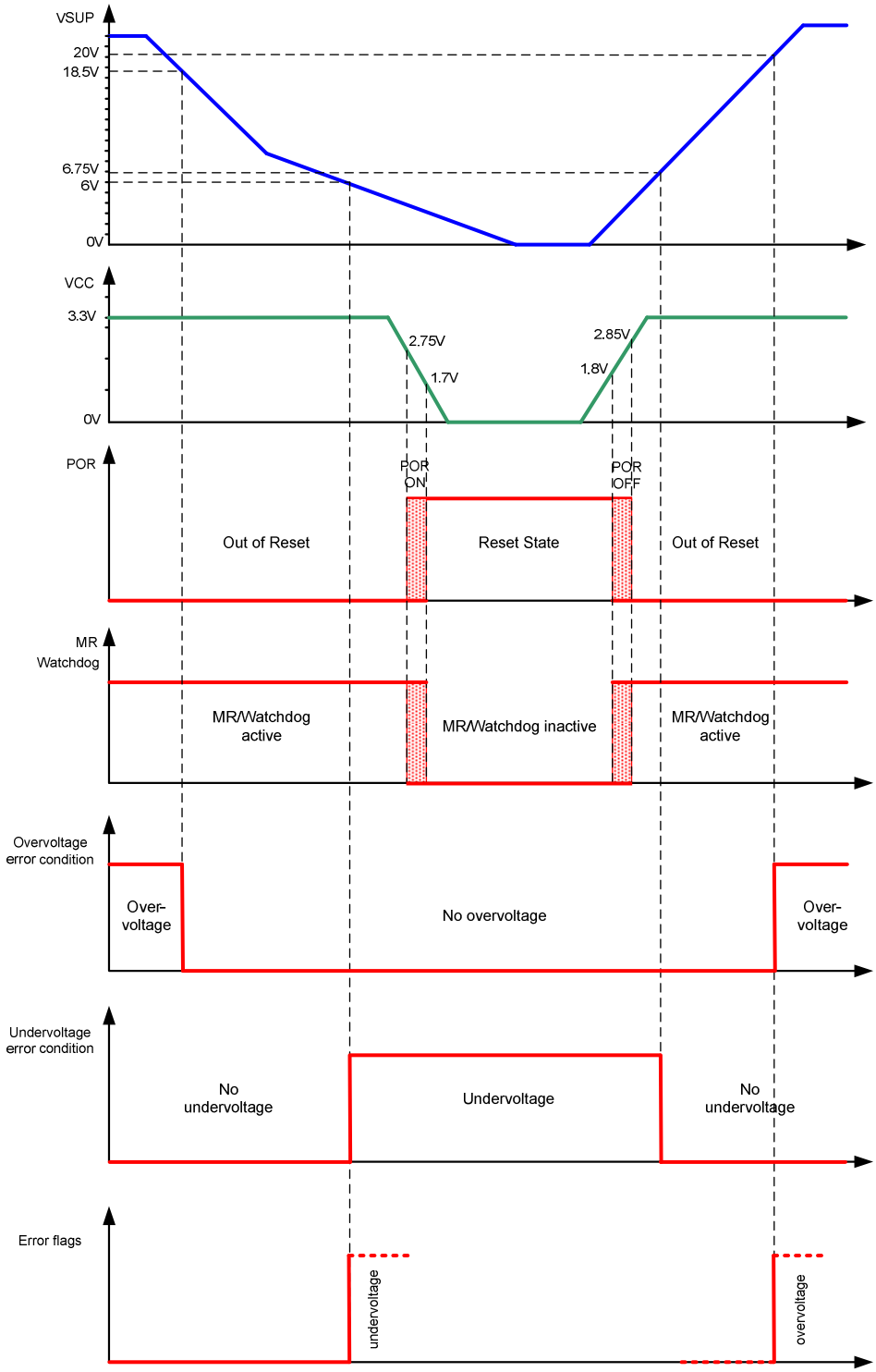


Figure 18 : Supply Voltage Behaviour

8.17. Wake-up from Sleep or Standby

The figure below shows what happens when switching operation mode, and the behaviour of the *DR* pin, the *SLEEPB* pin and the watchdog timer.

When a NRM command is uploaded during Sleep or Standby, the following will happen:
- the *DR* pin goes low for a time t_{wakeup_stby} or t_{wakeup_slp}
- the watchdog timer is initialised and starts counting, when waking up from Sleep
- the device changes to Normal Running Mode, enabling the appropriate blocks
- the *SLEEPB* pin goes high

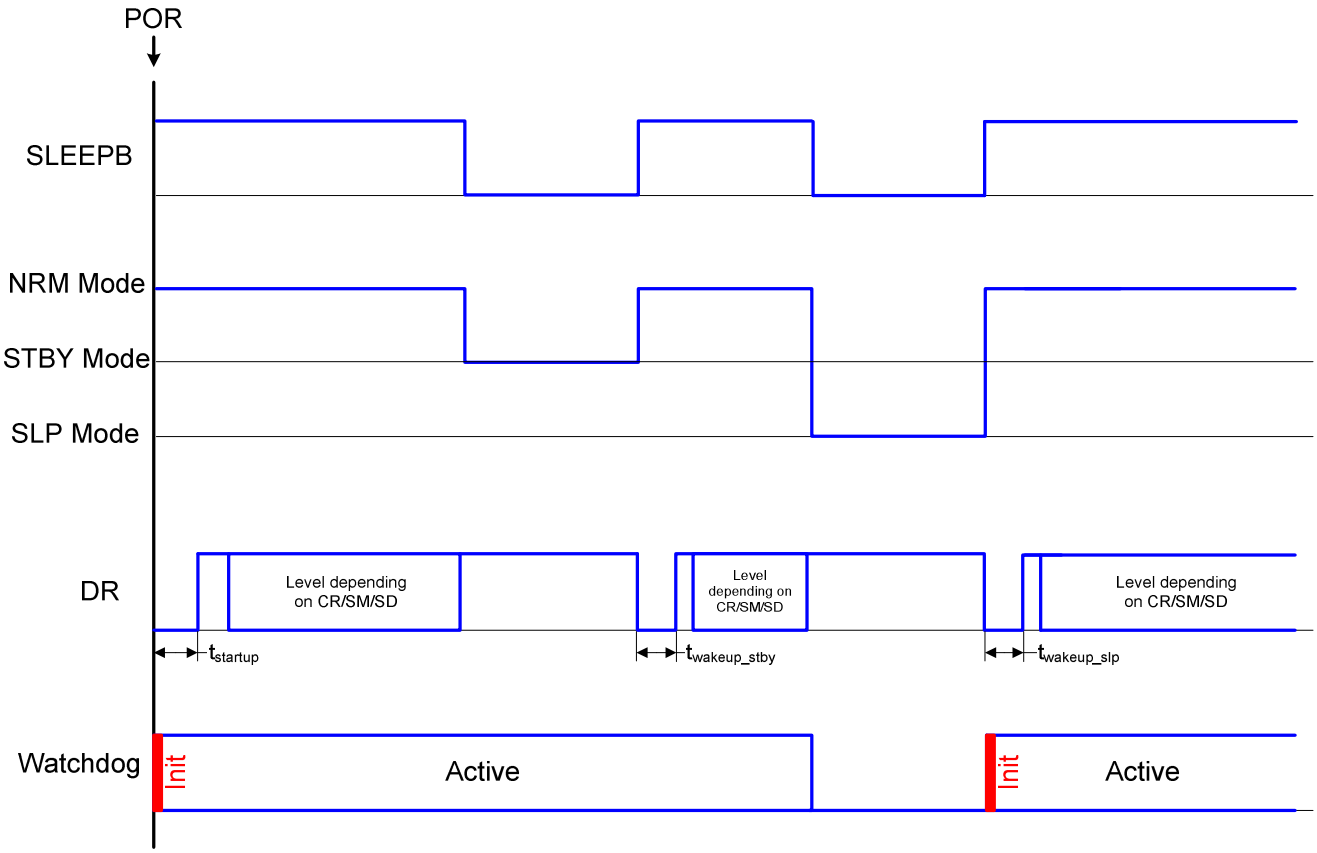


Figure 19 : Behaviour of DR and Watchdog when switching mode

8.18. CRC Calculation

The 8-bit CRC calculation will be based on the polynomial $x^8 + x^2 + x^1 + x^0$. This polynomial is widely used in the industry, it is e.g. used for generating:

- the Header Error Correction field in ATM (Asynchronous Transfer Mode) cells
- the Packet Error Code in SMBus data packets

Some probabilities of detecting errors when using this polynomial:

- 100% detection of one bit errors
- 100% detection of double bit errors (adjacent bits)
- 100% detection of two single-bit errors for frames less than 128 bits in length
- 100% detection of any odd number of bits in error
- 100% detection of burst errors up to 8 bits
- 99.61% detection of any random error

A possible hardware implementation using a Linear Feedback Shift Register (LFSR) is shown in the figure below:

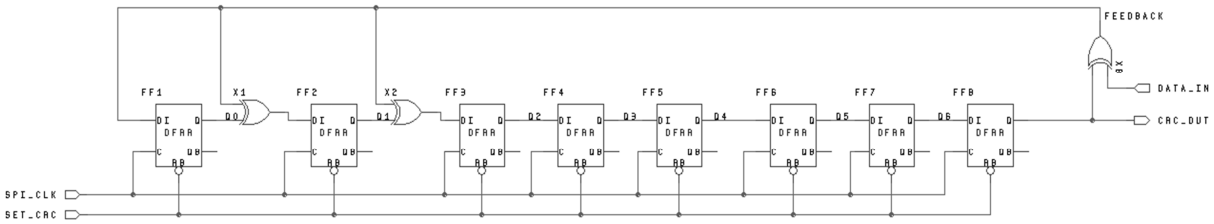


Figure 20 : 8-bit CRC implementation using a LFSR

The generation of the CRC requires the following steps:
Reset all flip-flops
0x00 is the initial value, shifting in all zeroes does not affect the CRC
Shift in the read-out data bytes. First byte is Data Byte 1 (= Internal Status Flags),
last byte is Data Byte (X+1) (with X defined in Figure 12).
When the last byte has been shifted in, the flip-flops contain the CRC: CRC=FF[8..1].

An easy method to check if there were no transmission errors is to calculate the CRC of the whole read-out data stream including the CRC Byte. When the calculated CRC results in 0x00, the transmission was most likely error free. If the resulting CRC is not equal to zero, then an error occurred in the transmission and the complete data stream should be ignored.

Some CRC results for example messages are given in Table 25.

ASCII String messages	CRC result
-None-	0x00
"A"	0xC0
"123456789"	0xF4
a string of 256 upper case "A" characters with no line breaks	0x8E

Table 25 : CRC examples

8.19. Global Timing Diagrams

A global timing diagram with separate SM-RO cycles is given in Figure 21. After power-up there is a Power-On-Reset phase (POR) to initialize the sensor into a reset state. When the device is ready to accept the first command, the *DR* pin goes high. In Figure 21 the first command is the WR command to define the contents of the user registers (optionally). The first measurement cycle is e.g. initiated by uploading a SM command. After completion of the measurement cycle, the *DR* goes high. This indicates that the read-out cycle can be started. A RO command has to be uploaded to bring the data on the *MISO* pin. When the read-out is completed, a new measurement cycle can be started. In Figure 21 a SM command is used. This starts a next measurement cycle. Once *DR* is high, a read-out can be done again.

In between different Measurement/Read-Out cycles, the user registers can be changed with WR commands. Optionally those registers can be read back with the RR command to check if the right values were uploaded.

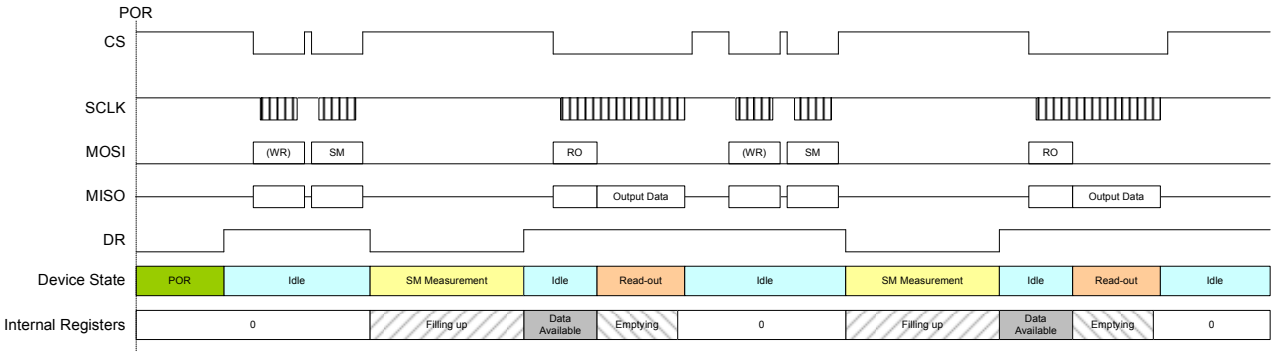


Figure 21 : Global timing diagram with separate SM-RO

Figure 22 shows a timing diagram wherein separate SM-RO cycles are mixed with combined SM-RO cycles. After the Power-On-Reset phase, a SM measurement cycle is started. Once the *DR* pin is high, the data can be read out. A SM command with extra clocks is used to combine the read-out and the start of the next measurement cycle. With the extra clocks, the data of the internal registers is transferred to the *MISO* pin. When the *CS* pin goes high, the next measurement cycle (SM) will be started.
Once the *DR* pin is high, a normal RO command is uploaded to bring the data to the *MISO* pin. If needed, the settings in the user registers can be changed with the WR command and optionally the RR command can be used to check if the right values were uploaded.
A new measurement cycle can be started with e.g. a normal SM command. When the *DR* pin is high, the data can be transferred by uploading e.g. a SM command that combines the read-out and the start of a new measurement cycle.

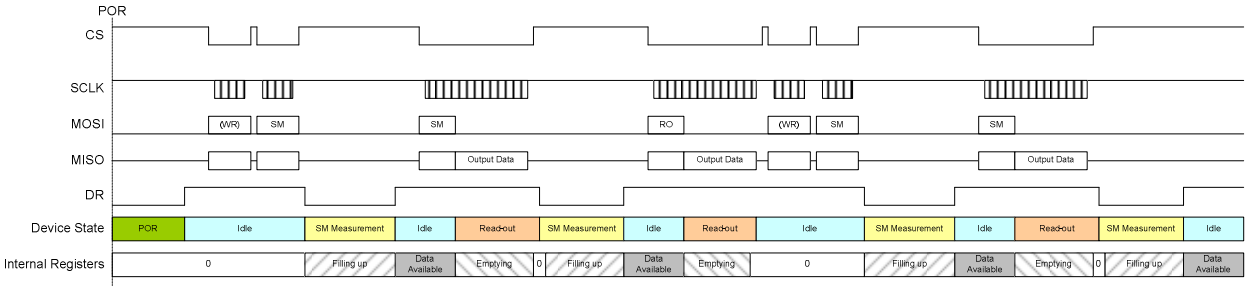


Figure 22: Global timing diagram with separate SM-RO and combined SM-RO together

9. Application Information

9.1. Application circuit

The exact drive circuit for the LEDs, the shunt resistor, photodiodes and power supply filter components can change for each application. The table below summarizes a possible set of external components.
A typical application diagram is shown in Figure 23. Note that the capacitor on Cext has a defined range of 10..100nF, however 68nF is highly recommended to give the best results.

Ambient Detector	Active Light Detector	LED
SFH2270	BPW34FA	SFH4232
SFH3410	VBPW34FA	SFH4250
SFH3710	VBP104FAS	SFH4253
SFH5711	SFH2400FA	SFH4257
SFH2430	SFH2701	VSMY1850X01
BP104S		VSMY3850
TEMD6010FX01		VSMB3940
TEMD6200FX02		
TEMT6000X01		
TEMT6200FX01		

Table 26 : External Components

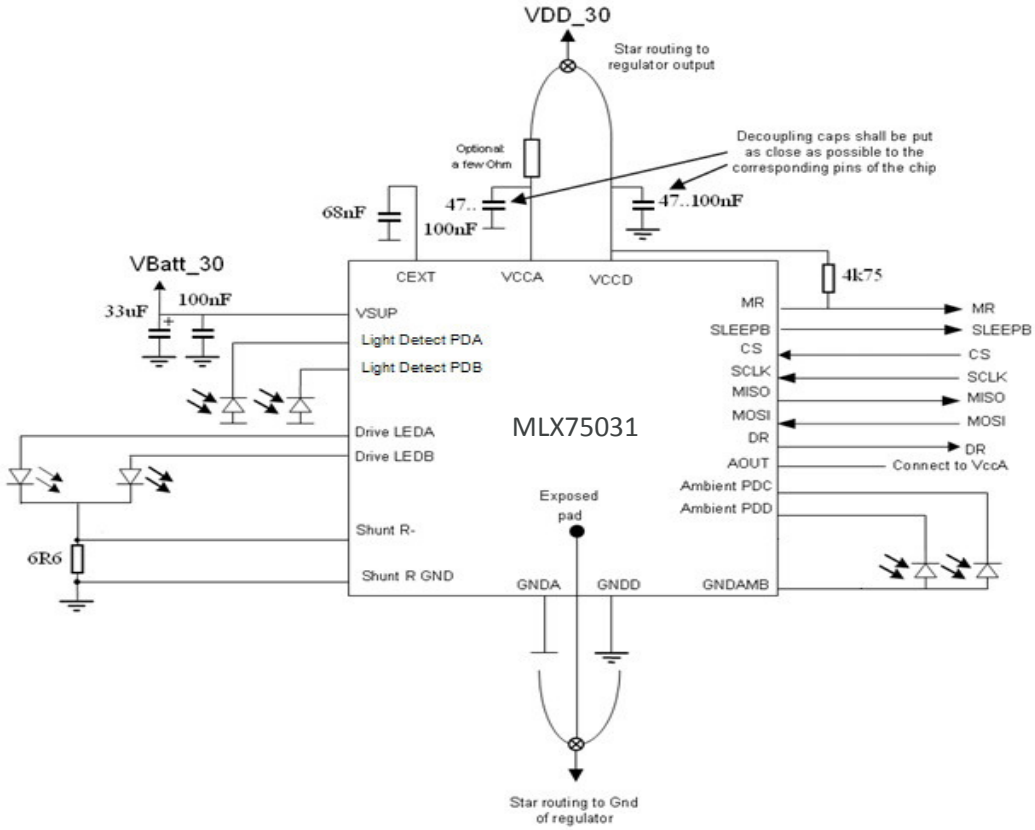


Figure 23 : Typical application circuit

10. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
(classification reflow profiles according to table 5-2)

- EIA/JEDEC JESD22-A113

Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
(reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20

Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat

- EIA/JEDEC JESD22-B106 and EN60749-15

Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15

Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21

Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

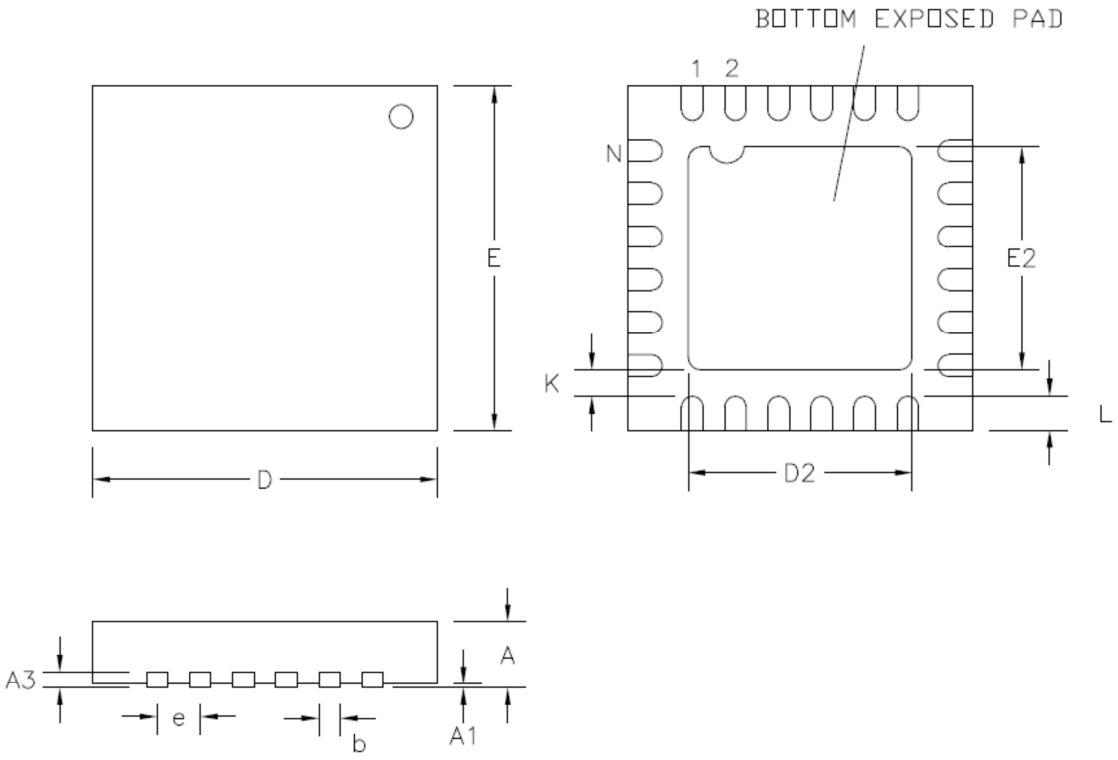
Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: https://www.melexis.com/en/quality-environment

11. General Recommendations - ESD/EMC Precautions

The application circuit board should be designed to minimize electro-magnetic compatibility problems.
The chip is an ESD sensitive device and should be handled according to guideline EN 61340-5-1 (“Protection of electronic devices from electrostatic phenomena”).

12. Package Information

12.1. QFN 4x4 (24 pins): Quad Flat No-lead with exposed pad



	D x E	N	e		A	A1	A3	D2	E2	L	K	b
Quad	All dimensions in mm											
	4 x 4	24	0.50 ±0.05	min	0.80	0.00	0.20 REF	2.50	2.50	0.35	0.20	0.18
				max	1.00	0.05		2.70	2.70	0.45	–	0.30

Table 27 : Package Drawing Dimensions

Package	Θjc [°C/W]	Θja [°C/W] (JEDEC 1s0p board)	Θja [°C/W] (JEDEC 1s2p board)
QFN 4x4	16	154	50

Table 28 : ϑJA values

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