# RX62T Group, RX62G Group
Renesas MCUs

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100-MHz 32-bit RX MCUs, FPU, 165 DMIPS, 12-bit ADC (3 S/H circuits, double data register, amplifier, comparator): two units, 10-bit ADC one unit, the three ADC units are capable of simultaneous 7-ch. sampling, 100-MHz PWM (two three-phase complementary channels and four single-phase complementary channels or three three-phase complementary channels and one single-phase complementary channel)

## Features

### ■ 32-bit RX CPU core
- Max. operating frequency: 100 MHz
  Capable of 165 DMIPS in operation at 100 MHz
- Single precision 32-bit IEEE-754 floating point
- Accumulator handles 64-bit results (for a single instruction) from 32- × 32-bit operations
- Multiplication and division unit handles 32- × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Fast interrupt
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- Background JTAG debugging plus high-speed tracing

### ■ Operating voltage
- Single 3.3- or 5-V supply; 5-V analog supply is possible with 3.3-V products

### ■ Low-power design and architecture
- Four low-power modes

### ■ On-chip main flash memory, no wait states
- 100-MHz operation, 10-ns read cycle
- No wait states for reading at full CPU speed
- 64-Kbyte/128-Kbyte/256-Kbyte capacities
- For instructions and operands
- User code programmable via the SCI or JTAG

### ■ On-chip data flash memory
- Max. 32 Kbytes, reprogrammable up to 30,000 times
- Erasing and programming impose no load on the CPU.

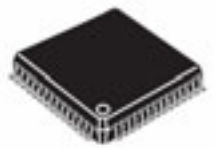
### ■ On-chip SRAM, no wait states
- 8-Kbyte/16-Kbyte SRAM
- For instructions and operands

### ■ DMA
- DTC: The single unit is capable of transfer on multiple channels

### ■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

### ■ Clock functions
- External crystal oscillator or internal PLL for operation at 8 to 12.5 MHz
- Internal 125-kHz LOCO for the IWDT
- Detection of main oscillator stoppage (for IEC 60730 compliance)

### ■ Independent watchdog timer (for IEC60730compliance)
- 125-kHz LOCO clock operation
- Software is incapable of stopping the robust WDT.



PLQP0112JA-A 20×20mm, 0.65mm pitch
PLQP0100KB-A 14×14mm, 0.5mm pitch
PLQP0080JA-A 14×14mm, 0.65mm pitch
PLQP0064KB-A 10×10mm, 0.5mm pitch
PLQP0064GA-A 14x14 mm, 0.8mm pitch

### ■ Up to 7 communications interfaces
- 1: CAN (compliant with ISO11898-1), incorporating 32 mailboxes
- 3: SCIs, with asynchronous mode (incorporating noise cancellation), clock-synchronous mode, and smart-card interface mode
- 1: I2C bus interface, capable of SMBus operation
- 1: RSPI
- 1: LIN

### ■ Up to 16 16-bit timers
- 8: 16-bit MTU3: 100-MHz operation, input capture, output compare, two three-phase complementary PWM output channels, complementary PWM imposing no load on the CPU, phase-counting mode
- 4: 16-bit GPT: 100-MHz operation, input capture, output compare, four complementary single-phase PWM output channels, or one three-phase complementary PWM output channel and one single-phase complementary PWM output channel, complementary PWM imposing no load on the CPU, operation linked with comparator (for counting and control of PWM-signal negation), detection of abnormal oscillation frequencies (for IEC 60730 compliance)
- 4: 16-bit CMT

### ■ Generation of delays in PWM waveforms (only for the RX62G Group)
- The timing with which signals on the 16-bit GPT PWM output pin rise and fall can be controlled with an accuracy of up to 312 ps (in operation at 100 MHz).

### ■ Three A/D converter units for 1-MHz operation, for a total of 20 channels
- Three units are capable of simultaneous sampling on seven channels
- Self diagnosis (for IEC60730 compliance)
- 8: Two 12-bit ADC units: three sample-and-hold circuits, double data registers, amplifier, comparator
- 12: Single 10-bit ADC unit

### ■ CRC (cyclic redundancy check) calculation unit
- Monitoring of data being transferred (for IEC 60730 compliance)
- Monitoring of data in memory (for IEC 60730 compliance)

### ■ Up to 61 input–output ports and up to 21 input-only ports
- PORT registers: Monitoring of output ports (for IEC 60730 compliance)

### ■ Operating temp. range
- –40°C to +85°C
- –40°C to +105°C

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

**Table 1.1 Outline of Specifications (1 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | • Maximum operating frequency: 100MHz<br>• 32-bit RX CPU<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>• General purpose: Sixteen 32-bit registers<br>• Control: Nine 32-bit registers<br>• Accumulator: One 64-bit register<br>• Basic instructions: 73<br>• Floating-point instructions: 8<br>• DSP instructions: 9<br>• Addressing modes: 10<br>• Data arrangement<br>• Instructions: Little endian<br>• Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 x 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits<br>• Memory-protection unit (MPU) |
| | FPU | • Single precision (32-bit) floating point<br>• Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | ROM | • ROM capacity: 256 Kbytes (max.)<br>• Two on-board programming modes<br>• Boot mode (The user MAT is programmable via the SCI)<br>• User program mode<br>• Off-board programming<br>• A PROM programmer can be used to program the user mat. |
| | RAM | • RAM capacity: 16 Kbytes (max.) |
| | Data flash | • Data flash capacity: 32 Kbytes (max.)<br>• Supports background operations (BGO) |
| MCU operating mode | | • Single-chip mode |
| Clock | Clock generation circuit | • One circuit: Main clock oscillator<br>• Internal oscillator: Low-speed on-chip oscillator dedicated to IWDT<br>• Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency<br>• Oscillation stoppage detection<br>• Independent frequency-division and multiplication settings for the system clock (ICLK) and peripheral module clock (PCLK)<br>• The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the system clock (ICLK): 8 to 100 MHz.<br>• Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz |
| Reset | | Pin reset, power-on reset (automatic power-on reset when the power is turned on), voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset |
| Voltage detection circuit (LVD) | | When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated. |
| Low power consumption | Low power consumption facilities | • Module stop function<br>• Four low power consumption modes<br>• Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |

**Table 1.1 Outline of Specifications (2 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Interrupt | Interrupt controller (ICU) | • Peripheral function interrupts: 101 sources<br>• External interrupts: 9 (NMI and IRQ0 to IRQ7 pins)<br>• Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt)<br>• 16 levels specifiable for the order of priority |
| Data transfer | Data transfer controller (DTC) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| I/O ports | Programmable I/O ports | I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/<br>80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP<br>• I/O: 61/55/44/44/37<br>• Input only: 21/21/13/13/9<br>• Open-drain outputs: 2/2/2/2/2 ($I^2C$ bus interface pins)<br>• Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins)<br>The 5-V version of the 64-pin product does not have large-current outputs.<br>• Reading out the states of pins is always possible. |
| Timers | Multi-function timer pulse unit 3 (MTU3) | • 16 bits x 8 channels<br>• Up to 24 pulse inputs/outputs and three pulse inputs<br>• Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available.<br>• 24 output compare or input capture registers<br>• Counter clearing (clearing is synchronizable with compare match or input capture)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Input to and output from all registers in synchronization with counter operation<br>• Buffered operation<br>• Cascade-connected operation<br>• 38 kinds of interrupt source<br>• Automatic transfer of register data<br>• Pulse output modes<br>Toggled, PWM, complementary PWM, and reset synchronous PWM<br>• Complementary PWM output mode<br>Outputs non-overlapping waveforms for controlling 3-phase inverters<br>Automatic specification of dead times<br>PWM duty cycle: Selectable as any value from 0% to 100%<br>Delay can be applied to requests for A/D conversion.<br>Non-generation of interrupt requests at peak or trough values of counters can be selected.<br>Double buffering<br>• Reset-synchronous PWM mode<br>Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles.<br>• Phase-counting mode<br>• Counter functionality for dead-time compensation<br>• Generation of triggers for A/D converters<br>• Differential timing for initiation of A/D conversion |
| | Port output enable 3 (POE3) | • Control of the high-impedance state of the MTU3 and GPT's waveform output pins<br>5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11<br>Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level)<br>Initiation by comparator-detection of analog level input to the 12-bit A/D converter<br>Initiation by oscillation-stoppage detection<br>Initiation by software<br>• Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection |

**Table 1.1 Outline of Specifications (3 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | General PWM timer (GPT/GPTa) | • 16 bits x 4 channels<br>• Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels<br>• Clock sources independently selectable for all channels<br>• 2 input/output pins per channel<br>• 2 output compare/input capture registers per channel<br>• For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use.<br>• In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms.<br>• Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow)<br>• Synchronizable operation of the several counters<br>• Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting)<br>• Generation of dead times in PWM operation<br>• Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times<br>• Starting, clearing, and stopping counters in response to external or internal triggers<br>• Internal trigger sources: output of the internal comparator detection, software, and compare-match<br>• The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation).<br>• PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall with an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for GPTa). |
| | Compare match timer (CMT) | • (16 bits x 2 channels) x 2 units<br>• Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Watchdog timer (WDT) | • 8 bits x 1 channel<br>• Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072)<br>• Switchable between watchdog timer mode and interval timer mode |
| | Independent watchdog timer (IWDT) | • 14 bits x 1 channel<br>• Counter-input clock: low-speed on-chip oscillator dedicated to IWDT |
| Communications | Serial communications interface (SCIb) | • 3 channels<br>• Serial communications modes:<br>Asynchronous, clock synchronous, and smart-card interface<br>• Multiprocessor communications<br>• On-chip baud rate generator allows selection of the desired bit rate<br>• Choice of LSB-first or MSB-first transfer<br>• Noise cancellation (only available in asynchronous mode) |
| | $I^2C$ bus interface (RIIC) | • 1 channel<br>• Communications formats<br>$I^2C$ bus format/SMBus format<br>Master/slave selectable |

**Table 1.1 Outline of Specifications (4 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Communications | CAN module (CAN) (as an optional function) | • 1 channel<br>• 32 mailboxes |
| | Serial peripheral interface (RSPI) | • 1 unit<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Buffered structure<br>• Double buffers for both transmission and reception |
| | LIN module (LIN) | • 1 channel (LIN master)<br>• Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol |
| A/D converter | 12-bit A/D converter (S12ADA) | • 12 bits (2 units x 4 channels)<br>• 12-bit resolution<br>• Conversion time:<br>1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V<br>2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.)<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>Additionally, sample-and-hold circuit for each unit is included. (three channels per unit)<br>• A/D-conversion register settings for each input pin.<br>• Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100).<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8- or 10-bit precision output<br>Right-shifting of the results of conversion for output by two or four bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0).<br>• Amplification of input signals by a programmable gain amplifier (three channels per unit)<br>Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps)<br>• Window comparators (three channels per unit) |

**Table 1.1 Outline of Specifications (5 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| A/D converter | 10-bit A/D converter (ADA) | • 10 bits (1 unit x 12 channels)<br>• 10-bit resolution<br>• Conversion time:<br>1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V<br>2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>• A/D-conversion register settings for each input pin<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8-bit precision output<br>Right-shifting the results of conversion for output by two bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF). |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Operating frequency | | ICLK: 8 to 100 MHz<br>PCLK: 8 to 50 MHz |
| Power supply voltage | | • 3-V version<br>VCC = PLLVCC = 2.7 to 3.6V<br>AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V<br>VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0<br>VREF = 3.0 to AVCC, or 4.0 to AVCC<br>• 5-V version<br>VCC = PLLVCC = 4.0 to 5.5V<br>AVCC0 = AVCC = 4.0 to 5.5V<br>VREFH0 = 4.0 to AVCC0<br>VREF = 4.0 to AVCC |
| Operating temperature | | D version: -40 to +85°C, G version: -40 to +105°C*1 |
| Packages | | 112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch)<br>100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch)<br>80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch)<br>64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch)<br>64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch) |

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

**Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)**

| Functions | | RX62G Group | | RX62T Group | | | | |
|---|---|---|---|---|---|---|---|---|
| Pin number | | 112 Pins | 100 Pins | 112 Pins | 100 Pins | 80 Pins (R5F562TxGDFF) | 80 Pins | 64 Pins |
| Data transfer | Data transfer controller (DTC) | √ | | | | | | |
| Interrupt controller (ICU) | Input on the NMI pin | √ | | | | | | |
| | Input on the IRQ pins | √ (8) | | | | | | √ (4) |
| Timers | Multi-function timer pulse unit 3 (MTU3) | √ | | | | √*1 | | |
| | General PWM timer (GPT) | — | | √ | | √*1 | | |
| | General PWM timer (GPTa) | √ | | — | | | | |
| | MTU3/GPT complementary PWM pin | 12 | | | | | 6 | |
| | Port output enable 3 (POE3) | √ (POE pins: 5) | | | | | | √ (POE pins: 3) |
| | Compare match timer (CMT) | √ | | | | | | |
| | Watchdog timer (WDT) | √ | | | | | | |
| | Independent watchdog timer (IWDT) | √ | | | | | | |
| Communication function | Serial communications interface (SCI) | √ | | | | | | |
| | I²C bus interface (RIIC) | √ | | | | | | |
| | CAN module (CAN) (as an optional function) | √ | | | | | | |
| | LIN module (LIN) | √ | | | | | | |
| | Serial peripheral interface (RSPI) | √ | | | | | | |
| 12-bit A/D converter (S12ADA) | | √ (4 ch. x 2 units) | | | | | | |
| | Simultaneous sampling on three channels | √ (2 units) | | | | | | |
| | Programmable gain amplifier | √ (3 ch. x 2 units) | | | | | | |
| | Window comparator | √ (3 ch. x 2 units) | | | | | | |
| 10-bit A/D converter (ADA) | | √ (12 ch.) | | | | √ (4 ch.) | | — |
| CRC calculator (CRC) | | √ | | | | | | |
| I/O ports | I/O pins | 61 | 55 | 61 | 55 | 44 | 44 | 37 |
| | Input pins | 21 | 21 | 21 | 21 | 13 | 13 | 9 |

**Table 1.2 Functions of RX62T Group and RX62G Group Products (2 / 2)**

| Functions | RX62G Group | | RX62T Group | | | | |
|---|---|---|---|---|---|---|---|
| **Pin number** | **112 Pins** | **100 Pins** | **112 Pins** | **100 Pins** | **80 Pins (R5F562T xGDFF)** | **80 Pins** | **64 Pins** |
| Package | LQFP2020 (0.65-mm pitch) | LQFP1414 (0.5-mm pitch) | LQFP2020 (0.65-mm pitch) | LQFP1414 (0.5-mm pitch) | LQFP1414 (0.65-mm pitch) | LQFP1414 (0.65-mm pitch) | LQFP1010 (0.5-mm pitch) LQFP1414 (0.8-mm pitch) |

O: Supported, —: Not supported

Note 1. For the MTU and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. See Table 1.3 for details.

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products (1 / 2)**

| Group | Part No. | Order Part No. | Package | ROM Capacity | RAM Capacity | Data Flash Capacity | Power Supply Voltage | CAN | Operating Temp. Range |
|---|---|---|---|---|---|---|---|---|---|
| RX62T | R5F562TAADFH | R5F562TAADFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V | Support-ed | -40 to +85°C (D version) |
| | R5F562TAADFP | R5F562TAADFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562TAADFF | R5F562TAADFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TAGDFF | R5F562TAGDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TAADFM | R5F562TAADFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562TAADFK | R5F562TAADFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T7ADFH | R5F562T7ADFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562T7ADFP | R5F562T7ADFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562T7ADFF | R5F562T7ADFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7GDFF | R5F562T7GDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7ADFM | R5F562T7ADFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T7ADFK | R5F562T7ADFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T6ADFF | R5F562T6ADFF#V3 | PLQP0080JA-A | 64 Kbytes | 8 Kbytes | | | | |
| | R5F562T6ADFM | R5F562T6ADFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T6ADFK | R5F562T6ADFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562TABDFH | R5F562TABDFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V | | |
| | R5F562TABDFP | R5F562TABDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562TABDFF | R5F562TABDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TABDFM | R5F562TABDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562TABDFK | R5F562TABDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T7BDFH | R5F562T7BDFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562T7BDFP | R5F562T7BDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562T7BDFF | R5F562T7BDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7BDFM | R5F562T7BDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T7BDFK | R5F562T7BDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T6BDFF | R5F562T6BDFF#V3 | PLQP0080JA-A | 64 Kbytes | 8 Kbytes | | | | |
| | R5F562T6BDFM | R5F562T6BDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T6BDFK | R5F562T6BDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562TADDFH | R5F562TADDFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | 4.0 to 5.5 V | Not Support-ed | |
| | R5F562TADDFP | R5F562TADDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562TADDFF | R5F562TADDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TADDFM | R5F562TADDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562TADDFK | R5F562TADDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T7DDFH | R5F562T7DDFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562T7DDFP | R5F562T7DDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562T7DDFF | R5F562T7DDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7DDFM | R5F562T7DDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T7DDFK | R5F562T7DDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T6DDFF | R5F562T6DDFF#V3 | PLQP0080JA-A | 64 Kbytes | 8 Kbytes | | | | |
| | R5F562T6DDFM | R5F562T6DDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T6DDFK | R5F562T6DDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562TAEDFH | R5F562TAEDFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | 2.7 to 3.6 V | | |
| | R5F562TAEDFP | R5F562TAEDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562TAEDFF | R5F562TAEDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TAEDFM | R5F562TAEDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562TAEDFK | R5F562TAEDFK#V3 | PLQP0064GA-A | | | | | | |

**Table 1.3 List of Products (2 / 2)**

| Group | Part No. | Order Part No. | Package | ROM Capacity | RAM Capacity | Data Flash Capacity | Power Supply Voltage | CAN | Operating Temp. Range |
|---|---|---|---|---|---|---|---|---|---|
| RX62T | R5F562T7EDFH | R5F562T7EDFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | 2.7 to 3.6 V | Not Support-ed | -40 to +85°C (D version) |
| | R5F562T7EDFP | R5F562T7EDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562T7EDFF | R5F562T7EDFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7EDFM | R5F562T7EDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T7EDFK | R5F562T7EDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T6EDFF | R5F562T6EDFF#V3 | PLQP0080JA-A | 64 Kbytes | 8 Kbytes | | | | |
| | R5F562T6EDFM | R5F562T6EDFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T6EDFK | R5F562T6EDFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562TAAGFH | R5F562TAAGFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V | Support-ed | -40 to +105°C (G version) *1 |
| | R5F562TAAGFP | R5F562TAAGFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562TAAGFF | R5F562TAAGFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TAGGFF | R5F562TAGGFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TAAGFM | R5F562TAAGFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562TAAGFK | R5F562TAAGFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T7AGFH | R5F562T7AGFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562T7AGFP | R5F562T7AGFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562T7AGFF | R5F562T7AGFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7GGFF | R5F562T7GGFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7AGFM | R5F562T7AGFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T7AGFK | R5F562T7AGFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T6AGFF | R5F562T6AGFF#V3 | PLQP0080JA-A | 64 Kbytes | 8 Kbytes | | | | |
| | R5F562T6AGFM | R5F562T6AGFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T6AGFK | R5F562T6AGFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562TABGFH | R5F562TABGFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V | | |
| | R5F562TABGFP | R5F562TABGFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562TABGFF | R5F562TABGFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562TABGFM | R5F562TABGFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562TABGFK | R5F562TABGFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T7BGFH | R5F562T7BGFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562T7BGFP | R5F562T7BGFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562T7BGFF | R5F562T7BGFF#V3 | PLQP0080JA-A | | | | | | |
| | R5F562T7BGFM | R5F562T7BGFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T7BGFK | R5F562T7BGFK#V3 | PLQP0064GA-A | | | | | | |
| | R5F562T6BGFF | R5F562T6BGFF#V3 | PLQP0080JA-A | 64 Kbytes | 8 Kbytes | | | | |
| | R5F562T6BGFM | R5F562T6BGFM#V3 | PLQP0064KB-A | | | | | | |
| | R5F562T6BGFK | R5F562T6BGFK#V3 | PLQP0064GA-A | | | | | | |
| RX62G | R5F562GAADFH | R5F562GAADFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V | Support-ed | -40 to +85°C (D version) |
| | R5F562GAADFP | R5F562GAADFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562G7ADFH | R5F562G7ADFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562G7ADFP | R5F562G7ADFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562GADDFH | R5F562GADDFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | | Not Support-ed | |
| | R5F562GADDFP | R5F562GADDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562G7DDFH | R5F562G7DDFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562G7DDFP | R5F562G7DDFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562GAAGFH | R5F562GAAGFH#V3 | PLQP0112JA-A | 256 Kbytes | 16 Kbytes | 32 Kbytes | VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V | Support-ed | -40 to +105°C (G versio) *1 |
| | R5F562GAAGFP | R5F562GAAGFP#V3 | PLQP0100KB-A | | | | | | |
| | R5F562G7AGFH | R5F562G7AGFH#V3 | PLQP0112JA-A | 128 Kbytes | 8 Kbytes | 8 Kbytes | | | |
| | R5F562G7AGFP | R5F562G7AGFP#V3 | PLQP0100KB-A | | | | | | |

Note 1. Please contact us if you are using a G version.

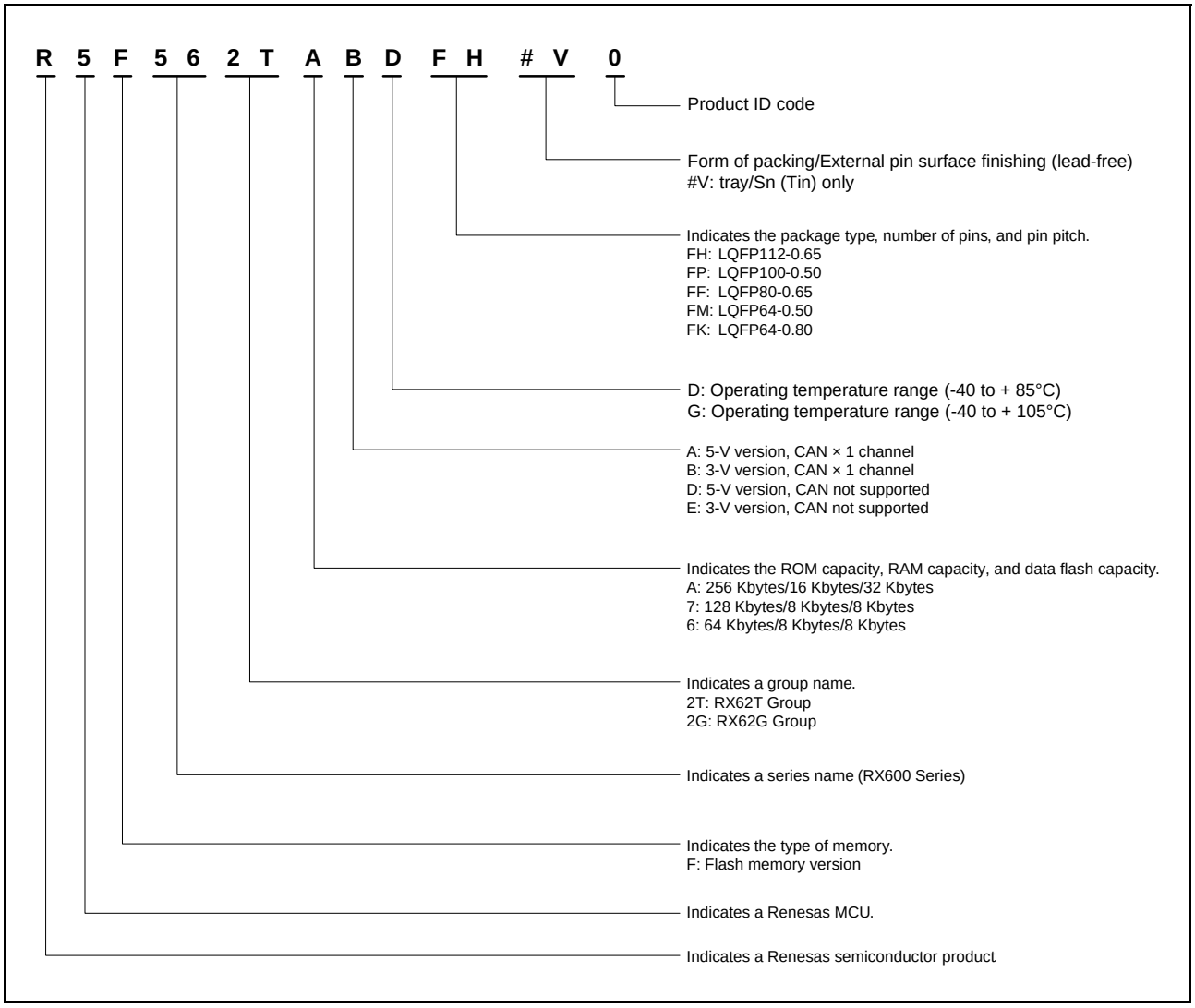
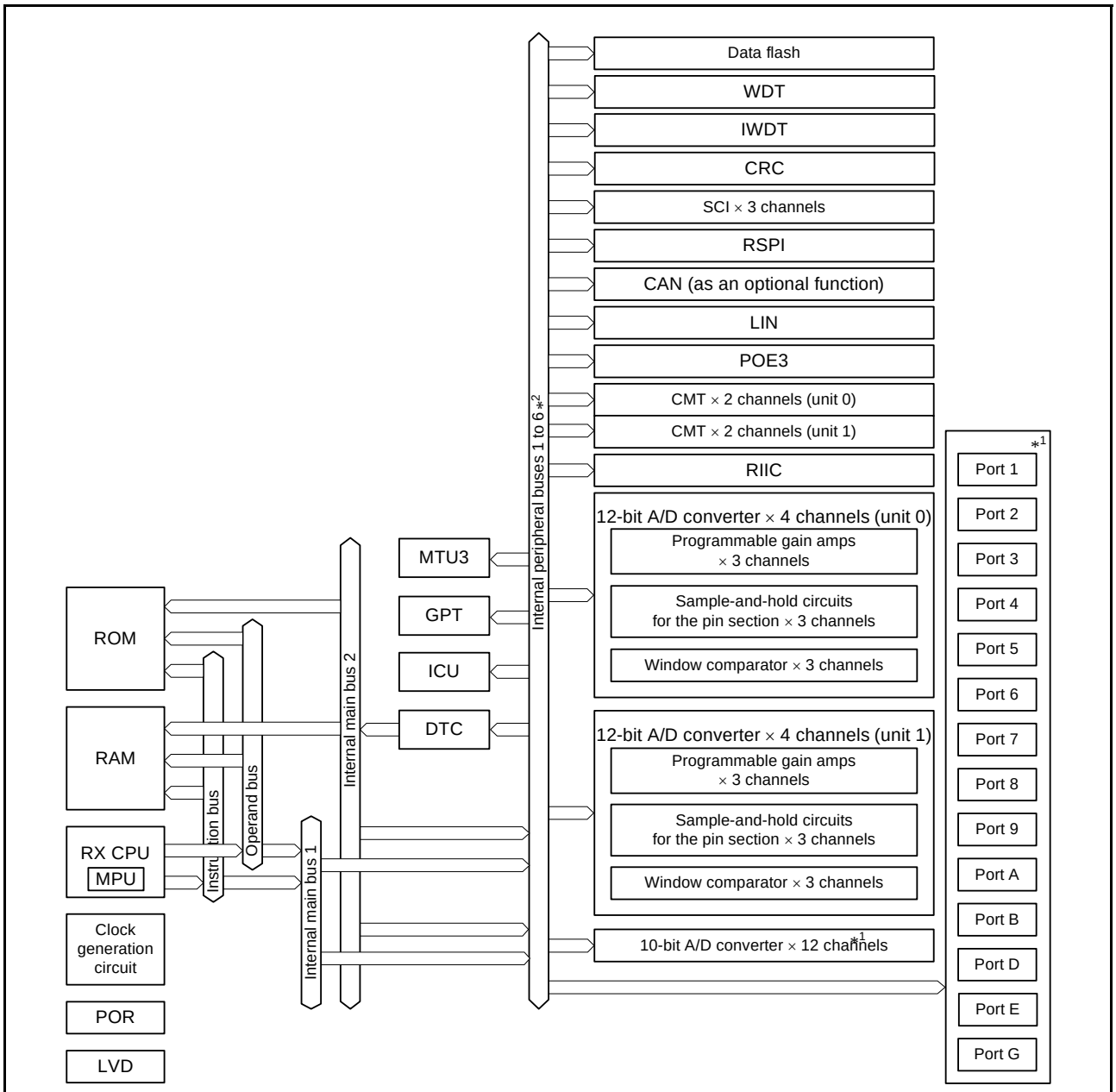



**Figure 1.1 How to Read the Product Part No.**

## 1.3 Block Diagram

Figure 1.2 shows a block diagram.




[Legend]

| | | | |
|---|---|---|---|
| POR: | Power-on reset circuit | CAN: | CAN module |
| DTC: | Data transfer controller | LIN: | LIN module |
| MTU3: | Multi-function timer pulse unit 3 | RSPI: | Renesas serial peripheral interface |
| POE3: | Port output enable 3 | LVD: | Voltage detection circuit |
| GPT: | General PWM timer | ICU: | Interrupt controller |
| CMT: | Compare match timer | WDT: | Watchdog timer |
| SCI: | Serial communications interface | IWDT: | Independent watchdog timer |
| RIIC: | $I^2C$ bus interface | CRC: | CRC (cyclic redundancy check) calculator |
| MPU: | Memory-Protection Unit | | |

Notes: 1. The installation of the 10-bit A/D converter and ports 1 to G is different depending on the package.
2. For details on the internal peripheral bus configuration, see section 12, Buses in the User's manual: Hardware.

**Figure 1.2 Block Diagram**

## 1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

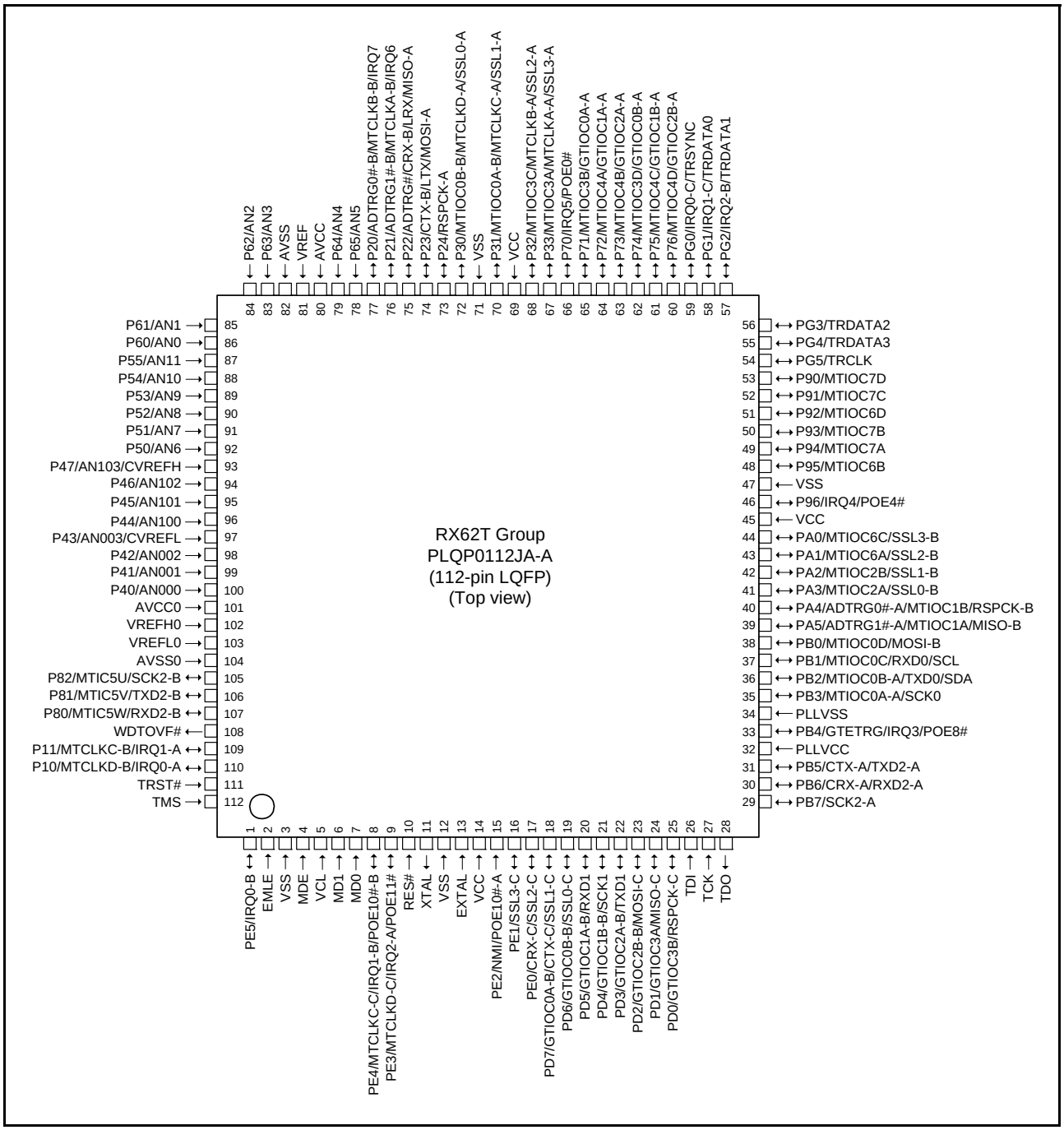



**Figure 1.3 Pin Assignment of the 112-Pin LQFP**

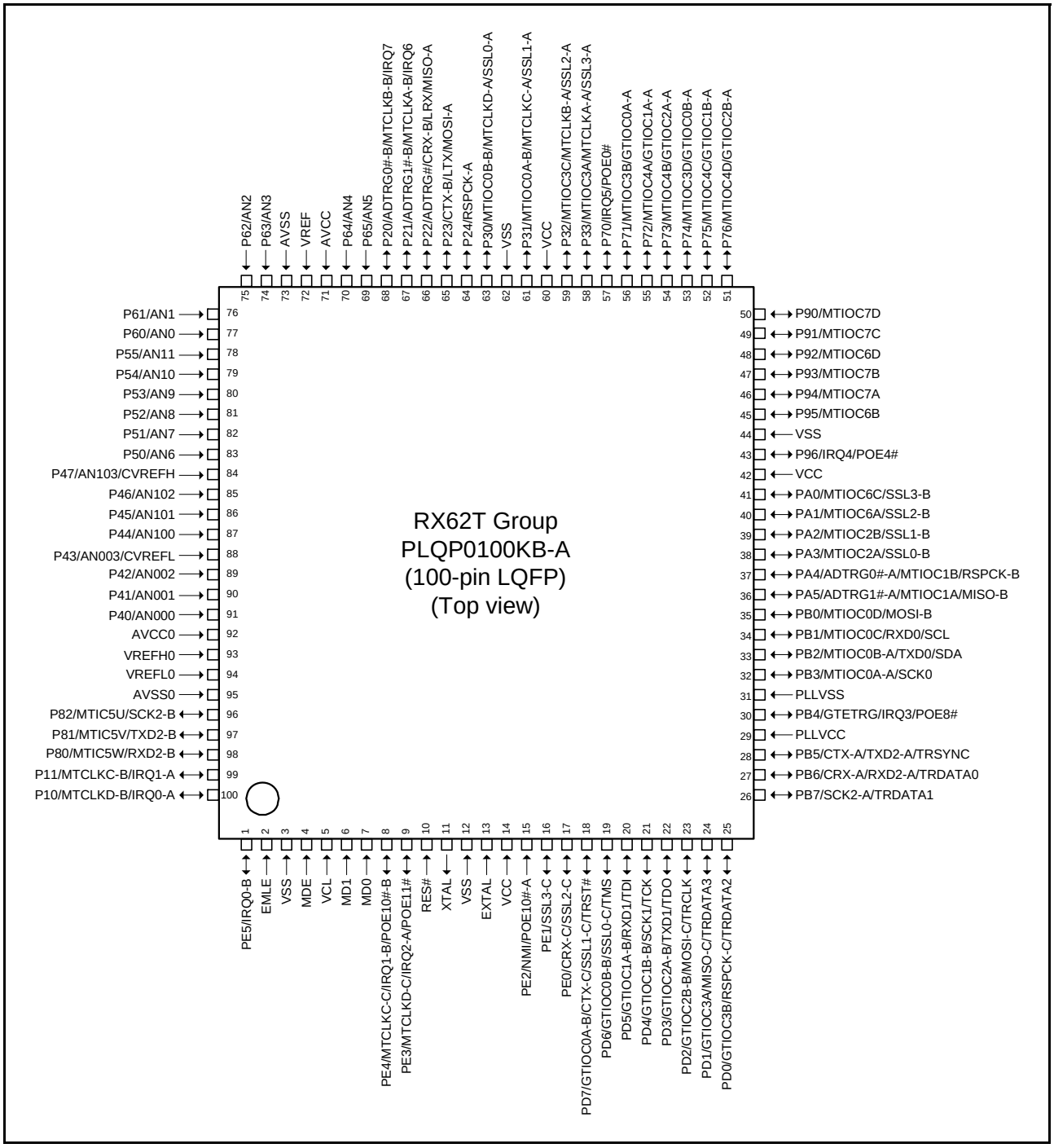



**Figure 1.4 Pin Assignment of the 100-Pin LQFP**

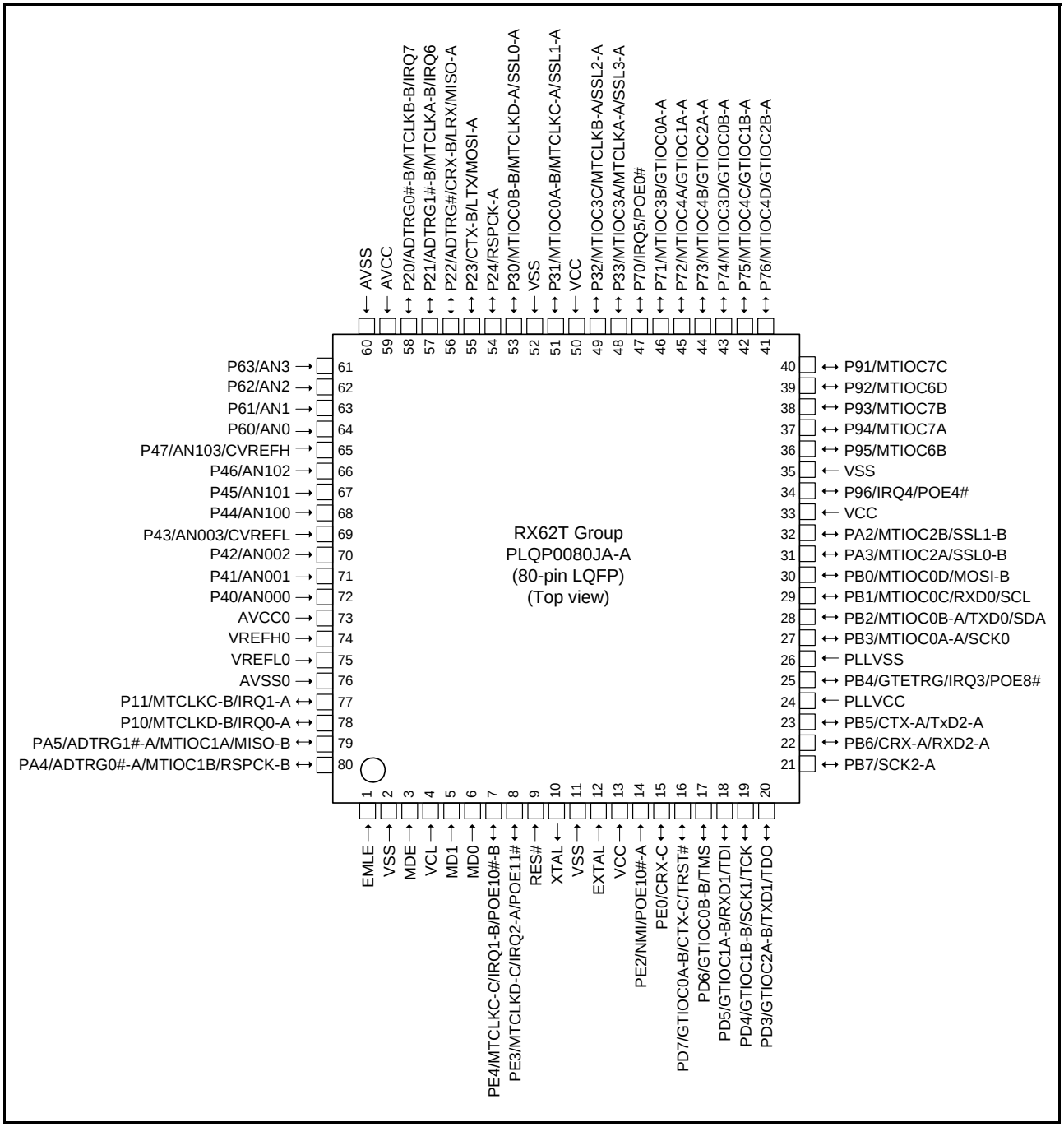



**Figure 1.5 Pin Assignment of the 80-Pin LQFP**

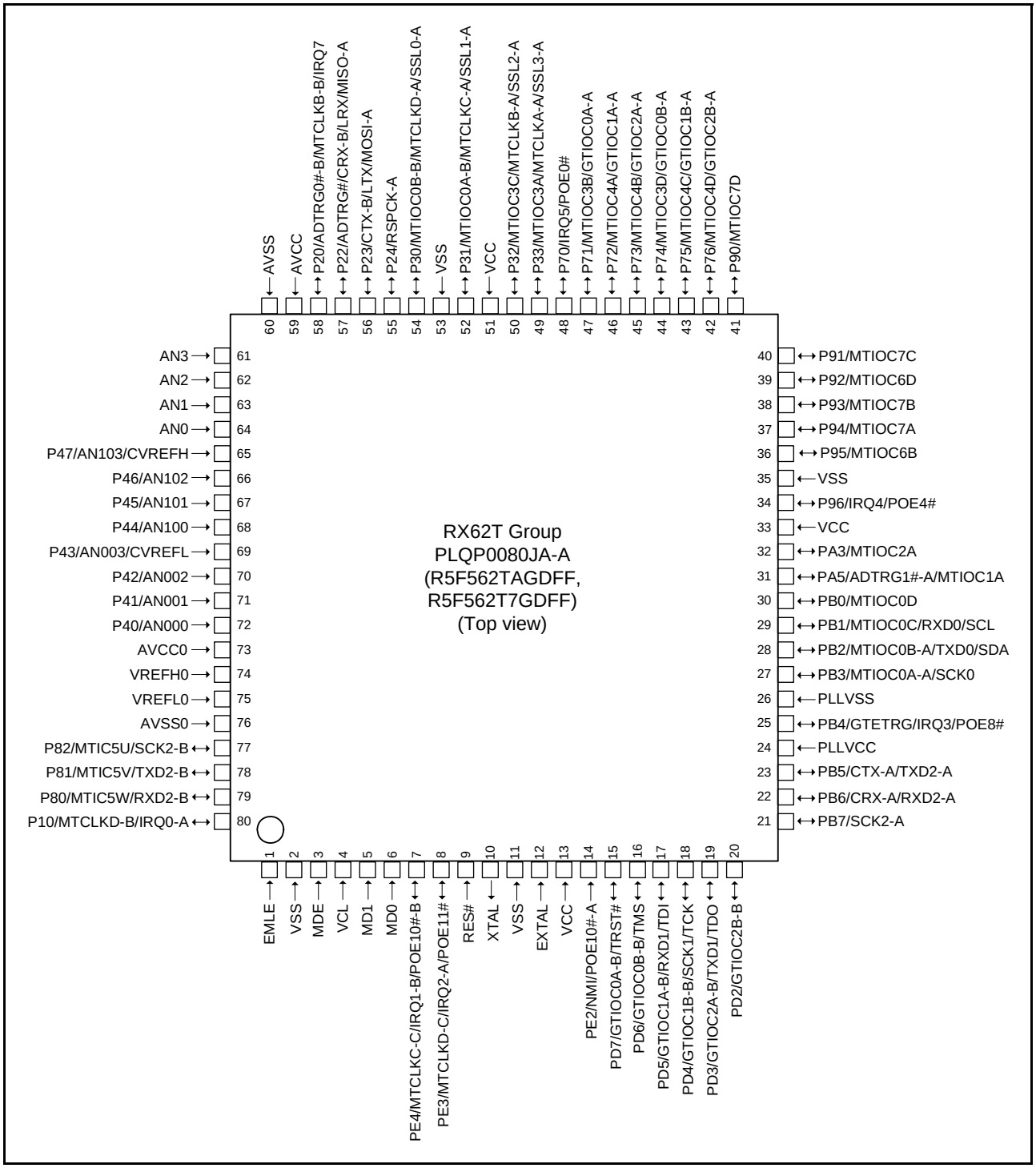



**Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)**

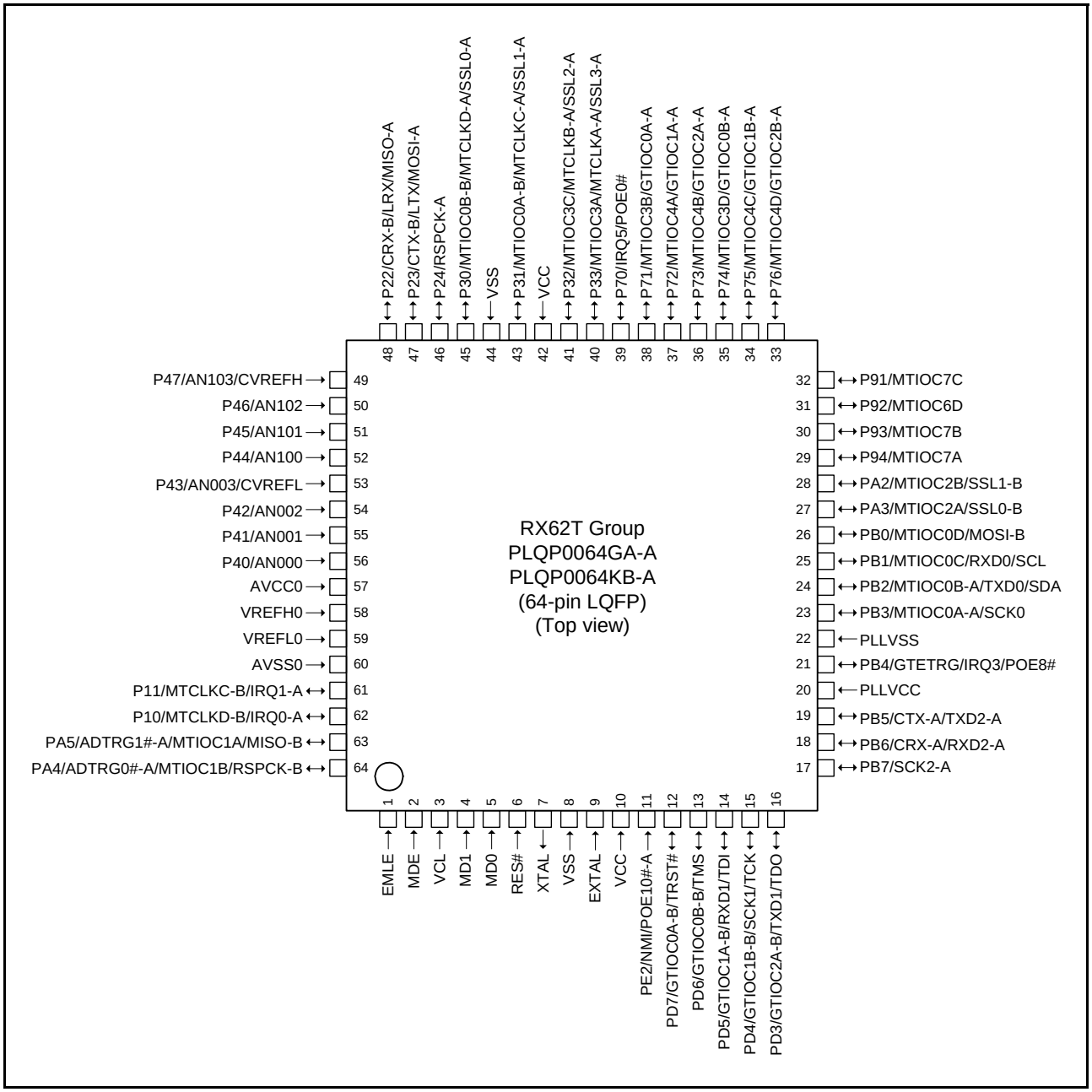



**Figure 1.7 Pin Assignment of the 64-Pin LQFP**

**Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)**

| Pin No. (112-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | | PE5 | | | | IRQ0-B | | |
| 2 | EMLE | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | MDE | | | | | | | |
| 5 | VCL | | | | | | | |
| 6 | MD1 | | | | | | | |
| 7 | MD0 | | | | | | | |
| 8 | | PE4 | | MTCLKC-C | | IRQ1-B | POE10#-B | |
| 9 | | PE3 | | MTCLKD-C | | IRQ2-A | POE11# | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | | PE2 | | | | NMI | POE10#-A | |
| 16 | | PE1 | | | SSL3-C | | | |
| 17 | | PE0 | | | CRX-C/ SSL2-C | | | |
| 18 | | PD7 | | GTIOC0A-B | CTX-C/ SSL1-C | | | |
| 19 | | PD6 | | GTIOC0B-B | SSL0-C | | | |
| 20 | | PD5 | | GTIOC1A-B | RXD1 | | | |
| 21 | | PD4 | | GTIOC1B-B | SCK1 | | | |
| 22 | | PD3 | | GTIOC2A-B | TXD1 | | | |
| 23 | | PD2 | | GTIOC2B-B | MOSI-C | | | |
| 24 | | PD1 | | GTIOC3A | MISO-C | | | |
| 25 | | PD0 | | GTIOC3B | RSPCK-C | | | |
| 26 | | | | | | | | TDI |
| 27 | | | | | | | | TCK |
| 28 | | | | | | | | TDO |
| 29 | | PB7 | | | SCK2-A | | | |
| 30 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 31 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 32 | PLLVCC | | | | | | | |
| 33 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 34 | PLLVSS | | | | | | | |
| 35 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 36 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 37 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 38 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 39 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 40 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |
| 41 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 42 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 43 | | PA1 | | MTIOC6A | SSL2-B | | | |

**Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (2 / 3)**

| Pin No. (112-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 44 | | PA0 | | MTIOC6C | SSL3-B | | | |
| 45 | VCC | | | | | | | |
| 46 | | P96 | | | | IRQ4 | POE4# | |
| 47 | VSS | | | | | | | |
| 48 | | P95 | | MTIOC6B | | | | |
| 49 | | P94 | | MTIOC7A | | | | |
| 50 | | P93 | | MTIOC7B | | | | |
| 51 | | P92 | | MTIOC6D | | | | |
| 52 | | P91 | | MTIOC7C | | | | |
| 53 | | P90 | | MTIOC7D | | | | |
| 54 | | PG5 | | | | | | TRCLK |
| 55 | | PG4 | | | | | | TRDATA3 |
| 56 | | PG3 | | | | | | TRDATA2 |
| 57 | | PG2 | | | | IRQ2-B | | TRDATA1 |
| 58 | | PG1 | | | | IRQ1-C | | TRDATA0 |
| 59 | | PG0 | | | | IRQ0-C | | TRSYNC |
| 60 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 61 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 62 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 63 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 64 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 65 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 66 | | P70 | | | | IRQ5 | POE0# | |
| 67 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 68 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 69 | VCC | | | | | | | |
| 70 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 71 | VSS | | | | | | | |
| 72 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 73 | | P24 | | | RSPCK-A | | | |
| 74 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 75 | | P22 | ADTRG# | | CRX-B/ LRX/ MISO-A | | | |
| 76 | | P21 | ADTRG1#-B | MTCLKA-B | | IRQ6 | | |
| 77 | | P20 | ADTRG0#-B | MTCLKB-B | | IRQ7 | | |
| 78 | | P65 | AN5 | | | | | |
| 79 | | P64 | AN4 | | | | | |

**Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (3 / 3)**

| Pin No. (112-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 80 | AVCC | | | | | | | |
| 81 | VREF | | | | | | | |
| 82 | AVSS | | | | | | | |
| 83 | | P63 | AN3 | | | | | |
| 84 | | P62 | AN2 | | | | | |
| 85 | | P61 | AN1 | | | | | |
| 86 | | P60 | AN0 | | | | | |
| 87 | | P55 | AN11 | | | | | |
| 88 | | P54 | AN10 | | | | | |
| 89 | | P53 | AN9 | | | | | |
| 90 | | P52 | AN8 | | | | | |
| 91 | | P51 | AN7 | | | | | |
| 92 | | P50 | AN6 | | | | | |
| 93 | | P47 | AN103/ CVREFH | | | | | |
| 94 | | P46 | AN102 | | | | | |
| 95 | | P45 | AN101 | | | | | |
| 96 | | P44 | AN100 | | | | | |
| 97 | | P43 | AN003/ CVREFL | | | | | |
| 98 | | P42 | AN002 | | | | | |
| 99 | | P41 | AN001 | | | | | |
| 100 | | P40 | AN000 | | | | | |
| 101 | AVCC0 | | | | | | | |
| 102 | VREFH0 | | | | | | | |
| 103 | VREFL0 | | | | | | | |
| 104 | AVSS0 | | | | | | | |
| 105 | | P82 | | MTIC5U | SCK2-B | | | |
| 106 | | P81 | | MTIC5V | TXD2-B | | | |
| 107 | | P80 | | MTIC5W | RXD2-B | | | |
| 108 | | | | WDTOVF# | | | | |
| 109 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 110 | | P10 | | MTCLKD-B | | IRQ0-A | | |
| 111 | | | | | | | | TRST# |
| 112 | | | | | | | | TMS |

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| | | | | | | | | |
| 1 | | PE5 | | | | IRQ0-B | | |
| 2 | EMLE | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | MDE | | | | | | | |
| 5 | VCL | | | | | | | |
| 6 | MD1 | | | | | | | |
| 7 | MD0 | | | | | | | |
| 8 | | PE4 | | MTCLKC-C | | IRQ1-B | POE10#-B | |
| 9 | | PE3 | | MTCLKD-C | | IRQ2-A | POE11# | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | | PE2 | | | | NMI | POE10#-A | |
| 16 | | PE1 | | | SSL3-C | | | |
| 17 | | PE0 | | | CRX-C/ SSL2-C | | | |
| 18 | | PD7 | | GTIOC0A-B | CTX-C/ SSL1-C | | | TRST# |
| 19 | | PD6 | | GTIOC0B-B | SSL0-C | | | TMS |
| 20 | | PD5 | | GTIOC1A-B | RXD1 | | | TDI |
| 21 | | PD4 | | GTIOC1B-B | SCK1 | | | TCK |
| 22 | | PD3 | | GTIOC2A-B | TXD1 | | | TDO |
| 23 | | PD2 | | GTIOC2B-B | MOSI-C | | | TRCLK |
| 24 | | PD1 | | GTIOC3A | MISO-C | | | TRDATA3 |
| 25 | | PD0 | | GTIOC3B | RSPCK-C | | | TRDATA2 |
| 26 | | PB7 | | | SCK2-A | | | TRDATA1 |
| 27 | | PB6 | | | CRX-A/ RXD2-A | | | TRDATA0 |
| 28 | | PB5 | | | CTX-A/ TXD2-A | | | TRSYNC |
| 29 | PLLVCC | | | | | | | |
| 30 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 31 | PLLVSS | | | | | | | |
| 32 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 33 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 34 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 35 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 36 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 37 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |
| 38 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 39 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 40 | | PA1 | | MTIOC6A | SSL2-B | | | |

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 41 | | PA0 | | MTIOC6C | SSL3-B | | | |
| 42 | VCC | | | | | | | |
| 43 | | P96 | | | | IRQ4 | POE4# | |
| 44 | VSS | | | | | | | |
| 45 | | P95 | | MTIOC6B | | | | |
| 46 | | P94 | | MTIOC7A | | | | |
| 47 | | P93 | | MTIOC7B | | | | |
| 48 | | P92 | | MTIOC6D | | | | |
| 49 | | P91 | | MTIOC7C | | | | |
| 50 | | P90 | | MTIOC7D | | | | |
| 51 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 52 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 53 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 54 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 55 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 56 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 57 | | P70 | | | | IRQ5 | POE0# | |
| 58 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 59 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 60 | VCC | | | | | | | |
| 61 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 62 | VSS | | | | | | | |
| 63 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 64 | | P24 | | | RSPCK-A | | | |
| 65 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 66 | | P22 | ADTRG# | | CRX-B/ LRX/ MISO-A | | | |
| 67 | | P21 | ADTRG1#-B | MTCLKA-B | | IRQ6 | | |
| 68 | | P20 | ADTRG0#-B | MTCLKB-B | | IRQ7 | | |
| 69 | | P65 | AN5 | | | | | |
| 70 | | P64 | AN4 | | | | | |
| 71 | AVCC | | | | | | | |
| 72 | VREF | | | | | | | |
| 73 | AVSS | | | | | | | |
| 74 | | P63 | AN3 | | | | | |
| 75 | | P62 | AN2 | | | | | |
| 76 | | P61 | AN1 | | | | | |

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 77 | | P60 | AN0 | | | | | |
| 78 | | P55 | AN11 | | | | | |
| 79 | | P54 | AN10 | | | | | |
| 80 | | P53 | AN9 | | | | | |
| 81 | | P52 | AN8 | | | | | |
| 82 | | P51 | AN7 | | | | | |
| 83 | | P50 | AN6 | | | | | |
| 84 | | P47 | AN103/ CVREFH | | | | | |
| 85 | | P46 | AN102 | | | | | |
| 86 | | P45 | AN101 | | | | | |
| 87 | | P44 | AN100 | | | | | |
| 88 | | P43 | AN003/ CVREFL | | | | | |
| 89 | | P42 | AN002 | | | | | |
| 90 | | P41 | AN001 | | | | | |
| 91 | | P40 | AN000 | | | | | |
| 92 | AVCC0 | | | | | | | |
| 93 | VREFH0 | | | | | | | |
| 94 | VREFL0 | | | | | | | |
| 95 | AVSS0 | | | | | | | |
| 96 | | P82 | | MTIC5U | SCK2-B | | | |
| 97 | | P81 | | MTIC5V | TXD2-B | | | |
| 98 | | P80 | | MTIC5W | RXD2-B | | | |
| 99 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 100 | | P10 | | MTCLKD-B | | IRQ0-A | | |

**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | EMLE | | | | | | | |
| 2 | VSS | | | | | | | |
| 3 | MDE | | | | | | | |
| 4 | VCL | | | | | | | |
| 5 | MD1 | | | | | | | |
| 6 | MD0 | | | | | | | |
| 7 | | PE4 | | MTCLKC-C | | IRQ1-B | POE10#-B | |
| 8 | | PE3 | | MTCLKD-C | | IRQ2-A | POE11# | |
| 9 | RES# | | | | | | | |
| 10 | XTAL | | | | | | | |
| 11 | VSS | | | | | | | |
| 12 | EXTAL | | | | | | | |
| 13 | VCC | | | | | | | |
| 14 | | PE2 | | | | NMI | POE10#-A | |
| 15 | | PE0 | | | CRX-C | | | |
| 16 | | PD7 | | GTIOC0A-B | CTX-C | | | TRST# |
| 17 | | PD6 | | GTIOC0B-B | | | | TMS |
| 18 | | PD5 | | GTIOC1A-B | RXD1 | | | TDI |
| 19 | | PD4 | | GTIOC1B-B | SCK1 | | | TCK |
| 20 | | PD3 | | GTIOC2A-B | TXD1 | | | TDO |
| 21 | | PB7 | | | SCK2-A | | | |
| 22 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 23 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 24 | PLLVCC | | | | | | | |
| 25 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 26 | PLLVSS | | | | | | | |
| 27 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 28 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 29 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 30 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 31 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 32 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 33 | VCC | | | | | | | |
| 34 | | P96 | | | | IRQ4 | POE4# | |
| 35 | VSS | | | | | | | |
| 36 | | P95 | | MTIOC6B | | | | |
| 37 | | P94 | | MTIOC7A | | | | |
| 38 | | P93 | | MTIOC7B | | | | |
| 39 | | P92 | | MTIOC6D | | | | |
| 40 | | P91 | | MTIOC7C | | | | |
| 41 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |

**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 42 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 43 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 44 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 45 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 46 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 47 | | P70 | | | | IRQ5 | POE0# | |
| 48 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 49 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 50 | VCC | | | | | | | |
| 51 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 52 | VSS | | | | | | | |
| 53 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 54 | | P24 | | | RSPCK-A | | | |
| 55 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 56 | | P22 | ADTRG# | | CRX-B/ LRX/ MISO-A | | | |
| 57 | | P21 | ADTRG1#-B | MTCLKA-B | | IRQ6 | | |
| 58 | | P20 | ADTRG0#-B | MTCLKB-B | | IRQ7 | | |
| 59 | AVCC | | | | | | | |
| 60 | AVSS | | | | | | | |
| 61 | | P63 | AN3 | | | | | |
| 62 | | P62 | AN2 | | | | | |
| 63 | | P61 | AN1 | | | | | |
| 64 | | P60 | AN0 | | | | | |
| 65 | | P47 | AN103/ CVREFH | | | | | |
| 66 | | P46 | AN102 | | | | | |
| 67 | | P45 | AN101 | | | | | |
| 68 | | P44 | AN100 | | | | | |
| 69 | | P43 | AN003/ CVREFL | | | | | |
| 70 | | P42 | AN002 | | | | | |
| 71 | | P41 | AN001 | | | | | |
| 72 | | P40 | AN000 | | | | | |
| 73 | AVCC0 | | | | | | | |
| 74 | VREFH0 | | | | | | | |
| 75 | VREFL0 | | | | | | | |

**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (3 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 76 | AVSS0 | | | | | | | |
| 77 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 78 | | P10 | | MTCLKD-B | | IRQ0-A | | |
| 79 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 80 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |

**Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (1 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communication | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | EMLE | | | | | | | |
| 2 | VSS | | | | | | | |
| 3 | MDE | | | | | | | |
| 4 | VCL | | | | | | | |
| 5 | MD1 | | | | | | | |
| 6 | MD0 | | | | | | | |
| 7 | | PE4 | | MTCLKC-C | | IRQ1-B | POE10#-B | |
| 8 | | PE3 | | MTCLKD-C | | IRQ2-A | POE11# | |
| 9 | RES# | | | | | | | |
| 10 | XTAL | | | | | | | |
| 11 | VSS | | | | | | | |
| 12 | EXTAL | | | | | | | |
| 13 | VCC | | | | | | | |
| 14 | | PE2 | | | | NMI | POE10#-A | |
| 15 | | PD7 | | GTIOC0A-B | | | | TRST# |
| 16 | | PD6 | | GTIOC0B-B | | | | TMS |
| 17 | | PD5 | | GTIOC1A-B | RXD1 | | | TDI |
| 18 | | PD4 | | GTIOC1B-B | SCK1 | | | TCK |
| 19 | | PD3 | | GTIOC2A-B | TXD1 | | | TDO |
| 20 | | PD2 | | GTIOC2B-B | | | | |
| 21 | | PB7 | | | SCK2-A | | | |
| 22 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 23 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 24 | PLLVCC | | | | | | | |
| 25 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 26 | PLLVSS | | | | | | | |
| 27 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 28 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 29 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 30 | | PB0 | | MTIOC0D | | | | |
| 31 | | PA5 | ADTRG1#-A | MTIOC1A | | | | |
| 32 | | PA3 | | MTIOC2A | | | | |
| 33 | VCC | | | | | | | |
| 34 | | P96 | | | | IRQ4 | POE4# | |
| 35 | VSS | | | | | | | |
| 36 | | P95 | | MTIOC6B | | | | |
| 37 | | P94 | | MTIOC7A | | | | |
| 38 | | P93 | | MTIOC7B | | | | |
| 39 | | P92 | | MTIOC6D | | | | |
| 40 | | P91 | | MTIOC7C | | | | |
| 41 | | P90 | | MTIOC7D | | | | |

**Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (2 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communication | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 42 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 43 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 44 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 45 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 46 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 47 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 48 | | P70 | | | | IRQ5 | POE0# | |
| 49 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 50 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 51 | VCC | | | | | | | |
| 52 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 53 | VSS | | | | | | | |
| 54 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 55 | | P24 | | | RSPCK-A | | | |
| 56 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 57 | | P22 | ADTRG# | | CRX-B/ LRX/ MISO-A | | | |
| 58 | | P20 | ADTRG0#-B | MTCLKB-B | | IRQ7 | | |
| 59 | AVCC | | | | | | | |
| 60 | AVSS | | | | | | | |
| 61 | | P63 | AN3 | | | | | |
| 62 | | P62 | AN2 | | | | | |
| 63 | | P61 | AN1 | | | | | |
| 64 | | P60 | AN0 | | | | | |
| 65 | | P47 | AN103/ CVREFH | | | | | |
| 66 | | P46 | AN102 | | | | | |
| 67 | | P45 | AN101 | | | | | |
| 68 | | P44 | AN100 | | | | | |
| 69 | | P43 | AN003/ CVREFL | | | | | |
| 70 | | P42 | AN002 | | | | | |
| 71 | | P41 | AN001 | | | | | |
| 72 | | P40 | AN000 | | | | | |
| 73 | AVCC0 | | | | | | | |
| 74 | VREFH0 | | | | | | | |
| 75 | VREFL0 | | | | | | | |

**Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communication | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 76 | AVSS0 | | | | | | | |
| 77 | | P82 | | MTIC5U | SCK2-B | | | |
| 78 | | P81 | | MTIC5V | TXD2-B | | | |
| 79 | | P80 | | MTIC5W | RXD2-B | | | |
| 80 | | P10 | | MTCLKD-B | | IRQ0-A | | |

**Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)**

| Pin No. (64-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | EMLE | | | | | | | |
| 2 | MDE | | | | | | | |
| 3 | VCL | | | | | | | |
| 4 | MD1 | | | | | | | |
| 5 | MD0 | | | | | | | |
| 6 | RES# | | | | | | | |
| 7 | XTAL | | | | | | | |
| 8 | VSS | | | | | | | |
| 9 | EXTAL | | | | | | | |
| 10 | VCC | | | | | | | |
| 11 | | PE2 | | | | NMI | POE10#-A | |
| 12 | | PD7 | | GTIOC0A-B | | | | TRST# |
| 13 | | PD6 | | GTIOC0B-B | | | | TMS |
| 14 | | PD5 | | GTIOC1A-B | RXD1 | | | TDI |
| 15 | | PD4 | | GTIOC1B-B | SCK1 | | | TCK |
| 16 | | PD3 | | GTIOC2A-B | TXD1 | | | TDO |
| 17 | | PB7 | | | SCK2-A | | | |
| 18 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 19 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 20 | PLLVCC | | | | | | | |
| 21 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 22 | PLLVSS | | | | | | | |
| 23 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 24 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 25 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 26 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 27 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 28 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 29 | | P94 | | MTIOC7A | | | | |
| 30 | | P93 | | MTIOC7B | | | | |
| 31 | | P92 | | MTIOC6D | | | | |
| 32 | | P91 | | MTIOC7C | | | | |
| 33 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 34 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 35 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 36 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 37 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 38 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 39 | | P70 | | | | IRQ5 | POE0# | |

**Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)**

| Pin No. (64-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debuggi ng |
|---|---|---|---|---|---|---|---|---|
| 40 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 41 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 42 | VCC | | | | | | | |
| 43 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 44 | VSS | | | | | | | |
| 45 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 46 | | P24 | | | RSPCK-A | | | |
| 47 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 48 | | P22 | | | CRX-B/ LRX/ MISO-A | | | |
| 49 | | P47 | AN103/ CVREFH | | | | | |
| 50 | | P46 | AN102 | | | | | |
| 51 | | P45 | AN101 | | | | | |
| 52 | | P44 | AN100 | | | | | |
| 53 | | P43 | AN003/ CVREFL | | | | | |
| 54 | | P42 | AN002 | | | | | |
| 55 | | P41 | AN001 | | | | | |
| 56 | | P40 | AN000 | | | | | |
| 57 | AVCC0 | | | | | | | |
| 58 | VREFH0 | | | | | | | |
| 59 | VREFL0 | | | | | | | |
| 60 | AVSS0 | | | | | | | |
| 61 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 62 | | P10 | | MTCLKD-B | | IRQ0-A | | |
| 63 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 64 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |

## 1.5 Pin Functions

Table 1.9 lists the pin functions.

**Table 1.9 Pin Functions (1 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. |
| | VCL | Input | Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | PLLVCC | Input | Power supply pin for the PLL circuit. Connect it to the system power supply. |
| | PLLVSS | Input | Ground pin for the PLL circuit. |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| Operating mode control | MD0<br>MD1<br>MDE | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| On-chip emulator | TRST# | Input | On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. Not included in the 80-/64-pin versions. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. Not included in the 80-/64-pin versions. |
| | TRDATA0 to TRDATA3 | Output | These pins output the trace information. Not included in the 80-/64-pin versions. |
| Interrupt (ICU) | NMI | Input | Non-maskable interrupt request signal. |
| | IRQ0-A/IRQ0-B/IRQ0-C<br>IRQ1-A/IRQ1-B/IRQ1-C<br>IRQ2-A/IRQ2-B<br>IRQ3 to IRQ7 | Input | Interrupt request signals. The IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 100-pin version. The IRQ0-B/IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 80-pin version. The IRQ0-B/IRQ0-C/IRQ1-B/IRQ1-/IRQ2-A/IRQ2-B/IRQ4/IRQ6/IRQ7 pin is not included in the 64-pin version. |

**Table 1.9 Pin Functions (2 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Multi-function timer pulse unit 3 (MTU3) | MTIOC0A-A/MTIOC0A-B<br>MTIOC0B-A/MTIOC0B-B<br>MTIOC0C, MTIOC0D | I/O | The MTU0.TGRA to MTU0.TGRD input capture input/output compare output/PWM output pins. |
| | MTIOC1A, MTIOC1B | I/O | The MTU1.TGRA and MTU1.TGRB input capture input/output compare output/PWM output pins. |
| | MTIOC2A, MTIOC2B | I/O | The MTU2.TGRA and MTU2.TGRB input capture input/output compare output/PWM output pins. |
| | MTIOC3A, MTIOC3B<br>MTIOC3C, MTIOC3D | I/O | The MTU3.TGRA and MTU3.TGRD input capture input/output compare output/PWM output pins.<br>Pins MTIOC3B and MTIOC3D can be used for large-current output. |
| | MTIOC4A, MTIOC4B<br>MTIOC4C, MTIOC4D | I/O | The MTU4.TGRA and MTU4.TGRD input capture input/output compare output/PWM output pins.<br>These pins can be used for large-current output. |
| | MTIC5U, MTIC5V, MTIC5W | Input | The MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW input capture input/dead time compensation input pins. Not included in the 80-/64-pin versions. |
| | MTIOC6A, MTIOC6B<br>MTIOC6C, MTIOC6D | I/O | The MTU6.TGRA to MTU6.TGRD input capture input/output compare output/PWM output pins.<br>Pins MTIOC6B and MTIOC6D can be used for large-current output. The MTIOC6A/MTIOC6C pin is not included in the 80-pin version. The MTIOC6A/MTIOC6B/MTIOC6C pin is not included in the 64-pin version. |
| | MTIOC7A, MTIOC7B<br>MTIOC7C, MTIOC7D | I/O | The MTU7.TGRA to MTU7.TGRD input capture input/output compare output/PWM output pins.<br>These pins can be used for large-current output. The MTIOC7D pin is not included in the 80-/64-pin versions. |
| | MTCLKA-A/MTCLKA-B<br>MTCLKB-A/MTCLKB-B<br>MTCLKC-A/MTCLKC-B/<br>MTCLKC-C<br>MTCLKD-A/MTCLKD-B/<br>MTCLKD-C | Input | Input pins for external clock signals. The MTCLKA-B/MTCLKB-B/MTCLKC-C/MTCLKD-C pin is not included in the 64-pin version. |
| General PWM timer (GPT) | GTIOC0A-A/GTIOC0A-B<br>GTIOC0B-A/GTIOC0B-B | I/O | The GPT0.GTCCRA and GPT0.GTCCRB CCRB input capture input/output compare output/PWM output pins.<br>Pins GTIOC0A-A and GTIOC0B-A can be used for large-current output. |
| | GTIOC1A-A/GTIOC1A-B<br>GTIOC1B-A/GTIOC1B-B | I/O | The GPT1.GTCCRA and GPT1.GTCCRB input capture input/output compare output/PWM output pins.<br>Pins GTIOC1A-A and GTIOC1B-A can be used for large-current output. |
| | GTIOC2A-A/GTIOC2A-B<br>GTIOC2B-A/GTIOC2B-B | I/O | The GPT2.GTCCRA and GPT2.GTCCRB input capture input/output compare output/PWM output pins.<br>Pins GTIOC2A-A and GTIOC2B-A can be used for large-current output. The GTIOC2B-B pin is not included in the 80-pin version. |
| | GTIOC3A, GTIOC3B | I/O | The GPT3.GTCCRA and GPT3.GTCCRB input capture input/output compare output/PWM output pins. Not included in the 80-/64-pin versions. |
| | GTETRG | Input | External trigger input pin for the GPT |
| Port output enable 3 (POE3) | POE0#, POE4#, POE8#<br>POE10#-A/POE10#-B<br>POE11# | Input | Input pins for request signals to place the MTU3 and GPT large-current pins in the high impedance state. The POE4#/POE10#-B/POE11# pin is not included in the 64-pin version. |
| Watchdog timer (WDT) | WDTOVF# | Output | Output pin for the counter-overflow signal in watchdog-timer mode. Not included in the 100-/80-/64-pin versions. |

**Table 1.9 Pin Functions (3 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCIb) | TXD0, TXD1, TXD2-A/TXD2-B | Output | Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions. |
| | RXD0, RXD1, RXD2-A/ RXD2-B | Input | Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions. |
| | SCK0, SCK1, SCK2-A/ SCK2-B | I/O | Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions. |
| $I^2C$ bus interface (RIIC) | SCL | I/O | Input/output pin for $I^2C$ bus interface clocks. Bus can be directly driven by the NMOS open drain output. |
| | SDA | I/O | Input/output pin for $I^2C$ bus interface data. Bus can be directly driven by the NMOS open drain output. |
| CAN module (CAN) (as an optional function) | CRX-A/CRX-B/CRX-C | Input | Input pin for the CAN. The CRX-C pin is not included in the 64-pin version. |
| | CTX-A/CTX-B/CTX-C | Output | Output pin for the CAN. The CTX-C pin is not included in the 64-pin version. |
| LIN module (LIN) | LRX | Input | Input pin for the LIN. |
| | LTX | Output | Output pin for the LIN. |
| Serial peripheral interface (RSPI) | RSPCK-A/RSPCK-B/ RSPCK-C | I/O | Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions. |
| | MOSI-A/MOSI-B/MOSI-C | I/O | Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions. |
| | MISO-A/MISO-B/MISO-C | I/O | Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions. |
| | SSL0-A/SSL0-B/SSL0-C | I/O | Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/ SSL3-C pin is not included in the 80-/64-pin versions. |
| | SSL1-A/SSL1-B/SSL1-C<br>SSL2-A/SSL2-B/SSL2-C<br>SSL3-A/SSL3-B/SSL3-C | Output | |
| A/D converter | AN000 to AN003<br>AN100 to AN103 | Input | Input pins for the analog signals to be processed by the 12-bit A/D converter. |
| | AN0 to AN11 | Input | Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version. |
| | ADTRG0#-A/ADTRG0#-B<br>ADTRG1#-A/ADTRG1#-B<br>ADTRG# | Input | Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version. |
| | CVREFH | Input | Input pin for the high-level reference voltage to the comparator |
| | CVREFL | Input | Input pin for the low-level reference voltage to the comparator |
| Analog power supply | AVCC0 | Input | Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. |
| | AVSS0 | Input | Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V). |
| | VREFH0 | Input | Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply. |
| | VREFL0 | Input | Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V). |
| | AVCC | Input | Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version. |
| | AVSS | Input | Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version. |
| | VREF | Input | Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions. |

**Table 1.9 Pin Functions (4 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| I/O ports | P10, P11 | I/O | 2-bit input/output pins. |
| | P20 to P24 | I/O | 5-bit input/output pins. The P20/P21 pin is not included in the 64-pin version. |
| | P30 to P33 | I/O | 4-bit input/output pins. |
| | P40 to P47 | Input | 8-bit input pins. |
| | P50 to P55 | Input | 6-bit input pins. Not included in the 80-/64-pin versions. |
| | P60 to P65 | Input | 6-bit input pins. The P64/P6 pin is not included in the 80-pin version. Not included in the 64-pin version. |
| | P70 to P76 | I/O | 7-bit input/output pins. |
| | P80 to P82 | I/O | 3-bit input/output pins. Not included in the 80-/64-pin versions. |
| | P90 to P96 | I/O | 7-bit input/output pins. The P90 pin is not included in the 80-pin version. The P90/P95/P96 pin is not included in the 64-pin version. |
| | PA0 to PA5 | I/O | 6-bit input/output pins. The PA0/PA1 pin is not included in the 80-/64-pin versions. |
| | PB0 to PB7 | I/O | 8-bit input/output pins. |
| | PD0 to PD7 | I/O | 8-bit input/output pins. The PD0/PD1/PD2 pin is not included in the 80-/64-pin versions. |
| | PE0, PE1, PE3 to PE5 | I/O | 5-bit input/output pins. The PE1/PE5 pin is not included in the 80-pin version. Not included in the 64-pin version. |
| | PE2 | Input | 1-bit input pin. |
| | PG0 to PG5 | I/O | 6-bit input/output pins. Not included in the 100-/80-/64-pin versions. |

Note: • Which pins are and are not incorporated depends on the package.
For details, see the list of pins and pin functions in Table 1.4 to Table 1.8.

# 2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

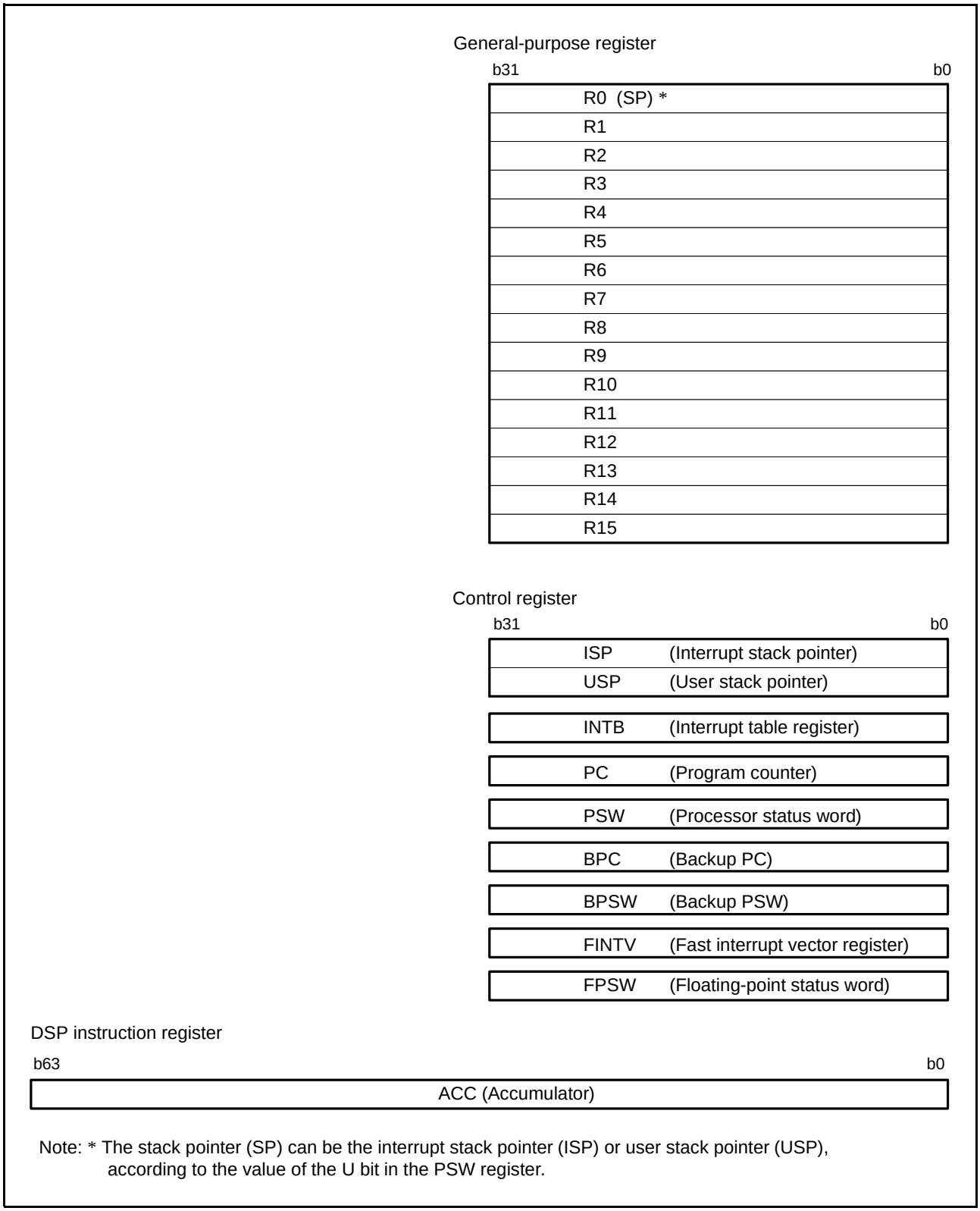



**Figure 2.1 Register Set of the CPU**

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.
Set INTB to a multiple of four.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

### (8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

### (9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

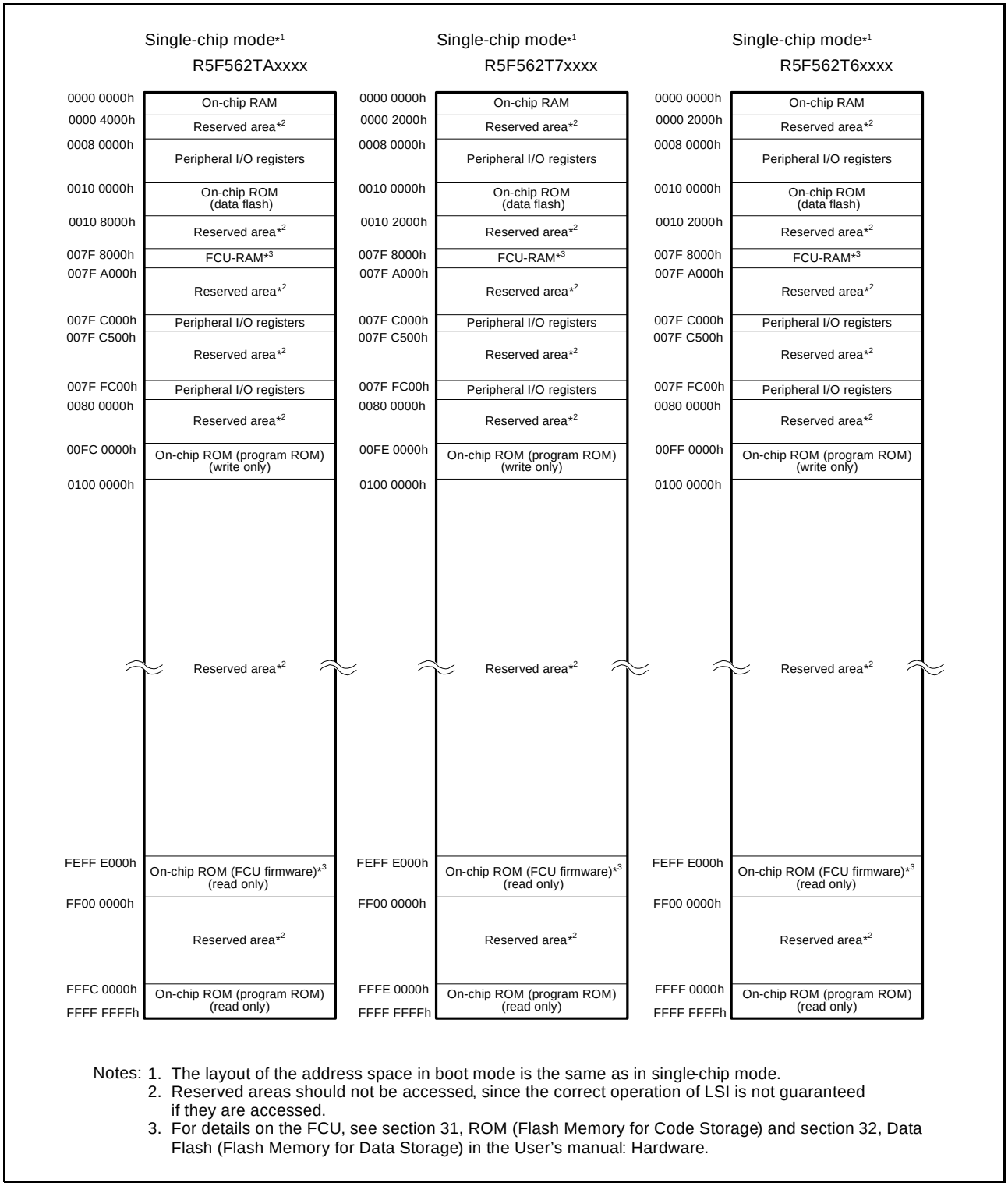
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

# 3. Address Space

## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas. Figure 3.1 shows the memory maps.




Notes: 1. The layout of the address space in boot mode is the same as in single-chip mode.
2. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
3. For details on the FCU, see section 31, ROM (Flash Memory for Code Storage) and section 32, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

**Figure 3.1 Memory Map (RX62T Group)**

# 4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

## (1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

## (2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "—" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

## (3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.

(b) Read the value from the I/O register to a general register.

(c) Execute the operation using the value read.

(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

### (4) Number of Access Cycles to I/O Registers

The number of access cycles to I/O registers is obtained by following equation.*

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided cycles for clock synchronization +
Number of bus cycles for internal peripheral buses 1, 2, 4, and 6

The number of bus cycles for internal peripheral buses 1, 2, 4, and 6 differs according to the register to be accessed. For the number of access cycles to each I/O register, see Table 4.1, List of I/O Registers.

When peripheral functions connected to internal peripheral bus 6 are accessed, the number of divided cycles for clock synchronization is added.

Although the number of divided cycles for clock synchronization differs depending on the number of frequency ratio between ICLK and PCLK or bus access timing, the sum of the number of bus cycles for internal main bus 1 and the number of divided cycles for clock synchronization will be one PCLK at a maximum. Therefore, one PCLK is added to the number of access cycles shown in Table 4.1.

Note: • This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DTC).

## 4.1 I/O Register Addresses (Address Order)

**Table 4.1 List of I/O Registers (Address Order) (1 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 0000h | SYSTEM | Mode monitor register | MDMONR | 16 | 16 | 3 ICLK |
| 0008 0002h | SYSTEM | Mode status register | MDSR | 16 | 16 | 3 ICLK |
| 0008 0006h | SYSTEM | System control register 0 | SYSCR0 | 16 | 16 | 3 ICLK |
| 0008 0008h | SYSTEM | System control register 1 | SYSCR1 | 16 | 16 | 3 ICLK |
| 0008 000Ch | SYSTEM | Standby control register | SBYCR | 16 | 16 | 3 ICLK |
| 0008 0010h | SYSTEM | Module stop control register A | MSTPCRA | 32 | 32 | 3 ICLK |
| 0008 0014h | SYSTEM | Module stop control register B | MSTPCRB | 32 | 32 | 3 ICLK |
| 0008 0018h | SYSTEM | Module stop control register C | MSTPCRC | 32 | 32 | 3 ICLK |
| 0008 0020h | SYSTEM | System clock control register | SCKCR | 32 | 32 | 3 ICLK |
| 0008 0040h | SYSTEM | Oscillation stop detection control register | OSTDCR | 16 | 16 | 3 ICLK |
| 0008 1300h | BSC | Bus error status clear register | BERCLR | 8 | 8 | 2 ICLK |
| 0008 1304h | BSC | Bus error monitoring enable register | BEREN | 8 | 8 | 2 ICLK |
| 0008 1308h | BSC | Bus error status register 1 | BERSR1 | 8 | 8 | 2 ICLK |
| 0008 130Ah | BSC | Bus error status register 2 | BERSR2 | 16 | 16 | 2 ICLK |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | 2 ICLK |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | 2 ICLK |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | 2 ICLK |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | 2 ICLK |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | 2 ICLK |
| 0008 6400h | MPU | Region 0 start page-number register | RSPAGE0 | 32 | 32 | 1 ICLK |
| 0008 6404h | MPU | Region 0 end page-number register | REPAGE0 | 32 | 32 | 1 ICLK |
| 0008 6408h | MPU | Region 1 start page-number register | RSPAGE1 | 32 | 32 | 1 ICLK |
| 0008 640Ch | MPU | Region 1 end page-number register | REPAGE1 | 32 | 32 | 1 ICLK |
| 0008 6410h | MPU | Region 2 start page-number register | RSPAGE2 | 32 | 32 | 1 ICLK |
| 0008 6414h | MPU | Region 2 end page-number register | REPAGE2 | 32 | 32 | 1 ICLK |
| 0008 6418h | MPU | Region 3 start page-number register | RSPAGE3 | 32 | 32 | 1 ICLK |
| 0008 641Ch | MPU | Region 3 end page-number register | REPAGE3 | 32 | 32 | 1 ICLK |
| 0008 6420h | MPU | Region 4 start page-number register | RSPAGE4 | 32 | 32 | 1 ICLK |
| 0008 6424h | MPU | Region 4 end page-number register | REPAGE4 | 32 | 32 | 1 ICLK |
| 0008 6428h | MPU | Region 5 start page-number register | RSPAGE5 | 32 | 32 | 1 ICLK |
| 0008 642Ch | MPU | Region 5 end page-number register | REPAGE5 | 32 | 32 | 1 ICLK |
| 0008 6430h | MPU | Region 6 start page-number register | RSPAGE6 | 32 | 32 | 1 ICLK |
| 0008 6434h | MPU | Region 6 end page-number register | REPAGE6 | 32 | 32 | 1 ICLK |
| 0008 6438h | MPU | Region 7 start page-number register | RSPAGE7 | 32 | 32 | 1 ICLK |
| 0008 643Ch | MPU | Region 7 end page-number register | REPAGE7 | 32 | 32 | 1 ICLK |
| 0008 6500h | MPU | Memory-protection enable register | MPEN | 32 | 32 | 1 ICLK |
| 0008 6504h | MPU | Background access control register | MPBAC | 32 | 32 | 1 ICLK |
| 0008 6508h | MPU | Memory-protection error status-clearing register | MPECLR | 32 | 32 | 1 ICLK |
| 0008 650Ch | MPU | Memory-protection error status register | MPESTS | 32 | 32 | 1 ICLK |
| 0008 6514h | MPU | Data memory-protection error address register | MPDEA | 32 | 32 | 1 ICLK |
| 0008 6520h | MPU | Region search address register | MPSA | 32 | 32 | 1 ICLK |
| 0008 6524h | MPU | Region search operation register | MPOPS | 16 | 16 | 1 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (2 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 6526h | MPU | Region invalidation operation register | MPOPI | 16 | 16 | 1 ICLK |
| 0008 6528h | MPU | Instruction-hit region register | MHITI | 32 | 32 | 1 ICLK |
| 0008 652Ch | MPU | Data-hit region register | MHITD | 32 | 32 | 1 ICLK |
| 0008 7010h | ICU | Interrupt request register 016 | IR016 | 8 | 8 | 2 ICLK |
| 0008 7015h | ICU | Interrupt request register 021 | IR021 | 8 | 8 | 2 ICLK |
| 0008 7017h | ICU | Interrupt request register 023 | IR023 | 8 | 8 | 2 ICLK |
| 0008 701Bh | ICU | Interrupt request register 027 | IR027 | 8 | 8 | 2 ICLK |
| 0008 701Ch | ICU | Interrupt request register 028 | IR028 | 8 | 8 | 2 ICLK |
| 0008 701Dh | ICU | Interrupt request register 029 | IR029 | 8 | 8 | 2 ICLK |
| 0008 701Eh | ICU | Interrupt request register 030 | IR030 | 8 | 8 | 2 ICLK |
| 0008 701Fh | ICU | Interrupt request register 031 | IR031 | 8 | 8 | 2 ICLK |
| 0008 702Ch | ICU | Interrupt request register 044 | IR044 | 8 | 8 | 2 ICLK |
| 0008 702Dh | ICU | Interrupt request register 045 | IR045 | 8 | 8 | 2 ICLK |
| 0008 702Eh | ICU | Interrupt request register 046 | IR046 | 8 | 8 | 2 ICLK |
| 0008 702Fh | ICU | Interrupt request register 047 | IR047 | 8 | 8 | 2 ICLK |
| 0008 7038h | ICU | Interrupt request register 056 | IR056 | 8 | 8 | 2 ICLK |
| 0008 7039h | ICU | Interrupt request register 057 | IR057 | 8 | 8 | 2 ICLK |
| 0008 703Ah | ICU | Interrupt request register 058 | IR058 | 8 | 8 | 2 ICLK |
| 0008 703Bh | ICU | Interrupt request register 059 | IR059 | 8 | 8 | 2 ICLK |
| 0008 703Ch | ICU | Interrupt request register 060 | IR060 | 8 | 8 | 2 ICLK |
| 0008 7040h | ICU | Interrupt request register 064 | IR064 | 8 | 8 | 2 ICLK |
| 0008 7041h | ICU | Interrupt request register 065 | IR065 | 8 | 8 | 2 ICLK |
| 0008 7042h | ICU | Interrupt request register 066 | IR066 | 8 | 8 | 2 ICLK |
| 0008 7043h | ICU | Interrupt request register 067 | IR067 | 8 | 8 | 2 ICLK |
| 0008 7044h | ICU | Interrupt request register 068 | IR068 | 8 | 8 | 2 ICLK |
| 0008 7045h | ICU | Interrupt request register 069 | IR069 | 8 | 8 | 2 ICLK |
| 0008 7046h | ICU | Interrupt request register 070 | IR070 | 8 | 8 | 2 ICLK |
| 0008 7047h | ICU | Interrupt request register 071 | IR071 | 8 | 8 | 2 ICLK |
| 0008 7060h | ICU | Interrupt request register 096 | IR096 | 8 | 8 | 2 ICLK |
| 0008 7062h | ICU | Interrupt request register 098 | IR098 | 8 | 8 | 2 ICLK |
| 0008 7066h | ICU | Interrupt request register 102 | IR102 | 8 | 8 | 2 ICLK |
| 0008 7067h | ICU | Interrupt request register 103 | IR103 | 8 | 8 | 2 ICLK |
| 0008 706Ah | ICU | Interrupt request register 106 | IR106 | 8 | 8 | 2 ICLK |
| 0008 7072h | ICU | Interrupt request register 114 | IR114 | 8 | 8 | 2 ICLK |
| 0008 7073h | ICU | Interrupt request register 115 | IR115 | 8 | 8 | 2 ICLK |
| 0008 7074h | ICU | Interrupt request register 116 | IR116 | 8 | 8 | 2 ICLK |
| 0008 7075h | ICU | Interrupt request register 117 | IR117 | 8 | 8 | 2 ICLK |
| 0008 7076h | ICU | Interrupt request register 118 | IR118 | 8 | 8 | 2 ICLK |
| 0008 7077h | ICU | Interrupt request register 119 | IR119 | 8 | 8 | 2 ICLK |
| 0008 7078h | ICU | Interrupt request register 120 | IR120 | 8 | 8 | 2 ICLK |
| 0008 7079h | ICU | Interrupt request register 121 | IR121 | 8 | 8 | 2 ICLK |
| 0008 707Ah | ICU | Interrupt request register 122 | IR122 | 8 | 8 | 2 ICLK |
| 0008 707Bh | ICU | Interrupt request register 123 | IR123 | 8 | 8 | 2 ICLK |
| 0008 707Ch | ICU | Interrupt request register 124 | IR124 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (3 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 707Dh | ICU | Interrupt request register 125 | IR125 | 8 | 8 | 2 ICLK |
| 0008 707Eh | ICU | Interrupt request register 126 | IR126 | 8 | 8 | 2 ICLK |
| 0008 707Fh | ICU | Interrupt request register 127 | IR127 | 8 | 8 | 2 ICLK |
| 0008 7080h | ICU | Interrupt request register 128 | IR128 | 8 | 8 | 2 ICLK |
| 0008 7081h | ICU | Interrupt request register 129 | IR129 | 8 | 8 | 2 ICLK |
| 0008 7082h | ICU | Interrupt request register 130 | IR130 | 8 | 8 | 2 ICLK |
| 0008 7083h | ICU | Interrupt request register 131 | IR131 | 8 | 8 | 2 ICLK |
| 0008 7084h | ICU | Interrupt request register 132 | IR132 | 8 | 8 | 2 ICLK |
| 0008 7085h | ICU | Interrupt request register 133 | IR133 | 8 | 8 | 2 ICLK |
| 0008 7086h | ICU | Interrupt request register 134 | IR134 | 8 | 8 | 2 ICLK |
| 0008 7087h | ICU | Interrupt request register 135 | IR135 | 8 | 8 | 2 ICLK |
| 0008 7088h | ICU | Interrupt request register 136 | IR136 | 8 | 8 | 2 ICLK |
| 0008 7089h | ICU | Interrupt request register 137 | IR137 | 8 | 8 | 2 ICLK |
| 0008 708Ah | ICU | Interrupt request register 138 | IR138 | 8 | 8 | 2 ICLK |
| 0008 708Bh | ICU | Interrupt request register 139 | IR139 | 8 | 8 | 2 ICLK |
| 0008 708Ch | ICU | Interrupt request register 140 | IR140 | 8 | 8 | 2 ICLK |
| 0008 708Dh | ICU | Interrupt request register 141 | IR141 | 8 | 8 | 2 ICLK |
| 0008 708Eh | ICU | Interrupt request register 142 | IR142 | 8 | 8 | 2 ICLK |
| 0008 708Fh | ICU | Interrupt request register 143 | IR143 | 8 | 8 | 2 ICLK |
| 0008 7090h | ICU | Interrupt request register 144 | IR144 | 8 | 8 | 2 ICLK |
| 0008 7091h | ICU | Interrupt request register 145 | IR145 | 8 | 8 | 2 ICLK |
| 0008 7092h | ICU | Interrupt request register 146 | IR146 | 8 | 8 | 2 ICLK |
| 0008 7095h | ICU | Interrupt request register 149 | IR149 | 8 | 8 | 2 ICLK |
| 0008 7096h | ICU | Interrupt request register 150 | IR150 | 8 | 8 | 2 ICLK |
| 0008 7097h | ICU | Interrupt request register 151 | IR151 | 8 | 8 | 2 ICLK |
| 0008 7098h | ICU | Interrupt request register 152 | IR152 | 8 | 8 | 2 ICLK |
| 0008 7099h | ICU | Interrupt request register 153 | IR153 | 8 | 8 | 2 ICLK |
| 0008 70AAh | ICU | Interrupt request register 170 | IR170 | 8 | 8 | 2 ICLK |
| 0008 70ABh | ICU | Interrupt request register 171 | IR171 | 8 | 8 | 2 ICLK |
| 0008 70ACh | ICU | Interrupt request register 172 | IR172 | 8 | 8 | 2 ICLK |
| 0008 70ADh | ICU | Interrupt request register 173 | IR173 | 8 | 8 | 2 ICLK |
| 0008 70AEh | ICU | Interrupt request register 174 | IR174 | 8 | 8 | 2 ICLK |
| 0008 70AFh | ICU | Interrupt request register 175 | IR175 | 8 | 8 | 2 ICLK |
| 0008 70B0h | ICU | Interrupt request register 176 | IR176 | 8 | 8 | 2 ICLK |
| 0008 70B1h | ICU | Interrupt request register 177 | IR177 | 8 | 8 | 2 ICLK |
| 0008 70B2h | ICU | Interrupt request register 178 | IR178 | 8 | 8 | 2 ICLK |
| 0008 70B3h | ICU | Interrupt request register 179 | IR179 | 8 | 8 | 2 ICLK |
| 0008 70B4h | ICU | Interrupt request register 180 | IR180 | 8 | 8 | 2 ICLK |
| 0008 70B5h | ICU | Interrupt request register 181 | IR181 | 8 | 8 | 2 ICLK |
| 0008 70B6h | ICU | Interrupt request register 182 | IR182 | 8 | 8 | 2 ICLK |
| 0008 70B7h | ICU | Interrupt request register 183 | IR183 | 8 | 8 | 2 ICLK |
| 0008 70B8h | ICU | Interrupt request register 184 | IR184 | 8 | 8 | 2 ICLK |
| 0008 70BAh | ICU | Interrupt request register 186 | IR186 | 8 | 8 | 2 ICLK |
| 0008 70BBh | ICU | Interrupt request register 187 | IR187 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (4 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 70BCh | ICU | Interrupt request register 188 | IR188 | 8 | 8 | 2 ICLK |
| 0008 70BDh | ICU | Interrupt request register 189 | IR189 | 8 | 8 | 2 ICLK |
| 0008 70BEh | ICU | Interrupt request register 190 | IR190 | 8 | 8 | 2 ICLK |
| 0008 70C0h | ICU | Interrupt request register 192 | IR192 | 8 | 8 | 2 ICLK |
| 0008 70C1h | ICU | Interrupt request register 193 | IR193 | 8 | 8 | 2 ICLK |
| 0008 70C2h | ICU | Interrupt request register 194 | IR194 | 8 | 8 | 2 ICLK |
| 0008 70C3h | ICU | Interrupt request register 195 | IR195 | 8 | 8 | 2 ICLK |
| 0008 70C4h | ICU | Interrupt request register 196 | IR196 | 8 | 8 | 2 ICLK |
| 0008 70D6h | ICU | Interrupt request register 214 | IR214 | 8 | 8 | 2 ICLK |
| 0008 70D7h | ICU | Interrupt request register 215 | IR215 | 8 | 8 | 2 ICLK |
| 0008 70D8h | ICU | Interrupt request register 216 | IR216 | 8 | 8 | 2 ICLK |
| 0008 70D9h | ICU | Interrupt request register 217 | IR217 | 8 | 8 | 2 ICLK |
| 0008 70DAh | ICU | Interrupt request register 218 | IR218 | 8 | 8 | 2 ICLK |
| 0008 70DBh | ICU | Interrupt request register 219 | IR219 | 8 | 8 | 2 ICLK |
| 0008 70DCh | ICU | Interrupt request register 220 | IR220 | 8 | 8 | 2 ICLK |
| 0008 70DDh | ICU | Interrupt request register 221 | IR221 | 8 | 8 | 2 ICLK |
| 0008 70DEh | ICU | Interrupt request register 222 | IR222 | 8 | 8 | 2 ICLK |
| 0008 70DFh | ICU | Interrupt request register 223 | IR223 | 8 | 8 | 2 ICLK |
| 0008 70E0h | ICU | Interrupt request register 224 | IR224 | 8 | 8 | 2 ICLK |
| 0008 70E1h | ICU | Interrupt request register 225 | IR225 | 8 | 8 | 2 ICLK |
| 0008 70F6h | ICU | Interrupt request register 246 | IR246 | 8 | 8 | 2 ICLK |
| 0008 70F7h | ICU | Interrupt request register 247 | IR247 | 8 | 8 | 2 ICLK |
| 0008 70F8h | ICU | Interrupt request register 248 | IR248 | 8 | 8 | 2 ICLK |
| 0008 70F9h | ICU | Interrupt request register 249 | IR249 | 8 | 8 | 2 ICLK |
| 0008 70FEh | ICU | Interrupt request register 254 | IR254 | 8 | 8 | 2 ICLK |
| 0008 711Bh | ICU | DTC activation enable register 027 | DTCER027 | 8 | 8 | 2 ICLK |
| 0008 711Ch | ICU | DTC activation enable register 028 | DTCER028 | 8 | 8 | 2 ICLK |
| 0008 711Dh | ICU | DTC activation enable register 029 | DTCER029 | 8 | 8 | 2 ICLK |
| 0008 711Eh | ICU | DTC activation enable register 030 | DTCER030 | 8 | 8 | 2 ICLK |
| 0008 711Fh | ICU | DTC activation enable register 031 | DTCER031 | 8 | 8 | 2 ICLK |
| 0008 712Dh | ICU | DTC activation enable register 045 | DTCER045 | 8 | 8 | 2 ICLK |
| 0008 712Eh | ICU | DTC activation enable register 046 | DTCER046 | 8 | 8 | 2 ICLK |
| 0008 7140h | ICU | DTC activation enable register 064 | DTCER064 | 8 | 8 | 2 ICLK |
| 0008 7141h | ICU | DTC activation enable register 065 | DTCER065 | 8 | 8 | 2 ICLK |
| 0008 7142h | ICU | DTC activation enable register 066 | DTCER066 | 8 | 8 | 2 ICLK |
| 0008 7143h | ICU | DTC activation enable register 067 | DTCER067 | 8 | 8 | 2 ICLK |
| 0008 7144h | ICU | DTC activation enable register 068 | DTCER068 | 8 | 8 | 2 ICLK |
| 0008 7145h | ICU | DTC activation enable register 069 | DTCER069 | 8 | 8 | 2 ICLK |
| 0008 7146h | ICU | DTC activation enable register 070 | DTCER070 | 8 | 8 | 2 ICLK |
| 0008 7147h | ICU | DTC activation enable register 071 | DTCER071 | 8 | 8 | 2 ICLK |
| 0008 7162h | ICU | DTC activation enable register 098 | DTCER098 | 8 | 8 | 2 ICLK |
| 0008 7166h | ICU | DTC activation enable register 102 | DTCER102 | 8 | 8 | 2 ICLK |
| 0008 7167h | ICU | DTC activation enable register 103 | DTCER103 | 8 | 8 | 2 ICLK |
| 0008 716Ah | ICU | DTC activation enable register 106 | DTCER106 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (5 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7172h | ICU | DTC activation enable register 114 | DTCER114 | 8 | 8 | 2 ICLK |
| 0008 7173h | ICU | DTC activation enable register 115 | DTCER115 | 8 | 8 | 2 ICLK |
| 0008 7174h | ICU | DTC activation enable register 116 | DTCER116 | 8 | 8 | 2 ICLK |
| 0008 7175h | ICU | DTC activation enable register 117 | DTCER117 | 8 | 8 | 2 ICLK |
| 0008 7179h | ICU | DTC activation enable register 121 | DTCER121 | 8 | 8 | 2 ICLK |
| 0008 717Ah | ICU | DTC activation enable register 122 | DTCER122 | 8 | 8 | 2 ICLK |
| 0008 717Dh | ICU | DTC activation enable register 125 | DTCER125 | 8 | 8 | 2 ICLK |
| 0008 717Eh | ICU | DTC activation enable register 126 | DTCER126 | 8 | 8 | 2 ICLK |
| 0008 7181h | ICU | DTC activation enable register 129 | DTCER129 | 8 | 8 | 2 ICLK |
| 0008 7182h | ICU | DTC activation enable register 130 | DTCER130 | 8 | 8 | 2 ICLK |
| 0008 7183h | ICU | DTC activation enable register 131 | DTCER131 | 8 | 8 | 2 ICLK |
| 0008 7184h | ICU | DTC activation enable register 132 | DTCER132 | 8 | 8 | 2 ICLK |
| 0008 7186h | ICU | DTC activation enable register 134 | DTCER134 | 8 | 8 | 2 ICLK |
| 0008 7187h | ICU | DTC activation enable register 135 | DTCER135 | 8 | 8 | 2 ICLK |
| 0008 7188h | ICU | DTC activation enable register 136 | DTCER136 | 8 | 8 | 2 ICLK |
| 0008 7189h | ICU | DTC activation enable register 137 | DTCER137 | 8 | 8 | 2 ICLK |
| 0008 718Ah | ICU | DTC activation enable register 138 | DTCER138 | 8 | 8 | 2 ICLK |
| 0008 718Bh | ICU | DTC activation enable register 139 | DTCER139 | 8 | 8 | 2 ICLK |
| 0008 718Ch | ICU | DTC activation enable register 140 | DTCER140 | 8 | 8 | 2 ICLK |
| 0008 718Dh | ICU | DTC activation enable register 141 | DTCER141 | 8 | 8 | 2 ICLK |
| 0008 718Eh | ICU | DTC activation enable register 142 | DTCER142 | 8 | 8 | 2 ICLK |
| 0008 718Fh | ICU | DTC activation enable register 143 | DTCER143 | 8 | 8 | 2 ICLK |
| 0008 7190h | ICU | DTC activation enable register 144 | DTCER144 | 8 | 8 | 2 ICLK |
| 0008 7191h | ICU | DTC activation enable register 145 | DTCER145 | 8 | 8 | 2 ICLK |
| 0008 7195h | ICU | DTC activation enable register 149 | DTCER149 | 8 | 8 | 2 ICLK |
| 0008 7196h | ICU | DTC activation enable register 150 | DTCER150 | 8 | 8 | 2 ICLK |
| 0008 7197h | ICU | DTC activation enable register 151 | DTCER151 | 8 | 8 | 2 ICLK |
| 0008 7198h | ICU | DTC activation enable register 152 | DTCER152 | 8 | 8 | 2 ICLK |
| 0008 7199h | ICU | DTC activation enable register 153 | DTCER153 | 8 | 8 | 2 ICLK |
| 0008 71AEh | ICU | DTC activation enable register 174 | DTCER174 | 8 | 8 | 2 ICLK |
| 0008 71AFh | ICU | DTC activation enable register 175 | DTCER175 | 8 | 8 | 2 ICLK |
| 0008 71B0h | ICU | DTC activation enable register 176 | DTCER176 | 8 | 8 | 2 ICLK |
| 0008 71B1h | ICU | DTC activation enable register 177 | DTCER177 | 8 | 8 | 2 ICLK |
| 0008 71B2h | ICU | DTC activation enable register 178 | DTCER178 | 8 | 8 | 2 ICLK |
| 0008 71B3h | ICU | DTC activation enable register 179 | DTCER179 | 8 | 8 | 2 ICLK |
| 0008 71B4h | ICU | DTC activation enable register 180 | DTCER180 | 8 | 8 | 2 ICLK |
| 0008 71B5h | ICU | DTC activation enable register 181 | DTCER181 | 8 | 8 | 2 ICLK |
| 0008 71B6h | ICU | DTC activation enable register 182 | DTCER182 | 8 | 8 | 2 ICLK |
| 0008 71B7h | ICU | DTC activation enable register 183 | DTCER183 | 8 | 8 | 2 ICLK |
| 0008 71B8h | ICU | DTC activation enable register 184 | DTCER184 | 8 | 8 | 2 ICLK |
| 0008 71BAh | ICU | DTC activation enable register 186 | DTCER186 | 8 | 8 | 2 ICLK |
| 0008 71BBh | ICU | DTC activation enable register 187 | DTCER187 | 8 | 8 | 2 ICLK |
| 0008 71BCh | ICU | DTC activation enable register 188 | DTCER188 | 8 | 8 | 2 ICLK |
| 0008 71BDh | ICU | DTC activation enable register 189 | DTCER189 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (6 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 71BEh | ICU | DTC activation enable register 190 | DTCER190 | 8 | 8 | 2 ICLK |
| 0008 71C0h | ICU | DTC activation enable register 192 | DTCER192 | 8 | 8 | 2 ICLK |
| 0008 71C1h | ICU | DTC activation enable register 193 | DTCER193 | 8 | 8 | 2 ICLK |
| 0008 71C2h | ICU | DTC activation enable register 194 | DTCER194 | 8 | 8 | 2 ICLK |
| 0008 71C3h | ICU | DTC activation enable register 195 | DTCER195 | 8 | 8 | 2 ICLK |
| 0008 71C4h | ICU | DTC activation enable register 196 | DTCER196 | 8 | 8 | 2 ICLK |
| 0008 71D7h | ICU | DTC activation enable register 215 | DTCER215 | 8 | 8 | 2 ICLK |
| 0008 71D8h | ICU | DTC activation enable register 216 | DTCER216 | 8 | 8 | 2 ICLK |
| 0008 71DBh | ICU | DTC activation enable register 219 | DTCER219 | 8 | 8 | 2 ICLK |
| 0008 71DCh | ICU | DTC activation enable register 220 | DTCER220 | 8 | 8 | 2 ICLK |
| 0008 71DFh | ICU | DTC activation enable register 223 | DTCER223 | 8 | 8 | 2 ICLK |
| 0008 71E0h | ICU | DTC activation enable register 224 | DTCER224 | 8 | 8 | 2 ICLK |
| 0008 71F7h | ICU | DTC activation enable register 247 | DTCER247 | 8 | 8 | 2 ICLK |
| 0008 71F8h | ICU | DTC activation enable register 248 | DTCER248 | 8 | 8 | 2 ICLK |
| 0008 71FEh | ICU | DTC activation enable register 254 | DTCER254 | 8 | 8 | 2 ICLK |
| 0008 7202h | ICU | Interrupt request enable register 02 | IER02 | 8 | 8 | 2 ICLK |
| 0008 7203h | ICU | Interrupt request enable register 03 | IER03 | 8 | 8 | 2 ICLK |
| 0008 7205h | ICU | Interrupt request enable register 05 | IER05 | 8 | 8 | 2 ICLK |
| 0008 7207h | ICU | Interrupt request enable register 07 | IER07 | 8 | 8 | 2 ICLK |
| 0008 7208h | ICU | Interrupt request enable register 08 | IER08 | 8 | 8 | 2 ICLK |
| 0008 720Ch | ICU | Interrupt request enable register 0C | IER0C | 8 | 8 | 2 ICLK |
| 0008 720Dh | ICU | Interrupt request enable register 0D | IER0D | 8 | 8 | 2 ICLK |
| 0008 720Eh | ICU | Interrupt request enable register 0E | IER0E | 8 | 8 | 2 ICLK |
| 0008 720Fh | ICU | Interrupt request enable register 0F | IER0F | 8 | 8 | 2 ICLK |
| 0008 7210h | ICU | Interrupt request enable register 10 | IER10 | 8 | 8 | 2 ICLK |
| 0008 7211h | ICU | Interrupt request enable register 11 | IER11 | 8 | 8 | 2 ICLK |
| 0008 7212h | ICU | Interrupt request enable register 12 | IER12 | 8 | 8 | 2 ICLK |
| 0008 7213h | ICU | Interrupt request enable register 13 | IER13 | 8 | 8 | 2 ICLK |
| 0008 7215h | ICU | Interrupt request enable register 15 | IER15 | 8 | 8 | 2 ICLK |
| 0008 7216h | ICU | Interrupt request enable register 16 | IER16 | 8 | 8 | 2 ICLK |
| 0008 7217h | ICU | Interrupt request enable register 17 | IER17 | 8 | 8 | 2 ICLK |
| 0008 7218h | ICU | Interrupt request enable register 18 | IER18 | 8 | 8 | 2 ICLK |
| 0008 721Ah | ICU | Interrupt request enable register 1A | IER1A | 8 | 8 | 2 ICLK |
| 0008 721Bh | ICU | Interrupt request enable register 1B | IER1B | 8 | 8 | 2 ICLK |
| 0008 721Ch | ICU | Interrupt request enable register 1C | IER1C | 8 | 8 | 2 ICLK |
| 0008 721Eh | ICU | Interrupt request enable register 1E | IER1E | 8 | 8 | 2 ICLK |
| 0008 721Fh | ICU | Interrupt request enable register 1F | IER1F | 8 | 8 | 2 ICLK |
| 0008 72E0h | ICU | Software interrupt activation register | SWINTR | 8 | 8 | 2 ICLK |
| 0008 72F0h | ICU | Fast interrupt set register | FIR | 16 | 16 | 2 ICLK |
| 0008 7300h | ICU | Interrupt source priority register 00 | IPR00 | 8 | 8 | 2 ICLK |
| 0008 7301h | ICU | Interrupt source priority register 01 | IPR01 | 8 | 8 | 2 ICLK |
| 0008 7302h | ICU | Interrupt source priority register 02 | IPR02 | 8 | 8 | 2 ICLK |
| 0008 7303h | ICU | Interrupt source priority register 03 | IPR03 | 8 | 8 | 2 ICLK |
| 0008 7304h | ICU | Interrupt source priority register 04 | IPR04 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (7 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7305h | ICU | Interrupt source priority register 05 | IPR05 | 8 | 8 | 2 ICLK |
| 0008 7306h | ICU | Interrupt source priority register 06 | IPR06 | 8 | 8 | 2 ICLK |
| 0008 7307h | ICU | Interrupt source priority register 07 | IPR07 | 8 | 8 | 2 ICLK |
| 0008 7314h | ICU | Interrupt source priority register 14 | IPR14 | 8 | 8 | 2 ICLK |
| 0008 7318h | ICU | Interrupt source priority register 18 | IPR18 | 8 | 8 | 2 ICLK |
| 0008 7320h | ICU | Interrupt source priority register 20 | IPR20 | 8 | 8 | 2 ICLK |
| 0008 7321h | ICU | Interrupt source priority register 21 | IPR21 | 8 | 8 | 2 ICLK |
| 0008 7322h | ICU | Interrupt source priority register 22 | IPR22 | 8 | 8 | 2 ICLK |
| 0008 7323h | ICU | Interrupt source priority register 23 | IPR23 | 8 | 8 | 2 ICLK |
| 0008 7324h | ICU | Interrupt source priority register 24 | IPR24 | 8 | 8 | 2 ICLK |
| 0008 7325h | ICU | Interrupt source priority register 25 | IPR25 | 8 | 8 | 2 ICLK |
| 0008 7326h | ICU | Interrupt source priority register 26 | IPR26 | 8 | 8 | 2 ICLK |
| 0008 7327h | ICU | Interrupt source priority register 27 | IPR27 | 8 | 8 | 2 ICLK |
| 0008 7340h | ICU | Interrupt source priority register 40 | IPR40 | 8 | 8 | 2 ICLK |
| 0008 7344h | ICU | Interrupt source priority register 44 | IPR44 | 8 | 8 | 2 ICLK |
| 0008 7348h | ICU | Interrupt source priority register 48 | IPR48 | 8 | 8 | 2 ICLK |
| 0008 7349h | ICU | Interrupt source priority register 49 | IPR49 | 8 | 8 | 2 ICLK |
| 0008 7351h | ICU | Interrupt source priority register 51 | IPR51 | 8 | 8 | 2 ICLK |
| 0008 7352h | ICU | Interrupt source priority register 52 | IPR52 | 8 | 8 | 2 ICLK |
| 0008 7353h | ICU | Interrupt source priority register 53 | IPR53 | 8 | 8 | 2 ICLK |
| 0008 7354h | ICU | Interrupt source priority register 54 | IPR54 | 8 | 8 | 2 ICLK |
| 0008 7355h | ICU | Interrupt source priority register 55 | IPR55 | 8 | 8 | 2 ICLK |
| 0008 7356h | ICU | Interrupt source priority register 56 | IPR56 | 8 | 8 | 2 ICLK |
| 0008 7357h | ICU | Interrupt source priority register 57 | IPR57 | 8 | 8 | 2 ICLK |
| 0008 7358h | ICU | Interrupt source priority register 58 | IPR58 | 8 | 8 | 2 ICLK |
| 0008 7359h | ICU | Interrupt source priority register 59 | IPR59 | 8 | 8 | 2 ICLK |
| 0008 735Ah | ICU | Interrupt source priority register 5A | IPR5A | 8 | 8 | 2 ICLK |
| 0008 735Bh | ICU | Interrupt source priority register 5B | IPR5B | 8 | 8 | 2 ICLK |
| 0008 735Ch | ICU | Interrupt source priority register 5C | IPR5C | 8 | 8 | 2 ICLK |
| 0008 735Dh | ICU | Interrupt source priority register 5D | IPR5D | 8 | 8 | 2 ICLK |
| 0008 735Eh | ICU | Interrupt source priority register 5E | IPR5E | 8 | 8 | 2 ICLK |
| 0008 735Fh | ICU | Interrupt source priority register 5F | IPR5F | 8 | 8 | 2 ICLK |
| 0008 7360h | ICU | Interrupt source priority register 60 | IPR60 | 8 | 8 | 2 ICLK |
| 0008 7367h | ICU | Interrupt source priority register 67 | IPR67 | 8 | 8 | 2 ICLK |
| 0008 7368h | ICU | Interrupt source priority register 68 | IPR68 | 8 | 8 | 2 ICLK |
| 0008 7369h | ICU | Interrupt source priority register 69 | IPR69 | 8 | 8 | 2 ICLK |
| 0008 736Ah | ICU | Interrupt source priority register 6A | IPR6A | 8 | 8 | 2 ICLK |
| 0008 736Bh | ICU | Interrupt source priority register 6B | IPR6B | 8 | 8 | 2 ICLK |
| 0008 736Ch | ICU | Interrupt source priority register 6C | IPR6C | 8 | 8 | 2 ICLK |
| 0008 736Dh | ICU | Interrupt source priority register 6D | IPR6D | 8 | 8 | 2 ICLK |
| 0008 736Eh | ICU | Interrupt source priority register 6E | IPR6E | 8 | 8 | 2 ICLK |
| 0008 736Fh | ICU | Interrupt source priority register 6F | IPR6F | 8 | 8 | 2 ICLK |
| 0008 7380h | ICU | Interrupt source priority register 80 | IPR80 | 8 | 8 | 2 ICLK |
| 0008 7381h | ICU | Interrupt source priority register 81 | IPR81 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (8 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7382h | ICU | Interrupt source priority register 82 | IPR82 | 8 | 8 | 2 ICLK |
| 0008 7388h | ICU | Interrupt source priority register 88 | IPR88 | 8 | 8 | 2 ICLK |
| 0008 7389h | ICU | Interrupt source priority register 89 | IPR89 | 8 | 8 | 2 ICLK |
| 0008 738Ah | ICU | Interrupt source priority register 8A | IPR8A | 8 | 8 | 2 ICLK |
| 0008 738Bh | ICU | Interrupt source priority register 8B | IPR8B | 8 | 8 | 2 ICLK |
| 0008 7390h | ICU | Interrupt source priority register 90 | IPR90 | 8 | 8 | 2 ICLK |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | 2 ICLK |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | 2 ICLK |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | 2 ICLK |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | 2 ICLK |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | 2 ICLK |
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | 2 ICLK |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | 2 ICLK |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | 2 ICLK |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | 2 ICLK |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | 2 ICLK |
| 0008 7582h | ICU | Non-maskable interrupt clear register | NMICLR | 8 | 8 | 2 ICLK |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | 2 ICLK |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLK*3 |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLK*3 |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8028h | WDT | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8028h | WDT | Write window A register | WINA | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8029h | WDT | Timer counter | TCNT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 802Ah | WDT | Write window B register | WINB | 16 | 16 | 2, 3 PCLK*3 |
| 0008 802Bh | WDT | Reset control/status register | RSTCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8040h | ADA | A/D data register A | ADDRA | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8042h | ADA | A/D data register B | ADDRB | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8044h | ADA | A/D data register C | ADDRC | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8046h | ADA | A/D data register D | ADDRD | 16 | 16 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (9 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8048h | ADA | A/D data register E | ADDRE | 16 | 16 | 2, 3 PCLK*3 |
| 0008 804Ah | ADA | A/D data register F | ADDRF | 16 | 16 | 2, 3 PCLK*3 |
| 0008 804Ch | ADA | A/D data register G | ADDRG | 16 | 16 | 2, 3 PCLK*3 |
| 0008 804Eh | ADA | A/D data register H | ADDRH | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8050h | ADA | A/D control/status register | ADCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8051h | ADA | A/D control register | ADCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 805Bh | ADA | A/D sampling state register | ADSSTR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 805Dh | ADA | A/D self-diagnostic register | ADDIAGR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8060h | ADA | A/D data register I | ADDRI | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8062h | ADA | A/D data register J | ADDRJ | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8064h | ADA | A/D data register K | ADDRK | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8066h | ADA | A/D data register L | ADDRL | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8070h | ADA | A/D start trigger select register | ADSTRGR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8072h | ADA | A/D data placement register | ADDPR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8240h | SCI0 | Serial mode register | SMR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8241h | SCI0 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8242h | SCI0 | Serial control register | SCR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8243h | SCI0 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8244h | SCI0 | Serial status register | SSR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8245h | SCI0 | Receive data register | RDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8246h | SCI0 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8247h | SCI0 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8240h | SMCI0 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8241h | SMCI0 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8242h | SMCI0 | Serial control register | SCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8243h | SMCI0 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8244h | SMCI0 | Serial status register | SSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8245h | SMCI0 | Receive data register | RDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8246h | SMCI0 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8248h | SCI1 | Serial mode register | SMR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8249h | SCI1 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Ah | SCI1 | Serial control register | SCR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Bh | SCI1 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Ch | SCI1 | Serial status register | SSR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Dh | SCI1 | Receive data register | RDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Eh | SCI1 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Fh | SCI1 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8248h | SMCI1 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8249h | SMCI1 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Ah | SMCI1 | Serial control register | SCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Bh | SMCI1 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Ch | SMCI1 | Serial status register | SSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Dh | SMCI1 | Receive data register | RDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 824Eh | SMCI1 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (10 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8250h | SCI2 | Serial mode register | SMR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8251h | SCI2 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8252h | SCI2 | Serial control register | SCR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8253h | SCI2 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8254h | SCI2 | Serial status register | SSR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8255h | SCI2 | Receive data register | RDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8256h | SCI2 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8257h | SCI2 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8250h | SMCI2 | Serial mode register | SMR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8251h | SMCI2 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8252h | SMCI2 | Serial control register | SCR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8253h | SMCI2 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8254h | SMCI2 | Serial status register | SSR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8255h | SMCI2 | Receive data register | RDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8256h | SMCI2 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8300h | RIIC | I2C bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8301h | RIIC | I2C bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8302h | RIIC | I2C bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8303h | RIIC | I2C bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8304h | RIIC | I2C bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8305h | RIIC | I2C bus function enable register | ICFER | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8306h | RIIC | I2C bus status enable register | ICSER | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8307h | RIIC | I2C bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8308h | RIIC | I2C bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8309h | RIIC | I2C bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Ah | RIIC | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Ah | RIIC | Internal counter L for timeout | TMOCNTL | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Bh | RIIC | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Bh | RIIC | Internal counter U for timeout | TMOCNTU | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Bh | RIIC | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Ch | RIIC | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Dh | RIIC | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Eh | RIIC | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 830Fh | RIIC | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8310h | RIIC | I2C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8311h | RIIC | I2C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8312h | RIIC | I2C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8313h | RIIC | I2C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8380h | RSPI | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8381h | RSPI | RSPI slave select polarity register | SSLP | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8382h | RSPI | RSPI pin control register | SPPCR | 8 | 8 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (11 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8383h | RSPI | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8384h | RSPI | RSPI data register | SPDR | 16, 32 | 16, 32 | 2, 3 PCLK*3 |
| 0008 8388h | RSPI | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8389h | RSPI | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Ah | RSPI | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Bh | RSPI | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Ch | RSPI | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Dh | RSPI | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Eh | RSPI | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Fh | RSPI | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8390h | RSPI | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8392h | RSPI | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8394h | RSPI | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8396h | RSPI | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8398h | RSPI | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 839Ah | RSPI | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 839Ch | RSPI | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 839Eh | RSPI | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9000h | S12AD0 | A/D control register | ADCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 9004h | S12AD0 | A/D channel select register | ADANS | 16 | 16 | 2, 3 PCLK*3 |
| 0008 900Ah | S12AD0 | A/D programmable gain amplifier register | ADPG | 16 | 16 | 2, 3 PCLK*3 |
| 0008 900Eh | S12AD0 | A/D control extended register | ADCER | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9010h | S12AD0 | A/D start trigger select register | ADSTRGR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9012h | S12AD | Comparator operating mode select register 0 | ADCMPMD0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9014h | S12AD | Comparator operating mode select register 1 | ADCMPMD1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9016h | S12AD | Comparator filter mode register 0 | ADCMPNR0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9018h | S12AD | Comparator filter mode register 1 | ADCMPNR1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 901Ah | S12AD | Comparator detection flag register | ADCMPFR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 901Ch | S12AD | Comparator interrupt select register | ADCMPSEL | 16 | 16 | 2, 3 PCLK*3 |
| 0008 901Eh | S12AD0 | A/D data register Diag | ADRD | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9020h | S12AD0 | A/D data register 0A | ADDR0A | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9022h | S12AD0 | A/D data register 1 | ADDR1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9024h | S12AD0 | A/D data register 2 | ADDR2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9026h | S12AD0 | A/D data register 3 | ADDR3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9030h | S12AD0 | A/D data register 0B | ADDR0B | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9060h | S12AD0 | A/D sampling state register | ADSSTR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 9080h | S12AD1 | A/D control register | ADCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 9084h | S12AD1 | A/D channel select register | ADANS | 16 | 16 | 2, 3 PCLK*3 |
| 0008 908Ah | S12AD1 | A/D programmable gain amplifier register | ADPG | 16 | 16 | 2, 3 PCLK*3 |
| 0008 908Eh | S12AD1 | A/D control extended register | ADCER | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9090h | S12AD1 | A/D start trigger select register | ADSTRGR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 909Eh | S12AD1 | A/D data register Diag | ADRD | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90A0h | S12AD1 | A/D data register 0A | ADDR0A | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90A2h | S12AD1 | A/D data register 1 | ADDR1 | 16 | 16 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (12 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 90A4h | S12AD1 | A/D data register 2 | ADDR2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90A6h | S12AD1 | A/D data register 3 | ADDR3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90B0h | S12AD1 | A/D data register 0B | ADDR0B | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90E0h | S12AD1 | A/D sampling state register | ADSSTR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C001h | PORT1 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C002h | PORT2 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C003h | PORT3 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C007h | PORT7 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C008h | PORT8 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C009h | PORT9 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Ah | PORTA | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Bh | PORTB | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Dh | PORTD | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Eh | PORTE | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C010h | PORTG | Data direction register | DDR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C021h | PORT1 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C022h | PORT2 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C023h | PORT3 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C027h | PORT7 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C028h | PORT8 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C029h | PORT9 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Ah | PORTA | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Bh | PORTB | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Dh | PORTD | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Eh | PORTE | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C030h | PORTG | Data register | DR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C041h | PORT1 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C042h | PORT2 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C043h | PORT3 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C044h | PORT4 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C045h | PORT5 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C046h | PORT6 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C047h | PORT7 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C048h | PORT8 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C049h | PORT9 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Ah | PORTA | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Bh | PORTB | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Dh | PORTD | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Eh | PORTE | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C050h | PORTG | Port register | PORT*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C061h | PORT1 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C062h | PORT2 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C063h | PORT3 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C064h | PORT4 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (13 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C065h | PORT5 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C066h | PORT6 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C067h | PORT7 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C068h | PORT8 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C069h | PORT9 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C06Ah | PORTA | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C06Bh | PORTB | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C06Dh | PORTD | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C06Eh | PORTE | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C070h | PORTG | Input buffer control register | ICR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C108h | IOPORT | Port function register 8 | PF8IRQ | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C109h | IOPORT | Port function register 9 | PF9IRQ | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C10Ah | IOPORT | Port function register A | PFAADC | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C10Ch | IOPORT | Port function register C | PFCMTU | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C10Dh | IOPORT | Port function register D | PFDGPT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C10Fh | IOPORT | Port function register F | PFFSCI | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C110h | IOPORT | Port function register G | PFGSPI | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C111h | IOPORT | Port function register H | PFHSPI | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C113h | IOPORT | Port function register J | PFJCAN | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C114h | IOPORT | Port function register K | PFKLIN | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C116h | IOPORT | Port function register M | PFMPOE | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C117h | IOPORT | Port function register N | PFNPOE | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C280h | SYSTEM | Deep standby control register | DPSBYCR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C281h | SYSTEM | Deep standby wait control register | DPSWCR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C282h | SYSTEM | Deep standby interrupt enable register | DPSIER | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C283h | SYSTEM | Deep standby interrupt flag register | DPSIFR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C284h | SYSTEM | Deep standby interrupt edge register | DPSIEGR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C285h | SYSTEM | Reset status register | RSTSR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C289h | FLASH | Flash write erase protection register | FWEPROR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C28Ch | SYSTEM | Key code register for low-voltage detection control register | LVDKEYR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C28Dh | SYSTEM | Voltage detection control register | LVDCR | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C290h | SYSTEM | Deep standby backup register 0 | DPSBKR0 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C291h | SYSTEM | Deep standby backup register 1 | DPSBKR1 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C292h | SYSTEM | Deep standby backup register 2 | DPSBKR2 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C293h | SYSTEM | Deep standby backup register 3 | DPSBKR3 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C294h | SYSTEM | Deep standby backup register 4 | DPSBKR4 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C295h | SYSTEM | Deep standby backup register 5 | DPSBKR5 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C296h | SYSTEM | Deep standby backup register 6 | DPSBKR6 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C297h | SYSTEM | Deep standby backup register 7 | DPSBKR7 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C298h | SYSTEM | Deep standby backup register 8 | DPSBKR8 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C299h | SYSTEM | Deep standby backup register 9 | DPSBKR9 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C29Ah | SYSTEM | Deep standby backup register 10 | DPSBKR10 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C29Bh | SYSTEM | Deep standby backup register 11 | DPSBKR11 | 8 | 8 | 4, 5 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (14 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C29Ch | SYSTEM | Deep standby backup register 12 | DPSBKR12 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C29Dh | SYSTEM | Deep standby backup register 13 | DPSBKR13 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C29Eh | SYSTEM | Deep standby backup register 14 | DPSBKR14 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C29Fh | SYSTEM | Deep standby backup register 15 | DPSBKR15 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A0h | SYSTEM | Deep standby backup register 16 | DPSBKR16 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A1h | SYSTEM | Deep standby backup register 17 | DPSBKR17 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A2h | SYSTEM | Deep standby backup register 18 | DPSBKR18 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A3h | SYSTEM | Deep standby backup register 19 | DPSBKR19 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A4h | SYSTEM | Deep standby backup register 20 | DPSBKR20 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A5h | SYSTEM | Deep standby backup register 21 | DPSBKR21 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A6h | SYSTEM | Deep standby backup register 22 | DPSBKR22 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A7h | SYSTEM | Deep standby backup register 23 | DPSBKR23 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A8h | SYSTEM | Deep standby backup register 24 | DPSBKR24 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2A9h | SYSTEM | Deep standby backup register 25 | DPSBKR25 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2AAh | SYSTEM | Deep standby backup register 26 | DPSBKR26 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2ABh | SYSTEM | Deep standby backup register 27 | DPSBKR27 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2ACh | SYSTEM | Deep standby backup register 28 | DPSBKR28 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2ADh | SYSTEM | Deep standby backup register 29 | DPSBKR29 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2AEh | SYSTEM | Deep standby backup register 30 | DPSBKR30 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C2AFh | SYSTEM | Deep standby backup register 31 | DPSBKR31 | 8 | 8 | 4, 5 PCLK*3 |
| 0008 C4C0h | POE | Input level control/status register 1 | ICSR1 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4C2h | POE | Output level control/status register 1 | OCSR1 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4C4h | POE | Input level control/status register 2 | ICSR2 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4C6h | POE | Output level control/status register 2 | OCSR2 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4C8h | POE | Input level control/status register 3 | ICSR3 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4CAh | POE | Software port output enable register | SPOER | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C4CBh | POE | Port output enable control register 1 | POECR1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C4CCh | POE | Port output enable control register 2 | POECR2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 C4CEh | POE | Port output enable control register 3 | POECR3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 C4D0h | POE | Port output enable control register 4 | POECR4 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 C4D2h | POE | Port output enable control register 5 | POECR5 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 C4D4h | POE | Port output enable control register 6 | POECR6 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 C4D6h | POE | Input level control/status register 4 | ICSR4 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4D8h | POE | Input level control/status register 5 | ICSR5 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0008 C4DAh | POE | Active level setting register 1 | ALR1 | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0009 0200h to 0009 03FFh | CAN0*2 | Mailbox registers 0 to 31 | MB0 to MB 31 | 128 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0400h | CAN0*2 | Mask register 0 | MKR0 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0404h | CAN0*2 | Mask register 1 | MKR1 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0408h | CAN0*2 | Mask register 2 | MKR2 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 040Ch | CAN0*2 | Mask register 3 | MKR3 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0410h | CAN0*2 | Mask register 4 | MKR4 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0414h | CAN0*2 | Mask register 5 | MKR5 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0418h | CAN0*2 | Mask register 6 | MKR6 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (15 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0009 041Ch | CAN0*2 | Mask register 7 | MKR7 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0420h | CAN0*2 | FIFO received ID compare register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0424h | CAN0*2 | FIFO received ID compare register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0428h | CAN0*2 | Mask invalid register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 042Ch | CAN0*2 | Mailbox interrupt enable register | MIER | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0820h to 0009 083Fh | CAN0*2 | Message control registers 0 to 31 | MCTL0 to MCTL31 | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0840h | CAN0*2 | Control register | CTLR | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0009 0842h | CAN0*2 | Status register | STR | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0009 0844h | CAN0*2 | Bit configuration register | BCR | 32 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 0848h | CAN0*2 | Receive FIFO control register | RFCR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0849h | CAN0*2 | Receive FIFO pointer control register | RFPCR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 084Ah | CAN0*2 | Transmit FIFO control register | TFCR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 084Bh | CAN0*2 | Transmit FIFO pointer control register | TFPCR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 084Ch | CAN0*2 | Error interrupt enable register | EIER | 8 | 8 | 2, 3 PCLK*3 |
| 0009 084Dh | CAN0*2 | Error interrupt factor judge register | EIFR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 084Eh | CAN0*2 | Receive error count register | RECR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 084Fh | CAN0*2 | Transmit error count register | TECR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0850h | CAN0*2 | Error code store register | ECSR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0851h | CAN0*2 | Channel search support register | CSSR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0852h | CAN0*2 | Mailbox search status register | MSSR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0853h | CAN0*2 | Mailbox search mode register | MSMR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 0854h | CAN0*2 | Time stamp register | TSR | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0009 0856h | CAN0*2 | Acceptance filter support register | AFSR | 16 | 8, 16 | 2, 3 PCLK*3 |
| 0009 0858h | CAN0*2 | Test control register | TCR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 4001h | LIN0 | LIN wake-up baud rate select register | LWBR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 4002h | LIN0 | LIN baud rate prescaler 0 register | LBRP0 | 8 | 8, 16 | 2, 3 PCLK*3 |
| 0009 4003h | LIN0 | LIN baud rate prescaler 1 register | LBRP1 | 8 | 8, 16 | 2, 3 PCLK*3 |
| 0009 4004h | LIN0 | LIN self-test control register | LSTC | 8 | 8 | 2, 3 PCLK*3 |
| 0009 4008h | LIN0 | Mode register | L0MD | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 4009h | LIN0 | Break field setting register | L0BRK | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 400Ah | LIN0 | Space setting register | L0SPC | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 400Bh | LIN0 | Wake-up setting register | L0WUP | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 400Ch | LIN0 | Interrupt enable register | L0IE | 8 | 8, 16 | 2, 3 PCLK*3 |
| 0009 400Dh | LIN0 | Error detection enable register | L0EDE | 8 | 8, 16 | 2, 3 PCLK*3 |
| 0009 400Eh | LIN0 | Control register | L0C | 8 | 8 | 2, 3 PCLK*3 |
| 0009 4010h | LIN0 | Transmission control register | L0TC | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 4011h | LIN0 | Mode status register | L0MST | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 4012h | LIN0 | Status register | L0ST | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 4013h | LIN0 | Error status register | L0EST | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 4014h | LIN0 | Response field set register | L0RFC | 8 | 8, 16 | 2, 3 PCLK*3 |
| 0009 4015h | LIN0 | Buffer register | L0IDB | 8 | 8, 16 | 2, 3 PCLK*3 |
| 0009 4016h | LIN0 | Check sum buffer register | L0CBR | 8 | 8 | 2, 3 PCLK*3 |
| 0009 4018h | LIN0 | Data 1 buffer register | L0DB1 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (16 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0009 4019h | LIN0 | Data 2 buffer register | L0DB2 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Ah | LIN0 | Data 3 buffer register | L0DB3 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Bh | LIN0 | Data 4 buffer register | L0DB4 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Ch | LIN0 | Data 5 buffer register | L0DB5 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Dh | LIN0 | Data 6 buffer register | L0DB6 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Eh | LIN0 | Data 7 buffer register | L0DB7 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Fh | LIN0 | Data 8 buffer register | L0DB8 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 000C 1200h | MTU3 | Timer control register | TCR | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1201h | MTU4 | Timer control register | TCR | 8 | 8 | 5 ICLK |
| 000C 1202h | MTU3 | Timer mode register 1 | TMDR1 | 8 | 8, 16 | 5 ICLK |
| 000C 1203h | MTU4 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1204h | MTU3 | Timer I/O control register H | TIORH | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1205h | MTU3 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1206h | MTU4 | Timer I/O control register H | TIORH | 8 | 8, 16 | 5 ICLK |
| 000C 1207h | MTU4 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1208h | MTU3 | Timer interrupt enable register | TIER | 8 | 8, 16 | 5 ICLK |
| 000C 1209h | MTU4 | Timer interrupt enable register | TIER | 8 | 8 | 5 ICLK |
| 000C 120Ah | MTU | Timer output master enable register A | TOERA | 8 | 8 | 5 ICLK |
| 000C 120Dh | MTU | Timer gate control register A | TGCRA | 8 | 8 | 5 ICLK |
| 000C 120Eh | MTU | Timer output control register 1A | TOCR1A | 8 | 8, 16 | 5 ICLK |
| 000C 120Fh | MTU | Timer output control register 2A | TOCR2A | 8 | 8 | 5 ICLK |
| 000C 1210h | MTU3 | Timer counter | TCNT | 16 | 16, 32 | 5 ICLK |
| 000C 1212h | MTU4 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1214h | MTU | Timer cycle data register A | TCDRA | 16 | 16, 32 | 5 ICLK |
| 000C 1216h | MTU | Timer dead time data register A | TDDRA | 16 | 16 | 5 ICLK |
| 000C 1218h | MTU3 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 121Ah | MTU3 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 121Ch | MTU4 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 121Eh | MTU4 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 1220h | MTU | Timer subcounter A | TCNTSA | 16 | 16, 32 | 5 ICLK |
| 000C 1222h | MTU | Timer cycle buffer register A | TCBRA | 16 | 16 | 5 ICLK |
| 000C 1224h | MTU3 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 1226h | MTU3 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 1228h | MTU4 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 122Ah | MTU4 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 122Ch | MTU3 | Timer status register | TSR | 8 | 8, 16 | 5 ICLK |
| 000C 122Dh | MTU4 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1230h | MTU | Timer interrupt skipping set register 1A | TITCR1A | 8 | 8, 16 | 5 ICLK |
| 000C 1231h | MTU | Timer interrupt skipping counter 1A | TITCNT1A | 8 | 8 | 5 ICLK |
| 000C 1232h | MTU | Timer buffer transfer set register A | TBTERA | 8 | 8 | 5 ICLK |
| 000C 1234h | MTU | Timer dead time enable register A | TDERA | 8 | 8 | 5 ICLK |
| 000C 1236h | MTU | Timer output level buffer register A | TOLBRA | 8 | 8 | 5 ICLK |
| 000C 1238h | MTU3 | Timer buffer operation transfer mode register | TBTM | 8 | 8, 16 | 5 ICLK |
| 000C 1239h | MTU4 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 5 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (17 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 123Ah | MTU | Timer interrupt skipping mode register A | TITMRA | 8 | 8 | 5 ICLK |
| 000C 123Bh | MTU | Timer interrupt skipping set register 2A | TITCR2A | 8 | 8 | 5 ICLK |
| 000C 123Ch | MTU | Timer interrupt skipping counter 2A | TITCNT2A | 8 | 8 | 5 ICLK |
| 000C 1240h | MTU4 | Timer A/D converter start request control register | TADCR | 16 | 16 | 5 ICLK |
| 000C 1244h | MTU4 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16, 32 | 5 ICLK |
| 000C 1246h | MTU4 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 5 ICLK |
| 000C 1248h | MTU4 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16, 32 | 5 ICLK |
| 000C 124Ah | MTU4 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 5 ICLK |
| 000C 1260h | MTU | Timer waveform control register A | TWCRA | 8 | 8 | 5 ICLK |
| 000C 1270h | MTU3 | Timer mode register 2A | TMDR2A | 8 | 8 | 5 ICLK |
| 000C 1272h | MTU3 | Timer general register E | TGRE | 16 | 16 | 5 ICLK |
| 000C 1274h | MTU4 | Timer general register E | TGRE | 16 | 16 | 5 ICLK |
| 000C 1276h | MTU4 | Timer general register F | TGRF | 16 | 16 | 5 ICLK |
| 000C 1280h | MTU | Timer start register A | TSTRA | 8 | 8, 16 | 5 ICLK |
| 000C 1281h | MTU | Timer synchronous register A | TSYRA | 8 | 8 | 5 ICLK |
| 000C 1282h | MTU | Timer counter synchronous start register | TCSYSTR | 8 | 8 | 5 ICLK |
| 000C 1284h | MTU | Timer read/write enable register A | TRWERA | 8 | 8 | 5 ICLK |
| 000C 1300h | MTU0 | Timer control register | TCR | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1301h | MTU0 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1302h | MTU0 | Timer I/O control register H | TIORH | 8 | 8, 16 | 5 ICLK |
| 000C 1303h | MTU0 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1304h | MTU0 | Timer interrupt enable register | TIER | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1305h | MTU0 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1306h | MTU0 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1308h | MTU0 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 130Ah | MTU0 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 130Ch | MTU0 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 130Eh | MTU0 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 1320h | MTU0 | Timer general register E | TGRE | 16 | 16, 32 | 5 ICLK |
| 000C 1322h | MTU0 | Timer general register F | TGRF | 16 | 16 | 5 ICLK |
| 000C 1324h | MTU0 | Timer interrupt enable register 2 | TIER2 | 8 | 8, 16 | 5 ICLK |
| 000C 1325h | MTU0 | Timer status register 2 | TSR2 | 8 | 8 | 5 ICLK |
| 000C 1326h | MTU0 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 5 ICLK |
| 000C 1380h | MTU1 | Timer control register | TCR | 8 | 8, 16 | 5 ICLK |
| 000C 1381h | MTU1 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1382h | MTU1 | Timer I/O control register | TIOR | 8 | 8 | 5 ICLK |
| 000C 1384h | MTU1 | Timer interrupt enable register | TIER | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1385h | MTU1 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1386h | MTU1 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1388h | MTU1 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 138Ah | MTU1 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (18 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 1390h | MTU1 | Timer input capture control register | TICCR | 8 | 8 | 5 ICLK |
| 000C 1400h | MTU2 | Timer control register | TCR | 8 | 8, 16 | 5 ICLK |
| 000C 1401h | MTU2 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1402h | MTU2 | Timer I/O control register | TIOR | 8 | 8 | 5 ICLK |
| 000C 1404h | MTU2 | Timer interrupt enable register | TIER | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1405h | MTU2 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1406h | MTU2 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1408h | MTU2 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 140Ah | MTU2 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 1A00h | MTU6 | Timer control register | TCR | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1A01h | MTU7 | Timer control register | TCR | 8 | 8 | 5 ICLK |
| 000C 1A02h | MTU6 | Timer mode register 1 | TMDR1 | 8 | 8, 16 | 5 ICLK |
| 000C 1A03h | MTU7 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1A04h | MTU6 | Timer I/O control register H | TIORH | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1A05h | MTU6 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1A06h | MTU7 | Timer I/O control register H | TIORH | 8 | 8, 16 | 5 ICLK |
| 000C 1A07h | MTU7 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1A08h | MTU6 | Timer interrupt enable register | TIER | 8 | 8, 16 | 5 ICLK |
| 000C 1A09h | MTU7 | Timer interrupt enable register | TIER | 8 | 8 | 5 ICLK |
| 000C 1A0Ah | MTU | Timer output master enable register B | TOERB | 8 | 8 | 5 ICLK |
| 000C 1A0Eh | MTU | Timer output control register 1B | TOCR1B | 8 | 8, 16 | 5 ICLK |
| 000C 1A0Fh | MTU | Timer output control register 2B | TOCR2B | 8 | 8 | 5 ICLK |
| 000C 1A10h | MTU6 | Timer counter | TCNT | 16 | 16, 32 | 5 ICLK |
| 000C 1A12h | MTU7 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1A14h | MTU | Timer cycle data register B | TCDRB | 16 | 16, 32 | 5 ICLK |
| 000C 1A16h | MTU | Timer dead time data register B | TDDRB | 16 | 16 | 5 ICLK |
| 000C 1A18h | MTU6 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 1A1Ah | MTU6 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 1A1Ch | MTU7 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 1A1Eh | MTU7 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 1A20h | MTU | Timer subcounter B | TCNTSB | 16 | 16, 32 | 5 ICLK |
| 000C 1A22h | MTU | Timer cycle buffer register B | TCBRB | 16 | 16 | 5 ICLK |
| 000C 1A24h | MTU6 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 1A26h | MTU6 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 1A28h | MTU7 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 1A2Ah | MTU7 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 1A2Ch | MTU6 | Timer status register | TSR | 8 | 8, 16 | 5 ICLK |
| 000C 1A2Dh | MTU7 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1A30h | MTU | Timer interrupt skipping set register 1B | TITCR1B | 8 | 8, 16 | 5 ICLK |
| 000C 1A31h | MTU | Timer interrupt skipping counter 1B | TITCNT1B | 8 | 8 | 5 ICLK |
| 000C 1A32h | MTU | Timer buffer transfer set register B | TBTERB | 8 | 8 | 5 ICLK |
| 000C 1A34h | MTU | Timer dead time enable register B | TDERB | 8 | 8 | 5 ICLK |
| 000C 1A36h | MTU | Timer output level buffer register B | TOLBRB | 8 | 8 | 5 ICLK |
| 000C 1A38h | MTU6 | Timer buffer operation transfer mode register | TBTM | 8 | 8, 16 | 5 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (19 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 1A39h | MTU7 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 5 ICLK |
| 000C 1A3Ah | MTU | Timer interrupt skipping mode register B | TITMRB | 8 | 8 | 5 ICLK |
| 000C 1A3Bh | MTU | Timer interrupt skipping set register 2B | TITCR2B | 8 | 8 | 5 ICLK |
| 000C 1A3Ch | MTU | Timer interrupt skipping counter 2B | TITCNT2B | 8 | 8 | 5 ICLK |
| 000C 1A40h | MTU7 | Timer A/D converter start request control register | TADCR | 16 | 16 | 5 ICLK |
| 000C 1A44h | MTU7 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16, 32 | 5 ICLK |
| 000C 1A46h | MTU7 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 5 ICLK |
| 000C 1A48h | MTU7 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16, 32 | 5 ICLK |
| 000C 1A4Ah | MTU7 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 5 ICLK |
| 000C 1A50h | MTU6 | Timer synchronous clear register | TSYCR | 8 | 8 | 5 ICLK |
| 000C 1A60h | MTU | Timer waveform control register B | TWCRB | 8 | 8 | 5 ICLK |
| 000C 1A70h | MTU | Timer mode register 2B | TMDR2B | 8 | 8 | 5 ICLK |
| 000C 1A72h | MTU6 | Timer general register E | TGRE | 16 | 16 | 5 ICLK |
| 000C 1A74h | MTU7 | Timer general register E | TGRE | 16 | 16 | 5 ICLK |
| 000C 1A76h | MTU7 | Timer general register F | TGRF | 16 | 16 | 5 ICLK |
| 000C 1A80h | MTU | Timer start register B | TSTRB | 8 | 8, 16 | 5 ICLK |
| 000C 1A81h | MTU | Timer synchronous register B | TSYRB | 8 | 8 | 5 ICLK |
| 000C 1A84h | MTU | Timer read/write enable register B | TRWERB | 8 | 8 | 5 ICLK |
| 000C 1C80h | MTU5 | Timer counter U | TCNTU | 16 | 16, 32 | 5 ICLK |
| 000C 1C82h | MTU5 | Timer general register U | TGRU | 16 | 16 | 5 ICLK |
| 000C 1C84h | MTU5 | Timer control register U | TCRU | 8 | 8 | 5 ICLK |
| 000C 1C86h | MTU5 | Timer I/O control register U | TIORU | 8 | 8 | 5 ICLK |
| 000C 1C90h | MTU5 | Timer counter V | TCNTV | 16 | 16, 32 | 5 ICLK |
| 000C 1C92h | MTU5 | Timer general register V | TGRV | 16 | 16 | 5 ICLK |
| 000C 1C94h | MTU5 | Timer control register V | TCRV | 8 | 8 | 5 ICLK |
| 000C 1C96h | MTU5 | Timer I/O control register V | TIORV | 8 | 8 | 5 ICLK |
| 000C 1CA0h | MTU5 | Timer counter W | TCNTW | 16 | 16, 32 | 5 ICLK |
| 000C 1CA2h | MTU5 | Timer general register W | TGRW | 16 | 16 | 5 ICLK |
| 000C 1CA4h | MTU5 | Timer control register W | TCRW | 8 | 8 | 5 ICLK |
| 000C 1CA6h | MTU5 | Timer I/O control register W | TIORW | 8 | 8 | 5 ICLK |
| 000C 1CB0h | MTU5 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1CB2h | MTU5 | Timer interrupt enable register | TIER | 8 | 8 | 5 ICLK |
| 000C 1CB4h | MTU5 | Timer start register | TSTR | 8 | 8 | 5 ICLK |
| 000C 1CB6h | MTU5 | Timer compare match clear register | TCNTCMPCLR | 8 | 8 | 5 ICLK |
| 000C 2000h | GPT | General PWM timer software start register | GTSTR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2004h | GPT | General PWM timer hardware source start control register | GTHSCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2006h | GPT | General PWM timer hardware source clear control register | GTHCCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2008h | GPT | General PWM timer hardware start source select register | GTHSSR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |

**Table 4.1 List of I/O Registers (Address Order) (20 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 200Ah | GPT | General PWM timer hardware stop/clear source select register | GTHPSR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 200Ch | GPT | General PWM timer write-protection register | GTWP | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 200Eh | GPT | General PWM timer sync register | GTSYNC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2010h | GPT | General PWM timer external trigger input interrupt register | GTETINT | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2014h | GPT | General PWM timer buffer operation disable register | GTBDR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2018h | GPT | General PWM timer start write protection register | GTSWP | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2080h | GPT | LOCO count control register | LCCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2082h | GPT | LOCO count status register | LCST | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2084h | GPT | LOCO count value register | LCNT | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2086h | GPT | LOCO count result average register | LCNTA | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2088h | GPT | LOCO count result register 0 | LCNT00 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 208Ah | GPT | LOCO count result register 1 | LCNT01 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 208Ch | GPT | LOCO count result register 2 | LCNT02 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 208Eh | GPT | LOCO count result register 3 | LCNT03 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2090h | GPT | LOCO count result register 4 | LCNT04 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2092h | GPT | LOCO count result register 5 | LCNT05 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2094h | GPT | LOCO count result register 6 | LCNT06 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2096h | GPT | LOCO count result register 7 | LCNT07 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| '000C 2098h | GPT | LOCO count result register 8 | LCNT08 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 209Ah | GPT | LOCO count result register 9 | LCNT09 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 209Ch | GPT | LOCO count result register 10 | LCNT10 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 209Eh | GPT | LOCO count result register 11 | LCNT11 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 20A0h | GPT | LOCO count result register 12 | LCNT12 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 20A2h | GPT | LOCO count result register 13 | LCNT13 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 20A4h | GPT | LOCO count result register 14 | LCNT14 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 20A6h | GPT | LOCO count result register 15 | LCNT15 | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 20A8h | GPT | LOCO count upper permissible deviation register | LCNTDU | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 20AAh | GPT | LOCO count lower permissible deviation register | LCNTDL | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2100h | GPT0 | General PWM timer I/O control register | GTIOR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2102h | GPT0 | General PWM timer interrupt output setting register | GTINTAD | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2104h | GPT0 | General PWM timer control register | GTCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2106h | GPT0 | General PWM timer buffer enable register | GTBER | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2108h | GPT0 | General PWM timer count direction register | GTUDC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 210Ah | GPT0 | General PWM timer interrupt and A/D converter start request skipping setting register | GTITC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 210Ch | GPT0 | General PWM timer status register | GTST | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 210Eh | GPT0 | General PWM timer counter | GTCNT | 16 | 16 | 3 to 5 ICLK*4 |
| 000C 2110h | GPT0 | General PWM timer compare capture register A | GTCCRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2112h | GPT0 | General PWM timer compare capture register B | GTCCRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2114h | GPT0 | General PWM timer compare capture register C | GTCCRC | 16 | 16, 32 | 3 to 5 ICLK*4 |

**Table 4.1 List of I/O Registers (Address Order) (21 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 2116h | GPT0 | General PWM timer compare capture register D | GTCCRD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2118h | GPT0 | General PWM timer compare capture register E | GTCCRE | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 211Ah | GPT0 | General PWM timer compare capture register F | GTCCRF | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 211Ch | GPT0 | General PWM timer cycle setting register | GTPR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 211Eh | GPT0 | General PWM timer cycle setting buffer register | GTPBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2120h | GPT0 | General PWM timer cycle setting double-buffer register | GTPDBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2124h | GPT0 | A/D converter start request timing register A | GTADTRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2126h | GPT0 | A/D converter start request timing buffer register A | GTADTBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2128h | GPT0 | A/D converter start request timing double-buffer register A | GTADTDBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 212Ch | GPT0 | A/D converter start request timing register B | GTADTRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 212Eh | GPT0 | A/D converter start request timing buffer register B | GTADTBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2130h | GPT0 | A/D converter start request timing double-buffer register B | GTADTDBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2134h | GPT0 | General PWM timer output negate control register | GTONCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2136h | GPT0 | General PWM timer dead time control register | GTDTCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2138h | GPT0 | General PWM timer dead time value register | GTDVU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 213Ah | GPT0 | General PWM timer dead time value register | GTDVD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 213Ch | GPT0 | General PWM timer dead time buffer register | GTDBU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 213Eh | GPT0 | General PWM timer dead time buffer register | GTDBD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2140h | GPT0 | General PWM timer output protection function status register | GTSOS | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2142h | GPT0 | General PWM timer output protection function temporary release register | GTSOTR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2180h | GPT1 | General PWM timer I/O control register | GTIOR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2182h | GPT1 | General PWM timer interrupt output setting register | GTINTAD | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2184h | GPT1 | General PWM timer control register | GTCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2186h | GPT1 | General PWM timer buffer enable register | GTBER | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2188h | GPT1 | General PWM timer count direction register | GTUDC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 218Ah | GPT1 | General PWM timer interrupt and A/D converter start request skipping setting register | GTITC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 218Ch | GPT1 | General PWM timer status register | GTST | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 218Eh | GPT1 | General PWM timer counter | GTCNT | 16 | 16 | 3 to 5 ICLK*4 |
| 000C 2190h | GPT1 | General PWM timer compare capture register A | GTCCRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2192h | GPT1 | General PWM timer compare capture register B | GTCCRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2194h | GPT1 | General PWM timer compare capture register C | GTCCRC | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2196h | GPT1 | General PWM timer compare capture register D | GTCCRD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2198h | GPT1 | General PWM timer compare capture register E | GTCCRE | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 219Ah | GPT1 | General PWM timer compare capture register F | GTCCRF | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 219Ch | GPT1 | General PWM timer cycle setting register | GTPR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 219Eh | GPT1 | General PWM timer cycle setting buffer register | GTPBR | 16 | 16, 32 | 3 to 5 ICLK*4 |

**Table 4.1 List of I/O Registers (Address Order) (22 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 21A0h | GPT1 | General PWM timer cycle setting double-buffer register | GTPDBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21A4h | GPT1 | A/D converter start request timing register A | GTADTRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21A6h | GPT1 | A/D converter start request timing buffer register A | GTADTBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21A8h | GPT1 | A/D converter start request timing double-buffer register A | GTADTDBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21ACh | GPT1 | A/D converter start request timing register B | GTADTRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21AEh | GPT1 | A/D converter start request timing buffer register B | GTADTBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21B0h | GPT1 | A/D converter start request timing double-buffer register B | GTADTDBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21B4h | GPT1 | General PWM timer output negate control register | GTONCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21B6h | GPT1 | General PWM timer dead time control register | GTDTCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21B8h | GPT1 | General PWM timer dead time value register | GTDVU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21BAh | GPT1 | General PWM timer dead time value register | GTDVD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21BCh | GPT1 | General PWM timer dead time buffer register | GTDBU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21BEh | GPT1 | General PWM timer dead time buffer register | GTDBD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21C0h | GPT1 | General PWM timer output protection function status register | GTSOS | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 21C2h | GPT1 | General PWM timer output protection temporary release register | GTSOTR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2200h | GPT2 | General PWM timer I/O control register | GTIOR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2202h | GPT2 | General PWM timer interrupt output setting register | GTINTAD | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2204h | GPT2 | General PWM timer control register | GTCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2206h | GPT2 | General PWM timer buffer enable register | GTBER | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2208h | GPT2 | General PWM timer count direction register | GTUDC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 220Ah | GPT2 | General PWM timer interrupt and A/D converter start request skipping setting register | GTITC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 220Ch | GPT2 | General PWM timer status register | GTST | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 220Eh | GPT2 | General PWM timer counter | GTCNT | 16 | 16 | 3 to 5 ICLK*4 |
| 000C 2210h | GPT2 | General PWM timer compare capture register A | GTCCRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2212h | GPT2 | General PWM timer compare capture register B | GTCCRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2214h | GPT2 | General PWM timer compare capture register C | GTCCRC | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2216h | GPT2 | General PWM timer compare capture register D | GTCCRD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2218h | GPT2 | General PWM timer compare capture register E | GTCCRE | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 221Ah | GPT2 | General PWM timer compare capture register F | GTCCRF | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 221Ch | GPT2 | General PWM timer cycle setting register | GTPR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 221Eh | GPT2 | General PWM timer cycle setting buffer register | GTPBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2220h | GPT2 | General PWM timer cycle setting double-buffer register | GTPDBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2224h | GPT2 | A/D converter start request timing register A | GTADTRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2226h | GPT2 | A/D converter start request timing buffer register A | GTADTBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2228h | GPT2 | A/D converter start request timing double-buffer register A | GTADTDBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |

**Table 4.1 List of I/O Registers (Address Order) (23 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 222Ch | GPT2 | A/D converter start request timing register B | GTADTRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 222Eh | GPT2 | A/D converter start request timing buffer register B | GTADTBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2230h | GPT2 | A/D converter start request timing double-buffer register B | GTADTDBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2234h | GPT2 | General PWM timer output negate control register | GTONCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2236h | GPT2 | General PWM timer dead time control register | GTDTCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2238h | GPT2 | General PWM timer dead time value register | GTDVU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 223Ah | GPT2 | General PWM timer dead time value register | GTDVD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 223Ch | GPT2 | General PWM timer dead time buffer register | GTDBU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 223Eh | GPT2 | General PWM timer dead time buffer register | GTDBD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2240h | GPT2 | General PWM timer output protection function status register | GTSOS | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2242h | GPT2 | General PWM timer output protection temporary release register | GTSOTR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2280h | GPT3 | General PWM timer I/O control register | GTIOR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2282h | GPT3 | General PWM timer interrupt output setting register | GTINTAD | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2284h | GPT3 | General PWM timer control register | GTCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2286h | GPT3 | General PWM timer buffer enable register | GTBER | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2288h | GPT3 | General PWM timer count direction register | GTUDC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 228Ah | GPT3 | General PWM timer interrupt and A/D converter start request skipping setting register | GTITC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 228Ch | GPT3 | General PWM timer status register | GTST | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 228Eh | GPT3 | General PWM timer counter | GTCNT | 16 | 16 | 3 to 5 ICLK*4 |
| 000C 2290h | GPT3 | General PWM timer compare capture register A | GTCCRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2292h | GPT3 | General PWM timer compare capture register B | GTCCRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2294h | GPT3 | General PWM timer compare capture register C | GTCCRC | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2296h | GPT3 | General PWM timer compare capture register D | GTCCRD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2298h | GPT3 | General PWM timer compare capture register E | GTCCRE | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 229Ah | GPT3 | General PWM timer compare capture register F | GTCCRF | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 229Ch | GPT3 | General PWM timer cycle setting register | GTPR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 229Eh | GPT3 | General PWM timer cycle setting buffer register | GTPBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A0h | GPT3 | General PWM timer cycle setting double-buffer register | GTPDBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A4h | GPT3 | A/D converter start request timing register A | GTADTRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A6h | GPT3 | A/D converter start request timing buffer register A | GTADTBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A8h | GPT3 | A/D converter start request timing double-buffer register A | GTADTDBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22ACh | GPT3 | A/D converter start request timing register B | GTADTRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22AEh | GPT3 | A/D converter start request timing buffer register B | GTADTBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22B0h | GPT3 | A/D converter start request timing double-buffer register B | GTADTDBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22B4h | GPT3 | General PWM timer output negate control register | GTONCR | 16 | 16, 32 | 3 to 5 ICLK*4 |

**Table 4.1 List of I/O Registers (Address Order) (24 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 22B6h | GPT3 | General PWM timer dead time control register | GTDTCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22B8h | GPT3 | General PWM timer dead time value register | GTDVU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22BAh | GPT3 | General PWM timer dead time value register | GTDVD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22BCh | GPT3 | General PWM timer dead time buffer register | GTDBU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22BEh | GPT3 | General PWM timer dead time buffer register | GTDBD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22C0h | GPT3 | General PWM timer output protection function status register | GTSOS | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22C2h | GPT3 | General PWM timer output protection temporary release register | GTSOTR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2300h | GPT0 | PWM output delay control register | GTDLYCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2302h | GPT1 | PWM output delay control register | GTDLYCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2304h | GPT2 | PWM output delay control register | GTDLYCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2306h | GPT3 | PWM output delay control register | GTDLYCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2318h | GPT0 | GTIOCA rising output delay register | GTDLYRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 231Ah | GPT0 | GTIOCB rising output delay register | GTDLYRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 231Ch | GPT1 | GTIOCA rising output delay register | GTDLYRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 231Eh | GPT1 | GTIOCB rising output delay register | GTDLYRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2320h | GPT2 | GTIOCA rising output delay register | GTDLYRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2322h | GPT2 | GTIOCB rising output delay register | GTDLYRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2324h | GPT3 | GTIOCA falling output delay register | GTDLYRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2326h | GPT3 | GTIOCB falling output delay register | GTDLYRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2328h | GPT0 | GTIOCA falling output delay register | GTDLYFA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 232Ah | GPT0 | GTIOCB falling output delay register | GTDLYFB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 232Ch | GPT1 | GTIOCA falling output delay register | GTDLYFA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 232Eh | GPT1 | GTIOCB falling output delay register | GTDLYFB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2330h | GPT2 | GTIOCA falling output delay register | GTDLYFA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2332h | GPT2 | GTIOCB falling output delay register | GTDLYFB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2334h | GPT3 | GTIOCA falling output delay register | GTDLYFA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2336h | GPT3 | GTIOCB falling output delay register | GTDLYFB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 007F C402h | FLASH | Flash mode register | FMODR | 8 | 8 | 2, 3 PCLK*3 |
| 007F C410h | FLASH | Flash access status register | FASTAT | 8 | 8 | 2, 3 PCLK*3 |
| 007F C411h | FLASH | Flash access error interrupt enable register | FAEINT | 8 | 8 | 2, 3 PCLK*3 |
| 007F C412h | FLASH | Flash ready interrupt enable register | FRDYIE | 8 | 8 | 2, 3 PCLK*3 |
| 007F C440h | FLASH | Data flash read enable register 0 | DFLRE0 | 16 | 16 | 2, 3 PCLK*3 |
| 007F C442h | FLASH | Data flash read enable register 1 | DFLRE1 | 16 | 16 | 2, 3 PCLK*3 |
| 007F C450h | FLASH | Data flash programming/erasure enable register 0 | DFLWE0 | 16 | 16 | 2, 3 PCLK*3 |
| 007F C452h | FLASH | Data flash programming/erasure enable register 1 | DFLWE1 | 16 | 16 | 2, 3 PCLK*3 |
| 007F C454h | FLASH | FCU RAM enable register | FCURAME | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFB0h | FLASH | Flash status register 0 | FSTATR0 | 8 | 8 | 2, 3 PCLK*3 |
| 007F FFB1h | FLASH | Flash status register 1 | FSTATR1 | 8 | 8 | 2, 3 PCLK*3 |
| 007F FFB2h | FLASH | Flash P/E mode entry register | FENTRYR | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFB4h | FLASH | Flash protect register | FPROTR | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFB6h | FLASH | Flash reset register | FRESETR | 16 | 16 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (25 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 007F FFBAh | FLASH | FCU command register | FCMDR | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFC8h | FLASH | FCU processing switching register | FCPSR | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFCAh | FLASH | Data flash blank check control register | DFLBCCNT | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFCCh | FLASH | Flash P/E status register | FPESTAT | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFCEh | FLASH | Data flash blank check status register | DFLBCSTAT | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFE8h | FLASH | Peripheral clock notification register | PCKAR | 16 | 16 | 2, 3 PCLK*3 |

Note 1. This register is not supported by the 100-pin LQFP version.
Note 2. This register is not supported by the product without the CAN function.
Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).
Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

## 4.2 I/O Register Bits

Register addresses and bit names of the peripheral modules are described below.
Each line cover eight bits, and 16-bit and 32-bit registers are shown as 2 or 4 lines, respectively.

**Table 4.2 List of I/O Registers (Bit Order) (1 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| SYSTEM | MDMONR | — | — | — | — | — | — | — | — |
| | | MDE | — | — | — | — | — | MD1 | MD0 |
| SYSTEM | MDSR | — | — | — | — | — | — | — | — |
| | | — | — | — | BOTS | — | — | — | IROM |
| SYSTEM | SYSCR0 | KEY[7:0] | | | | | | | |
| | | — | — | — | — | — | — | — | ROME |
| SYSTEM | SYSCR1 | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | RAME |
| SYSTEM | SBYCR | SSBY | — | — | | | STS[4:0] | | |
| | | — | — | — | — | — | — | — | — |
| SYSTEM | MSTPCRA | ACSE | — | — | MSTPA28 | — | — | — | MSTPA24 |
| | | MSTPA23 | — | — | — | — | — | MSTPA17 | MSTPA16 |
| | | MSTPA15 | MSTPA14 | — | — | — | — | MSTPA9 | — |
| | | MSTPA7 | — | — | — | — | — | — | — |
| SYSTEM | MSTPCRB | MSTPB31 | MSTPB30 | MSTPB29 | — | — | — | — | — |
| | | MSTPB23 | — | MSTPB21 | — | — | — | MSTPB17 | — |
| | | — | — | — | — | — | — | — | — |
| | | MSTPB7 | — | — | — | — | — | — | MSTPB0 |
| SYSTEM | MSTPCRC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | MSTPC0 |
| SYSTEM | SCKCR | — | — | — | — | | | ICK[3:0] | |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | | | PCK[3:0] | |
| | | — | — | — | — | — | — | — | — |
| SYSTEM | OSTDCR | KEY[7:0] | | | | | | | |
| | | OSTDE | OSTDF | — | — | — | — | — | — |
| BSC | BERCLR | — | — | — | — | — | — | — | STSCLR |
| BSC | BEREN | — | — | — | — | — | — | — | IGAEN |
| BSC | BERSR1 | — | | MST[2:0] | | — | — | — | IA |
| BSC | BERSR2 | ADDR[12:0] | | | | | | | |
| | | | | ADDR[12:0] | | | — | — | — |
| DTC | DTCCR | — | — | — | RRS | — | — | — | — |
| DTC | DTCVBR | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| DTC | DTCADMOD | — | — | — | — | — | — | — | SHORT |
| DTC | DTCST | — | — | — | — | — | — | — | DTCST |
| DTC | DTCSTS | ACT | — | — | — | — | — | — | — |
| | | | | | VECN[7:0] | | | | |
| MPU | RSPAGE0 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | RSPN[27:0] | | — | — | — | — |

**Table 4.2 List of I/O Registers (Bit Order) (2 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MPU | REPAGE0 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |
| MPU | RSPAGE1 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | RSPN[27:0] | | | — | — | — | — |
| MPU | REPAGE1 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |
| MPU | RSPAGE2 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | RSPN[27:0] | | | — | — | — | — |
| MPU | REPAGE2 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |
| MPU | RSPAGE3 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | RSPN[27:0] | | | — | — | — | — |
| MPU | REPAGE3 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |
| MPU | RSPAGE4 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | RSPN[27:0] | | | — | — | — | — |
| MPU | REPAGE4 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |
| MPU | RSPAGE5 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | RSPN[27:0] | | | — | — | — | — |
| MPU | REPAGE5 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |
| MPU | RSPAGE6 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | RSPN[27:0] | | | — | — | — | — |
| MPU | REPAGE6 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | REPN[27:0] | | | | UAC[2:0] | | V |

**Table 4.2 List of I/O Registers (Bit Order) (3 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MPU | RSPAGE7 | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | | RSPN[27:0] | | | | |
| | | | | RSPN[27:0] | | — | — | — | — |
| MPU | REPAGE7 | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | | REPN[27:0] | | | | |
| | | | | REPN[27:0] | | | UAC[2:0] | | V |
| MPU | MPEN | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | MPEN |
| MPU | MPBAC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | | UBAC[2:0] | | — |
| MPU | MPECLR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | CLR |
| MPU | MPESTS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DRW | DA | IA |
| MPU | MPDEA | | | | DEA[31:0] | | | | |
| | | | | | DEA[31:0] | | | | |
| | | | | | DEA[31:0] | | | | |
| | | | | | DEA[31:0] | | | | |
| MPU | MPSA | | | | SA[31:0] | | | | |
| | | | | | SA[31:0] | | | | |
| | | | | | SA[31:0] | | | | |
| | | | | | SA[31:0] | | | | |
| MPU | MPOPS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | S |
| MPU | MPOPI | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | INV |
| MPU | MHITI | — | — | — | — | — | — | — | — |
| | | | | | HITI[7:0] | | | | |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | | UHACI[2:0] | | — |
| MPU | MHITD | — | — | — | — | — | — | — | — |
| | | | | | HITD[7:0] | | | | |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | | UHACD[2:0] | | — |
| ICU | IR016 | — | — | — | — | — | — | — | IR |
| ICU | IR021 | — | — | — | — | — | — | — | IR |
| ICU | IR023 | — | — | — | — | — | — | — | IR |
| ICU | IR027 | — | — | — | — | — | — | — | IR |
| ICU | IR028 | — | — | — | — | — | — | — | IR |
| ICU | IR029 | — | — | — | — | — | — | — | IR |
| ICU | IR030 | — | — | — | — | — | — | — | IR |
| ICU | IR031 | — | — | — | — | — | — | — | IR |

**Table 4.2 List of I/O Registers (Bit Order) (4 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | IR044 | — | — | — | — | — | — | — | IR |
| ICU | IR045 | — | — | — | — | — | — | — | IR |
| ICU | IR046 | — | — | — | — | — | — | — | IR |
| ICU | IR047 | — | — | — | — | — | — | — | IR |
| ICU | IR056 | — | — | — | — | — | — | — | IR |
| ICU | IR057 | — | — | — | — | — | — | — | IR |
| ICU | IR058 | — | — | — | — | — | — | — | IR |
| ICU | IR059 | — | — | — | — | — | — | — | IR |
| ICU | IR060 | — | — | — | — | — | — | — | IR |
| ICU | IR064 | — | — | — | — | — | — | — | IR |
| ICU | IR065 | — | — | — | — | — | — | — | IR |
| ICU | IR066 | — | — | — | — | — | — | — | IR |
| ICU | IR067 | — | — | — | — | — | — | — | IR |
| ICU | IR068 | — | — | — | — | — | — | — | IR |
| ICU | IR069 | — | — | — | — | — | — | — | IR |
| ICU | IR070 | — | — | — | — | — | — | — | IR |
| ICU | IR071 | — | — | — | — | — | — | — | IR |
| ICU | IR096 | — | — | — | — | — | — | — | IR |
| ICU | IR098 | — | — | — | — | — | — | — | IR |
| ICU | IR102 | — | — | — | — | — | — | — | IR |
| ICU | IR103 | — | — | — | — | — | — | — | IR |
| ICU | IR106 | — | — | — | — | — | — | — | IR |
| ICU | IR114 | — | — | — | — | — | — | — | IR |
| ICU | IR115 | — | — | — | — | — | — | — | IR |
| ICU | IR116 | — | — | — | — | — | — | — | IR |
| ICU | IR117 | — | — | — | — | — | — | — | IR |
| ICU | IR118 | — | — | — | — | — | — | — | IR |
| ICU | IR119 | — | — | — | — | — | — | — | IR |
| ICU | IR120 | — | — | — | — | — | — | — | IR |
| ICU | IR121 | — | — | — | — | — | — | — | IR |
| ICU | IR122 | — | — | — | — | — | — | — | IR |
| ICU | IR123 | — | — | — | — | — | — | — | IR |
| ICU | IR124 | — | — | — | — | — | — | — | IR |
| ICU | IR125 | — | — | — | — | — | — | — | IR |
| ICU | IR126 | — | — | — | — | — | — | — | IR |
| ICU | IR127 | — | — | — | — | — | — | — | IR |
| ICU | IR128 | — | — | — | — | — | — | — | IR |
| ICU | IR129 | — | — | — | — | — | — | — | IR |
| ICU | IR130 | — | — | — | — | — | — | — | IR |
| ICU | IR131 | — | — | — | — | — | — | — | IR |
| ICU | IR132 | — | — | — | — | — | — | — | IR |
| ICU | IR133 | — | — | — | — | — | — | — | IR |
| ICU | IR134 | — | — | — | — | — | — | — | IR |
| ICU | IR135 | — | — | — | — | — | — | — | IR |
| ICU | IR136 | — | — | — | — | — | — | — | IR |
| ICU | IR137 | — | — | — | — | — | — | — | IR |
| ICU | IR138 | — | — | — | — | — | — | — | IR |
| ICU | IR139 | — | — | — | — | — | — | — | IR |
| ICU | IR140 | — | — | — | — | — | — | — | IR |
| ICU | IR141 | — | — | — | — | — | — | — | IR |
| ICU | IR142 | — | — | — | — | — | — | — | IR |
| ICU | IR143 | — | — | — | — | — | — | — | IR |

**Table 4.2 List of I/O Registers (Bit Order) (5 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | IR144 | — | — | — | — | — | — | — | IR |
| ICU | IR145 | — | — | — | — | — | — | — | IR |
| ICU | IR146 | — | — | — | — | — | — | — | IR |
| ICU | IR149 | — | — | — | — | — | — | — | IR |
| ICU | IR150 | — | — | — | — | — | — | — | IR |
| ICU | IR151 | — | — | — | — | — | — | — | IR |
| ICU | IR152 | — | — | — | — | — | — | — | IR |
| ICU | IR153 | — | — | — | — | — | — | — | IR |
| ICU | IR170 | — | — | — | — | — | — | — | IR |
| ICU | IR171 | — | — | — | — | — | — | — | IR |
| ICU | IR172 | — | — | — | — | — | — | — | IR |
| ICU | IR173 | — | — | — | — | — | — | — | IR |
| ICU | IR174 | — | — | — | — | — | — | — | IR |
| ICU | IR175 | — | — | — | — | — | — | — | IR |
| ICU | IR176 | — | — | — | — | — | — | — | IR |
| ICU | IR177 | — | — | — | — | — | — | — | IR |
| ICU | IR178 | — | — | — | — | — | — | — | IR |
| ICU | IR179 | — | — | — | — | — | — | — | IR |
| ICU | IR180 | — | — | — | — | — | — | — | IR |
| ICU | IR181 | — | — | — | — | — | — | — | IR |
| ICU | IR182 | — | — | — | — | — | — | — | IR |
| ICU | IR183 | — | — | — | — | — | — | — | IR |
| ICU | IR184 | — | — | — | — | — | — | — | IR |
| ICU | IR186 | — | — | — | — | — | — | — | IR |
| ICU | IR187 | — | — | — | — | — | — | — | IR |
| ICU | IR188 | — | — | — | — | — | — | — | IR |
| ICU | IR189 | — | — | — | — | — | — | — | IR |
| ICU | IR190 | — | — | — | — | — | — | — | IR |
| ICU | IR192 | — | — | — | — | — | — | — | IR |
| ICU | IR193 | — | — | — | — | — | — | — | IR |
| ICU | IR194 | — | — | — | — | — | — | — | IR |
| ICU | IR195 | — | — | — | — | — | — | — | IR |
| ICU | IR196 | — | — | — | — | — | — | — | IR |
| ICU | IR214 | — | — | — | — | — | — | — | IR |
| ICU | IR215 | — | — | — | — | — | — | — | IR |
| ICU | IR216 | — | — | — | — | — | — | — | IR |
| ICU | IR217 | — | — | — | — | — | — | — | IR |
| ICU | IR218 | — | — | — | — | — | — | — | IR |
| ICU | IR219 | — | — | — | — | — | — | — | IR |
| ICU | IR220 | — | — | — | — | — | — | — | IR |
| ICU | IR221 | — | — | — | — | — | — | — | IR |
| ICU | IR222 | — | — | — | — | — | — | — | IR |
| ICU | IR223 | — | — | — | — | — | — | — | IR |
| ICU | IR224 | — | — | — | — | — | — | — | IR |
| ICU | IR225 | — | — | — | — | — | — | — | IR |
| ICU | IR246 | — | — | — | — | — | — | — | IR |
| ICU | IR247 | — | — | — | — | — | — | — | IR |
| ICU | IR248 | — | — | — | — | — | — | — | IR |
| ICU | IR249 | — | — | — | — | — | — | — | IR |
| ICU | IR254 | — | — | — | — | — | — | — | IR |
| ICU | DTCER027 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER028 | — | — | — | — | — | — | — | DTCE |

**Table 4.2 List of I/O Registers (Bit Order) (6 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | DTCER029 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER030 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER031 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER045 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER046 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER064 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER065 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER066 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER067 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER068 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER069 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER070 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER071 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER098 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER102 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER103 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER106 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER114 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER115 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER116 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER117 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER121 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER122 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER125 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER126 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER129 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER130 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER131 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER132 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER134 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER135 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER136 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER137 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER138 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER139 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER140 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER141 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER142 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER143 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER144 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER145 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER149 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER150 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER151 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER152 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER153 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER174 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER175 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER176 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER177 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER178 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER179 | — | — | — | — | — | — | — | DTCE |

**Table 4.2 List of I/O Registers (Bit Order) (7 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | DTCER180 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER181 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER182 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER183 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER184 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER186 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER187 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER188 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER189 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER190 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER192 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER193 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER194 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER195 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER196 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER215 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER216 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER219 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER220 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER223 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER224 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER247 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER248 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER254 | — | — | — | — | — | — | — | DTCE |
| ICU | IER02 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER03 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER05 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER07 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER08 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER0C | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER0D | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER0E | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER0F | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER10 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER11 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER12 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER13 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER15 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER16 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER17 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER18 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER1A | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER1B | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER1C | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER1E | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | IER1F | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 | IEN0 |
| ICU | SWINTR | — | — | — | — | — | — | — | SWINT |
| ICU | FIR | FIEN | — | — | — | — | — | — | — |
| | | FVCT[7:0] | | | | | | | |
| ICU | IPR00 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR01 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR02 | — | — | — | — | IPR[3:0] | | | |

**Table 4.2 List of I/O Registers (Bit Order) (8 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | IPR03 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR04 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR05 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR06 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR07 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR14 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR18 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR20 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR21 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR22 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR23 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR24 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR25 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR26 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR27 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR40 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR44 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR48 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR49 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR51 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR52 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR53 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR54 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR55 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR56 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR57 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR58 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR59 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR5A | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR5B | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR5C | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR5D | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR5E | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR5F | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR60 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR67 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR68 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR69 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR6A | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR6B | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR6C | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR6D | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR6E | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR6F | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR80 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR81 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR82 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR88 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR89 | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR8A | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR8B | — | — | — | — | IPR[3:0] | | | |
| ICU | IPR90 | — | — | — | — | IPR[3:0] | | | |

**Table 4.2 List of I/O Registers (Bit Order) (9 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | IRQCR0 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR1 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR2 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR3 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR4 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR5 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR6 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | IRQCR7 | — | — | — | — | IRQMD[1:0] | | — | — |
| ICU | NMISR | — | — | — | — | — | OSTST | LVDST | NMIST |
| ICU | NMIER | — | — | — | — | — | OSTEN | LVDEN | NMIEN |
| ICU | NMICLR | — | — | — | — | — | OSTCLR | — | NMICLR |
| ICU | NMICR | — | — | — | — | NMIMD | — | — | — |
| CMT | CMSTR0 | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | STR1 | STR0 |
| CMT0 | CMCR | — | — | — | — | — | — | — | — |
| | | — | CMIE | — | — | — | — | CKS[1:0] | |
| CMT0 | CMCNT | | | | | | | | |
| CMT0 | CMCOR | | | | | | | | |
| CMT1 | CMCR | — | — | — | — | — | — | — | — |
| | | — | CMIE | — | — | — | — | CKS[1:0] | |
| CMT1 | CMCNT | | | | | | | | |
| CMT1 | CMCOR | | | | | | | | |
| CMT | CMSTR1 | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | STR3 | STR2 |
| CMT2 | CMCR | — | — | — | — | — | — | — | — |
| | | — | CMIE | — | — | — | — | CKS[1:0] | |
| CMT2 | CMCNT | | | | | | | | |
| CMT2 | CMCOR | | | | | | | | |
| CMT3 | CMCR | — | — | — | — | — | — | — | — |
| | | — | CMIE | — | — | — | — | CKS[1:0] | |
| CMT3 | CMCNT | | | | | | | | |
| CMT3 | CMCOR | | | | | | | | |
| WDT | TCSR | — | TMS | TME | — | — | | CKS[2:0] | |
| WDT | WINA | | | | | | | | |
| WDT | TCNT | | | | | | | | |
| WDT | WINB | | | | | | | | |
| WDT | RSTCSR | WOVF | RSTE | — | — | — | — | — | — |
| IWDT | IWDTCR | — | — | — | — | — | — | — | — |
| | | | CKS[3:0] | | | — | — | TOPS[1:0] | |
| IWDT | IWDTSR | — | UNDFF | | | CNTVAL[13:0] | | | |
| | | | | | CNTVAL[13:0] | | | | |
| AD0 | ADDRA*1 | — | — | — | — | — | — | | |

**Table 4.2 List of I/O Registers (Bit Order) (10 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| AD0 | ADDRB*1 | — | — | — | — | — | — | | |
| AD0 | ADDRC*1 | — | — | — | — | — | — | | |
| AD0 | ADDRD*1 | — | — | — | — | — | — | | |
| AD0 | ADDRE*1 | — | — | — | — | — | — | | |
| AD0 | ADDRF*1 | — | — | — | — | — | — | | |
| AD0 | ADDRG*1 | — | — | — | — | — | — | | |
| AD0 | ADDRH*1 | — | — | — | — | — | — | | |
| AD0 | ADCSR | — | ADIE | ADST | — | | CH[3:0] | | |
| AD0 | ADCR | — | — | — | — | CKS[1:0] | | MODE[1:0] | |
| AD0 | ADSSTR | | | | | | | | |
| AD0 | ADDIAGR | — | — | — | — | — | — | DIAG[1:0] | |
| AD0 | ADDRI*1 | — | — | — | — | — | — | | |
| AD0 | ADDRJ*1 | — | — | — | — | — | — | | |
| AD0 | ADDRK *1 | — | — | — | — | — | — | | |
| AD0 | ADDRL*1 | — | — | — | — | — | — | | |
| AD0 | ADSTRGR | — | — | — | | | ADSTRS[4:0] | | |
| AD0 | ADDPR | DPSEL | — | — | — | — | — | — | DPPRC |
| SCI0 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI0 | BRR | | | | | | | | |
| SCI0 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI0 | TDR | | | | | | | | |
| SCI0 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI0 | RDR | | | | | | | | |
| SCI0 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI0 | SEMR | — | — | NFEN | ABCS | — | — | — | — |
| SMCI0 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI0 | BRR | | | | | | | | |
| SMCI0 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI0 | TDR | | | | | | | | |
| SMCI0 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI0 | RDR | | | | | | | | |
| SMCI0 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI1 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI1 | BRR | | | | | | | | |
| SCI1 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI1 | TDR | | | | | | | | |
| SCI1 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI1 | RDR | | | | | | | | |
| SCI1 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |

**Table 4.2 List of I/O Registers (Bit Order) (11 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| SCI1 | SEMR | — | — | NFEN | ABCS | — | — | — | — |
| SMCI1 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI1 | BRR | | | | | | | | |
| SMCI1 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI1 | TDR | | | | | | | | |
| SMCI1 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI1 | RDR | | | | | | | | |
| SMCI1 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI2 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI2 | BRR | | | | | | | | |
| SCI2 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI2 | TDR | | | | | | | | |
| SCI2 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI2 | RDR | | | | | | | | |
| SCI2 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SMCI2 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI2 | BRR | | | | | | | | |
| SMCI2 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI2 | TDR | | | | | | | | |
| SMCI2 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI2 | RDR | | | | | | | | |
| SMCI2 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| CRC | CRCCR | DORCLR | — | — | — | — | LMS | GPS[1:0] | |
| CRC | CRCDIR | | | | | | | | |
| CRC | CRCDOR | | | | | | | | |
| RIIC0 | ICCR1 | ICE | IICRST | CLO | SOWP | SCLO | SDAO | SCLI | SDAI |
| RIIC0 | ICCR2 | BBSY | MST | TRS | — | SP | RS | ST | — |
| RIIC0 | ICMR1 | MTWP | | CKS[2:0] | | BCWP | | BC[2:0] | |
| RIIC0 | ICMR2 | DLCS | | SDDL[2:0] | | TMWE | TMOH | TMOL | TMOS |
| RIIC0 | ICMR3 | SMBS | WAIT | RDRFS | ACKWP | ACKBT | ACKBR | NF[1:0] | |
| RIIC0 | ICFER | — | SCLE | NFE | NACKE | SALE | NALE | MALE | TMOE |
| RIIC0 | ICSER | HOAE | — | DIDE | — | GCAE | SAR2E | SAR1E | SAR0E |
| RIIC0 | ICIER | TIE | TEIE | RIE | NAKIE | SPIE | STIE | ALIE | TMOIE |
| RIIC0 | ICSR1 | HOA | — | DID | — | GCA | AAS2 | AAS1 | AAS0 |
| RIIC0 | ICSR2 | TDRE | TEND | RDRF | NACKF | STOP | START | AL | TMOF |
| RIIC0 | SARL0 | | | | SVA[6:0] | | | | SVA0 |
| RIIC0 | TMOCNTL | | | | | | | | |
| RIIC0 | SARU0 | — | — | — | — | — | | SVA[1:0] | FS |
| RIIC0 | TMOCNTU | | | | | | | | |
| RIIC0 | SARL1 | | | | SVA[6:0] | | | | SVA0 |
| RIIC0 | SARU1 | — | — | — | — | — | | SVA[1:0] | FS |
| RIIC0 | SARL2 | | | | SVA[6:0] | | | | SVA0 |
| RIIC0 | SARU2 | — | — | — | — | — | | SVA[1:0] | FS |
| RIIC0 | ICBRL | — | — | — | | | BRL[4:0] | | |
| RIIC0 | ICBRH | — | — | — | | | BRH[4:0] | | |
| RIIC0 | ICDRT | | | | | | | | |
| RIIC0 | ICDRR | | | | | | | | |
| RSPI0 | SPCR | SPRIE | SPE | SPTIE | SPEIE | MSTR | MODFEN | TXMD | SPMS |

**Table 4.2 List of I/O Registers (Bit Order) (12 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| RSPI0 | SSLP | — | — | — | — | SSLP3 | SSLP2 | SSLP1 | SSLP0 |
| RSPI0 | SPPCR | — | — | MOIFE | MOIFV | — | — | SPLP2 | SPLP |
| RSPI0 | SPSR | SPRF | — | SPTEF | — | PERF | MODF | IDLNF | OVRF |
| RSPI0 | SPDR | H[15:0] | | | | | | | |
| | | H[15:0] | | | | | | | |
| | | L[15:0] | | | | | | | |
| | | L[15:0] | | | | | | | |
| RSPI0 | SPSCR | — | — | — | — | — | | SPSLN[2:0] | |
| RSPI0 | SPSSR | — | | SPECM[2:0] | | — | | SPCP[2:0] | |
| RSPI0 | SPBR | SPR7 | SPR6 | SPR5 | SPR4 | SPR3 | SPR2 | SPR1 | SPR0 |
| RSPI0 | SPDCR | — | — | SPLW | SPRDTD | SLSEL[1:0] | | SPFC[1:0] | |
| RSPI0 | SPCKD | — | — | — | — | — | | SCKDL[2:0] | |
| RSPI0 | SSLND | — | — | — | — | — | | SLNDL[2:0] | |
| RSPI0 | SPND | — | — | — | — | — | | SPNDL[2:0] | |
| RSPI0 | SPCR2 | — | — | — | — | PTE | SPIIE | SPOE | SPPE |
| RSPI0 | SPCMD0 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD1 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD2 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD3 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD4 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD5 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD6 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD7 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| S12AD0 | ADCSR | ADST | ADCS[1:0] | | ADIE | CKS[1:0] | | TRGE | EXTRG |
| S12AD0 | ADANS | — | — | CH[1:0] | | — | PG002SEL | PG001SEL | PG000SEL |
| | | — | — | — | — | — | PG002EN | PG001EN | PG000EN |
| S12AD0 | ADPG | — | — | — | — | PG002GAIN[3:0] | | | |
| | | PG001GAIN[3:0] | | | | PG000GAIN[3:0] | | | |
| S12AD0 | ADCER | ADRFMT | — | ADIEW | ADIE2 | DIAGM | DIAGLD | DIAGVAL[1:0] | |
| | | — | — | ACE | — | — | ADPRC[1:0] | | SHBYP |
| S12AD0 | ADSTRGR | — | — | — | ADSTRS1[4:0] | | | | |
| | | — | — | — | ADSTRS0[4:0] | | | | |
| S12AD | ADCMPMD0 | — | — | CEN102[1:0] | | CEN101[1:0] | | CEN100[1:0] | |
| | | — | — | CEN002[1:0] | | CEN001[1:0] | | CEN000[1:0] | |
| S12AD | ADCMPMD1 | — | VSELL1 | VSELH1 | CSEL1 | — | VSELL0 | VSELH0 | CSEL0 |
| | | — | | REFH[2:0] | | — | | REFL[2:0] | |
| S12AD | ADCMPNR0 | — | — | — | — | C002NR[3:0] | | | |
| | | C001NR[3:0] | | | | C000NR[3:0] | | | |
| S12AD | ADCMPNR1 | — | — | — | — | C102NR[3:0] | | | |
| | | C101NR[3:0] | | | | C100NR[3:0] | | | |
| S12AD | ADCMPFR | — | — | C102FLAG | C101FLAG | C100FLAG | C002FLAG | C001FLAG | C000FLAG |
| S12AD | ADCMPSEL | — | — | — | — | — | — | POERQ | IE |
| | | — | — | SEL102 | SEL101 | SEL100 | SEL002 | SEL001 | SEL000 |

**Table 4.2 List of I/O Registers (Bit Order) (13 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| S12AD0 | ADRD*2 | DIAGST[1:0] | | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR0A*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR1*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR2*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR3*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR0B*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADSSTR | | | | | | | | |
| S12AD1 | ADCSR | ADST | ADCS[1:0] | | ADIE | CKS[1:0] | | TRGE | EXTRG |
| S12AD1 | ADANS | — | — | CH[1:0] | | — | PG102SEL | PG101SEL | PG100SEL |
| | | — | — | — | — | — | PG102EN | PG101EN | PG100EN |
| S12AD1 | ADPG | — | — | — | — | PG102GAIN[3:0] | | | |
| | | PG101GAIN[3:0] | | | | PG100GAIN[3:0] | | | |
| S12AD1 | ADCER | ADRFMT | — | ADIEW | ADIE2 | DIAGM | DIAGLD | DIAGVAL[1:0] | |
| | | — | — | ACE | — | — | ADPRC[1:0] | | SHBYP |
| S12AD1 | ADSTRGR | — | — | — | ADSTRS1[4:0] | | | | |
| | | — | — | — | ADSTRS0[4:0] | | | | |
| S12AD1 | ADRD*2 | DIAGST[1:0] | | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR0A*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR1*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR2*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR3*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR0B*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADSSTR | | | | | | | | |
| PORT1 | DDR | — | — | — | — | — | — | B1 | B0 |
| PORT2 | DDR | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | DDR | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT7 | DDR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT8 | DDR | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | DDR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | DDR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | DDR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | DDR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | DDR | — | — | B5 | B4 | B3 | — | B1 | B0 |
| PORTG | DDR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT1 | DR | — | — | — | — | — | — | B1 | B0 |
| PORT2 | DR | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | DR | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT7 | DR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

**Table 4.2 List of I/O Registers (Bit Order) (14 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| PORT8 | DR | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | DR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | DR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | DR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | DR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | DR | — | — | B5 | B4 | B3 | — | B1 | B0 |
| PORTG | DR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT1 | PORT | — | — | — | — | — | — | B1 | B0 |
| PORT2 | PORT | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | PORT | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT4 | PORT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT5 | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT6 | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT7 | PORT | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT8 | PORT | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | PORT | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | PORT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | PORT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTG | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT1 | ICR | — | — | — | — | — | — | B1 | B0 |
| PORT2 | ICR | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | ICR | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT4 | ICR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT5 | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT6 | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT7 | ICR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT8 | ICR | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | ICR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | ICR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | ICR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | ICR | — | — | B5 | B4 | B3 | — | B1 | B0 |
| PORTG | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| IOPORT | PF8IRQ | — | — | — | — | ITS1[1:0] | | ITS0[1:0] | |
| IOPORT | PF9IRQ | — | — | — | — | — | ITS2 | — | — |
| IOPORT | PFAADC | — | — | — | — | — | — | ADTRG1S | ADTRG0S |
| IOPORT | PFCMTU | TCLKS[1:0] | | — | — | — | — | MTUS1 | MTUS0 |
| IOPORT | PFDGPT | — | — | — | — | — | — | — | GPTS |
| IOPORT | PFFSCI | — | — | — | — | — | SCI2S | — | — |
| IOPORT | PFGSPI | SSL3E | SSL2E | SSL1E | SSL0E | MISOE | MOSIE | RSPCKE | — |
| IOPORT | PFHSPI | — | — | — | — | — | — | RSPIS[1:0] | |
| IOPORT | PFJCAN | CANS[1:0] | | — | — | — | — | — | CANE |
| IOPORT | PFKLIN | — | — | — | — | — | — | — | LINE |
| IOPORT | PFMPOE | — | — | — | POE11E | POE10E | POE8E | POE4E | POE0E |
| IOPORT | PFNPOE | POE10S | — | — | — | — | — | — | — |
| SYSTEM | DPSBYCR | DPSBY | IOKEEP | — | — | — | — | — | — |
| SYSTEM | DPSWCR | — | — | WTSTS[5:0] | | | | | |
| SYSTEM | DPSIER | DNMIE | — | — | DLVDE | — | — | DIRQ1E | DIRQ0E |

**Table 4.2 List of I/O Registers (Bit Order) (15 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| SYSTEM | DPSIFR | DNMIF | — | — | DLVDF | — | — | DIRQ1F | DIRQ0F |
| SYSTEM | DPSIEGR | DNMIEG | — | — | — | — | — | DIRQ1EG | DIRQ0EG |
| SYSTEM | RSTSR | DPSRSTF | — | — | — | — | LVD2F | LVD1F | PORF |
| FLASH | FWEPROR | — | — | — | — | — | — | FLWE[1:0] | |
| SYSTEM | LVDKEYR | KEY[7:0] | | | | | | | |
| SYSTEM | LVDCR | LVD2E | LVD2RI | — | — | LVD1E | LVD1RI | — | — |
| SYSTEM | DPSBKR0 | | | | | | | | |
| SYSTEM | DPSBKR1 | | | | | | | | |
| SYSTEM | DPSBKR2 | | | | | | | | |
| SYSTEM | DPSBKR3 | | | | | | | | |
| SYSTEM | DPSBKR4 | | | | | | | | |
| SYSTEM | DPSBKR5 | | | | | | | | |
| SYSTEM | DPSBKR6 | | | | | | | | |
| SYSTEM | DPSBKR7 | | | | | | | | |
| SYSTEM | DPSBKR8 | | | | | | | | |
| SYSTEM | DPSBKR9 | | | | | | | | |
| SYSTEM | DPSBKR10 | | | | | | | | |
| SYSTEM | DPSBKR11 | | | | | | | | |
| SYSTEM | DPSBKR12 | | | | | | | | |
| SYSTEM | DPSBKR13 | | | | | | | | |
| SYSTEM | DPSBKR14 | | | | | | | | |
| SYSTEM | DPSBKR15 | | | | | | | | |
| SYSTEM | DPSBKR16 | | | | | | | | |
| SYSTEM | DPSBKR17 | | | | | | | | |
| SYSTEM | DPSBKR18 | | | | | | | | |
| SYSTEM | DPSBKR19 | | | | | | | | |
| SYSTEM | DPSBKR20 | | | | | | | | |
| SYSTEM | DPSBKR21 | | | | | | | | |
| SYSTEM | DPSBKR22 | | | | | | | | |
| SYSTEM | DPSBKR23 | | | | | | | | |
| SYSTEM | DPSBKR24 | | | | | | | | |
| SYSTEM | DPSBKR25 | | | | | | | | |
| SYSTEM | DPSBKR26 | | | | | | | | |
| SYSTEM | DPSBKR27 | | | | | | | | |
| SYSTEM | DPSBKR28 | | | | | | | | |
| SYSTEM | DPSBKR29 | | | | | | | | |
| SYSTEM | DPSBKR30 | | | | | | | | |
| SYSTEM | DPSBKR31 | | | | | | | | |
| POE | ICSR1 | — | — | — | POE0F | — | — | — | PIE1 |
| | | — | — | — | — | — | — | POE0M[1:0] | |
| POE | OCSR1 | OSF1 | — | — | — | — | — | OCE1 | OIE1 |
| | | — | — | — | — | — | — | — | — |
| POE | ICSR2 | — | — | — | POE4F | — | — | — | PIE2 |
| | | — | — | — | — | — | — | POE4M[1:0] | |
| POE | OCSR2 | OSF2 | — | — | — | — | — | OCE2 | OIE2 |
| | | — | — | — | — | — | — | — | — |
| POE | ICSR3 | — | — | — | POE8F | — | — | POE8E | PIE3 |
| | | — | — | — | — | — | — | POE8M[1:0] | |
| POE | SPOER | — | — | — | GPT23HIZ | GPT01HIZ | MTUCH0HIZ | MTUCH67HIZ | MTUCH34HIZ |
| POE | POECR1 | — | — | — | — | MTU0DZE | MTU0CZE | MTU0BZE | MTU0AZE |

**Table 4.2 List of I/O Registers (Bit Order) (16 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| POE | POECR2 | — | — | — | — | — | MTU3BDZE | MTU4ACZE | MTU4BDZE |
| | | — | — | — | — | — | MTU6BDZE | MTU7ACZE | MTU7BDZE |
| POE | POECR3 | — | — | — | — | — | — | GPT3ABZE | GPT2ABZE |
| | | — | — | — | — | — | — | GPT1ABZE | GPT0ABZE |
| POE | POECR4 | — | — | IC5ADDMT67ZE | IC4ADDMT67ZE | IC3ADDMT67ZE | — | IC1ADDMT67ZE | CMADDMT67ZE |
| | | — | — | IC5ADDMT34ZE | IC4ADDMT34ZE | IC3ADDMT34ZE | IC2ADDMT34ZE | — | CMADDMT34ZE |
| POE | POECR5 | — | — | — | — | — | — | — | — |
| | | — | — | IC5ADDMT0ZE | IC4ADDMT0ZE | — | IC2ADDMT0ZE | IC1ADDMT0ZE | CMADDMT0ZE |
| POE | POECR6 | — | — | — | IC4ADDGPT23ZE | IC3ADDGPT23ZE | IC2ADDGPT23ZE | IC1ADDGPT23ZE | CMADDGPT23ZE |
| | | — | — | IC5ADDGPT01ZE | — | IC3ADDGPT01ZE | IC2ADDGPT01ZE | IC1ADDGPT01ZE | CMADDGPT01ZE |
| POE | ICSR4 | — | — | — | POE10F | — | — | POE10E | PIE4 |
| | | — | — | — | — | — | — | POE10M[1:0] | |
| POE | ALR1 | — | — | — | — | — | — | — | — |
| | | OLSEN | — | OLSG2B | OLSG2A | OLSG1B | OLSG1A | OLSG0B | OLSG0A |
| POE | ICSR5 | — | — | — | POE11F | — | — | POE11E | PIE5 |
| | | — | — | — | — | — | — | POE11M[1:0] | |
| CAN0*3 | MB.ID | IDE | RTR | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17:0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| | MB.DLC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | | DLC[3:0] | | |
| | MB.DATA 0 to 7 | | | | | | | | |
| | MB.TS | | | | TSH[7:0] | | | | |
| | | | | | TSL[7:0] | | | | |
| CAN0*3 | MKR0 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKR1 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKR2 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKR3 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKR4 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (17 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| CAN0*3 | MKR5 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKR6 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKR7 | — | — | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17 0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | FIDCR0 | IDE | RTR | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17:0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | FIDCR1 | IDE | RTR | — | | | SID[10:0] | | |
| | | | | SID[10:0] | | | | EID[17:0] | |
| | | | | | EID[17:0] | | | | |
| | | | | | EID[17:0] | | | | |
| CAN0*3 | MKIVLR | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| CAN0*3 | MIER | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| CAN0*3 | MCTL.TX | TRMREQ | RECREQ | — | ONESHOT | — | TRMABT | TRMACTIVE | SENTDATA |
| | MCTL.RX | TRMREQ | RECREQ | — | ONESHOT | — | MSGLOST | INVALDATA | NEWDATA |
| CAN0*3 | CTLR | — | — | RBOC | BOM[1:0] | | SLPM | CANM[1:0] | |
| | | TSPS[1:0] | | TSRC | TPM | MLM | IDFM[1:0] | | MBM |
| CAN0*3 | STR | — | RECST | TRMST | BOST | EPST | SLPST | HLTST | RSTST |
| | | EST | TABST | FMLST | NMLST | TFST | RFST | SDST | NDST |
| CAN0*3 | BCR | | TSEG1[3:0] | | | — | — | BRP[9:0] | |
| | | | | | BRP[9:0] | | | | |
| | | — | — | SJW[1:0] | | — | | TSEG2[2:0] | |
| | | — | — | — | — | — | — | — | — |
| CAN0*3 | RFCR | RFEST | RFWST | RFFST | RFMLF | | RFUST[2:0] | | RFE |
| CAN0*3 | RFPCR | — | — | — | — | — | — | — | — |
| CAN0*3 | TFCR | TFEST | TFFST | — | — | | TFUST[2:0] | | TFE |
| CAN0*3 | TFPCR | — | — | — | — | — | — | — | — |
| CAN0*3 | EIER | BLIE | OLIE | ORIE | BORIE | BOEIE | EPIE | EWIE | BEIE |
| CAN0*3 | EIFR | BLIF | OLIF | ORIF | BORIF | BOEIF | EPIF | EWIF | BEIF |
| CAN0*3 | RECR | — | — | — | — | — | — | — | — |
| CAN0*3 | TECR | — | — | — | — | — | — | — | — |
| CAN0*3 | ECSR | EDPM | ADEF | BE0F | BE1F | CEF | AEF | FEF | SEF |
| CAN0*3 | CSSR | — | — | — | — | — | — | — | — |
| CAN0*3 | MSSR | SEST | — | — | | | MBNST[4:0] | | |
| CAN0*3 | MSMR | — | — | — | — | — | — | MBSM[1:0] | |
| CAN0*3 | TSR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |

**Table 4.2 List of I/O Registers (Bit Order) (18 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| CAN0*3 | AFSR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| CAN0*3 | TCR | — | — | — | — | — | TSTM[1:0] | | TSTE |
| LIN0 | LWBR | — | — | — | — | — | — | — | LWBR0 |
| LIN0 | LBRP0 | | | | | | | | |
| LIN0 | LBRP1 | | | | | | | | |
| LIN0 | LSTC | | | | | | | | LSTM |
| LIN0 | L0MD | — | — | — | — | LCKS[1:0] | | — | — |
| LIN0 | L0BRK | — | — | BDT[1:0] | | | BLT[3:0] | | |
| LIN0 | L0SPC | — | — | IBS[1:0] | | — | | IBSH[2:0] | |
| LIN0 | L0WUP | | WUTL[3:0] | | | — | — | — | — |
| LIN0 | L0IE | — | — | — | — | — | ERRIE | FRCIE | FTCIE |
| LIN0 | L0EDE | — | — | — | — | FERE | FTERE | PBERE | BERE |
| LIN0 | L0C | — | — | — | — | — | — | OM1 | OM0 |
| LIN0 | L0TC | — | — | — | — | — | — | RTS | FTS |
| LIN0 | L0MST | — | — | — | — | — | — | OMM1 | OMM0 |
| LIN0 | L0ST | HTRC | D1RC | — | — | ERR | — | FRC | FTC |
| LIN0 | L0EST | — | — | CSER | — | FER | FTER | PBER | BER |
| LIN0 | L0RFC | — | FSM | CSM | RFT | | RFDL[3:0] | | |
| LIN0 | L0IDB | IDP | | | | ID | | | |
| LIN0 | L0CBR | | | | | | | | |
| LIN0 | L0DB1 | | | | | | | | |
| LIN0 | L0DB2 | | | | | | | | |
| LIN0 | L0DB3 | | | | | | | | |
| LIN0 | L0DB4 | | | | | | | | |
| LIN0 | L0DB5 | | | | | | | | |
| LIN0 | L0DB6 | | | | | | | | |
| LIN0 | L0DB7 | | | | | | | | |
| LIN0 | L0DB8 | | | | | | | | |
| MTU3 | TCR | | CCLR[2:0] | | | CKEG[1:0] | | TPSC[2:0] | |
| MTU4 | TCR | | CCLR[2:0] | | | CKEG[1:0] | | TPSC[2:0] | |
| MTU3 | TMDR1 | — | — | BFB | BFA | | | MD[3:0] | |
| MTU4 | TMDR1 | — | — | BFB | BFA | | | MD[3:0] | |
| MTU3 | TIORH | | IOB[3:0] | | | | | IOA[3:0] | |
| MTU3 | TIORL | | IOD[3:0] | | | | | IOC[3:0] | |
| MTU4 | TIORH | | IOB[3:0] | | | | | IOA[3:0] | |
| MTU4 | TIORL | | IOD[3:0] | | | | | IOC[3:0] | |
| MTU3 | TIER | TTGE | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU4 | TIER | TTGE | TTGE2 | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU | TOERA | — | — | OE4D | OE4C | OE3D | OE4B | OE4A | OE3B |
| MTU | TGCRA | — | BDC | N | P | FB | WF | VF | UF |
| MTU | TOCR1A | — | PSYE | — | — | TOCL | TOCS | OLSN | OLSP |
| MTU | TOCR2A | BF[1:0] | | OLS3N | OLS3P | OLS2N | OLS2P | OLS1N | OLS1P |
| MTU3 | TCNT | | | | | | | | |
| MTU4 | TCNT | | | | | | | | |
| MTU | TCDRA | | | | | | | | |
| MTU | TDDRA | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (19 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MTU3 | TGRA | | | | | | | | |
| MTU3 | TGRB | | | | | | | | |
| MTU4 | TGRA | | | | | | | | |
| MTU4 | TGRB | | | | | | | | |
| MTU | TCNTSA | | | | | | | | |
| MTU | TCBRA | | | | | | | | |
| MTU3 | TGRC | | | | | | | | |
| MTU3 | TGRD | | | | | | | | |
| MTU4 | TGRC | | | | | | | | |
| MTU4 | TGRD | | | | | | | | |
| MTU3 | TSR | TCFD | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU4 | TSR | TCFD | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU | TITCR1A | T3AEN | | T3ACOR[2:0] | | T4VEN | | T4VCOR[2:0] | |
| MTU | TBTERA | — | | T3ACOR[2:0] | | — | | T4VCNT[2:0]] | |
| MTU | TBTERA | — | — | — | — | — | — | BTE[1:0] | |
| MTU | TDERA | — | — | — | — | — | — | — | TDER |
| MTU | TOLBRA | — | — | OLS3N | OLS3P | OLS2N | OLS2P | OLS1N | OLS1P |
| MTU3 | TBTM | — | — | — | — | — | — | TTSB | TTSA |
| MTU4 | TBTM | — | — | — | — | — | — | TTSB | TTSA |
| MTU | TITMRA | — | — | — | — | — | — | — | TITM |
| MTU | TITCR2A | — | — | — | — | — | | TRG4COR[2:0] | |
| MTU | TITCNT2A | — | — | — | — | — | | TRG4COR[2:0] | |
| MTU4 | TADCR | BF[1:0] | | — | — | — | — | — | — |
| | | UT4AE | DT4AE | UT4BE | DT4BE | ITA3AE | ITA4VE | ITB3AE | ITB4VE |
| MTU4 | TADCORA | | | | | | | | |
| MTU4 | TADCORB | | | | | | | | |
| MTU4 | TADCOBRA | | | | | | | | |
| MTU4 | TADCOBRB | | | | | | | | |
| MTU | TWCRA | CCE | — | — | — | — | — | — | WRE |
| MTU | TMDR2A | — | — | — | — | — | — | — | DRS |
| MTU3 | TGRE | | | | | | | | |
| MTU4 | TGRE | | | | | | | | |
| MTU4 | TGRF | | | | | | | | |
| MTU | TSTRA | CST4 | CST3 | — | — | — | CST2 | CST1 | CST0 |
| MTU | TSYRA | SYNC4 | SYNC3 | — | — | — | SYNC2 | SYNC1 | SYNC0 |
| MTU | TCSYSTR | SCH0 | SCH1 | SCH2 | SCH3 | SCH4 | — | SCH6 | SCH7 |
| MTU | TRWERA | — | — | — | — | — | — | — | RWE |
| MTU0 | TCR | | CCLR[2:0] | | | CKEG[1:0] | | TPSC[2:0] | |

**Table 4.2 List of I/O Registers (Bit Order) (20 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MTU0 | TMDR1 | — | BFE | BFB | BFA | | | MD[3:0] | |
| MTU0 | TIORH | | IOB[3:0] | | | | | IOA[3:0] | |
| MTU0 | TIORL | | IOD[3:0] | | | | | IOC[3:0] | |
| MTU0 | TIER | TTEG | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU0 | TSR | — | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU0 | TCNT | | | | | | | | |
| MTU0 | TGRA | | | | | | | | |
| MTU0 | TGRB | | | | | | | | |
| MTU0 | TGRC | | | | | | | | |
| MTU0 | TGRD | | | | | | | | |
| MTU0 | TGRE | | | | | | | | |
| MTU0 | TGRF | | | | | | | | |
| MTU0 | TIER2 | TTGE2 | — | — | — | — | — | TGIEF | TGIEE |
| MTU0 | TSR2 | — | — | — | — | — | — | TGFF | TGFE |
| MTU0 | TBTM | — | — | — | — | — | TTSE | TTSB | TTSA |
| MTU1 | TCR | — | CCLR[1:0] | | CKEG[1:0] | | | TPSC[2:0] | |
| MTU1 | TMDR1 | — | — | — | — | | | MD[3:0] | |
| MTU1 | TIOR | | IOB[3:0] | | | | | IOA[3:0] | |
| MTU1 | TIER | TTEG | — | TCIEU | TCIEV | — | — | TGIEB | TGIEA |
| MTU1 | TSR | TCFD | — | TCFU | TCFV | — | — | TGFB | TGFA |
| MTU1 | TCNT | | | | | | | | |
| MTU1 | TGRA | | | | | | | | |
| MTU1 | TGRB | | | | | | | | |
| MTU1 | TICCR | — | — | — | — | I2BE | I2AE | I1BE | I1AE |
| MTU2 | TCR | — | CCLR[1:0] | | CKEG[1:0] | | | TPSC[2:0] | |
| MTU2 | TMDR1 | — | — | — | — | | | MD[3:0] | |
| MTU2 | TIOR | | IOB[3:0] | | | | | IOA[3:0] | |
| MTU2 | TIER | TTGE | — | TCIEU | TCIEV | — | — | TGIEB | TGIEA |
| MTU2 | TSR | TCFD | — | TCFU | TCFV | — | — | TGFB | TGFA |
| MTU2 | TCNT | | | | | | | | |
| MTU2 | TGRA | | | | | | | | |
| MTU2 | TGRB | | | | | | | | |
| MTU6 | TCR | | CCLR[20] | | CKEG[1:0] | | | TPSC[2:0] | |
| MTU7 | TCR | | CCLR[20] | | CKEG[1:0] | | | TPSC[2:0] | |
| MTU6 | TMDR1 | — | — | BFB | BFA | | | MD[3:0] | |
| MTU7 | TMDR1 | — | — | BFB | BFA | | | MD[3:0] | |
| MTU6 | TIORH | | IOB[3:0] | | | | | IOA[3:0] | |
| MTU6 | TIORL | | IOD[3:0] | | | | | IOC[3:0] | |
| MTU7 | TIORH | | IOB[3:0] | | | | | IOA[3:0] | |

**Table 4.2 List of I/O Registers (Bit Order) (21 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MTU7 | TIORL | IOD[3:0] | | | | IOC[3:0] | | | |
| MTU6 | TIER | TTEG | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU7 | TIER | TTEG | TTEG2 | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU | TOERB | — | — | OE7D | OE7C | OE6D | OE7B | OE7A | OE6B |
| MTU | TOCR1B | — | PSYE | — | — | TOCL | TOCS | OLSN | OLSP |
| MTU6 | TCNT | | | | | | | | |
| MTU7 | TCNT | | | | | | | | |
| MTU | TCDRB | | | | | | | | |
| MTU | TDDRB | | | | | | | | |
| MTU6 | TGRA | | | | | | | | |
| MTU6 | TGRB | | | | | | | | |
| MTU7 | TGRA | | | | | | | | |
| MTU7 | TGRB | | | | | | | | |
| MTU | TCNTSB | | | | | | | | |
| MTU | TCBRB | | | | | | | | |
| MTU6 | TGRC | | | | | | | | |
| MTU6 | TGRD | | | | | | | | |
| MTU7 | TGRC | | | | | | | | |
| MTU7 | TGRD | | | | | | | | |
| MTU6 | TSR | TCFD | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU7 | TSR | TCFD | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU | TITCR1B | T6AEN | | T6ACOR[2:0] | | T7VEN | | T7VCOR[2:0] | |
| MTU | TITCNT1B | — | | T6ACNT[2:0] | | — | | T7VCNT[2:0] | |
| MTU | TBTERB | — | — | — | — | — | — | BTE[1:0] | |
| MTU | TDERB | — | — | — | — | — | — | — | TDER |
| MTU | TOLBRB | — | — | OLS3N | OLS3P | OLS2N | OLS2P | OLS1N | OLS1P |
| MTU6 | TBTM | — | — | — | — | — | — | TTSB | TTSA |
| MTU7 | TBTM | — | — | — | — | — | — | TTSB | TTSA |
| MTU | TITMRB | — | — | — | — | — | — | — | TITM |
| MTU | TITCR2B | — | — | — | — | — | | TRGCOR[2:0] | |
| MTU | TITCNT2B | — | — | — | — | — | | TRG7CNT[2:0] | |
| MTU7 | TADCR | BF[1:0] | | — | — | — | — | — | — |
| | | UT7AE | DT7AE | UT7BE | DT7BE | ITA6AE | ITA7VE | ITB6AE | ITB7VE |
| MTU7 | TADCORA | | | | | | | | |
| MTU7 | TADCORB | | | | | | | | |
| MTU7 | TADCOBRA | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (22 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MTU7 | TADCOBRB | | | | | | | | |
| MTU | TSYCR | CE0A | CE0D | CE0C | CE0D | CE1A | CE1B | CE2A | CE2B |
| MTU | TWCRB | CCE | — | — | — | — | — | SCC | WRE |
| MTU | TMDR2B | — | — | — | — | — | — | — | DRS |
| MTU6 | TGRE | | | | | | | | |
| MTU7 | TGRE | | | | | | | | |
| MTU7 | TGRF | | | | | | | | |
| MTU | TSTRB | CST7 | CST6 | — | — | — | — | — | — |
| MTU | TSYRB | SYNC7 | SYNC6 | — | — | — | — | — | — |
| MTU | TRWERB | — | — | — | — | — | — | — | RWE |
| MTU5 | TCNTU | | | | | | | | |
| MTU5 | TGRU | | | | | | | | |
| MTU5 | TCRU | — | — | — | — | — | — | TPSC[1:0] | |
| MTU5 | TIORU | — | — | — | | | IOC[4:0] | | |
| MTU5 | TCNTV | | | | | | | | |
| MTU5 | TGRV | | | | | | | | |
| MTU5 | TCRV | — | — | — | — | — | — | TPSC[1:0] | |
| MTU5 | TIORV | — | — | — | | | IOC[4:0] | | |
| MTU5 | TCNTW | | | | | | | | |
| MTU5 | TGRW | | | | | | | | |
| MTU5 | TCRW | — | — | — | — | — | — | TPSC[1:0] | |
| MTU5 | TIORW | — | — | — | | | IOC[4:0] | | |
| MTU5 | TSR | — | — | — | — | — | CMFU5 | CMFV5 | CMFW5 |
| MTU5 | TIER | — | — | — | — | — | TGIE5U | TGIE5V | TGIE5W |
| MTU5 | TSTR | — | — | — | — | — | CSTU5 | CSTV5 | CSTW5 |
| MTU5 | TCNTCMPCLR | — | — | — | — | — | CMPCLR5U | CMPCLR5V | CMPCLR5W |
| GPT | GTSTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | CST3 | CST2 | CST1 | CST0 |
| GPT | GTHSCR | CPHW3[1:0] | | CPHW2[1:0] | | CPHW1[1:0] | | CPHW0[1:0] | |
| | | CSHW3[1:0] | | CSHW2[1:0] | | CSHW1[1:0] | | CSHW0[1:0] | |
| GPT | GTHCCR | — | — | — | — | CCSW3 | CCSW2 | CCSW1 | CCSW0 |
| | | CCHW3[1:0] | | CCHW2[1:0] | | CCHW1[1:0] | | CCHW0[1:0] | |
| GPT | GTHSSR | CSHSL3[3:0] | | | | | CSHSL2[3:0] | | |
| | | CSHSL1[3:0] | | | | | CSHSL0[3:0] | | |
| GPT | GTHPSR | CSHPL3[3:0] | | | | | CSHPL2[3:0] | | |
| | | CSHPL1[3:0] | | | | | CSHPL0[3:0] | | |
| GPT | GTWP | — | — | — | — | — | — | — | — |
| | | — | — | — | — | WP3 | WP2 | WP1 | WP0 |
| GPT | GTSYNC | — | — | SYNC3[1:0] | | — | — | SYNC2[1:0] | |
| | | — | — | SYNC1[1:0] | | — | — | SYNC0[1:0] | |
| GPT | GTETINT | — | — | — | — | — | — | ETINF | ETIPF |
| | | — | — | — | — | — | — | ETINEN | ETIPEN |

**Table 4.2 List of I/O Registers (Bit Order) (23 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT | GTBDR | BD33 | BD32 | BD31 | BD30 | BD23 | BD22 | BD21 | BD20 |
| | | BD13 | BD12 | BD11 | BD10 | BD03 | BD02 | BD01 | BD00 |
| GPT | GTSWP | — | — | — | — | — | — | — | — |
| | | — | — | — | — | SWP3 | SWP2 | SWP1 | SWP0 |
| GPT | LCCR | LPSC[1:0] | | TPSC[1:0] | | LCNTAT | | LCTO[2:0] | |
| | | — | LCINTO | LCINTD | LCINTC | — | LCNTS | LCNTCR | LCNTE |
| GPT | LCST | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | LISO | LISD | LISC |
| GPT | LCNTA | | | | | | | | |
| GPT | LCNT00 | | | | | | | | |
| GPT | LCNT01 | | | | | | | | |
| GPT | LCNT02 | | | | | | | | |
| GPT | LCNT03 | | | | | | | | |
| GPT | LCNT04 | | | | | | | | |
| GPT | LCNT05 | | | | | | | | |
| GPT | LCNT06 | | | | | | | | |
| GPT | LCNT07 | | | | | | | | |
| GPT | LCNT08 | | | | | | | | |
| GPT | LCNT09 | | | | | | | | |
| GPT | LCNT10 | | | | | | | | |
| GPT | LCNT11 | | | | | | | | |
| GPT | LCNT12 | | | | | | | | |
| GPT | LCNT13 | | | | | | | | |
| GPT | LCNT14 | | | | | | | | |
| GPT | LCNT15 | | | | | | | | |
| GPT | LCNTDU | | | | | | | | |
| GPT | LCNTDL | | | | | | | | |
| GPT0 | GTIOR | OBHLD | OBDFLT | | | GTIOB[5:0] | | | |
| | | OAHLD | OADFLT | | | GTIOA[5:0] | | | |
| GPT0 | GTINTAD | ADTRBDEN | ADTRBUEN | ADTRADEN | ADTRAUEN | EINT | — | — | — |
| | | GTINTPR[1:0] | | GTINTF | GTINTE | GTINTD | GTINTC | GTINTB | GTINTA |

**Table 4.2 List of I/O Registers (Bit Order) (24 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT0 | GTCR | — | — | CCLR[1:0] | | — | — | TPCS[1:0] | |
| | | — | — | — | — | — | | MD[2:0] | |
| GPT0 | GTBER | — | ADTDB | ADTTB[1:0] | | — | ADTDA | ADTTA[1:0] | |
| | | — | CCRSWT | PR[1:0] | | CCRB[1:0] | | CCRA[1:0] | |
| GPT0 | GTUDC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | UDF | UD |
| GPT0 | GTITC | — | ADTBL | — | ADTAL | — | IVTT[2:0] | | |
| | | IVTC[1:0] | | ITLF | ITLE | ITLD | ITLC | ITLB | ITLA |
| GPT0 | GTST | TUCF | — | — | — | DTEF | | ITCNT[2:0] | |
| | | TCFPU | TCFPO | TCFF | TCFE | TCFD | TCFC | TCFB | TCFA |
| GPT0 | GTCNT | | | | | | | | |
| GPT0 | GTCCRA | | | | | | | | |
| GPT0 | GTCCRB | | | | | | | | |
| GPT0 | GTCCRC | | | | | | | | |
| GPT0 | GTCCRD | | | | | | | | |
| GPT0 | GTCCRE | | | | | | | | |
| GPT0 | GTCCRF | | | | | | | | |
| GPT0 | GTPR | | | | | | | | |
| GPT0 | GTPBR | | | | | | | | |
| GPT0 | GTPDBR | | | | | | | | |
| GPT0 | GTADTRA | | | | | | | | |
| GPT0 | GTADTBRA | | | | | | | | |
| GPT0 | GTADTDBRA | | | | | | | | |
| GPT0 | GTADTRB | | | | | | | | |
| GPT0 | GTADTBRB | | | | | | | | |
| GPT0 | GTADTDBRB | | | | | | | | |
| GPT0 | GTONCR | OBE | OAE | — | SWN | — | — | — | NFV |
| | | | NFS[3:0] | | | NVB | NVA | NEB | NEA |
| GPT0 | GTDTCR | — | — | — | — | — | — | — | TDFER |
| | | — | — | TDBDE | TDBUE | — | — | — | TDE |
| GPT0 | GTDVU | | | | | | | | |
| GPT0 | GTDVD | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (25 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT0 | GTDBU | | | | | | | | |
| GPT0 | GTDBD | | | | | | | | |
| GPT0 | GTSOS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT0 | GTSOTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | SOTR |
| GPT1 | GTIOR | OBHLD | OBDFLT | | | GTIOB[5:0] | | | |
| | | OAHLD | OADFLT | | | GTIOA[5:0] | | | |
| GPT1 | GTINTAD | ADTRBDEN | ADTRBUEN | ADTRADEN | ADTRAUEN | EINT | — | — | — |
| | | GTINTPR[1:0] | | GTINTF | GTINTE | GTINTD | GTINTC | GTINTB | GTINTA |
| GPT1 | GTCR | — | — | CCLR[1:0] | | — | — | TPCS[1:0] | |
| | | — | — | — | — | — | | MD[2:0] | |
| GPT1 | GTBER | — | ADTDB | ADTTB[1:0] | | — | ADTDA | ADTTA[1:0] | |
| | | — | CCRSWT | PR[1:0] | | CCRB[1:0] | | CCRA[1:0] | |
| GPT1 | GTUDC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | UDF | UD |
| GPT1 | GTITC | — | ADTBL | — | ADTAL | — | | IVTT[2:0] | |
| | | IVTC[1:0] | | ITLF | ITLE | ITLD | ITLC | ITLB | ITLA |
| GPT1 | GTST | TUCF | — | — | — | DTEF | | ITCNT[2:0] | |
| | | TCFPU | TCFPO | TCFF | TCFE | TCFD | TCFC | TCFB | TCFA |
| GPT1 | GTCNT | | | | | | | | |
| GPT1 | GTCCRA | | | | | | | | |
| GPT1 | GTCCRB | | | | | | | | |
| GPT1 | GTCCRC | | | | | | | | |
| GPT1 | GTCCRD | | | | | | | | |
| GPT1 | GTCCRE | | | | | | | | |
| GPT1 | GTCCRF | | | | | | | | |
| GPT1 | GTPR | | | | | | | | |
| GPT1 | GTPBR | | | | | | | | |
| GPT1 | GTPDBR | | | | | | | | |
| GPT1 | GTADTRA | | | | | | | | |
| GPT1 | GTADTBRA | | | | | | | | |
| GPT1 | GTADTDBRA | | | | | | | | |
| GPT1 | GTADTRB | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (26 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT1 | GTADTBRB | | | | | | | | |
| GPT1 | GTADTDBRB | | | | | | | | |
| GPT1 | GTONCR | OBE | OAE | — | SWN | — | — | — | NFV |
| | | NFS[3:0] | | | | NVB | NVA | NEB | NEA |
| GPT1 | GTDTCR | — | — | — | — | — | — | — | TDFER |
| | | — | — | TDBDE | TDBUE | — | — | — | TDE |
| GPT1 | GTDVU | | | | | | | | |
| GPT1 | GTDVD | | | | | | | | |
| GPT1 | GTDBU | | | | | | | | |
| GPT1 | GTDBD | | | | | | | | |
| GPT1 | GTSOS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT1 | GTSOTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | SOTR |
| GPT2 | GTIOR | OBHLD | OBDFLT | GTIOB[5:0] | | | | | |
| | | OAHLD | OADFLT | GTIOA[5:0] | | | | | |
| GPT2 | GTINTAD | ADTRBDEN | ADTRBUEN | ADTRADEN | ADTRAUEN | EINT | — | — | — |
| | | GTINTPR[1:0] | | GTINTF | GTINTE | GTINTD | GTINTC | GTINTB | GTINTA |
| GPT2 | GTCR | — | — | CCLR[1:0] | | — | — | TPCS[1:0] | |
| | | — | — | — | — | — | MD[2:0] | | |
| GPT2 | GTBER | — | ADTDB | ADTTB[1:0] | | — | ADTDA | ADTTA[1:0] | |
| | | — | CCRSWT | PR[1:0] | | CCRB[1:0] | | CCRA[1:0] | |
| GPT2 | GTUDC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | UDF | UD |
| GPT2 | GTITC | — | ADTBL | — | ADTAL | — | IVTT[2:0] | | |
| | | IVTC[1:0] | | ITLF | ITLE | ITLD | ITLC | ITLB | ITLA |
| GPT2 | GTST | TUCF | — | — | — | DTEF | ITCNT[2:0] | | |
| | | TCFPU | TCFPO | TCFF | TCFE | TCFD | TCFC | TCFB | TCFA |
| GPT2 | GTCNT | | | | | | | | |
| GPT2 | GTCCRA | | | | | | | | |
| GPT2 | GTCCRB | | | | | | | | |
| GPT2 | GTCCRC | | | | | | | | |
| GPT2 | GTCCRD | | | | | | | | |
| GPT2 | GTCCRE | | | | | | | | |
| GPT2 | GTCCRF | | | | | | | | |
| GPT2 | GTPR | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (27 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT2 | GTPBR | | | | | | | | |
| GPT2 | GTPDBR | | | | | | | | |
| GPT2 | GTADTRA | | | | | | | | |
| GPT2 | GTADTBRA | | | | | | | | |
| GPT2 | GTADTDBRA | | | | | | | | |
| GPT2 | GTADTRB | | | | | | | | |
| GPT2 | GTADTBRB | | | | | | | | |
| GPT2 | GTADTDBRB | | | | | | | | |
| GPT2 | GTONCR | OBE | OAE | — | SWN | — | — | — | NFV |
| | | | NFS[3:0] | | | NVB | NVA | NEB | NEA |
| GPT2 | GTDTCR | — | — | — | — | — | — | — | TDFER |
| | | — | — | TDBDE | TDBUE | — | — | — | TDE |
| GPT2 | GTDVU | | | | | | | | |
| GPT2 | GTDVD | | | | | | | | |
| GPT2 | GTDBU | | | | | | | | |
| GPT2 | GTDBD | | | | | | | | |
| GPT2 | GTSOS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT2 | GTSOTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | SOTR |
| GPT3 | GTIOR | OBHLD | OBDFLT | | | GTIOB[5:0] | | | |
| | | OAHLD | OADFLT | | | GTIOA[5:0] | | | |
| GPT3 | GTINTAD | ADTRBDEN | ADTRBUEN | ADTRADEN | ADTRAUEN | EINT | — | — | — |
| | | GTINTPR[1:0] | | GTINTF | GTINTE | GTINTD | GTINTC | GTINTB | GTINTA |
| GPT3 | GTCR | — | — | CCLR[1:0] | | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| GPT3 | GTBER | — | ADTDB | ADTTB[1:0] | | — | ADTDA | ADTTA[1:0] | |
| | | — | CCRSWT | PR[1:0] | | CCRB[1:0] | | CCRA[1:0] | |
| GPT3 | GTUDC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | UDF | UD |
| GPT3 | GTITC | — | ADTBL | — | ADTAL | — | | IVTT[2:0] | |
| | | IVTC[1:0] | | ITLF | ITLE | ITLD | ITLC | ITLB | ITLA |
| GPT3 | GTST | TUCF | — | — | — | DTEF | | ITCNT[2:0] | |
| | | TCFPU | TCFPO | TCFF | TCFE | TCFD | TCFC | TCFB | TCFA |
| GPT3 | GTCNT | | | | | | | | |
| GPT3 | GTCCRA | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (28 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT3 | GTCCRB | | | | | | | | |
| GPT3 | GTCCRC | | | | | | | | |
| GPT3 | GTCCRD | | | | | | | | |
| GPT3 | GTCCRE | | | | | | | | |
| GPT3 | GTCCRF | | | | | | | | |
| GPT3 | GTPR | | | | | | | | |
| GPT3 | GTPBR | | | | | | | | |
| GPT3 | GTPDBR | | | | | | | | |
| GPT3 | GTADTRA | | | | | | | | |
| GPT3 | GTADTBRA | | | | | | | | |
| GPT3 | GTADTDBRA | | | | | | | | |
| GPT3 | GTADTRB | | | | | | | | |
| GPT3 | GTADTBRB | | | | | | | | |
| GPT3 | GTADTDBRB | | | | | | | | |
| GPT3 | GTONCR | OBE | OAE | — | SWN | — | — | — | NFV |
| | | | | NFS[3:0] | | NVB | NVA | NEB | NEA |
| GPT3 | GTDTCR | — | — | — | — | — | — | — | TDFER |
| | | — | — | TDBDE | TDBUE | — | — | — | TDE |
| GPT3 | GTDVU | | | | | | | | |
| | | | | | | | | | |
| GPT3 | GTDVD | | | | | | | | |
| GPT3 | GTDBU | | | | | | | | |
| GPT3 | GTDBD | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT3 | GTSOS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT3 | GTSOTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | SOTR |
| GPT0 | GTDLYCR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DLYEN | DLYRST | DLLEN |
| GPT1 | GTDLYCR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DLYEN | DLYRST | DLLEN |

**Table 4.2 List of I/O Registers (Bit Order) (29 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT2 | GTDLYCR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DLYEN | DLYRST | DLLEN |
| GPT3 | GTDLYCR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DLYEN | DLYRST | DLLEN |
| GPT0 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT0 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT1 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT1 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT2 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT2 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT3 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT3 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT0 | GTDLYFA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT0 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT1 | GTDLYFA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT1 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT2 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT2 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT3 | GTDLYFA | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| GPT3 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | | | DLY[4:0] | | |
| FLASH | FMODR | — | — | — | FRDMD | | — | — | — |
| FLASH | FASTAT | ROMAE | — | — | CMDLK | DFLAE | — | DFLRPE | DFLWPE |
| FLASH | FAEINT | ROMAEIE | — | — | CMDLKIE | DFLAEIE | — | DFLRPEIE | DFLWPEIE |
| FLASH | FRDYIE | — | — | — | — | — | — | — | FRDYIE |
| FLASH | DFLRE0 | | | | KEY[7:0] | | | | |
| | | DBRE07 | DBRE06 | DBRE05 | DBRE04 | DBRE03 | DBRE02 | DBRE01 | DBRE00 |
| FLASH | DFLRE1 | | | | KEY[7:0] | | | | |
| | | DBRE15 | DBRE14 | DBRE13 | DBRE12 | DBRE11 | DBRE10 | DBRE09 | DBRE08 |
| FLASH | DFLWE0 | | | | KEY[7:0] | | | | |
| | | DBWE07 | DBWE06 | DBWE05 | DBWE04 | DBWE03 | DBWE02 | DBWE01 | DBWE00 |
| FLASH | DFLWE1 | | | | KEY[7:0] | | | | |
| | | DBWE15 | DBWE14 | DBWE13 | DBWE12 | DBWE11 | DBWE10 | DBWE09 | DBWE08 |
| FLASH | FCURAME | | | | KEY[7:0] | | | | |
| | | — | — | — | — | — | — | — | FCRME |

**Table 4.2 List of I/O Registers (Bit Order) (30 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| FLASH | FSTATR0 | FRDY | ILGLERR | ERSERR | PRGERR | SUSRDY | — | ERSSPD | PRGSPD |
| FLASH | FSTATR1 | FCUERR | — | — | FLOCKST | — | — | — | — |
| FLASH | FENTRYR | FEKEY[7:0] | | | | | | | |
| | | FENTRYD | — | — | — | — | — | — | FENTRY0 |
| FLASH | FPROTR | FPKEY[7:0] | | | | | | | |
| | | — | — | — | — | — | — | — | FPROTCN |
| FLASH | FRESETR | FRKEY[7:0] | | | | | | | |
| | | — | — | — | — | — | — | — | FRESET |
| FLASH | FCMDR | CMDR[7:0] | | | | | | | |
| | | PCMDR[7:0] | | | | | | | |
| FLASH | FCPSR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | ESUSPMD |
| FLASH | DFLBCCNT | — | — | — | — | — | | BCADR[7:0] | |
| | | BCADR[7:0] | | | | | | — | BCSIZE |
| FLASH | FPESTAT | — | — | — | — | — | — | — | — |
| | | PEERRST[7:0] | | | | | | | |
| FLASH | DFLBCSTAT | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | BCST |
| FLASH | PCKAR | — | — | — | — | — | — | — | — |
| | | PCKA[7:0] | | | | | | | |

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC<br>PLLVCC | -0.3 to +6.5 | V |
| Input voltage (except for ports 4 to 6) | | $V_{IN}$ | -0.3 to VCC+0.3 | V |
| Input voltage (port 4) | | $V_{IN}$ | -0.3 to AVCC0+0.3 | V |
| Input voltage (ports 5 and 6) | | $V_{IN}$ | -0.3 to AVCC+0.3 | V |
| Analog power supply voltage | | AVCC0, AVCC*1 | -0.3 to +6.5 | V |
| Reference power supply voltage | | VREFH0*1 | -0.3 to AVCC0+0.3 | V |
| | | VREF*1 | -0.3 to AVCC+0.3 | |
| Analog input voltage (port 4) | | $V_{AN}$ | -0.3 to AVCC0+0.3 | V |
| Analog input voltage (ports 5 and 6) | | $V_{AN}$ | -0.3 to AVCC+0.3 | V |
| Operating temperature | D version | $T_{opr}$ | -40 to +85 | °C |
| | G version | $T_{opr}$ | -40 to +105 | °C |
| Storage temperature | | $T_{stg}$ | -55 to +125 | °C |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.
- When the 12-bit converter is not in use:
  Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:
  Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:
  Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.

## 5.2 DC Characteristics

**Table 5.2 DC Characteristics (1) (1 / 3)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | CAN input pin<br>IRQ input pin<br>MTU3 input pin<br>POE3 input pin<br>SCI input pin<br>A/D trigger input pin<br>NMI input pin<br>GPT input pin<br>LIN input pin<br>RES# | $V_{IH}$ | VCC×0.8 | - | VCC+0.3 | V | |
| | | $V_{IL}$ | -0.3 | - | VCC×0.2 | | |
| | | $\Delta V_T$ | VCC ×0.06 | - | - | | |
| | RIIC input pin (IICBus) | $V_{IH}$ | VCC×0.7 | - | VCC+0.3 | | |
| | | $V_{IL}$ | -0.3 | - | VCC×0.3 | | |
| | | $\Delta V_T$ | VCC ×0.05 | - | - | | |
| | Port 4*1 (also usable as an analog port) | $V_{IH}$ | AVCC0 ×0.8 | - | AVCC0 +0.3 | | |
| | | $V_{IL}$ | - 0.3 | - | AVCC0 ×0.2 | | |
| | | $\Delta V_T$ | AVCC0 ×0.06 | - | - | | |
| | Ports 5 and 6*1 (also usable as analog ports) | $V_{IH}$ | AVCC ×0.8 | - | AVCC +0.3 | | |
| | | $V_{IL}$ | -0.3 | - | AVCC ×0.2 | | |
| | | $\Delta V_T$ | AVCC ×0.06 | - | - | | |
| | Ports 1 to 3*1<br>Ports 7 to B*1<br>Ports D, E, and G*1 | $V_{IH}$ | VCC×0.8 | - | VCC+0.3 | | |
| | | $V_{IL}$ | -0.3 | - | VCC×0.2 | | |
| | | $\Delta V_T$ | VCC ×0.06 | - | - | | |
| Input high voltage (except Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | VCC×0.9 | - | VCC+0.3 | V | |
| | EXTAL<br>RSPI input pin | | VCC×0.8 | | VCC+0.3 | | |
| | RIIC input pin (SMBus) | | 2.1 | | VCC+0.3 | | Conditions 1 and 2 |
| Input low voltage (except Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | -0.3 | - | VCC×0.1 | V | |
| | EXTAL<br>RSPI input pin | | -0.3 | - | VCC×0.2 | | |
| | RIIC input pin (SMBus) | | -0.3 | - | 0.8 | | Conditions 1 and 2 |

**Table 5.2 DC Characteristics (1) (2 / 3)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output high voltage | All output pins (except for P71 to P76 and P90 to P95) | $V_{OH}$ | VCC-0.5 | - | - | V | $I_{OH}$ = -1 mA |
| | P71 to P76 | | VCC-0.5 | - | - | | $I_{OH}$ = -1mA<br>64-pin LQFP<br>Condition 3 |
| | | | VCC-1.0 | - | - | | $I_{OH}$ = -5mA<br>64-pin LQFP<br>Other than condition 3 |
| | P90 to P95 | | VCC-0.5 | - | - | | $I_{OH}$ = -1mA<br>80-pin LQFP or<br>64-pin LQFP |
| | | | VCC-1.0 | - | - | | $I_{OH}$ = -5 mA<br>112-pin LQFP or<br>100-pin LQFP |
| Output low voltage | All output pins (except for P71 to P76, P90 to P95, and RIIC) | $V_{OL}$ | - | - | 0.5 | V | $I_{OL}$ = 1.0 mA |
| | P71 to P76 | | - | - | 0.5 | | $I_{OL}$ = 1.0 mA<br>64-pin LQFP<br>Other than condition 3 |
| | | | - | - | 1.1 | | $I_{OL}$ = 15 mA<br>Conditions 1 and 2 |
| | | | - | - | 1.4 | | $I_{OL}$ = 15 mA<br>Other than 64-pin LQFP<br>Condition 3 |
| | P90 to P95 | | - | - | 0.5 | | $I_{OL}$ = 1.0 mA<br>80-pin LQFP or<br>64-pin LQFP |
| | | | - | - | 1.1 | | $I_{OL}$ = 15 mA<br>112-pin LQFP or<br>100-pin LQFP<br>Conditions 1 and 2 |
| | | | - | - | 1.4 | | $I_{OL}$ = 1 mA<br>112-pin LQFP or<br>100-pin LQFP<br>Condition 3 |
| | RIIC pin | | - | - | 0.4 | | $I_{OL}$ = 3 mA |
| | | | - | - | 0.6 | | $I_{OL}$ = 6 mA |
| Input leakage current | RES#, MD pin, EMLE | $\lvert I_{in} \rvert$ | - | - | 1.0 | µA | $V_{in}$ = 0 V,<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | Ports 1 to A, PB0, PB3 to PB7, D, E, G | $\lvert I_{TSI} \rvert$ | - | - | 1.0 | µA | $V_{in}$ = 0 V,<br>$V_{in}$ = VCC |
| | Ports PB1 and PB2 | | - | - | 5.0 | | |

**Table 5.2 DC Characteristics (1) (3 / 3)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input capacitance | All input pins (except for ports PB1 and PB2) | $C_{in}$ | - | - | 15 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| | Ports PB1 and PB2 | | - | - | 30 | | |

Note 1. This includes the multiplexed input pins, except in cases where port pins PB1 and PB2 are used as RIIC input pins or port pins P22 to P24, P30, PA3 to PA5, PB0, PD0 to PD2, or PD6 are used as RSPI input pins.

**Table 5.3 DC Characteristics (2)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply current*1 | In operation | Max.*2 | $I_{CC}$*3 | - | - | 70 | mA | ICLK = 100 MHz PCLK = 50 MHz |
| | | Normal*4 | | - | 35 | - | | |
| | | Increased by BGO operation*5 | | - | 15 | - | | |
| | Sleep | | | | 22 | 60 | | |
| | All-module-clock-stop mode*6 | | | | 14 | 28 | | |
| | Standby mode | Software standby mode | | - | 0.10 | 3 | mA | |
| | | Deep software standby mode | | - | 20 | 60 | µA | |
| Analog power supply current | During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit) | | $AI_{CC0}$ | - | 3 | 5 | mA | |
| | During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit) | | | - | 3 | 5 | mA | |
| | Programmable gain amp (per channel) | | | - | 1 | 2 | mA | |
| | Window comparator (1 channel) | | | | 0.5 | 1 | mA | |
| | Window comparator (6 channels) | | | - | 1 | 2 | mA | |
| | During 12-bit A/D conversion (per unit) | | | - | 60 | 90 | µA | |
| | During 10-bit A/D conversion (per unit) | | $AI_{CC}$ | - | 0.9 | 2 | mA | |
| | Waiting for 10-bit A/D conversion (all units) | | | - | 0.3 | 3 | µA | |
| Reference power supply current | During 12-bit A/D conversion (per unit) | | $AI_{REFH0}$ | - | 1.6 | 3 | mA | |
| | Waiting for 12-bit A/D conversion (all units) | | | - | 1.6 | 3 | mA | |
| | During 10-bit A/D conversion (per unit) | | $AI_{REF}$ | - | 0.1 | 1 | mA | |
| | Waiting for 10-bit A/D conversion (all units) | | | - | 0.1 | 3 | µA | |
| VCC rising gradient | | | $SV_{CC}$ | - | - | 20 | ms/V | |

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. $I_{CC}$ depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max. = 0.54 x f + 16 (max.)
ICC max. = 0.3 x f + 5 (normal operation)
ICC max. = 0.44 x f + 16 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 6. The values are for reference.

**Table 5.4 Permissible Output Currents**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | $I_{OL}$ | - | - | 2.0*1 | mA |
| Permissible output low current (max. value per pin) | $I_{OL}$ | - | - | 4.0*1 | mA |
| Permissible output low current (total) | $\Sigma I_{OL}$ | - | - | 110 | mA |
| Permissible output high current (average value per pin) | $-I_{OH}$ | - | - | 2.0*1 | mA |
| Permissible output high current (max. value per pin) | $-I_{OH}$ | - | - | 4.0*1 | mA |
| Permissible output high current (total) | $\Sigma -I_{OH}$ | - | - | 35 | mA |

Caution: To protect the LSI's reliability, the output current values should not exceed the permissible output current.

Note 1. $I_{OL}$ = 15 mA (max.)/ $-I_{OH}$ = 5 mA (max.) for P71 to P76 and P90 to P95. Note, however, that up to 6 (112-pin or 100-pin LQFP) or 3 (80-pin or 64-pin LQFP) pins can accept over 2.0-mA $I_{OL}$ / $-I_{OH}$ at the same time.

**Table 5.5 Permissible Power Consumption (Only for G Version)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Total permissible power consumption*1 | Pd | — | 325 | mW | 85°C < Ta ≤ 105°C |

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Note 1. The total power consmuption of the whole chip including output current.

## 5.3 AC Characteristics

**Table 5.6 Operation Frequency Value**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | f | 8 | - | 100 | MHz |
| | Peripheral module clock (PCLK) | | 8 | - | 50 | |

### 5.3.1 Clock Timing

**Table 5.7 Clock Timing**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Oscillation settling time after reset (crystal) | $t_{OSC1}$ | 10 | - | ms | Figure 5.1 |
| Oscillation settling time after leaving software standby mode (crystal) | $t_{OSC2}$ | 10 | - | ms | Figure 5.2 |
| Oscillation settling time after leaving deep software standby mode (crystal) | $t_{OSC3}$ | 10 | - | ms | Figure 5.3 |
| EXTAL external clock output delay settling time | $t_{DEXT}$ | 1 | - | ms | Figure 5.1 |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 35 | - | ns | Figure 5.4 |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 35 | - | ns | |
| EXTAL external clock rising time | $t_{EXr}$ | - | 5 | ns | |
| EXTAL external clock falling time | $t_{EXf}$ | - | 5 | ns | |
| On-chip oscillator (IWDTCLK) oscillation frequency | $f_{IWDTCLK}$ | 62.5 | 187.5 | kHz | |

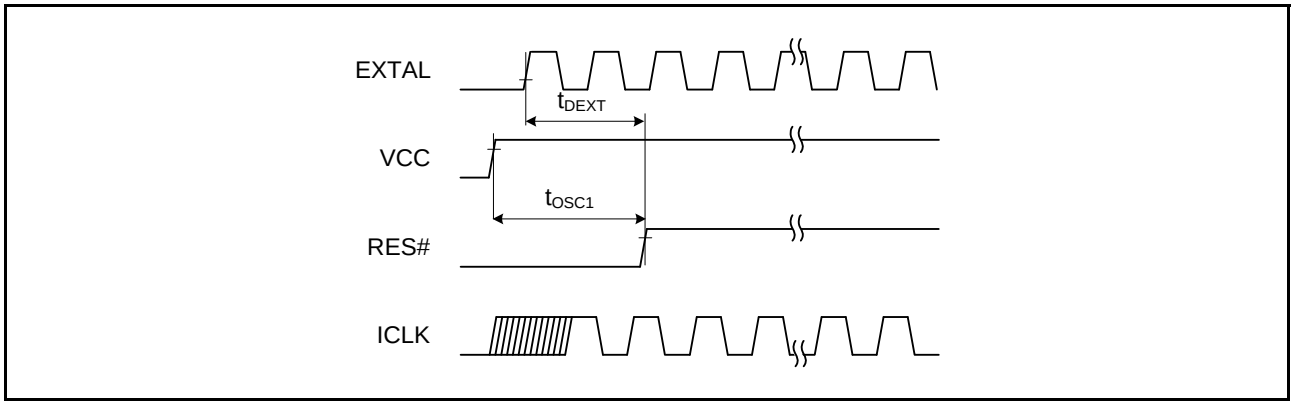



**Figure 5.1 Oscillation Settling Timing**

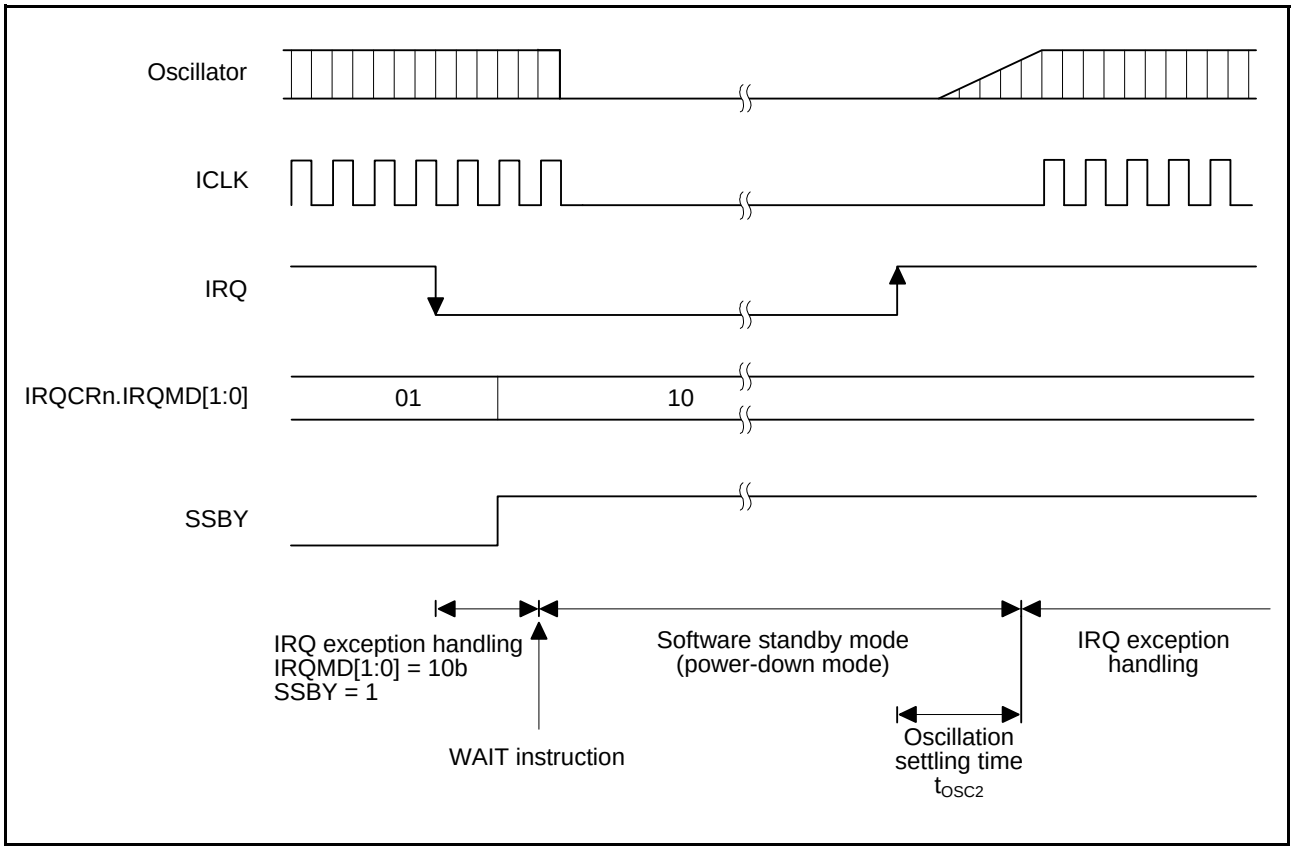



**Figure 5.2 Oscillation Settling Timing after Software Standby Mode**

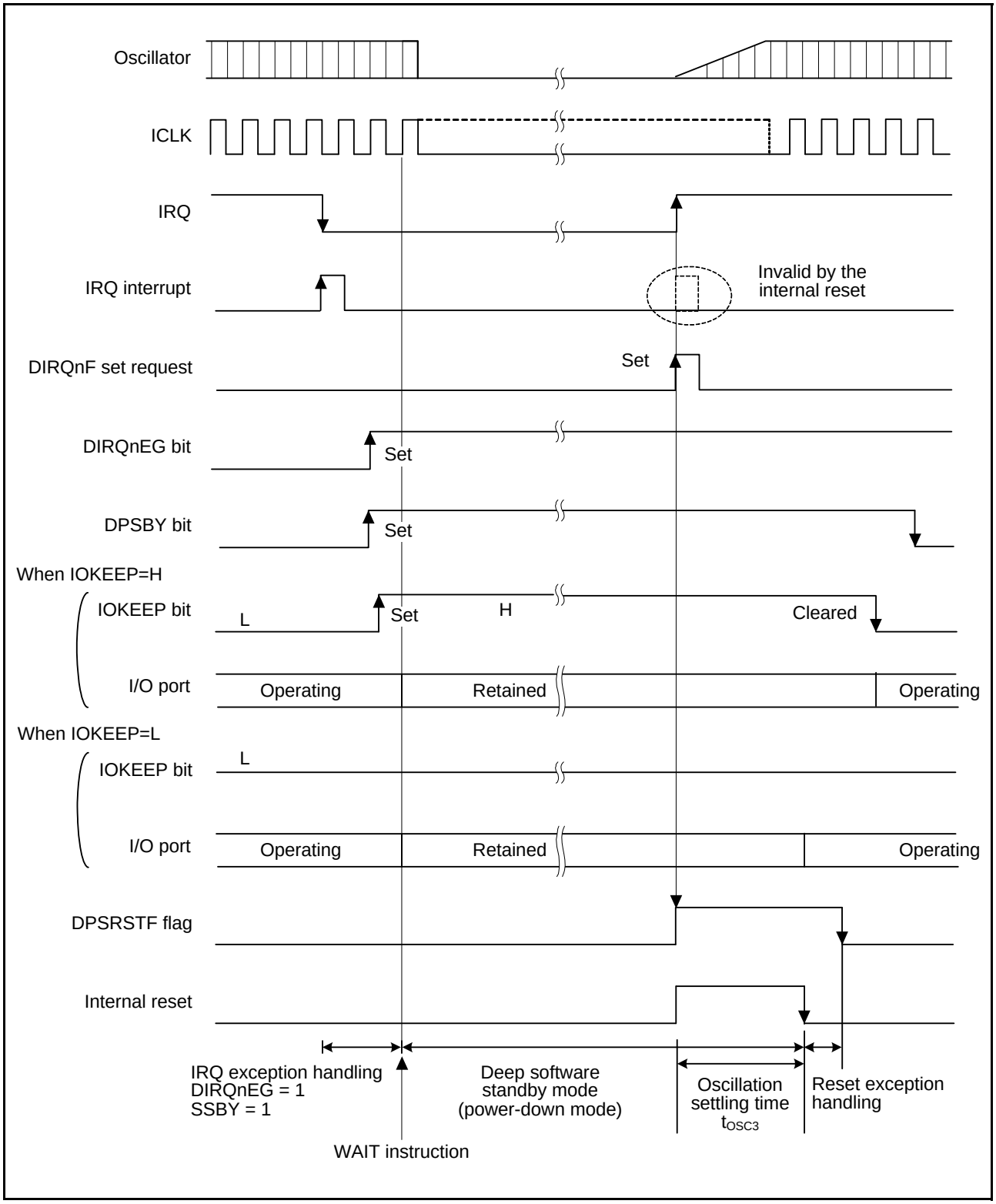



**Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode**

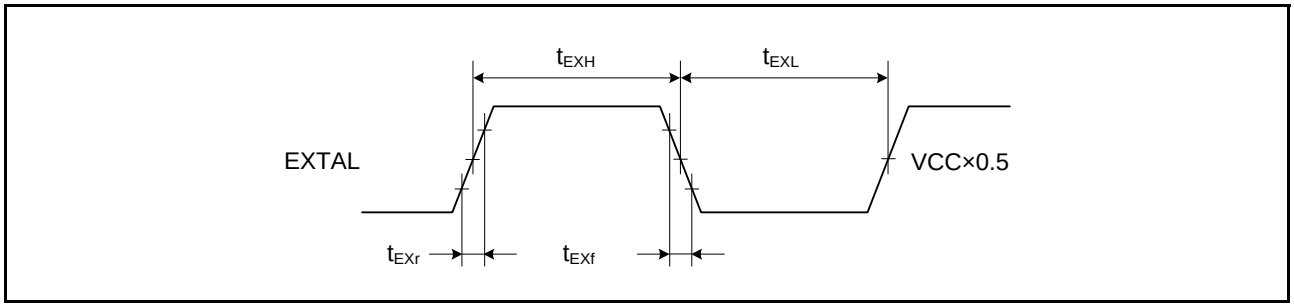



**Figure 5.4 EXTAL External Input Clock Timing**

## 5.3.2 Control Signal Timing

**Table 5.8 Control Signal Timing**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1) | $t_{RESW}$*2 | 20 | - | $t_{Icyc}$*4 | Figure 5.5 |
| | | 1.5 | - | µs | |
| Internal reset time*3 | $t_{RESW2}$ | 35 | - | µs | |
| NMI pulse width | $t_{NMIW}$ | 200 | - | ns | Figure 5.6 |
| IRQ pulse width | $t_{IRQW}$ | 200 | - | ns | Figure 5.7 |

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.
Note 2. Both the time and the number of cycles should satisfy the specifications.
Note 3. This is to specify the FCU reset.
Note 4. ICLK cycles.

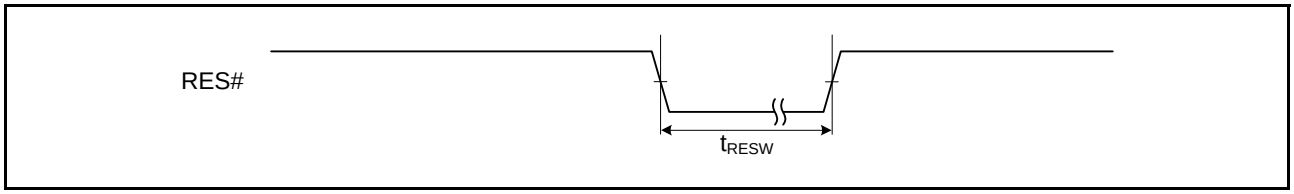



**Figure 5.5 Reset Input Timing**

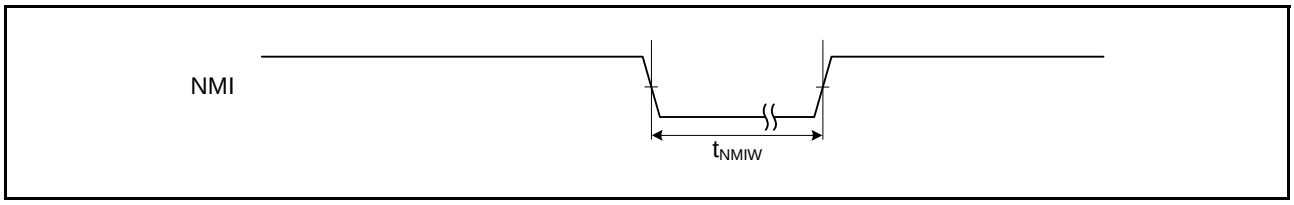



**Figure 5.6 NMI Interrupt Input Timing**

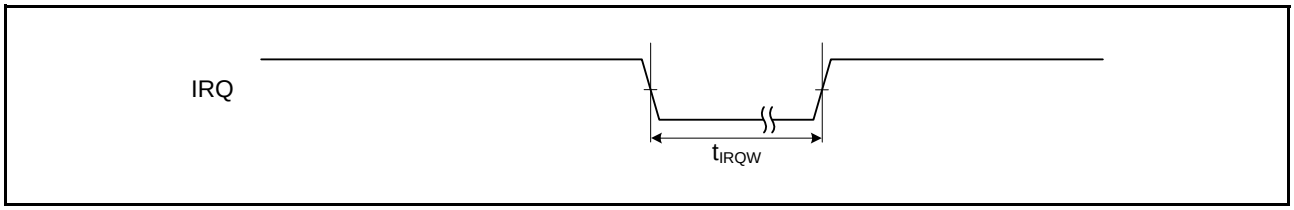



**Figure 5.7 IRQ Interrupt Input Timing**

## 5.3.3 Timing of On-Chip Peripheral Modules

**Table 5.9 Timing of On-Chip Peripheral Modules (1)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | $4 \times t_{Pcyc}$ | - | ns | Figure 5.8 |
| | | Clock synchronous | | $6 \times t_{Pcyc}$ | - | | |
| | Input clock pulse width | | $t_{SCKW}$ | $0.4 \times t_{Pcyc}$ | $0.6 \times t_{Scyc}$ | ns | |
| | Input clock rise time | | $t_{SCKr}$ | - | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | - | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | $16 \times t_{Pcyc}$ | - | ns | |
| | | Clock synchronous | | $6 \times t_{Pcyc}$ | - | ns | |
| | Output clock pulse width | | $t_{SCKW}$ | $0.4 \times t_{Scyc}$ | $0.6 \times t_{Scyc}$ | ns | |
| | Output clock rise time | | $t_{SCKr}$ | - | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | - | 20 | ns | |
| | Transmit data delay time (clock synchronous) | | $t_{TXD}$ | - | 40 | ns | Figure 5.9 |
| | Receive data setup time (clock synchronous) | | $t_{RXS}$ | 40 | - | ns | |
| | Receive data hold time (clock synchronous) | | $t_{RXH}$ | 40 | - | ns | |

Note: • $t_{Pcyc}$: PCLK cycle

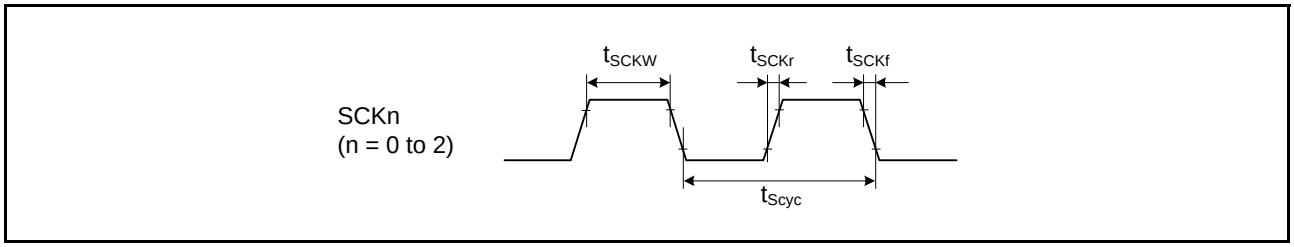



**Figure 5.8 SCK Clock Input Timing**

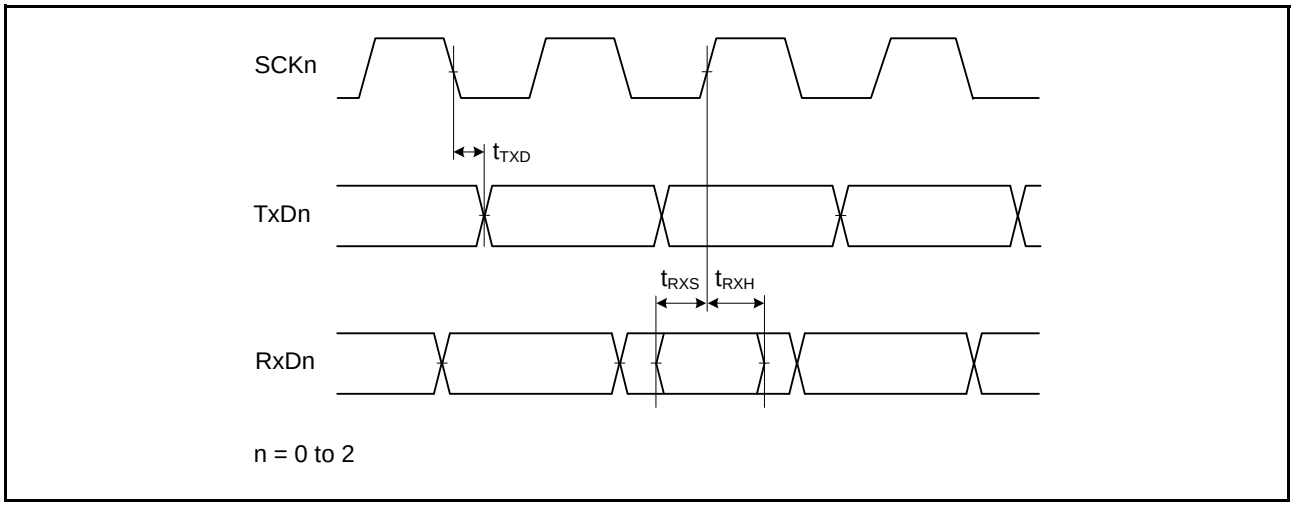



**Figure 5.9 SCI Input/Output Timing: Clock Synchronous Mode**

**Table 5.10 Timing of On-Chip Peripheral Modules (2)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min.*1 *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (standard mode) | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 1300 | - | ns | Figure 5.10 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 1000 | - | ns | |
| | SCL, SDA input rising time | $t_{Sr}$ | - | 1000 | ns | |
| | SCL, SDA input falling time | $t_{Sf}$ | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | - | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | Re-start condition input setup time | $t_{STAS}$ | 1000 | - | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |
| RIIC (fast mode) | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 600 | - | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rising time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input falling time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | - | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | Re-start condition input setup time | $t_{STAS}$ | 300 | - | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

Note: • $t_{IICcyc}$: Cycles of internal base clock (IICφ) for the RIIC module
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

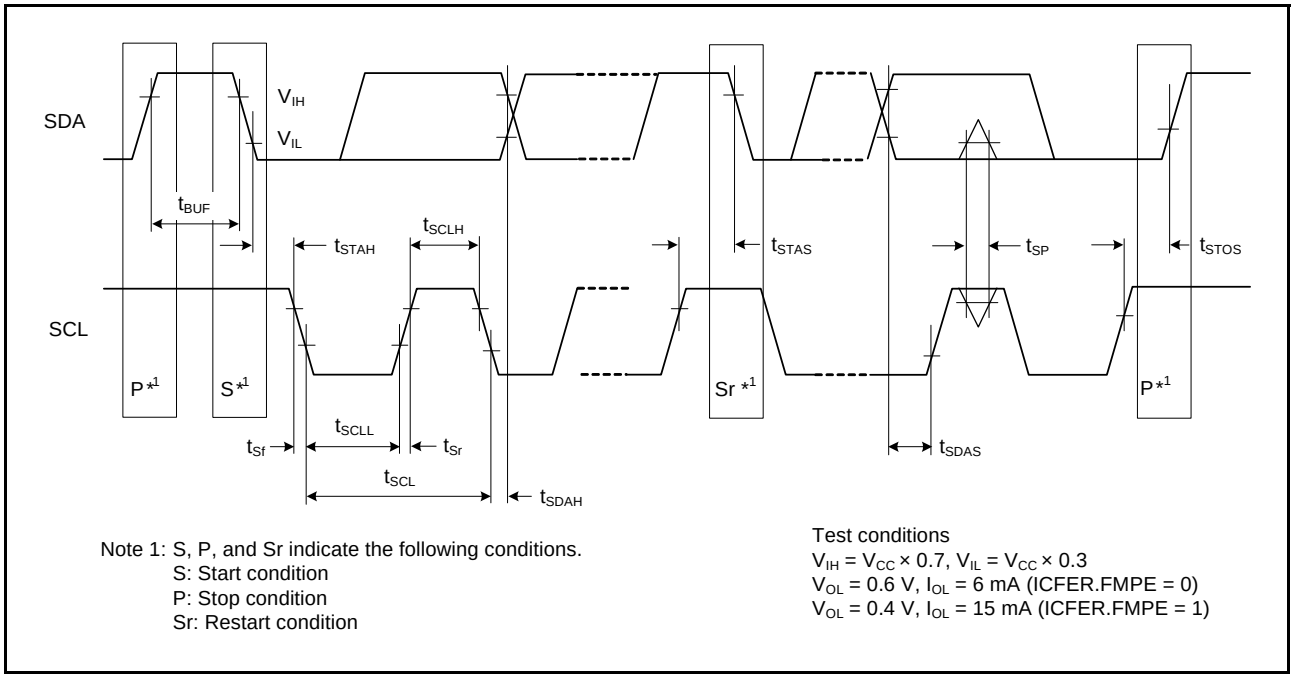



**Figure 5.10 I2C Bus Interface Input/Output Timing**

**Table 5.11 Timing of On-Chip Peripheral Modules (3)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | $t_{SPcyc}$ | 4 | 4096 | $t_{Pcyc}$ | Figure 5.11 |
| | | Slave | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | ($t_{Spcyc}$ - $t_{SPCKR}$ - $t_{SPCKF}$) / 2-3 | - | ns | |
| | | Slave | | ($t_{Spcyc}$ - $t_{SPCKR}$ - $t_{SPCKF}$) / 2 | - | | |
| | RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | ($t_{Spcyc}$ - $t_{SPCKR}$ - $t_{SPCKF}$) / 2-3 | - | ns | |
| | | Slave | | ($t_{Spcyc}$ - $t_{SPCKR}$ - $t_{SPCKF}$) / 2 | - | | |
| | RSPCK clock rise/fall time | Output | $t_{SPCKR}$ $t_{SPCKF}$ | - | 5 | ns | |
| | | Input | | - | 1 | µs | |
| | Data input setup time | Master | $t_{SU}$ | 25 | - | ns | Figure 5.12 to Figure 5.15 |
| | | Slave | | 0 | - | | |
| | Data input hold time | Master | $t_H$ | 0 | - | ns | |
| | | Slave | | 20+2×$t_{Pcyc}$ | - | | |
| | SSL setup time | Master | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | 4 | - | $t_{Pcyc}$ | |
| | SSL hold time | Master | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | 4 | - | $t_{Pcyc}$ | |
| | Data output delay time | Master | $t_{OD}$ | - | 20 | ns | |
| | | Slave | | - | 3×$t_{Pcyc}$ +40 | | |
| | Data output hold time | Master | $t_{OH}$ | 0 | - | ns | |
| | | Slave | | 0 | - | | |
| | Successive transmission delay time | Master | $t_{TD}$ | $t_{SPcyc}$+2×$t_{Pcyc}$ | 8×$t_{SPcyc}$ +2×$t_{Pcyc}$ | ns | |
| | | Slave | | 4×$t_{Pcyc}$ | - | | |
| | MOSI, MISO rise/fall time | Output | $t_{DR}$ $t_{DF}$ | - | 15 | ns | Figure 5.12 to Figure 5.15 |
| | | Input | | - | 1 | µs | |
| | SSL rise/fall time | Output | $t_{SSLR}$ $t_{SSLF}$ | - | 15 | ns | |
| | | Input | | - | 1 | µs | |
| | Slave access time | | $t_{SA}$ | - | 4 | $t_{Pcyc}$ | Figure 5.12 to Figure 5.15 |
| | Slave output release time | | $t_{REL}$ | - | 3 | $t_{Pcyc}$ | |

Note: • Note 1: $t_{Pcyc}$: PCLK cycle

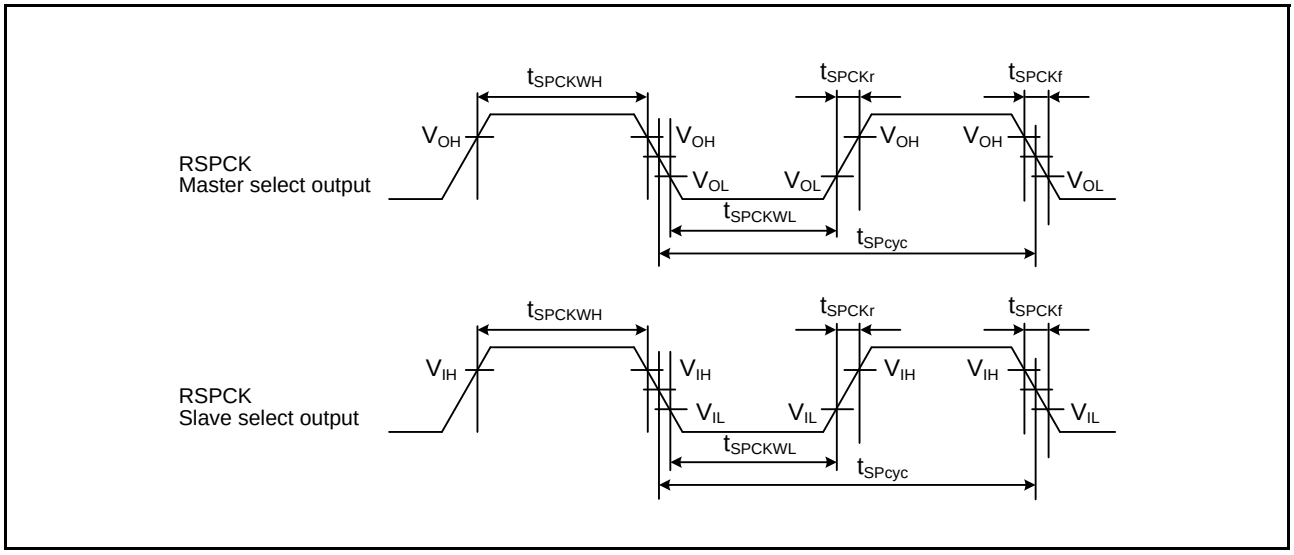



**Figure 5.11 RSPI Clock Timing**

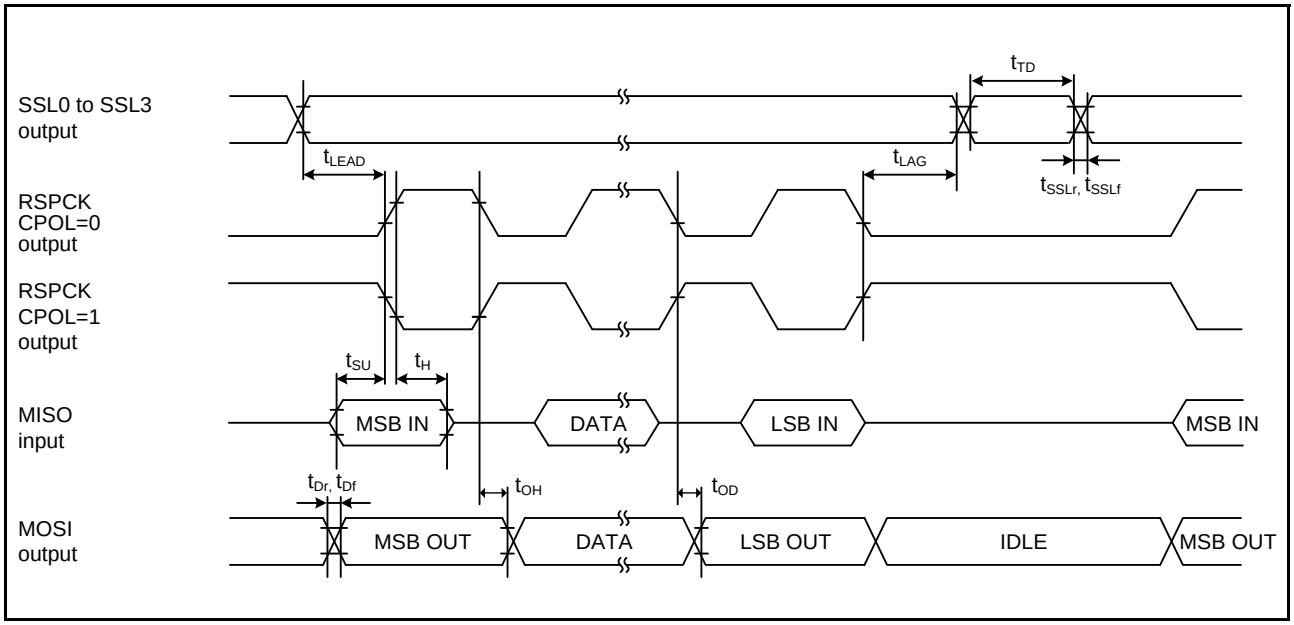



**Figure 5.12 RSPI Timing (Master, CPHA = 0)**

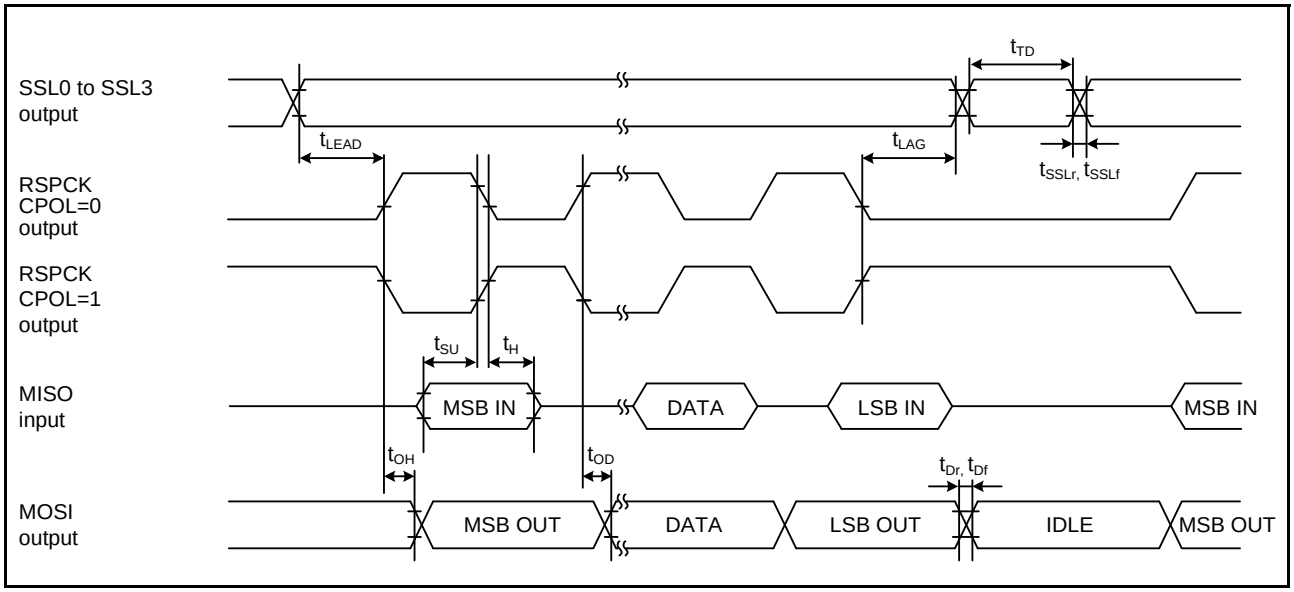



**Figure 5.13 RSPI Timing (Master, CPHA = 1)**

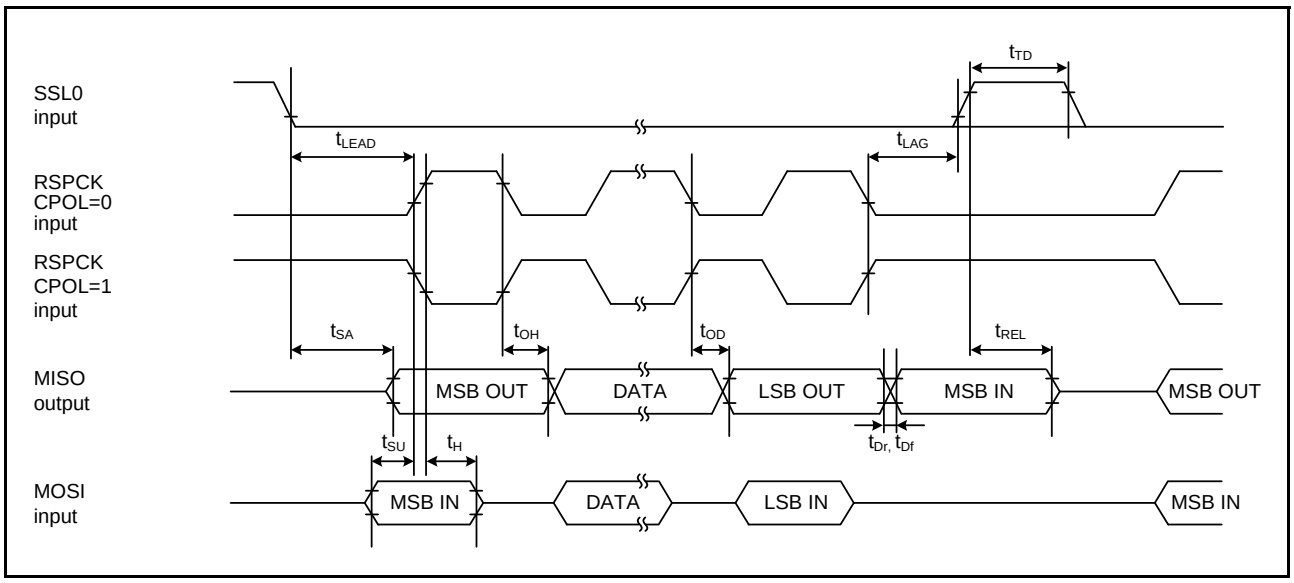



**Figure 5.14 RSPI Timing (Slave, CPHA = 0)**

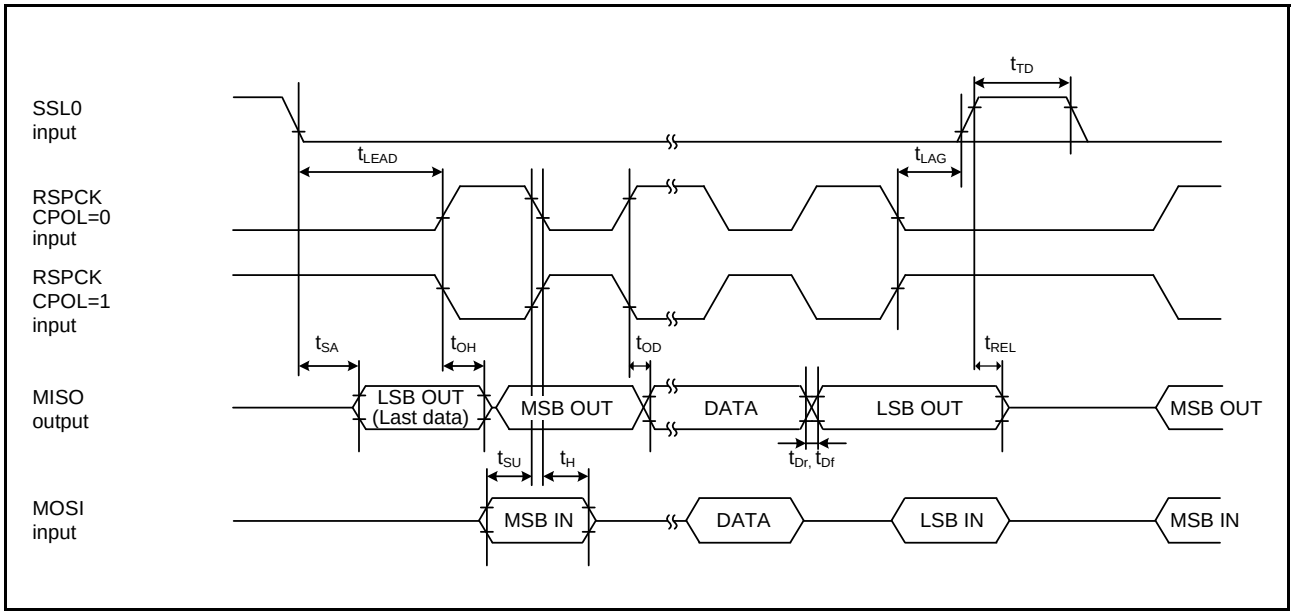



**Figure 5.15 RSPI Timing (Slave, CPHA = 1)**

**Table 5.12 Timing of On-Chip Peripheral Modules (4)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| MTU3 | Input capture input pulse width (single-edge setting) | $t_{TICW}$ | 3.0 | - | $t_{Icyc}$ | Figure 5.16 |
| | Input capture input pulse width (both-edge setting) | $t_{TICW}$ | 5.0 | - | $t_{Icyc}$ | |
| | Timer clock pulse width (single-edge setting) | $t_{TCKWH/L}$ | 3.0 | - | $t_{Icyc}$ | Figure 5.17 |
| | Timer clock pulse width (both-edge setting) | $t_{TCKWH/L}$ | 5.0 | - | $t_{Icyc}$ | |
| | Timer clock pulse width (phase coefficient mode) | $t_{TCKWH/L}$ | 5.0 | - | $t_{Icyc}$ | |
| GPT | Input capture input pulse width (single-edge setting) | $t_{GTICW}$ | 3.0 | - | $t_{Icyc}$ | Figure 5.18 |
| | Input capture input pulse width (both-edge setting) | $t_{GTICW}$ | 5.0 | - | $t_{Icyc}$ | |

Note: • $t_{Icyc}$: ICLK cycle

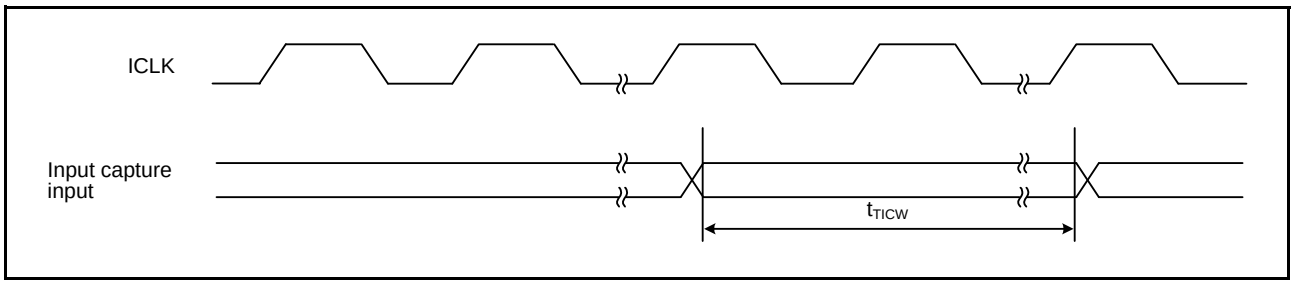



**Figure 5.16 MTU3 Input/Output Timing**

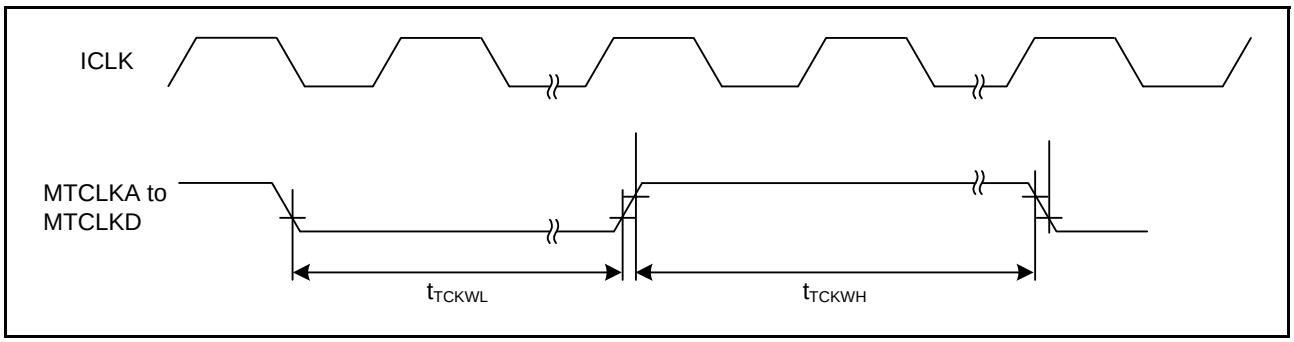



**Figure 5.17 MTU3 Clock Input Timing**

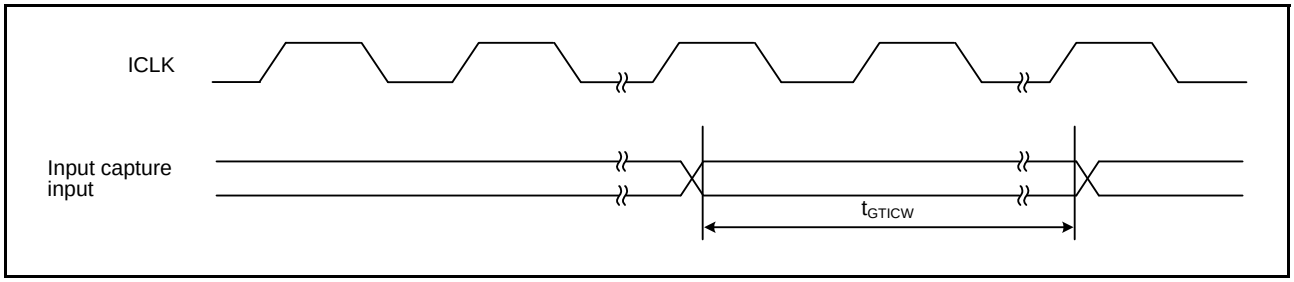



**Figure 5.18 GPT Input/Output Timing**

**Table 5.13 Timing of On-Chip Peripheral Modules (5)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| POE3 | POE# input pulse width | $t_{POEW}$ | 1.5 | - | $t_{Pcyc}$ | Figure 5.19 |

Note: • $t_{Pcyc}$: PCLK cycle

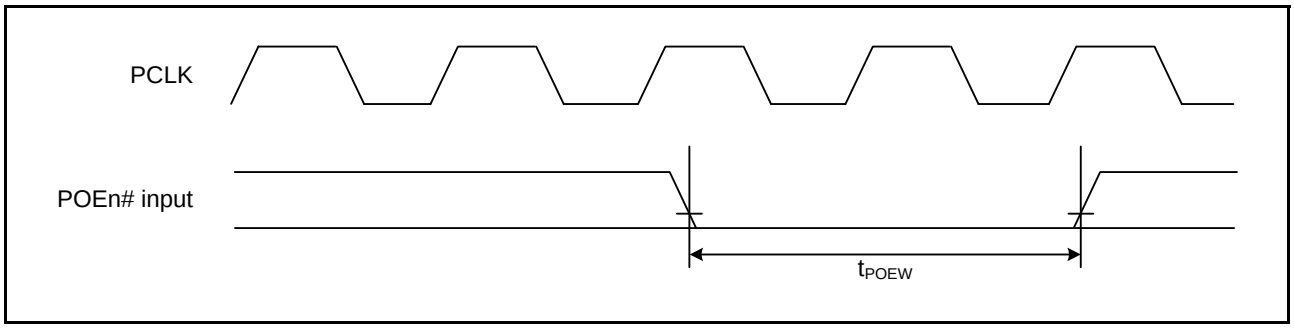



**Figure 5.19 POE3# Clock Timing**

## 5.3.4 Timing of PWM Delay Generation Circuit

**Table 5.14 Timing of the PWM Delay Generation Circuit**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V
AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr.

| Item | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | — | 312.5 | — | ps | ICLK = 100 MHz |
| DNL*1 | — | ±2.0 | — | LSB | |

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

## 5.4 A/D Conversion Characteristics

**Table 5.15 10-Bit A/D Conversion Characteristics**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 10 | 10 | 10 | Bit | |
| Conversion time*1<br>(AD clock = 25-MHz operation) | 2.0 | - | - | μs | Sampling 25 states |
| Analog input capacitance | - | - | 4 | pF | |
| Integral nonlinearity error | - | - | ±3.0 | LSB | |
| Offset error | - | - | ±3.0 | LSB | |
| Full-scale error | - | - | ±3.0 | LSB | |
| Quantization error | - | ±0.5 | - | LSB | |
| Absolute accuracy | - | - | ±4.0 | LSB | |
| Permissible signal source impedance | - | - | 1.0 | kΩ | |

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3.

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 10 | 10 | 10 | Bit | |
| Conversion time*1<br>(AD clock = 50-MHz operation) | 1.0 | - | - | μs | Sampling 25 states |
| Analog input capacitance | - | - | 4 | pF | |
| Integral nonlinearity error | - | - | ±3.0 | LSB | |
| Offset error | - | - | ±3.0 | LSB | |
| Full-scale error | - | - | ±3.0 | LSB | |
| Quantization error | - | ±0.5 | - | LSB | |
| Absolute accuracy | - | - | ±4.0 | LSB | |
| Permissible signal source impedance | - | - | 1.0 | kΩ | |

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

**Table 5.16 12-Bit A/D Conversion Characteristics**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr, ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 12 | 12 | 12 | Bit | |
| Conversion time*1 (AD clock = 25-MHz operation) | | 2.0 | - | - | µs | Sampling 20 states |
| Analog input capacitance | | - | - | 6 | pF | |
| Integral nonlinearity error | | - | - | ±4.0 | LSB | |
| Offset error | | - | - | ±7.5 | LSB | |
| Full-scale error | | - | - | ±7.5 | LSB | |
| Quantization error | | - | ±0.5 | - | LSB | |
| Absolute accuracy | When a sample-and-hold circuit is in use | - | - | ±8.0 | LSB | AVin = 0.25 to $AV_{REFH}$ - 0.25 |
| | When a sample-and-hold circuit is not in use | - | - | ±8.0 | LSB | AVin = $AV_{REFL}$ to $AV_{REFH}$ |
| Permissible signal source impedance | | - | - | 3.0 | kΩ | |

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3. ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz.

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 12 | 12 | 12 | Bit | |
| Conversion time*1 (AD clock = 25-MHz operation) | | 1.0 | - | - | µs | Sampling 20 states |
| Analog input capacitance | | - | - | 6 | pF | |
| Integral nonlinearity error | | - | - | ±4.0 | LSB | |
| Offset error | | - | - | ±7.5 | LSB | |
| Full-scale error | | - | - | ±7.5 | LSB | |
| Quantization error | | - | ±0.5 | - | LSB | |
| Absolute accuracy | When a sample-and-hold circuit is in use | - | - | ±8.0 | LSB | AVin = 0.25 to $AV_{REFH}$ - 0.25 |
| | When a sample-and-hold circuit is not in use | - | - | ±8.0 | LSB | AVin = $AV_{REFL}$ to $AV_{REFH}$ |
| Permissible signal source impedance | | - | - | 3.0 | kΩ | |

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

**Table 5.17 Characteristics of the Programmable Gain Amplifier**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Analog input capacitance | | Cin | - | - | 6 | pF | |
| Input offset voltage | | Voff | - | - | 8 | mV | |
| Input voltage range (Vin) | Gain × 2.000 | Vin | 0.050 x AVcc | - | 0.450 x AVcc | V | |
| | Gain × 2.500 | | 0.047 x AVcc | - | 0.360 x AVcc | | |
| | Gain × 3.077 | | 0.045 x AVcc | - | 0.292 x AVcc | | |
| | Gain × 3.636 | | 0.042 x AVcc | - | 0.247 x AVcc | | |
| | Gain × 4.000 | | 0.040 x AVcc | - | 0.212 x AVcc | | |
| | Gain × 4.444 | | 0.036 x AVcc | - | 0.191 x AVcc | | |
| | Gain × 5.000 | | 0.033 x AVcc | - | 0.170 x AVcc | | |
| | Gain × 5.714 | | 0.031 x AVcc | - | 0.148 x AVcc | | |
| | Gain × 6.667 | | 0.029 x AVcc | - | 0.127 x AVcc | | |
| | Gain × 10.000 | | 0.025 x AVcc | - | 0.08 x AVcc | | |
| | Gain × 13.333 | | 0.023 x AVcc | - | 0.06 x AVcc | | |
| Slew rate | | SR | 10 | - | - | V/µs | |
| Gain error | Gain × 2.000 | - | - | - | 1 | % | |
| | Gain × 2.500 | | - | - | 1 | | |
| | Gain × 3.077 | | - | - | 1 | | |
| | Gain × 3.636 | | - | - | 1.5 | | |
| | Gain × 4.000 | | - | - | 1.5 | | |
| | Gain × 4.444 | | - | - | 2 | | |
| | Gain × 5.000 | | - | - | 2 | | |
| | Gain × 5.714 | | - | - | 2 | | |
| | Gain × 6.667 | | - | - | 3 | | |
| | Gain × 10.000 | | - | - | 4 | | |
| | Gain × 13.333 | | - | - | 4 | | |

**Table 5.18 Comparator Characteristics**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Analog input capacitance | Cin | - | - | 6 | pF | |
| REFH pin offset voltage | Voff | - | - | 5 | mV | |
| REFL pin offset voltage | | - | - | 5 | mV | |
| REFH input voltage range | Vin | 1.7 | - | AVcc – 0.3 | V | |
| REFL input voltage range | | 0.3 | - | AVcc – 1.7 | V | |
| REFH reply time | tCR | - | - | 1 | µs | |
| REFL reply time | tCF | - | - | 1 | µs | |

## 5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

**Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 and 2.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | $V_{POR}$ | 2.48 | 2.60 | 2.72 | V | Figure 5.20 |
| | Voltage detection circuit (LVD) | Vdet1 | 2.68 | 2.80 | 2.92 | | Figure 5.21 |
| | | Vdet2 | 2.98 | 3.10 | 3.22 | | Figure 5.22 |
| Internal reset time | | $t_{POR}$ | 20 | 35 | 50 | ms | Figure 5.21 and Figure 5.22 |
| Min. VCC down time*1 | | $t_{VOFF}$ | 200 | - | - | us | Figure 5.20 to Figure 5.22 |
| Reply delay time | | tdet | - | - | 200 | us | |

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | $V_{POR}$ | 3.70 | 3.90 | 4.10 | V | Figure 5.20 |
| | Voltage detection circuit (LVD) | Vdet1 | 3.95 | 4.15 | 4.35 | | Figure 5.21 |
| | | Vdet2 | 4.40 | 4.60 | 4.80 | | Figure 5.22 |
| Internal reset time | | $t_{POR}$ | 20 | 35 | 50 | ms | Figure 5.21 and Figure 5.22 |
| Min. VCC down time*1 | | $t_{VOFF}$ | 200 | - | - | us | Figure 5.20 to Figure 5.22 |
| Reply delay time | | tdet | - | - | 200 | us | |

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for the POR/ LVD.

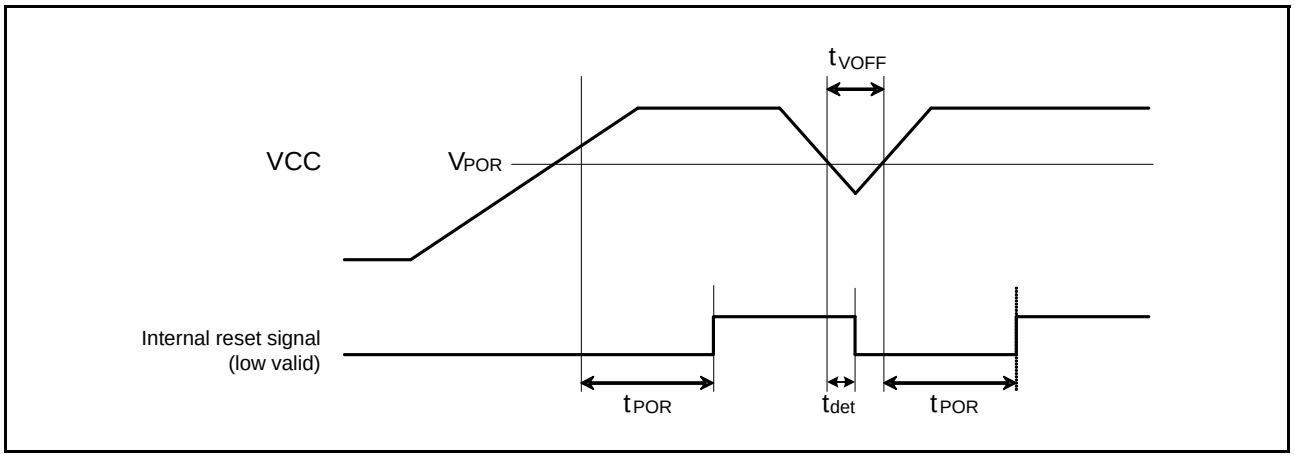



**Figure 5.20 Power-on Reset Timing**

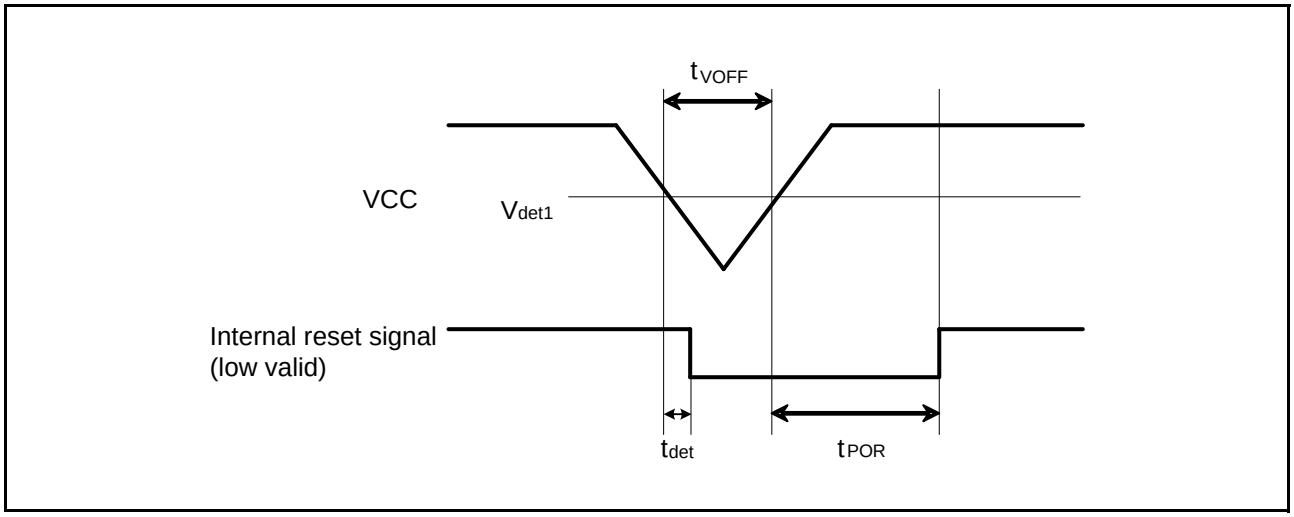



**Figure 5.21 Voltage Detection Circuit Timing (Vdet1)**

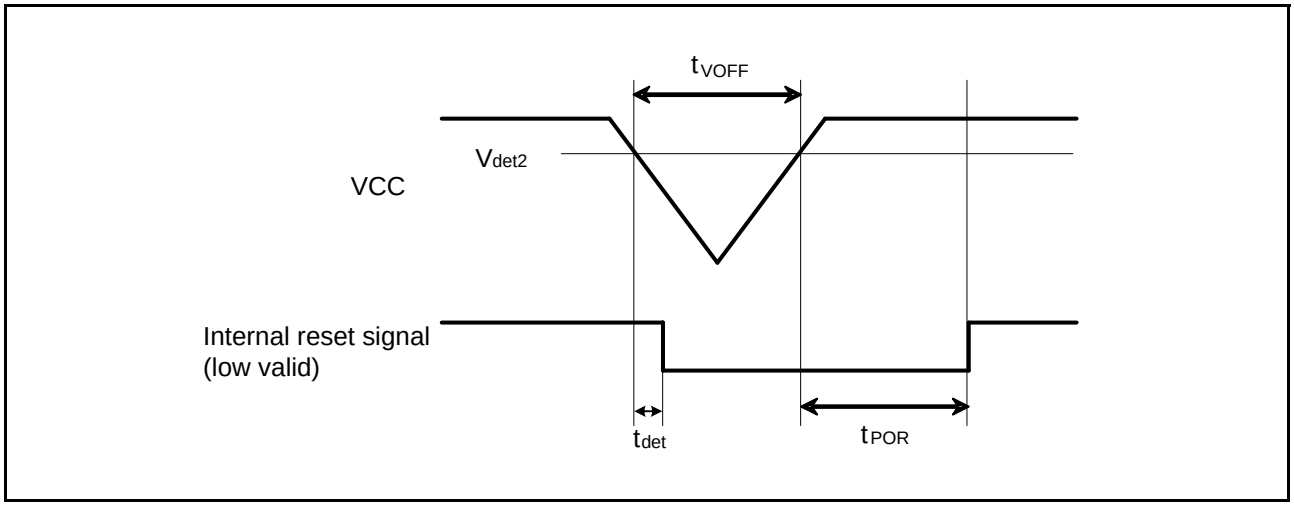



**Figure 5.22 Voltage Detection Circuit Timing (Vdet2)**

## 5.6 Oscillation Stop Detection Timing

**Table 5.20 Oscillation Stop Detection Circuit Characteristics**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | tdr | - | - | 1.0 | ms | Figure 5.23 |
| Internal oscillation frequency when oscillation stop is detected | $f_{MAIN}$ | 0.5 | - | 7.0 | MHz | |

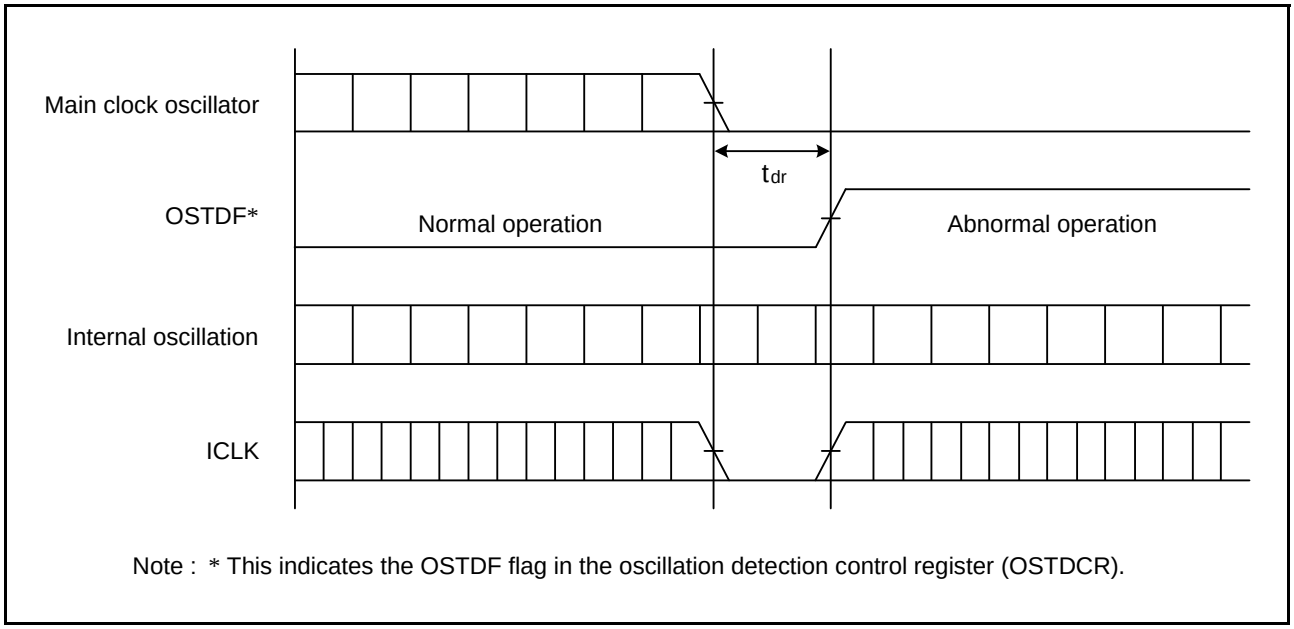



**Figure 5.23 Oscillation Stop Detection Timing**

## 5.7 ROM (Flash Memory for Code Storage) Characteristics

**Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Rewrite/erase cycle*1 | $N_{PEC}$ | 1000 | — | — | Times | |
| Data hold time | $t_{DRP}$ | 30*2 | — | — | Year | Ta = +85C° |

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

**Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Programming time | 256 bytes | $t_{P256}$ | — | 2 | 12 | ms | PCLK = 50 MHz<br>$N_{PEC} \leq 100$ |
| | 4 Kbytes | $t_{P4K}$ | — | 23 | 50 | ms | |
| | 16 Kbytes | $t_{P16K}$ | — | 90 | 200 | ms | |
| | 256 byte | $t_{P256}$ | — | 2.4 | 14.4 | ms | PCLK = 50 MHz<br>$N_{PEC} > 100$ |
| | 4 Kbytes | $t_{P4K}$ | — | 27.6 | 60 | ms | |
| | 16 Kbytes | $t_{P16K}$ | — | 108 | 240 | ms | |
| Erasure time | 4 Kbytes | $t_{E4K}$ | — | 25 | 60 | ms | PCLK = 50 MHz<br>$N_{PEC} \leq 100$ |
| | 16 Kbytes | $t_{E16K}$ | — | 100 | 240 | ms | |
| | 4 Kbytes | $t_{E4K}$ | — | 30 | 72 | ms | PCLK = 50 MHz<br>$N_{PEC} > 100$ |
| | 16 Kbytes | $t_{E16K}$ | — | 120 | 288 | ms | |
| Suspend delay time during writing | | $t_{SPD}$ | — | — | 120 | µs | Figure 5.24<br>PCLK = 50 MHz |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 120 | µs | |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | ms | |
| Suspend delay time during erasing (in erasure priority mode) | | $t_{SEED}$ | — | — | 1.7 | ms | |

## 5.8 Data Flash (Flash Memory for Data Storage) Characteristics

**Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Rewrite/erase cycle*1 | $N_{DPEC}$ | 30000 | — | — | Times | |
| Data hold time | $t_{DDRP}$ | 30*2 | — | — | Year | Ta = +85C° |

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

**Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2)**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Programming time | 8 bytes | $t_{DP8}$ | — | 0.4 | 2 | ms | PCLK = 50 MHz |
| | 128 bytes | $t_{DP128}$ | — | 1 | 5 | ms | |
| Erasure time | 2 Kbytes | $t_{DE2K}$ | — | 70 | 250 | ms | PCLK = 50 MHz |
| Blank check time | 8 bytes | $t_{DBC8}$ | — | — | 30 | µs | PCLK = 50 MHz |
| | 2 Kbytes | $t_{DBC2K}$ | — | — | 0.7 | ms | |
| Suspend delay time during writing | | $t_{DSPD}$ | — | — | 120 | µs | Figure 5.24 PCLK = 50 MHz |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{DSESD1}$ | — | — | 120 | µs | |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{DSESD2}$ | — | — | 1.7 | ms | |
| Suspend delay time during erasing (in erasure priority mode) | | $t_{DSEED}$ | — | — | 1.7 | ms | |

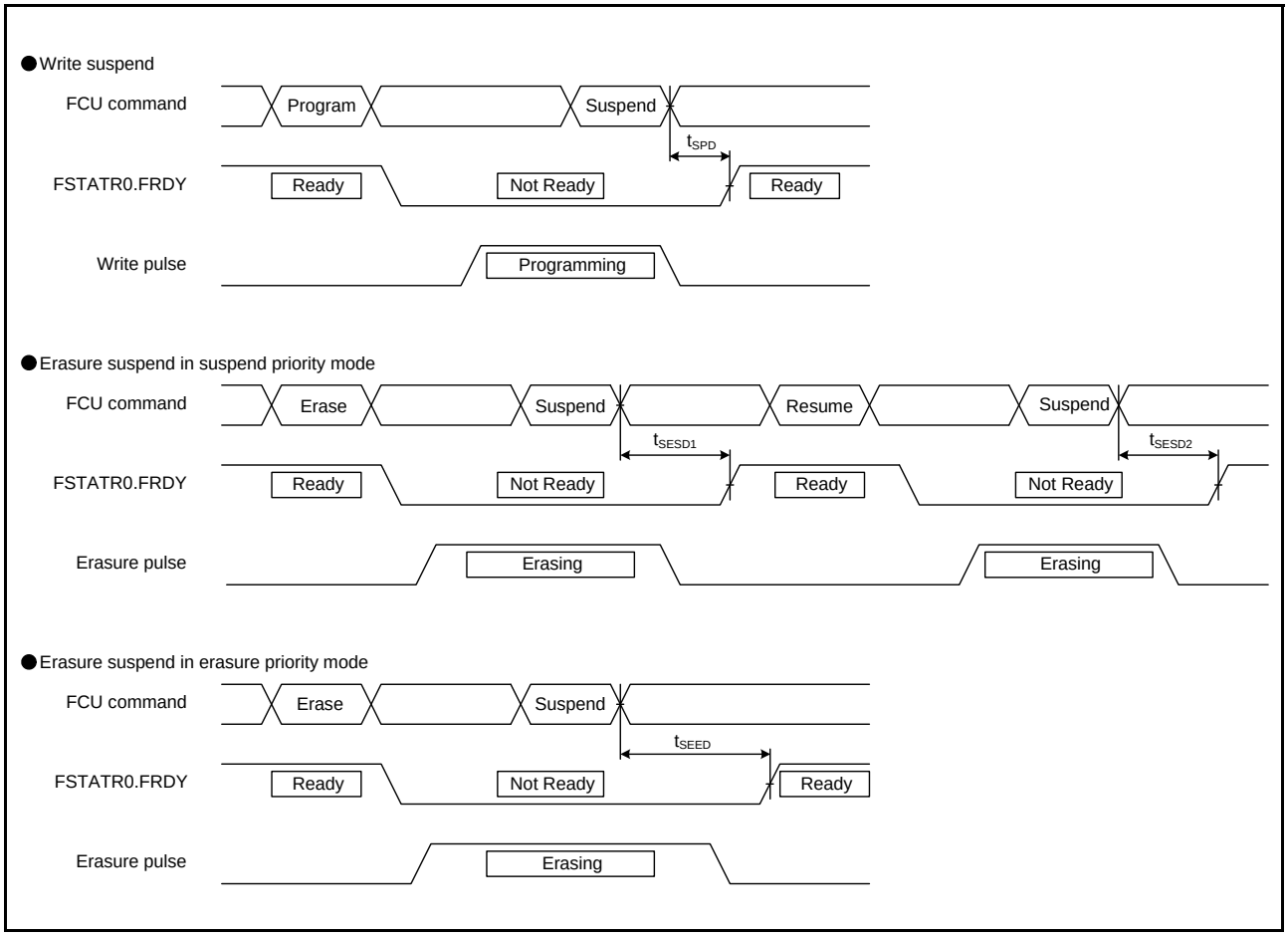
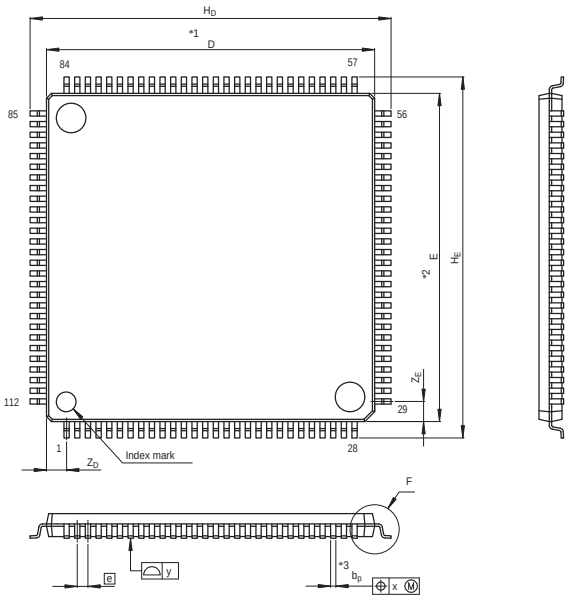


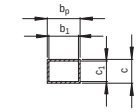

**Figure 5.24 Flash Memory Write/Erase Suspend Timing**

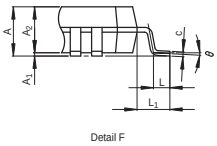
# Appendix 1.Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP112-20x20-0.65 | PLQP0112JA-A | FP-112E / FP-112EV | 1.2g |





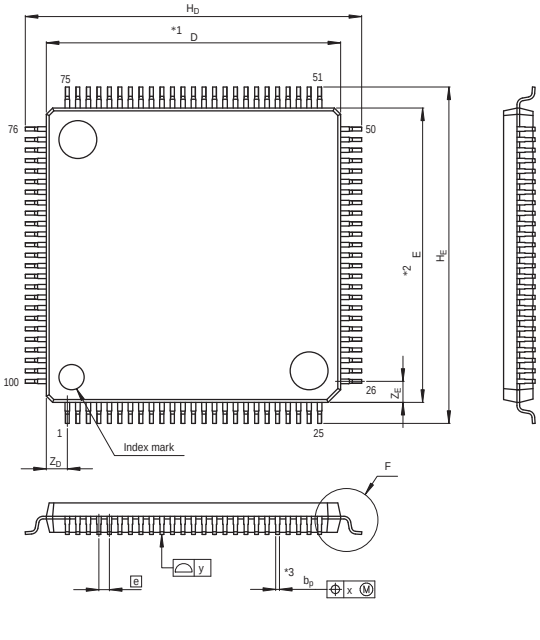



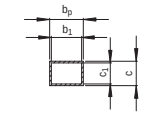

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

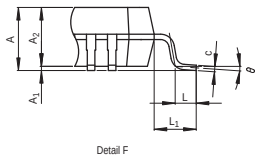
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.27 | 0.32 | 0.37 |
| $b_1$ | — | 0.30 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.225 | — |
| $Z_E$ | — | 1.225 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure A 112-Pin LQFP (PLQP0112JA-A) Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g |



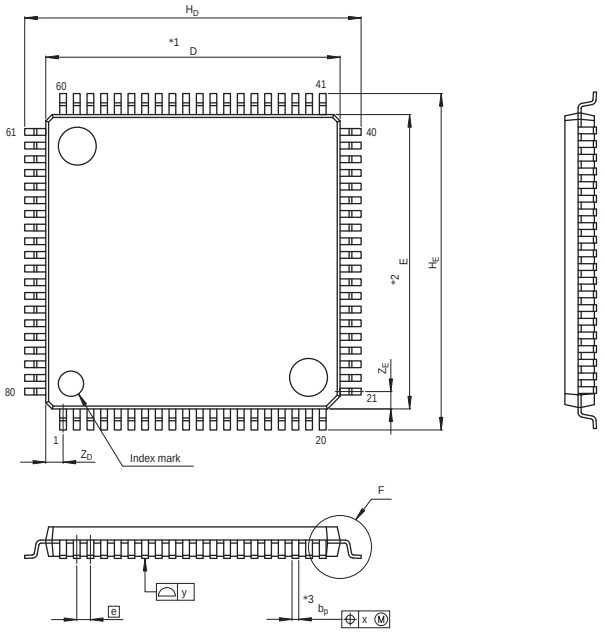




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

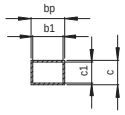
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure B 100-Pin LQFP (PLQP0100KB-A) Package Dimensions

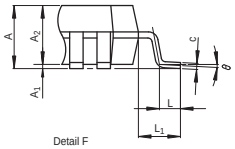
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP80-14x14-0.65 | PLQP0080JA-A | FP-80W / FP-80WV | 0.6g |






Terminal cross section



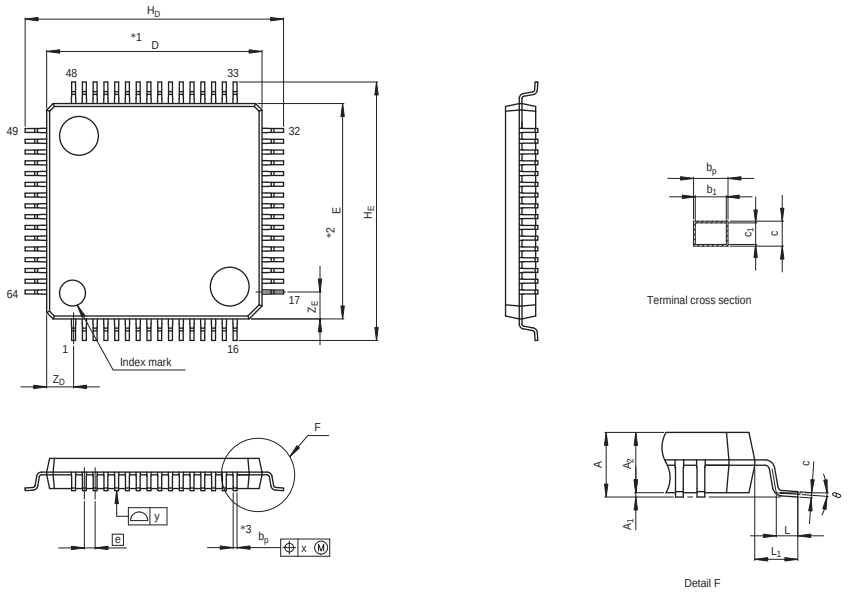

Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.27 | 0.32 | 0.37 |
| $b_1$ | — | 0.30 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.825 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure C 80-Pin LQFP (PLQP0080JA-A) Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |

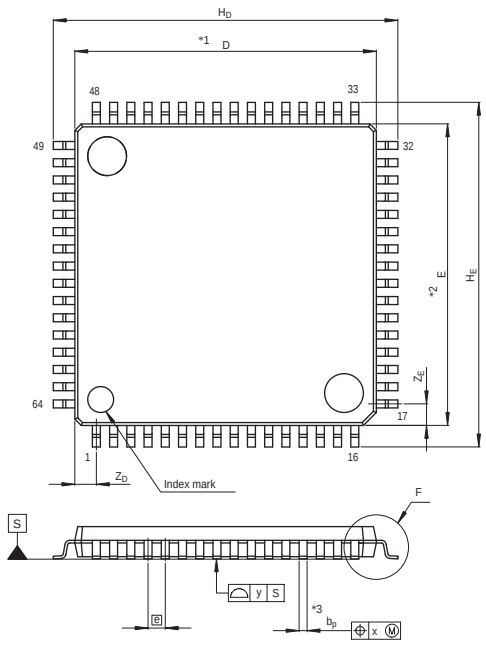



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

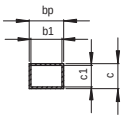
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions

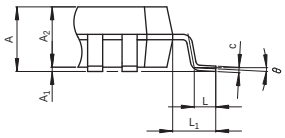
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-14x14-0.80 | PLQP0064GA-A | 64P6U-A/ — | 0.7g |






Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.32 | 0.37 | 0.42 |
| $b_1$ | — | 0.35 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.8 | — |
| x | — | — | 0.20 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.0 | — |

Figure E 64-Pin LQFP (PLQP0064GA-A) Package Dimensions

# REVISION HISTORY — RX62T Group, RX62G Group Datasheet

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Apr 20, 2011 | — | First edition issued |
| 1.30 | May 22, 2013 | 1 | Features, Package lineup, added |
| | | | 1. Overview |
| | | 2 | Table 1.1 Outline of Specifications (1/5) Description of CPU, added |
| | | 3 | Table 1.1 Outline of Specifications (2/5) Description of Programmable I/O ports, changed |
| | | 6 | Table 1.1 Outline of Specifications (5/5), 64-pin packaged, added |
| | | 7 | Table 1.2 Functions of RX62T Group Products, 64-pin package, and MTU3/GPT complementary PWM pins added |
| | | 8 | Table 1.3 List of Products, 64-pin package part number, changed |
| | | 9 | Figure 1.1 How to Read the Product Part No., 64-pin package part number, changed |
| | | 9 | Figure 1.1 How to Read the Product Part No., 5-V version, two-motor control supported, added |
| | | 10 | Figure 1.2 Block Diagram, changed |
| | | 14 | Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-motor Control Supported), added |
| | | 15 | Figure 1.7 Pin Assignment of the 64-Pin LQFP, Figure PLQP0064GA-A, added |
| | | 25 to 27 | Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) , added |
| | | 30 to 33 | Table 1.9 Pin Functions, changed |
| | | | 4. I/O Register |
| | | 38to 61 | Table 4.1 List of I/O Registers (Address Order), MPU, added |
| | | 47 | Table 4.1 List of I/O Registers (Address Order) TMOCNTL, TMOCNTU register, added |
| | | 57 | Table 4.1 List of I/O Registers (Address Order), GTSWP register, added |
| | | | 5. Electrical Characteristics |
| | | 62 | Table 5.1 Absolute Maximum Ratings, note changed |
| | | 64 | Table 5.2 DC Characteristics (1) (2/3) Test Conditions of P90 to P95, changed |
| | | 66 | Table 5.3 DC Characteristics (2), note changed |
| | | 67 | Table 5.4 Permissible Output Currents, note changed |
| | | 72 | Table 5.7 Control Signal Timing, notes changed |
| | | 73 | Table 5.8 Timing of On-Chip Peripheral Modules (1), changed |
| | | | Appendix 1.Package Dimensions |
| | | 96 | Figure E 64-Pin LQFP (PLQP0064GA-A), added |
| 2.00 | Jan 10, 2014 | 1 | Features, changed |
| | | | 1. Overview |
| | | 2 to 6 | Table 1.1 Outline of Specifications, changed; Note 1, added |
| | | 7, 8 | Table 1.2 Functions of RX62T Group and RX62G Group Products, changed |
| | | 9, 10 | Table 1.3 List of Products, changed; Note 1, added |
| | | 11 | Figure 1.1 How to Read the Product Part No., changed |
| | | 15 | Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version), added |
| | | 27 to 29 | Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF), added |
| | | | 4. I/O Registers |
| | | 43 to 67 | Table 4.1 List of I/O Registers (Address Order), changed |
| | | 68 to 97 | Table 4.2 List of I/O Registers (Bit Order), changed |
| | | | 5. Electrical Characteristics |
| | | — | Conditions in the table, change to Ta = -40 to +105°C from Ta = -40 to +85°C. |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Jan 10, 2014 | 98 | Table 5.1 Absolute Maximum Ratings, changed |
| | | 102 | Table 5.3 DC Characteristics (2): Note 3, changed |
| | | 103 | Table 5.5 Permissible Power Consumption, added |
| | | 117 | 5.3.4 Timing of PWM Delay Generation Circuit, added |
| | | 117 | Table 5.14 Timing of the PWM Delay Generation Circuit, added |
| | | 120 | Table 5.17 Characteristics of the Programmable Gain Amplifier, changed |
| | | 125 | Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1), changed |
| | | 125 | Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2), added |
| | | 126 | Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1), changed |
| | | 126 | Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2), added |

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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