NB3V60113GV3

1.8 V 12.288 MHz OmniClock Generator with Single Ended (LVCMOS) Output

The NB3V60113GV3, which is a member of the OmniClock family, is a low power PLL−based clock generator. The device accepts a 6.144 MHz single ended (LVCMOS) reference clock as input. It generates one single ended (LVCMOS) output of 12.288 MHz. The device can be powered down using the Power Down pin (PD#).

Features

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply: 1.8 V ± 0.1 V
- I/O Standards
  - Input: 6.144 MHz Reference Clock (LVCMOS)
  - Output: 12.288 MHz (LVCMOS)
- Output Drive Current for Single Ended Output: 8 mA
- Power Saving Mode through Power Down Pin
- Temperature Range −40°C to 85°C
- Packaged in 8−Pin WDFN
- These are Pb−Free Devices

Typical Application

- Audio Systems (Lightning Audio Module)

ON Semiconductor®

www.onsemi.com



WDFN8
CASE 511AT

MARKING DIAGRAM



V3 = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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BLOCK DIAGRAM

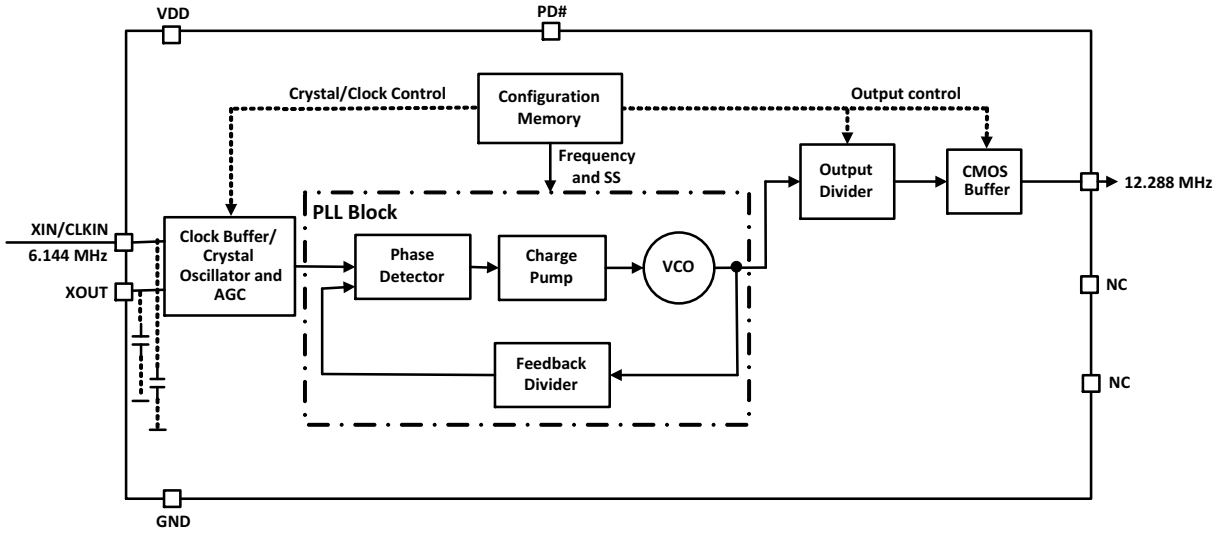


Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

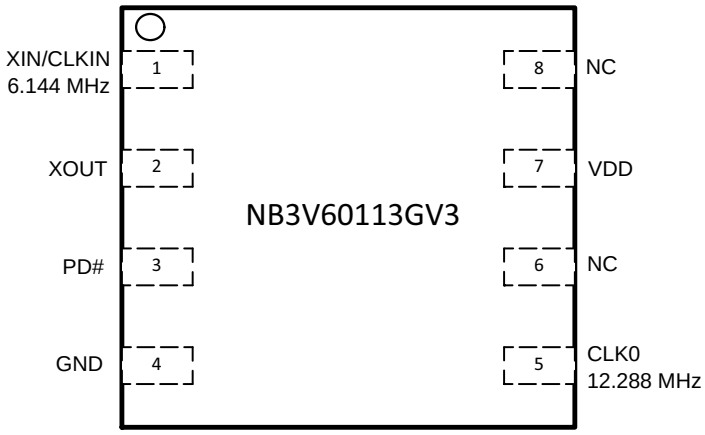


Figure 2. Pin Connections (Top View) – WDFN8

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	XIN/CLKIN	Input	6.144 MHz single−ended external reference input clock (LVCMOS)
2	XOUT	Output	Crystal output. Float this pin when external reference clock is connected at XIN
3	PD#	Input	Asynchronous LVCMOS input. Active Low Master Reset to disable the device and set outputs Low. Internal pull−down resistor. This pin needs to be pulled High for normal operation of the chip.
4	GND	Ground	Power supply ground
5	CLK0	Output	12.288 MHz Single−ended (LVCMOS) output
6	NC	−	No Connection. Not to be connected to any circuit
7	VDD	Power	1.8 V Power Supply
8	NC	−	No Connection. Not to be connected to any circuit

Table 2. POWER DOWN FUNCTION TABLE

PD#	Function
0	Device Powered Down
1	Device Powered Up

NOTE: PD# has internal pull down resistor.

Table 3. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model	2 kV
Internal Input Default State Pull up/ down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	130 k
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter		Rating	Unit
VDD	Positive power supply with respect to Ground		−0.5 to +4.6	V
V_I	Input Voltage with respect to chip ground		−0.5 to VDD + 0.5	V
T_A	Operating Ambient Temperature Range (Industrial Grade)		−40 to +85	°C
T_{STG}	Storage temperature		−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 sec)		265	°C
θ_{JA}	Thermal Resistance (Junction−to−ambient) (Note 3)	0 lfpm 500 lfpm	129 84	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−case)		35 to 40	°C/W
T_J	Junction temperature		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power). ESD51.7 type board. Back side Copper heat spreader area 100 sq mm, 2 oz (0.070 mm) copper thickness.

Table 5. RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Core Power Supply Voltage	1.8 V operation	1.7	1.8	1.9	V
CL	Clock output load capacitance for LVCMOS clock				15	pF
fclkin	Reference Clock Frequency	Single ended Clock input (LVCMOS)		6.144		MHz
C_X	XIN / XOUT pin stray Capacitance			4.5		pF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 1.8 V ± 0.1 V; GND = 0 V, T_A = −40°C to +85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD_1.8\ V}$	Power Supply current	fout = 12.288 MHz		13		mA
I_{PD}	Power Down Supply Current	PD# is Low to make all outputs OFF			20	μA
V_{IH}	Input HIGH Voltage	Pin XIN/CLKIN	0.65 V_{DD}		V_{DD}	V
		Pin PD#	0.85 V_{DD}		V_{DD}	
V_{IL}	Input LOW Voltage	Pin XIN/CLKIN	0		0.35 V_{DD}	V
		Pin PD#	0		0.15 V_{DD}	
Cin	Input Capacitance	Pin PD#		4	6	pF
LVCMOS OUTPUT						
V_{OH}	Output HIGH Voltage	V_{DD} = 1.8 V I_{OH} = 8 mA	0.75*V_{DD}			V
V_{OL}	Output LOW Voltage	V_{DD} = 1.8 V I_{OL} = 8 mA			0.25*V_{DD}	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 7. AC ELECTRICAL CHARACTERISTICS (V_{DD} = 1.8 V ± 0.1 V, GND = 0 V, T_A = −40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fout	Single Ended Output Frequency			12.288		MHz
t_{PU}	Stabilization time from Power−up	V_{DD} = 1.8 V		3.0		ms
t_{PD}	Stabilization time from Power Down	Time from falling edge on PD# pin to tri−stated outputs (Asynchronous)		3.0		ms
Eppm	Synthesis Error			0		ppm
SINGLE ENDED OUTPUT (V_{DD} = 1.8 V ± 0.1 V; T_A = −40°C to 85°C)						
$t_{JITTER−1.8\ V}$	Period Jitter Peak−to−Peak	Configuration Dependent		200		ps
	Cycle−Cycle Peak Jitter	Configuration Dependent		200		
t_r / $t_{f\ 1.8\ V}$	Rise/Fall Time	Measured between 20% to 80% with 15 pF load, f_{out} = 12.288 MHz, V_{DD} = 1.8 V		1		ns
t_{DC}	Output Clock Duty Cycle	V_{DD} = 1.8 V; Duty Cycle of Ref clock is 50% PLL Clock	45	50	55	%

PARAMETER MEASUREMENT TEST CIRCUIT

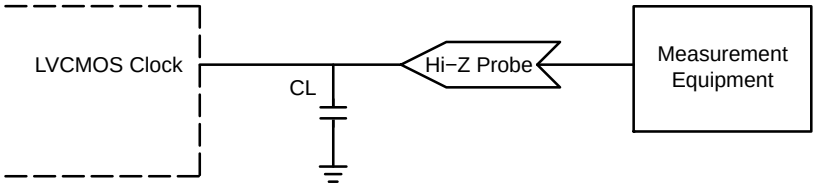


Figure 3. LVCMOS Clock Parameter Measurement

TIMING MEASUREMENT DEFINITIONS

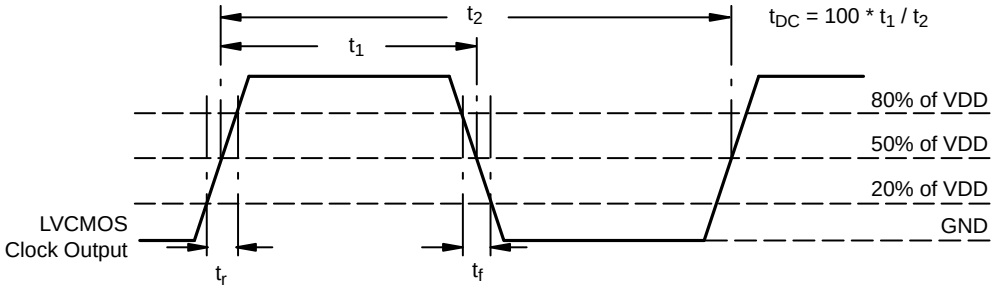


Figure 4. LVCMOS Measurement for AC Parameters

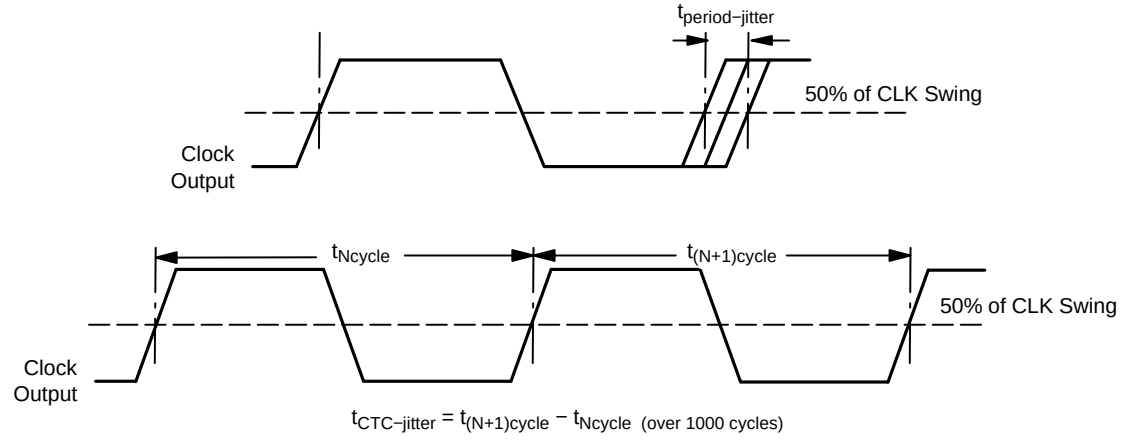


Figure 5. Period and Cycle−Cycle Jitter Measurement

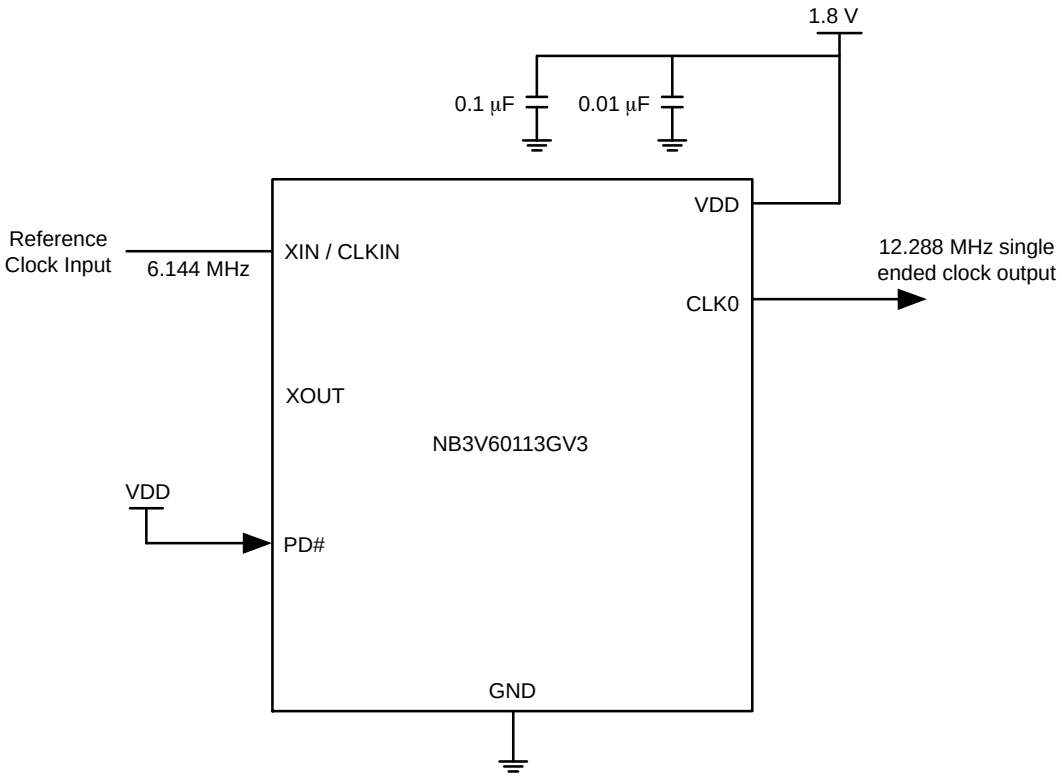


Figure 6. Typical Application Setup

ORDERING INFORMATION

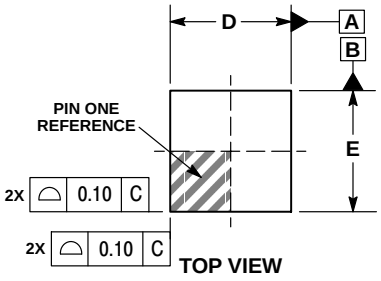
Device	Case	Package	Shipping†
NB3V60113GV3MTR2G	511AT	DFN−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

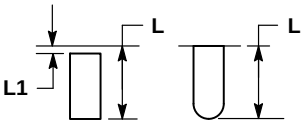
NOTE: Please contact your ON Semiconductor sales representative for information on un−programmed versions of this device.

PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511AT
ISSUE O



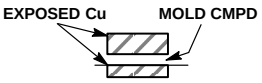
TOP VIEW



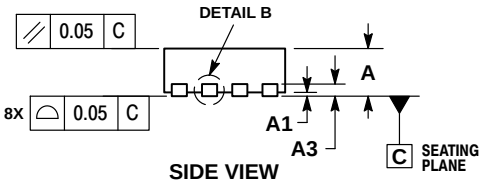
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

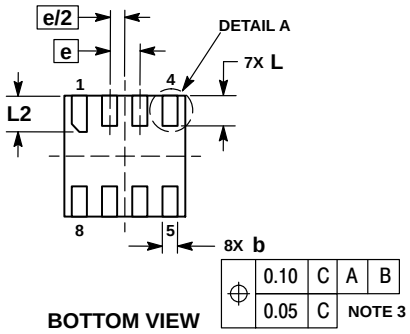
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70



DETAIL B
ALTERNATE CONSTRUCTIONS

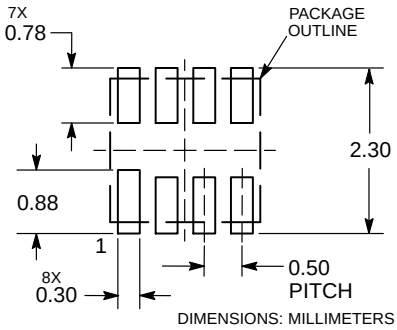


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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