LMH6502 Wideband, Low Power, Linear-in-dB Variable Gain Amplifier

Check for Samples: LMH6502

FEATURES

- **V_S = ±5V, T_A = 25°C, R_F = 1kΩ, R_G = 174Ω, R_L = 100Ω, A_V = $A_{V(MAX)}$ = 10 Typical Values Unless Specified.**
- **-3dB BW: 130MHz**
- **Gain Control BW: 100MHz**
- **Adjustment Range (Typical Over Temp): 70dB**
- **Gain Matching (Limit): ±0.6dB**
- **Slew Rate: 1800V/µs**
- **Supply Current (No Load): 27mA**
- **Linear Output Current: ±75mA**
- **Output Voltage (R_L = 100Ω): ±3.2V**
- **Input Voltage Noise: 7.7nV/√Hz**
- **Input Current Noise: 2.4pA/√Hz**
- **THD (20MHz, R_L = 100Ω, V_O = $2V_{PP}$): −53dBc**
- **Replacement for CLC520**

APPLICATIONS

- **Variable Attenuator**
- **AGC**
- **Voltage Controller Filter**
- **Video Imaging Processing**

DESCRIPTION

The LMH™6502 is a wideband DC coupled differential input voltage controlled gain stage followed by a high-speed current feedback Op Amp which can directly drive a low impedance load. Gain adjustment range is more than 70dB for up to 10MHz.

Maximum gain is set by external components and the gain can be reduced all the way to cut-off. Power consumption is 300mW with a speed of 130MHz. Output referred DC offset voltage is less than 350mV over the entire gain control voltage range. Device-to-device Gain matching is within ±0.6dB at maximum gain. Furthermore, gain at any V_G is tested and the tolerance is ensured. The output current feedback Op Amp allows high frequency large signals (Slew Rate = 1800V/µs) and can also drive heavy load current (75mA). Differential inputs allow common mode rejection in low level amplification or in applications where signals are carried over relatively long wires. For single ended operation, the unused input can easily be tied to ground (or to a virtual half-supply in single supply application). Inverting or non-inverting gains could be obtained by choosing one input polarity or the other.

To provide ease of use when working with a single supply, V_G range is set to be from 0V to +2V relative to pin 11 potential (ground pin). In single supply operation, this ground pin is tied to a "virtual" half supply.

LMH6502 gain control is linear in dB for a large portion of the total gain control range. This makes the device suitable for AGC circuits among other applications. For linear gain control applications, see the LMH6503 datasheet. The LMH6502 is available in the SOIC and TSSOP package.

Typical Application

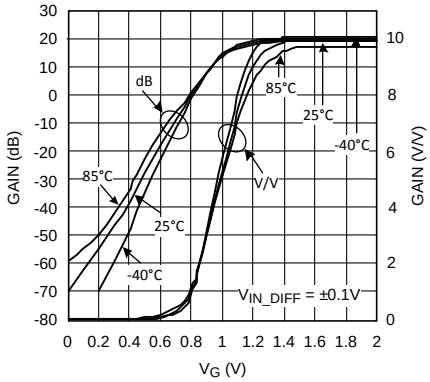


Figure 1. Gain vs. V_G for Various Temperature

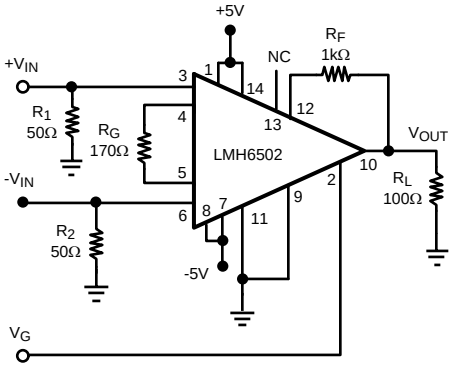


Figure 2. A_{VMAX} = 10V/V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3):	Human Body	2KV
	Machine Model	200V
Input Current		±10mA
V_{IN} Differential		±(V^+ -V^-)
Output Current		120mA(4)
Supply Voltages (V^+ - V^-)		12.6V
Voltage at Input/ Output pins		V^+ +0.8V,V^- - 0.8V
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+150°C
Soldering Information:	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specific specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations or value specified, whichever is lower.

Operating Ratings(1)

Supply Voltages (V^+ - V^-)			5V to 12V
Temperature Range			−40°C to +85°C
Thermal Resistance:	14-Pin SOIC	(θ_{JC})	45°C/W
		(θ_{JA})	138°C/W
	14-Pin TSSOP	(θ_{JC})	51°C/W
		(θ_{JA})	160°C/W

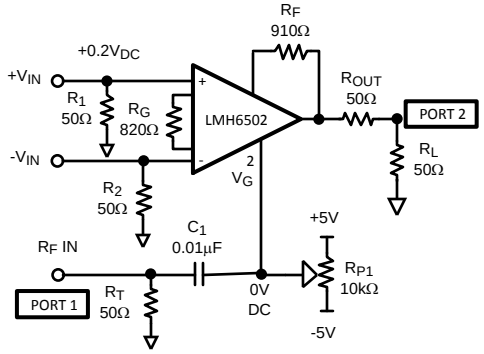
(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specific specifications, see the Electrical Characteristics tables.

Electrical Characteristics[1]

Unless otherwise specified, all limits specified for T_J = 25°C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN_DIFF} = ±0.1V, R_L = 100Ω, V_G = +2V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[2]	Max[2]	Units
Frequency Domain Response						
BW	-3dB Bandwidth	V_{OUT} < 0.5_{PP}		130		MHz
		V_{OUT} < 0.5_{PP}, $A_{V(MAX)}$ = 100		50		
GF	Gain Flatness	V_{OUT} < $0.5V_{PP}$ 0.6V ≤ V_G ≤ 2V, ±0.3dB		30		MHz
Att Range	Flat Band (Relative to Max Gain) Attenuation Range[3]	±0.2dB, f < 30MHz		16		dB
		±0.1dB, f < 30MHz		7.5		
BW Control	Gain control Bandwidth	V_G = 1V[4]		100		MHz
PL	Linear Phase Deviation	DC to 60MHz		1.5		deg
G Delay	Group Delay	DC to 130MHz		2.5		ns
CT (dB)	Feed-through	V_G = 0V, 30MHz (Output Referred)		−47		dB
GR	Gain Adjustment Range	f < 10MHz		72		dB
		f < 30MHz		67		
Time Domain Response						
t_r, t_f	Rise and Fall Time	0.5V Step		2.2		ns
OS %	Overshoot	0.5V Step		10		%
SR	Slew Rate	4V Step		1800		V/µs
Δ G Rate	Gain Change Rate	V_{IN} = 0.3V, 10%-90% of Final Output		4.8		dB/ns
Distortion & Noise Performance						
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz		−55		dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 20MHz		−57		dBc
THD	Total Harmonic Distortion	$2V_{PP}$, 20MHz		−53		dBc
En tot	Total Equivalent Input Noise	1MHz to 150MHz		7.7		nV/√Hz
I_N	Input Noise Current	1MHz to 150MHz		2.4		pA/√Hz
DG	Differential Gain	f = 4.43MHz, R_L = 150Ω, Neg. Sync		0.34		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm. Bold numbers refer to over temperature limits.
(3) Flat Band Attenuation (Relative to Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB) relative to A_{VMAX} gain. For example, for f < 30MHz, here are the Flat Band Attenuation ranges:
±0.2dB 20dB down to 4dB = 16dB range
±0.1dB 20dB down to 12.5 dB = 7.5dB range
(4) Gain Control Frequency Response Schematic:



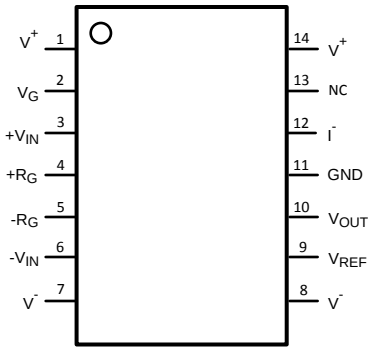
Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN_DIFF} = ±0.1V, R_L = 100Ω, V_G = +2V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[2]	Max[2]	Units
DP	Differential Phase	f = 4.43MHz, R_L = 150Ω, Neg. Sync		0.10		deg
DC & Miscellaneous Performance						
GACCU	Gain Accuracy (See Application Information)	V_G = 2.0V		0.0	+0.6	dB
		1V < V_G < 2V		+0.6/−0.3	+3.1/−3.6	
G Match	Gain Matching (See Application Information)	V_G = 2.0V		–	±0.6	dB
		1 < V_G < 2V		–	+2.8/−3.9	
K	Gain Multiplier (See Application Information)		1.61 **1.58**	1.72	1.84 **1.91**	V/V
V_{CM}	Input Voltage Range	Pin 3 & 6 Common Mode, |CMRR| > 55dB[5]	±2.0 **±1.70**	±2.2		V
V_{IN_DIFF}	Differential Input Voltage	Between pins 3 & 6	±0.3 **±0.12**	±0.39		V
I_{RG_MAX}	R_G Current	Pins 4 & 5	±1.70 **±1.56**	±2.22		mA
I_{BIAS}	Bias Current	Pins 3 & 6[6]		9	18 **20**	µA
		Pins 3 & 6[6], V_S = ±2.5V		2.5	5 **6**	
TC I_{BIAS}	Bias Current Drift	Pin 3 & 6[7]		100		nA/°C
I_{OFF}	Offset Current	Pin 3 & 6		0.01	2.0 **3.6**	µA
TC I_{OFF}	Offset Current Drift	See[7]		5		nA/°C
R_{IN}	Input Resistance	Pin 3 & 6		750		kΩ
C_{IN}	Input Capacitance	Pin 3 & 6		5		pF
I_{VG}	V_G Bias Current	Pin 2, V_G = 0V[6]		−300		µA
TC I_{VG}	V_G Bias Drift	Pin 2[7]		20		nA/°C
R_{VG}	V_G Input Resistance	Pin 2		10		kΩ
C_{VG}	V_G Input Capacitance	Pin 2		1.3		pF
V_{OUT}	Output Voltage Range	R_L = 100Ω	±3.00 **±2.95**	±3.20		V
		R_L = Open	±3.95 **±3.82**	±4.00		
R_{OUT}	Output Impedance	DC		0.1		Ω
I_{OUT}	Output Current	V_{OUT} = ±4V from Rails	±80 **±75**	±90		mA
$V_{O\ OFFSET}$	Output Offset Voltage	0V < V_G < 2V		±80	±300 **±380**	mV
+PSRR	+Power Supply Rejection Ratio[8]	Input Referred, 1V change, V_G = 2.2V		−69	−47 **−45**	dB
−PSRR	−Power Supply Rejection Ratio[8]	Input Referred, 1V change, V_G = 2.2V		−58	−41 **−40**	dB
CMRR	Common Mode Rejection Ratio[5]	Input Referred,V_G = 2V −1.8V < V_{CM} < 1.8V		−72		dB
I_S	Supply Current	No Load		27	38 **41**	mA
		V_S = ±2.5V, R_L= Open		9.3	16 **19**	

(5) CMRR definition: $[|\Delta V_{OUT}/\Delta V_{CM}| / A_V]$ with 0.1V differential input voltage.
(6) Positive current corresponds to current flowing in the device.
(7) Drift determined by dividing the change in parameter distribution average at temperature extremes by the total temperature change.
(8) +PSRR definition: $[|\Delta V_{OUT}/\Delta V^+| / A_V]$, −PSRR definition: $[|\Delta V_{OUT}/\Delta V^-| / A_V]$ with 0.1V differential input voltage.

Connection Diagram



14-Pin SOIC/TSSOP (Top View)
See Package Numbers D (R-PDSO-G14) and PW (R-PDSO-G14)

Typical Performance Characteristics

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{GMAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

Small Signal Frequency for Various V_G

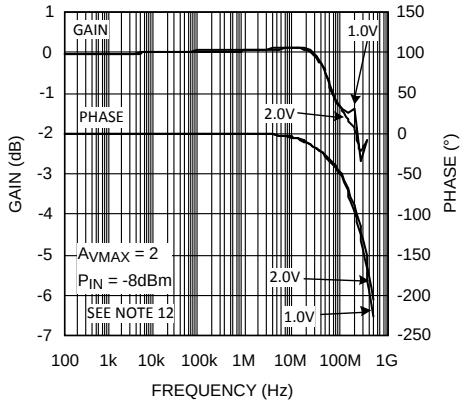


Figure 3.

Large Signal Frequency for Various V_G

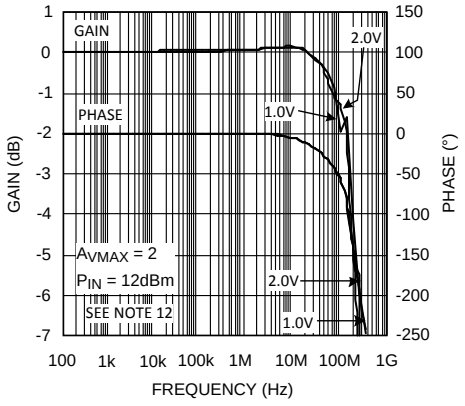


Figure 4.

Frequency Response Over Temperature (A_V = 10)

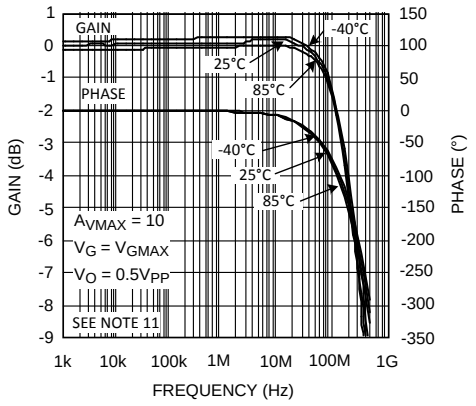


Figure 5.

Frequency Response for Various V_G (A_{VMAX} = 10)

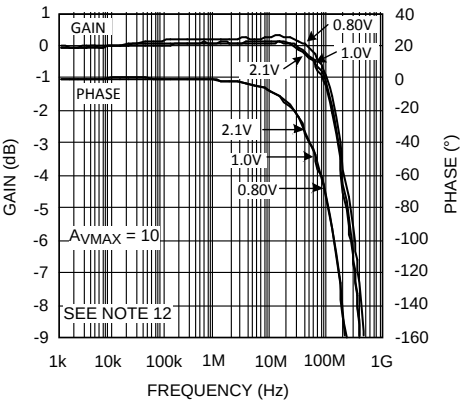


Figure 6.

Frequency Response for Various V_G (A_{VMAX} = 10) (±2.5V)

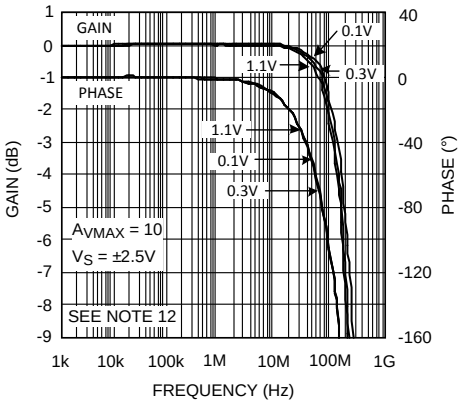


Figure 7.

Small Signal Frequency Response for Various A_{VMAX}

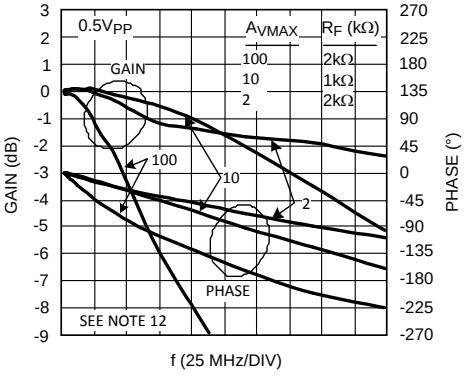


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{GMAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

Large Signal Frequency Response for Various A_{VMAX}

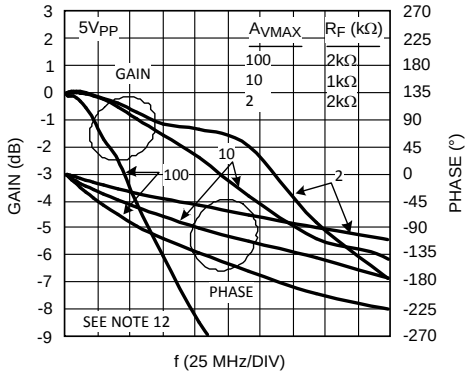


Figure 9.

Frequency Response for Various V_G (A_{VMAX}= 105) (Small Signal)

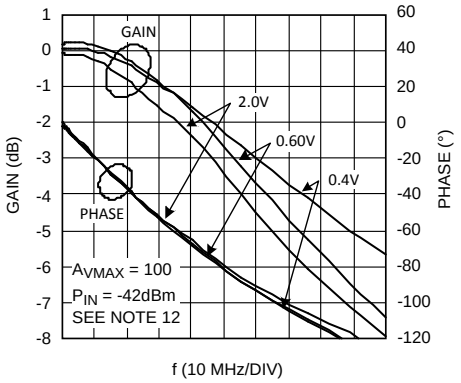


Figure 10.

Frequency Response for Various V_G (A_{VMAX}= 105) (Large Signal)

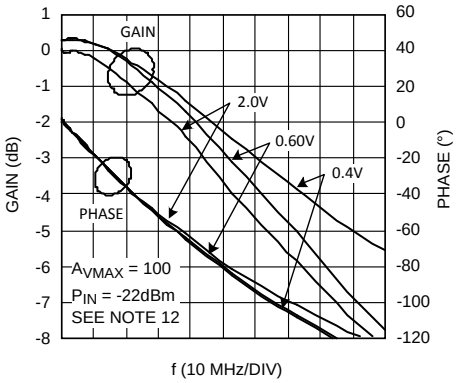


Figure 11.

I_S vs. V_S

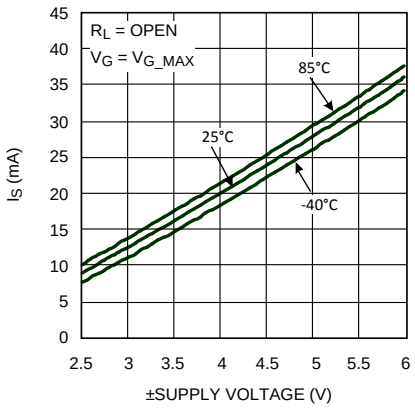


Figure 12.

I_S vs. V_S

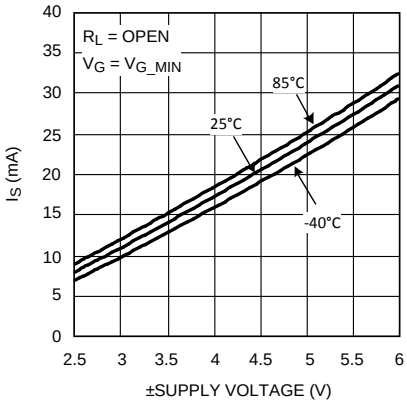


Figure 13.

Input Bias Current vs. V_S

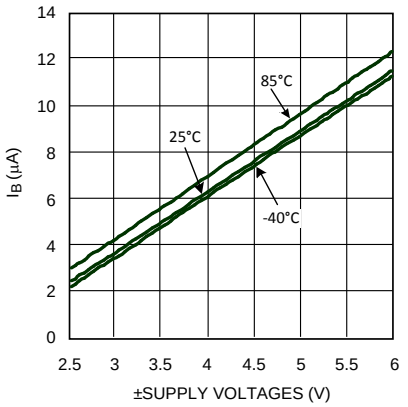


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{GMAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

A_{VMAX} vs. V_{CM}

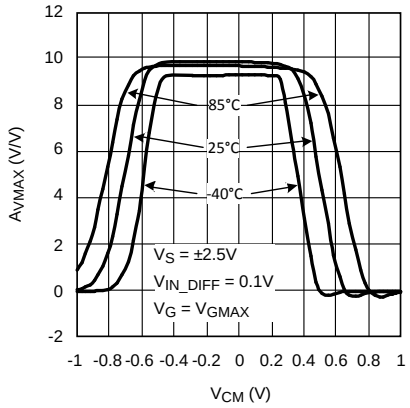


Figure 15.

A_{VMAX} vs. V_{CM}

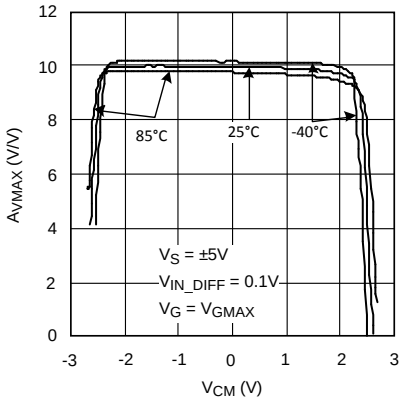


Figure 16.

PSRR ±5V

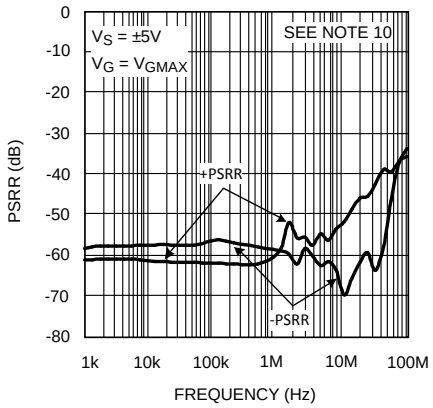


Figure 17.

PSRR ±2.5V

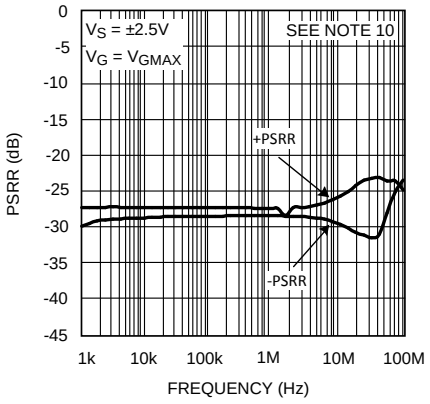


Figure 18.

CMRR ±5V

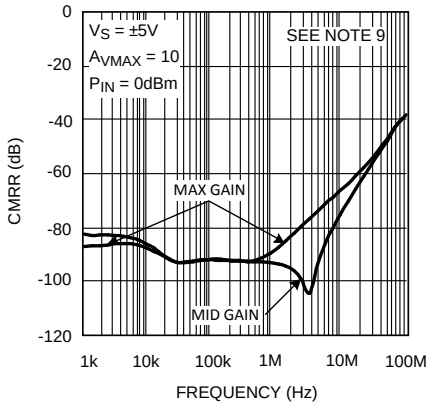


Figure 19.

CMRR ±2.5V

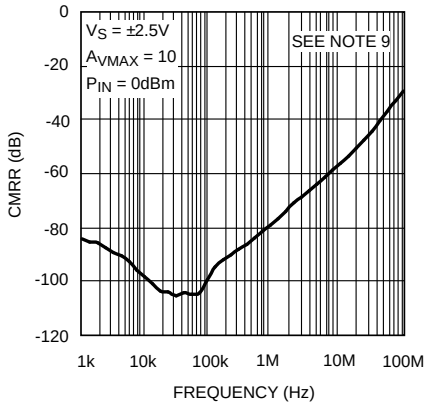


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{GMAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

A_{VMAX} vs. Supply Voltage

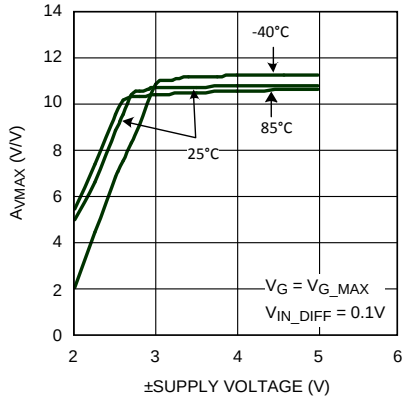


Figure 21.

Supply Current vs. V_{CM}

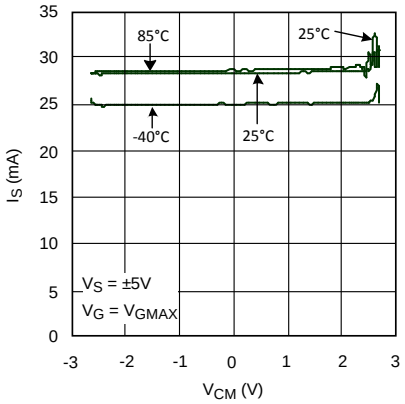


Figure 22.

Supply Current vs. V_{CM}

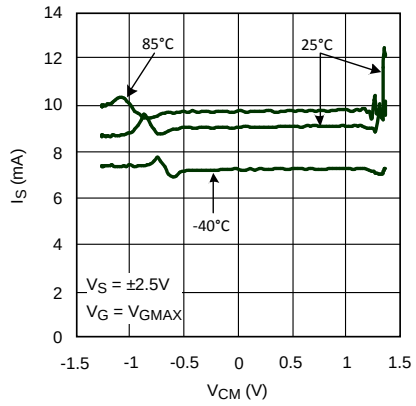


Figure 23.

Output Offset Voltage vs. V_{CM} (Typical Unit #1)

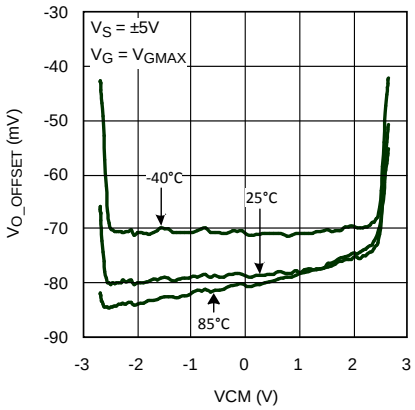


Figure 24.

Output Offset Voltage vs. V_{CM} (Typical Unit #2)

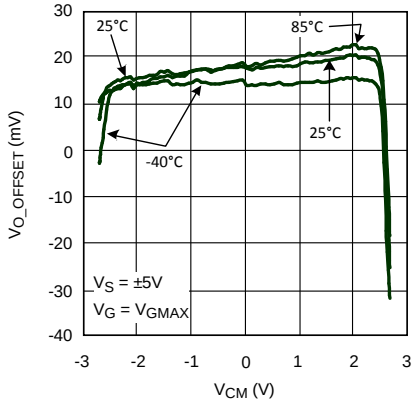


Figure 25.

Output Offset Voltage vs. V_{CM} (Typical Unit #3)

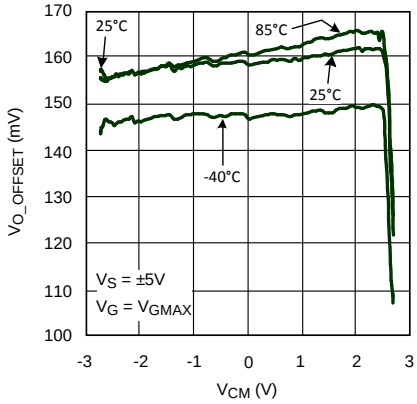


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{GMAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

Feed through Isolation

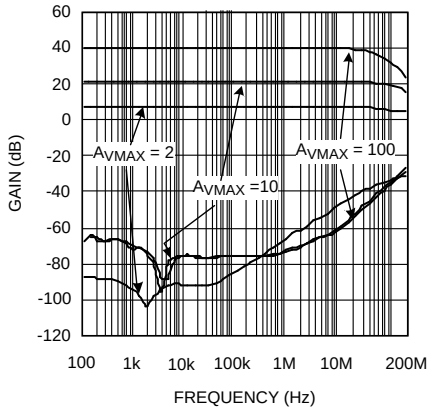


Figure 27.

Gain Flatness and Linear Phase Deviation vs. V_G

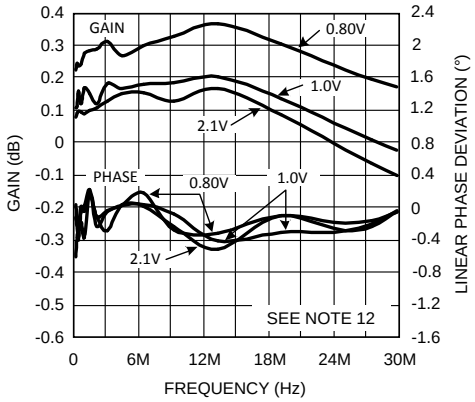


Figure 28.

Gain Flatness Frequency vs. Gain (1)

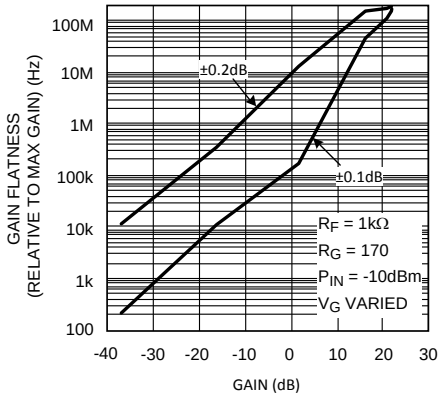


Figure 29.

Group Delay vs. Frequency

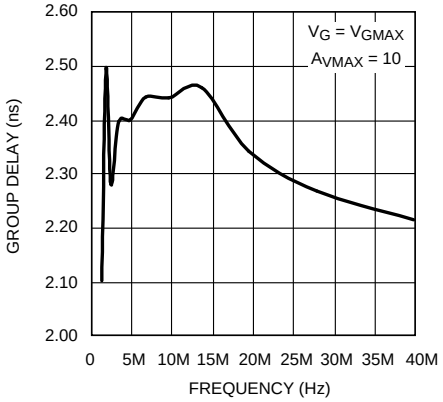


Figure 30.

K Factor vs. R_G

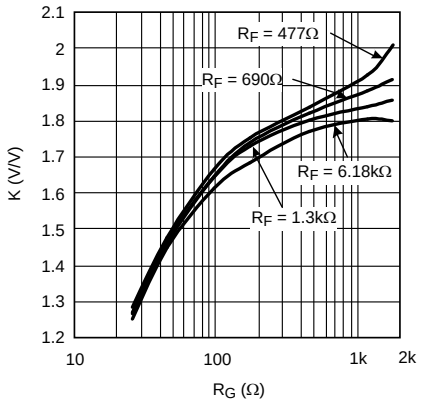


Figure 31.

Gain vs. V_G Including Limits

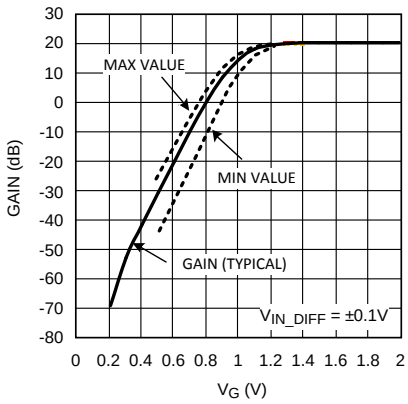


Figure 32.

(1) Flat Band Attenuation (Relative to Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB) relative to A_{VMAX} gain. For example, for f < 30MHz, here are the Flat Band Attenuation ranges:
±0.2dB 20dB down to 4dB = 16dB range
±0.1dB 20dB down to 12.5 dB = 7.5dB range

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{GMAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

BW vs. R_F

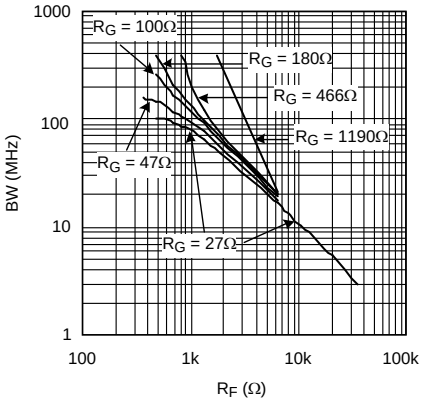


Figure 33.

Gain vs. V_G (±5V)

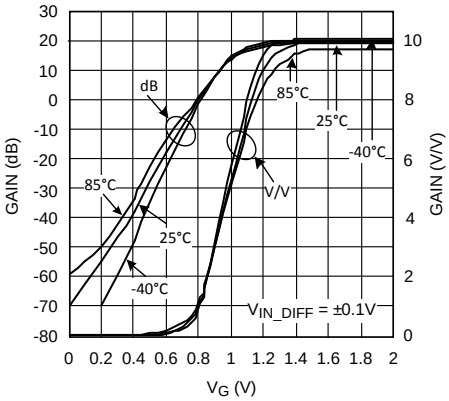


Figure 34.

Gain vs. V_G (±2.5V)

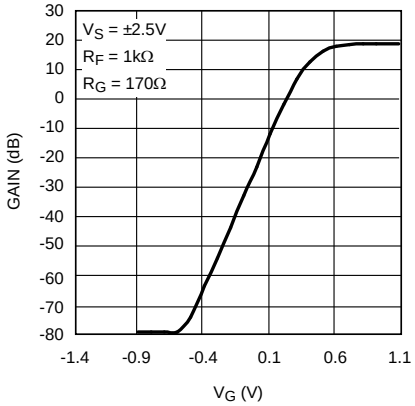


Figure 35.

Output Offset Voltage vs. V_G (Typical Unit #1)

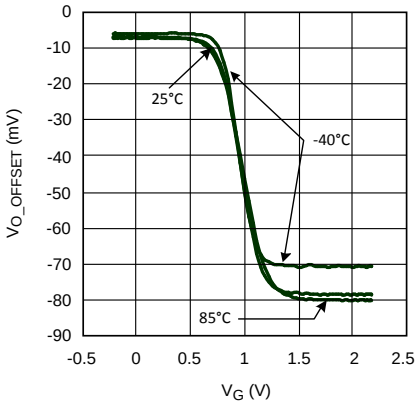


Figure 36.

Output Offset Voltage vs. V_G (Typical Unit #2)

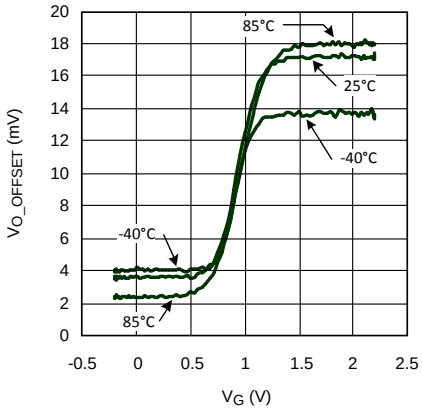


Figure 37.

Output Offset Voltage vs. V_G (Typical Unit #3)

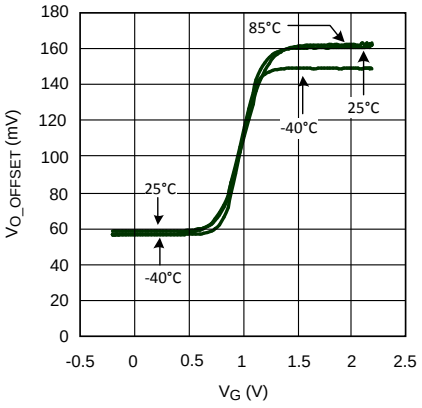


Figure 38.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{GMAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

Output Offset Voltage vs. ±V_S for various V_G (Typical Unit# 1)

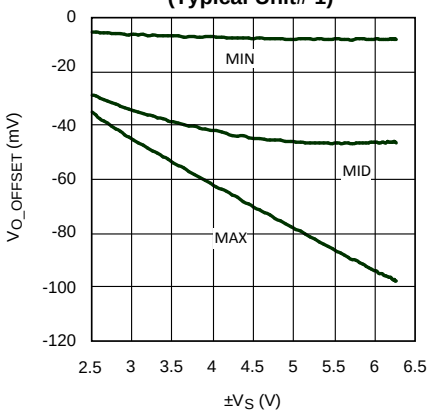


Figure 39.

Output Offset Voltage vs. ±V_S for various V_G (Typical Unit# 2)

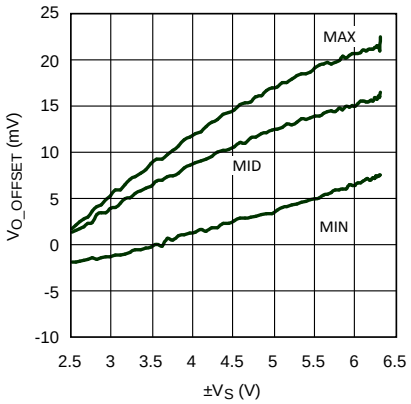


Figure 40.

Output Offset Voltage vs. ±V_S for various V_G (Typical Unit# 3)

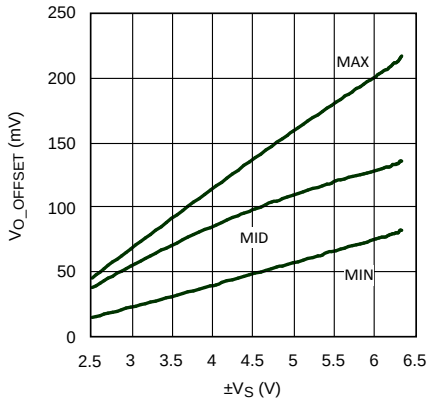


Figure 41.

Noise vs. Frequency (A_{VMAX} = 2)

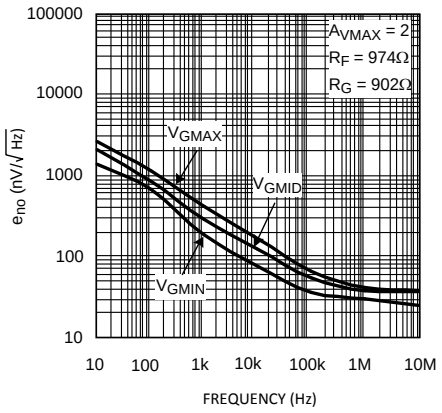


Figure 42.

Noise vs. Frequency (A_{VMAX} = 10)

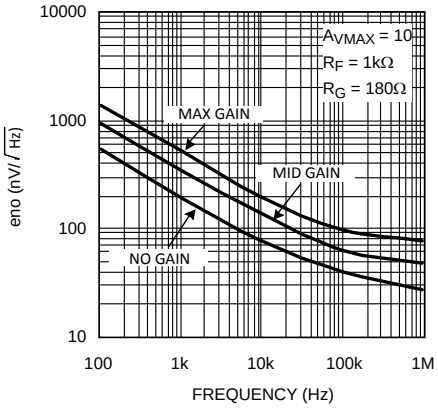


Figure 43.

Noise vs. Frequency (A_{VMAX} = 105)

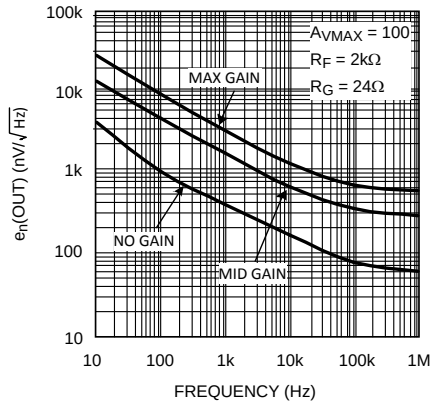


Figure 44.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{GMAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

−1dB Compression

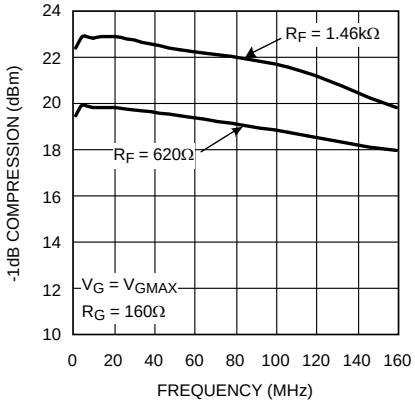


Figure 45.

Output Voltage vs. Output Current

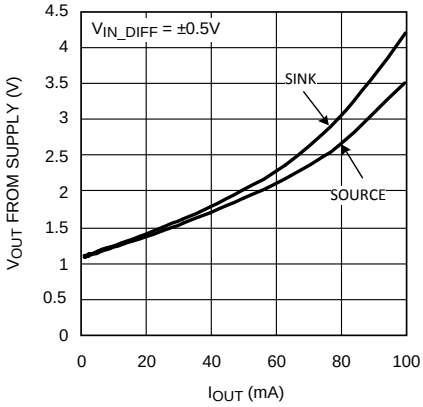


Figure 46.

HD2 & HD3 vs. P_{OUT}

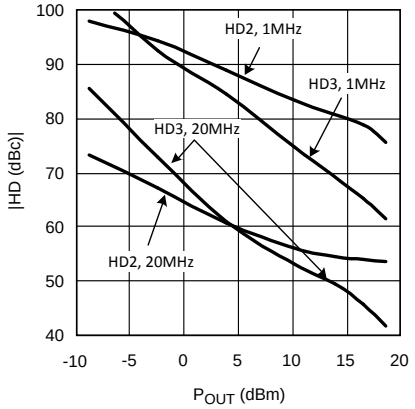


Figure 47.

THD vs. P_{OUT}

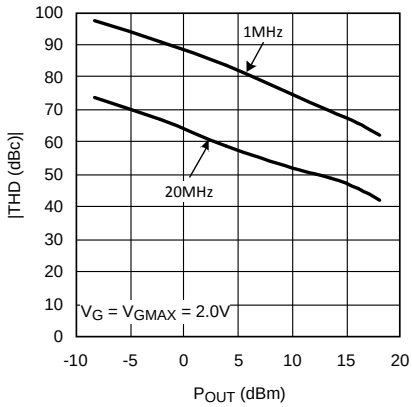


Figure 48.

THD vs. P_{OUT}

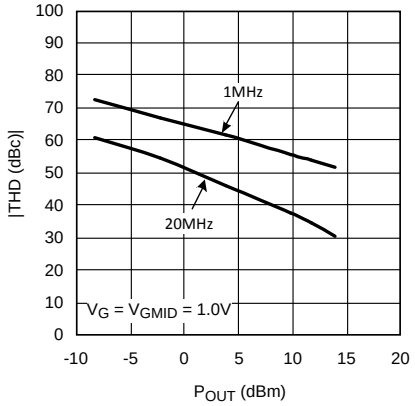


Figure 49.

HD2 & HD3 vs. V_G

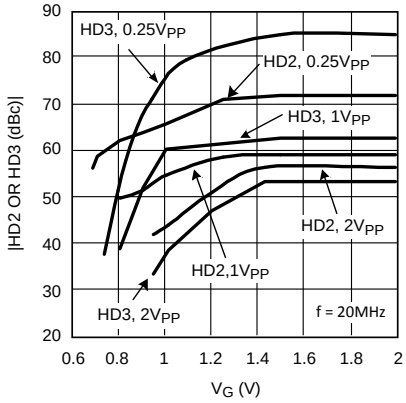


Figure 50.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{GMAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

THD vs. V_G

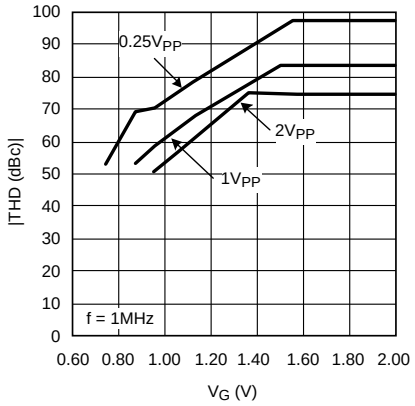


Figure 51.

THD vs. V_G

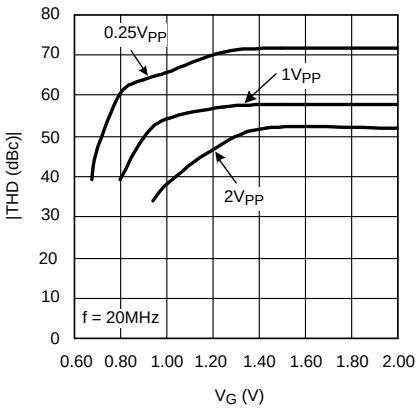


Figure 52.

V_G Bias Current vs. V_G

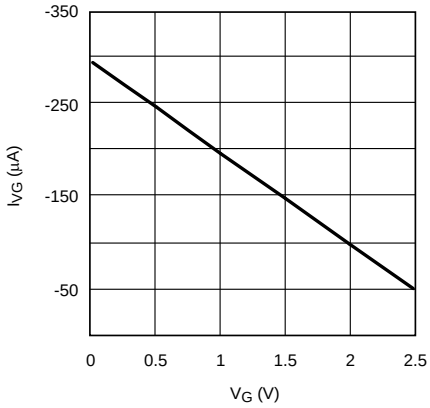


Figure 53.

Step Response Plot

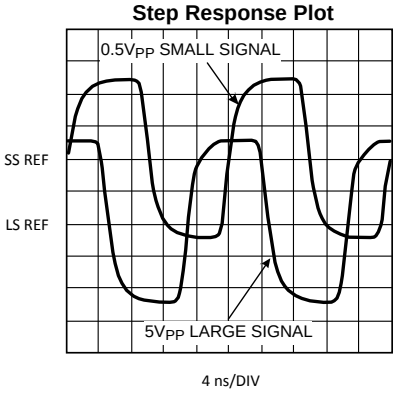


Figure 54.

Step Response Plot

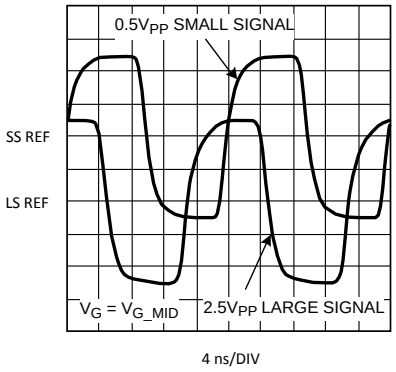


Figure 55.

Gain vs. V_G Step

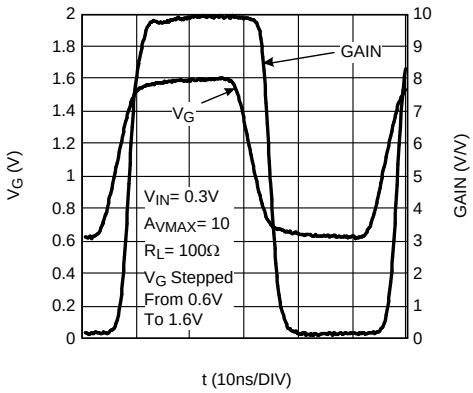


Figure 56.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{GMAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output.

Feedthrough from V_G

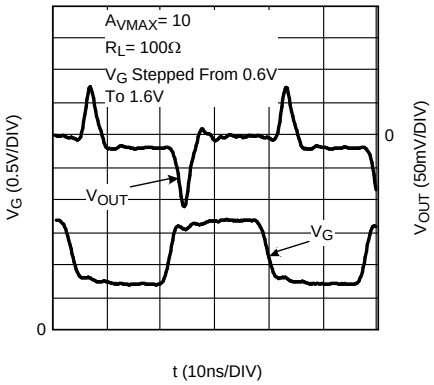


Figure 57.

APPLICATION INFORMATION

THEORY OF OPERATION

A simplified schematic is shown in Figure 58. $+V_{IN}$ and $-V_{IN}$ are buffered with closed loop voltage followers inducing a signal current in Rg proportional to $(+V_{IN})$ - $(-V_{IN})$, the differential input voltage. This current controls a current source which supplies two well-matched transistor, Q1 and Q2.

The current flowing through Q2 is converted to the final output voltage using R_F and the output amplifier, U1. By changing the fraction of the signal current "I" which flows through Q2, the gain is changed. This is done by changing the voltage applied differentially to the bases of Q1 and Q2. For example, with V_G = 0V, Q1 conducts heavily and Q2 is off. With none of "I" flowing through R_F, the LMH6502's input to output gain is strongly attenuated. With V_G = +2V, Q1 is off and the entire signal current flows through Q2 to R_F producing maximum gain. With V_G set to 1V, the bases of Q1 and Q2 are set to approximately the same voltage, Q1 and Q2 have the same collector currents - equal to one half of the signal current "I", thus the gain is approximately one half the maximum gain.

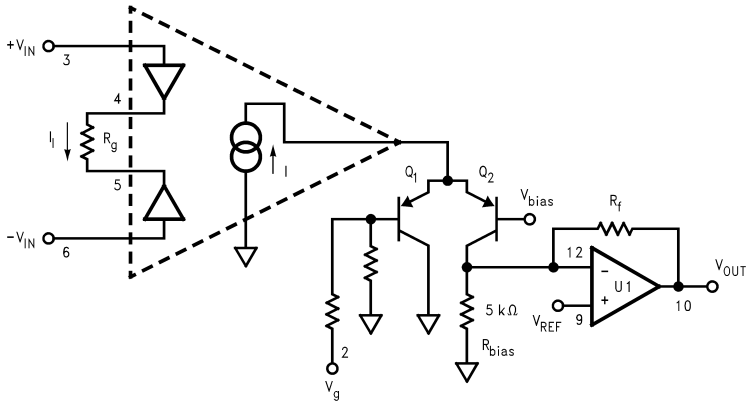


Figure 58. LMH6502 Block Diagram

CHOOSING R_F & R_G

Maximum input amplitude and maximum gain are the two key specifications that determine component values in a LMH6502 application.

The output stage op amp is a current-feedback type amplifier optimized for R_F = 1kΩ. R_G can then be computed as:

$$R_G = \frac{R_F \times 1.72}{A_{VMAX}} - 3\Omega \text{ WITH } R_F = 1K\Omega \quad (1)$$

To determine whether the maximum input amplitude will overdrive the LMH6502, compute:

$$V_{DMAX} = (R_G + 3.0\Omega) \times 1.70mA \quad (2)$$

the maximum differential input voltage for linear operation. If the maximum input amplitude exceeds the above V_{DMAX} limit, then LMH6502 should either be moved to a location in the signal chain where input amplitudes are reduced, or the LMH6502 gain A_{VMAX} should be reduced or the values for R_G and R_F should be increased. The overall system performance impact is different based on the choice made. If the input amplitude is reduced, re-compute the impact on signal-to-noise ratio. If A_{VMAX} is reduced, post LMH6502 amplifier gain, should be increased, or another gain stage added to make up for reduced system gain. To increase R_G and R_F, compute the lowest acceptable value for R_G:

$$R_G > 590 \times V_{DMAX} - 3\Omega \quad (3)$$

Operating with R_G larger than this value insures linear operation of the input buffers.

R_F may be computed from selected R_G and A_{VMAX}: R_F should be > = 1kΩ for overall best performance, however R_F < 1kΩ can be implemented if necessary using a loop gain reducing resistor to ground on the inverting summing node of the output amplifier (see application note OA-13 (SNOA366) for details).

ADJUSTING OFFSET

Offset can be broken into two parts; an input-referred term and an output-referred term. The input-referred offset shows up as a variation in output voltage as V_G is changed. This can be trimmed using the circuit in Figure 59 by placing a low frequency square wave (V_{LOW} = 0V, V_{HIGH} = 2V into V_G with V_{IN} = 0V, the input referred V_{OS} term shows up as a small square wave riding a DC value. Adjust R_{10} to null the V_{OS} square wave term to zero. After adjusting the input-referred offset, adjust R_{14} (with V_{IN} = 0, V_G = 0) until V_{OUT} is zero. Finally, for inverting applications V_{IN} may be applied to pin 6 and the offset adjustment to pin 3. These steps will minimize the output offset voltage. However, since the offset term itself varies with the gain setting, the correction is not perfect and some residual output offset will remain at in-between V_G's. Also, this offset trim does not improve output offset temperature coefficient.

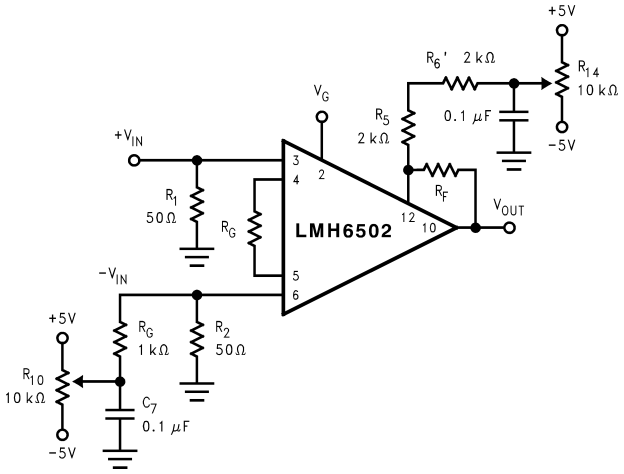


Figure 59. Nulling the output offset voltage

GAIN ACCURACY

Defined as the actual gain compared against the theoretical gain at a certain V_G (results expressed in dB).

Theoretical gain is given by:

$$A(V/V) = K \times \frac{R_F}{R_G} \times \frac{1}{1 + e^{\left[\frac{1 - V_G}{V_C}\right]}} \quad (4)$$

Where K = 1.72 (nominal) & V_C = 90mV @ room temperature.

For a V_G range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the worst case difference between the "Typical Gain" and the "Theoretical gain". The "Max" value would be the worst case difference between the max/min gain limit and the "Theoretical gain".

GAIN MATCHING

Defined as the limit on gain variation at a certain V_G (expressed in dB). Specified as "Max" only (no "Typical"). For a V_G range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case difference between the max/min gain limit and the typical gain.

NOISE

Figure 60 describes the LMH6502's output-referred spot noise density as a function of frequency with A_{VMAX} = 10V/V. The plot includes all the noise contributing terms. However, with both inputs terminated in 50Ω, the input noise contribution is minimal. At A_{VMAX} = 10V/V, the LMH6502 has a typical input-referred spot noise density (e_{in}) of 7.7nV/$\sqrt{Hz}$ flat-band. For applications extending well into the flat-band region, the input RMS voltage noise can be determined from the following single-pole model:

$$V_{RMS} = e_{in} * \sqrt{1.57 * (-3dB\ BANDWIDTH)} \quad (5)$$

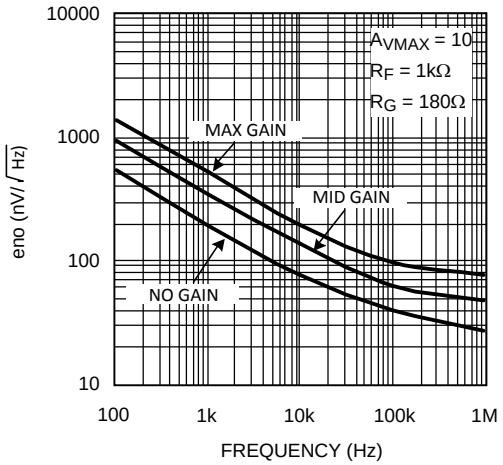


Figure 60. Output Referred Voltage Noise vs. Frequency

CIRCUIT LAYOUT CONSIDERATIONS & EVALUATION BOARD

A good high frequency PCB layout including ground plane construction and power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the I⁻ input (pin 12); keep node trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect. For best performance at low maximum gains (A_{VMAX} < 10) $+R_G$ and $-R_G$ connections should be treated in a similar fashion. Capacitance to ground should be minimized by removing the ground plane from under the body of R_G. Parasitic or load capacitance directly on the output (pin 10) degrades phase margin leading to frequency response peaking.

The LMH6502 is fully stable when driving a 100Ω load. With reduced load (e.g. 1kΩ) there is a possibility of instability at very high frequencies beyond 400MHz especially with a capacitive load. When the LMH6502 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100Ω and 39pF in series tied between the LMH6502 output and ground). C_L can also be isolated from the output by placing a small resistor in series with the output (pin 10).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6502MA	SOIC	LMH730033

SINGLE SUPPLY OPERATION

It is possible to operate the LMH6502 with a single supply. To do so, tie pin 11 (GND) to a potential about mid point between V^+ and V^-. Two examples are shown in Figure 61 & Figure 62.

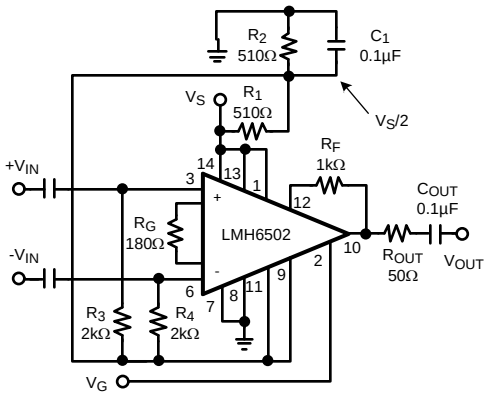


Figure 61. AC Coupled Single Supply VGA

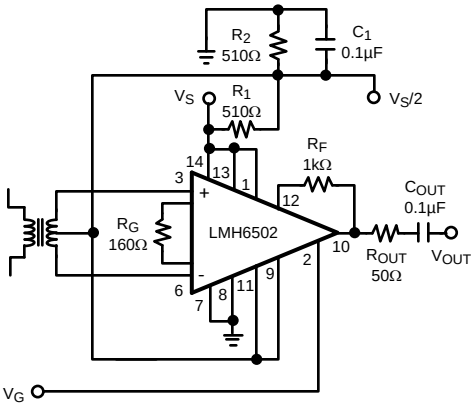


Figure 62. Transformer Coupled Single Supply VGA

OPERATING AT LOWER SUPPLY VOLTAGES

The LMH6502 is rated for operation down to 5V supplies (V^+ -V^-). There are some specifications shown for operation at ±2.5V within the data sheet (i.e. Frequency Response, CMRR, PSRR, Gain vs. V_G, etc.). Compared to ±5V operation, at lower supplies:

a) V_G range shifts lower.
Here are the approximate expressions for various V_G voltages as a function of V^+:

Table 1. V_G Definition Based on V^+

V_G	Definition	Expression (V)
V_{G_MIN}	Gain Cut-off	$0.2 \times V^+ - 1$
V_{G_MID}	$A_{VMAX}/2$	$0.2 \times V^+$
V_{G_MAX}	A_{VMAX}	$0.2 \times V^+ + 1$

b) V_{G_LIMIT} (maximum permissible voltage on V_G) is reduced. This is due to limitations within the device arising from transistor headroom. Beyond this limit, device performance will be affected (non-destructive). This could reveal itself as premature high frequency response roll-off. With ±2.5V supplies, V_{G_LIMIT} is below 1.1V whereas V_G = 1.5V is needed to get maximum gain. This means that operating under these conditions has reduced the maximum permissible voltage on V_G to a level below what is needed to get Max gain. If supply voltages are asymmetrical with V^+ being lower, further "pinching" of V_G range could result; for example, with V^+ = 2V, and V^- = −3V, V_{G_LIMIT} = 0.40V which results in maximum gain being 2.5dB less than what would be expected when V_S is higher.

c) "Max_gain" reduces. There is an intrinsic reduction in max gain when the total supply voltage is reduced (see Typical Performance Characteristics plots for Gain vs. V_G (V_S = ±2.5V). In addition, there is the more drastic mechanism described in "b" above. Beyond V_{G_LIMIT}, high frequency response is also effected.

Application Circuits

AGC LOOP

Figure 63 shows a typical AGC circuit. The LMH6502 is followed up with a LMH6714 for higher overall gain. The output of the LMH6714 is rectified and fed to an inverting integrator using a LMH6657 (wideband voltage feedback op amp). When the output voltage, V_{OUT}, is too large the integrator output voltage ramps down reducing the net gain of the LMH6502 and V_{OUT}. If the output voltage is too small, the integrator ramps up increasing the net gain and the output voltage. Actual output level is set with R_1. To prevent shifts in DC output voltage with DC changes in input signal level, trim pot R_2 is provided. AGC circuits are always limited in the range of input signals over which constant output level can be maintained. In this circuit, we would expect that reasonable AGC action could be maintained for at least 40dB. In practice, rectifier dynamic range limits reduce this slightly.

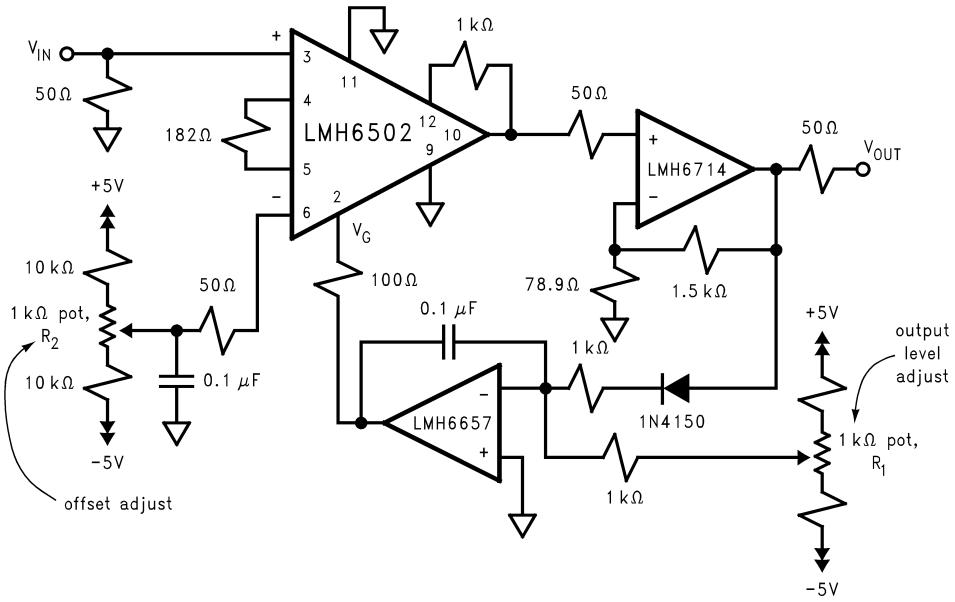


Figure 63. Automatic Gain Control (AGC) Loop

FREQUENCY SHAPING

Frequency Shaping Frequency shaping and bandwidth extension of the LMH6502 can be accomplished using parallel networks connected across the R_G ports. The network shown in the Figure 64 schematic will effectively extend the LMH6502's bandwidth.

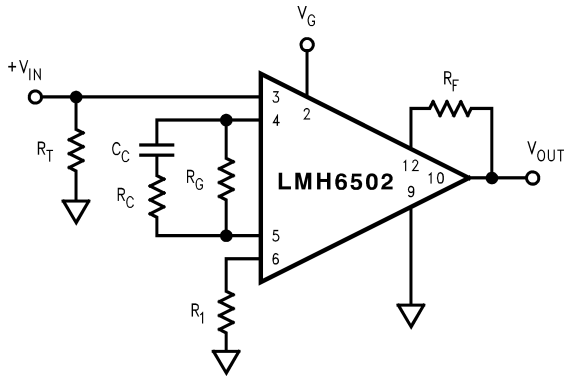


Figure 64. Frequency Shaping

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6502MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH6502MA	Samples
LMH6502MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH6502MA	Samples
LMH6502MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 02MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

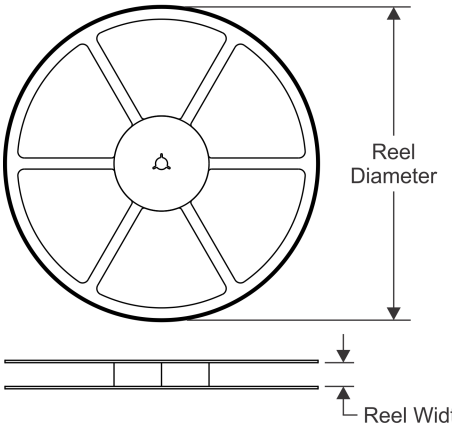
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

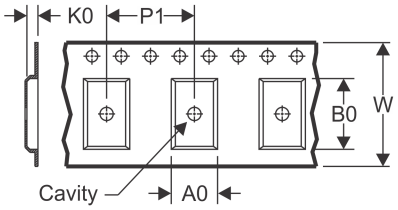
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

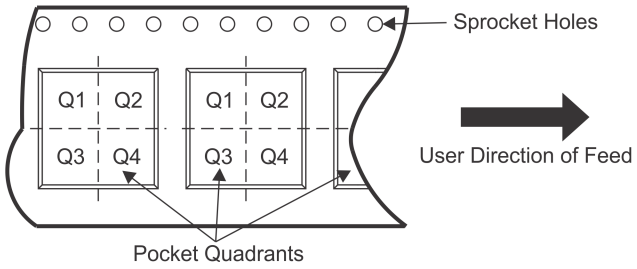


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

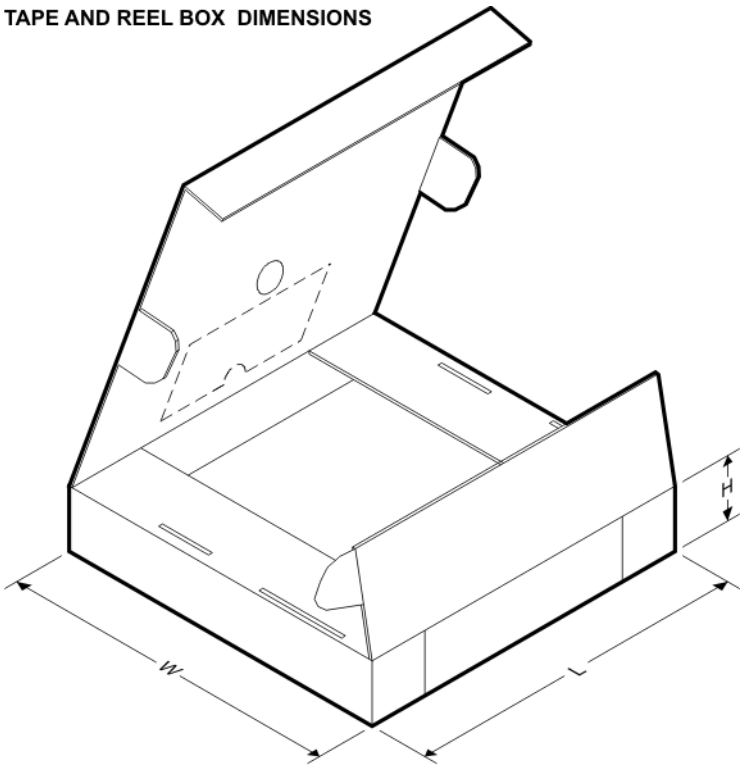
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6502MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

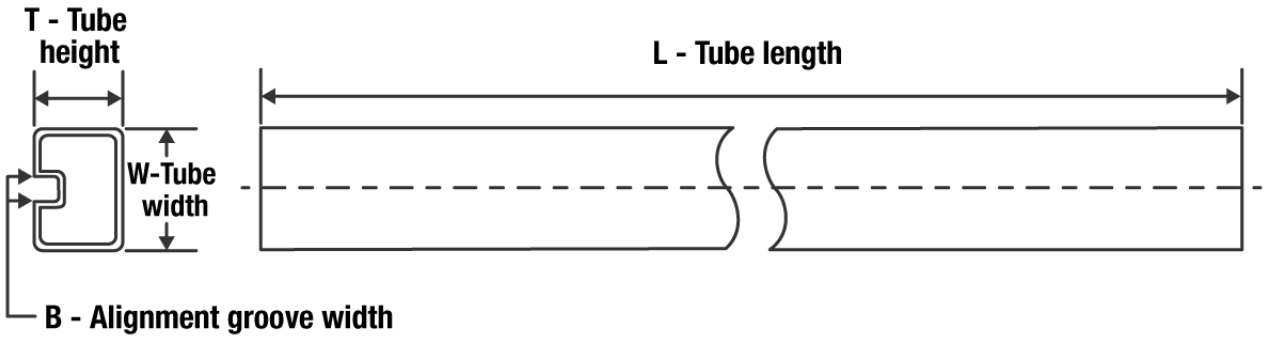
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6502MAX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

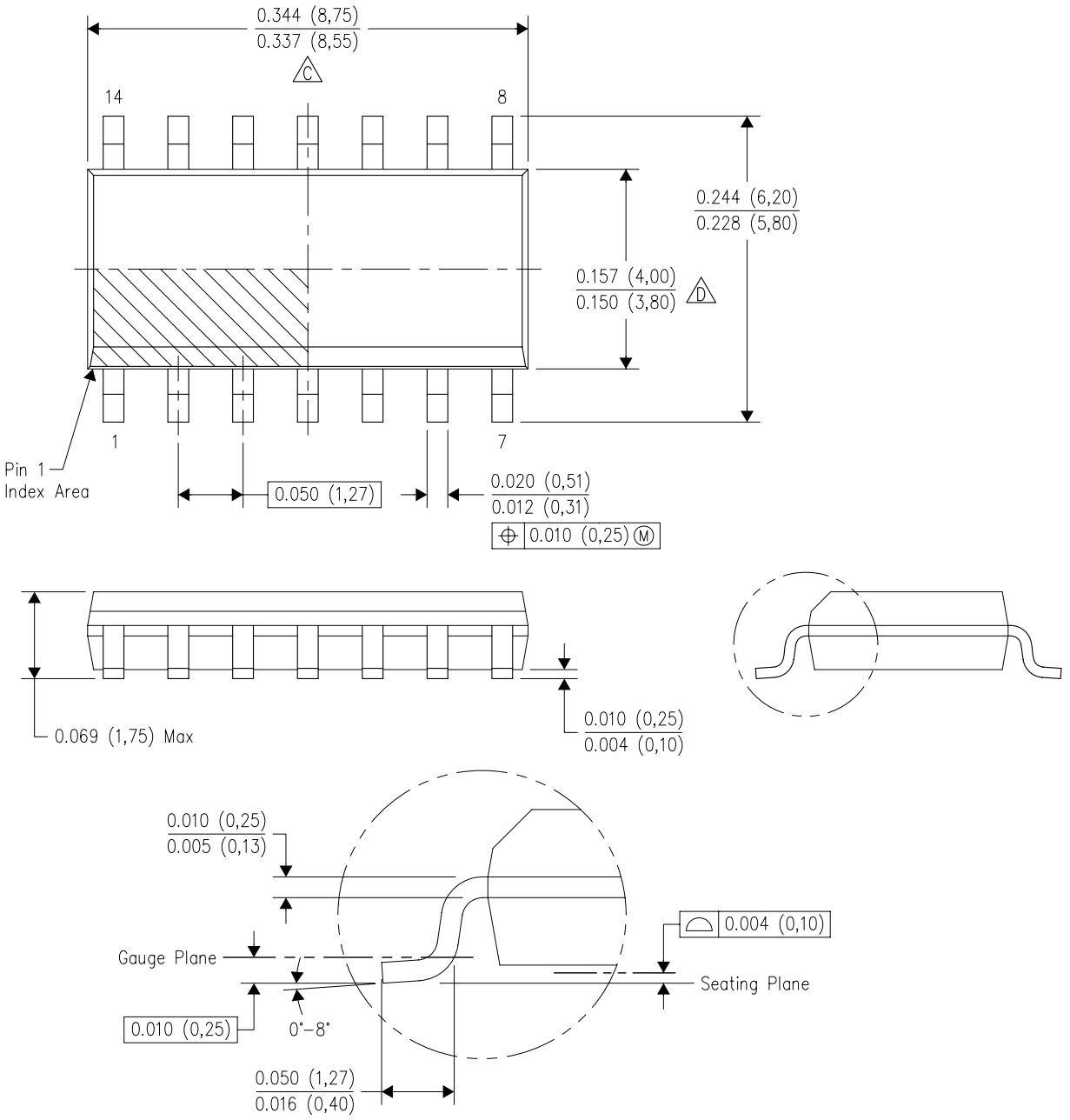
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6502MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMH6502MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

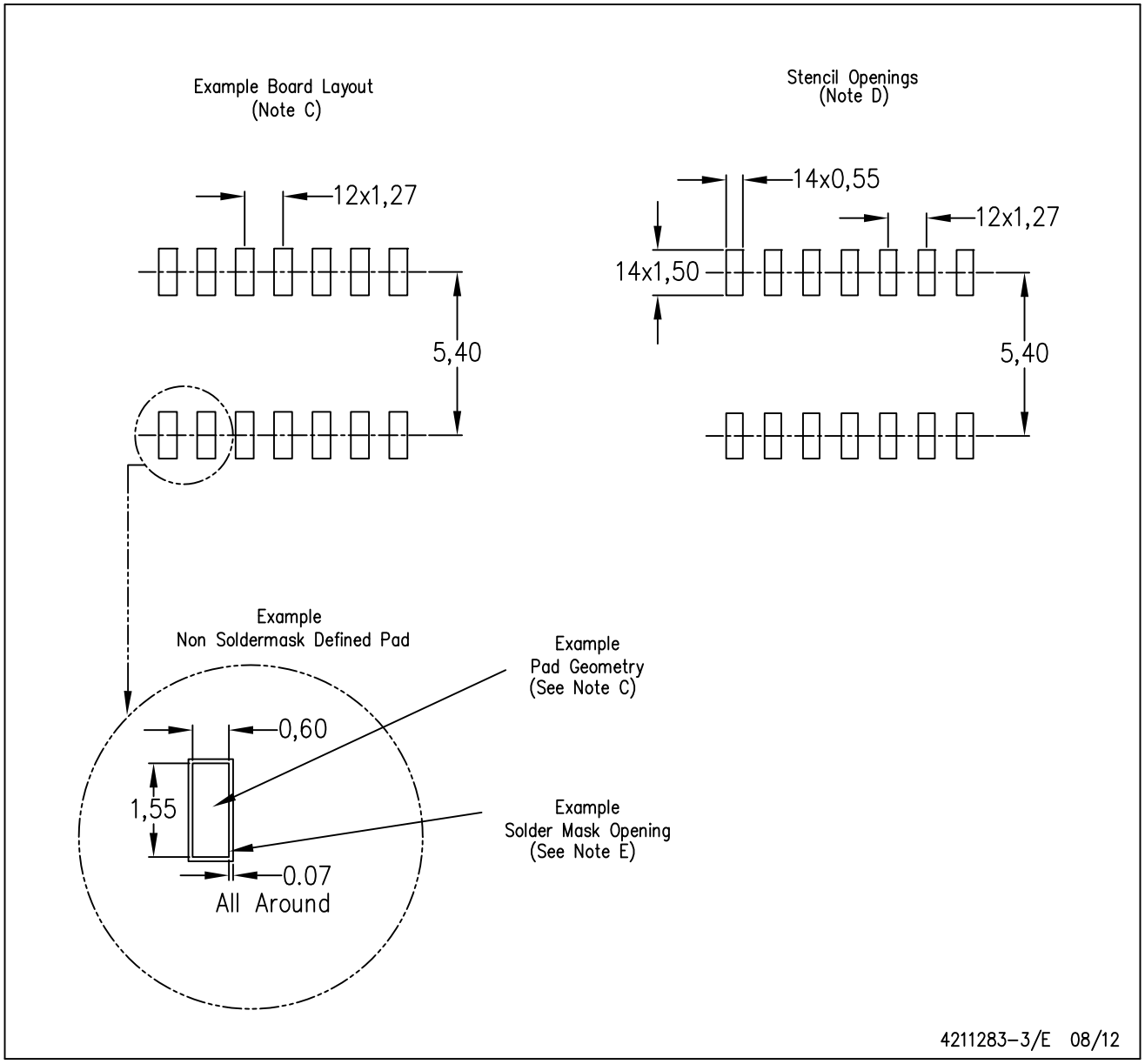
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

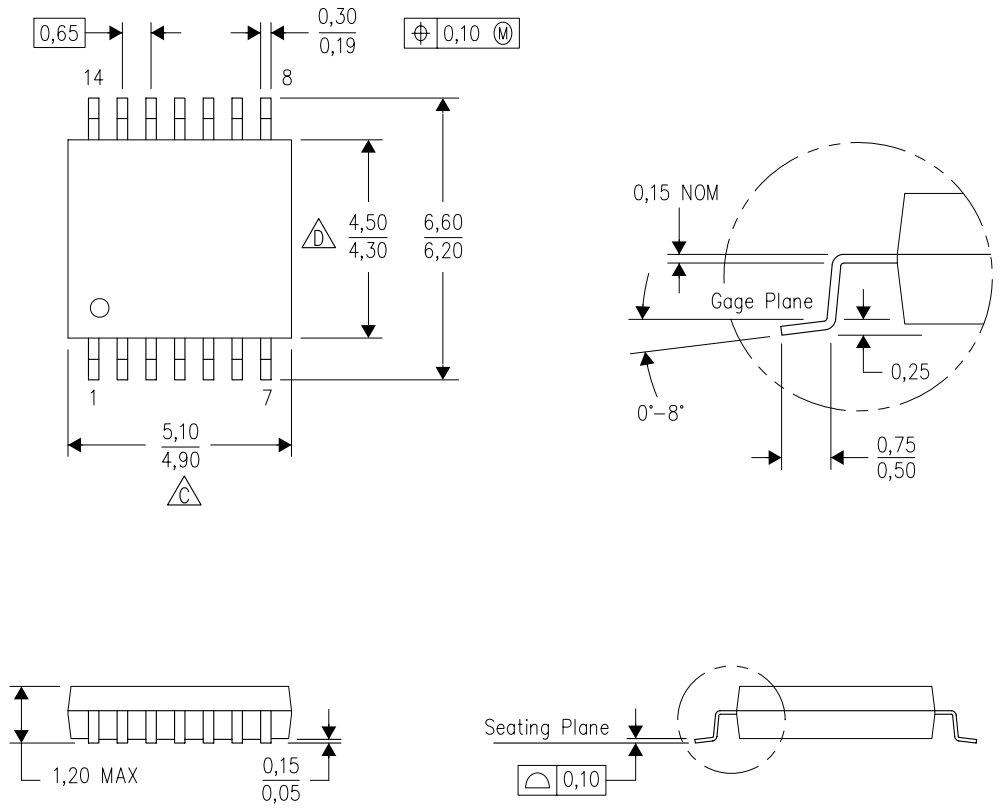
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

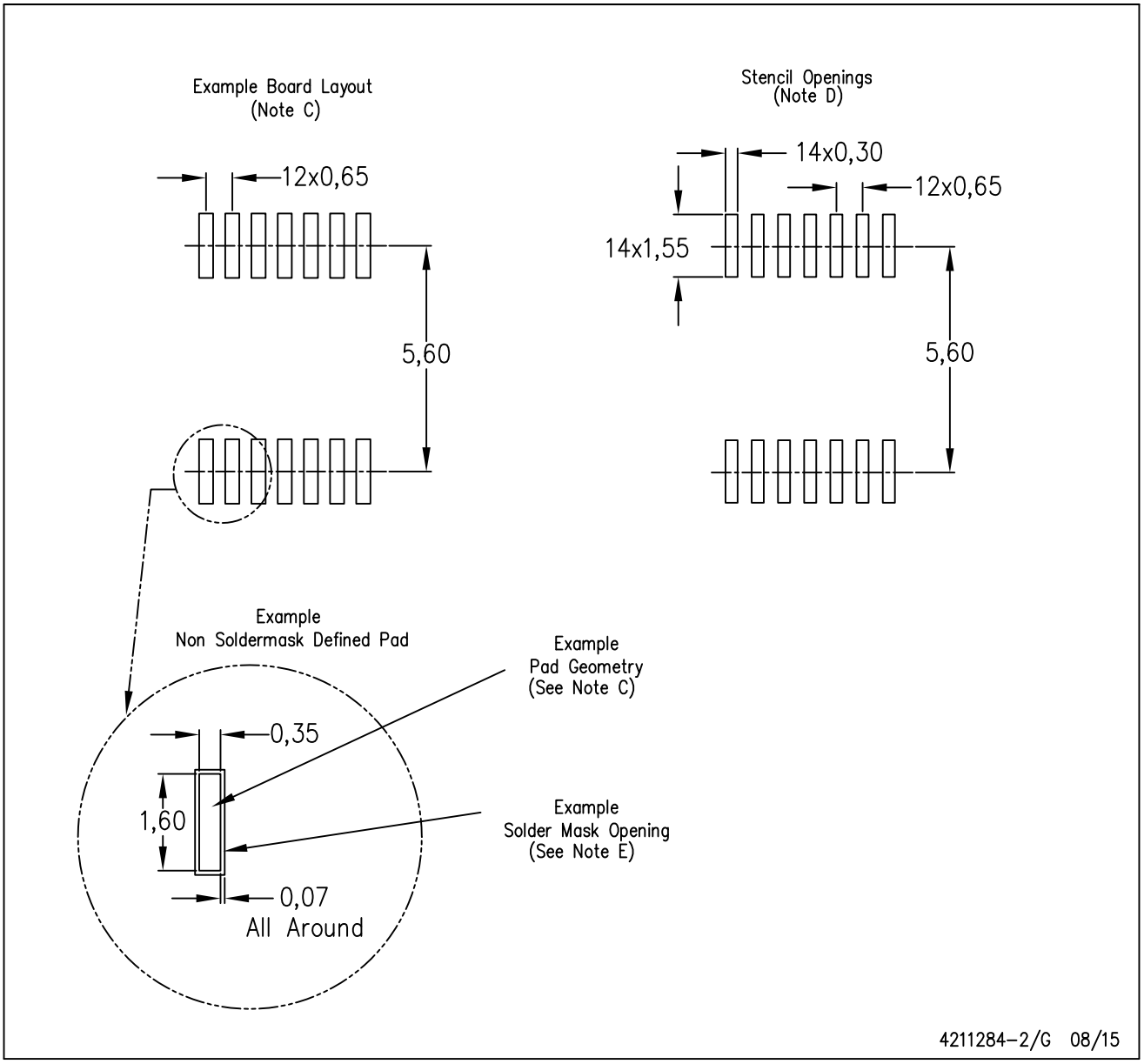
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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