



Read-Only, Pin Configured 24-Bit Σ - Δ ADC with Excitation Current Sources

AD7783

FEATURES

Single-Channel, 24-Bit Σ - Δ ADC

Pin Configurable (No Programmable Registers)

ISOURCE Select™

Pin Programmable Input Ranges (± 2.56 V or ± 160 mV)

Fixed 19.79 Hz Update Rate

Simultaneous 50 Hz and 60 Hz Rejection

24-Bit No Missing Codes

18.5-Bit p-p Resolution (± 2.56 V Range)

16.5-Bit p-p Resolution (± 160 mV Range)

INTERFACE

Master or Slave Mode of Operation

Slave Mode

3-Wire Serial

SPI®, QSPI™, MICROWIRE™, and DSP-Compatible

Schmitt Trigger on SCLK

POWER

Specified for Single 3 V and 5 V Operation

Normal: 1.3 mA @ 3 V

Power-Down: 9 μ A

ON-CHIP FUNCTIONS

Rail-to-Rail Input Buffer and PGA

APPLICATIONS

Sensor Measurement

Industrial Process Control

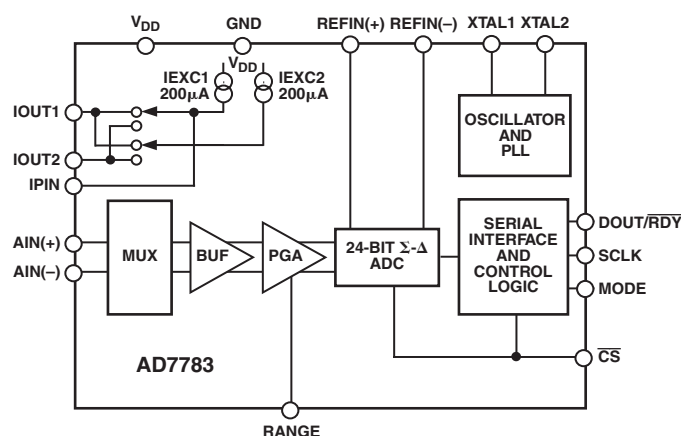
Temperature Measurement

Pressure Measurement

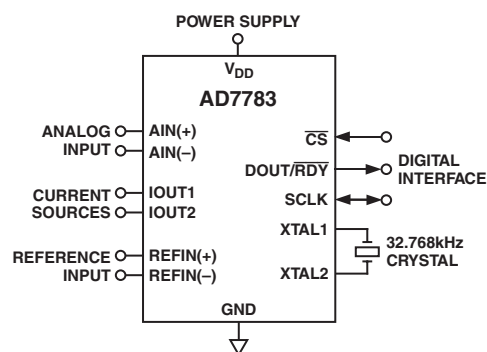
Weigh Scales

Portable Instrumentation

FUNCTIONAL BLOCK DIAGRAM



BASIC CONNECTION DIAGRAM



GENERAL DESCRIPTION

The AD7783 is a complete analog front end for low frequency measurement applications. The 24-bit sigma-delta ADC contains one fully differential input channel that can be configured with a gain of 1 or 16 allowing full-scale input signal ranges of ± 2.56 V or ± 160 mV from a $+2.5$ V differential reference input. It also contains two 200 μ A integrated current sources.

The AD7783 has an extremely simple, read-only digital interface that can be operated in master mode or slave mode.

There are no on-chip registers to be programmed. The input signal range and current source selection are configured using two external pins.

The device operates from a 32.768 kHz crystal with an on-chip PLL generating the required internal operating frequency. The output data rate from the part is fixed via the master clock at 19.79 Hz and provides simultaneous 50 Hz and 60 Hz rejection at this update rate. At this update rate, 18-bit p-p resolution can be obtained.

The part operates from a single 3 V or 5 V supply. When operating from 3 V supplies, the power dissipation for the part is 3.9 mW. The AD7783 is available in a 16-lead TSSOP.

Another part in the AD778x family is the AD7782. It is similar to the AD7783 except it has no integrated current sources and two differential input channels.

REV. C

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AD7783* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7783 Evaluation Board

DOCUMENTATION

Application Notes

- AN-202: An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change
- AN-311: How to Reliably Protect CMOS Circuits Against Power Supply Overvoltage
- AN-397: Electrically Induced Damage to Standard Linear Integrated Circuits:
- AN-607: Selecting a Low Bandwidth (<15 kSPS) Sigma-Delta ADC
- AN-608: Input Buffers on Sigma-Delta ADCs
- AN-609: Chopping on Sigma-Delta ADCs
- AN-610: The PGA on Sigma-Delta ADCs
- AN-611: 50 Hz/60Hz Rejection on Sigma-Delta ADCs
- AN-615: Peak-to-Peak Resolution Versus Effective Resolution
- AN-968: Current Sources: Options and Circuits

Data Sheet

- AD7783: Read-Only, Pin Configured 24-Bit Σ - Δ ADC With Excitation Current Sources Data Sheet

TOOLS AND SIMULATIONS

- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Delta-Sigma Rocks RF, As ADC Designers Jump On Jitter
- MS-2210: Designing Power Supplies for High Speed ADC
- Remote Three-Wire RTDs Can Multiplex Accurately To Measurement System

DESIGN RESOURCES

- AD7783 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7783 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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AD7783—SPECIFICATIONS¹

($V_{DD} = 2.7\text{ V to }3.6\text{ V or }4.75\text{ V to }5.25\text{ V}$, $REFIN(+) = 2.5\text{ V}$; $REFIN(-) = GND$; $GND = 0\text{ V}$; $XTAL1/XTAL2 = 32.768\text{ kHz Crystal}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.)

Parameter	AD7783B	Unit	Test Conditions
ADC CHANNEL SPECIFICATION			
Output Update Rate	19.79	Hz nom	
ADC CHANNEL			
No Missing Codes ²	24	Bits min	
Resolution	16	Bits p-p	$\pm 160\text{ mV Range}$, $RANGE = 0$
	18	Bits p-p	$\pm 2.56\text{ V Range}$, $RANGE = 1$
Output Noise	See Table I		
Integral Nonlinearity	± 10	ppm of FSR max	Typically 2 ppm, $FSR = \frac{2 \times 1.024 \cdot REFIN}{Gain}$
Offset Error	± 3	$\mu\text{V typ}$	$AIN(+) = AIN(-) = 2.5\text{ V}$
Offset Error Drift versus Temperature	± 10	$\text{nV}/^{\circ}\text{C typ}$	
Full-Scale Error	± 10	$\mu\text{V typ}$	$V_{DD} = 3\text{ V}$
Gain Drift versus Temperature	± 0.5	$\text{ppm}/^{\circ}\text{C typ}$	
Power Supply Rejection (PSR)	100	dB typ	Input Range = $\pm 160\text{ mV}$, $V_{IN} = 1/16\text{ V}$
	85	dB typ	Input Range = $\pm 2.56\text{ V}$, $V_{IN} = 1\text{ V}$
ANALOG INPUTS			
Differential Input Voltage Ranges	± 160 ± 2.56	mV nom V nom	Range = 0 Range = 1
ADC Range Matching	± 2	$\mu\text{V typ}$	Input Voltage = 159 mV on Both Ranges
Absolute AIN Voltage Limits	$GND + 100\text{ mV}$ $V_{DD} - 100\text{ mV}$	V min V max	
Analog Input Current ²			
DC Input Current	± 1	nA max	
DC Input Current Drift	± 5	$\text{pA}/^{\circ}\text{C typ}$	
Normal-Mode Rejection ^{2, 3}			
@ 50 Hz	60	dB min	50 Hz $\pm 1\text{ Hz}$
@ 60 Hz	94	dB min	60 Hz $\pm 1\text{ Hz}$
Common-Mode Rejection			
@ DC	105	dB min	Input Range = $\pm 160\text{ mV}$, $V_{IN} = 1/16\text{ V}$ 125 dB typ, 110 dB typ when Input Range = $\pm 2.56\text{ V}$
@ 50 Hz ²	100	dB min	50 Hz $\pm 1\text{ Hz}$
@ 60 Hz ²	100	dB min	60 Hz $\pm 1\text{ Hz}$
REFERENCE INPUT			
REFIN Voltage	2.5	V nom	$REFIN = REFIN(+) - REFIN(-)$
REFIN Voltage Range ²	1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits ²	$GND - 30\text{ mV}$ $V_{DD} + 30\text{ mV}$	V min V max	
Average Reference Input Current	0.5	$\mu\text{A/V typ}$	
Average Reference Input Current Drift	± 0.01	$\text{nA}/^{\circ}\text{C typ}$	
Normal-Mode Rejection ^{2, 3}			
@ 50 Hz	60	dB min	50 Hz $\pm 1\text{ Hz}$
@ 60 Hz	94	dB min	60 Hz $\pm 1\text{ Hz}$
Common-Mode Rejection			
@ DC	100	dB typ	Input Range = $\pm 160\text{ mV}$, $V_{IN} = 1/16\text{ V}$
@ 50 Hz	110	dB typ	50 Hz $\pm 1\text{ Hz}$
@ 60 Hz	110	dB typ	60 Hz $\pm 1\text{ Hz}$
EXCITATION CURRENT SOURCES (IEXC1, IEXC2)			
Output Current	200	μA	
Initial Tolerance at 25°C	± 10	% typ	
Drift	200	$\text{ppm}/^{\circ}\text{C typ}$	
Initial Current Matching at 25°C	± 2.5	% max	No Load
Drift Matching	20	$\text{ppm}/^{\circ}\text{C typ}$	
Line Regulation	2.5	$\mu\text{A/V max}$	$V_{DD} = 5\text{ V} \pm 5\%$. Typically 1.25 $\mu\text{A/V}$.
Load Regulation	300	nA/V typ	
Output Compliance	$V_{DD} - 0.6$ $GND - 30\text{ mV}$	V max V min	

Parameter	AD7783B	Unit	Test Conditions
LOGIC INPUTS			
All Inputs Except SCLK and XTAL1 ²			
V _{INL} , Input Low Voltage	0.8	V max	V _{DD} = 5 V
	0.4	V max	V _{DD} = 3 V
V _{INH} , Input High Voltage	2.0	V min	V _{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input) ²			
V _{T(+)}	1.4/2	V min/V max	V _{DD} = 5 V
V _{T(-)}	0.8/1.4	V min/V max	V _{DD} = 5 V
V _{T(+)} – V _{T(-)}	0.3/0.85	V min/V max	V _{DD} = 5 V
V _{T(+)}	0.95/2	V min/V max	V _{DD} = 3 V
V _{T(-)}	0.4/1.1	V min/V max	V _{DD} = 3 V
V _{T(+)} – V _{T(-)}	0.3/0.85	V min/V max	V _{DD} = 3 V
XTAL1 Only ²			
V _{INL} , Input Low Voltage	0.8	V max	V _{DD} = 5 V
V _{INH} , Input High Voltage	3.5	V min	V _{DD} = 5 V
V _{INL} , Input Low Voltage	0.4	V max	V _{DD} = 3 V
V _{INH} , Input High Voltage	2.5	V min	V _{DD} = 3 V
Input Currents	±1	μA max	V _{IN} = V _{DD}
	–70	μA max	V _{IN} = GND, Typically –40 μA at 5 V and –20 μA at 3 V
Input Capacitance	10	pF typ	All Digital Inputs
LOGIC OUTPUTS (Excluding XTAL2)			
V _{OH} , Output High Voltage ²	V _{DD} – 0.6	V min	V _{DD} = 3 V, I _{SOURCE} = 100 μA
V _{OL} , Output Low Voltage ²	0.4	V max	V _{DD} = 3 V, I _{SINK} = 100 μA
V _{OH} , Output High Voltage ²	4	V min	V _{DD} = 5 V, I _{SOURCE} = 200 μA
V _{OL} , Output Low Voltage ²	0.4	V max	V _{DD} = 5 V, I _{SINK} = 1.6 mA
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance	±10	pF typ	
Data Output Coding	Offset Binary		
START-UP TIME			
From Power-On	300	ms typ	
POWER REQUIREMENTS			
Power Supply Voltage			
V _{DD} – GND	2.7/3.6	V min/V max	V _{DD} = 3 V nom
	4.75/5.25	V min/V max	V _{DD} = 5 V nom
Power Supply Currents			
I _{DD} Current (Normal Mode) ⁴	1.5	mA max	V _{DD} = 3 V, 1.3 mA typ
	1.7	mA max	V _{DD} = 5 V, 1.5 mA typ
I _{DD} (Power-Down Mode, $\overline{CS}$ = 1)	9	μA max	V _{DD} = 3 V, 6 μA typ
	24	μA max	V _{DD} = 5 V, 20 μA typ

NOTES

¹Temperature range –40°C to +85°C.²Guaranteed by design and/or characterization data on production release.³When a 28.8 kHz crystal is used, normal-mode rejection is improved so that the rejection equals 75 dB at 50 Hz ±1 Hz and equals 66 dB at 60 Hz ±1 Hz.⁴Normal mode refers to the case where the ADC is running.

Specifications subject to change without notice.

TIMING CHARACTERISTICS^{1, 2}

($V_{DD} = 2.7\text{ V to }3.6\text{ V or }4.75\text{ V to }5.25\text{ V}$; $GND = 0\text{ V}$; $XTAL = 32.768\text{ kHz}$;
Input Logic 0 = 0 V, Logic 1 = V_{DD} , unless otherwise noted.)

Parameter	Limit at T_{MIN} , T_{MAX} (B Version)	Unit	Conditions/Comments
t_1	30.5176	$\mu\text{s typ}$	Crystal Oscillator Period
t_{ADC}	50.54	ms typ	19.79 Hz Update Rate
t_2	0	ns min	$\overline{CS}$ Falling Edge to DOUT Active
	60	ns max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$
	80	ns max	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$
t_3	$2 \times t_{ADC}$	ns typ	Channel Settling Time
t_4^3	0	ns min	SCLK Active Edge to Data Valid Delay ⁴
	60	ns max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$
	80	ns max	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$
t_7^5	10	ns min	Bus Relinquish Time after $\overline{CS}$ Inactive Edge
	80	ns max	
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Inactive Edge Hold Time
t_9	10	ns min	SCLK Inactive to DOUT High
	80	ns max	
Slave Mode Timing			
t_5	100	ns min	SCLK High Pulse Width
t_6	100	ns min	SCLK Low Pulse Width
Master Mode Timing			
t_5	$t_1/2$	$\mu\text{s typ}$	SCLK High Pulse Width
t_6	$t_1/2$	$\mu\text{s typ}$	SCLK Low Pulse Width
t_{10}	$t_1/2$	$\mu\text{s min}$	DOUT Low to First SCLK Active Edge ⁴
	$3t_1/2$	$\mu\text{s max}$	

NOTES

¹Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

²See Figure 2.

³These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

⁴SCLK active edge is falling edge of SCLK.

⁵These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

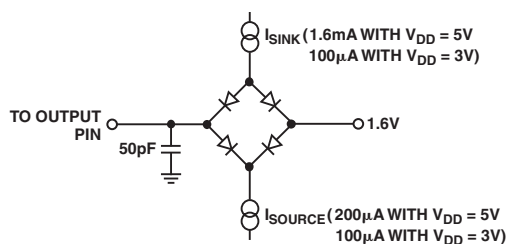


Figure 1. Load Circuit for Timing Characterization

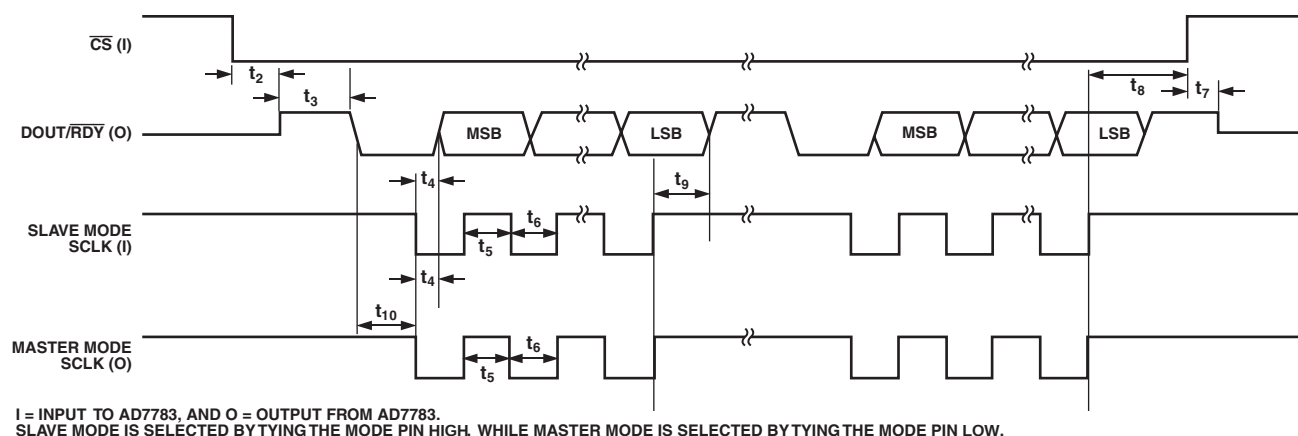


Figure 2. Slave/Master Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS*(T_A = 25°C, unless otherwise noted.)

V _{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V _{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V _{DD} + 0.3 V
Total AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to GND	−0.3 V to V _{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V _{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

TSSOP Package

θ _{JA} Thermal Impedance	97.9°C/W
θ _{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

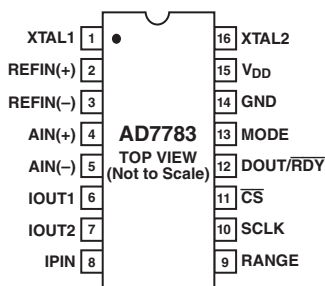
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7783 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



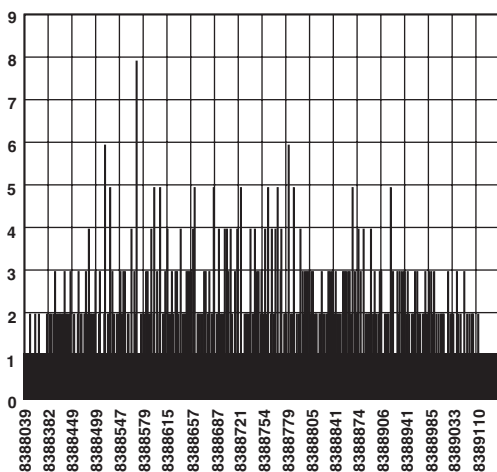
PIN CONFIGURATION



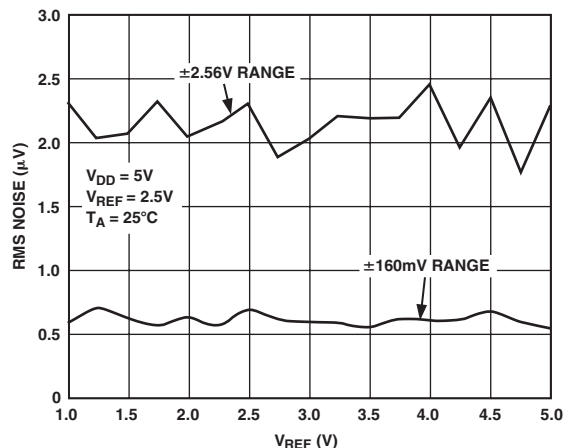
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	XTAL1	Input to the 32.768 kHz Crystal Oscillator Inverter.
2	REFIN(+)	Positive Reference Input. REFIN(+) can lie anywhere between V_{DD} and GND + 1 V. The nominal reference voltage (REFIN(+) – REFIN(-)) is 2.5 V, but the part functions with a reference from 1 V to V_{DD} .
3	REFIN(-)	Negative Reference Input. This reference input can lie anywhere between GND and $V_{DD} - 1$ V.
4	AIN(+)	Analog Input. AIN(+) is the positive terminal of the fully differential analog input pair AIN(+)/AIN(-).
5	AIN(-)	Analog Input. AIN(-) is the negative terminal of the fully differential analog input pair AIN(+)/AIN(-).
6	IOUT1	Output from Internal 200 μ A Excitation Current Source. Either current source IEXC1 or IEXC2 can be switched to this output using hardware control pin IPIN.
7	IOUT2	Output from Internal 200 μ A Excitation Current Source. Either current source IEXC1 or IEXC2 can be switched to this output using hardware control pin IPIN.
8	IPIN	Logic Input that Selects the Routing of the On-Chip Current Sources. When IPIN is tied to GND, IEXC1 is routed to IOUT1 and IEXC2 is routed to IOUT2. When IPIN is tied to V_{DD} , IEXC1 is routed to IOUT2 and IEXC2 is routed to IOUT1.
9	RANGE	Logic Input that Configures the Input Range on the Internal PGA. With RANGE = 0, the full-scale input range is ± 160 mV; the full-scale input range equals ± 2.56 V when RANGE = 1 for a 2.5 V reference.
10	SCLK	Serial Clock Input/Output for Data Transfers from the ADC. When the device is operated in master mode, SCLK is an output with one SCLK period equal to one XTAL period. In slave mode, SCLK is generated by an external source. In slave mode, all the data can be transmitted on a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted from the AD7783 in smaller batches of data. SCLK is Schmitt triggered (slave mode), making the interface suitable for opto-isolated applications.
11	$\overline{CS}$	Chip Select Input. $\overline{CS}$ is an active low logic input used to select the AD7783. When $\overline{CS}$ is low, the PLL establishes lock and allows the AD7783 to initiate a conversion. When $\overline{CS}$ is high, the conversion is aborted, DOUT and SCLK are three-stated, the AD7783 enters standby mode, and any conversion result in the output shift register is lost.
12	DOUT/ $\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/ $\overline{RDY}$ serves a dual purpose in this interface. When a conversion is initiated, DOUT/ $\overline{RDY}$ goes high and remains high until the conversion is complete. DOUT/ $\overline{RDY}$ will then return low to indicate that valid data is available to be read from the device. In slave mode, this acts as an interrupt to the processor, indicating that valid data is available. If data is not read after a conversion, DOUT/ $\overline{RDY}$ will go high before the next update occurs. In master mode, DOUT/ $\overline{RDY}$ goes low for at least half an SCLK cycle before the device produces SCLKs. When SCLK becomes active, data is output on the DOUT/ $\overline{RDY}$ pin. Data is output on the falling SCLK edge and is valid on the rising edge.
13	MODE	The MODE pin selects master or slave mode of operation. When MODE = 0, the AD7783 operates in master mode; the AD7783 is configured for slave mode when MODE = 1.
14	GND	Ground Reference Point for the AD7783.
15	V_{DD}	Supply Voltage, 3 V or 5 V Nominal.
16	XTAL2	Output from the 32.768 kHz Crystal Oscillator Inverter.

Typical Performance Characteristics—AD7783



TPC 1. Noise Distribution Histogram



TPC 2. RMS Noise vs. Reference Input

ADC CIRCUIT INFORMATION

Overview

The AD7783 incorporates a Σ - Δ ADC channel, on-chip programmable gain amplifier, and on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain gage, pressure transducer, or temperature measurement applications.

This ADC input is buffered and can be programmed to have an input voltage range of ± 160 mV or ± 2.56 V. The input channel is configured as a fully differential input. Buffering the input channel means that the part can accommodate significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog input if required. The device requires an external reference of 2.5 V nominal. Figure 3 shows the basic connections required to operate the part.

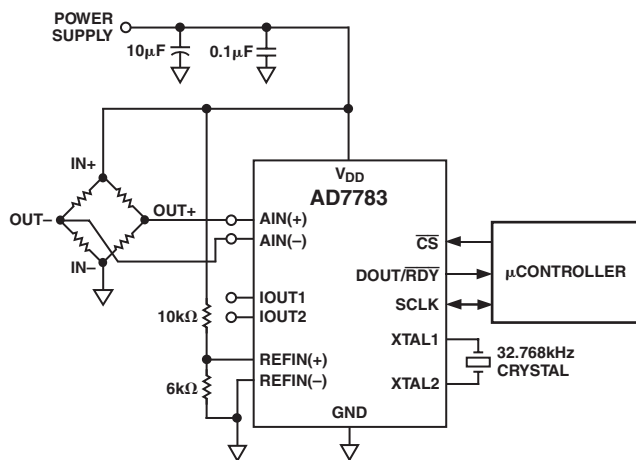


Figure 3. Basic Connection Diagram

The output rate of the AD7783 (f_{ADC}) equals

$$f_{ADC} = 32.768 \times 10^3 / (69 \times 8 \times 3)$$

while the settling time equals

$$t_{SETTLE} = \left(\frac{2}{f_{ADC}} \right) = 2 \times t_{ADC}$$

Normal-mode rejection is the major function of the digital filter on the AD7783. Simultaneous 50 Hz and 60 Hz rejection of better than 60 dB is achieved as notches are placed at both 50 Hz and 60 Hz. Figure 4 shows the filter rejection.

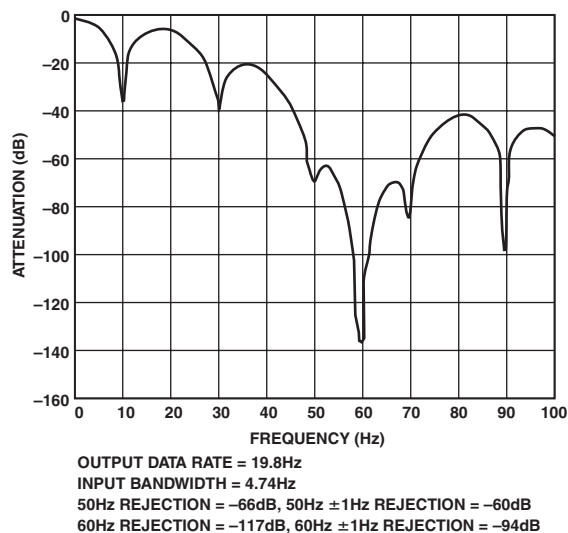


Figure 4. Filter Profile (Filter Notches at Both 50 Hz and 60 Hz)

NOISE PERFORMANCE

Table I shows the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for the two input voltage ranges. The numbers are typical and are generated at a differential input voltage of 0 V. The peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

Table I. Typical Output RMS Noise and Peak-to-Peak Resolution vs. Input Range

	Input Range	
	± 160 mV	± 2.56 V
Noise (μ V)	0.65	2.30
Peak-to-Peak Resolution (Bits)	16.5	18.5

DIGITAL INTERFACE

The AD7783's serial interface consists of four signals: $\overline{CS}$, SCLK, DOUT/RDY, and MODE. The MODE pin is used to select the master/slave mode of operation. When the part is configured as a master, SCLK is an output; SCLK is an input when slave mode is selected. Data transfers take place with respect to this SCLK signal. The DOUT/RDY line is used for accessing data from the data register. This pin also functions as a RDY line. When a conversion is complete, DOUT/RDY goes low to indicate that data is ready to be read from the AD7783's data register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when *not* to read from the device to ensure that a data read is not attempted while the register is being updated. The digital conversion is also output on this pin.

$\overline{CS}$ is used to select the device and to place the device in standby mode. When $\overline{CS}$ is taken low, the AD7783 is powered up, the PLL locks, and the device initiates a conversion. The device will continue to convert until $\overline{CS}$ is taken high. When $\overline{CS}$ is taken high, the AD7783 is placed in standby mode, minimizing the current consumption. The conversion is aborted, DOUT and SCLK are three-stated, and the result in the data register is lost.

Figure 2 shows the timing diagram for interfacing to the AD7783 with $\overline{CS}$ used to decode the part.

MASTER MODE (MODE = 0)

In this mode, SCLK is provided by the AD7783. With $\overline{CS}$ low, SCLK becomes active when a conversion is complete and generates 24 falling and rising edges. The DOUT/RDY pin, which is normally high, goes low to indicate that a conversion is complete. Data is output on the DOUT/RDY pin following the SCLK falling edge and is valid on the SCLK rising edge. When the 24-bit word has been output, SCLK idles high until the next conversion is complete. DOUT/RDY returns high and will remain high until another conversion is available. It then operates as a RDY signal again. The part will continue to convert until $\overline{CS}$ is taken high. SCLK and DOUT/RDY are three-stated when $\overline{CS}$ is taken high.

SLAVE MODE (MODE = 1)

In slave mode, the SCLK is generated externally. SCLK must idle high between data transfers. With $\overline{CS}$ low, DOUT/RDY goes low when a conversion is complete. Twenty-four SCLK pulses are needed to transfer the digital word from the AD7783. Twenty-four consecutive pulses can be generated or, alternatively, the data transfer can be split into batches. This is useful when interfacing to a microcontroller that uses 8-bit transfers. Data is output following the SCLK falling edge and is valid on the SCLK rising edge.

CIRCUIT DESCRIPTION

Analog Input Channel

The ADC has one fully differential input channel. It feeds into a high impedance input stage of the buffer amplifier. As a result, the ADC input can handle significant source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gages or resistance temperature detectors (RTDs).

The absolute input voltage range on the ADC input is restricted to a range between $GND + 100$ mV and $V_{DD} - 100$ mV. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded; otherwise, there will be a degradation in linearity and noise performance.

Programmable Gain Amplifier

The output from the buffer on the ADC is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA gain range is programmed via the RANGE pin. With an external 2.5 V reference applied, the PGA can be programmed to have a bipolar range of ± 160 mV (RANGE = 0) or ± 2.56 V (RANGE = 1). These are the ranges that should appear at the input to the on-chip PGA.

Bipolar Configuration/Output Coding

The analog input on the AD7783 accepts bipolar input voltage ranges. Signals on the AIN(+) input of the ADC are referenced

to the voltage on the AIN(–) input. For example, if AIN(–) is 2.5 V and the AD7783 is configured for an analog input range of ± 160 mV, the analog input range on the AIN(+) input is 2.34 V to 2.66 V (i.e., $2.5 \text{ V} \pm 0.16 \text{ V}$).

The coding is offset binary with a negative full-scale voltage resulting in a code of 000 . . . 000, a zero differential voltage resulting in a code of 100 . . . 000, and a positive full-scale voltage resulting in a code of 111 . . . 111. The output code for any analog input voltage can be represented as follows:

$$\text{Code} = 2^{N-1} \times \left[\left(\text{AIN} \times \text{GAIN} / (1.024 \times V_{\text{REF}}) \right) + 1 \right]$$

where AIN is the analog input voltage, GAIN is the PGA gain, i.e., 1 on the ± 2.56 V range and 16 on the ± 160 mV range, and $N = 24$.

Excitation Currents

The AD7783 also contains two matched 200 μA constant current sources. Both source current from V_{DD} that is directed to either the IOUT1 or IOUT2 pins of the device depending on the polarity of the IPIN pin. These current sources can be used to excite external resistive bridge or RTD sensors.

Crystal Oscillator

The AD7783 is intended for use with a 32.768 kHz watch crystal. A PLL internally locks onto a multiple of this frequency to provide a stable 4.194304 MHz clock for the ADC. The modulator sample rate is the same as the crystal oscillator frequency. The start-up time associated with 32.768 kHz crystals is typically 300 ms. In some cases, it will be necessary to connect capacitors on the crystal to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary depending on the manufacturer's specifications.

Reference Input

The AD7783 has a fully differential reference input capability for the channel. The common-mode range for differential inputs is from GND to V_{DD} . The reference input is unbuffered, and therefore excessive R-C source impedances will introduce gain errors. The reference voltage REFIN (REFIN(+) – REFIN(–)) is 2.5 V nominal for specified operation, but the AD7783 is functional with reference voltages from 1 V to V_{DD} . In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed as the application is ratiometric. If the AD7783 is used in a nonratiometric application, a low noise reference should be used. Recommended reference voltage sources for the AD7783 include the AD780, REF43, and REF192. It should also be noted that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Recommended reference voltage sources (e.g., AD780) will typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on the REFIN(+) without introducing gain errors in the system.

Deriving the reference input voltage across an external resistor will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN pins would not be recommended in this type of circuit configuration.

Grounding and Layout

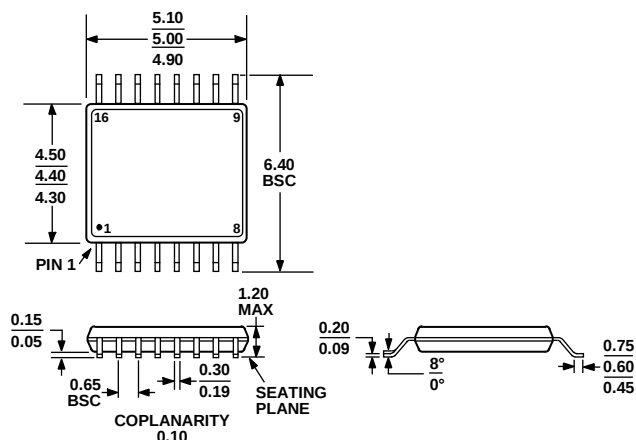
Since the analog inputs and reference inputs on the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided these noise sources do not saturate the analog modulator. As a result, the AD7783 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7783 is so high, and the noise levels from the AD7783 are so low, care must be taken with regard to grounding and layout. The printed circuit board that houses the AD7783 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes as it gives the best shielding.

It is recommended that the AD7783's GND pin be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The AD7783's ground plane should be allowed to run under the AD7783 to prevent noise coupling. The power supply lines to the AD7783 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. V_{DD} should be decoupled with 10 μF tantalum in parallel with 0.1 μF capacitors to GND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 μF ceramic capacitors to DGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 1. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD7783BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7783BRU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7783BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7783BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7783BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-AD7783EBZ	−40°C to +85°C	Evaluation Board	

¹ Z = RoHS Compliant Part.

REVISION HISTORY

10/11—Rev. B to Rev. C

Changes to Figure 2.....	5
Changes to Ordering Guide.....	10

8/04—Data Sheet Changed from Rev. A to Rev. B.

Change to Features.....	1
Changes to Ordering Guide.....	5

4/03—Data Sheet Changed from Rev. 0 to Rev. A.

Change to Specifications	2
Updated Outline Dimensions.....	10

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