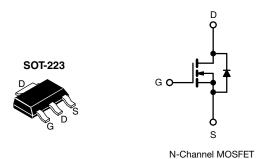


Vishay Siliconix

HALOGEN

FREE

### **Power MOSFET**



Marking code: FC

#### 

#### **FEATURES**

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- · Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>



Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Load (Dh) free and heleven free	SiHFL210TR-GE3 <sup>a</sup>
Lead (Pb)-free and halogen-free	IRFL210TRPbF-BE3 a, b
Lead (Pb)-free	IRFL210TRPbF <sup>a</sup>

#### Notes

- a. See device orientation
- b. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ( $T_C$	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	200	.,	
Gate-source voltage		$V_{GS}$	± 20	- V		
Continuous dusin surrent	\/ at 10.\/	T <sub>C</sub> = 25 °C T <sub>C</sub> = 100 °C	1	0.96		
Continuous drain current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	0.6	Α	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	7.7		
Linear derating factor				0.025	W/°C	
Linear derating factor (PCB mount) e			-	0.017	VV/ C	
Single pulse avalanche energy b			E <sub>AS</sub>	50	mJ	
Avalanche current a			I <sub>AR</sub>	0.96	А	
Repetitive avalanche energy <sup>a</sup>	petitive avalanche energy a		E <sub>AR</sub>	0.31	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		Б	3.1	W	
Maximum power dissipation (PCB mount) e	T <sub>A</sub> = 25 °C		$P_{D}$	2.0		
Peak diode recovery dv/dt c	•		dV/dt	5.0	V/ns	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	)	
Soldering recommendations (peak temperature) d	For	10 s	_	300	°C	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b.  $V_{DD} = 50$  V, starting  $T_J = 25$  °C, L = 81 mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 0.96$  A (see fig. 12)
- c.  $I_{SD} \le 3.3$  A,  $dI/dt \le 70$  A/ $\mu$ s,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150$  °C
- d. 1.6 mm from case
- e. When mounted on 1" square PCB (FR-4 or G-10 material)

Document Number: 91193



# Vishay Siliconix

THERMAL RESISTANCE RAT	INGS				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	40	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	-	60	

#### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static					L	L	
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		200	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I <sub>D</sub> = 1 mA	-	0.30	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>		V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>		= 200 V, V <sub>GS</sub> = 0 V	-	-	25	μΑ
			/, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	<u> </u>
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 0.58 A <sup>b</sup>	-	-	1.5	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub> =	= 50 V, I <sub>D</sub> = 0.58 A	0.51	-	-	S
Dynamic		1			1	ı	<u> </u>
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. 5}$		-	140	-	pF
Output capacitance	C <sub>oss</sub>			-	53	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	15	-	
Total gate charge	Qg		I <sub>D</sub> = 3.3 A, V <sub>DS</sub> = 160 V,	-	-	8.2	nC
Gate-source charge	$Q_{gs}$	V <sub>GS</sub> = 10 V	see fig. 6 and 13 b	-	-	1.8	
Gate-drain charge	$Q_gd$			-	-	4.5	
Turn-on delay time	t <sub>d(on)</sub>	$V_{DD} = 100 \text{ V, } I_D = 3.3 \text{ A,}$ $R_g = 24 \ \Omega, \ R_D = 30 \ \Omega, \text{ see fig. } 10^{\text{ b}}$		-	8.2	-	- ns
Rise time	t <sub>r</sub>			-	17	-	
Turn-off delay time	t <sub>d(off)</sub>			ı	14	-	
Fall time	t <sub>f</sub>			-	8.9	-	
Internal drain inductance	$L_D$	6 mm (0.25")	Between lead, 6 mm (0.25") from		4.0	-	nH
Internal source inductance	L <sub>S</sub>	package and center of die contact		-	6.0	-	1 11111
Drain-Source Body Diode Characteristic	es						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	0.96	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	7.7	
Body diode voltage	V <sub>SD</sub>	$T_J = 25  ^{\circ}\text{C},  I_S = 0.96  \text{A},  V_{GS} = 0  \text{V}^{ \text{b}}$		-	-	2.0	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.3 A, dI/dt = 100 A/μs b		-	150	310	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	0.60	1.4	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	v L <sub>s</sub> and	L <sub>D</sub> )

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

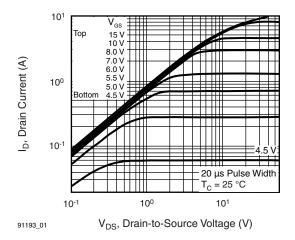
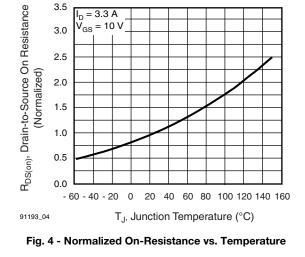


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C



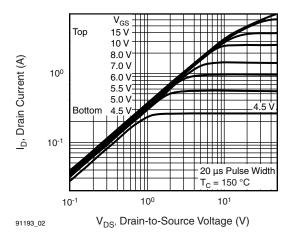


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

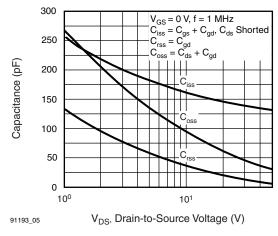


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

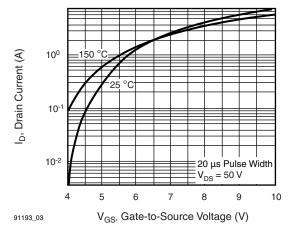


Fig. 3 - Typical Transfer Characteristics

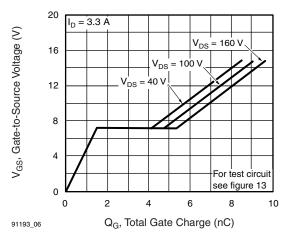


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



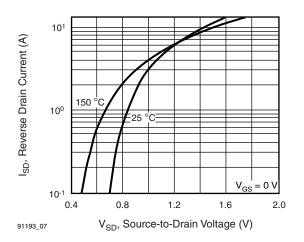


Fig. 7 - Typical Source-Drain Diode Forward Voltage

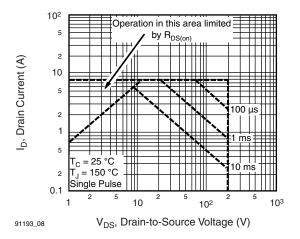


Fig. 8 - Maximum Safe Operating Area

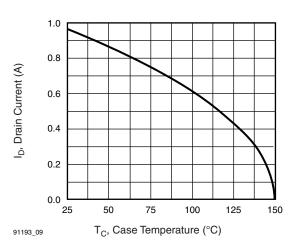


Fig. 9 - Maximum Drain Current vs. Case Temperature

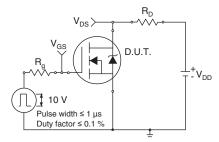


Fig. 10a - Switching Time Test Circuit

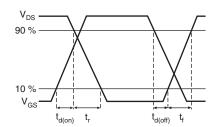


Fig. 10b - Switching Time Waveforms

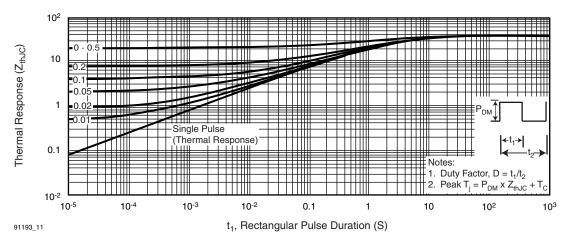


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



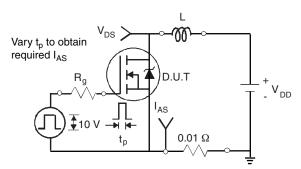


Fig. 12a - Unclamped Inductive Test Circuit

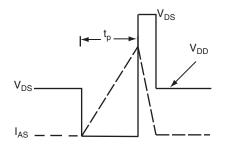


Fig. 12b - Unclamped Inductive Waveforms

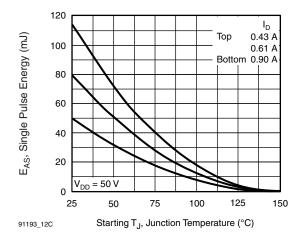


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

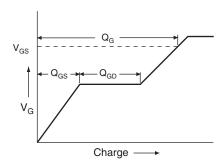


Fig. 13a - Basic Gate Charge Waveform

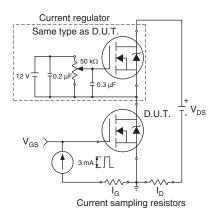
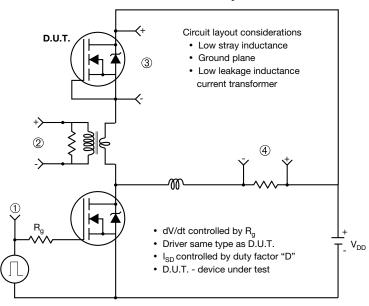


Fig. 13b - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



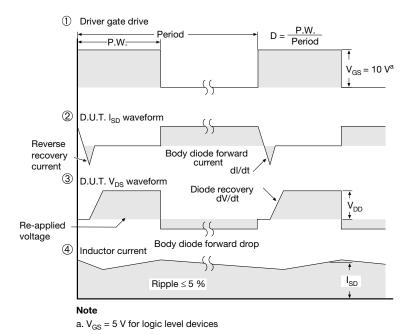


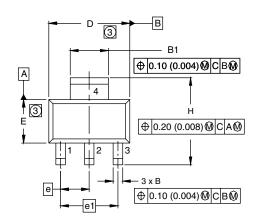
Fig. 14 - For N-Channel

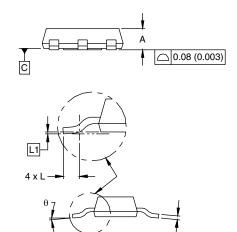
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### **SOT-223 (HIGH VOLTAGE)**





DIM.	MILLII	METERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	1.55	1.80	0.061	0.071	
В	0.65	0.85	0.026	0.033	
B1	2.95	3.15	0.116	0.124	
С	0.25	0.35	0.010	0.014	
D	6.30	6.70	0.248	0.264	
E	3.30	3.70	0.130	0.146	
е	2.30 BSC		0.0905 BSC		
e1	4.60 BSC		0.181	BSC	
Н	6.71	7.29	0.264	0.287	
L	0.91	-	0.036	-	
L1	0.061 BSC		0.0024	BSC	
θ	-	10'	-	10'	

ECN: S-82109-Rev. A, 15-Sep-08

DWG: 5969

#### Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension do not include mold flash.
- 4. Outline conforms to JEDEC outline TO-261AA.

Document Number: 91363 www.vishay.com Revision: 15-Sep-08



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