NIPPON PRECISION CIRCUITS LTD.

SM6103

CMOS 8-bit A/D Converter

OVERVIEW

The SM6103 is an 8-bit A/D converter fabricated in Molybdenum-gate CMOS. It features fast conversion times using a half-flash conversion method. It does not require an external sample-and-hold circuit, and can operate with or without an external microprocessor.

The SM6103 is AD7820- and ADC0820-equivalent and pin compatible. It is available in 20-pin plastic DIPs and 20-pin SOPs.

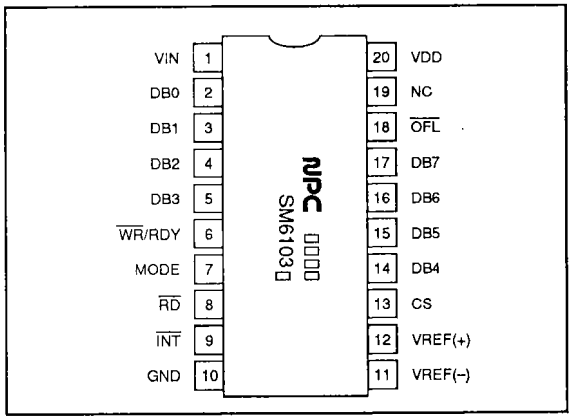
FEATURES

- 8-bit resolution
- 1.25 µs (max) conversion time in RD mode and 0.65 µs (max) in WR-RD mode
- AD7820- and ADC0820-equivalent and pin compatible
- External sample-and-hold circuit not required for input signals with less than 200 mV/s slew rate
- 8.5 mA (typ) current consumption (excluding VREF current)
- ±0.5 LSB non-linearity
- ±0.5 LSB differential non-linearity
- No external clock required
- Direct microprocessor interface
- TTL- and CMOS-compatible input/outputs
- Single 5 V supply
- 20-pin plastic DIP and 20-pin SOP
- Molybdenum-gate CMOS process

APPLICATIONS

- Data acquisition systems
- Measuring instruments
- Process control

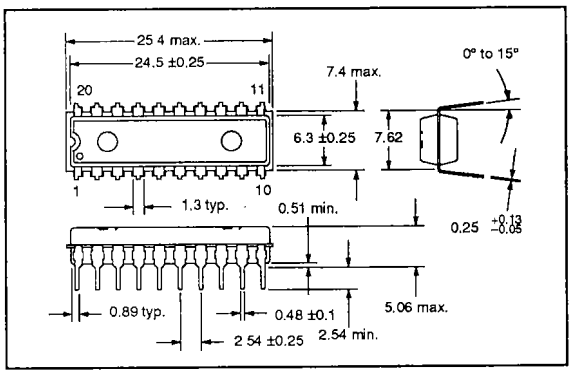
PINOUT



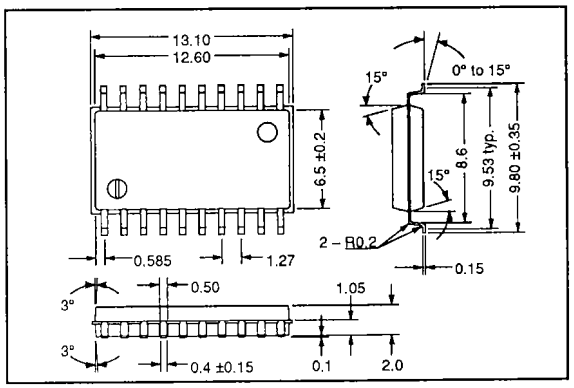
PACKAGE DIMENSIONS

Unit: mm

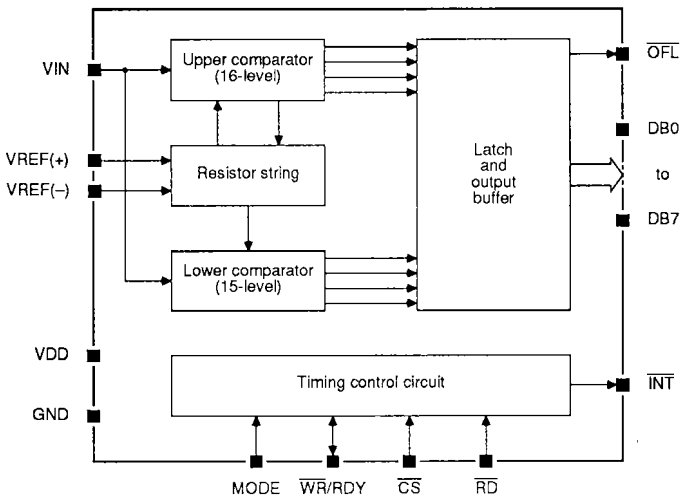
20-pin DIP (SM6103P)



20-pin SOP (SM6103S)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	VIN	Analog input. ($V_{REF-} \leq V_{IN} \leq V_{REF+}$)
2	DB0	Converter data output bit 0 (LSB)
3	DB1	Converter data output bit 1
4	DB2	Converter data output bit 2
5	DB3	Converter data output bit 3
6	$\overline{WR}$/RDY	WR-RD mode ($\overline{WR}$ input): Conversion is started on the falling edge of $\overline{WR}$. If $\overline{RD}$ is HIGH, the conversion is completed approx. 400 ns after the rising edge of $\overline{WR}$. $\overline{INT}$ then goes LOW and the data is latched. RD mode (RDY output): This is an N-channel open-drain output. RDY goes LOW on the falling edge of $\overline{CS}$. It enters a high-impedance state when conversion is completed.
7	MODE	Mode select input with internal pull-down resistance. RD mode when LOW or open and WR-RD mode when HIGH
8	RD	WR-RD mode: The results of the last conversion are output on DB0 to DB7 when $\overline{CS}$ and $\overline{INT}$ are LOW and $\overline{RD}$ is pulled LOW. If $\overline{RD}$ is pulled LOW before the internal conversion time has elapsed (approx. 400 ns), the conversion results are latched and output. RD mode: Conversion begins when $\overline{CS}$ is LOW and $\overline{RD}$ is pulled LOW. When conversion is completed, RDY goes high impedance and $\overline{INT}$ goes LOW.
9	$\overline{INT}$	$\overline{INT}$ goes LOW when conversion is completed and the data is latched. $\overline{INT}$ returns HIGH on the rising edge of $\overline{RD}$ or $\overline{CS}$
10	GND	Ground
11	VREF–	Reference voltage input (low end)
12	VREF+	Reference voltage input (high end)
13	$\overline{CS}$	Chip select input. $\overline{RD}$ and $\overline{WR}$ propagate through the internal circuits only when $\overline{CS}$ is LOW.
14	DB4	Converter data output bit 4
15	DB5	Converter data output bit 5
16	DB6	Converter data output bit 6
17	DB7	Converter data output bit 7 (MSB)

Number	Name	Description
18	$\overline{OFL}$	Overflow output. When the analog input voltage is (V_{REF+} – 0.5 LSB) or greater, $\overline{OFL}$ goes LOW. $\overline{OFL}$ can be used in cascade connection of 2 or more devices.
19	NC	No connection
20	VDD	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Storage tempeature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{sld}	260	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	T_{opr}	0	–	70	deg. C

DC Electrical Characteristics

V_{DD} = 5 V ±5%, T_a = –20 to 70 deg. C, V_{REF+} = 5 V ±5%, V_{REF-} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
VREF+ to VREF– reference resistance	R_{REF}		0.5	0.85	1.3	kΩ
VREF+ input voltage	V_{REF+}		V_{REF-}	–	V_{DD} + 0.3	V
VREF– input voltage	V_{REF-}		0	–	V_{REF+}	V
Analog input voltage	V_{IN}		–0.1		V_{DD} + 0.1	V
Analog input leakage current	I_{LEAK1}	V_{IN} = 0 V to V_{DD}, $V_{\overline{CS}}$ = V_{DD}	–	±0.1	±3	µA
$\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ HIGH-level input voltage	V_{IH1}		2.4	–	–	V
MODE HIGH-level input voltage	V_{IH2}		3.5	–	–	V
$\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ LOW-level input voltage	V_{IL1}		–	–	0.8	V
MODE LOW-level input voltage	V_{IL2}		–	–	1.5	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{CS}$ and $\overline{RD}$ HIGH-level input current	I_{IH1}	$V_{IH} = V_{DD}$	–	–	1	µA
$\overline{WR}$ HIGH-level input current	I_{IH2}	$V_{IH} = V_{DD}$	–	–	3	µA
MODE HIGH-level input current	I_{IH3}	$V_{IH} = V_{DD}$	–	60	–	µA
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and MODE LOW-level input current	I_{IL}	$V_{IL} = 0$ V	–1	–	–	µA
DB0 to DB7, $\overline{OFL}$ and $\overline{INT}$ HIGH-level output voltage	V_{OH}	$I_{source} = 360$ µA	4	–	–	V
DB0 to DB7, $\overline{OFL}$, $\overline{INT}$ and RDY LOW-level output voltage	V_{OL}	$I_{sink} = 1.6$ mA	–	–	0.4	V
DB0 to DB7 high-impedance leakage current	I_{LEAK2}	$V_{OUT} = V_{DD}$	–	–	3	µA
		$V_{OUT} = 0$ V	–3	–	–	
Current consumption	I_{DD}		–	8.5	16	mA
Analog input pin capacitance	C_{VIN}		–	25	–	pF
Logic output pin capacitance	C_{OUT}		–	5	–	pF
Logic input pin capacitance	C_{IN}		–	5	–	pF

AC Electrical Characteristics

V_{DD} = 5 V ±5%, V_{REF+} = 5 V ±5%, V_{REF-} = 0 V, $t_r = t_f$ = 20 ns, T_a = –20 to 70 deg. C

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
RD mode conversion time	t_{CRD}			–	0.8	1.25	µs
WR-RD mode conversion time	$t_{WR} + t_{RD} + t_{ACC1}$	$t_{WR-} = 220$ ns, $t_{RD} = 300$ ns		–	–	0.65	µs
Input signal slew rate	SR			–	–	0.2	V/µs
$\overline{CS}$ to RDY delay time	t_{RDY}	RD mode		–	30	60	ns
Data access time	t_{ACC}	RD mode. See note 2.		–	t_{CRD} + 20	t_{CRD} + 40	ns
$\overline{RD}$ to $\overline{INT}$ delay time	$t_{\overline{INTH}}$			–	50	100	ns
Data hold time	t_{DH}	See note 3.		–	50	100	ns
$\overline{WR}$ pulsewidth	t_{WR}	WR-RD mode		0.22	–	50	µs
$\overline{WR}$ to $\overline{RD}$ setup time	t_{RD}	WR-RD mode		300	–	–	ns
Data access time	t_{ACC1}	WR-RD mode. See note 2.		–	65	130	ns
$\overline{WR}$ to $\overline{INT}$ delay time	$t_{\overline{INTL}}$	WR-RD mode	$t_{RD} > t_i$	–	–	t_i	ns
			$t_{RD} < t_i$	–	t_{RD} + 50	t_{RD} + 100	
Internal comparator time	t_i	WR-RD mode		–	400	650	ns
Data access time	t_{ACC2}	WR-RD mode. See note 2.		–	50	100	ns
$\overline{RD}$ pulsewidth	$\overline{RD}_{PW}$	WR-RD mode		150	–	–	ns
$\overline{INT}$ to data delay time	t_{ID}	WR-RD mode (stand-alone operation) See note 2.		–	20	40	ns

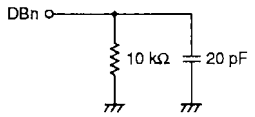
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Succeeding conversion wait time	t_p	WR-RD mode (stand-alone operation)	250	–	–	ns
		Other modes	100	–	–	

Notes

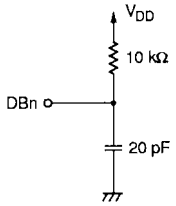
1. All timing is measured at a signal control level of 1.6 V.
2. Measured using the data access test circuits at output levels of 1.6 V.
3. Measured using the data hold test circuits at output levels of 1.6 V.

Data access test circuits

V_{OH} from high impedance

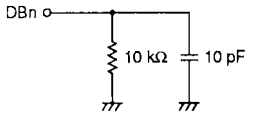


V_{OL} from high impedance

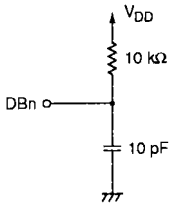


Data hold test circuit

High impedance from V_{OH}



High impedance from V_{OL}



Converter Characteristics

V_{DD} = 5 V ±5%, V_{REF+} = 5 ±0.5 V, V_{REF-} = 0 V, T_a = –20 to 70 deg. C

Parameter	Rating			Unit
	min	typ	max	
Resolution	–	–	8	bit
Non-linearity	–	–	±0.5	LSB
Differential non-linearity	–	–	±0.5	LSB
Offset error	–	–	±0.5	LSB
Gain error	–	–	±0.5	LSB

FUNCTIONAL DESCRIPTION

The SM6103 comprises two parallel A/D converters, one each for the upper and lower four bits of the 8-bit output.

When conversion begins, the fifteen comparators (sixteen including the overflow comparator) in the upper converter (upper four bits) set the threshold levels for the fifteen comparators in the lower converter (lower four bits). The data is then latched and buffered for output.

If the input analog signal rises above (V_{REF+} – 0.5 LSB), then $\overline{OFL}$ goes LOW immediately after conversion is completed to indicate the overflow condition.

The SM6103 has two basic modes of operation, set by the level on MODE. If MODE is LOW or open, RD mode is selected, and if MODE is HIGH, WR-RD mode is selected. The WR-RD mode also has sub-modes of operation, according to the timing of $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$.

RD Mode (MODE = LOW or open)

When $\overline{CS}$ is LOW, the CPU can strobe $\overline{RD}$ LOW. Conversion begins on the falling edge of $\overline{RD}$. $\overline{INT}$ goes LOW to signal the CPU that the conversion has completed approximately 0.8 µs later and the data is output. If RDY is connected to a pull-up resistor, RDY goes HIGH on the falling edge of $\overline{INT}$, thus acting as the bus wait signal for the CPU. $\overline{INT}$ returns HIGH and the outputs go high impedance on the rising edge of $\overline{RD}$ or $\overline{CS}$.

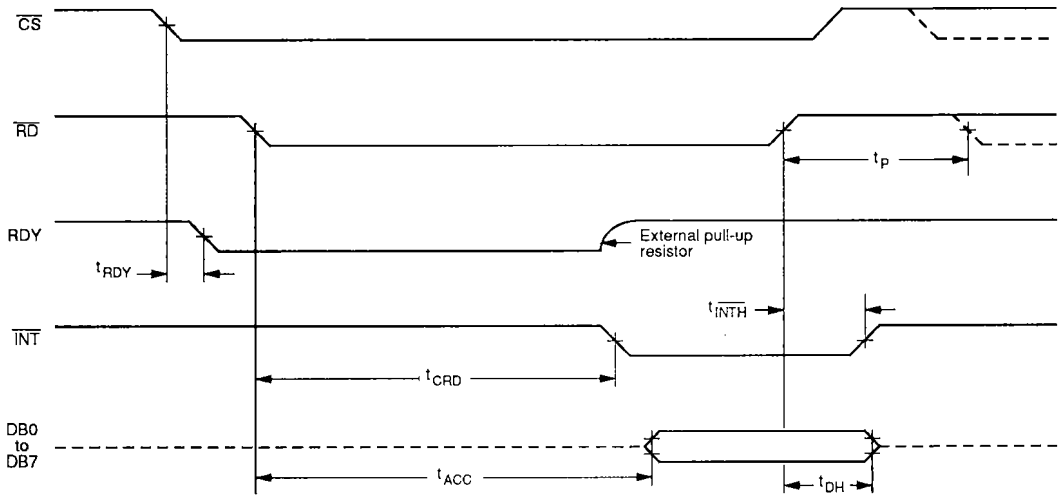


Figure 1. RD mode timing

WR-RD Mode (MODE = HIGH)

Mode A

When $\overline{CS}$ is LOW, either $\overline{RD}$ or $\overline{WR}$ can be pulled LOW. Conversion of the analog input begins on the falling edge of $\overline{WR}$. Conversion is completed and $\overline{INT}$ goes LOW approximately 400 ns after the rising edge of $\overline{WR}$, to inform the CPU that conversion is complete, and the output data is latched. When $\overline{RD}$ goes LOW, the output data is output on DB0 to DB7 to be read by the CPU. In this mode, the CPU is effectively performing interrupt processing.

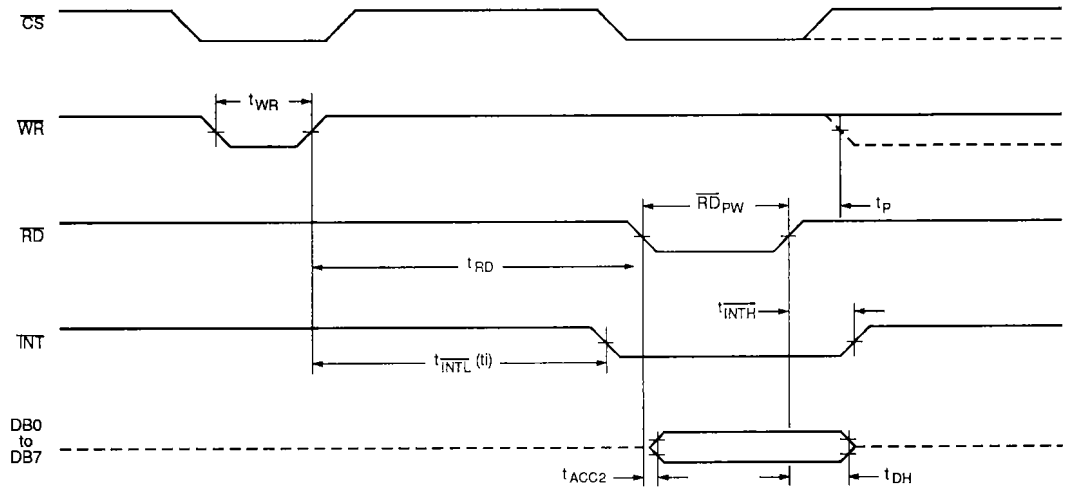


Figure 2. WR-RD mode (A) timing ($t_{RD} > t_i$)

Mode B

In mode B, $\overline{RD}$ is pulled LOW earlier to shorten the conversion cycle. Provided that the WR-RD setup time (t_{RD}) is satisfied, approximately 300 ns, $\overline{RD}$ can be pulled LOW to complete the conversion without error. $\overline{INT}$ then goes LOW and the output data is latched and output on DB0 to DB7. In this mode, the CPU is effectively polling the A/D converter.

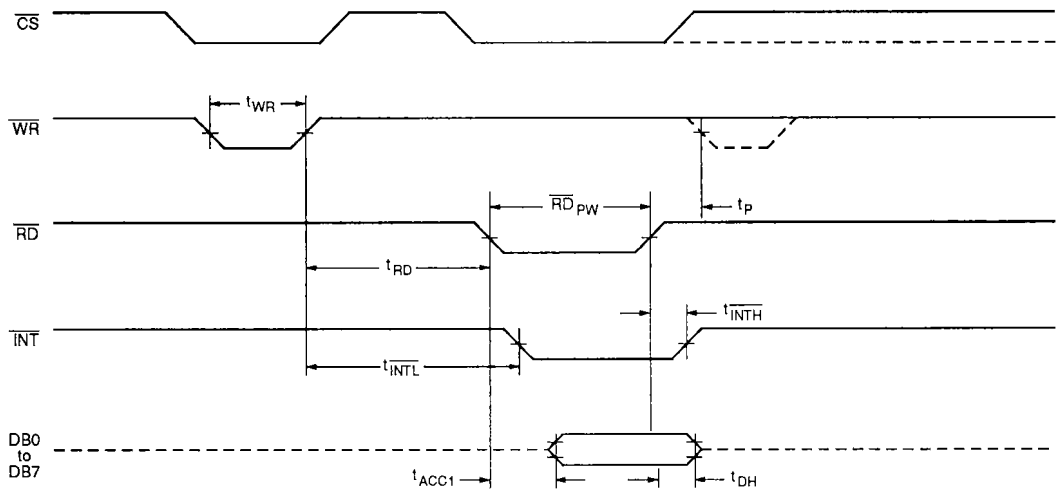


Figure 3. WR-RD mode (B) timing ($t_{RD} < t_i$)

Mode C

In mode C, $\overline{CS}$ and $\overline{RD}$ are both tied LOW to allow stand-alone operation (without an external microprocessor). Conversion begins on the falling edge of $\overline{WR}$. $\overline{INT}$ then goes HIGH on the rising edge of $\overline{WR}$, and the DB0 to DB7 outputs go high impedance. $\overline{INT}$ then goes LOW again approximately 400 ns after the rising edge of $\overline{WR}$, and the output data is output on DB0 to DB7.

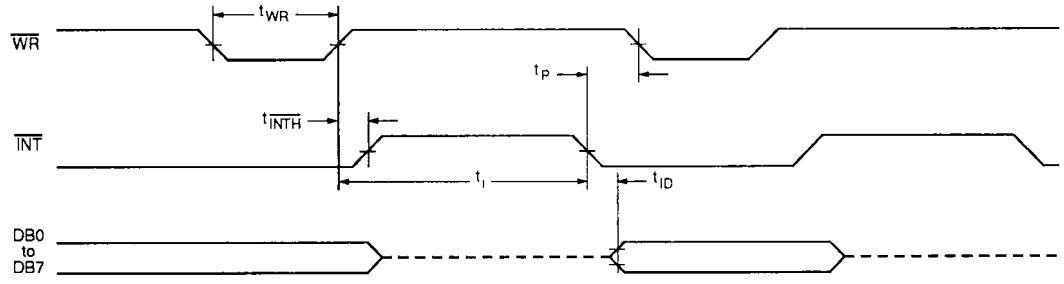
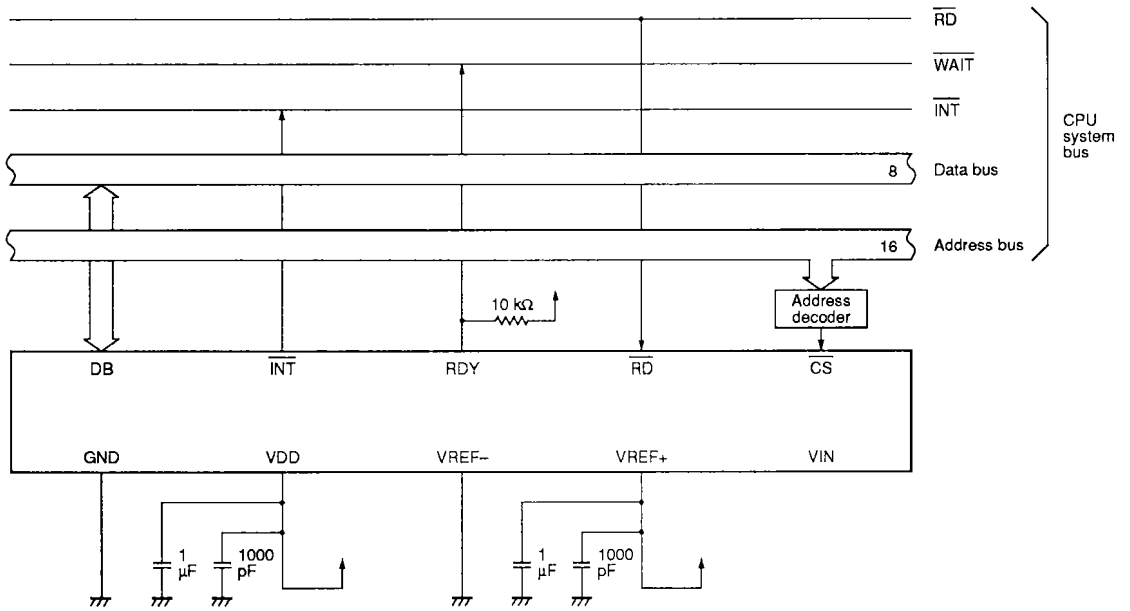


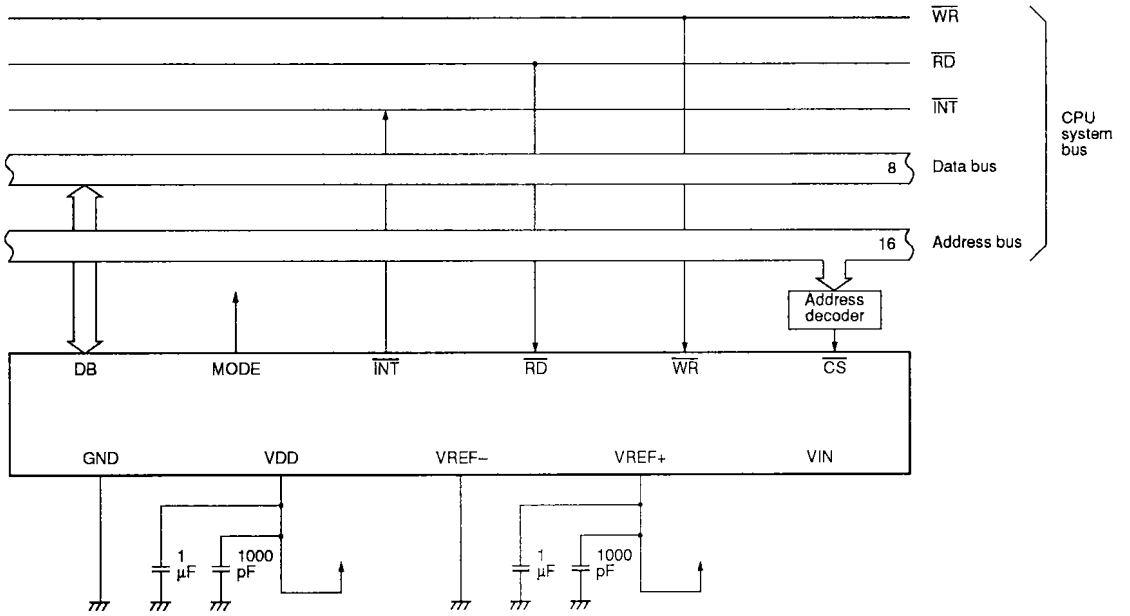
Figure 4. WR-RD mode (C) timing (stand-alone operation, $\overline{CS}$ = $\overline{RD}$ = LOW)

Standard Configuration

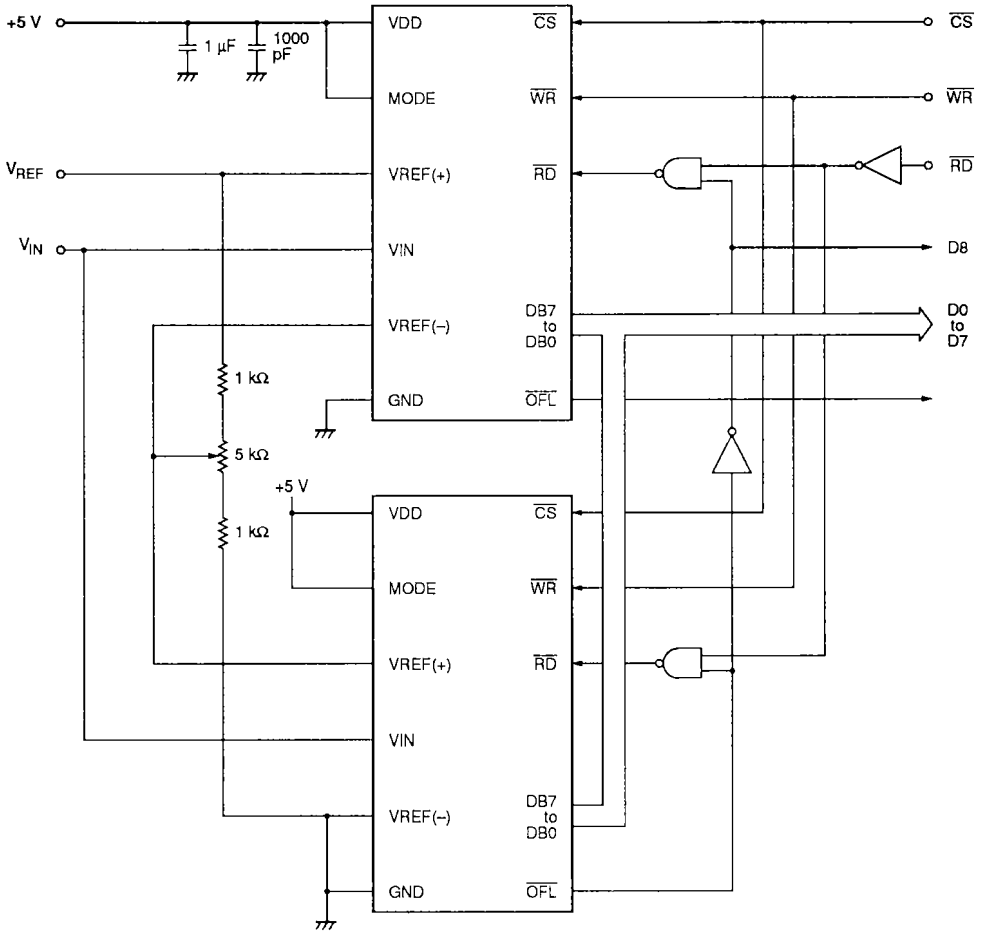
RD mode



WR-RD mode



TYPICAL APPLICATION (9-bit resolution)



DESIGN NOTE

The SM6103 uses CMOS chopper comparators where the analog input is alternately connected and disconnected from the input circuits. The analog input should, therefore, have a low impedance. Also, input buffering is recommended.

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