MK NAND FLASH Product Datasheet

Product List

MKPV32G08CT-ABG
4GB NAND Flash

http://www.mkfounder.com

Revision History

Version	Date	Description
Rev 1.0	2021/4/20	Original version

Notice :
The datasheet is prepared and approved by MK Founder semiconductor co., LTD.

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Table Of Contents

1 Introduction

1.1 Features

- Voltage Supply
  VCC: 3.3V (2.7V ~ 3.6V)
  VCCQ: 3.3V (2.7V ~ 3.6V)
- Organization
  Page Size: (16K + 1536) x Byte
  Data Register: (16K + 1536) x Byte
  Block Size: (12.375M + 1.188M) Byte
  Unit Device Capacity: (12.375M + 1.188M) Byte x 350
- Automatic Program and Erase
  Page Program: (16K + 1536)Byte
  Block Erase: (12.375M + 1.188M) Byte
- Page Read Operation
  Random Read: 90ns (Max.)
  Data Transfer Rate: up to 200Mbps or 100Mhz (VCCQ : 3.3V)
- Write Cycle Time
  Page Program Time: 1.0ms
  Block Erase Time: 5ms
- Toggle DDR Data Interface
- ECC Requirement: 48bits / 1KByte
- Randomizer Function Required by Controller
  Command/Address/Data Multiplexed DQ Port
  Hardware Data Protection
  Program/Erase Lockout During Power Transitions
  Command Driven Operation
  Scalable DQ Driver Strength
- Operating temperature:
  Commercial: 0°C to +70°C
- Package
  48-pin TSOP

1.2 Product List

Part Number	Density	Interface	VCC Range	VCCQ Range
MKPV32G08CT-ABG	32Gb	Toggle DDR	2.7V ~ 3.6V	2.7V ~ 3.6V

1.3 General Description

Toggle DDR is a NAND interface for high performance applications which support data read and write operations using bidirectional DQS.
Toggle DDR NAND has implemented 'Double Data Rate' without a clock. It is compatible with functions and command which have been supported in conventional type NAND(i.e. SDR NAND) while providing high data transfer rate based on the high-speed Toggle DDR Interface and saving power with separated DQ voltage. For applications that require high capacity and high performance NAND, Toggle DDR NAND is the most appropriate.
Toggle DDR2.0 NAND supports the interface speed of up to 200Mbps (100Mhz), which is more than 10 times faster than the data transfer rate offered by SDR NAND (40Mbps). Toggle DDR NAND transfers data at high speed by using DQS signal that behaves as a clock, and DQS shall be used only when data is transferred for optimal power consumption.

1.4 Toggle DDR Interface According to Data Transfer Rate

Feature		up to 200Mbps
VCCQ		3.3V
I/O Type	CMOS	Support
	VREFQ Support	Not Support
	Differential Signaling for DQS	Not Support

NOTE :
1) VREFQ shall be used for DQx when differential signaling is used.

1.5 Definitions and Abbreviations

- DDR

Acronym for double data rate.

Address

The address is comprised of a column address with 2 cycles and a row address with 3 cycles. The row address identifies the page, block and LUN to be accessed. The column address identifies the byte within a page to access. The least significant bit of the column address shall always be zero.

- Column

The byte location within the page register.

- Row

Refer to the block and page to be accessed.

- Page

The smallest addressable unit for the Read and the Program operations.

- Block

Consists of multiple pages and is the smallest addressable unit for the Erase operation.

- Page register

Register used to transfer data to and from the Flash Array.

- Defect area

The defect area is where factory defects are marked by the manufacturer. Refer to the section 3.2

- Device

The packaged NAND unit. A device may contain more than a target.

- LUN (Logical Unit Number)

The minimum unit that can independently execute commands and report status. There are one or more LUNs per CE

- Target

An independent NAND Flash component with its own CE signal.

- SR[x] (Read Status)

SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to Chapter 5.2.14 for the definition of bit meanings within the status register.

- VREFQ

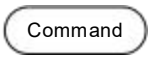
Input reference voltage.

- VTT

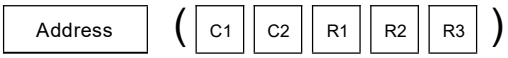
Termination voltage for output AC timing and DC level measurement.

1.6 Diagram Legend

Diagrams in the Toggle DDR3.0 datasheet use the following legend:
This legend shows the command data. Refer to the Table 28 for more information about the command data.



This legend shows the Address data. The address are comprised of 2 cycles column address and 3 cycles row address.

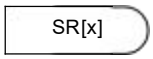


C1 : Column address 1
C2 : Column address 2
R1 : Row address 1
R2 : Row address 2
R3 : Row address 3

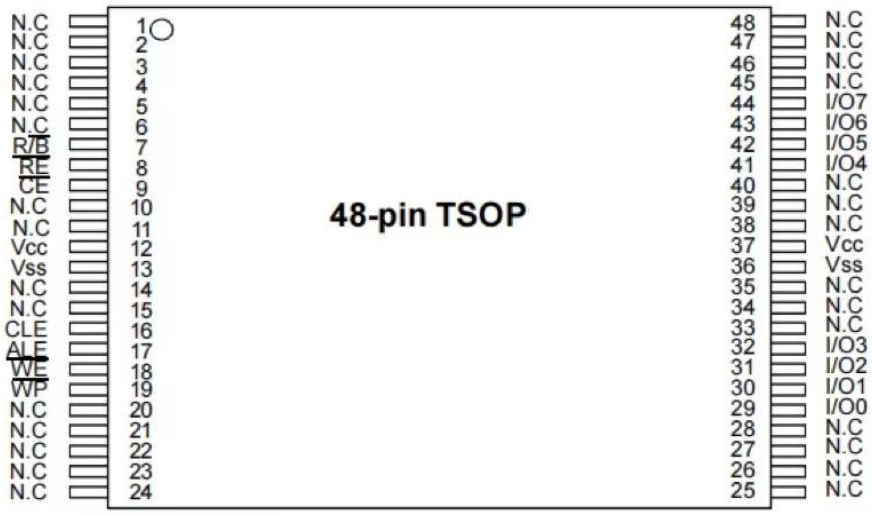
This legend shows Host writing data (data input) to the device.

This legend shows Host reading data (data output) from the device.

This legend shows Host reading the status register within a particular LUN.

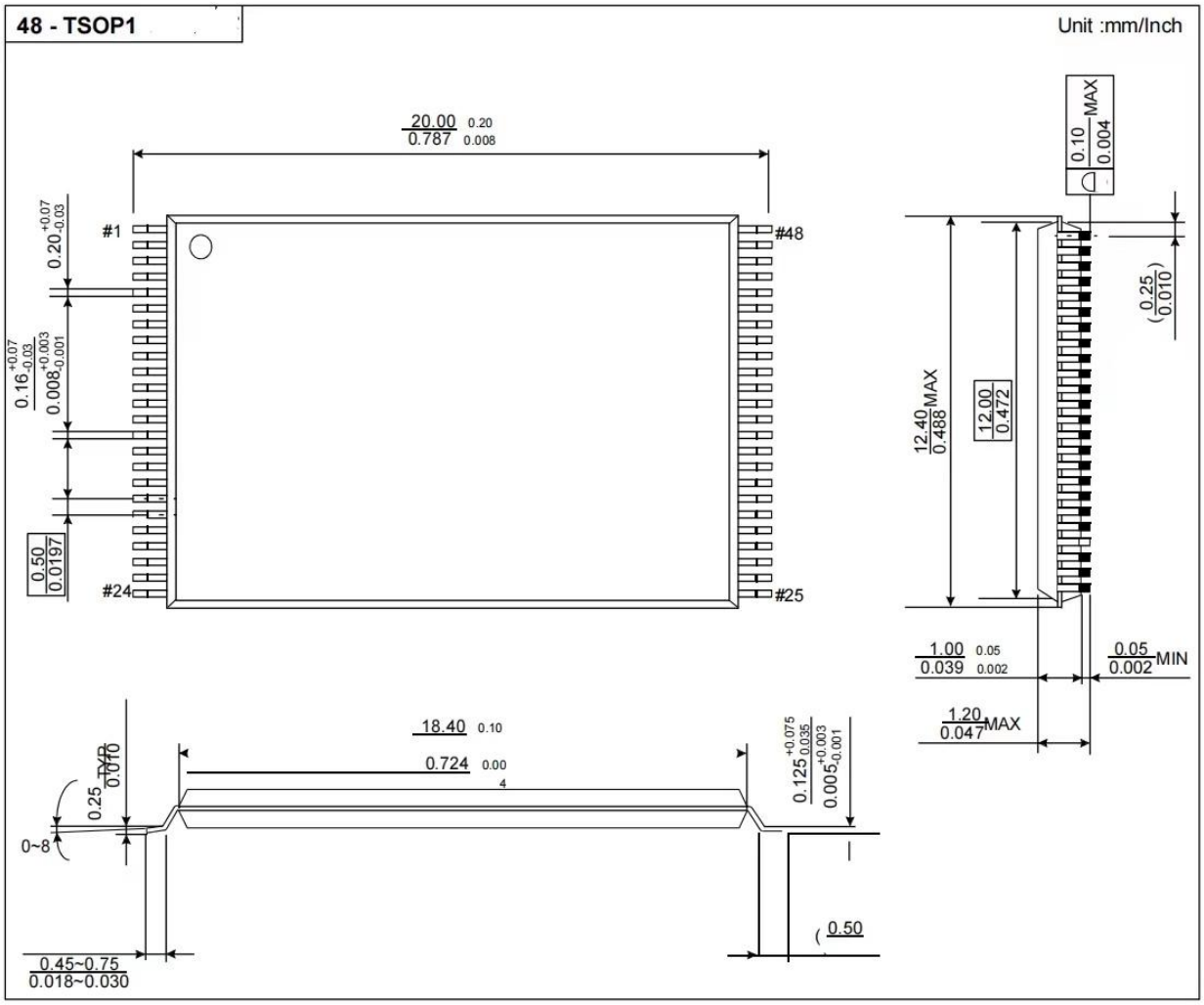


2 Signal Assignments



Note：48-Pin TSOP

3 Package Dimensions



4 PHYSICAL INTERFACE

4.1 Pin Descriptions

[Table 1] Pin Descriptions

Pin Name	Pin Function
DQ[7:0]	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data, and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the WE signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.
$\overline{CE}$	**CHIP ENABLE** The CE input is the device selection control. When the device is in the Busy state, CE high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$, (RE)	**READ ENABLE** The RE input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of RE, which also increments the internal column address counter by each one. The Read Enable RE is paired with differential signal RE to provide differential pair signaling to the system during reads.
WE	**WRITE ENABLE** The WE input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the WE pulse.
WP	**WRITE PROTECT** The WP pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read oper- ation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. R/B shall be tied to V_{CCQ}
V_{CC}	**POWER** V_{CC} is the power supply for device.
V_{SS}	**GROUND**
NC	**NO CONNECTION** A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.

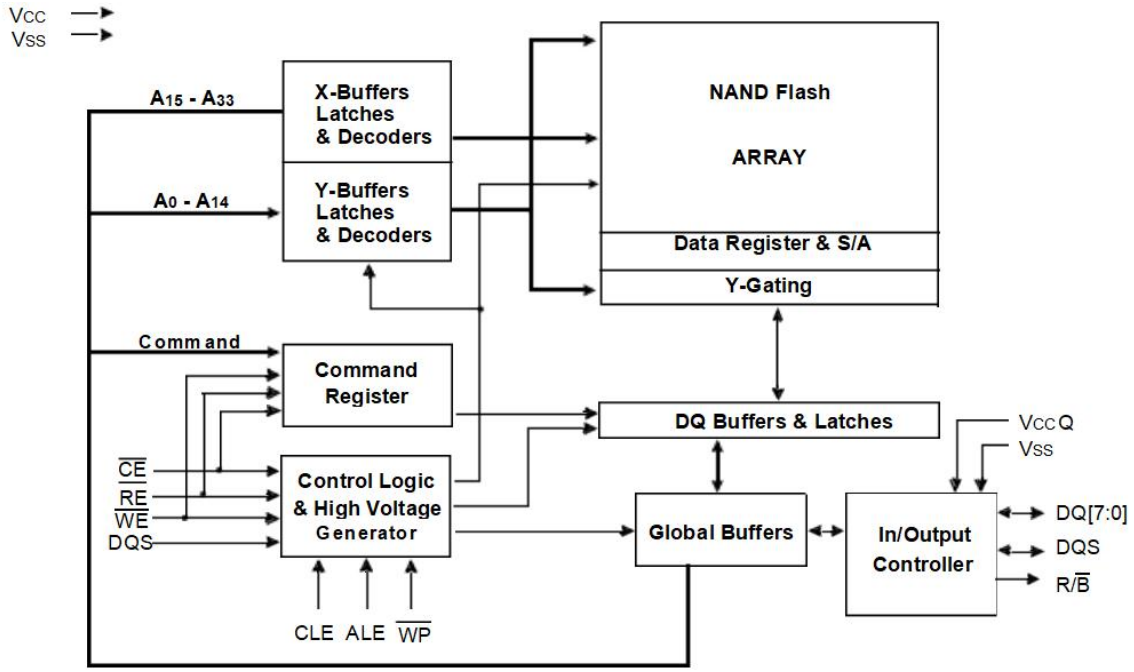


Figure 1. Functional Block Diagram

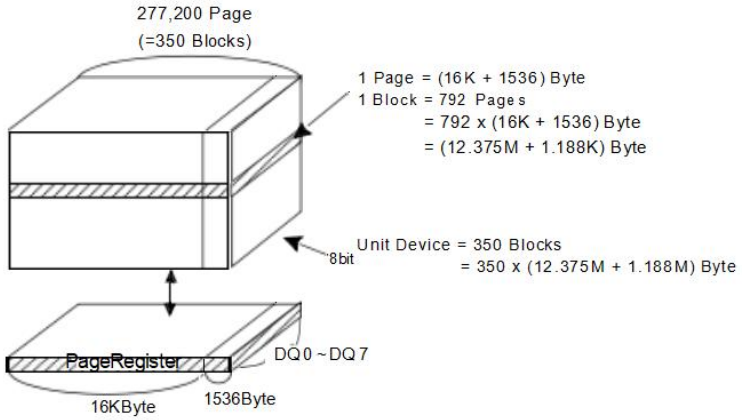


Figure 2. Array Organization of Unit Device

[Table 2] Address Mapping Table

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7	
1st Cycle	A01)	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	*L	
3rd Cycle	A15	A16	A17	A18	A19	A20	A21	A22	Row Address; Page Address : A15 - A24 Block Address : A25 ~ A33
4th Cycle	A23	A24	A25	A26	A27	A28	A29	A30	
5th Cycle	A31	A32	A33	**A34	*L	*L	*L	*L	

NOTE :

1) A0 must be set to "Low"

2) Data input/output unit should be 2-byte(16bit).

Column Address : Starting Address of the Register.

* When unused address bits shall be set to "Low".

* The device ignores any additional input of address cycles than required.

** A34 is used for DDP with a single CE

**A34 must be set to "Low" for SDP.

4.2 Valid Block

[Table 3] The Number of Valid Block per a CE

Part No.	Symbol	Min.	Typ.	Max.	Unit
MKPV32G08CT-ABG	NVB.	335	-	350	Blocks

NOTE :

1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.

2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

4.3 Absolute Maximum DC Rating

Stresses greater than those listing in Table 4 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating
conditions specified in Table 4 is not recommended. Extended exposure beyond these conditions may affect device reliability.

[Table 4] Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
		3.3 VccQ	
Voltage on any pin relative to VSS	VCC	-0.6 to +4.6	V
	VCCQ	-0.6 to +4.6	
	VIN	-0.6 to VCCQ + 0.3(<4.6)	
	VI/O		
	VPP	-0.6 to +16	
Storage Temperature	TSTG	-65 to +100	℃

NOTE :

Maximum DC voltage on input and I/O pins is VCCQ+0.3V which, during transition, may have overshoot that is defined in Table 7.

4.4 Operating Temperature Condition

[Table 5] Operating Temperature Condition

Symbol	Parameter	Rating	Unit
TOPER	Operating Temperature Range for Commercial	0 to +70	°C

NOTE :

1) Operating temperature (TOPER) is the case surface temperature on the center/top side of the NAND.

2) The normal temperature range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between 0-70°C for commercial under all operating conditions.

4.5 Recommended Operating Conditions

[Table 6] Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	2.7	3.3	3.6	V
Ground Voltage	VSS	0	0	0	V
Supply Voltage for 3.3V I/O Signaling	VCCQ	2.7	3.3	3.6	V
External High Voltage	VPP	11	12	13	V

NOTE :

1) VCC and VCCQ may be distinct and unique voltages. The device shall support one of the following VCC/VCCQ combinations，VCC= 3.3V, VCCQ = 3.3V

All parameters, timing modes and other characteristics are related to the supported voltage combination.

2) The maximum external VPP supply current per LUN is 5mA.

4.6 AC Overshoot / Undershoot Requirements

The device may have AC overshoot or undershoot from VCCQ and VSS levels. Table 7 defines the maximum values that the AC overshoot or undershoot may attain. These values apply for 3.3V VSS levels.

[Table 7] AC Overshoot / Undershoot Specification

Parameter	Maximum Value	Unit
	84~100Mhz	
Max. Peak Amplitude Allowed for Overshoot Area	1	V
Max. Peak Amplitude Allowed for Undershoot Area	1	V
Max. Overshoot Area Above VCCQ	1.5	V*ns
Max. Undershoot Area Above VSS	1.5	V*ns

NOTE :

1) This specification is intended for devices with no clamp protection and is guaranteed by design.

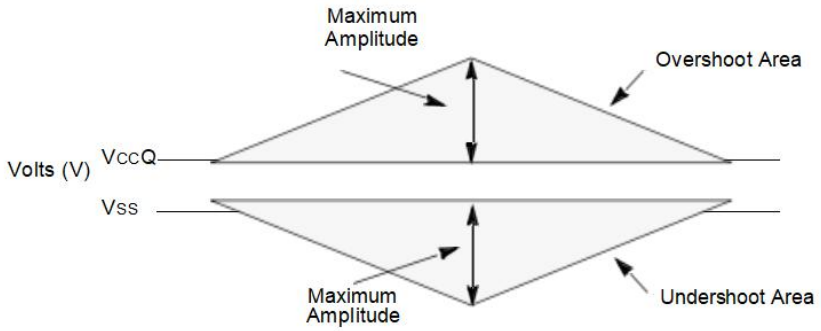


Figure 3. Overshoot / Undershoot Diagram

4.7 DC Operating Characteristics

[Table 8] DC & Operating Characteristics for VCCQ=3.3V

Parameter	Symbol	Test Conditions	1-Plane			Unit
			Min.	Typ.	Max.	
Page Read Operation Current	ICC1	-	-	-	50	mA
Page Program Operation Current	ICC2	-	-	-		
Erase Operation Current	ICC3	-	-	-		
DQ Burst Read Current	ICC4R	CLOAD=0pF (IOUT=0mA) CE=VIL, Half data switching tRC=10ns (100Mhz)	-	-	40	
	ICCQ4R		-	-	50	
DQ Burst Write Current	ICC4W	CE=VIL, Half data switching tDSC=10ns (100Mhz)	-	-	40	
	ICCQ4W		-	-	10	
Bus Idle Current	ICC5	-	-	-	10	
Stand-by Current (CMOS)	ISB	CE=VCCQ-0.2, WP=0V/VCCQ	-	-	50	µA
Input Leakage Current	ILI	VIN=0 to VCCQ (Max.)	-	-	±10	
Output Leakage Current	ILO	VUOT=0 to VCCQ (Max.)	-	-	±10	
Output High Voltage Level	VOH	IOH=-400µA	2.4	-	-	V
Output Low Voltage Level	VOL	IOL= 2.1mA	-	-	0.4	
Output Low Current (R/B)	IOL(R/B)	VOL=0.4V	8	10	-	mA

NOTE :

1) Typical value is measured at VCC=3.3V, TA=25°C. Not 100% tested.

2) VOH and VOL should be available on these two conditions; Output Strength is nominal and VCCQ=3.3V, Rpd/Rpu are all VCCQx0.5. If the driver strength settings are supported, Table 13 shall be used to derive the output driver impedance values.

4.8 AC & DC Input Measurement Levels

[Table 9] Single Ended without VREFQ AC & DC Input Level

Parameter	Symbol	Min.	Max.	Unit
DC Input Logic High	$V_{IH(DC)}$	0.7 x VccQ	VccQ + 0.3	V
DC Input Logic Low	$V_{IL(DC)}$	- 0.3	0.3 x VccQ	
AC Input Logic High	$V_{IH(AC)}$	0.8 x VccQ	-	
AC Input Logic Low	$V_{IL(AC)}$	-	0.2 x VccQ	

NOTE :
1) VIL can undershoot to -0.3V and VIH can overshoot to VCCQ +0.3V for durations of 20 ns or less.
2) VREFQ shall be used at high interface speed above 200Mbps.

4.9 VREFQ Tolerances

The DC-tolerance and AC-noise limits for the reference voltages. Figure 4 shows a valid reference voltage VREFQ(t) as a function of time.
VREFQ(DC) is the linear average of VREFQ(t) over a very long period of time (e.g. 1sec). This average has to meet the min/max requirements in Table 11. VREFQ(t) may temporarily deviate from VREFQ(DC) by no more than +/- 1% VCCQ
The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREFQ.
"VREFQ" shall be understood as VREFQ(DC), as defined in Figure 4.

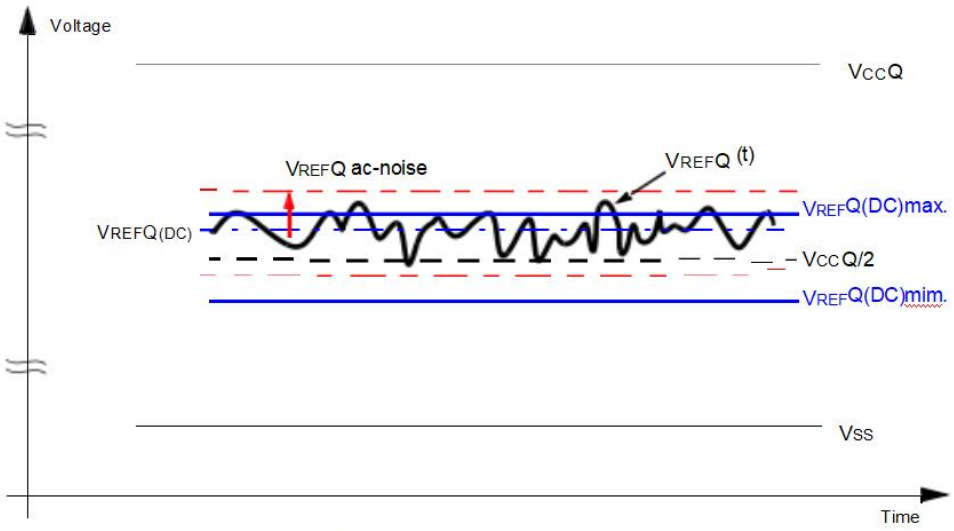


Figure 4. VREFQ(DC) Tolerance and VREFQ AC-noise Limits

4.10 Input/Output Capacitance (TA=25°C, VCC=3.3V, f=100Mhz)

[Table 10] Input/Output Capacitance

Item	Symbol	Test Condition	K9GBGD8U0E		Unit
			Min.	Max.	
Input/Output Capacitance	C_{DQ}	V_{IL}=0V	-	4.5	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	4.5	pF

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Under drive, Nominal options. The Toggle DDR supports all four driver strength settings. Devices that support driver strength settings shall comply with the output driver requirements in this section. A device is only required to meet driver strength values for 3.3V VCCQ, and is not required to meet driver strength values for 3.3V VCCQ and.

[Table 11] DQ Driver Strength Settings

Setting	Driver Strength	VccQ
Nominal	1.0x = 35 Ohms	3.3 V
Underdrive1	0.7x = 50 Ohms	

The impedance values corresponding to several different VCCQ values are defined in Table 13 for 3.3VQ. The test conditions that shall be used to verify the impedance values are specified in Table 12. The terms TOPER(Min.) and TOPER(Max.) are in reference to the minimum and maximum operating temperature defined for the device.

[Table 12] Testing Conditions for Impedance Values

Condition	Temperature	VccQ (3.3V)	Process
Minimum Impedance	T_{OPER}(Min.) Degrees Celsius	3.6 V	Fast - Fast
Nominal Impedance	25 Degrees Celsius	3.3 V	Typical
Maximum Impedance	T_{OPER}(Max.) Degrees Celsius	2.7 V	Slow - Slow

[Table 13] Output Driver Strength Impedance Values

Output Strength	Rpd/Rpu	V_{OUT} to Vss	Minimum	Nominal	Maximum	Units
			VccQ(3.3V)	VccQ(3.3V)	VccQ(3.3V)	
Nominal	Rpd	VccQ × 0.2	6.0	33.0	48.0	ohms
		VccQ × 0.5	16.0	35.0	51.0	ohms
		VccQ × 0.8	31.0	40.0	61.0	ohms
	Rpu	VccQ × 0.2	31.0	40.0	61.0	ohms
		VccQ × 0.5	16.0	35.0	51.0	ohms
		VccQ × 0.8	6.0	33.0	48.0	ohms
Underdrive 1	Rpd	VccQ × 0.2	16.0	47.0	64.0	ohms
		VccQ × 0.5	29.0	50.0	70.0	ohms
		VccQ × 0.8	43.0	56.0	83.0	ohms
	Rpu	VccQ × 0.2	43.0	56.0	83.0	ohms
		VccQ × 0.5	29.0	50.0	70.0	ohms
		VccQ × 0.8	16.0	47.0	64.0	ohms

[Table 14] Pull-up and Pull-down Output Impedance Mismatch

Driver Strength	3.3V		Unit
	Minimum	Maximum	
Nominal	0	9	ohms
Underdrive 1	0	12	ohms

NOTE :

1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.

2) Test conditions: VCCQ = VCCQ(min.), VOUT= VCCQ × 0.5, TA= TOPER

4.11 Input / Output Slew Rate

The input slew rate requirements that the device shall comply with are defined in Table 15 and Table 16. The output slew rate requirements that the device shall comply with are defined in Table 18. The testing conditions that shall be used to verify the input slew rate are listed in Table 17 and Table 19.

[Table 15] Derating factor

Input slew rate	200Mbps	Unit
	3.3VccQ	
2.0V/ns	-	ps
1.5V/ns	-	
1.0V/ns	0	
0.8V/ns	150	
0.6V/ns	350	

NOTE :

1) Derating factor is required when DQ slew rate is lower than minimum slew rate while the slew rate of DQS meets the minimum slew rate.

[Table 16] Input Slew Rate

VccQ	VIL	VIH	Min
			200Mbps
3.3V	0.2 x VccQ	0.8 x VccQ	1.0V/ns
Small swing	VREFQ -300mV	VREFQ +300mV	1.0V/ns

[Table 17] Testing Conditions for Input Slew Rate

Parameter	Value
Positive Input Transition	VIL (DC) to VIH (AC)
Negative Input Transition	VIH (DC) to VIL (AC)

[Table 18] Output Slew Rate Requirements

Parameter	VccQ=3.3V		Unit
	Minimum	Maximum	
Nominal	1.2	7.0	ohms
Underdrive 1	1.0	5.5	ohms

NOTE :
1) Measured with a test load of 5pF connected to VSS .
2) The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

[Table 19] Testing Conditions for Output Slew Rate

Parameter	Value
V_{OL}(DC)	0.3 * V_{CCQ}
V_{OH} (DC)	0.7 * V_{CCQ}
V_{OL}(AC)	0.2 * V_{CCQ}
V_{OH} (AC)	0.8 * V_{CCQ}
Positive Output Transition	V_{OL}(DC) to V_{OH} (AC)
Negative Output Transition	V_{OH} (DC) to V_{OL}(AC)
tRISE1)	Time during Rising Edge from V_{OL}(DC) to V_{OH} (AC)
tFALL1)	Time during Falling Edge from V_{OH} (DC) to V_{OL}(AC)
Output Slew Rate Rising Edge	(V_{OH} (AC) - V_{OL}(DC)) / tRISE
Output Slew Rate Falling Edge	(V_{OH} (DC) - V_{OL}(AC)) / tFALL
Output Capacitive load	C_L = 5pF

NOTE :
1)Refer to Figure 5.
2) Output slew rate is verified by design and characterization. It may not be subject to production test.
3) The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate.

Figure 5. tRISE and tFALL Definition for Output Slew Rate

4.12 R/B and SR[6] Relationship

R/B represents the status of the selected target. R/B goes busy when only a single LUN is busy while rest of LUNs on the same target are idle.

4.13 Write Protect

When WP is enabled, Flash array is blocked from any program and erase operations. This signal shall only be transitioned when a target is idle. The host shall be allowed to issue a new command after tWW once WP is enabled.
Figure 6 describes the tWW timing requirement, shown with the start of a Program command. And Figure 7 shows with the start of a Erase command.

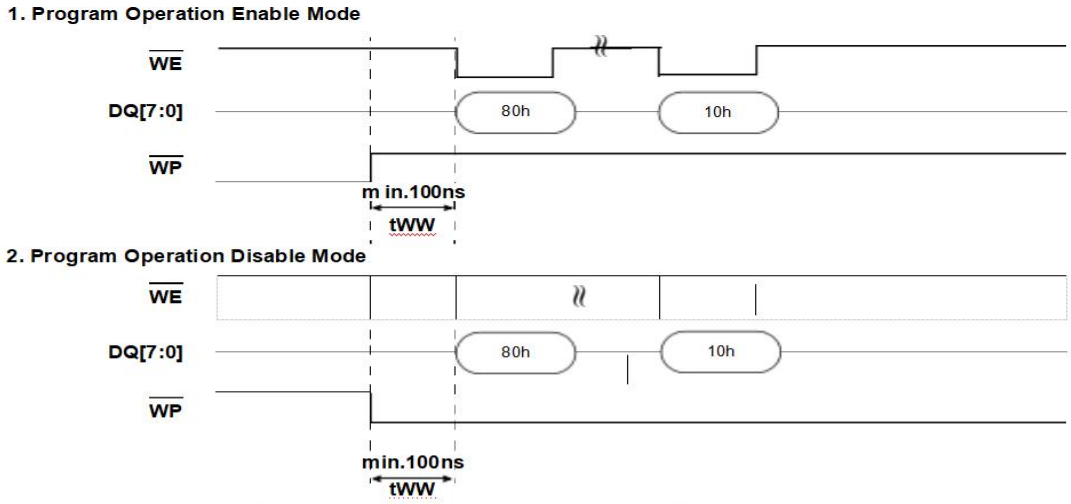


Figure 6. Write Protect Sequence Requirements of the Program Operation

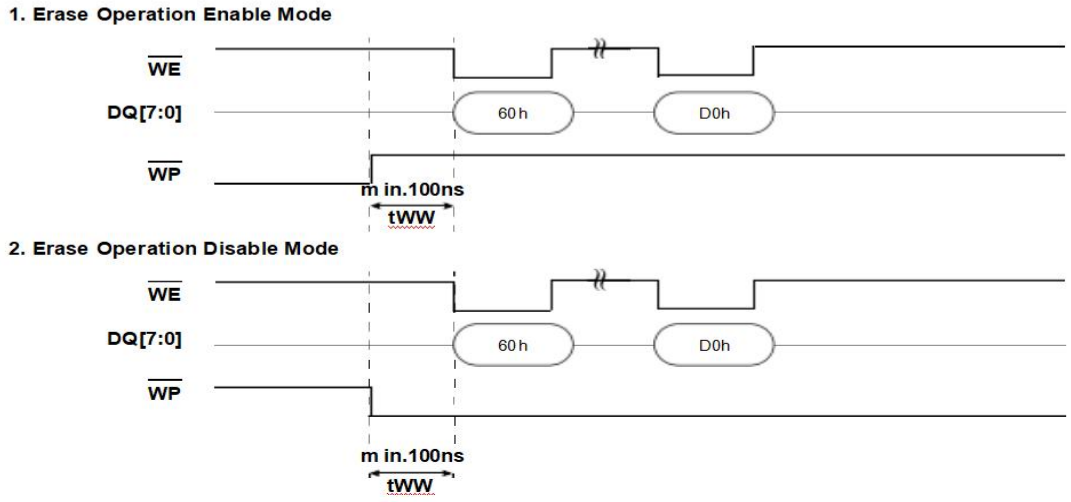


Figure 7. Write Protect Sequence Requirements of the Erase Operation

5 MEMORY ORGANIZATION

A device contains one or more targets. A target is controlled by one CE signal. A target is organized into one or more logical units (LUNs).
A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of plane operations supported for the LUN. The Flash array contains a number of blocks.
A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.
A page is the smallest addressable unit for read and program operations.
Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array. The byte location within the page register is referred to as the column.
There are two mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time. To get further parallelism within a LUN, plane addressing may be used to execute additional dependent operations in parallel.

5.1 Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The least significant bit of the column address shall always be zero for a DDR interface, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs.
When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.
For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.
The row address structure is shown in Figure 8 with the least significant row address bit to the right and the most significant row address bit to the left.

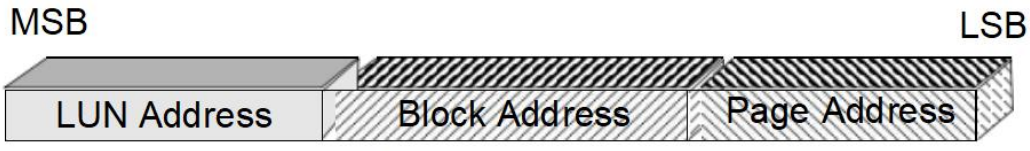


Figure 8. Row Address Layout

The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address.
A host shall not access an address of a page or block beyond maximum page address or block address.

5.2 Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

5.2.1 Device Requirements

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking, as shown in Figure 9, of the 1st page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

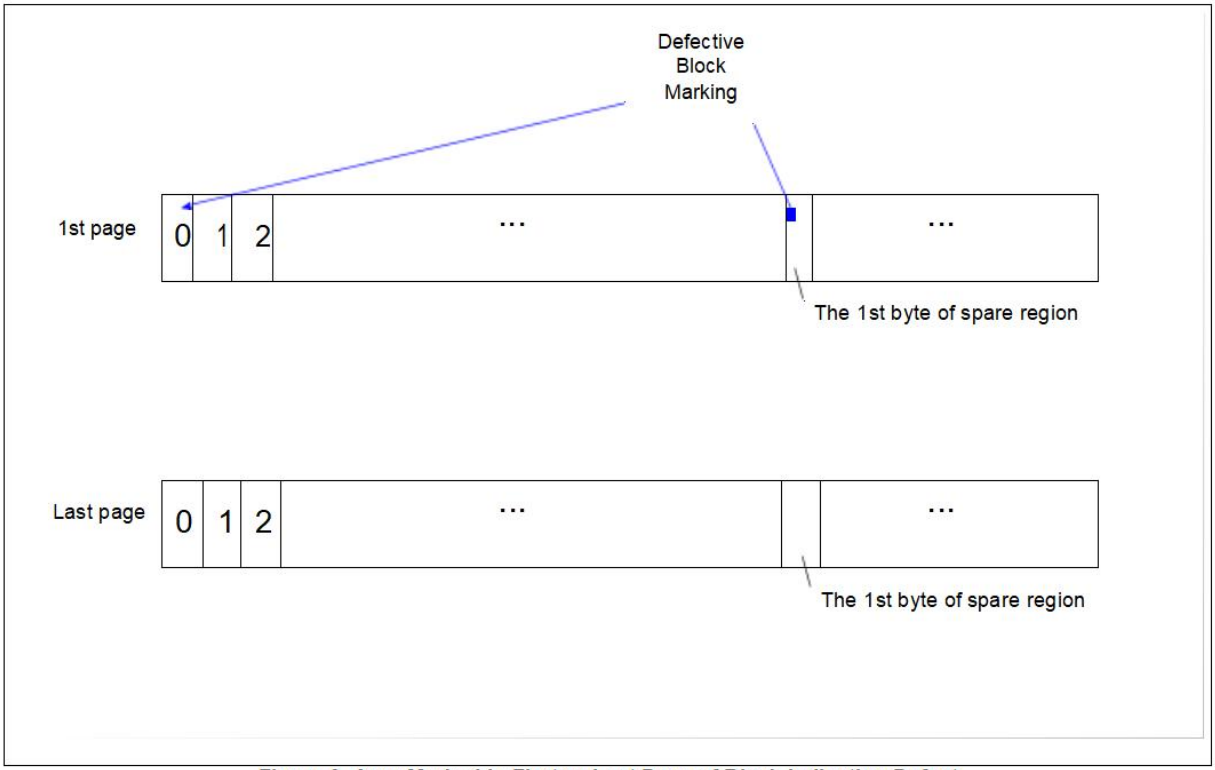


Figure 9. Area Marked in First or Last Page of Block Indicating Defect

5.2.2 Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.
Figure 10 outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The 1st byte of both main and spare region in non-defective blocks are read FFh.
A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of the first page of the block.
The host shall check the Defective Block Marking location of the first page on each block to verify the block is valid prior to any erase or program operations on that block.

NOTE :
Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.

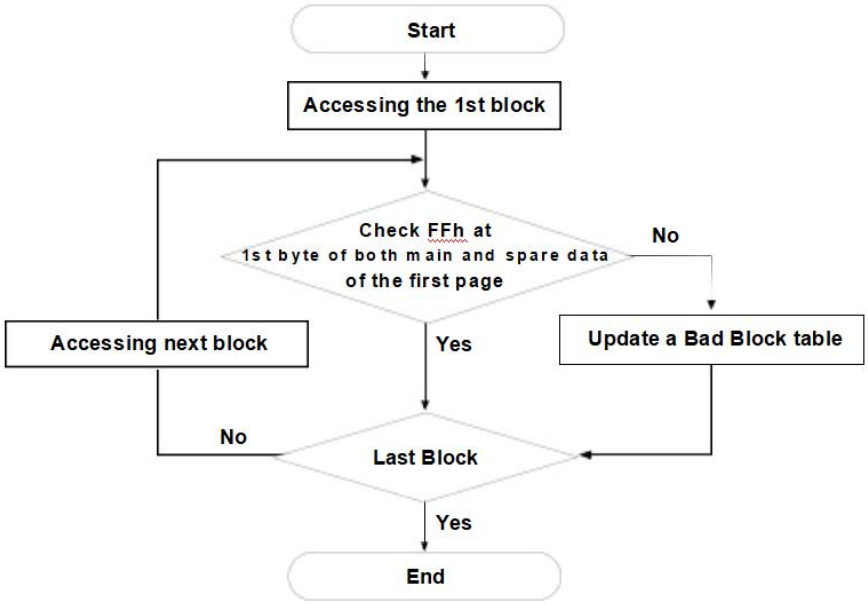


Figure 10. Flow Chart to Create Initial Invalid Block Table

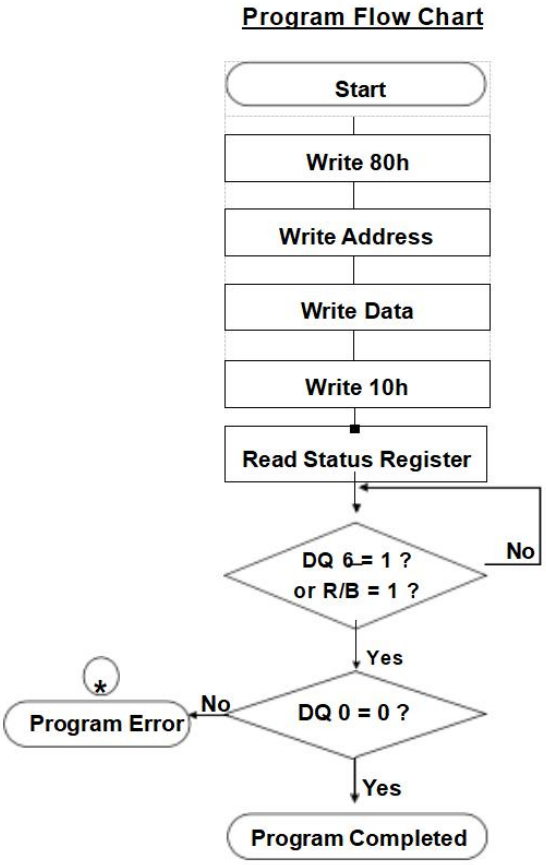
5.3 Error in Write or Read Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

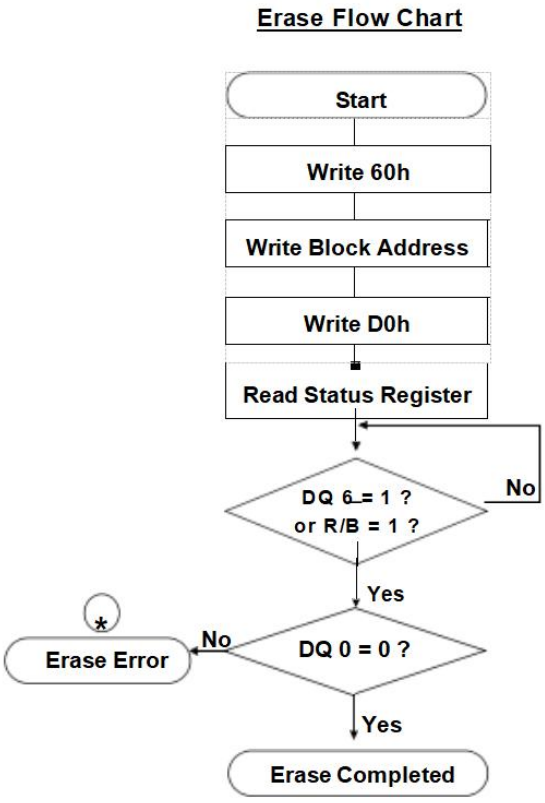
[Table 20] Failure Cases

Failure Mode		Detection and Countermeasure sequence
Write	Program Failure	Read Status after Program → Block Replacement
Erase	Erase Failure	Read Status after Erase → Block Replacement
Read	Failure	Verify ECC → ECC Correction

ECC :Error correcting code such as BCH code. (Example) 48bit correction / 1KByte

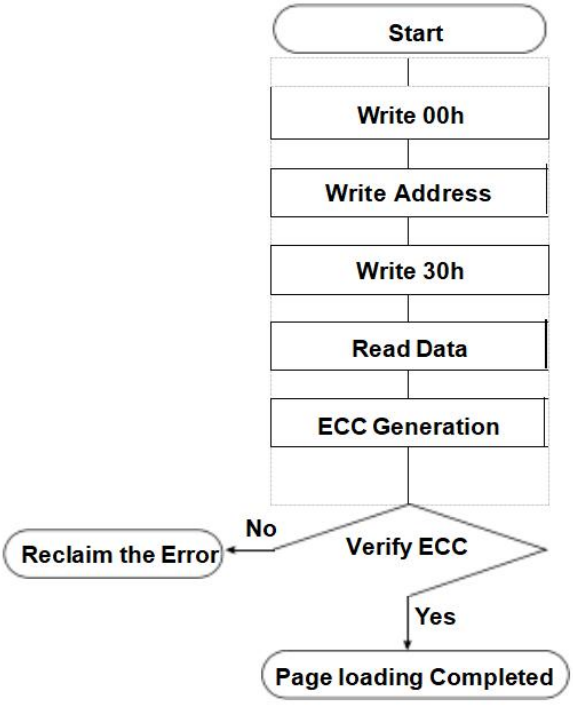


* : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

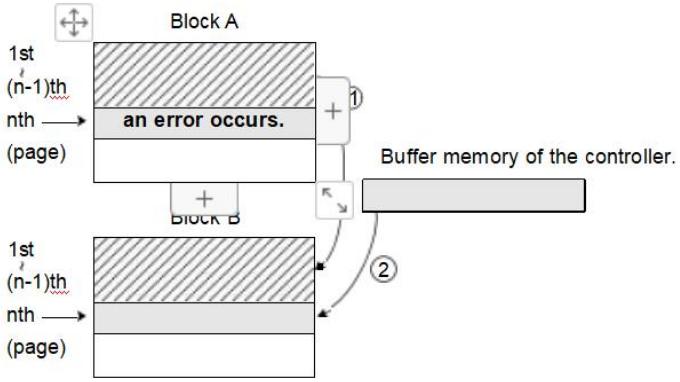


* : If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

5.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. A starting page in an erased block for programming shall be page 0 and blank pages (i.e. unprogrammed pages) between programmed pages are not allowed.

A page in 'group X_LSB' must be programmed before the program operation for a page in 'group X_MSB' is performed

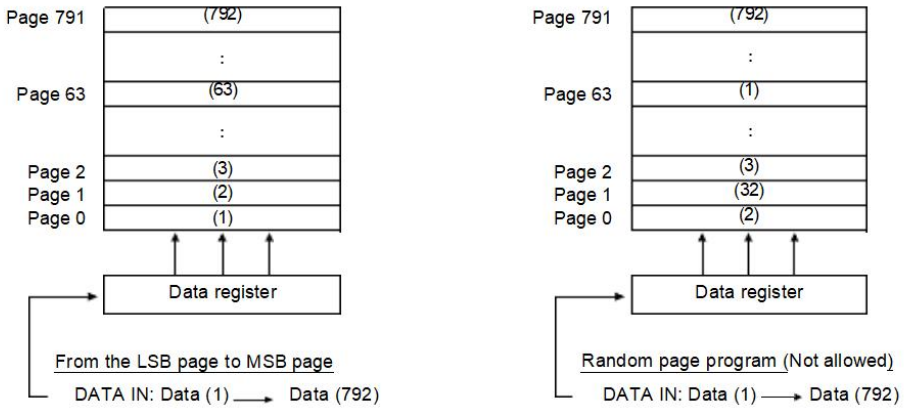


Figure 11. Addressing for Program Operation

[Table 21] Addressing for Program Operation

Device	DQ	DATA	ADDRESS				
	DQx	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
MKPV32G08CT-ABG	DQ0 ~ DQ7	17,920Byte	A0~A7	A8~A14	A15~A22	A23~A30	A31~A33

[Table 22] Paired Page A

Paired Page Address (1/2)				Paired Page Address (2/2)			
Group 1_LSB	Group 1_MSB	Group 2_LSB	Group 2_MSB	Group 1_LSB	Group 1_MSB	Group 2_LSB	Group 2_MSB
000h		001h		0CAh	0D0h	0CBh	0D1h
002h		003h		0CEh	0D4h	0CFh	0D5h
004h	008h	005h	009h	0D2h	0D8h	0D3h	0D9h
006h	00Ch	007h	00Dh	0D6h	0DCh	0D7h	0DDh
00Ah	010h	00Bh	011h	0DAh	0E0h	0DBh	0E1h
00Eh	014h	00Fh	015h	0DEh	0E4h	0DFh	0E5h
012h	018h	013h	019h	0E2h	0E8h	0E3h	0E9h
016h	01Ch	017h	01Dh	0E6h	0ECh	0E7h	0EDh
01Ah	020h	01Bh	021h	0EAh	0F0h	0EBh	0F1h
01Eh	024h	01Fh	025h	0EEh	0F4h	0EFh	0F5h
022h	028h	023h	029h	0F2h	0F8h	0F3h	0F9h
026h	02Ch	027h	02Dh	0F6h	0FCh	0F7h	0FDh
02Ah	030h	02Bh	031h	0FAh	100h	0FBh	101h
02Eh	034h	02Fh	035h	0FEh	104h	0FFh	105h
032h	038h	033h	039h	102h	108h	103h	109h
036h	03Ch	037h	03Dh	106h	10Ch	107h	10Dh
03Ah	040h	03Bh	041h	10Ah	110h	10Bh	111h
03Eh	044h	03Fh	045h	10Eh	114h	10Fh	115h
042h	048h	043h	049h	112h	118h	113h	119h
046h	04Ch	047h	04Dh	116h	11Ch	117h	11Dh
04Ah	050h	04Bh	051h	11Ah	120h	11Bh	121h
04Eh	054h	04Fh	055h	11Eh	124h	11Fh	125h
052h	058h	053h	059h	122h	128h	123h	129h
056h	05Ch	057h	05Dh	126h	12Ch	127h	12Dh
05Ah	060h	05Bh	061h	12Ah	130h	12Bh	131h
05Eh	064h	05Fh	065h	12Eh	134h	12Fh	135h
062h	068h	063h	069h	132h	138h	133h	139h
066h	06Ch	067h	06Dh	136h	13Ch	137h	13Dh
06Ah	070h	06Bh	071h	13Ah	140h	13Bh	141h
06Eh	074h	06Fh	075h	13Eh	144h	13Fh	145h
072h	078h	073h	079h	142h	148h	143h	149h
076h	07Ch	077h	07Dh	146h	14Ch	147h	14Dh
07Ah	080h	07Bh	081h	14Ah	150h	14Bh	151h
07Eh	084h	07Fh	085h	14Eh	154h	14Fh	155h
082h	088h	083h	089h	152h	158h	153h	159h
086h	08Ch	087h	08Dh	156h	15Ch	157h	15Dh
08Ah	090h	08Bh	091h	15Ah	160h	15Bh	161h
08Eh	094h	08Fh	095h	15Eh	164h	15Fh	165h
092h	098h	093h	099h	162h	168h	163h	169h
096h	09Ch	097h	09Dh	166h	16Ch	167h	16Dh
09Ah	0A0h	09Bh	0A1h	16Ah	170h	16Bh	171h
09Eh	0A4h	09Fh	0A5h	16Eh	174h	16Fh	175h
0A2h	0A8h	0A3h	0A9h	172h	178h	173h	179h
0A6h	0ACh	0A7h	0ADh	176h	17Ch	177h	17Dh
0AAh	0B0h	0ABh	0B1h	17Ah	180h	17Bh	181h
0AEh	0B4h	0AFh	0B5h	17Eh	184h	17Fh	185h
0B2h	0B8h	0B3h	0B9h	182h	188h	183h	189h
0B6h	0BCh	0B7h	0BDh	186h	18Ch	187h	18Dh
0BAh	0C0h	0BBh	0C1h	18Ah	190h	18Bh	191h
0BEh	0C4h	0BFh	0C5h	18Eh	194h	18Fh	195h
0C2h	0C8h	0C3h	0C9h	192h	198h	193h	199h

0C6h	0CCh	0C7h	0CDh	196h	19Ch	197h	19Dh

ddress Information

Paired Page Address (3/4)				Paired Page Address (4/4)			
Group 1_LSB	Group 1_MSB	Group 2_LSB	Group 2_MSB	Group 1_LSB	Group 1_MSB	Group 2_LSB	Group 2_MSB
19Ah	1A0h	19Bh	1A1h	25Ah	260h	25Bh	261h
19Eh	1A4h	19Fh	1A5h	25Eh	264h	25Fh	265h
1A2h	1A8h	1A3h	1A9h	262h	268h	263h	269h
1A6h	1ACh	1A7h	1ADh	266h	26Ch	267h	26Dh
1AAh	1B0h	1ABh	1B1h	26Ah	270h	26Bh	271h
1AEh	1B4h	1AFh	1B5h	26Eh	274h	26Fh	275h
1B2h	1B8h	1B3h	1B9h	272h	278h	273h	279h
1B6h	1BCh	1B7h	1BDh	276h	27Ch	277h	27Dh
1BAh	1C0h	1BBh	1C1h	27Ah	280h	27Bh	281h
1BEh	1C4h	1BFh	1C5h	27Eh	284h	27Fh	285h
1C2h	1C8h	1C3h	1C9h	282h	288h	283h	289h
1C6h	1CCh	1C7h	1CDh	286h	28Ch	287h	28Dh
1CAh	1D0h	1CBh	1D1h	28Ah	290h	28Bh	291h
1CEh	1D4h	1CFh	1D5h	28Eh	294h	28Fh	295h
1D2h	1D8h	1D3h	1D9h	292h	298h	293h	299h
1D6h	1DCh	1D7h	1DDh	296h	29Ch	297h	29Dh
1DAh	1E0h	1DBh	1E1h	29Ah	2A0h	29Bh	2A1h
1DEh	1E4h	1DFh	1E5h	29Eh	2A4h	29Fh	2A5h
1E2h	1E8h	1E3h	1E9h	2A2h	2A8h	2A3h	2A9h
1E6h	1ECh	1E7h	1EDh	2A6h	2ACh	2A7h	2ADh
1EAh	1F0h	1EBh	1F1h	2AAh	2B0h	2ABh	2B1h
1EEh	1F4h	1EFh	1F5h	2AEh	2B4h	2AFh	2B5h
1F2h	1F8h	1F3h	1F9h	2B2h	2B8h	2B3h	2B9h
1F6h	1FCh	1F7h	1FDh	2B6h	2BCh	2B7h	2BDh
1FAh	200h	1FBh	201h	2BAh	2C0h	2BBh	2C1h
1FEh	204h	1FFh	205h	2BEh	2C4h	2BFh	2C5h
202h	208h	203h	209h	2C2h	2C8h	2C3h	2C9h
206h	20Ch	207h	20Dh	2C6h	2CCh	2C7h	2CDh
20Ah	210h	20Bh	211h	2CAh	2D0h	2CBh	2D1h
20Eh	214h	20Fh	215h	2CEh	2D4h	2CFh	2D5h
212h	218h	213h	219h	2D2h	2D8h	2D3h	2D9h
216h	21Ch	217h	21Dh	2D6h	2DCh	2D7h	2DDh
21Ah	220h	21Bh	221h	2DAh	2E0h	2DBh	2E1h
21Eh	224h	21Fh	225h	2DEh	2E4h	2DFh	2E5h
222h	228h	223h	229h	2E2h	2E8h	2E3h	2E9h
226h	22Ch	227h	22Dh	2E6h	2ECh	2E7h	2EDh
22Ah	230h	22Bh	231h	2EAh	2F0h	2EBh	2F1h
22Eh	234h	22Fh	235h	2EEh	2F4h	2EFh	2F5h
232h	238h	233h	239h	2F2h	2F8h	2F3h	2F9h
236h	23Ch	237h	23Dh	2F6h	2FCh	2F7h	2FDh
23Ah	240h	23Bh	241h	2FAh	300h	2FBh	301h
23Eh	244h	23Fh	245h	2FEh	304h	2FFh	305h
242h	248h	243h	249h	302h	308h	303h	309h
246h	24Ch	247h	24Dh	306h	30Ch	307h	30Dh
24Ah	250h	24Bh	251h	30Ah	310h	30Bh	311h
24Eh	254h	24Fh	255h	30Eh	314h	30Fh	315h
252h	258h	253h	259h	312h		313h	
256h	25Ch	257h	25Dh	316h		317h	

NOTE :

When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged.

6 FUNCTION DESCRIPTION

6.1 Data Protection and Power Transition Sequence

6.1.1 Data Protection

The device is designed to offer protection from any involuntary program/erase during power transitions. An internal voltage detector disables all internal program/erase circuits when VCC is below about 2V. WP_n pin provides hardware protection and is recommended to be kept at VIL during power transitions. Although two step command sequence for program/erase provides protection from any operations by unintentional command input, keeping CLE and ALE at VIL prevents any spurious commands asserted during power transitions.
It is highly recommended to keep CE at VIH to prevent unnecessary current consumption during power transitions.

6.1.2 Power Up Sequence

For NAND devices that support VCCQ for I/O power supply, VCCQ must not exceed VCC during power up. The host must wait for R/B to be valid High before issuing Reset command (FFh) to initialize any targets that share same CE. The R/B_n signal becomes valid after 100us since both VCC and VCCQ reach 2.7V. The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/B_n becomes valid. Each target (CE_n) will be busy for a maximum of 5ms after the RESET command (FFh) is issued. The RESET busy time can be monitored by polling R/B or issuing the READ STATUS (70h) command. Each NAND LUN (i.e. die) may draw less than 10mA over 1ms prior to the execution of the first RESET command (FFh) after the device is powered on. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50mA. When VCC is enabled then VCCQ starts to be enabled during power up, host shall start to raise VREFQ. And before FFh is issued, VREFQ should be completely set.

6.1.3 Power Down Sequence

During power-down, VCCQ shall not exceed VCC .

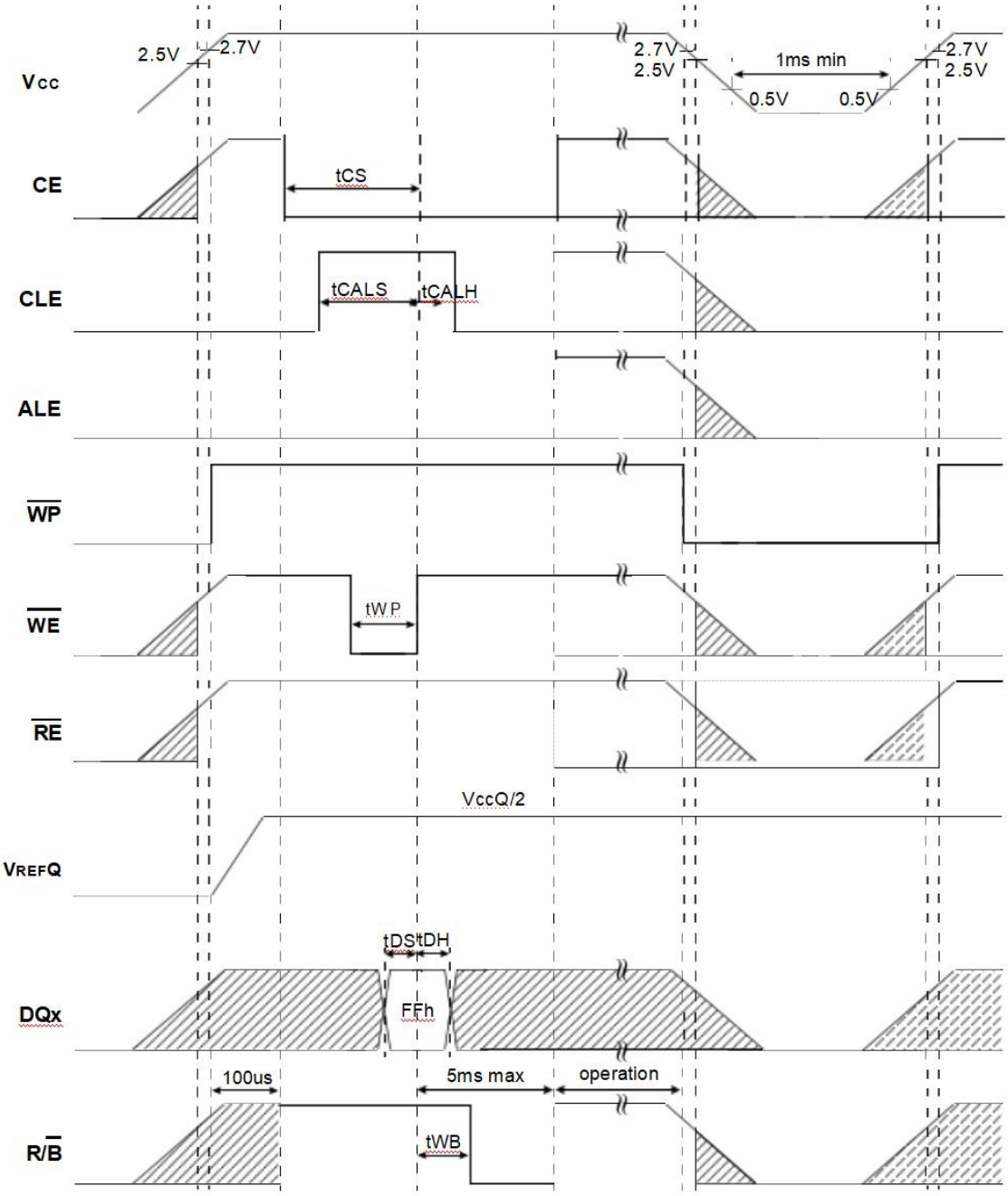


Figure 12. Initialization Timing

NOTE :

1) To minimize peak current during initialization, each LUN in a target can be selectively initialized by FAh (Reset LUN) command.

2) During power-up/down, Vcc should sustain 0.2V greater than VccQ until it reach 2.7V.

3) Once VCC drops under 2.5V, VCC is recommended that it be driven down to 0.5V and stay low under 0.5V for at least 1ms before VCC powered up.

4) Maximum DC voltage on input and I/O pins is VCCQ+0.3V which, during transition, may have overshoot that is defined in Table 7.

6.2 Mode Selection

Table 23 describes the bus state for the Toggle DDR. Commands, addresses and data is all written through DQ's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ pins.
Host reads or writes data to the device using DQS signal. And data is latched on the falling and rising both edge of DQS on data input.

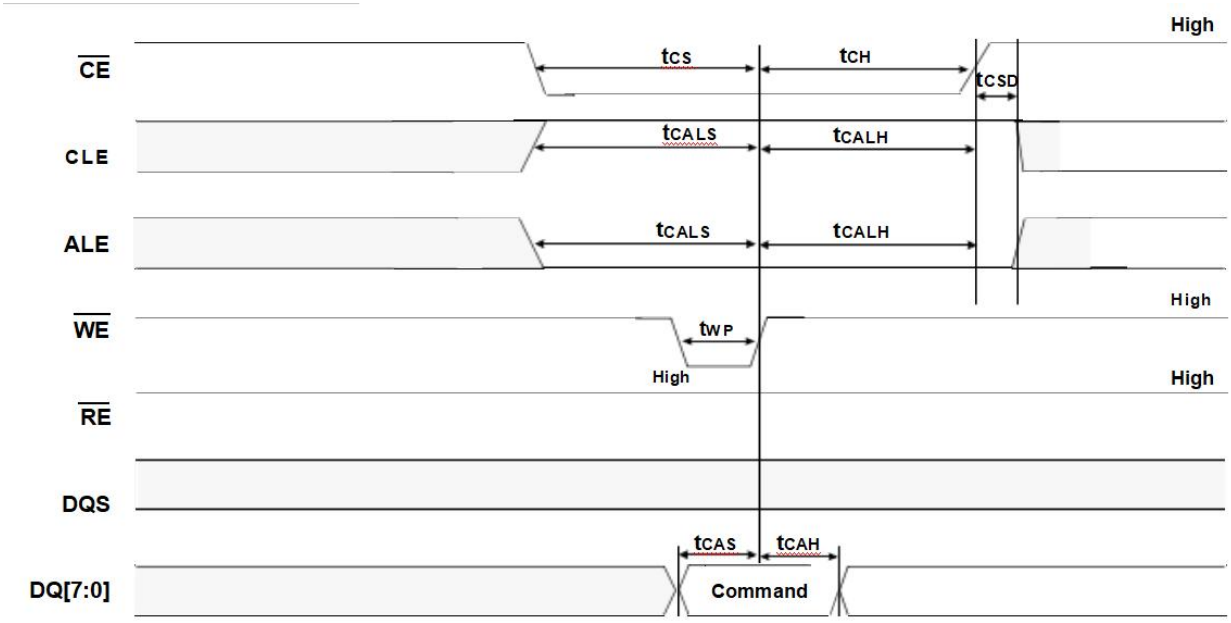
[Table 23] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$	Mode	
H	L	L	↓	H	X[1]	X	Read Mode	Command Input
L	H	L	↓	H	X	X		Address Input (5 cycles)
H	L	L	↓	H	X	H	Write Mode	Command Input
L	H	L	↓	H	X	H		Address Input (5 cycles)
L	L	L	H	H	↓↑	H	Data Input	
L	L	L	H	■ ■	↓ ■	X	Data Output	
X	X	X	X	H	X	X	During Read (Busy)	
X	X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	X	L	Write Protect	
X	X	H	X	X	X	0V/V$_{CC}$[2]	Stand-by	

NOTE :
1) X can be VIL or VIH .
2) WP should be biased to CMOS high or CMOS low for standby.
3) Data input by DQS transition in the middle of command input (e.g. 80h/81h/85h) and address input (e.g. 5 cycle of column address and row address) sequence is prohibited.

6.3 General Timing

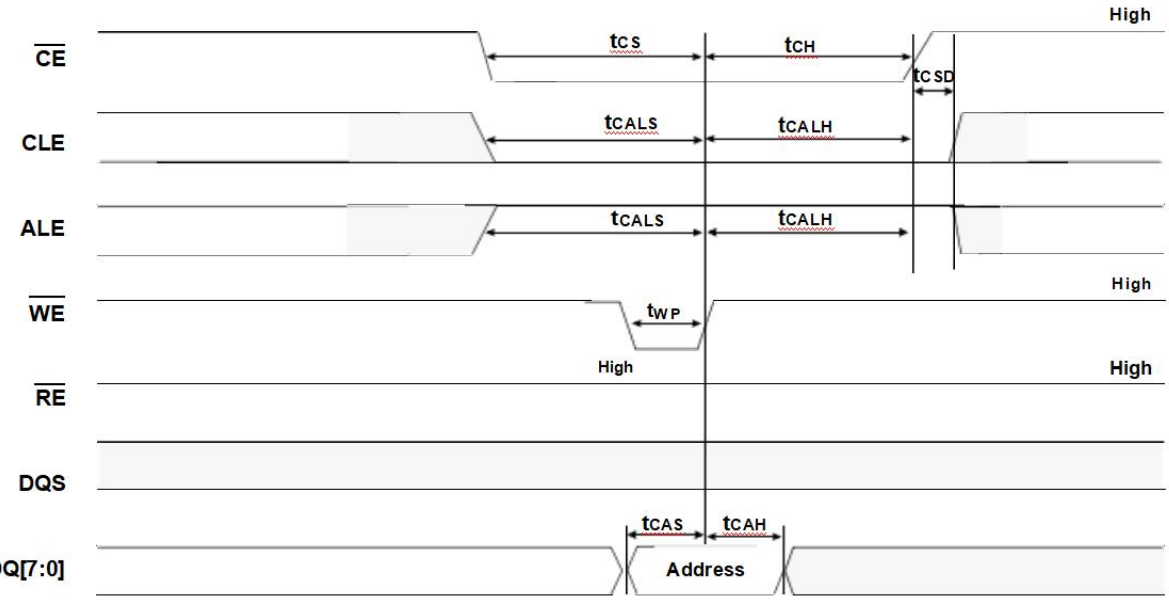
6.3.1 Command Latch Cycle



NOTE :

1) Command information is latched by WE going 'High' when CE is 'Low', CLE is 'High', and ALE is 'Low'.

6.3.2 Address Latch Cycle

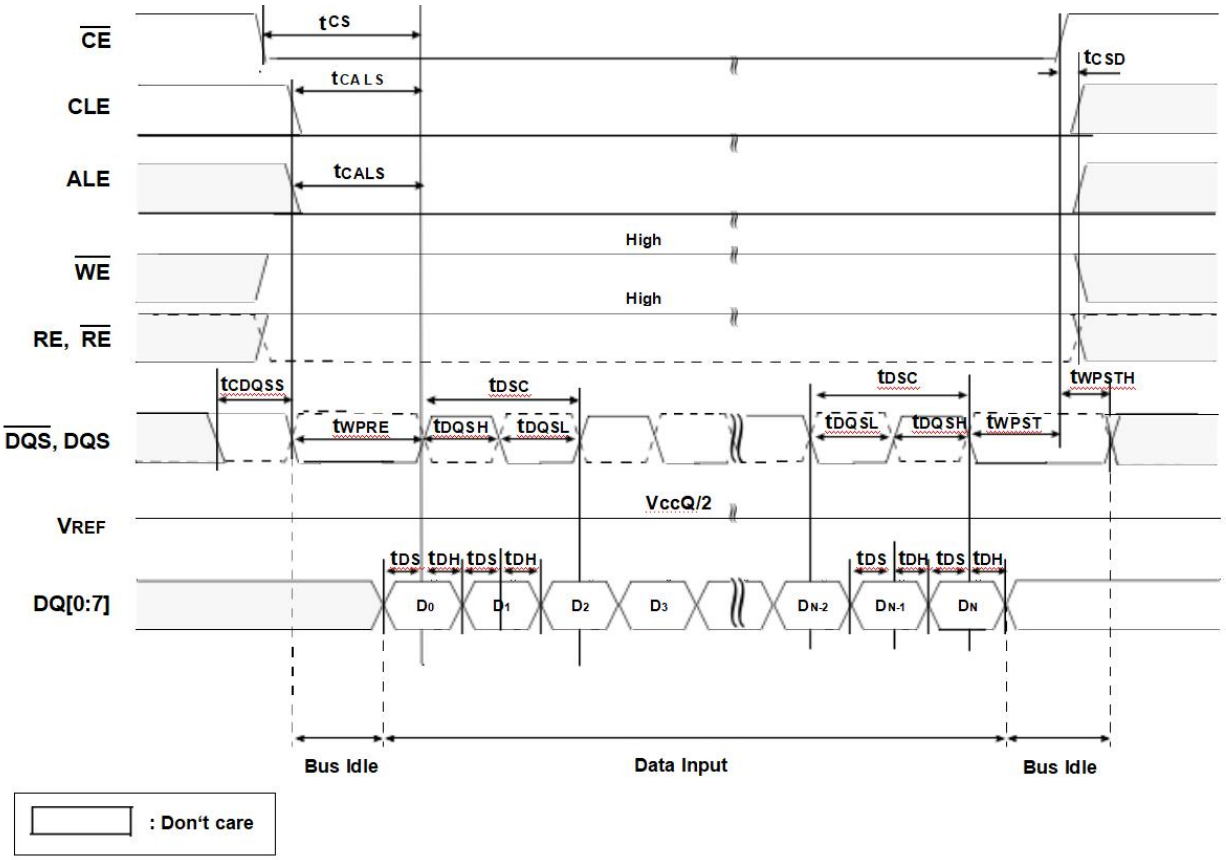


: Don't care

NOTE :

1) Address information is latched by WE going 'High' when CE is 'Low', CLE is 'Low', and ALE is 'High'.

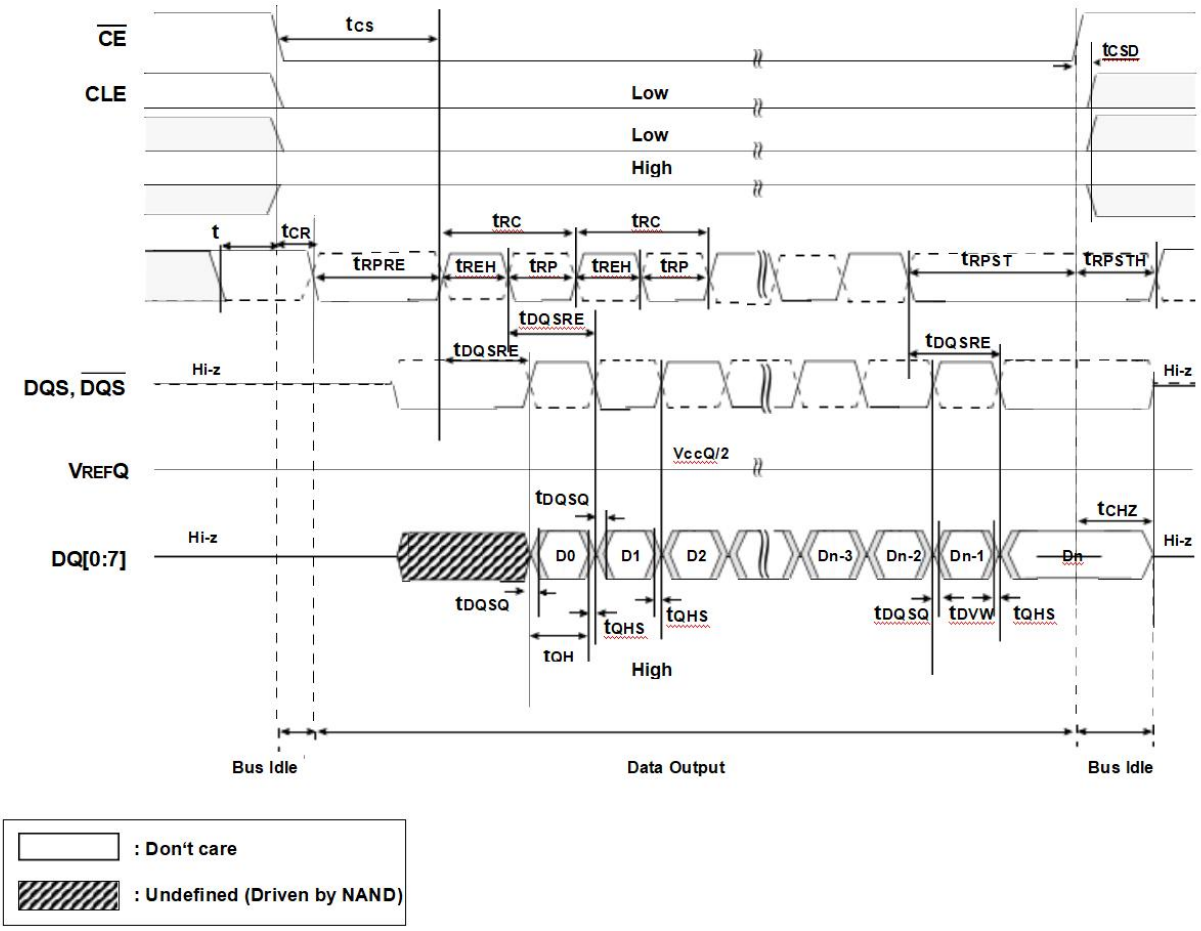
6.3.3 Basic Data Input Timing



NOTE :

1) DQS, DQS and Data input buffers are turned-on when CE and DQS goes 'Low' and Data inputs begin with DQS, DQS
2) ALE and CLE should not toggle during tWPRE period during tCALS.
3) DQS and Data input buffers are turned-off if either CLE or CE goes 'High'.
4) tCDQSS is defined from the last data input condition of the control signals such as CE
5) DQS can be high or low during tCDQSS.

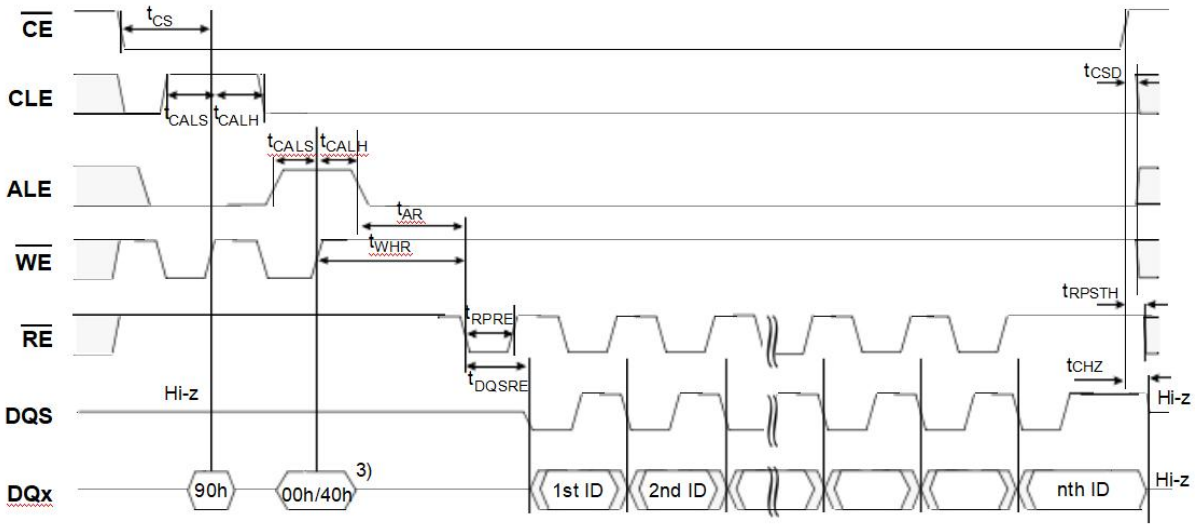
6.3.4 Basic Data Output Timing



NOTE :

1) DQS, DQS and DQ drivers are turned-on when CE goes Low for data out operation.
2) ALE and CLE should not toggle during tRPRE period regardless of tCALS.
3) DQS and DQ drivers turn from valid value to high-z if either CLE or CE goes high.
4) The least significant bit of the column address shall always be zero.
5) RE shall be high during tCRES

6.3.5 Read ID Operation



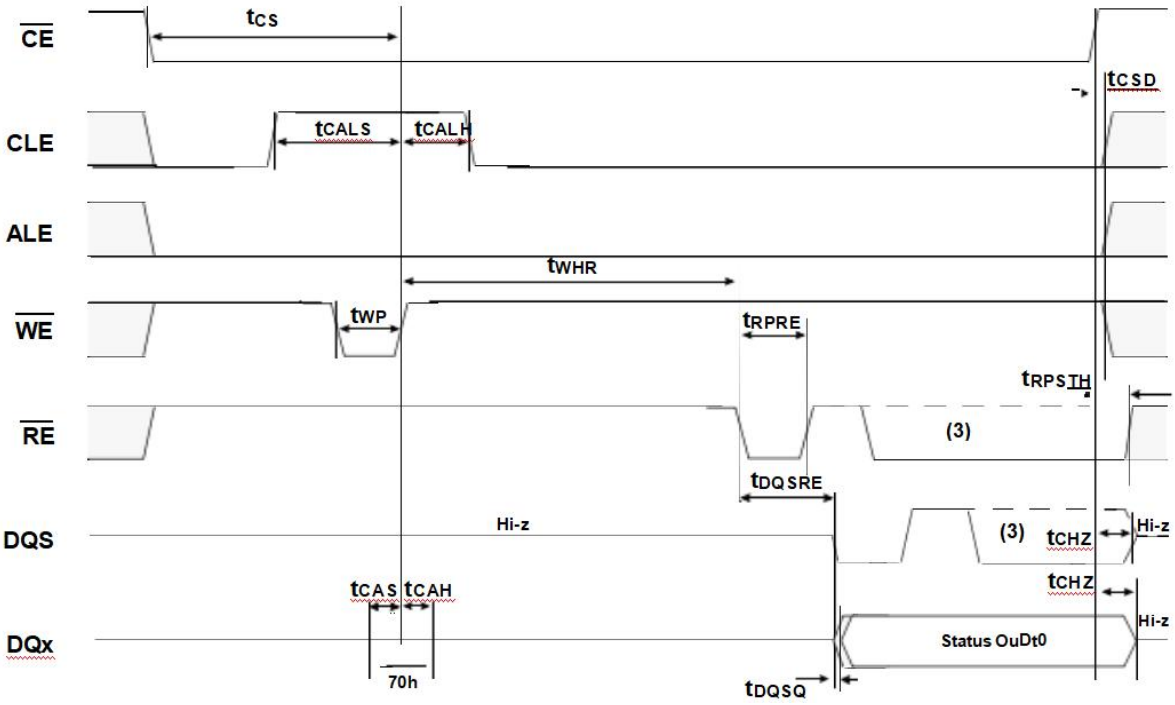
NOTE :

1) Even though toggle-mode NAND uses both low- and high-going edges of DQS for reads, ID read operation repeats each data byte twice, so that ID read timing becomes identical to that of conventional NAND.

2) DQS and DQ drivers turn from valid value to high-z when CE or CLE goes High.

3) Address 00h is for Samsung conventional and 40h is for new JEDEC ID information.

6.3.6 Read Status Cycle



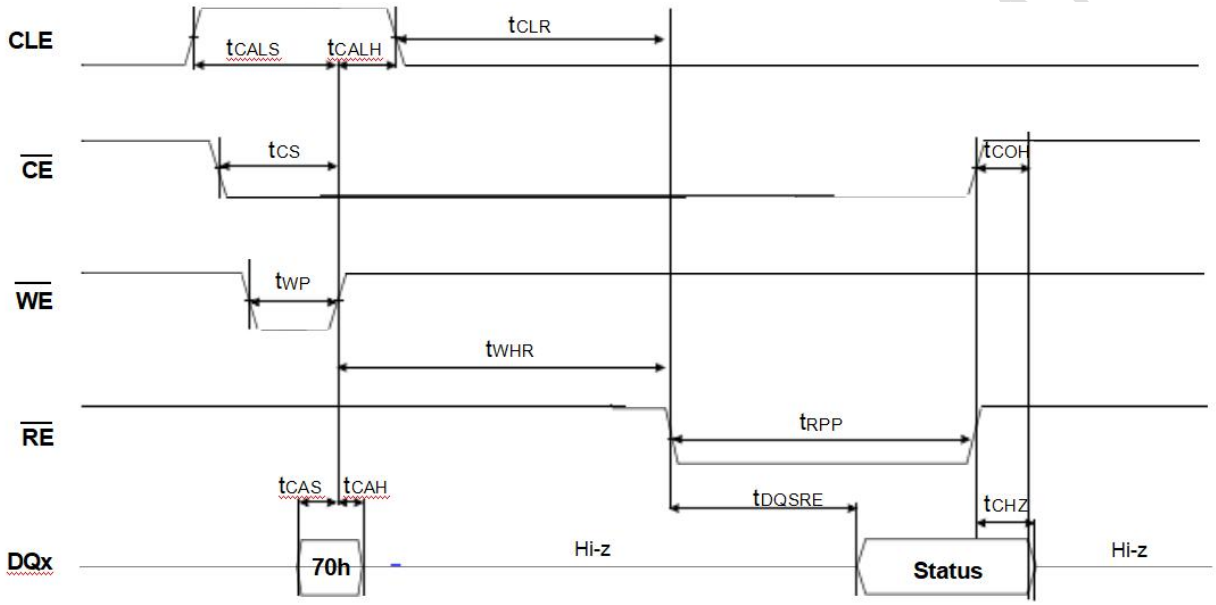
NOTE :

1) Even though toggle-mode NAND uses both low and high-going edges of DQS for reads, Read Status operation repeats same output until device status changes.

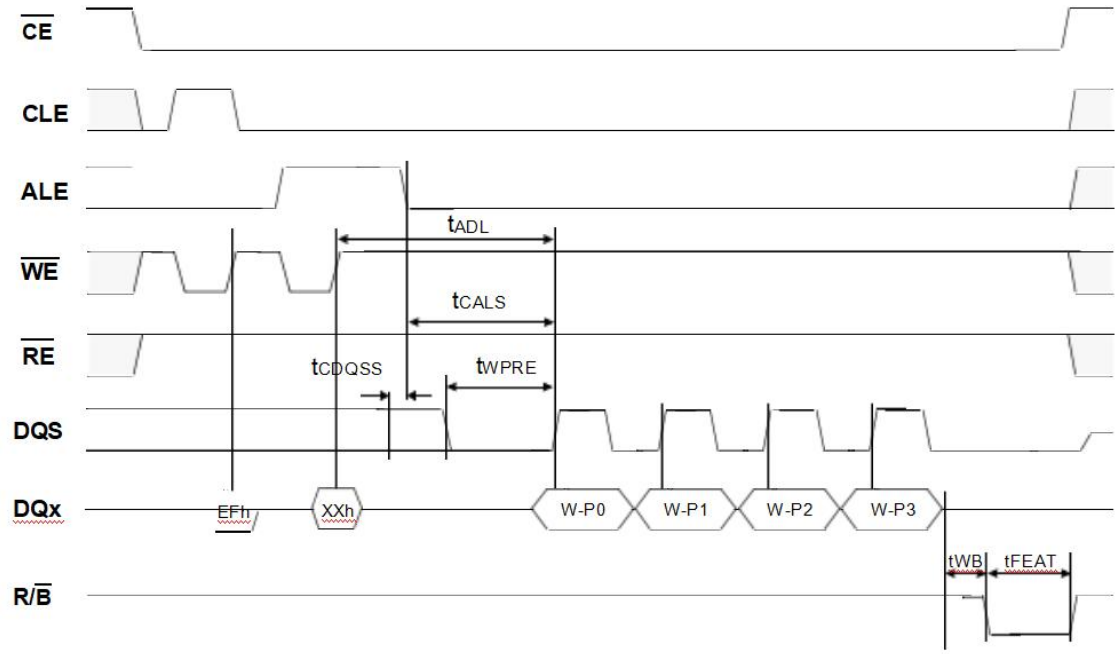
2) DQS and Data out buffers turn from valid value to high-z when CE or CLE goes High

3) RE can toggle more than once.

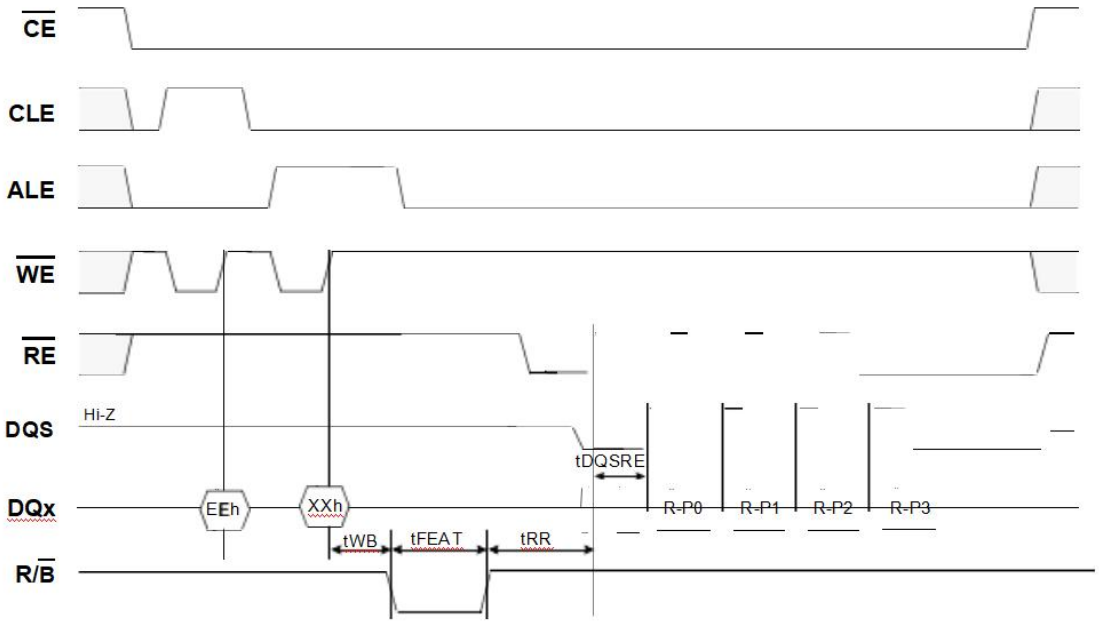
6.3.7 Read Status Cycle before Toggle DDR Setting at Initialization Sequence by FFh Command



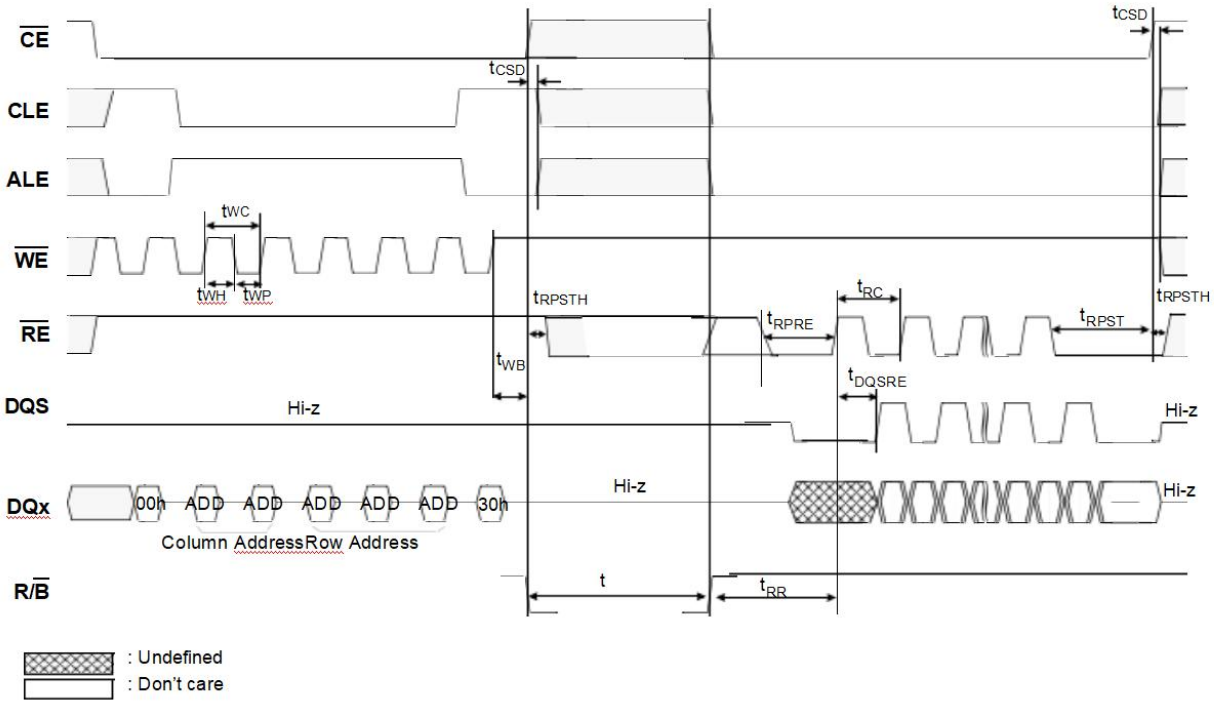
6.3.8 Set Feature



6.3.9 Get Feature

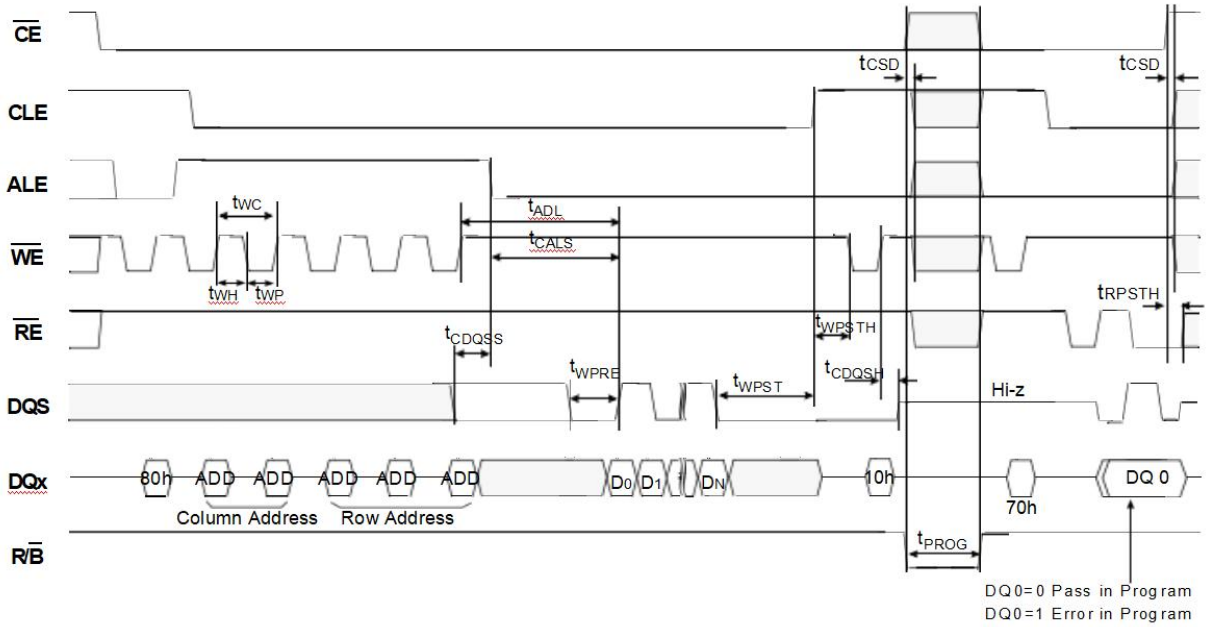


6.3.10 Page Read Operation



NOTE :
CE is once deasserted, it shall stay high over at least 35ns before it is asserted again.

6.3.11 Page Program Operation



NOTE :

CE is once deasserted, it shall stay high over at least 125ns before it is asserted again.

No data input is not allowed before the page program confirm command (10h).

6.4 AC Test Condition

[Table 24] AC Test Condition

Parameter	K9GBGD8U0E
Input Pulse Levels	V_{IL} to V_{IH}
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	$V_{CCQ}/2$
Output Load	CL= 5pF

NOTE :

MKPV32G08CT-ABG-XCB0:TA=0 to 70°C, XIB0 : TA=-40 to 85°C, VCC=2.7V~3.6V, unless otherwise noted.

6.5 AC Timing Characteristics

6.5.1 Timing Parameters Description

[Table 25] Toggle DDR Timing Parameters Description

Description
Data Transfer from Flash array to Register
Program Time
Erase Time
Address to Data Loading Time
ALE Low to RE Low
CLE/ALE Hold Time
CLE/ALE Setup Time
Command/Address Hold Time
Command/Address Setup Time
CE Hold Time
DQS Hold Time for data input finish
DQS Setup Time for data input start
CE High to Output Hi-Z
CLE High to Output Hi-Z
CLE to RE Low
Data Hold Time after CE disable
CE Low to RE Low
RE Set up Time
CE Setup Time
CE Disable to signal (CLE, ALE, WE) don't care
Command Write Cycle to Address Write Cycle Time for Random Data Input and Register Read Out mode
Data Hold Time
DQS Input High Pulse Width
DQS Input Low Pulse Width
Output skew among data output and corresponding DQS
RE to DQS and DQ delay
Data Strobe Cycle Time
Data Setup Time
Output data valid window
Busy time for Set Feature and Get Feature
Output hold time from DQS
DQS hold skew factor
Read Cycle Time
RE High pulse width
RE Low pulse width
RE Low width for Read Status at power-up
Read Preamble

tRPST	Read Postamble
tRPSTH	Read Postamble Hold Time
tRR	Ready to RE High
tRST	Device Resetting Time(Read/Program/Erase)
tWB	WE High to Busy
tWC	Write Cycle Time
tWH	WE High pulse width
tWHR	WE High to RE Low
tWHR2	WE High to RE Low for Random data out
tWP	WE Low pulse Width
tWPRE	Write Preamble
tWPST	Write Postamble
tWPSTH	Write Postamble Hold Time
tWW	WP High/Low to WE low
tCBSY	Dummy Busy Time for Cache Setting
tDCBSYR	Cache Busy in Cache Read

6.5.2 Timing Parameters Table

[Table 26] AC Timing Characteristics

Parameter	Symbol	100Mhz		Unit
		Min.	Max.	
Address to Data Loading Time	tADL	300	-	ns
ALE Low to RE Low	tAR	10	-	ns
CLE/ALE Hold Time	tCALH	5	-	ns
CLE/ALE Setup Time	tCALS	15	-	ns
Command/Address Hold Time	tCAH	5	-	ns
Command/Address Setup Time	tCAS	5	-	ns
DQS Hold Time for data input finish	tCDQSH	100	-	ns
DQS Setup Time for data input start	tCDQSS	100	-	ns
CE Hold Time	tCH	5	-	ns
CE High to Output Hi-Z	tCHZ	-	30	ns
CLE High to Output Hi-Z	tCLHZ	-	30	ns
CLE to RE Low	tCLR	10	-	ns
Data Hold Time after CE disable	tCOH	5	-	ns
CE Low to RE Low	tCR	10	-	ns
RE Set up time	tCRES	10	-	ns
CE Setup Time	tCS	25	-	ns
CE Disable to signal don't care	tCSD	10	-	ns
Command Write cycle to Address Write cycle Time for Random data input and Register Read Out mode	tCWAW	300	-	ns
Data Hold Time	tDH	0.9	-	ns
DQS Input High Pulse Width	tDQSH	0.45 *tRC	-	ns
DQS Input Low Pulse Width	tDQSL	0.45 *tRC	-	ns

Output skew among data output and corresponding DQS	tDQSQ	-	0.8	ns
RE to DQS and DQ delay	tDQSRE	5	25	ns
Data Strobe Cycle Time	tDSC	10	-	ns
Data Setup Time	tDS	0.9	-	ns
Output data valid window	tDVW	tDVW = tQH - tDQSQ		ns
Busy time for Set Feature and Get Feature	tFEAT	-	1	μs
Output hold time from DQS	tQH	tQH = min[tREH, tRP] - tQHS		ns
DQS hold skew factor	tQHS	-	0.8	ns
Read Cycle Time	tRC	10	-	ns
RE High pulse width	tREH	0.45 *tRC	-	ns
RE Low pulse width	tRP	0.45 *tRC	-	ns
RE Low width for Read Status at power-up	tRPP	30	-	ns
Read Preamble	tRPRE	15	-	ns
Read Postamble	tRPST	tDQSRE+ 0.5xtRC	-	ns
Read Postamble Hold Time	tRPSTH	25	-	ns
Ready to RE High	tRR	20	-	ns
Device Resetting Time (Read/Program/Erase)	tRST1)	10/30/200		μs
WE High to Busy	tWB	-	100	ns
Write Cycle Time	tWC	25	-	ns
WE High pulse width	tWH	11	-	ns
WE High to RE Low	tWHR	120	-	ns
WE High to RE Low for Random data out	tWHR2	300	-	ns
WE Low pulse Width	tWP	11	-	ns
Write Preamble	tWPRE	15	-	ns
Write Postamble	tWPST	6.5	-	ns
Write Postamble Hold Time	tWPSTH	25	-	ns
WP High/Low to WE low	tWW	100	-	ns

6.5.3 Read/Program/Erase Characteristics

[Table 27] NAND Read/Program/Erase Characteristics

Parameter	Symbol		Min	Typ	Max	Unit
Data Transfer from Flash Array to Register	R	4KB	-	40	-	μs
		16KB	-	60	90	
Program Time	PROG		-	1.0	5	ms
Dummy Busy Time for Cache Program	CBSY		-	-	PROG	ms
Cache Busy in Cache Read	DCBSYR		-	-	R	μs
Number of Partial Program Cycles in the Same Page	Nop		-	-	1	cycle
Block Erase Time	BERS		-	5	10	ms

NOTE :

1) Typical program time is measured at VCC=3.3V, TA=25°C. Not 100% tested.

2) Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V VCC and 25°C temperature.

3) Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B.

4) tCBSY depends on the timing between internal programming time and data in time.

7 COMMAND DESCRIPTION AND DEVICE OPERATION

7.1 Basic Command Sets

Toggle DDR NAND Flash Memory has addresses multiplexed into 8 I/Os. Command, address and data is all written through DQ[7:0] by bringing WE to low while CE is low. Those are latched on the rising edge of WE . Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ[7:0] pins. Commands which apply to a specific page or block typically have a second command and ones that apply to a target or a LUN have a first command only.

Table 28 below defines the basic command sets.

[Table 28] Basic Command Sets

Page Read	00h	5	30h		Y
Fast 4KB Read	00h	5	20h		Y
Sequential Cache Read	31h	-	-		Y
Read Start for Last Page Cache Read	3Fh	-	-		Y
Random Cache Read	00h	5	31h		Y
Page Program	80h	5	10h		Y
Cache Program	80h	5	15h		Y
Block Erase	60h	3	D0h		Y
Read for Copy-Back	00h	5	35h		Y
Copy-Back Program	85h	5	10h		Y
Random Data Input1)	85h	2	-		Y
Random Data Output1)	05h	2	E0h		Y
Set Feature	EFh	1	-		
Get Feature	EEh	1	-		
Set Feature-LUN Control within 1 CE	D5h	2	-		
Get Feature-LUN Control within 1 CE	D4h	2	-		
Read ID	90h	1	-		Y
Read Status	70h	-	-	Y	
Reset	FFh	-	-	Y	Y2)
Reset LUN	FAh	3	-	Y	Y

NOTE :
1) Random Data Input/Output can be executed in a page.
2) All LUNs tied to a CE are reset.
Caution :
Any undefined command inputs are prohibited except for above command set.

7.2 Basic Operation

7.2.1 Page Read Operation

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure 13 defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

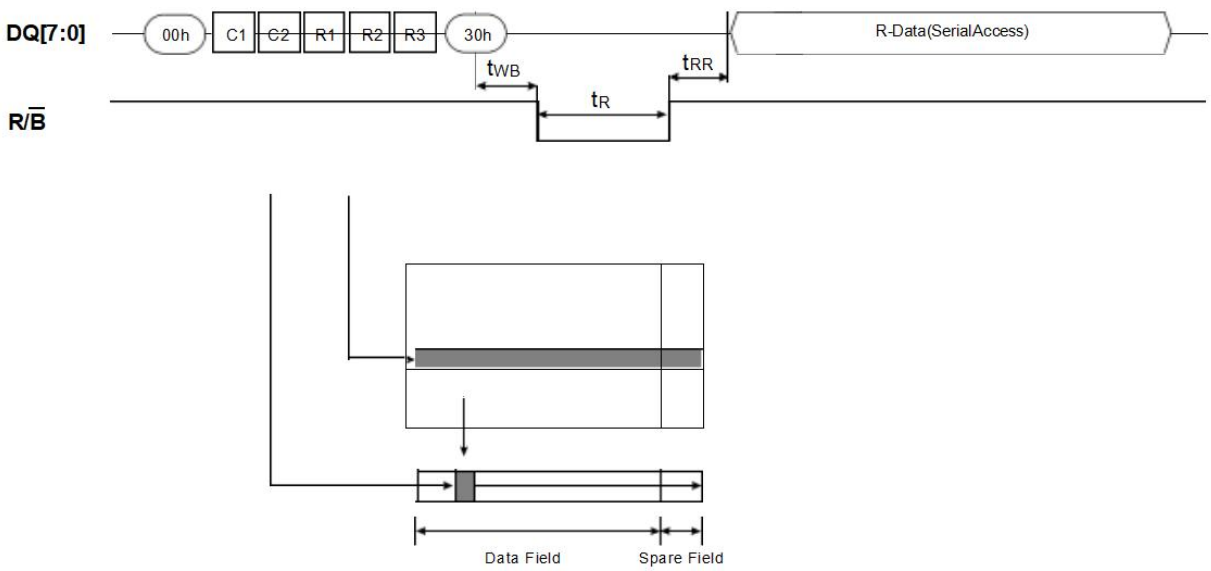


Figure 13. Page Read Sequence

7.2.1.1 Page Read Operation with Random Data Output

The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when the LUN is in a read idle condition. Figure 14 defines the Random Data Output behavior and timings. The host shall not read data from the LUN until tWHR (ns) after the second command (i.e. E0h) is written to the LUN.

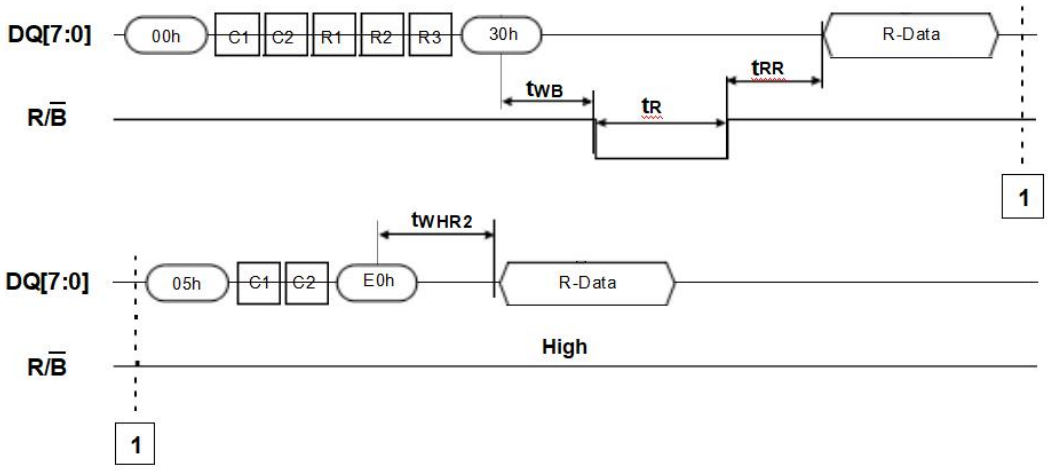


Figure 14. Page Read with Random Data Output Sequence

7.2.1.2 Data Out after Read Status

While monitoring the read status to determine when the tR (transfer from Flash array to a page register) is complete, the host shall re-issue the 00h command to start reading data. Issuing the 00h command will cause data to be returned starting at the selected column address.

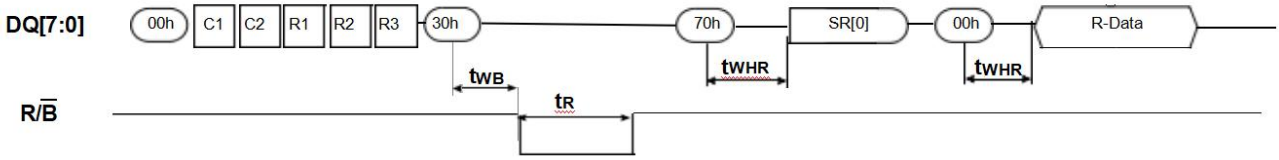


Figure 15. Data Out After Read Status Sequence

7.2.2 Sequential Cache Read Operation

The Sequential Cache Read offers loading page ahead operation, that is a page to be loaded from the Flash array while already loaded page is read by a host. A Read Page command shall be issued prior to the initial Sequential Cache Read command in a cache read sequence. A Sequential Cache Read command (i.e. 31h) shall be issued until the Sequential Cache Read Operation is completed by the Read Start for Last Page Cache Read command (i.e. 3Fh)
The Sequential Cache Read command may be issued after the Read function is complete (i.e. SR[6] is set to one). Data output always begins at column address 00h. When the Sequential Cache Read command (i.e. 31h) is issued, SR[6] is cleared to zero (i.e. busy). After the operation finishes, SR[6] turns to one (i.e. ready) and the host may begin to read the data loaded by the previous Sequential Cache Read operation. The data loaded by a Sequential Cache Read command from Flash array to a page register is copied to a cache register by a following Sequential Cache Read command. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Sequential Cache Read operation except RESET and READ STATUS commands are prohibited. And the data of a final page loaded onto a page register is transferred to a cache register by 3Fh command. The host shall not issue a Sequential Cache Read command (31h) after the last page of a block is read.

Figure 16 defines the Sequential Cache Read behavior and timings.

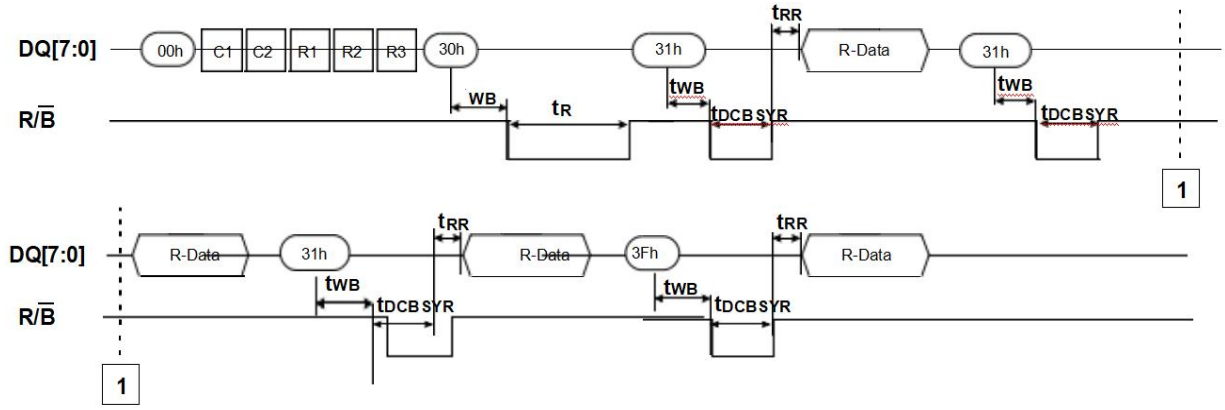


Figure 16. Sequential Cache Read Sequence

7.2.3 Fast 4KB Read

The Fast 4KB Read function transfers only half page (i.e. 4KB+384B) data in NAND array to page register. This function helps applications maximize random read or write throughput. Fast 4KB Read operation supports only a single plane based Read operation and it shall not support Cache Read operation. Since Fast 4KB Read function transfers only half page, to transfer other side half page data, another Fast 4KB Read operation is required.

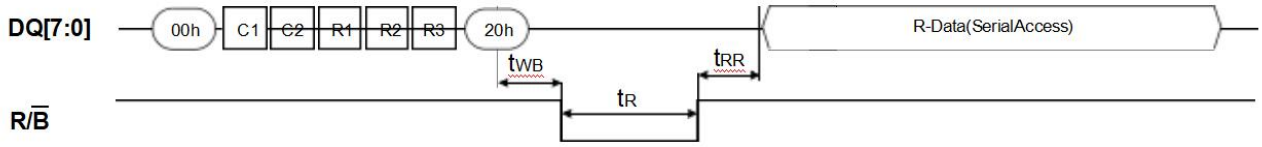


Figure 17. Fast 4KB Read Sequence

Target 4KB data shall be determined by latched address between 00h and 20h command. When the address between 0000h and 117Fh is set, the first half page data shall be transferred and when the address between 1180h and 22FFh is set, the second half page data shall be transferred. Figure 18 represents the page layout when Fast 4KB Read is used.

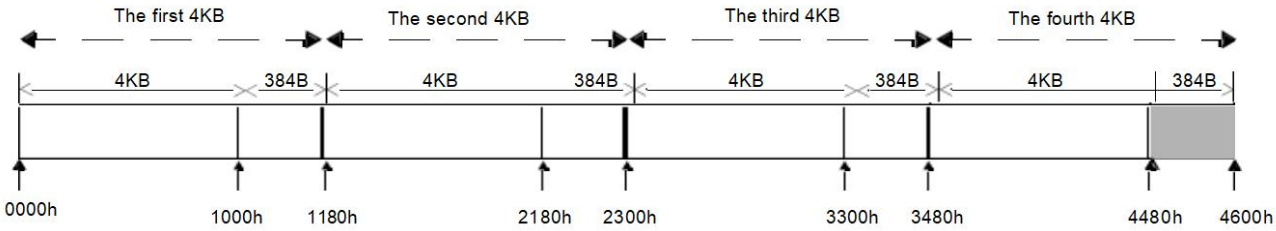


Figure 18. Page Layout for Fast 4KB Read

7.2.4 Random Cache Read Operation

A Read Page command shall be issued prior to the initial Random Cache Read command in a cache read sequence like the Sequential Cache Read operation. Column address shall be fixed to 00h during Random Cache Read operation. 3Fh command is required to finish the sequence and read the final cached page. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Random Cache Read operation except RESET and READ STATUS commands are prohibited. The page and block address can be accessed in a random manner while the plane address shall stay the same. Figure 19 defines the Random Cache Read behavior and timings.

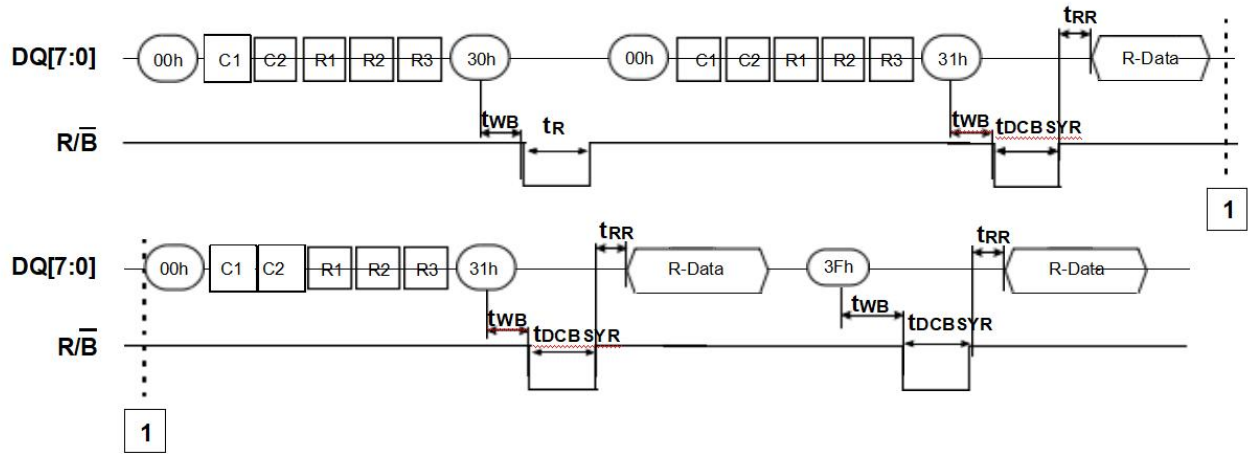


Figure 19. Random Cache Read Sequence

7.2.5 Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure 20 defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

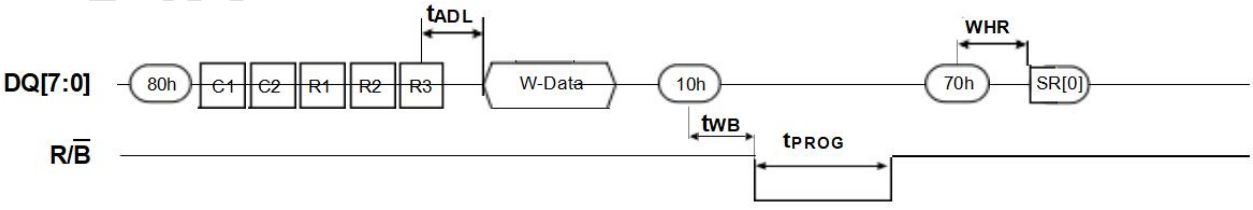


Figure 20. Page Program Sequence

7.2.5.1 Program Operation with Random Data Input

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random data input command (i.e. 85h). Random data input may be operated multiple times without limitation.

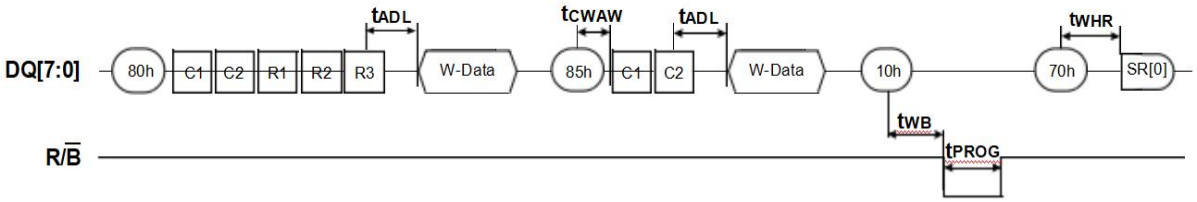


Figure 21. Program Operation with Random Data Input Sequence

7.2.6 Cache Program Operation

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/B returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Cache Program operation except RESET and READ STATUS commands are prohibited.

When command 10h is issued for the final page, R/B turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program Command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure 22 defines the Cache Program behavior and timings. Note that tPROG at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

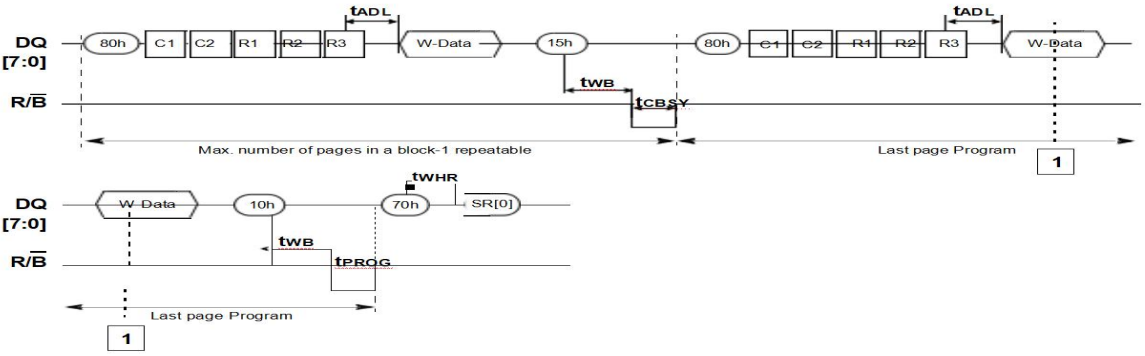


Figure 22. Cache Program Sequence

7.2.7 Block Erase Operation

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while plane and block address are valid.
After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one(i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure 23 defines the Block Erase behavior and timings.

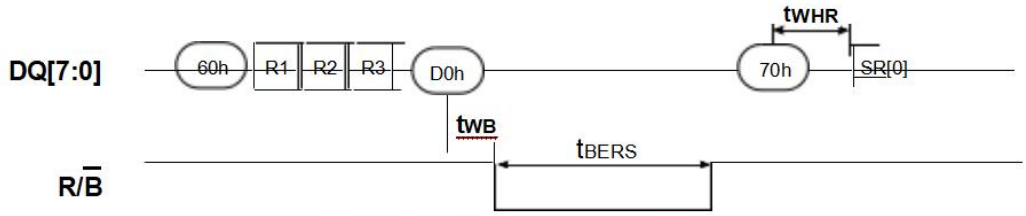


Figure 23. Block Erase Sequence

7.2.8 Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page without data re-loading when no error within the page is found. Since the time consuming reloading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block.
The Copy-Back operation consists of 'Read for Copy-Back' and 'Copy-Back Program'. A host reads a page of data from a source page using 'Read for
Copy-Back' and copies read data back to a destination page on the same LUN by 'Copy-Back Program' command. Copy-Back Program Operation shall work only within the same plane. Figure 24 defines the Copy-Back Program behavior and timings.

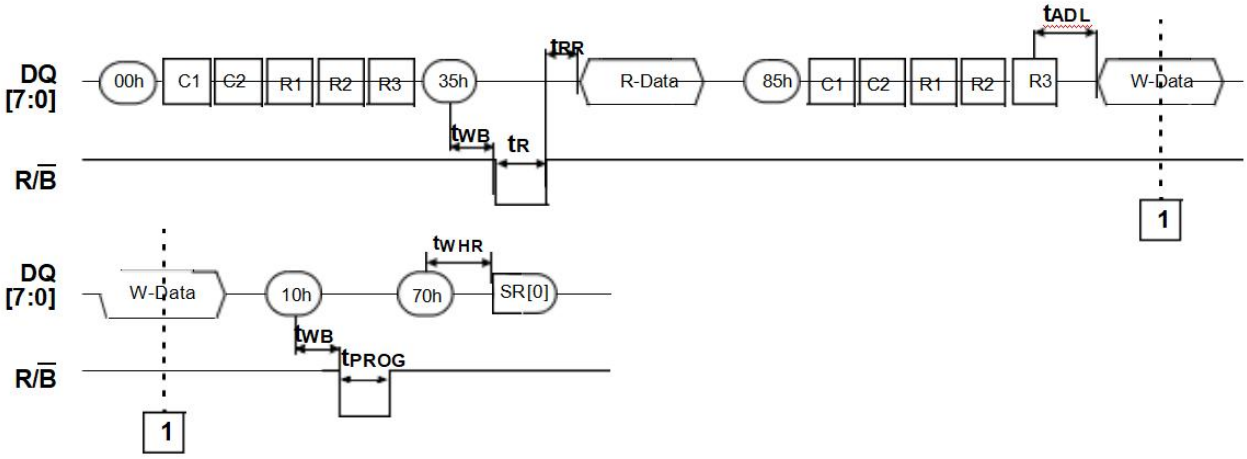


Figure 24. Copy-Back Program Sequence

7.2.8.1 Copy-Back Program Operation with Random Data Input

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure 25 defines the Copy-Back Program with Random Data Input behavior and timings.

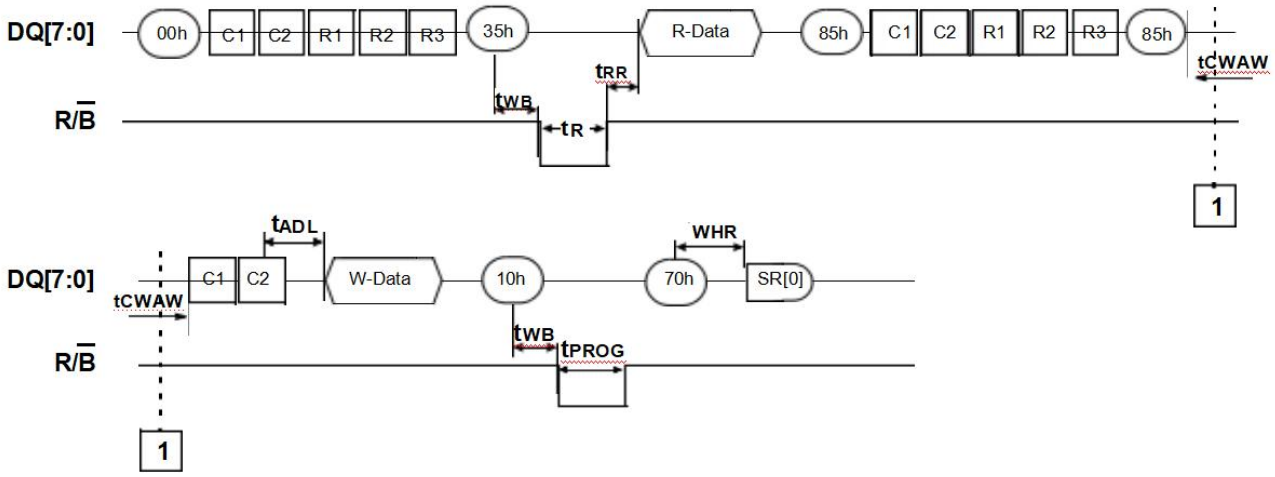


Figure 25. Copy-Back Program with Random Data Input Sequence

7.2.9 Set Feature Operation

Users may set particular features using 'Set Feature' operation. Once a feature is set by users, it shall not be changed until the device is powered off or setting is changed by users. Figure 26 defines the Set Features behavior and timings and Table 29 defines features that users can change.

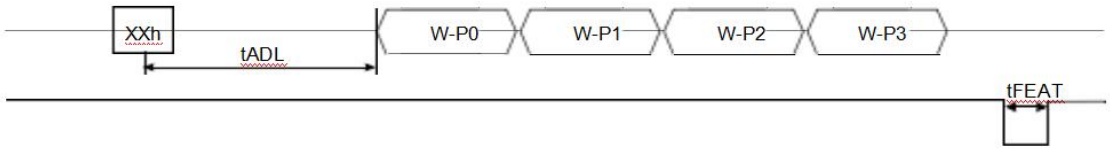


Figure 26. Set Feature Sequence

[Table 29] Set Feature EFh Addresses

Address	Description
02h	Toggle 2.0 specific setting
10h	Driver strength setting
30h	External VPP setting

7.2.9.1 Toggle 2.0 Specific Setting (02h)

This setting is required in order to use reference voltage and complementary signal. DQS latency cycle can also be configured by this SET FEATURE operation to read the first valid data correctly.
When VREFQ signal or complementary signals are set, those signals shall be applied before SET FEATURE sequence. The setting is done at the rising edge of R/B, thus the signals are used to check ready by READ STATUS operation.

[Table 30] Toggle 2.0 Specific Setting Assignment

P0	**I/O7**	**I/O6**	**I/O5**	**I/O4**	**I/O3**	**I/O2**	**I/O1**	**I/O0**
	N/A				Reserved	RE	DQS	VREFQ
P1	**I/O7**	**I/O6**	**I/O5**	**I/O4**	**I/O3**	**I/O2**	**I/O1**	**I/O0**
	# of Latency DQS cycle for WRITE				# of Latency DQS cycle for READ			

NOTE :
1) P2 and P3 are reserved.
2) P2, P3, N/A, and reserved shall be written with 00h.
3) When differential signaling (i.e. RE and DQS) is used, VREFQ shall be set to be enabled for DQ.
4) Setting value of Latency of DQS Cycle does not applied to Set/Get feature operation timing - always operating as default value.

[Table 31] Definition of Toggle 2.0 Specific Setting

	Description
VREFQ	0 : Disabled (Default) 1 : Enabled
DQS	0 : Disabled (Default) 1 : Enabled
RE	0 : Disabled (Default) 1 : Enabled
# of Latency DQS Cycle (WRITE)	0000 : No Latency DQS Cycle (Default) 0001 : One Latency DQS Cycle 0010 : Two Latency DQS Cycle
# of Latency DQS Cycle (READ)	0000 : No Latency DQS Cycle (Default) 0001 : One Latency DQS Cycle 0010 : Two Latency DQS Cycle

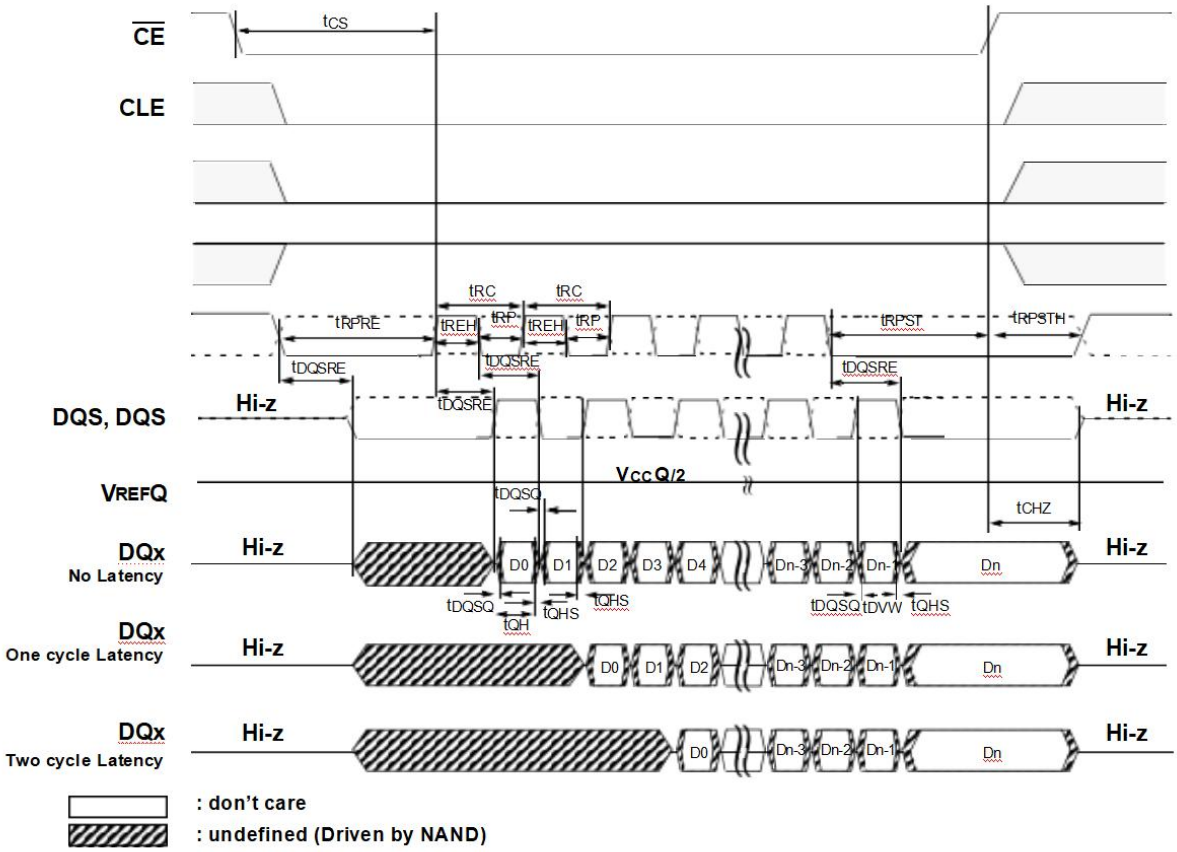


Figure 27. Example of DQS Latency (Read)

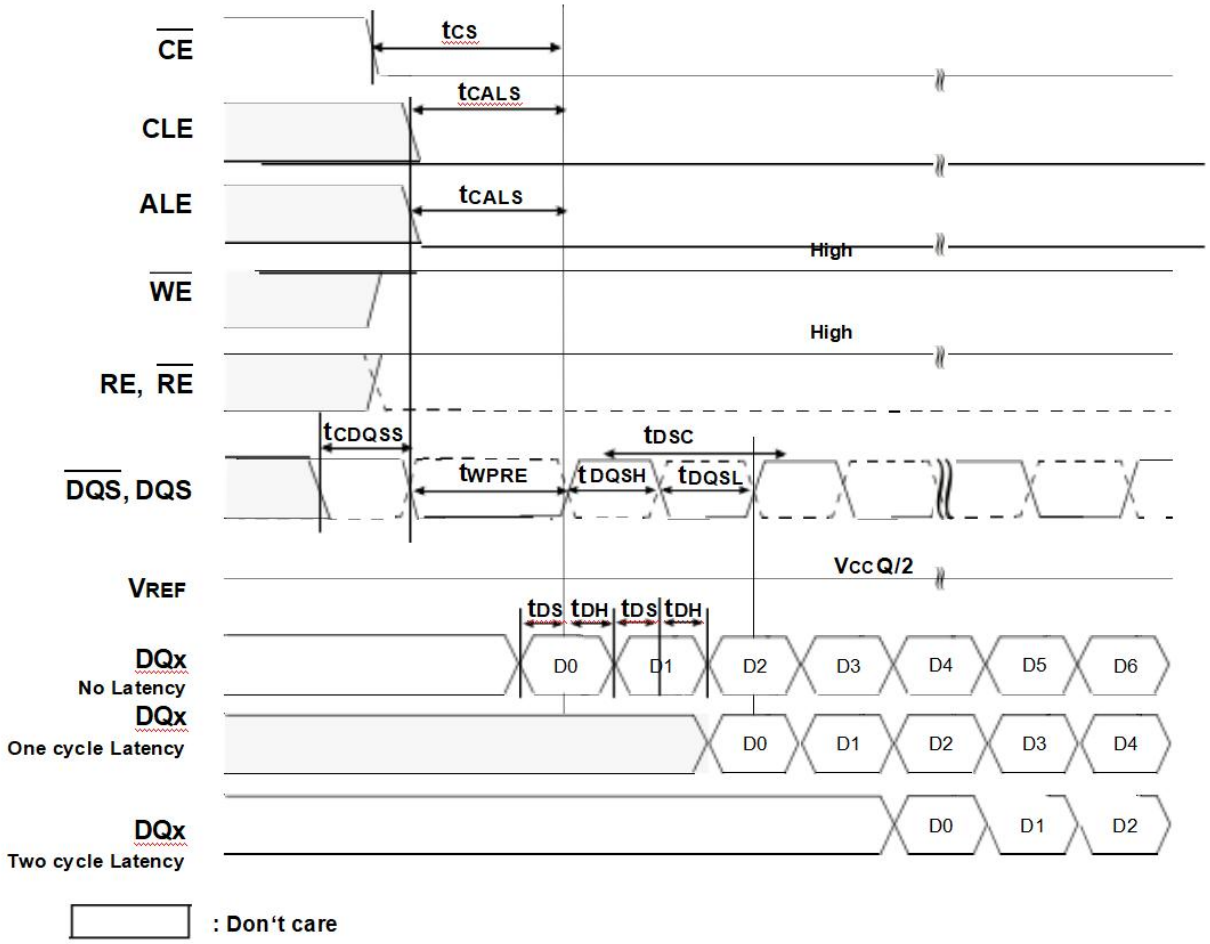


Figure 28. Example of DQS Latency (Write)

7.2.9.2 Driver Strength Setting (10h)

Driver strength is configured according to the P0 value.

[Table 32] Definition of Driver Strength Setting

P0 Value	Description
00h	Reserved
01h	Reserved
02h	Driver Multiplier : Underdriver(x0.7)
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	N/A
07h	Reserved
08h	N/A
09h ~ FFh	Reserved

NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

7.2.9.3 External VPP(30h)

(WARNING : SAMSUNG RECOMMENDS THE USER TO CONTACT AND CONSULT SAMSUNG BEFORE ENABLING THIS FUNCTION. ENABLING THIS FUNCTION MAY CAUSE MALFUNCTION, INCLUDING BUT NOT LIMITED TO PERMENANT DAMAGE TO THE CHIP).
External high voltage(i.e. typical 12V) feature offers power saving on program and read operations. The external high voltage shall be supplied prior to the feature setting and it shall persist within 11.0V to 13.0V until it is set to default (i.e. off). The maximum external VPP supply current per LUN is 5mA.

[Table 33] Definition of External VPP

P0 Value	Description
00h	OFF (Default)
01h	ON
02h ~ FFh	Reserved

NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

7.2.10 Set Feature Operation - LUN Control Within 1 $\overline{CE}$

Users may set particular features using 'Set Feature' operation by inputting chip address. Once a feature is set by users, it shall not be changed until the device is powered off or setting is changed by users. Figure 29 defines the Set Features behavior and timings.

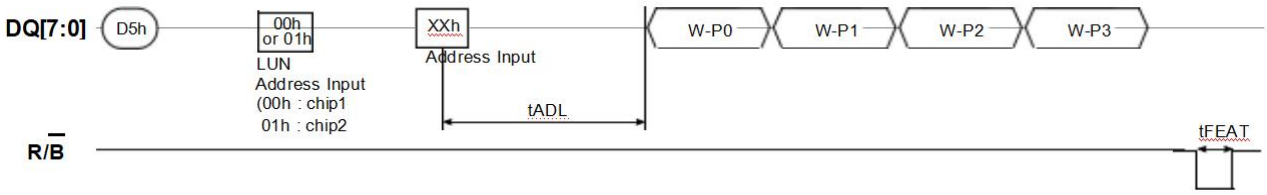


Figure 29. Set Feature Sequence - LUN control within 1$\overline{CE}$

7.2.10.1 Read Retry Setting (89h)

Read Retry feature can relieve fail bit by reading again when read error occurs. If read operation is fail, read level should be set through set feature-read retry (89h). Read operation at read level newly set can relieve fail bit.

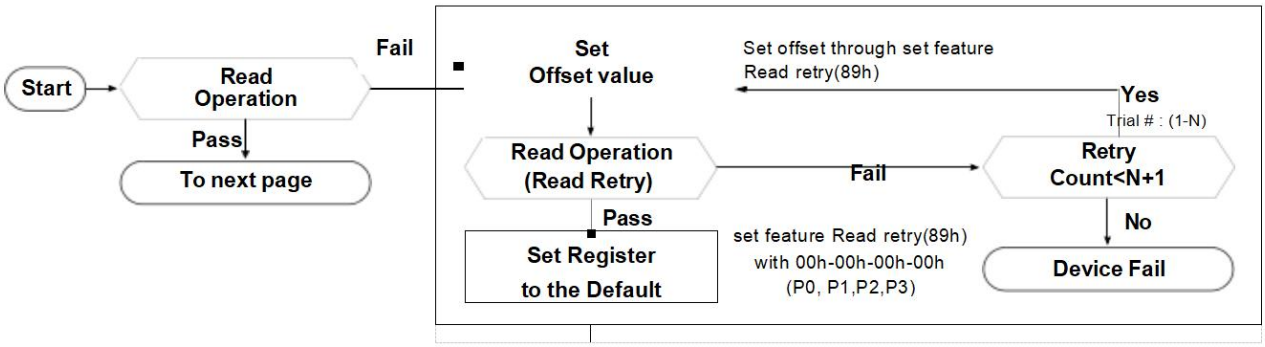


Figure 30. Read Retry Sequence

W-P0	W-P1	W-P2	W-P3	Description
00h	00h	00h	00h	Read Retry off (Default)
RP0, RP1, RP2, RP3 ≠ 00h				Read retry Offset Setting

[Table 34] Specific Data of Read Retry

P0/P1/P2/P3 value	Definition	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
0h	Default	0	0	0	0	0	0	0	0
1h	+ΔmV	0	0	0	0	0	0	0	1
2h	+2ΔmV	0	0	0	0	0	0	1	0
3h	+3ΔmV	0	0	0	0	0	0	1	1
4h	+4ΔmV	0	0	0	0	0	1	0	0
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
FCh	-4ΔmV	1	1	1	1	1	1	0	0
FDh	-3ΔmV	1	1	1	1	1	1	0	1
FEh	-2ΔmV	1	1	1	1	1	1	1	0
FFh	-ΔmV	1	1	1	1	1	1	1	1

7.2.11 Get Feature Operation

Users find how the target is set through ‘Get Feature’ command. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. P0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status). Figure 32 defines the Get Features behavior and timings.

If Read Status is used to monitor whether the tFEAT time is complete, the host shall issue Read command (i.e. 00h) to read P0-P1-P2-P3.

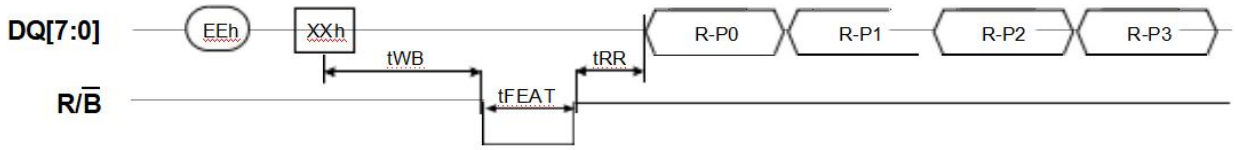


Figure 32. Get Feature Sequence

[Table 35] Get Feature EEh Addresses

Feature Address	Description
02h	Toggle 2.0 Specific Setting
10h	Driver Strength Setting
30h	External VPP Setting

7.2.12 Get Feature Operation - LUN Control within 1 $\overline{CE}$

Users find how the target is set through 'Get Feature' command by inputting chip address. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. P0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status). Figure 33 defines the Get Features behavior and timings.
If Read Status is used to monitor whether the tFEAT time is complete, the host shall issue Read command (i.e. 00h) to read P0-P1-P2-P3.

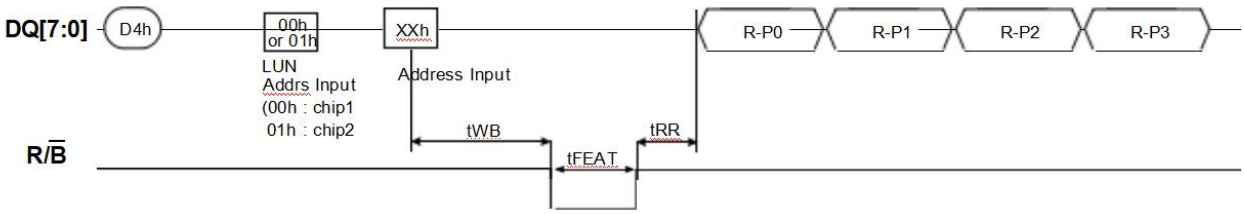


Figure 33. Get Feature Sequence - LUN control within 1$\overline{CE}$

7.2.13 Read ID Operation

The ID of a target is read by command 90h followed by 00h or 40h address. Read ID operation shall work on lower than 66Mhz. Figure 34 defines Read ID operation behavior and timings.

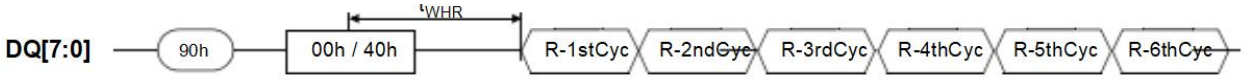


Figure 34. Read ID Sequence

7.2.13.1 00h Address ID Definition

Users can read six bytes of ID containing manufacturer code, device code and architecture information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

7.2.13.2 00h Address ID Cycle

Device		1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
			3.3VccQ				
MKPV32G08CT-ABG	SDP	ECh	D7h	84h	C3h	A0h	CAh

[Table 36] 00h Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4th Byte	Page Size, Block Size, Redundant Area Size.
5th Byte	Plane Number, ECC Level, Organization.
6th Byte	Device Technology, EDO, Interface.

[Table 37] 3rd ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleaving Operation between Multiple Chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

[Table 38] 4th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Page Size (w/o Redundant Area)	Reserved Reserved 8KB 16KB							0 0 1 1	0 1 0 1
Block Size (w/o Redundant Area)	4.6875MB 6MB 512KB 1MB 12.375MB 2MB 3MB 4MB	0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 0 0 1				
Redundant Area Size (Byte / Page Size)	768B 896B 1792B 2KB 1536B 512B 640B 1KB		0 0 0 0 1 1 1 1			0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1		

[Table 39] 5th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Plane Number	1 2 4 8 16					0 0 0 0 1	0 0 1 1 1	0 1 0 1 1	
ECC Level	1bit 2bit 4bit 8bit 16bit 24bit 40bit 60bit LDPC 70bit 48bit	0 0 0 0 0 0 0 0 1 1 1	0 0 1 1 0 0 1 1 0 0 1	0 0 0 0 1 1 1 1 0 0 0	0 1 0 1 0 1 0 1 0 1 0				
Reserved									0

[Table 40] 6th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Device Version	50nm 40nm 30nm 2xnm 2ynm 1xnm 1ynm 1znm					0 0 0 0 0 0 0 1	0 0 0 0 1 1 1 0	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 0
EDO	Not Support Support		0 1						
Interface	Conventional Mode Toggle Mode	0 1							
Reserved				0 0					

7.2.13.3 40h Address ID Definition

Toggle DDR NAND also provide a six bytes of JEDEC standard signature ID. Users can read the ID by command 90h followed by 40h address. Any data returned after the six bytes of JEDEC standard signature is considered reserved for future use.

[Table 41] 40h Address ID Cycle

1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
4Ah	45h	44h	45h	43h	02h

[Table 42] 40h Address ID Definition

Cycle	Description	IDQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st	J	0	1	0	0		0	1	0
2nd	E	0	1	0	0		0	1	1
3rd	D	0	1	0	0		1	0	0
4th	E	0	1	0	0		1	0	1
5th	C	0	1	0	0		0	1	1
6th	Conventional Asynchronous SDR Toggle DDR Synchronous DDR	0 0	0 0	0 0	0 0		0 0 1	0 1 0	1 0 0

7.2.14 Read Status Operation

In the case of non-Two-Plane operations, the Read Status function retrieves a status value for the last operation issued. If multiple Two-Plane operations are in progress on a single LUN, then Read Status returns the composite status value. Specifically, Read Status shall return the combined status value of the independent status register bits according to Table 43. Figure 35 defines the Read Status behavior and timings.

[Table 43] Read Status Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect

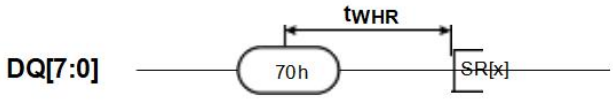


Figure 35. Read Status Sequence

7.2.15 Reset Operation

Toggle DDR NAND offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations except during power-on when Reset shall not be issued until R/B# is set to one (i.e. ready). The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Although the device is already in process of reset operation, a new reset command will be accepted. Figure 36 defines the Reset behavior and timings.

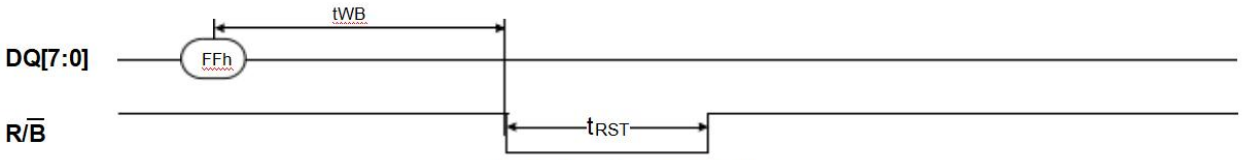


Figure 36. Reset Sequence

7.2.16 Reset LUN Operation

A certain LUN within a target can be reset by command FAh followed by row addresses. Row addresses are required to set a LUN to be reset. Figure 37 defines the Reset LUN behavior and timings.

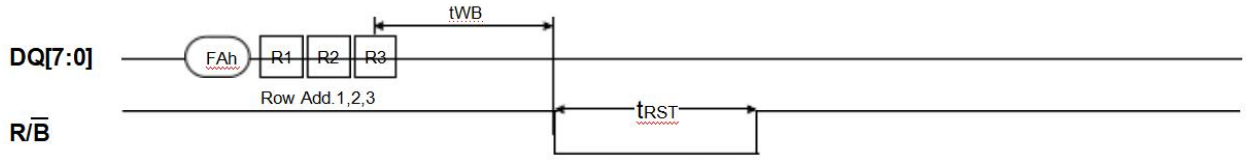


Figure 37. Single Chip Reset Sequence

7.3 Extended Operation

7.3.1 Extended Command Sets

Table 44 defines the Extended Command Sets. Primary and Secondary Commands are also categorized in the Table. Primary Commands are recommended to use when a particular function is implemented, while Secondary Commands are for alternative implementation for backward compatibility.

[Table 44] Extended Command Sets

Function	1st Set	Address Cycles for 1st Set	2nd Set	Address Cycles for 2nd Set
Device Identification Table Read	ECh--	1	-	-

7.3.2 Device Identification Table Read Operation

The device shall return a JEDEC standard formatted parameter page during the data out phase of the READ PARAMETER PAGE command when address 40h is inputted. The READ PARAMETER PAGE command is a ECh value for the command cycle and a 40h value for the address cycle, and the bytes of the parameter page are returned in the data output (DOUT) cycles.
After the command ECh address 40h is received by the NAND device, it will go busy for a period of time (tR in the figure) after which, the parameter page can be read from the device. The length and contents of the parameter page is to be determined. The timing associated with the bus cycles for the READ PARAMETER PAGE command is defined elsewhere in the JEDEC standard.
The READ ID command is used by the controller to identify the device that is attached. This command is used by the controller to gather information about the target flash device. Figure 38 defines the behavior and timings.

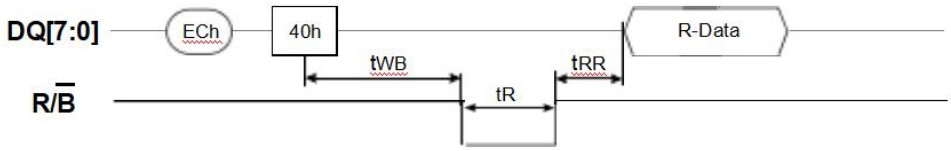


Figure 38. Device Identification Table Read Sequence

7.3.2.1 Device Identification Table Definition

Table 45 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data bytes are in a page.
All optional parameters that are not implemented shall be cleared to 00h by the target.

[Table 45] Parameter Page Definitions

Byte	O/M	Description
Revision Information and Features Block		
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)
4-5	M	Revision number 2-15: Reserved (0) 1: 1 = supports revision 1.0 0: Reserved (0)
6-7	M	Features supported 0-15 Reserved (0) <To be defined based on feature discussions.>
8-10	M	Optional commands supported 0-23: Reserved (0) <To be defined based on command set discussions.>
11-31		Reserved (0)
Manufacturer Information Block		
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64-69	M	JEDEC manufacturer ID (6 bytes)
70-71	TBD	TBD
72-79		Reserved (0)
Memory Organization Block		
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)

100	M	Number of logical units (LUNs)
TBD-TBD	TBD	TBD
Memory Organization Block		
101	M	Number of address cycles 4-7: Column address cycles 0-3: Row address cycles
102	M	Number of bits per cell
103	M	Number of programs per page
104	M	Multi-Plane addressing 4-7: Reserved (0) 0-3: Number of plane address bits
105	M	Multi-Plane operation attributes 3-7: Reserved (0) 2: Address restrictions for cache operations 1: 1= read cache supported 0: 1 = program cache supported
106-143		Reserved (0)
Electrical Parameters Block		

144	O	0:1 = supports 100ns speed grade(~10Mhz) 1:1 = supports 50ns speed grade(~20Mhz) 2:1 = supports 35ns speed grade(~28Mhz) 3:1 = supports 30ns speed grade(~33Mhz) 4:1 = supports 25ns speed grade(~40Mhz) 5:1 = supports 20ns speed grade(~50Mhz) 6-7 = Reserved
145	O	8-15 : Reserved(0)
146-147	O	Toggle DDR speed grade 0: 1 = supports 30 ns speed grade (~33 Mhz) 1: 1 = supports 25 ns speed grade (40 Mhz) 2: 1 = supports 15 ns speed grade (~66 Mhz) 3: 1 = supports 12 ns speed grade (~83 Mhz) 4: 1 = supports 10 ns speed grade (~100 Mhz) 5: 1 = supports 7.5 ns speed grade (~133 Mhz) 6: 1 = supports 6 ns speed grade (~166 Mhz) 7: 1 = supports 5 ns speed grade (~200 Mhz) 8:1 = supports 3.75 ns speed grade (~266Mhz) 9:1 = supports 3 ns speed grade (~333Mhz) 10:1 = supports 2.5 ns speed grade (~400Mhz) 11-15 = Reserved
148-149	O	0-15: Reserved (0)
150	O	0:1 = supports 100ns speed grade(~10Mhz) 1:1 = supports 50ns speed grade(~20Mhz) 2:1 = supports 35ns speed grade(~28Mhz) 3:1 = supports 30ns speed grade(~33Mhz) 4:1 = supports 25ns speed grade(~40Mhz) 5:1 = supports 20ns speed grade(~50Mhz) 6-7: Reserved (0)
151	O	Toggle DDR features 0-7: Reserved (0)
152	O	0-7: Reserved (0)
153-154	M	tPROG Maximum page program time (µs)
155-156	M	tBERS Maximum block erase time (µs)
157-158	M	tR Maximum page read time (µs)
159-160	O	tR Maximum Multi-Plane page read time (µs)
161-162	O	tCCS Minimum change column setup time (ns)

163-164	M	I/O pin capacitance, typical
165-166	M	Input pin capacitance, typical
167-168	O	Reserved
169	M	Driver strength support 3-7: Reserved (0) 2: 1 = supports Overdrive 2 driver strength 1: 1 = supports Overdrive 1 driver strength 0: 1 = supports driver strength settings
170-207		Reserved (0)
ECC and Endurance Block		
208	M	Guaranteed valid blocks at beginning of target
209-210	M	Block endurance for guaranteed valid blocks
211-218	M	ECC and endurance information block 0 Byte 211: Number of bits ECC correctability Byte 212: Codeword size Byte 213-214: Bad blocks maximum per LUN Byte 215-216: Block endurance Byte 217-218: Reserved (0)
219-226	O	ECC and endurance information block 1 Byte 219: Number of bits ECC correctability Byte 220: Codeword size Byte 221-222: Bad blocks maximum per LUN Byte 223-224: Block endurance Byte 225-226: Reserved (0)

227-234	O	ECC and endurance information block 2 Byte 227: Number of bits ECC correctability Byte 228: Codeword size Byte 229-230: Bad blocks maximum per LUN Byte 231-232: Block endurance Byte 233-234: Reserved (0)
235-242	O	ECC and endurance information block 3 Byte 235: Number of bits ECC correctability Byte 236: Codeword size Byte 237-238: Bad blocks maximum per LUN Byte 239-240: Block endurance Byte 241-242: Reserved (0)
243-271	Reserved (0)	
Reserved		
272-419		Reserved (0)
Vendor Specific Block		
420-421	M	Vendor specific Revision number
422-509		Vendor specific
CRC for Parameter Page		
510-511	M	Integrity CRC
Redundant Parameter Pages		
512-1023		Value of bytes 0-511
1024-1535		Value of bytes 0-511
1536+		Additional redundant parameter pages

Byte 0-3: Parameter page signature
This field contains the parameter page signature.
When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Ah.
Byte 1 shall be set to 45h.
Byte 2 shall be set to 53h.
Byte 3 shall be set to 44h.

Byte 4-5: Revision number
This field indicates the revisions of the standard that the target complies to.
The target may support multiple revisions of the standard.
This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.
Bit 1 when set to one indicates that the target supports revision 1.0.
Bits 2-15 are reserved and shall be cleared to zero.

Byte 6-7: Features supported
This field indicates the optional features that the target supports.

<TBD based on feature discussions.>

Byte 8-10: Optional commands supported
This field indicates the optional commands that the target supports.

<TBD based on command discussions.>

Byte 32-43: Device manufacturer
This field contains the manufacturer of the device.
The content of this field is an ASCII character string of twelve bytes.
The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string.
If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID.

Byte 44-63: Device model
This field contains the model number of the device.
The content of this field is an ASCII character string of twenty bytes.
The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

Byte 64-69: JEDEC manufacturer ID
This field contains the JEDEC manufacturer ID for the manufacturer of the device.

Byte 70-71: TBD

Byte 80-83: Number of data bytes per page
This field contains the number of data bytes per page.
The value reported in this field shall be a power of two.
The minimum value that shall be reported is 512 bytes.

Byte 84-85: Number of spare bytes per page

This field contains the number of spare bytes per page. There are no restrictions on the value.

<TBD: Recommendations should be developed based on ECC strength needed.>

Byte 86-89: Number of data bytes per partial page
This field contains the number of data bytes per partial page.
The value reported in this field shall be a power of two.
The minimum value that shall be reported is 512 bytes.

Byte 90-91: Number of spare bytes per partial page
This field contains the number of spare bytes per partial page.
There are no restrictions on the value.

Byte 92-95: Number of pages per block
This field contains the number of pages per block.

<TBD: Should reference address format.>

Byte 96-99: Number of blocks per logical unit
This field contains the number of blocks per logical unit.
There are no restrictions on this value.

<TBD: Should reference address format.>

Byte 100: Number of logical units (LUNs)
This field indicates the number of logical units the target supports.
Logical unit numbers are sequential, beginning with a LUN address of 0.
This field shall be greater than zero.

<TBD: Should reference address format.>

Byte 101: Number of Address Cycles
This field indicates the number of address cycles used for row and column addresses.
The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.
Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE :
Throughout this standard examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field .

Byte 102: Number of bits per cell
This field indicates the number of bits per cell in the Flash array.
This field shall be greater than zero.

Byte 103: Number of programs per page
This field indicates the maximum number of times a portion of a page may be programmed without an erase operation.
After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page.
This field shall be greater than zero.

Byte 104: Multi-Plane addressing
This field describes parameters for Multi-Plane addressing.
Bits 0-3 indicate the number of bits that are used for plane addresses.
This value shall be greater than 0h when Multi-Plane operations are supported.
Bits 4-7 are reserved.

Byte 105: Multi-Plane operation attributes
This field describes attributes for Multi-Plane operations.
This byte is mandatory when Multi-Plane operations are supported as indicated in the Features supported field.

Bit 0 indicates whether program cache is supported with Multi-Plane programs.
If set to one then program cache is supported for Multi-Plane program operations.
If cleared to zero then program cache is not supported for Multi-Plane program operations.
Note that program cache shall not be used with Multi-Plane copy-back program operations.
See bit 2 for restrictions on the plane addresses that may be used.

Bit 1 indicates whether read cache is supported with Multi-Plane reads.
If set to one then read cache is supported for Multi-Plane read operations.
If cleared to zero then read cache is not supported for Multi-Plane read operations.
Note that read cache shall not be used with Multi-Plane copy-back read operations.

Bit 2 indicates whether plane addresses may change during either:
a) a program cache sequence between 15h commands, or b) a read cache sequence between 31h commands.
If set to one and bit 0 is set to one, then the host may change the number and value of plane addresses in the program cache sequence. If set to one and bit 1 is set to one, then the host may change the number and value of plane addresses in the read cache sequence.
If cleared to zero and bit 0 is set to one, then for each program cache operation the plane addresses and number of plane addresses issued to the LUN shall be the same.
If cleared to zero and bit 1 is set to one, then for each read cache operation the plane addresses and number of plane addresses issued to the LUN shall be the same.
Bits 3-7 are reserved.

Byte 144-145: Asynchronous SDR speed grade.
Bit 0 when set to one indicates that the target supports the 100 ns Asynchronous SDR speed grade (~10 Mhz).
Bit 1 when set to one indicates that the target supports the 50 ns Asynchronous SDR speed grade (~20 Mhz).
Bit 2 when set to one indicates that the target supports the 35 ns Asynchronous SDR speed grade (~28 Mhz).
Bit 3 when set to one indicates that the target supports the 30 ns Asynchronous SDR speed grade (~33 Mhz).
Bit 4 when set to one indicates that the target supports the 25 ns Asynchronous SDR speed grade (~40 Mhz).
Bit 5 when set to one indicates that the target supports the 20 ns Asynchronous SDR speed grade (~50 Mhz).
Bit 6-15 are reserved.

Byte 146-147: Toggle DDR speed grade
This field indicates the Toggle DDR speed grades supported. The target shall support an inclusive range of speed grades.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 Mhz).
Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 Mhz).
Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 Mhz).
Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 Mhz).
Bit 4 when set to one indicates that the target supports the 10 ns speed grade (~100 Mhz).
Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 Mhz).
Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 Mhz).
Bit 7 when set to one indicates that the target supports the 5 ns speed grade (~200 Mhz).
Bit 8 when set to one indicates that the target supports the 3.75 ns speed grade (~266 Mhz).
Bits 9-15 are reserved and shall be cleared to zero.

Byte 148-149: Reserved

Byte 150: Asynchronous SDR speed grade.
Bit 0 when set to one indicates that the target supports the 100 ns Asynchronous SDR speed grade (~10 Mhz).
Bit 1 when set to one indicates that the target supports the 50 ns Asynchronous SDR speed grade (~20 Mhz).
Bit 2 when set to one indicates that the target supports the 35 ns Asynchronous SDR speed grade (~28 Mhz).
Bit 3 when set to one indicates that the target supports the 30 ns Asynchronous SDR speed grade (~33 Mhz).
Bit 4 when set to one indicates that the target supports the 25 ns Asynchronous SDR speed grade (~40 Mhz).
Bit 5 when set to one indicates that the target supports the 20 ns Asynchronous SDR speed grade (~50 Mhz).
Bit 6-7 are reserved.

Byte 151: Toggle DDR features
This field describes features and attributes for Toggle DDR operation.
This byte is mandatory when the Toggle DDR data interface is supported.
Bits 0-7 are reserved.

Byte 152: Reserved

Byte 153-154: Maximum page program time
This field indicates the maximum page program time (tPROG) in microseconds.

Byte 155-156: Maximum block erase time
This field indicates the maximum block erase time (tBERS) in microseconds.

Byte 157-158: Maximum page read time

This field indicates the maximum page read time (tR) in microseconds.

Byte 159-160: Maximum Multi-Plane **page read time**
This field indicates the maximum page read time (tR) for Multi-Plane page reads in microseconds.
Multi-Plane page read times may be longer than single page read times.
This field shall be supported if the target supports Multi-Plane reads as indicated in the Features supported field.

Byte 161-162: Minimum change column setup time
This field indicates the minimum change column setup time (tCCS) in nanoseconds.
This parameter is used for the asynchronous SDR and synchronous DDR data interfaces.

After issuing a Change Read Column command, the host shall not read data until a minimum of tCCS time has elapsed.
After issuing a Change Write Column command including all column address cycles, the host shall not write data until a minimum of tCCS time has elapsed. The value of tCCS shall always be longer than or equal to tWHR and tADL when the Toggle DDR or synchronous DDR data interface is supported.

Byte 163-164: I/O pin capacitance, typical
This field indicates the typical I/O pin capacitance for the target. This field is specified in 0.1 pF units.
For example, a value of 31 corresponds to 3.1 pF.
The variance from this value is less than +/- 0.5 pF per LUN. As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

Byte 165-166: Input pin capacitance, typical
This field indicates the typical input pin capacitance for the target.
This value applies to all inputs except the following: CE
This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF.
The variance from this value is less than +/- 0.5 pF per LUN.
As an example, if two LUNs are present than the total variance is less than +/- 1 pF.
Byte 167-168: Reserved

Byte 169: Driver strength support
This field describes if the target supports configurable driver strengths and its associated features.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in Table TBD.
If this bit is set to one, then the device shall support both the Nominal and Underdrive settings.
If this bit is set to one, then the device shall power-on with a driver strength at the Nominal value defined in Table TBD.

If this bit is cleared to zero, then the driver strength at power-on is undefined.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 1 when set to one indicates that the target supports the Overdrive 1 setting in Table TBD for use in the I/O Driver Strength setting. This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 2 when set to one indicates that the target supports the Overdrive 2 setting in Table TBD for use in the I/O Driver Strength setting. This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.
Bits 3-7 are reserved.

Byte 208: Guaranteed valid blocks at beginning of target
This field indicates the number of guaranteed valid blocks starting at block address 0 of the target.
The minimum value for this field is 1h.
The blocks are guaranteed to be valid for the endurance specified for this area when the host follows the specified number of bits to correct in ECC information block 0.

Byte 209-210: Block endurance for guaranteed valid blocks
This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area.
This value requires that the host is using at least the minimum ECC correctability reported in ECC information block 0. This value is not encoded. If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

Byte 211-218: ECC information block 0

This block of parameters describes a set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.

Byte 211: Number of bits ECC correctability.
This field indicates the number of bits that the host should be able to correct per codeword. The codeword size is reported in byte 212. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in bytes 215-216.
When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks specified in bytes 213-214 shall not be exceeded by the device.
All used bytes in the page shall be protected by ECC including the spare bytes if the ECC requirement reported in byte 211 has a value greater than zero. When this value is cleared to zero, the target shall return valid data.

Byte 212: Codeword size. The number of bits of ECC correctability specified in byte 211 is based on a particular ECC codeword size. The ECC codeword size is specified in this field as a power of two.
The minimum value that shall be reported is 512 bytes (a value of 9).

Byte 213-214: Bad blocks maximum per LUN.
This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN.
The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in this ECC and endurance information block.

Byte 215-216: Block endurance.
This field indicates the maximum number of program/erase cycles per addressable page/block.
This value assumes that the host is using the ECC correctability reported in byte 211.
The block endurance is reported in terms of a value and a multiplier according to the following equation:
value x $10^{multiplier}$. Byte 215 comprises the value. Byte 216 comprises the multiplier.
For example, a block endurance of 75,000 cycles would be reported as a value of 75 and a multiplier of 3 (75 x 103).
The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 105).

Byte 219-226: ECC information block 1
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 227-234: ECC information block 2
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 235-242: ECC information block 3
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 420-421: Vendor specific Revision number
This field indicates a vendor specific revision number.
This field should be used by vendors to indicate the supported layout for the vendor specific parameter page area and the vendor specific feature addresses. The format of this field is vendor specific.

Byte 422-509: Vendor specific
This field is reserved for vendor specific use.

Byte 510-511: Integrity CRC

The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 509 of the parameter page inclusive. The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:
G(X) = X16 + X15 + X2 + 1
This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Byte 512-1023: Redundant Parameter Page 1
This field shall contain the values of bytes 0-511 of the parameter page. Byte 512 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1024-1535: Redundant Parameter Page 2
This field shall contain the values of bytes 0-511 of the parameter page. Byte 1024 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511 and in the first redundant parameter page. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1536+: Additional Redundant Parameter Pages
Bytes at offset 1536 and above may contain additional redundant copies of the parameter page. There is no limit to the number of redundant parameter pages that the target may provide. The target may provide additional copies to guard against the case where all three mandatory copies have invalid CRC checks.

The host should determine whether an additional parameter page is present by checking the first word. If at least two out of four bytes match the parameter page signature, then an additional parameter page is present.

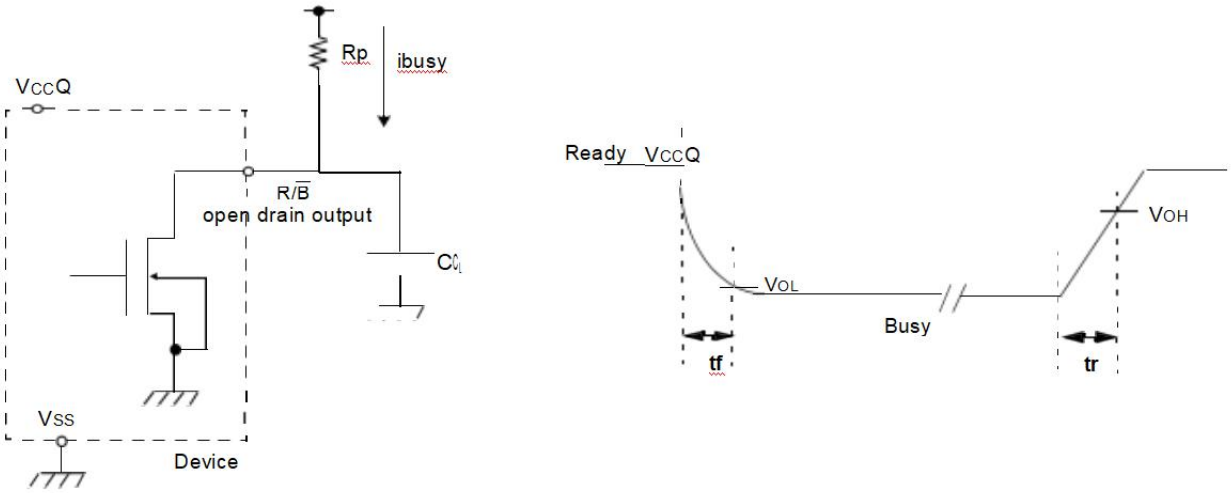
7.3.3 Register Read Out Mode 1

At program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows. To continue pro- gram operation after reading data, Copy-back Program operation (i.e. 85h- Address(5cycle) - Data - 10h) is required.

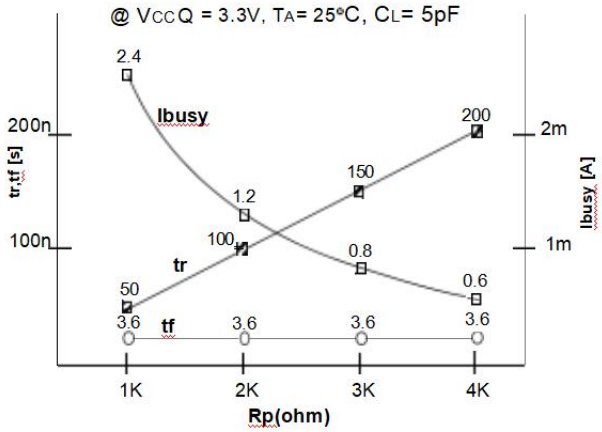
7.4 Ready/ $\overline{\text{B}}$usy

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain

driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.



Rp vs tr ,tf & Rp vs ibusy



Rp Value Guidance

$$Rp(min., 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp (max.) is determined by maximum permissible limit of tr