KP3000A Phase Control Thyristor

Feature

- Full diffusion process,capsule type ceramic package
- Amplifying gates
- Double sided cooling

Typical Application

- High power transmission
- DC and AC motor control,Controlied rectifier
- AC DC switch,phase-controlied rectifying
- Active and reactive invresion

$I_{T(AV)}$	3000A
V_{DRM}/V_{RRM}	100-6500V
I_{TSM}	38KA
I^2t	13005 10^3a^2s

SYMBOL	CHARCTERISTIC	TEST CONDITIONS	T_J (℃)	VALUE		UNIT
				Min	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wawe 50Hz Double side cooled, THS=97℃	125		3000	A
$I_{T(AV)}$	Mean on-state current	180° half sine wawe 50Hz Double side cooled, THS=55℃	125		3790	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repettive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}=V_{DRM}&$V_{RRM+100V}$	125	100	6500	V
I_{DRM} I_{RRM}	Repetitive peak current	V_{DM}=V_{DRM} V_{RM}=V_{RRM}	125		200	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125		38	KA
I^2t	I^2t for fusing coordination				1300	A^{2S}*10
V_{TO}	Threshold voltage		125		0.84	V
r_T	On-state slop resistance				0.09	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=5000A,F=15KN	25		2.4	V
dv/dt	Critical rate of rise of-state voltage	V_{DM}=0.67V_{DRM}	125		1000	V/us
di/dt	Critical rate of rise of on-state current	V_{DM}=67%V_{DRM} TO 1000A, Gate pulse tr≤0.5us I_{GM}=1.5A	125		250	A/us
I_{TM}	Reverse recovery current	I_{TM}=5000A，tq=1000us Di/dt=-20A/us. V_r=50V	125		250	A
t_{rr}	Reverse recovery time				24	us
Q_{rr}	Recovery charge				3000	uC
I_{GT}	Gate trigger current	V_A=12V,I_A=1A	25	40	300	mA
V_{GT}	Gate trigger voltage			0.8	3.0	V
I_H	Holding current			20	300	mA
V_{GD}	Npn-trigger gate voltage	V_{DM}=0.67V_{DRM}	125	0.3		V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At180° sine double side cooled Clamping force 5.0kn			0.011	℃/W
F_M	Mounting force			35	47	KN
T_{stq}	Stored temperature			-40	140	℃
W_t	Weight					g
Outline						

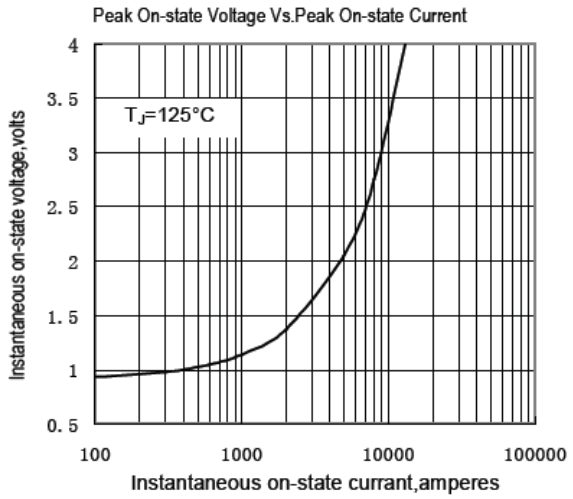


Fig.1

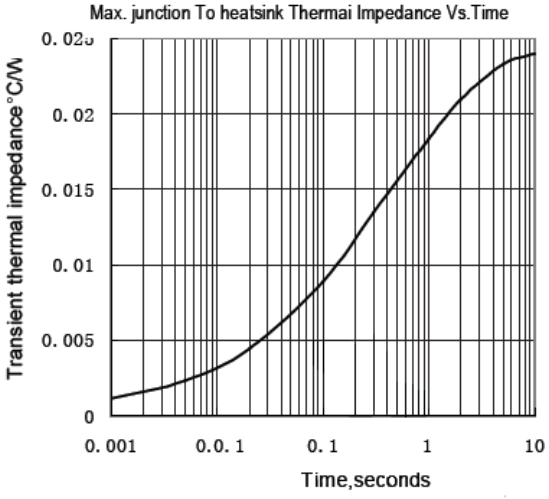


Fig.2

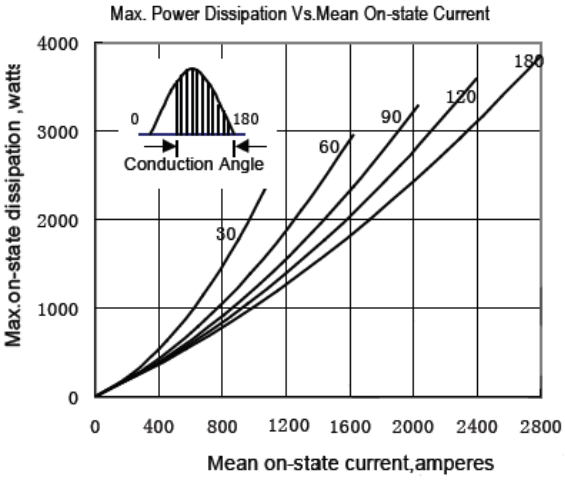


Fig.3

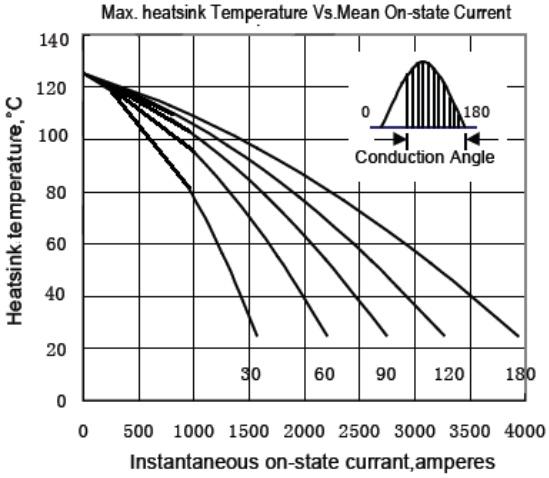


Fig.4

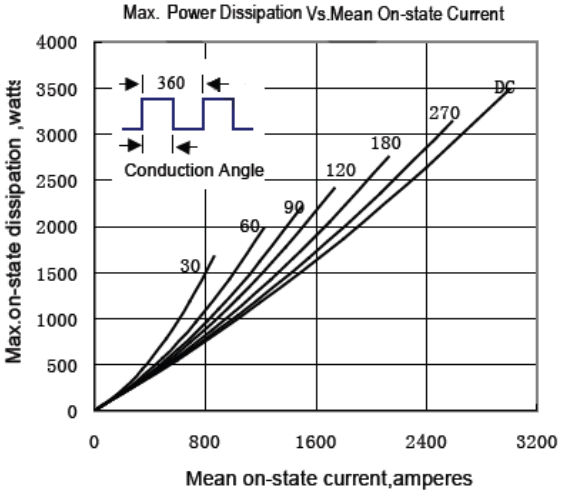


Fig.5

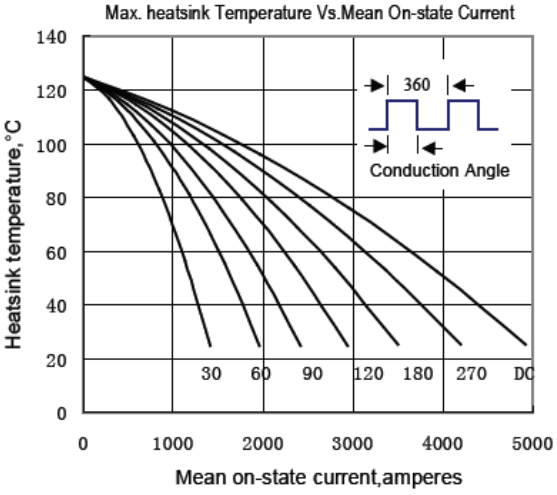


Fig.6

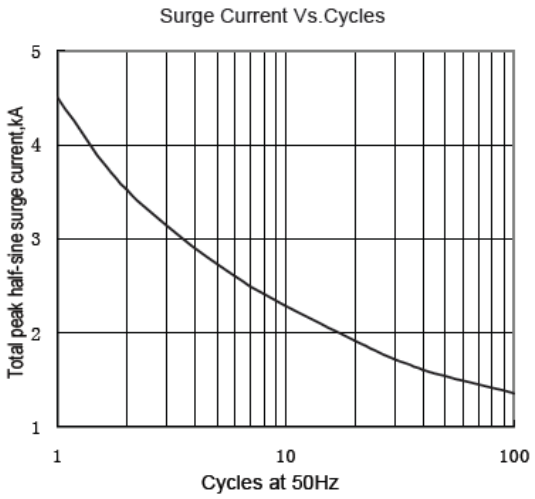


Fig.7

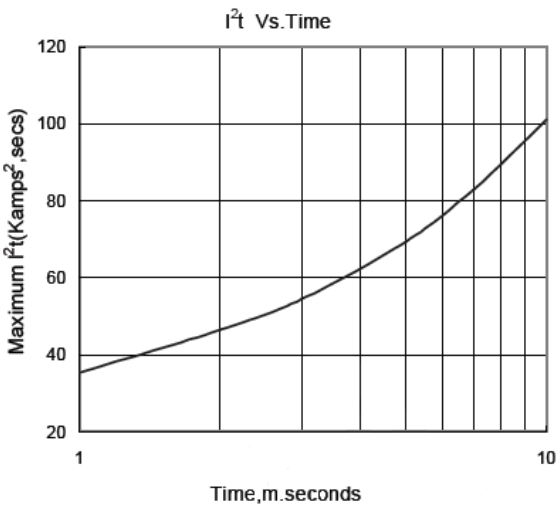


Fig.8

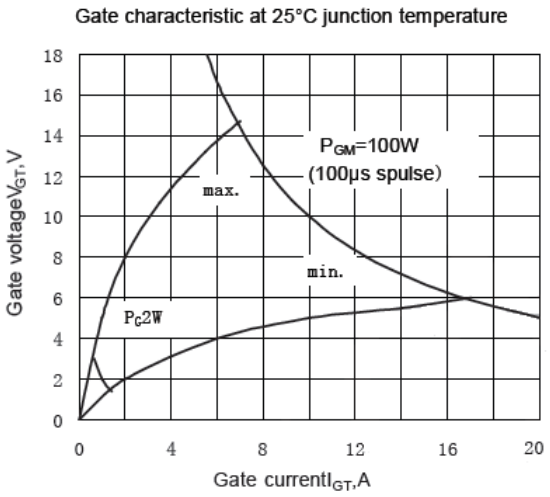


Fig.9

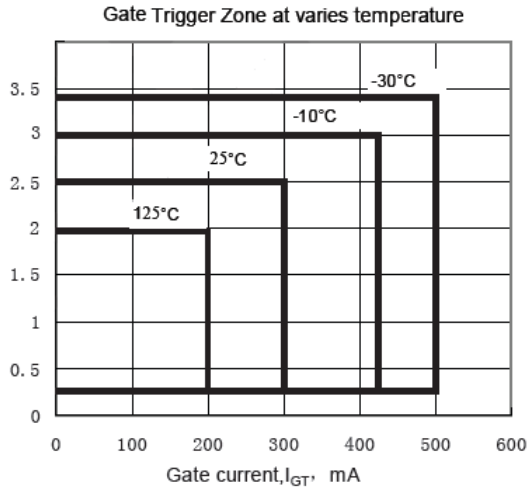


Fig.10

Outline:

