PEDS82V32520-01

OKI Semiconductor

This version: Jul. 2001

MS82V32520

Preliminary

524,288-Word × 32-Bit × 2-Bank FIFO-SGRAM

GENERAL DESCRIPTION

The MS82V32520 is a 32-Mbit system clock synchronous dynamic random access memory. In addition to the conventional random read/write access function, the MS82V32520 provides the automatic row address increment function and automatic bank switching function. Therefore, if once the row and column addresses are set, continuous serial accesses are possible while banks are automatically switched till input of the Precharge command. The MS82V32520 is ideal for digital camera and TV buffer memory applications.

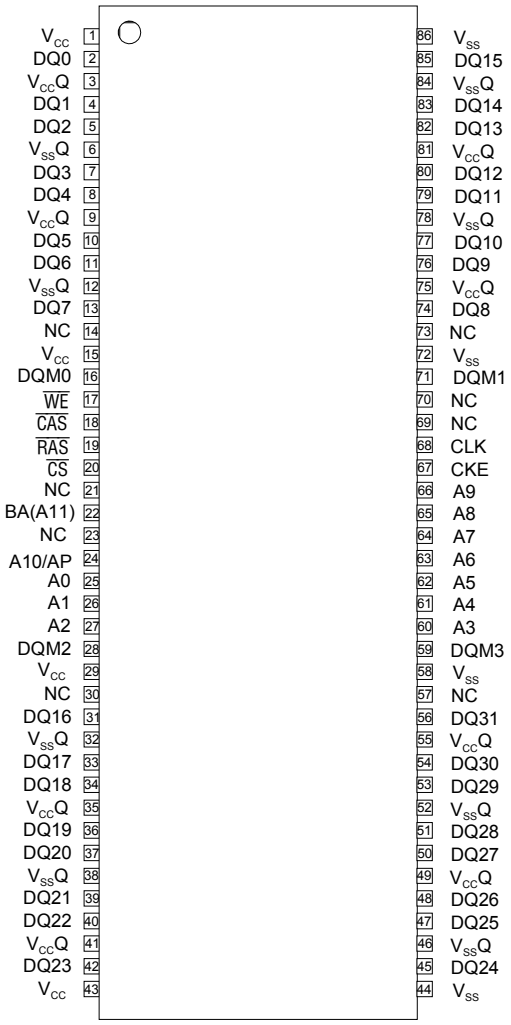
FEATURES

- 524,288 words × 32 bits × 2 banks memory (2,048 rows × 256 columns × 32 bits × 2 banks)
- Single 3.3 V ±0.3 V power supply
- LVTTL compatible inputs and outputs
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable $\overline{\text{CAS}}$ latency (2, 3)
- Automatic row address increment function and automatic bank switching function
- Power Down operation and Clock Suspend operation
- 4,096 refresh cycles/64 ms
- Auto refresh and self refresh capability
- Package:
  86-pin 400 mil plastic TSOP (II) (TSOP (2) 86-P-400-0.50-K) (Product : MS82V32520-xxTA)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Max. Operating Frequency	Access Time	Package
MS82V32520-75	133 MHz	5.5 ns	86-pin Plastic TSOP (II) (400 mil)
MS82V32520-8	125 MHz	6 ns	
MS82V32520-10	100 MHz	7 ns	

PIN CONFIGURATION (TOP VIEW)

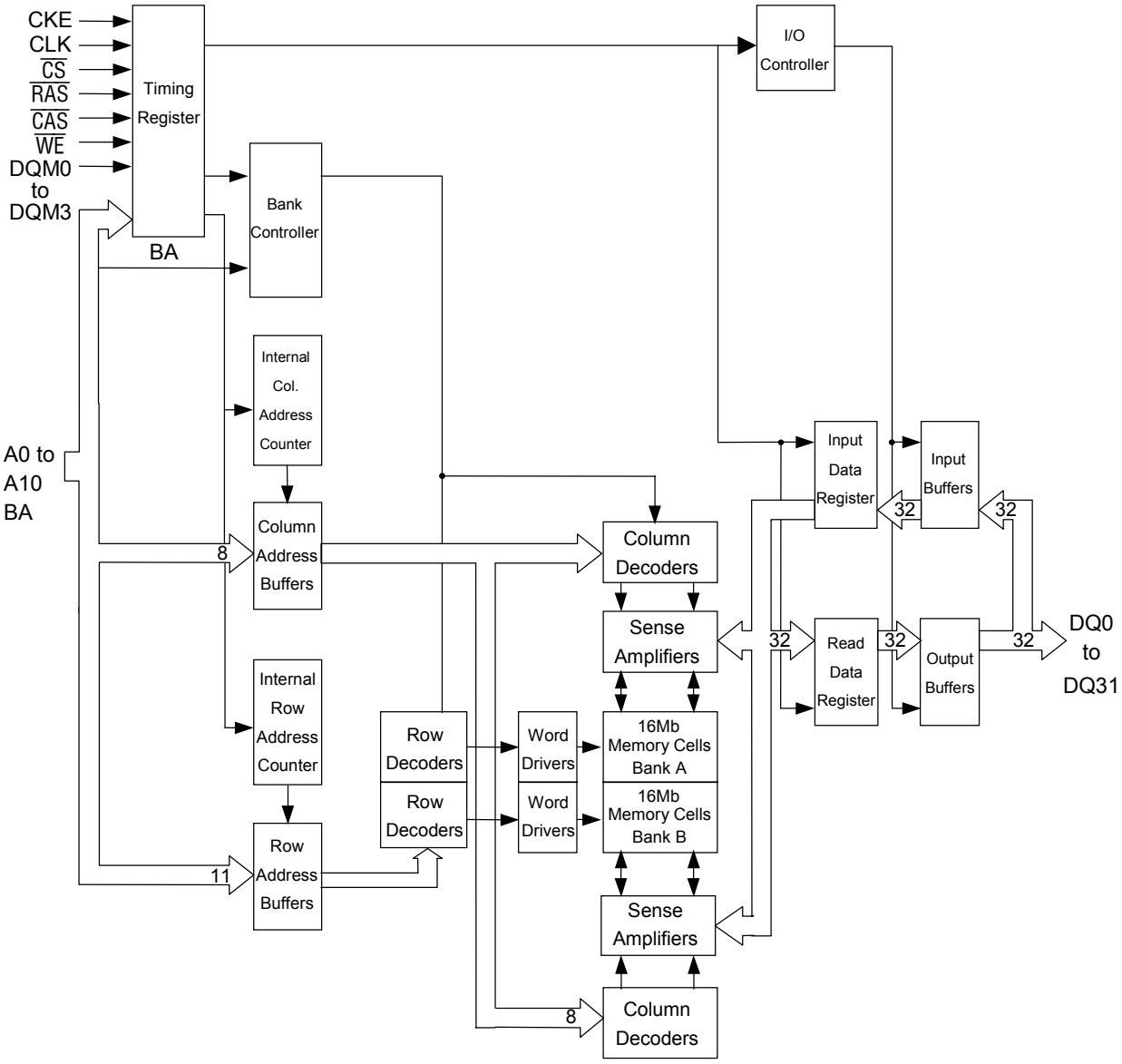


86-Pin Plastic TSOP (II)
(Type K)

Pin Name	Function	Pin Name	Function
A0 – A10	Row Address Inputs	$\overline{WE}$	Write Enable
A0 – A7	Column Address Inputs	DQM0 – DQM3	DQ Mask Enable
BA(A11)	Bank Address	DQ0 – DQ31	Data Inputs/outputs
CLK	System Clock Input	V_{CC}	Supply Voltage
CKE	Clock Enable	V_{SS}	Ground
$\overline{CS}$	Chip Select	$V_{CC}Q$	Supply Voltage for DQ
$\overline{RAS}$	Row Address Strobe	$V_{SS}Q$	Ground for DQ
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}Q$ pin.
The same GND voltage level must be provided to every V_{SS} pin and $V_{SS}Q$ pin.
For the four-bank 64Mb SDRAM, Pin 22 = BA0 and Pin 23 = BA1, and for the two-bank 64Mb SDRAM, Pin 22 = BA.
Therefore, when the MS82V32520 is used in place of a 64Mb SDRAM, care must be taken in bank address control.

BLOCK DIAGRAM



PIN DESCRIPTION

CLK	Fetches all inputs at the "H" edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, DQM0, DQM1, DQM2 and DQM3.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 – RA10 Column address: CA0 – CA7
BA	Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time. BA = “L”: Bank A BA = “H”: Bank B
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
DQM0 – DQM3	Masks the read data of two clocks later when DQM0 - DQM3 are set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM0 - DQM3 are set "H" at the "H" edge of the clock signal. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, and DQM3 controls DQ24 to DQ31.
DQ0 – DQ31	Data inputs/outputs are multiplexed on the same pin.

*Notes: 1. When $\overline{CS}$ is set "High" at a clock transition from "Low" to "High", all inputs except CLK, CKE, DQM0, DQM1, DQM2, and DQM3 are invalid.

2. When issuing an active, read or write command, the bank is selected by BA.

BA	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enabled or disabled by the A10/AP input when the read or write command is issued.

A10/AP	BA	Operation
0	0	After the end of burst, bank A holds the active status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the active status.
1	1	After the end of burst, bank B is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A10/AP and BA inputs.

A10/AP	BA	Operation
0	0	Bank A is precharged.
0	1	Bank B is precharged.
1	×	Both banks A and B are precharged.

COMMAND OPERATION

Mode Register Set Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = "Low")

The MS82V32520 has the mode register that defines the operation mode "$\overline{CAS}$ Latency, Burst Length, Burst Sequence". The Mode Register Set command should be executed just after the MS82V32520 is powered on. Before entering this command, all banks must be precharged. Next command can be issued after t_{RSC}.

Auto Refresh Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = "Low", $\overline{WE}$ = "High")

The Auto Refresh command performs refresh automatically by the address counter. The refresh operation must be performed 4,096 times within 64 ms and the next command can be issued after t_{RC} from last Auto Refresh command. Before entering this command, all banks must be precharged.

Self Refresh Entry/Exit Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{CKE}$ = "Low", $\overline{WE}$ = "High")

The self refresh operation continues after the Self Refresh Entry command is entered, with CKE level left "low". This operation terminates by making CKE level "high". The self refresh operation is performed automatically by the internal address counter on the MS82V32520 chip.
In self refresh mode, no external refresh control is required. Before entering self refresh mode, all banks must be precharged. Next command can be issued after t_{RC}.

Single Bank Precharge Command ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$, A10/AP = "Low", $\overline{CAS}$ = "High")

The Single Bank Precharge command triggers bank precharge operation. Precharge bank is selected by BA.

All Banks Precharge Command ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = "Low", $\overline{CAS}$, A10/AP = "High")

The All Bank Precharge command triggers precharge of both of the banks A and B.
If this command is executed during special bank active mode, the special bank active mode is terminated.

Bank Active Command ($\overline{CS}$, $\overline{RAS}$ = "Low", $\overline{CAS}$, $\overline{WE}$ = "High")

The Bank Active command activates the bank selected by BA. The Bank Active command corresponds to conventional DRAM's $\overline{RAS}$ falling operation. Row addresses "A0 – A10 and BA" are strobed.

Write Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$, A10/AP = "Low", $\overline{RAS}$ = "High")

The Write command is required to begin burst write operation. Then burst access initial bit column address is strobed.

Write with Auto Precharge Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = "Low", $\overline{RAS}$, A10/AP = "High")

The Write with Auto Precharge command is required to begin burst write operation with automatic precharge after the burst write. Any command that interrupts this operation cannot be issued.

Read Command ($\overline{CS}$, $\overline{CAS}$, A10/AP = "Low", $\overline{RAS}$, $\overline{WE}$ = "High")

The Read command is required to begin burst read operation. Then burst access initial bit column address is strobed.

Read with Auto Prechaege Command ($\overline{CS}$, $\overline{CAS}$ = "Low", $\overline{RAS}$, $\overline{WE}$, A10/AP = "High")

The Read with Auto Precharge command is required to begin burst read operation with auto precharge after the burst read. Any command that interrupts this operation cannot be issued.

No Operation Command ($\overline{CS}$ = "Low", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = "High")

The No Operation command does not trigger any operation.

Device Deselect Command ($\overline{CS}$ = "High")

The Device Deselect command disables the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address input. This command does not trigger any operation.

Data Write/Output Enable Command (DQMi = "Low")

The Data Write/Output Enable command enables DQ0 - DQ31 in read or write.
The each DQM0, 1, 2 and 3 corresponds to DQ0 - DQ7, DQ8 - DQ15, DQ16 - DQ23 and DQ24 - DQ31 respectively.

Data Mask/Output Disable Command (DQMi = "High")

The Data Mask/Output Disable command disables DQ0 - DQ31 in read or write. In read cycle output buffers are disabled after 2 clocks . In write cycle input buffers are disabled at the same clock. The each DQM0, 1, 2 and 3 corresponds to DQ0 - DQ7, DQ8 - DQ15, DQ16 - DQ23 and DQ24 - DQ31
respectively.

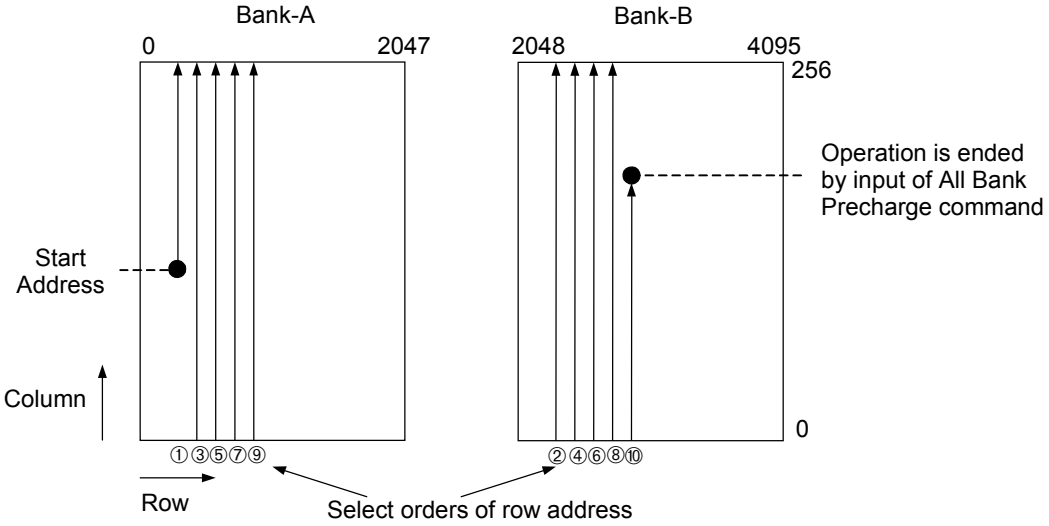
Burst Stop Command ($\overline{CS}$, $\overline{WE}$ = "Low", $\overline{RAS}$, $\overline{CAS}$ = "High")

The Burst Stop command stops burst access. After the Burst Stop command is entered, the output buffer goes into high impedance state.

SPECIAL READ/WRITE OPERATION

The special read or write operation is activated by executing the Read or Write command after selecting the special page mode with the Mode Register command.
The automatic bank switching and automatic row address increment operations are activated by executing the Bank Active command during Special Page mode, and the serial access starts from the address fetched with the Read or Write command. The burst operation starts from the start address toward the column. When the last column address is reached, the bank is automatically switched and the row address is also automatically incremented and the serial access continues from the start column address. The automatic bank switching and automatic row address increment operations continue until the All Bank Precharge command is executed each time the last column address is reached.
Since the bank switching and row address increment are automatically made during the special read or write operation, the row address proceeds as shown in the following figure.

(1) When a select row address is n (n<2048),
n→n + 2048→n + 1→n + 1 + 2048→n + 2→n + 2 + 2048···
(2) When a select row address is m (m>2047),
m→m + 1 – 2048→m + 1→m + 2 – 2048→m + 2→m + 3 – 2048···



TRUTH TABLE

Command Truth Table

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address		
					BA	A10/AP	A9 – A0
Device Deselect	H	×	×	×	×	×	×
No Operation	L	H	H	H	×	×	×
Mode Register Set	L	L	L	L	OP. CODE		
Auto Refresh	L	L	L	H	×	×	×
Bank Activate	L	L	H	H	BA	RA	
Read	L	H	L	H	BA	L	CA (A7 – A0)
Read with Auto Precharge	L	H	L	H	BA	H	CA (A7 – A0)
Write	L	H	L	L	BA	L	CA (A7 – A0)
Write with Auto Precharge	L	H	L	L	BA	H	CA (A7 – A0)
Precharge Select Bank	L	L	H	L	BA	L	×
Precharge All Banks	L	L	H	L	×	H	×
Burst Stop	L	H	H	L	×	×	×

DQM Truth Table

Function	DQMi
Data Write/Output Enable	L
Data Mask/Output Disable	H

Function Truth Table (1/3)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
Idle	H	×	×	×	×	×	NOP	
	L	H	H	H	×	×	NOP	
	L	H	H	L	BA	×	ILLEGAL	2
	L	H	L	×	BA	CA, A10	ILLEGAL	2
	L	L	H	H	BA	RA	Row Active	
	L	L	L	L	L	Op-Code	Mode Register Write	
	L	L	H	L	BA	A10	NOP	4
	L	L	L	H	×	×	Auto Refresh/Self refresh	5
Active (ACT)	H	×	×	×	×	×	NOP	
	L	H	H	×	×	×	NOP	
	L	H	L	H	BA	CA, A10	Read	
	L	H	L	L	BA	CA, A10	Write	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Precharge	
	L	L	L	×	×	×	ILLEGAL	
Active (Special Page Mode) (SACT)	H	×	×	×	×	×	NOP	
	L	H	H	×	×	×	NOP	
	L	H	L	H	BA	CA	Serial Read	
	L	H	L	L	BA	CA	Serial Write	
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A10: L	ILLEGAL	
	L	L	H	L	BA	A10: H	Precharge	
	L	L	L	×	×	×	ILLEGAL	
Read (RD)	H	×	×	×	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	H	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	L	×	×	Burst Stop → Row Active	
	L	H	L	H	BA	CA, A10	Term Burst, new Read	3
	L	H	L	L	BA	CA, A10	Term Burst, start Write	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Term Burst, execute Precharge	
	L	L	L	×	×	×	ILLEGAL	
Write (WT)	H	×	×	×	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	H	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	L	×	×	Burst Stop → Row Active	
	L	H	L	H	BA	CA, A10	Term Burst, start Read	3
	L	H	L	L	BA	CA, A10	Term Burst, new Write	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Term Burst, execute Precharge	3
	L	L	L	×	×	×	ILLEGAL	

Function Truth Table (2/3)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
Read with Auto Precharge (RAP)	H	×	×	×	×	×	NOP (Continue Burst to End and enter Precharge)	
	L	H	H	H	×	×	NOP (Continue Burst to End and enter Precharge)	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	H	BA	CA, A10	ILLEGAL	
	L	H	L	L	BA	CA, A10	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	ILLEGAL	2
	L	L	L	×	×	×	ILLEGAL	
Write with Auto Precharge (WAP)	H	×	×	×	×	×	NOP (Continue Burst to End and enter Precharge)	
	L	H	H	H	×	×	NOP (Continue Burst to End and enter Precharge)	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	H	BA	CA, A10	ILLEGAL	
	L	H	L	L	BA	CA, A10	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	ILLEGAL	2
	L	L	L	×	×	×	ILLEGAL	
Read (Special Page Mode) (SRD)	H	×	×	×	×	×	NOP (Continue serial read)	
	L	H	H	H	×	×	NOP (Continue serial read)	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	×	BA	CA	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A10: L	ILLEGAL	
	L	L	H	L	BA	A10: H	Precharging	
	L	L	L	×	×	×	ILLEGAL	
Write (Special Page Mode) (SWT)	H	×	×	×	×	×	NOP (Continue serial write)	
	L	H	H	H	×	×	NOP (Continue serial write)	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	×	BA	CA	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A10: L	ILLEGAL	
	L	L	H	L	BA	A10: H	Precharging	
	L	L	L	×	×	×	ILLEGAL	
Precharging (PRE)	H	×	×	×	×	×	NOP → Idle after t_{RP}	
	L	H	H	H	×	×	NOP → Idle after t_{RP}	
	L	H	H	L	BA	×	ILLEGAL	2
	L	H	L	×	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	NOP	4
	L	L	L	×	×	×	ILLEGAL	

Function Truth Table (3/3)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
Refreshing (REF)	H	×	×	×	×	×	NOP → Idle after t_{RC}	
	L	H	H	H	×	×	NOP → Idle after t_{RC}	
	L	H	H	L	BA	×	ILLEGAL	
	L	H	L	×	BA	CA	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A10	ILLEGAL	
	L	L	L	×	×	×	ILLEGAL	

ABBREVIATIONS
BA = Bank Address RA = Row Address CA = Column Address
NOP = No Operation command

Notes: 1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. To avoid bus contention, satisfy t_{CCD} and t_{DPL}.
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10/AP.
5. Illegal if any bank is not idle.

Function Truth Table for CKE

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Note
Self Refresh (SREF)	H	×	×	×	×	×	×	INVALID	
	L	H	H	×	×	×	×	Exit Self Refresh → ABI	
	L	H	L	H	H	H	×	Exit Self Refresh → ABI	
	L	H	L	H	H	L	×	ILLEGAL	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	NOP (Maintain Self Refresh)	
Power Down (PD)	H	×	×	×	×	×	×	INVALID	
	L	H	H	×	×	×	×	Exit Self Refresh → ABI	
	L	H	L	H	H	H	×	Exit Self Refresh → ABI	
	L	H	L	H	H	L	×	ILLEGAL	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	NOP (Continue power down mode)	
All Banks Idle (ABI)	H	H	×	×	×	×	×	Refer to Truth Table	6
	H	L	H	×	×	×	×	Enter Power Down	6
	H	L	L	H	H	H	×	Enter Power Down	6
	H	L	L	H	H	L	×	ILLEGAL	6
	H	L	L	H	L	×	×	ILLEGAL	6
	H	L	L	L	H	L	×	ILLEGAL	6
	H	L	L	L	L	H	×	Enter Self Refresh	6
	H	L	L	L	L	L	×	ILLEGAL	6
	L	L	×	×	×	×	×	NOP	6
Any State Other than Listed Above	H	H	×	×	×	×	×	Refer to Truth Table	
	H	L	×	×	×	×	×	Begin Clock Suspend Next Cycle	
	L	H	×	×	×	×	×	Enable Clock of Next Cycle	
	L	L	×	×	×	×	×	Continue Clock Suspension	

Note: 6. Power-down and self refresh can be entered only when all the banks are in an idle state.

Mode Set Address Keys

Operation Code			$\overline{CAS}$ Latency				Burst Type		Burst Length				
A8	A7	TM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Setting	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vender	0	0	1	Reserved	1	Interleave	0	0	1	2	Reserved
1	0	Use	0	1	0	2			0	1	0	4	4
1	1	Only	0	1	1	3			0	1	1	8	8
Write Burst Length *Note 1			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9		Length	1	0	1	Reserved			1	0	1	Reserved	Reserved
0		Burst	1	1	0	Reserved			1	1	0	Special page	Reserved
1		Single Bit	1	1	1	Reserved			1	1	1	Full Page	Reserved

*Note 1: To select Special Page mode, set A9 to “L”.
The write burst length during Special Page mode is set only for Burst.

POWER ON SEQUENCE

1. With CKE = "H", DQM = "H" and the other inputs in NOP state, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 μs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply an Auto-refresh 8 or more times.
5. Enter the mode register command.

Burst Length and Sequence

BL = 2

Starting Address (column address A0, binary)	Sequential Type	Interleave Type
0	0, 1	Not supported
1	1, 0	Not supported

BL = 4

Starting Address (column address A1, A0, binary)	Sequential Type	Interleave Type
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

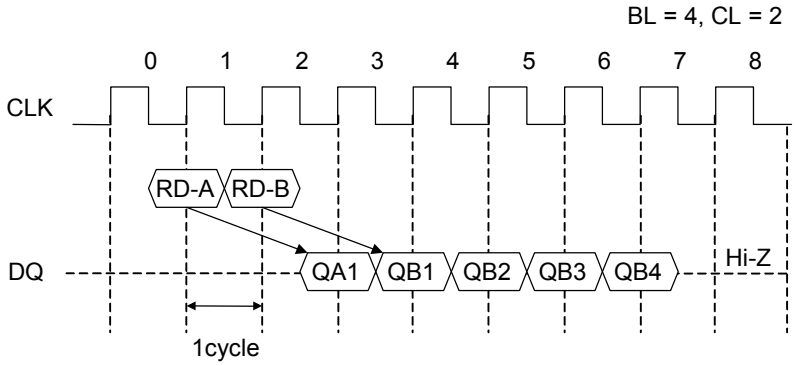
BL = 8

Starting Address (column address A2 - A0, binary)	Sequential Type	Interleave Type
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

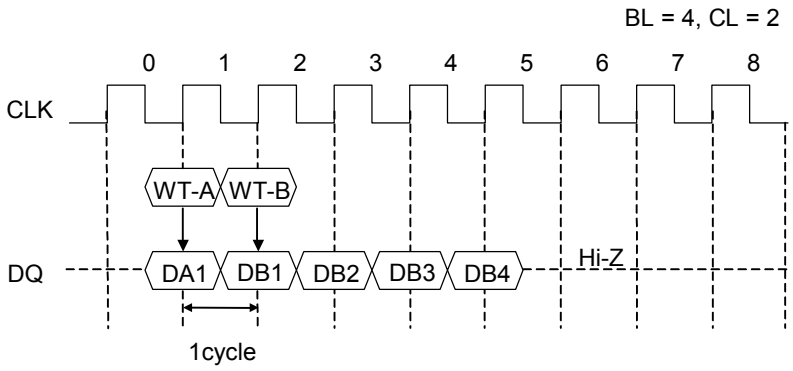
BL = Special, Full : Sequential only

READ/WRITE COMMAND INTERVAL

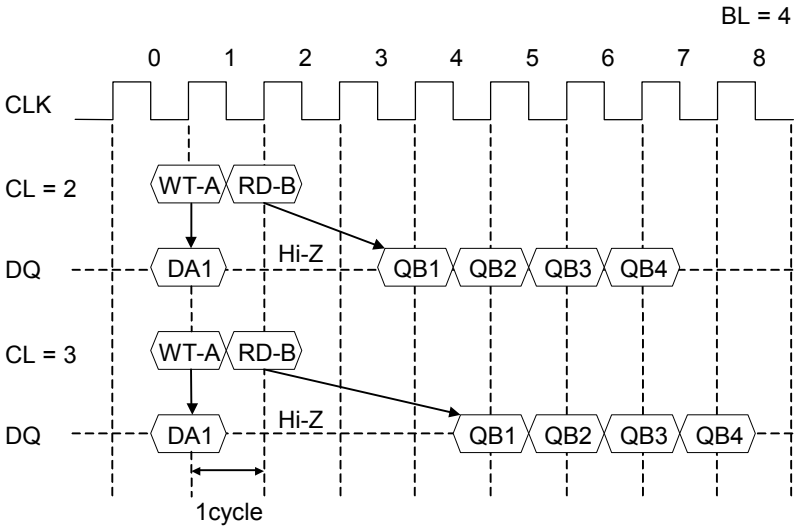
Read to Read Command Interval



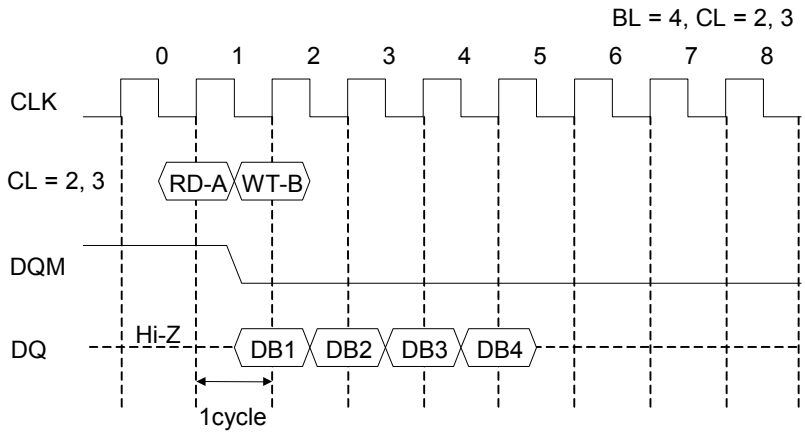
Write to Write Command Interval

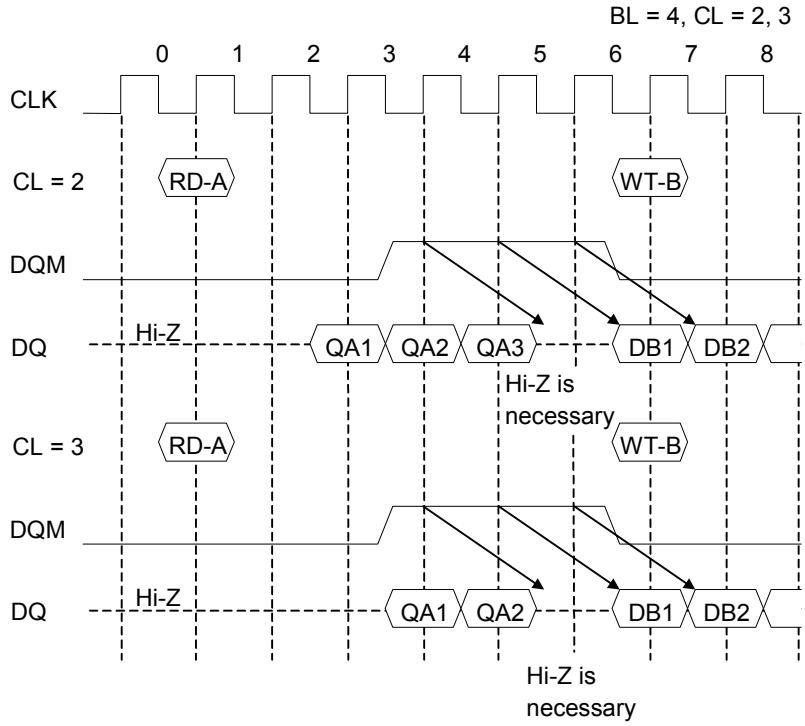


Write to Read Command Interval



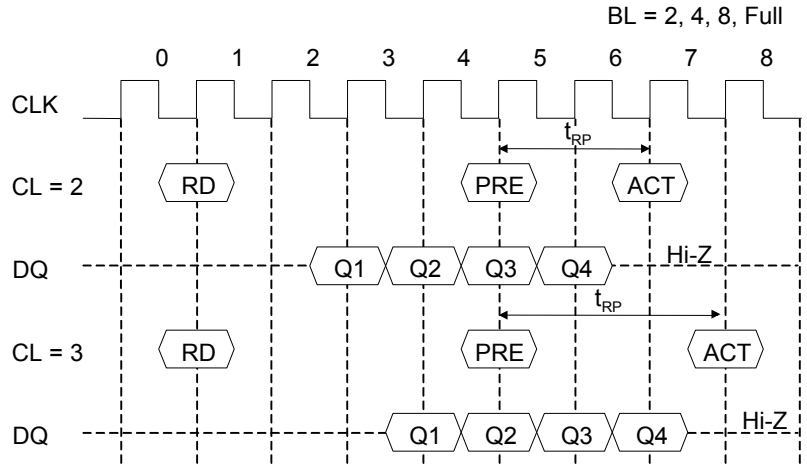
Read to Write Command Interval



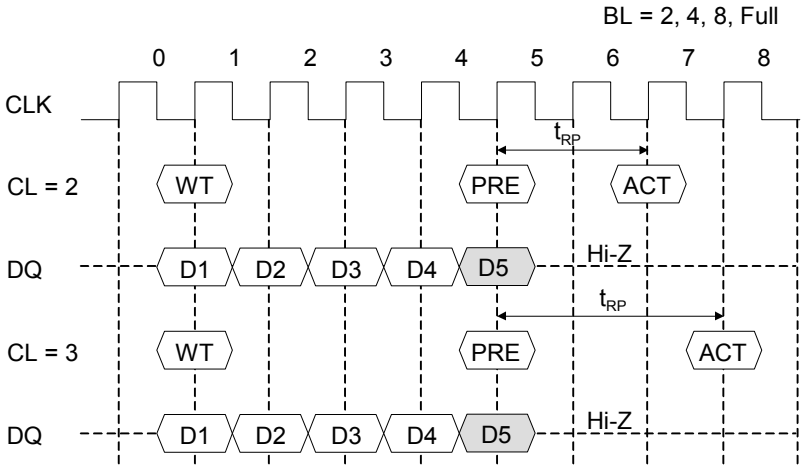


BURST TERMINATION

Burst Read Termination by Precharging in READ Cycle

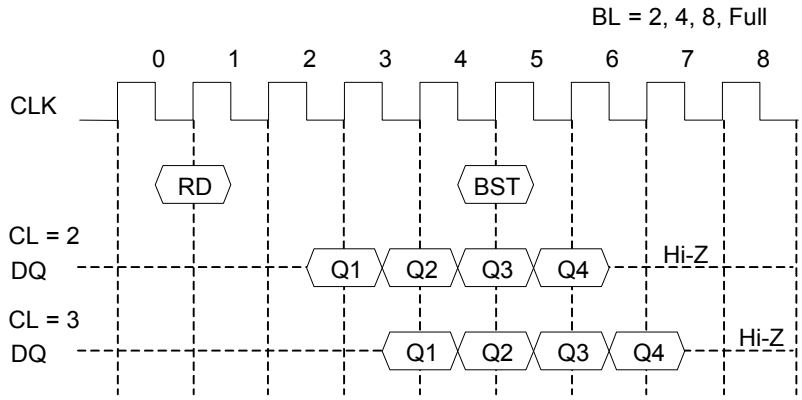


Burst Read Termination by Precharging in WRITE Cycle

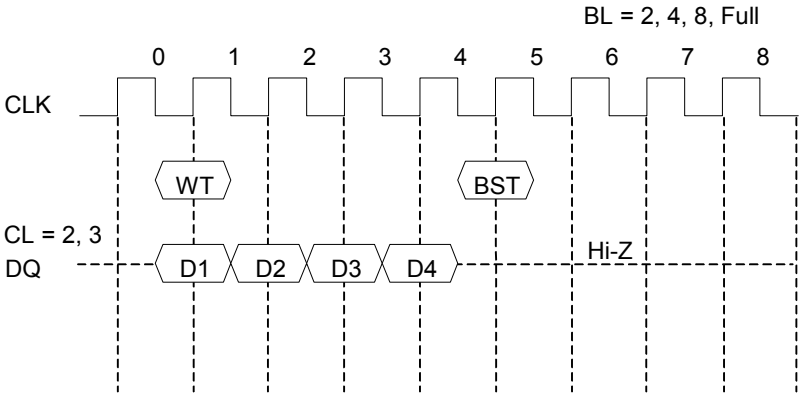


Note: D5 data will not be written

Read Burst Stop Command

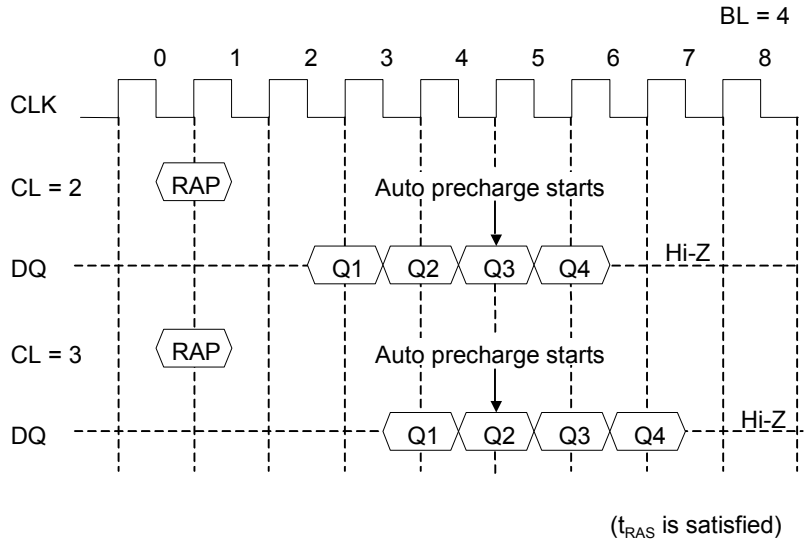


Write Burst Stop Command



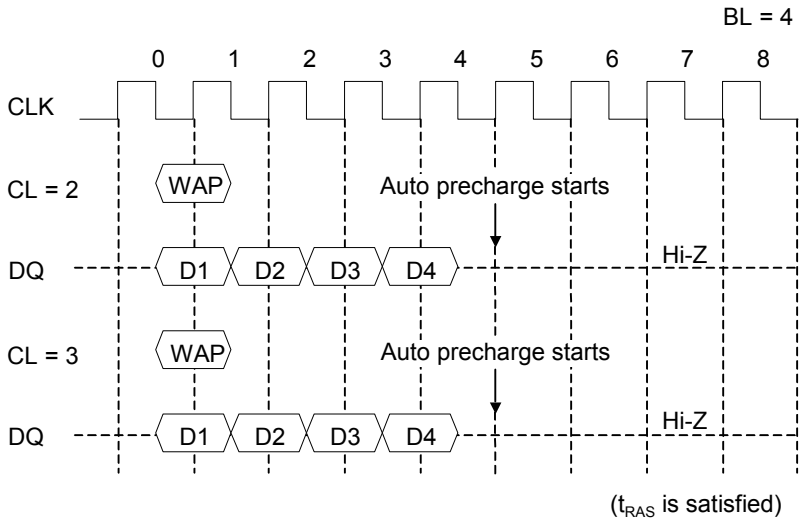
AUTO PRECHARGE

Read with Auto Precharge



(t_{RAS} is satisfied)

Write with Auto Precharge



(t_{RAS} is satisfied)

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Power Supply Pin Relative to GND	V_{CC}	–0.5 to 4.6	V
Voltage on Input Pin Relative to GND	V_{IN}, V_{OUT}	–0.5 to V_{CC} + 0.5 ≤ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25 °C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Capacitance

(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A10, BA)	C_{IN1}	—	5	pF
Input Capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ DQM 0 – DQM3)	C_{IN2}	—	5	pF
Output Capacitance (DQ0 – DQ31)	C_{OUT}	—	6	pF

DC Characteristics

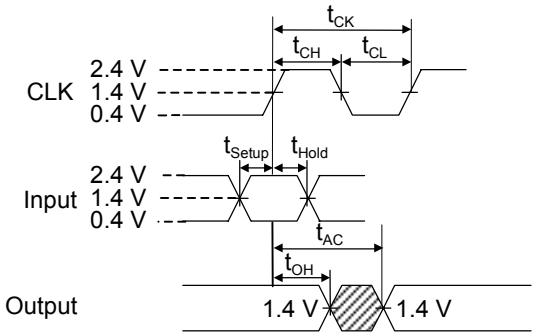
Parameter	Symbol	Test Condition		MS82V32520-75		MS82V32520-8		MS82V32520-10		Unit	Note
		CKE	Other	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	—	I_{OH}= –2.0 mA	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	—	I_{OL}= 2.0 mA	—	0.4	—	0.4	—	0.4	V	
Input Leakage Current	I_{LI}	—	—	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	—	—	–10	10	–10	10	–10	10	µA	
Operating Current (1 Bank)	I_{CC1}	CKE ≥ V_{IH}	t_{CK} = t_{CK} min. t_{RC} = t_{RC} min. No Burst	—	200	—	190	—	180	mA	1, 2
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}	t_{CK} = t_{CK} min.	—	2	—	2	—	2	mA	3
	I_{CC2PS}	CKE ≤ V_{IL}	CLK ≤ V_{IL} t_{CK} = ∞	—	2	—	2	—	2	mA	2
Precharge Standby Current in Non Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}	$\overline{CS}$ ≥ V_{IH} t_{CK} = t_{CK} min.	—	40	—	40	—	40	mA	2
	I_{CC2NS}	CKE ≥ V_{IH}	CLK ≤ V_{IL} t_{CK} = ∞	—	20	—	20	—	20	mA	
Active Standby Current in Power Down Mode	I_{CC3P}	CKE ≤ V_{IL}	t_{CK} = t_{CK} min.	—	3	—	3	—	3	mA	3
	I_{CC3PS}	CKE ≤ V_{IL}	CLK ≤ V_{IL} t_{CK} = ∞	—	3	—	3	—	3	mA	3
Active Standby Current in Non Power Down Mode	I_{CC3N}	CKE ≥ V_{IH}	$\overline{CS}$ ≥ V_{IH} t_{CK} = t_{CK} min.	—	50	—	50	—	50	mA	3
	I_{CC3NS}	CKE ≥ V_{IH}	CLK ≤ V_{IL} t_{CK} = ∞	—	30	—	30	—	30	mA	3
Operating Current (Burst Mode)	I_{CC4}	CKE ≥ V_{IH}	t_{CK} = t_{CK} min.	—	240	—	220	—	200	mA	2
Refresh Current	I_{CC5}	CKE ≥ V_{IH}	t_{RC} ≥ t_{RC} min.	—	200	—	190	—	180	mA	
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	—	—	3	—	3	—	3	mA	

Notes 1. The maximum value of power supply current is obtained with the output open.
2. Address and data are changed only one time during one cycle.
3. Address and data are changed only one time during two cycles.

AC Characteristics

Test conditions

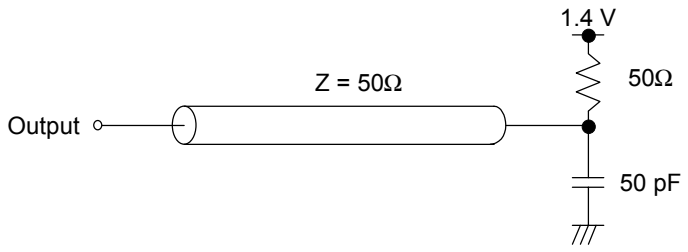
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX)}$.
- An access time is measured at 1.4 V.
- Input levels at the AC testing are 2.4 V/0.4 V.



Synchronous Characteristics

Parameter		Symbol	MS82V32520-75		MS82V32520-8		MS82V32520-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK3}	7.5	—	8	—	10	—	ns	
	$\overline{CAS}$ Latency = 2	t_{CK2}	12	—	12	—	15	—	ns	
Access Time from CLK	$\overline{CAS}$ Latency = 3	t_{AC3}	—	5.5	—	6	—	7	ns	1
	$\overline{CAS}$ Latency = 2	t_{AC2}	—	8	—	8	—	9	ns	1
CLK High Level Width		t_{CH}	3	—	3	—	3.5	—	ns	
CLK Low Level Width		t_{CL}	3	—	3	—	3.5	—	ns	
Data-out Hold Time		t_{OH}	2.5	—	2.5	—	2.5	—	ns	
Data-out Low-impedance Time		t_{LZ}	0	—	0	—	0	—	ns	
Data-out High-impedance Time		t_{HZ}	—	5.5	—	6	—	7	ns	
Data-in Setup Time		t_{DS}	2.5	—	2.5	—	2.5	—	ns	
Data-in Hold Time		t_{DH}	1	—	1	—	1	—	ns	
Address Setup Time		t_{AS}	2.5	—	2.5	—	2.5	—	ns	
Address Hold Time		t_{AH}	1	—	1	—	1	—	ns	
CKE Setup Time		t_{CKS}	2.5	—	2.5	—	2.5	—	ns	
CKE Hold Time		t_{CKH}	1	—	1	—	1	—	ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) Setup Time		t_{CMS}	2.5	—	2.5	—	2.5	—	ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) Hold Time		t_{CMH}	1	—	1	—	1	—	ns	

Note 1. Output load.

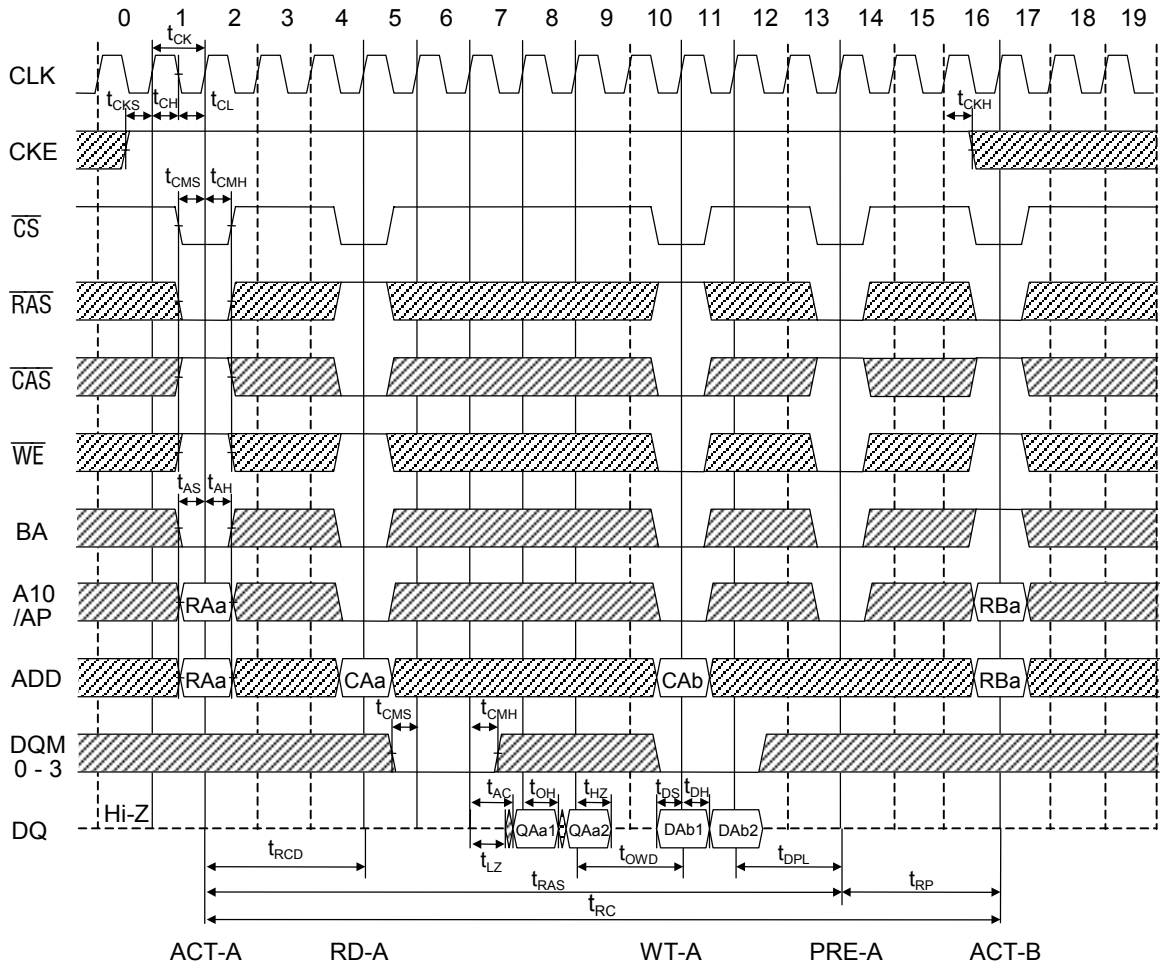


Asynchronous Characteristics

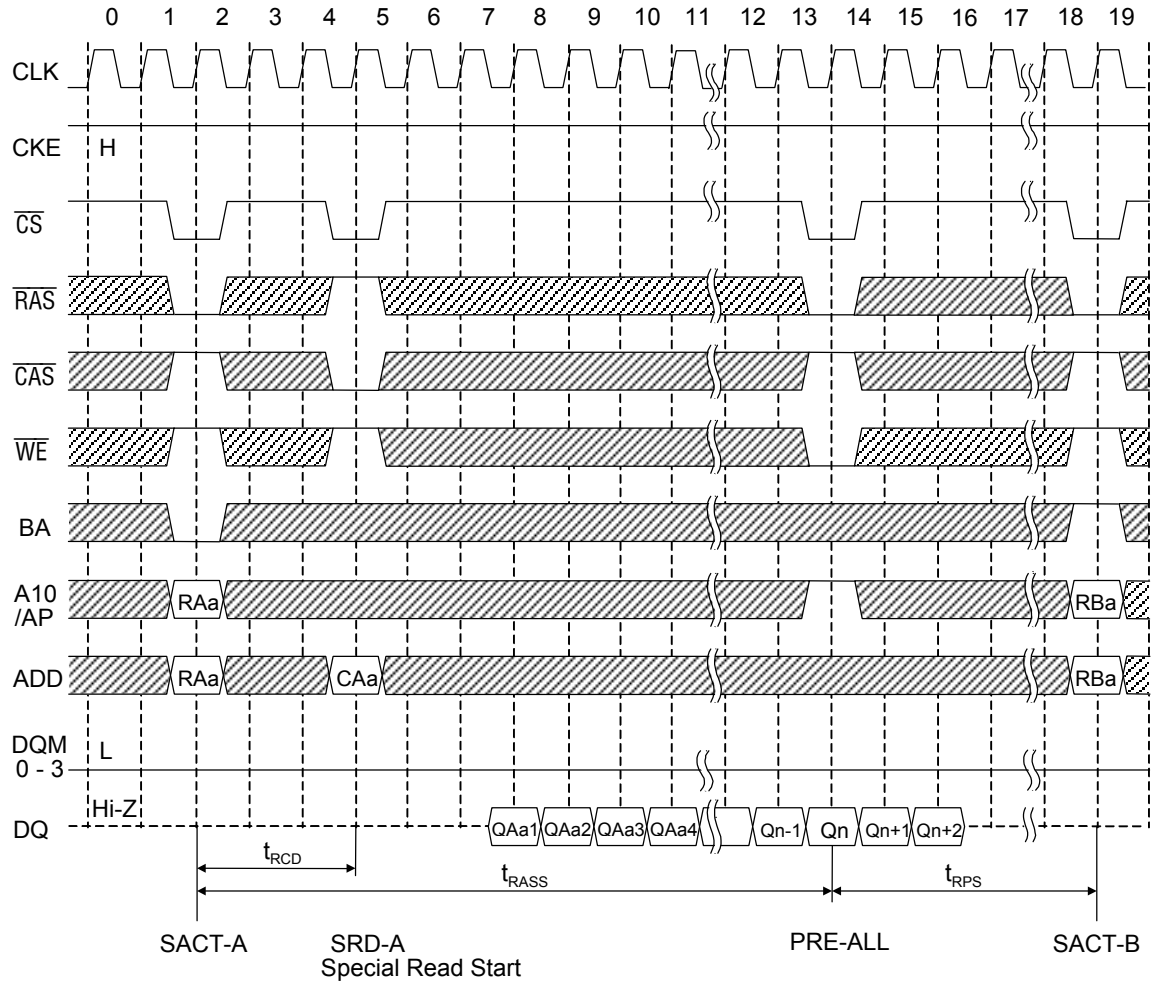
Parameter	Symbol	MS82V32520-75		MS82V32520-8		MS82V32520-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
REF to REF/ACT/SACT Command Period	t_{RC}	67.5	—	72	—	90	—	ns	
ACT to PRE Command Period	t_{RAS}	45	120k	48	120k	60	120k	ns	
SACT to PRE Command Period	t_{RASS}	6	—	6	—	6	—	CLK	
PRE to ACT Command Period	t_{RP}	22.5	—	24	—	30	—	ns	
PRE-ALL (Special Page) to SACT Command Period	t_{RPS}	9	—	9	—	9	—	CLK	
Delay Time ACT/SACT to READ/WRITE Command	t_{RCD}	22.5	—	24	—	30	—	ns	
ACT (0) to ACT (1) Command Period	t_{RRD}	15	—	16	—	20	—	ns	
READ/WRITE to READ/WRITE Command Period	t_{CCD}	7.5	—	8	—	10	—	ns	
Data-in to PRE Command Period	t_{DPL}	7.5	—	8	—	10	—	ns	
Data Output to WRITE Command Input Time	t_{OWD}	15	—	16	—	20	—	ns	
Mode Register Set Cycle Time	t_{RSC}	15	—	16	—	20	—	ns	
Transition Time	t_T	1	30	1	30	1	30	ns	
Refresh Time	t_{REF}	—	64	—	64	—	64	ms	

TIMING WAVEFORM

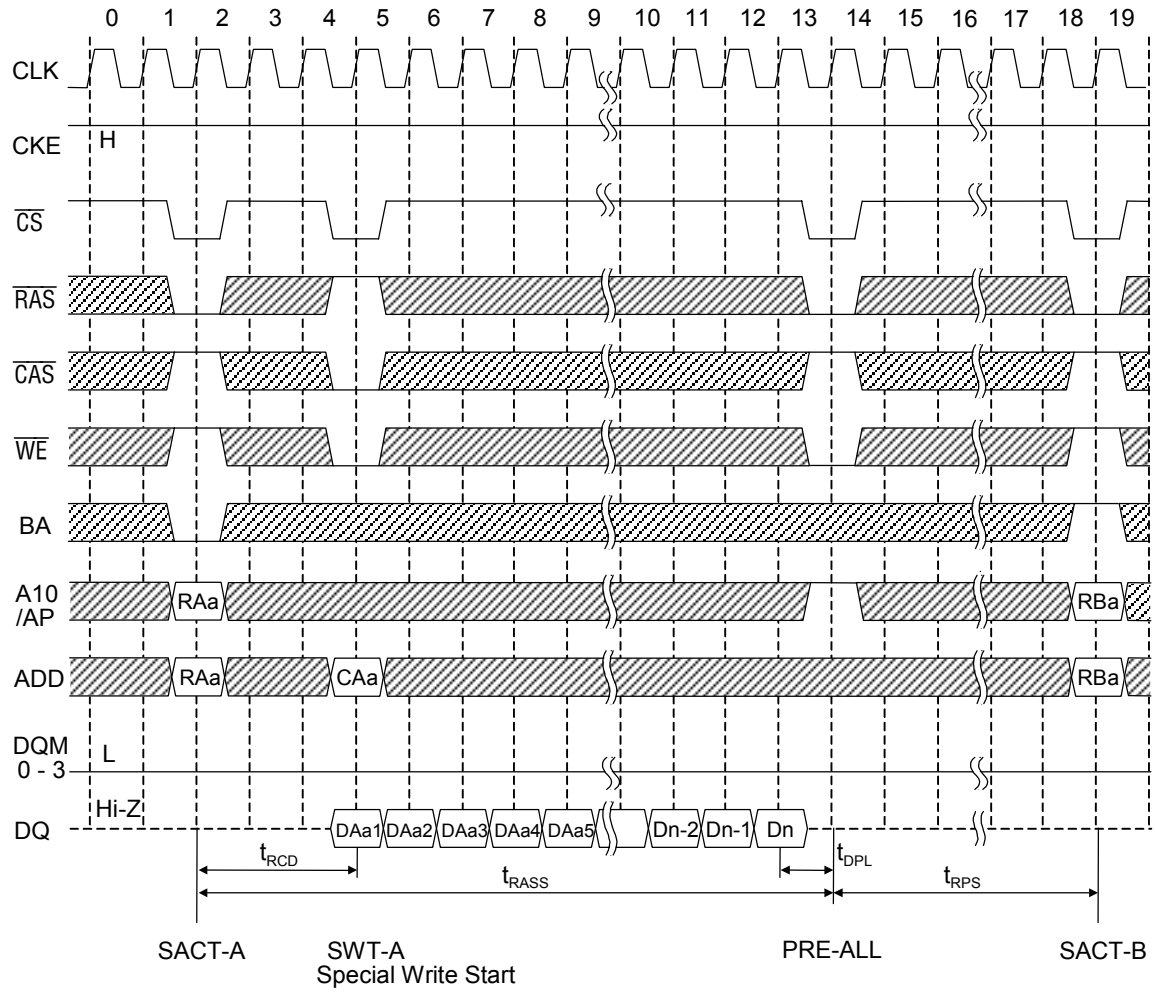
READ/WRITE CYCLE (BL = 2, CL = 3)



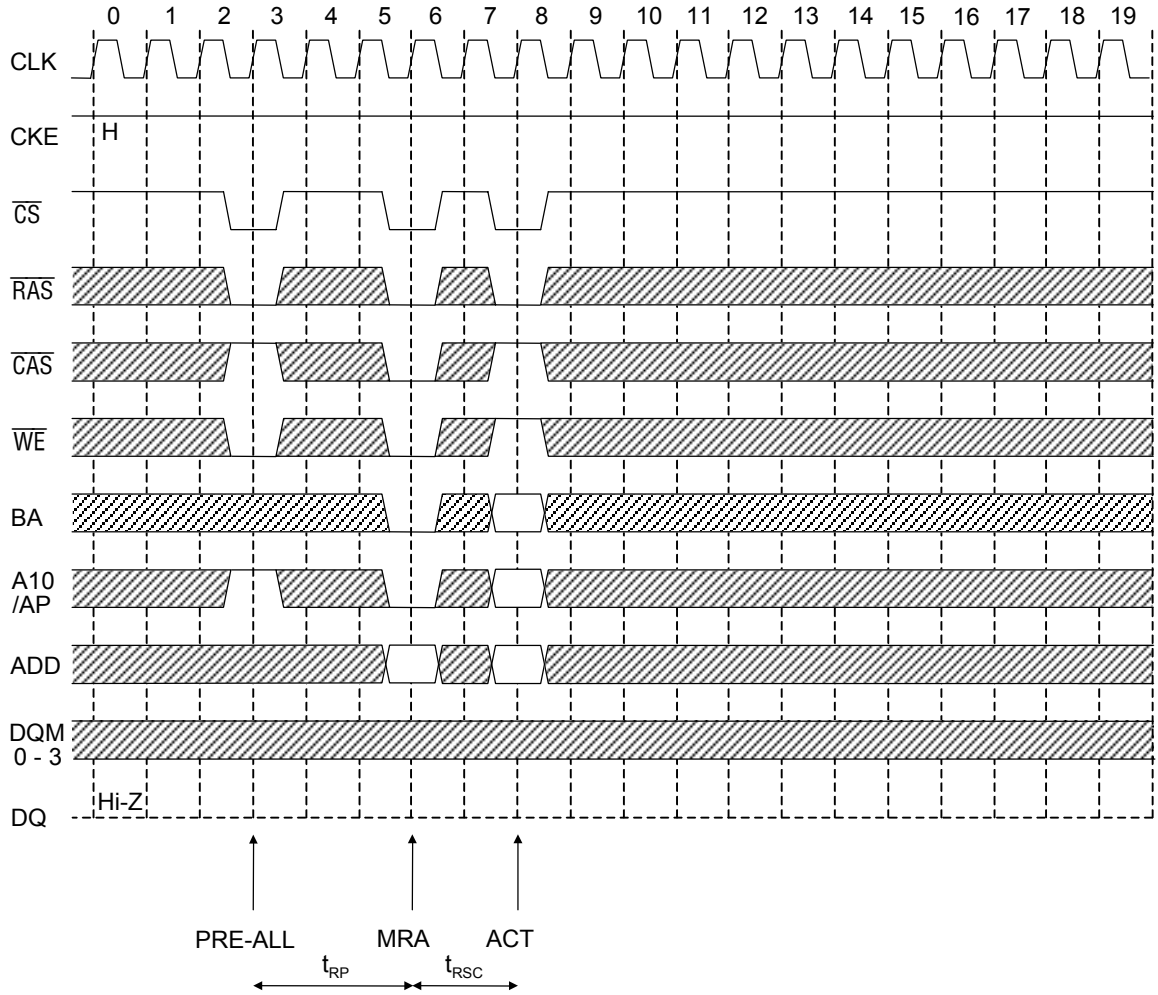
Special READ CYCLE (BL = Special Page, CL = 3)



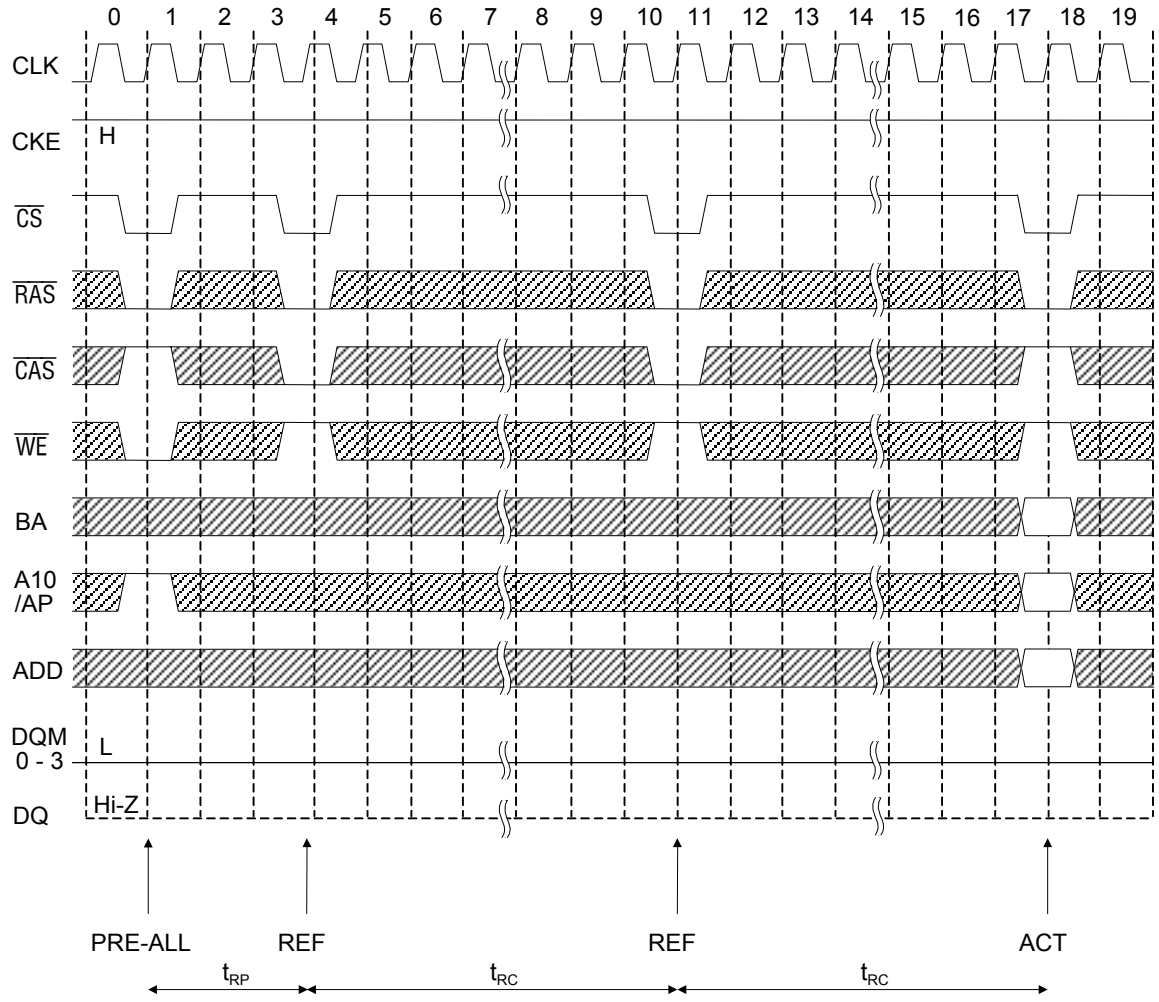
Special WRITE CYCLE (BL = Special Page, CL = 3)



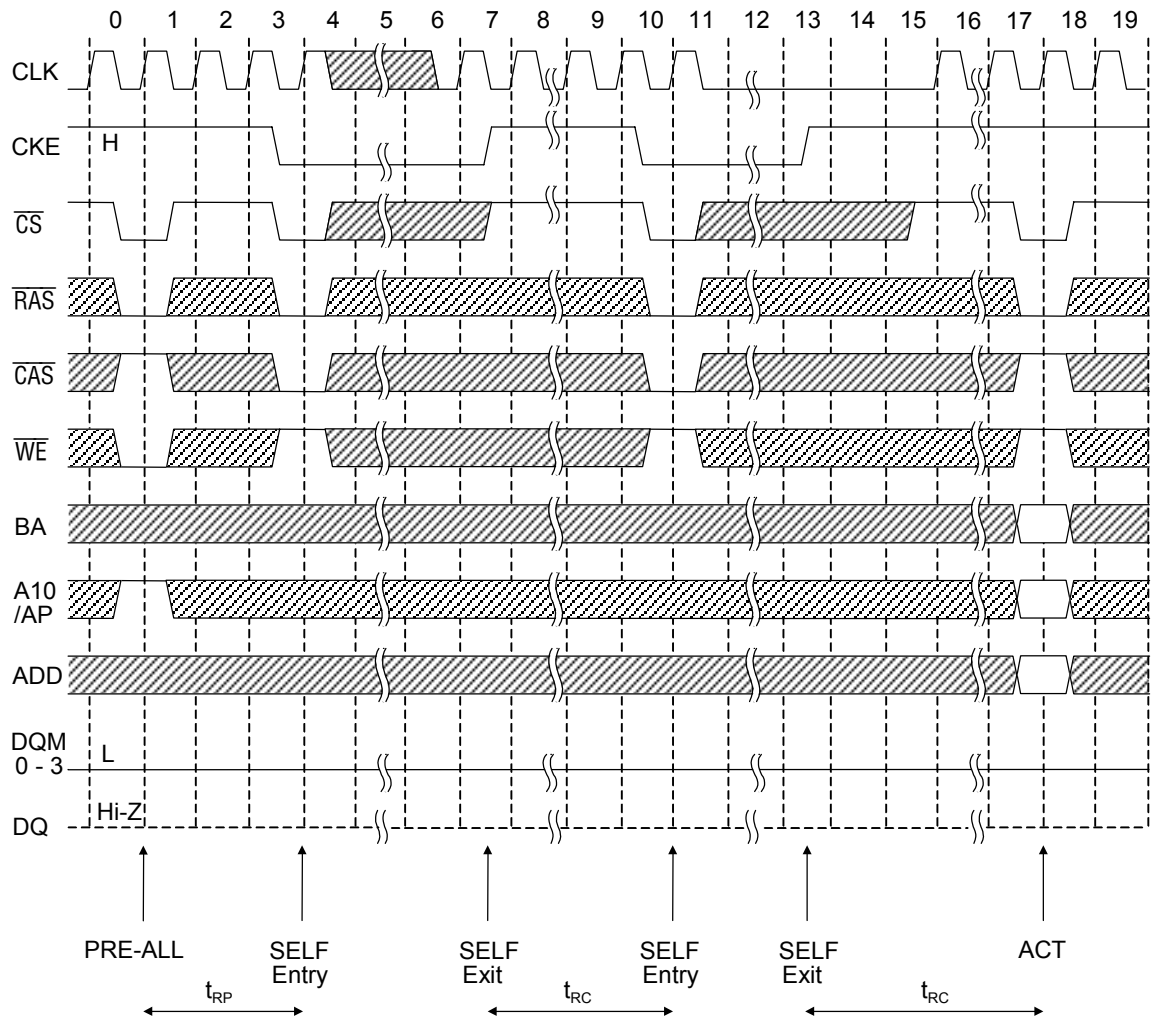
Mode Register Set



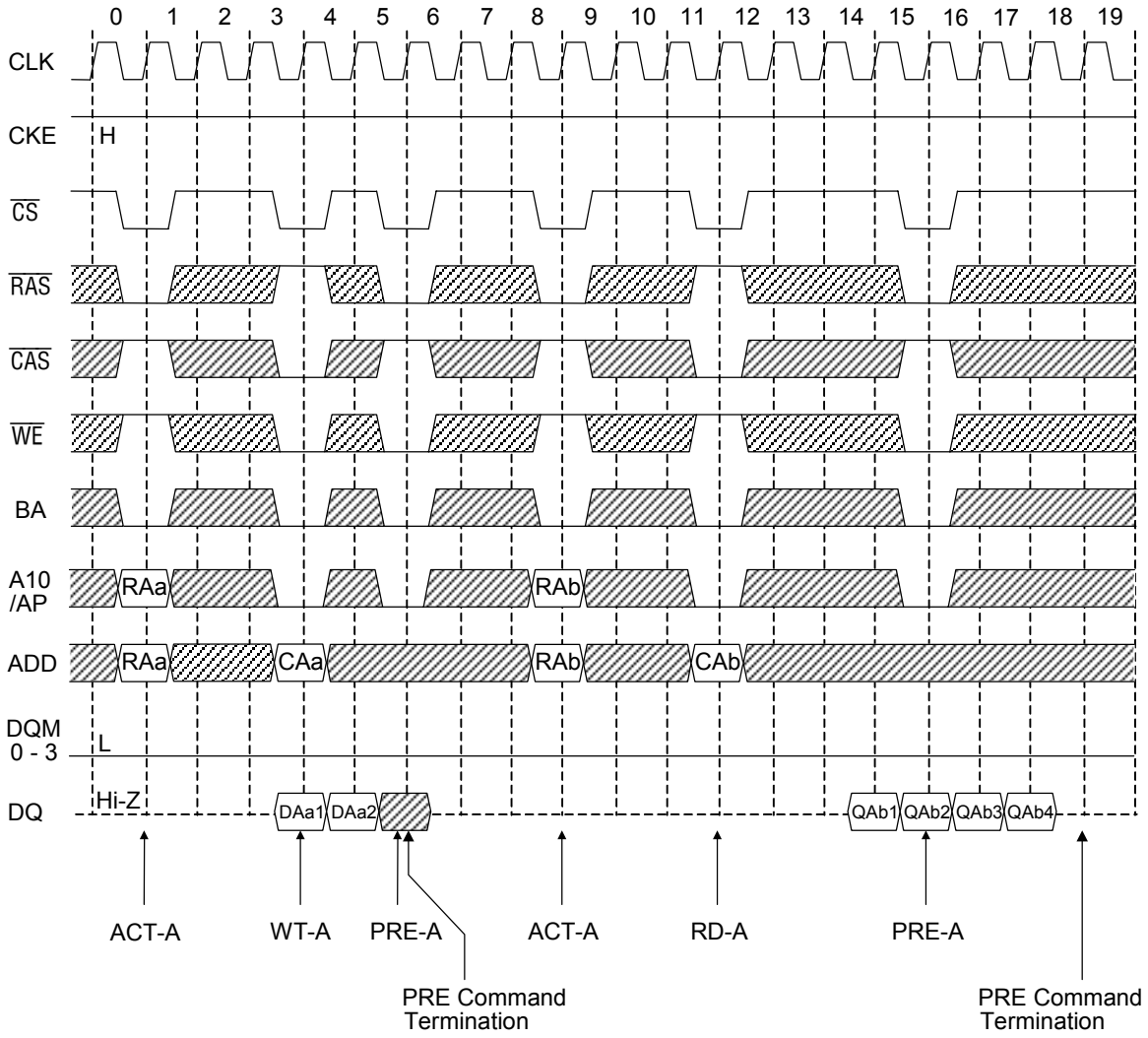
Auto Reflesh



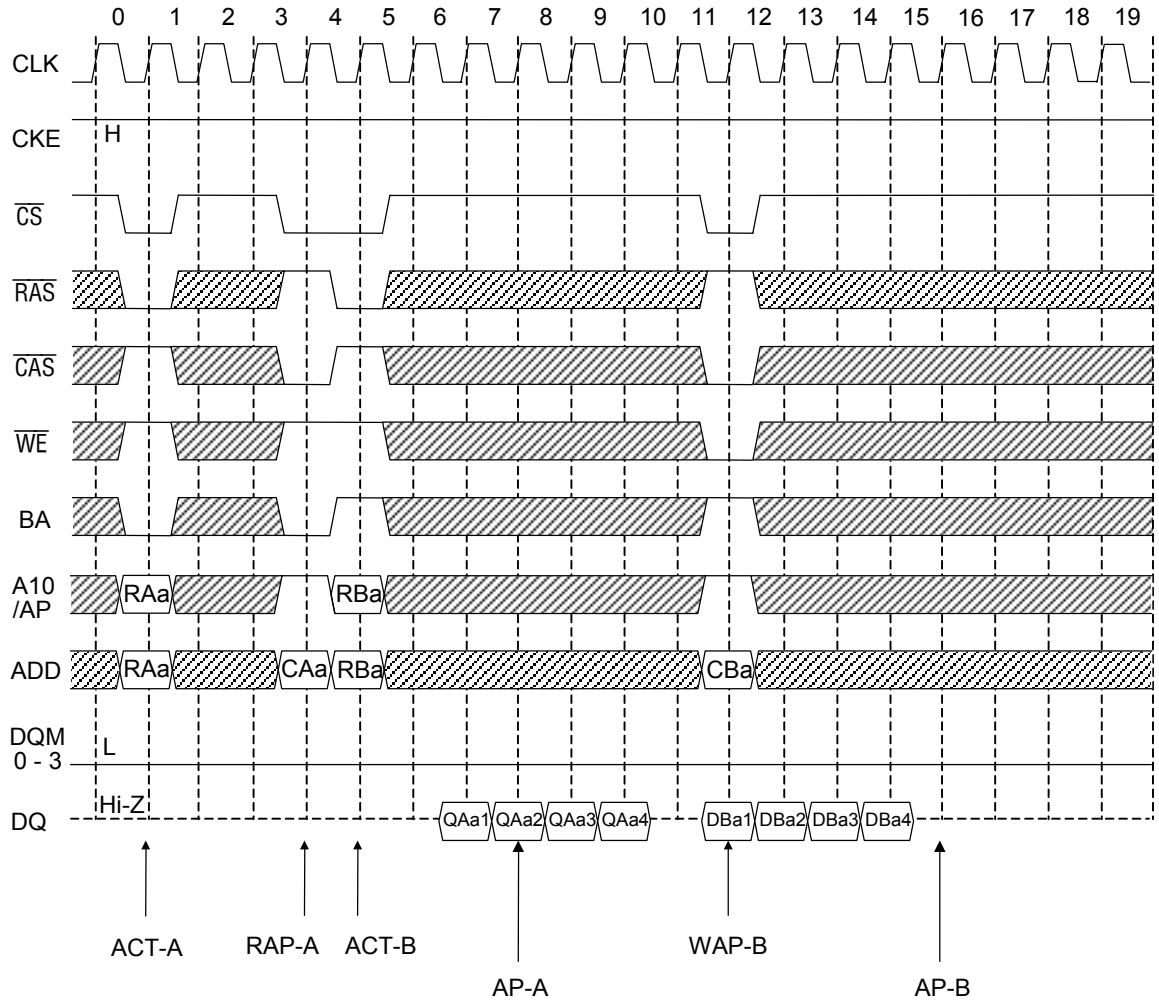
Self Reflesh (Entry and Exit)



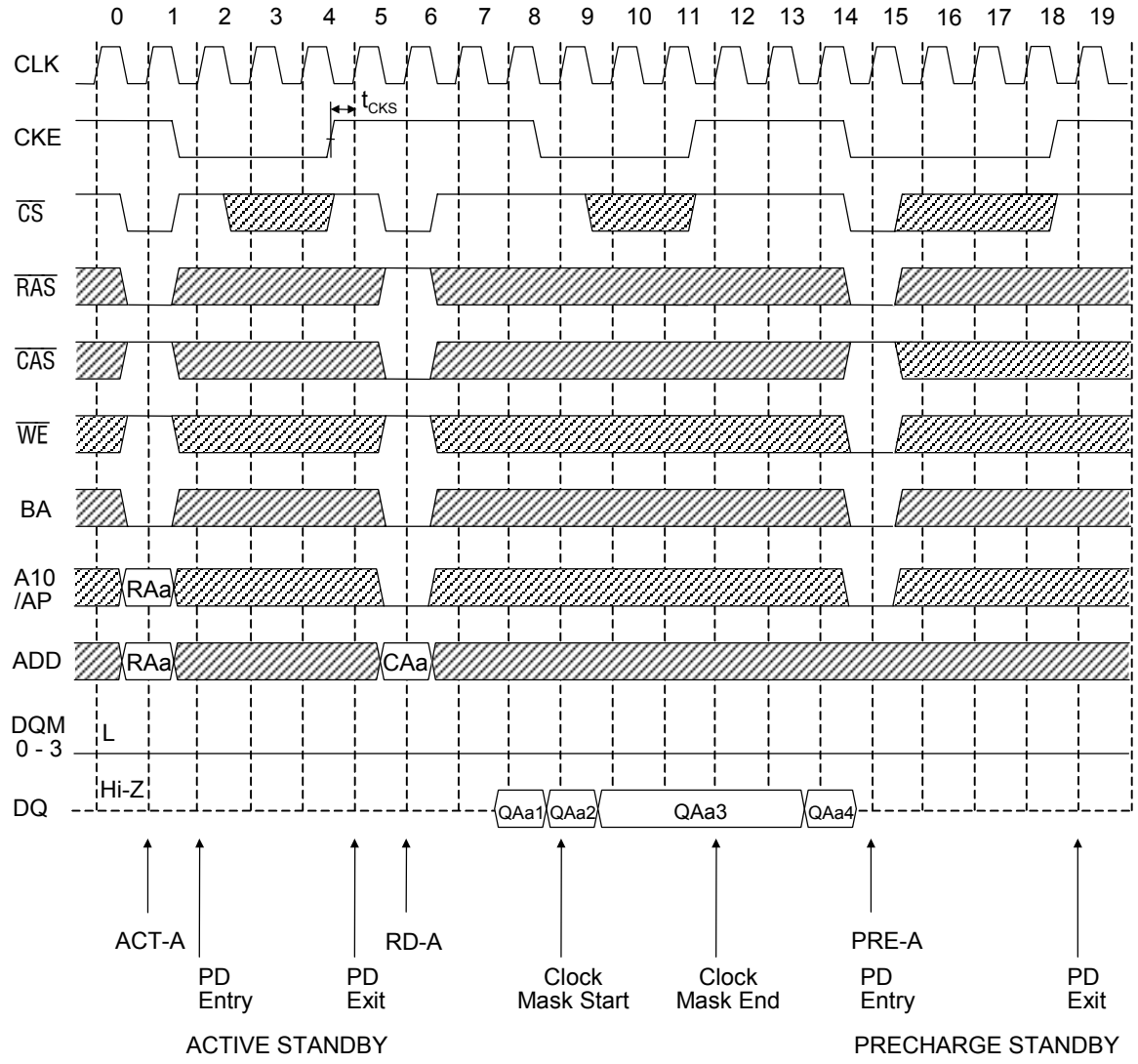
Burst Termination by Precharging (BL = 8, CL = 3)



Auto Precharging (BL = 4, CL = 3)

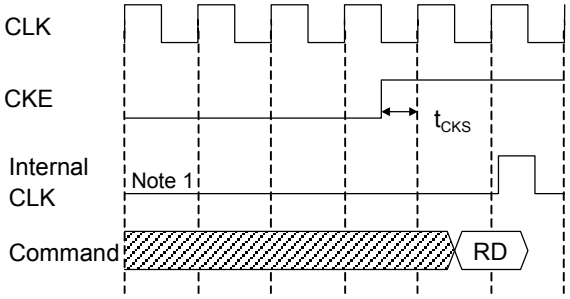


Power Down Mode and Clock Suspension (BL = 4, CL = 2)

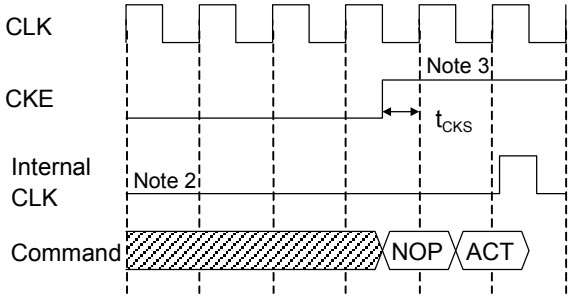


CLOCK Suspend Exit & Power Down Exit

1) Clock Suspend (= Active Power Down) Exit

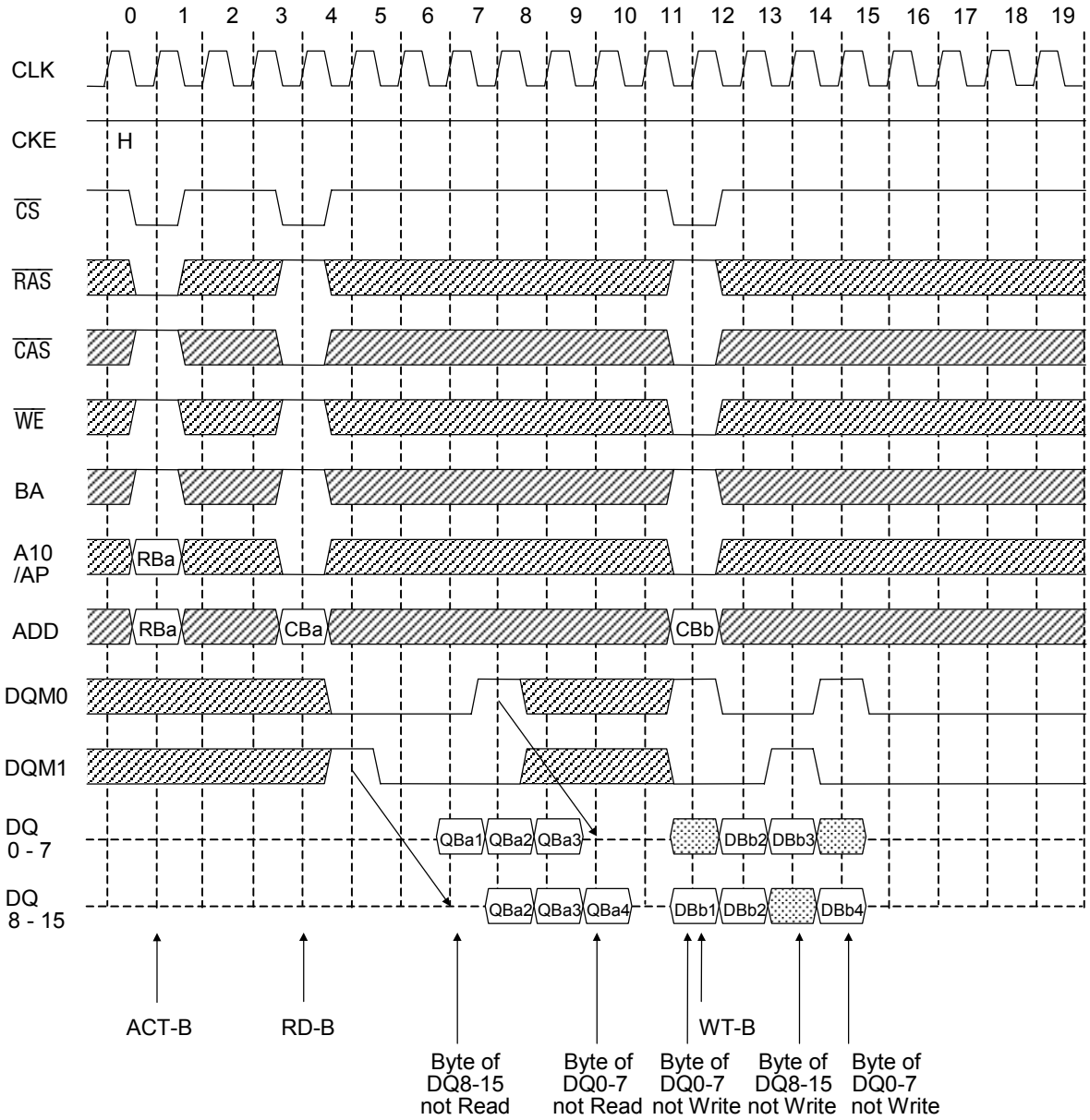


2) Power Down (= Precharge Power Down) Exit

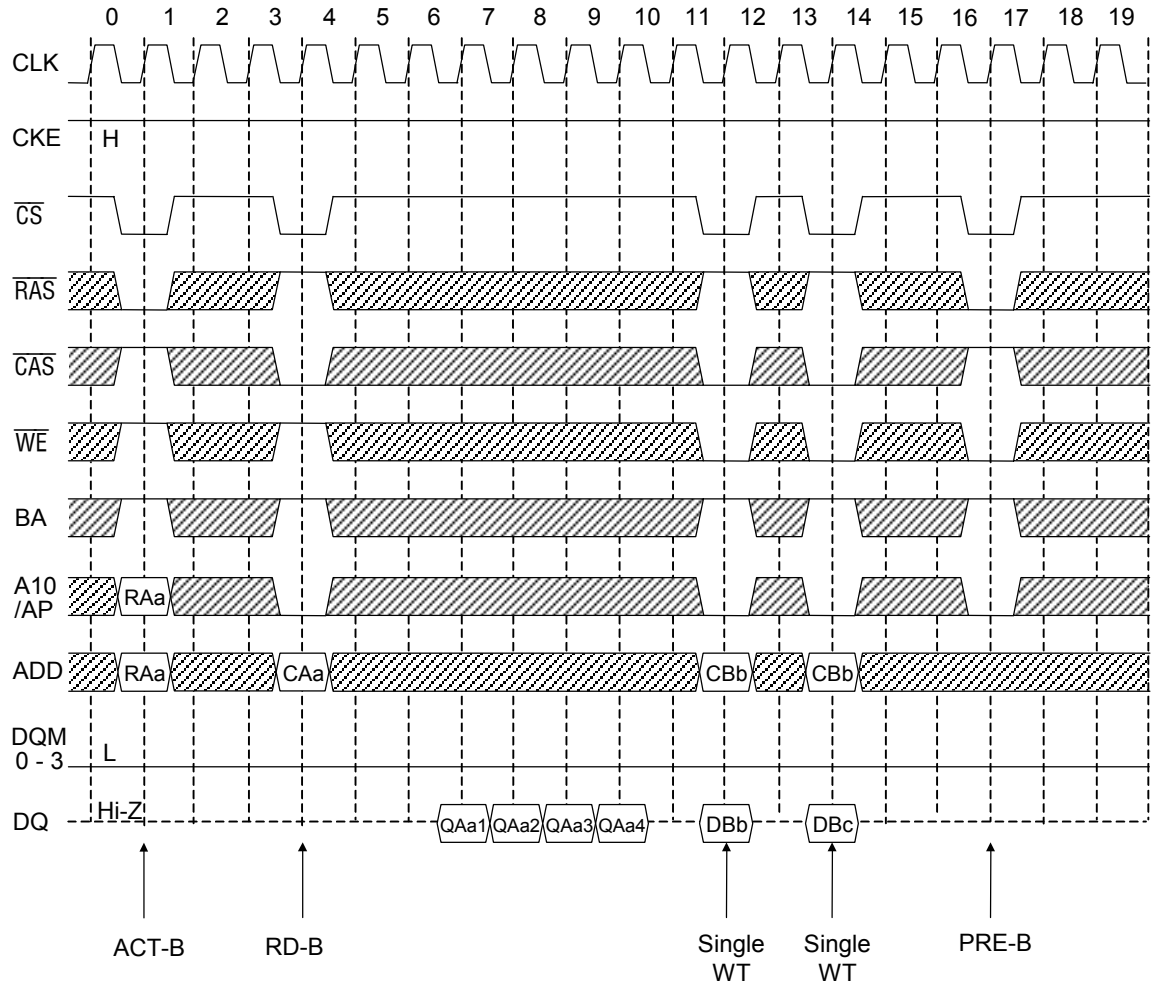


Notes: 1. Active power down: one or both bank active state.
2. Precharge power down: both bank precharge state.
3. NOP should be issued. And new command can be issued after 1 Clock.

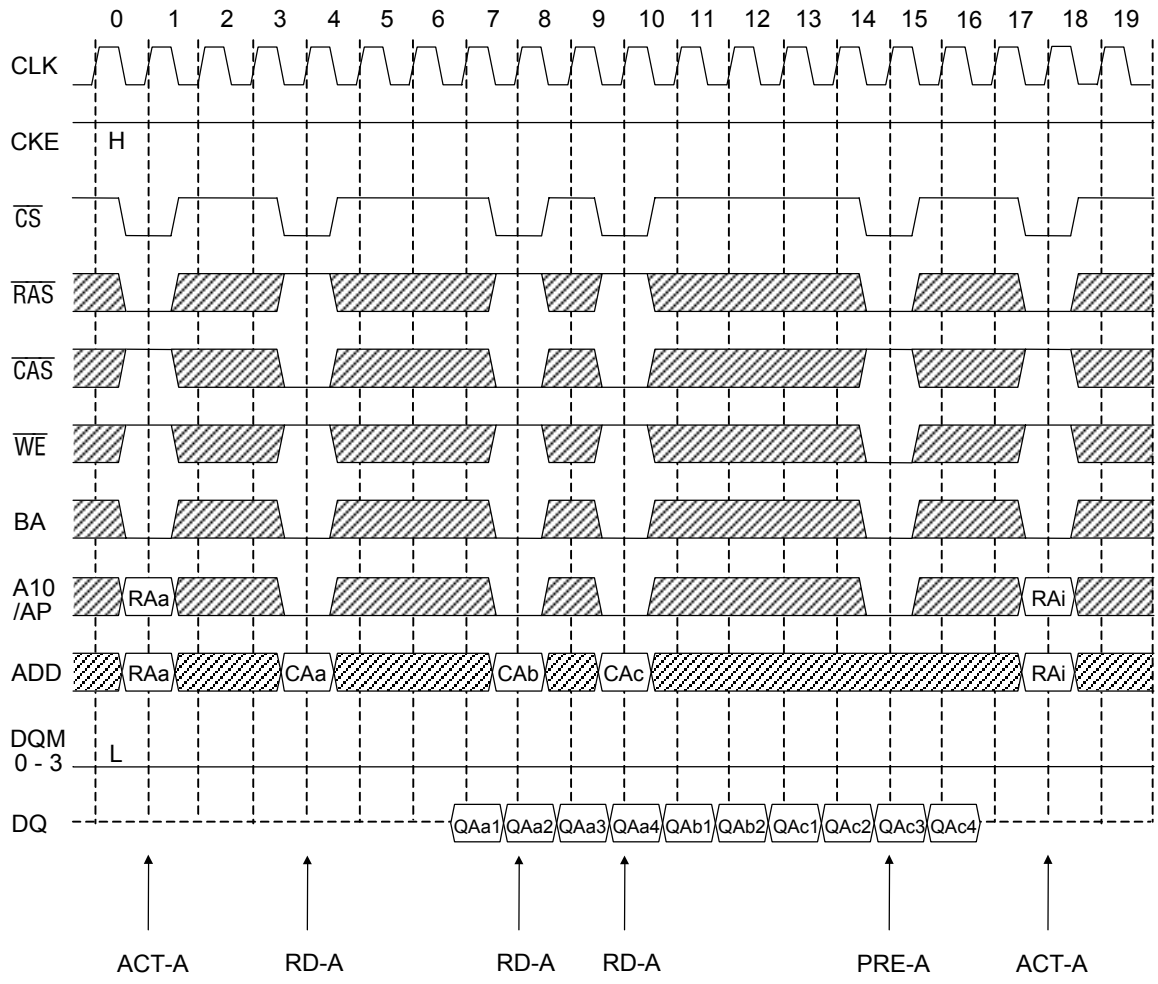
Byte Read/Write Operation (by DQM) (BL = 4, CL = 3)



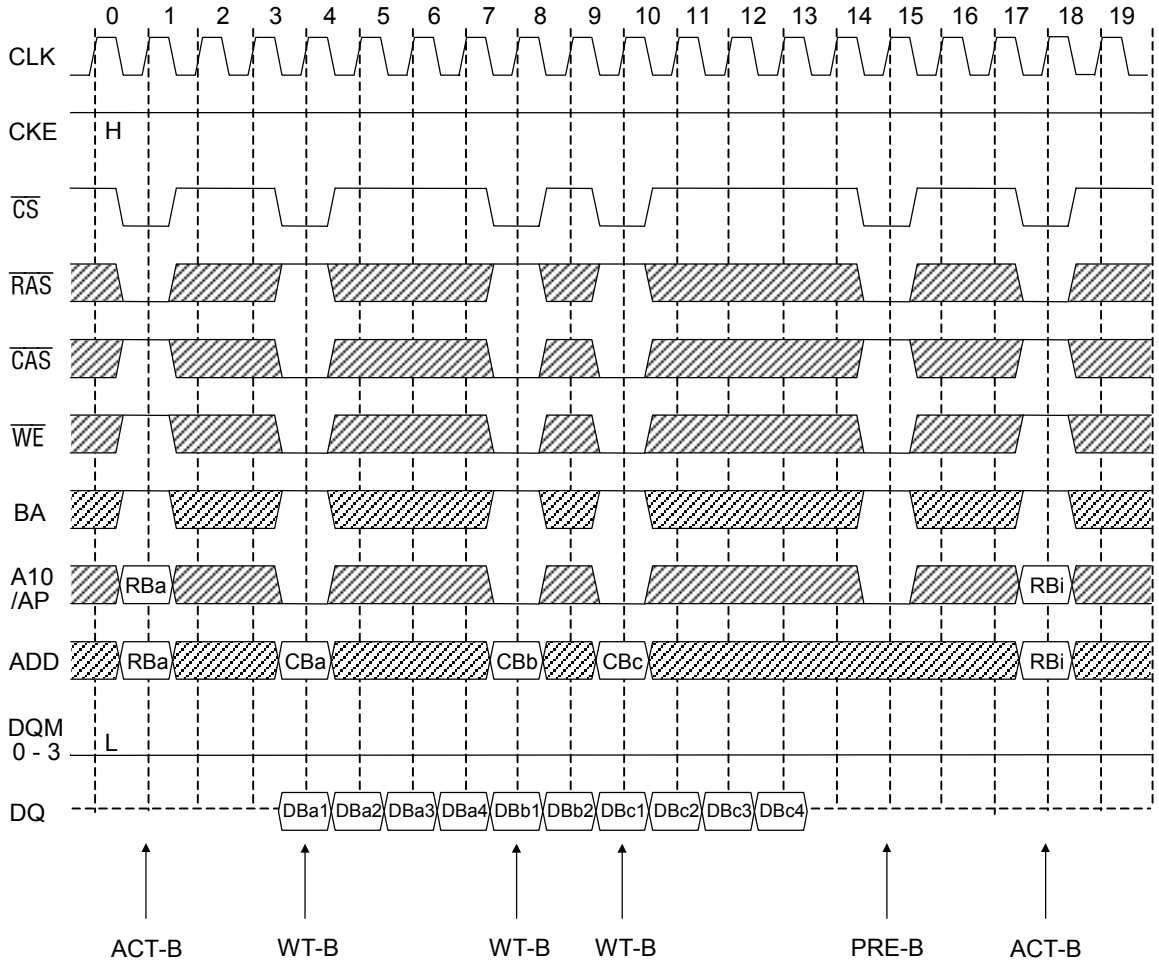
Burst Read and Single Write (BL = 4, CL = 3)



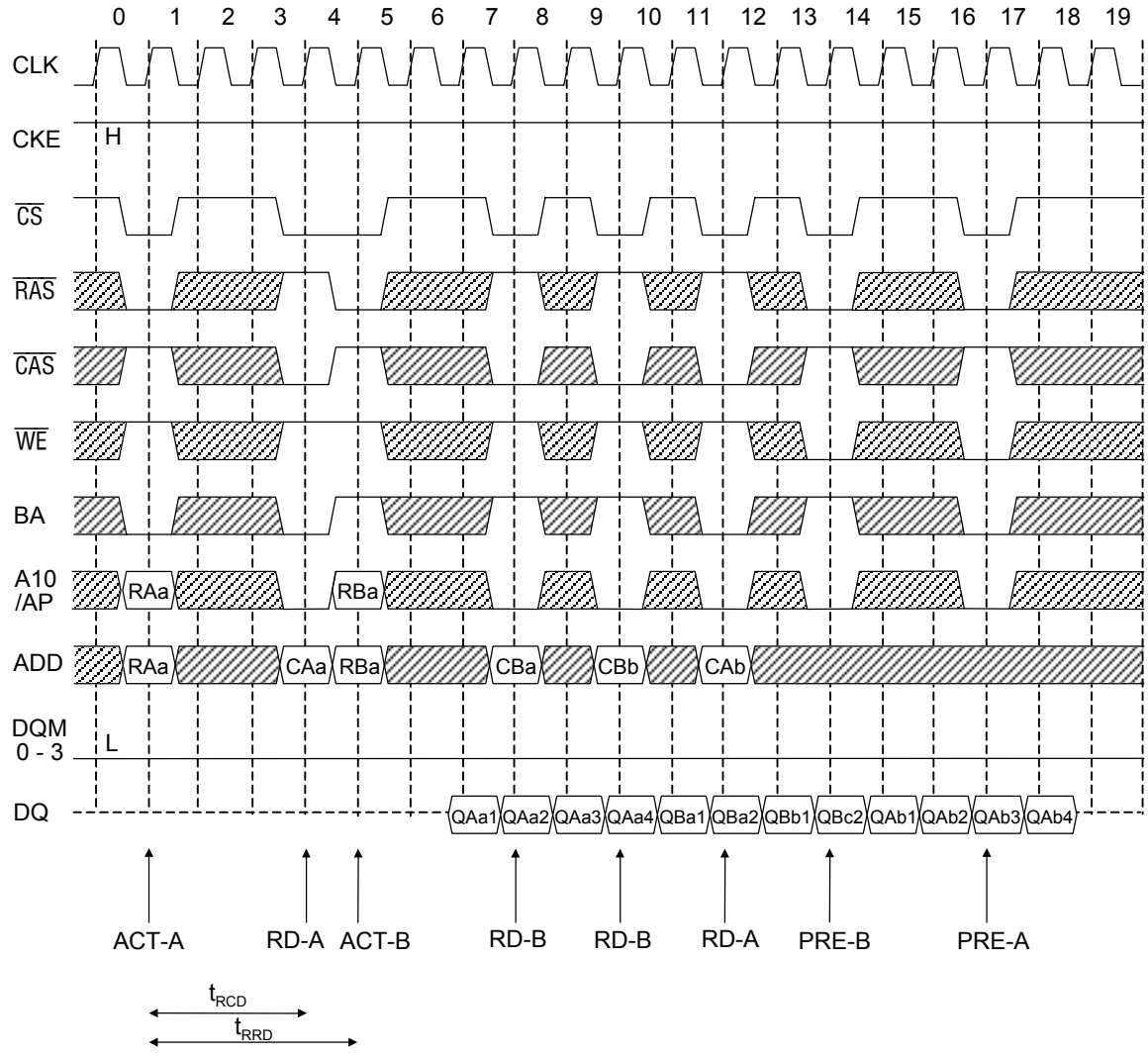
Random Column Read (Continuous Read of Same Bank) (BL = 4, CL = 3)



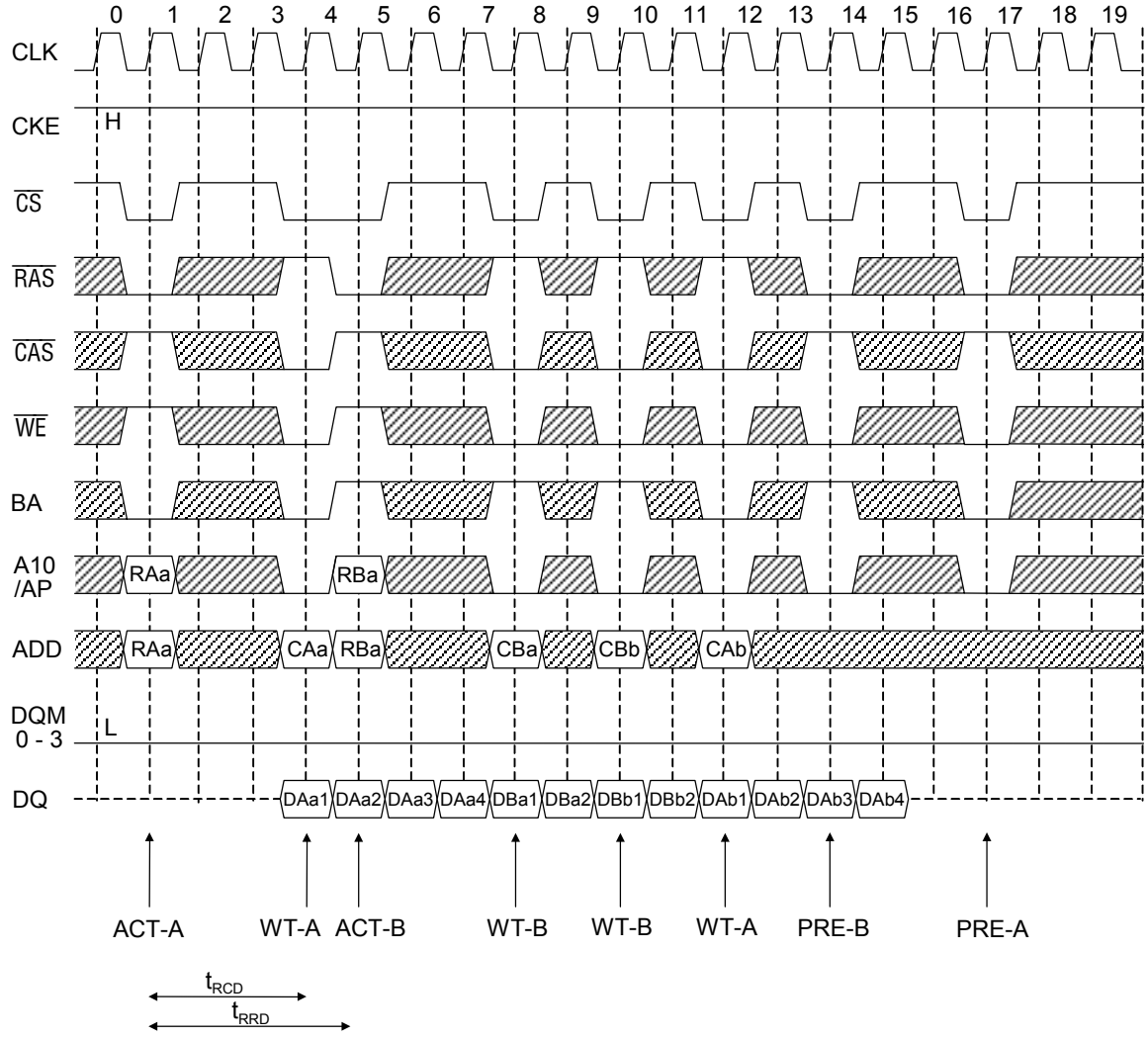
Random Column Write (Continuous Write of Same Bank) (BL = 4, CL = 3)



Interleaved Column Read (BL = 4, CL = 3)



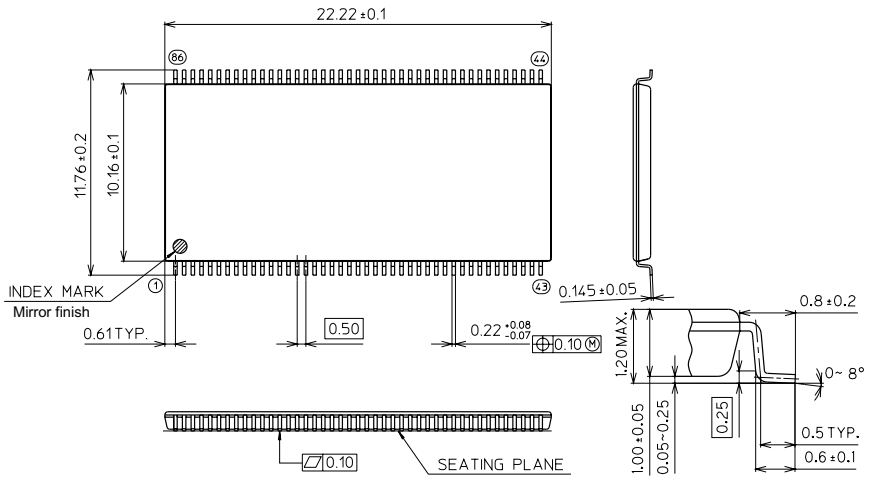
Interleaved Column Write (BL = 4, CL = 3)



PACKAGE DIMENSIONS

(Unit: mm)

TSOP(2)86-P-400-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.53 TYP.
Rev. No./Last Revised	1/Jul. 14, 1998

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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