MSP432P401x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Core
  - ARM® 32-Bit Cortex®-M4F CPU With Floating Point Unit and Memory Protection Unit
  - Frequency up to 48 MHz
  - Performance Benchmark:
    - 1.196 DMIPS/MHz (Dhrystone 2.1)
    - 3.41 CoreMark/MHz
  - Energy Benchmark:
    - 167.4 ULPBench® Score
- Memories
  - Up to 256KB of Flash Main Memory (Simultaneous Read and Execute During Program or Erase)
  - 16KB of Flash Information Memory
  - Up to 64KB of SRAM (Including 8KB of Backup Memory)
  - 32KB of ROM With MSPWare Driver Libraries
- Code Security Features
  - JTAG and SWD Lock
  - IP Protection (Up to Four Secure Flash Zones, Each With Configurable Start Address and Size)
- Operating Characteristics
  - Wide Supply Voltage Range: 1.62 V to 3.7 V
  - Temperature Range (Ambient): –40°C to 85°C
- Ultra-Low-Power Operating Modes
  - Active: 90 µA/MHz
  - Low-Frequency Active: 90 µA (at 128 kHz)
  - LPM3 (With RTC): 850 nA
  - LPM3.5 (With RTC): 800 nA
  - LPM4.5: 25 nA
- Flexible Clocking Features
  - Programmable Internal DCO (up to 48 MHz)
  - 32.768-kHz Low-Frequency Crystal Support (LFXT)
  - High-Frequency Crystal Support (HFXT) up to 48 MHz
  - Low-Frequency Trimmed Internal Reference Oscillator (REFO)
  - Very Low-Power Low-Frequency Internal Oscillator (VLO)
  - Module Oscillator (MODOSC)
  - System Oscillator (SYSOSC)
- Enhanced System Options
  - Programmable Supervision and Monitoring of Supply Voltage
  - Multiple-Class Resets for Better Control of Application and Debug
  - Eight-Channel DMA
  - Real-Time Clock (RTC) With Calendar and Alarm Functions
- Timing and Control
  - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
  - Two 32-Bit Timers, Each With Interrupt Generation Capability
- Serial Communication
  - Up to Four eUSCI_A Modules
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI (up to 16 Mbps)
  - Up to Four eUSCI_B Modules
    - I^2C (With Multiple-Slave Addressing)
    - SPI (up to 16 Mbps)
- Flexible I/O Features
  - Ultra-Low-Leakage I/Os (±20 nA Maximum)
  - Up to Four High-Drive I/Os (20-mA Capability)
  - All I/Os With Capacitive Touch Capability
  - Up to 48 I/Os With Interrupt and Wake-up Capability
  - Up to 24 I/Os With Port Mapping Capability
  - Eight I/Os With Glitch Filtering Capability
- Advanced Low-Power Analog Features
  - 14-Bit, 1-MSPS SAR ADC
  - Internal Voltage Reference With 10-ppm/°C Typical Stability
  - Two Analog Comparators
- Encryption and Data Integrity Accelerators
  - 128-, 192-, or 256-Bit AES Encryption and Decryption Accelerator
  - 32-Bit Hardware CRC Engine
- JTAG and Debug Support
  - Support for 4-Pin JTAG and 2-Pin SWD Debug Interfaces
  - Support for Serial Wire Trace
  - Support for Power Debug and Profiling of Applications

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1.2 Applications

- Industrial and Automation
  - Home Automation
  - Smoke Detectors
  - Barcode Scanners
- Metering
  - Electric Meters
  - Flow Meters
- Health and Fitness
  - Watches
  - Activity Monitors
  - Fitness Accessories
  - Blood Glucose Meters
- Consumer Electronics
  - Mobile Devices
  - Sensor Hubs

1.3 Description

The MSP432P401x device family is TI's latest addition to its portfolio of efficient ultra-low-power mixed-signal MCUs. The MSP432P401x family features the ARM Cortex-M4 processor in a wide configuration of device options including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount.

Overall, the MSP432P401x is an ideal combination of the TI MSP430™ low-power DNA, advance mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The devices ship with bundled driver libraries and are compatible with standardized components of the ARM ecosystem.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE(2)
MSP432P401RIPZ MSP432P401MIPZ	LQFP (100)	14 mm × 14 mm
MSP432P401RIZXH MSP432P401MIZXH	NFBGA (80)	5 mm × 5 mm
MSP432P401RIRGC MSP432P401MIRGC	VQFN (64)	9 mm × 9 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 9, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 9.

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1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the MSP432P401x devices.

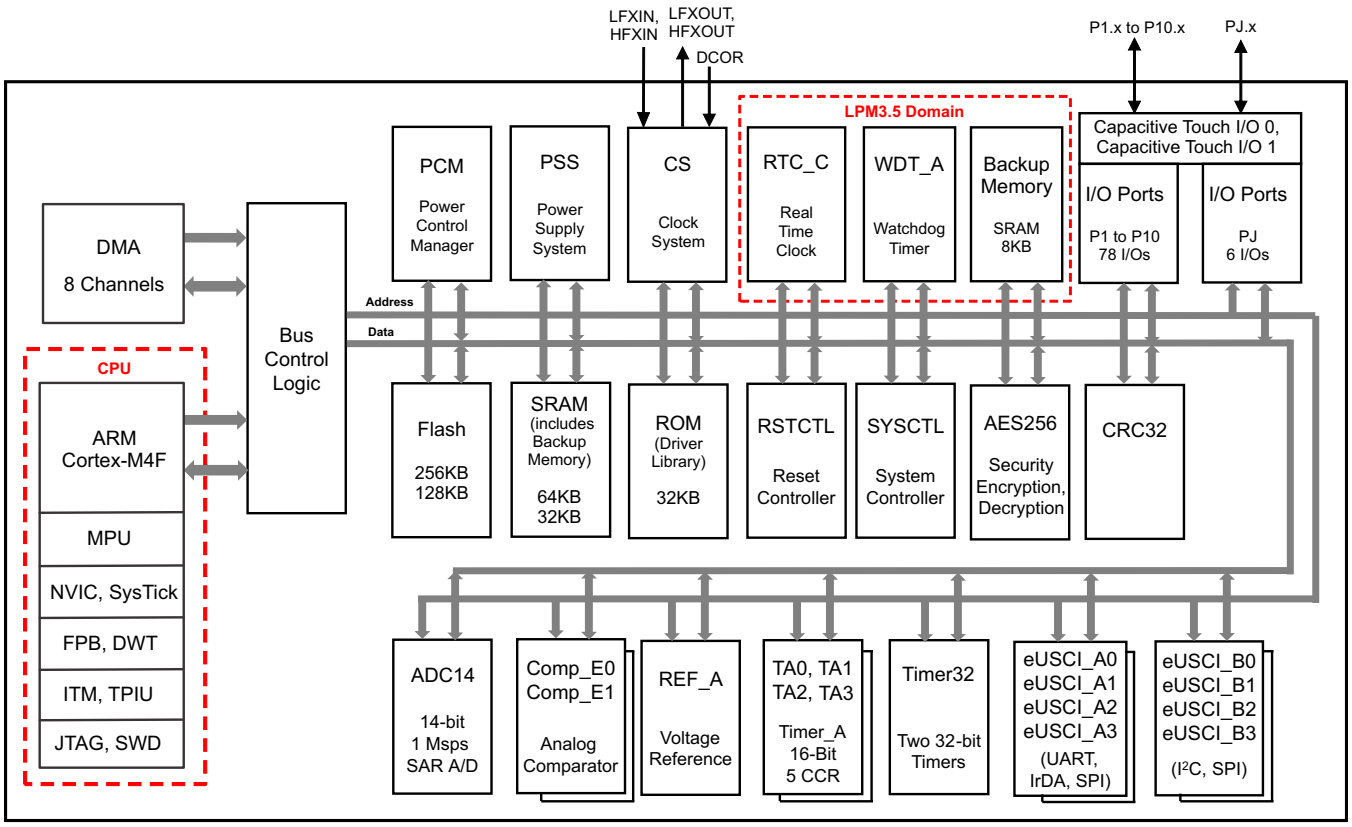


Figure 1-1. MSP432P401x Functional Block Diagram

The CPU and all the peripherals in the device interact with each other through a common AHB matrix. In some cases, there are bridges between the AHB ports and the peripherals. These bridges are transparent to the application from a memory map perspective and hence not shown in the block diagram.

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 31, 2015 to February 16, 2016	Page
• Changed the MIN value of the $N_{Endurance}$ parameter from 100k cycles to 20000 cycles in Table 5-53, *Flash Memory*	58

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3 Device Comparison

Table 3-1 lists the features of the MSP432P401x devices.

Table 3-1. Device Comparison(1)

DEVICE	FLASH (KB)	SRAM (KB)	ADC14 CHANNELS	Comparator-E0 CHANNELS	Comparator-E1 CHANNELS	Timer_A(2)	eUSCI		20-mA DRIVE I/O	TOTAL I/Os	PACKAGE TYPE
							CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I^2C			
MSP432P401RIPZ	256	64	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401MIPZ	128	32	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401RIZXH	256	64	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401MIZXH	128	32	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401RIRGC	256	64	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC
MSP432P401MIRGC	128	32	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 9, or see the TI website at www.ti.com.
(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

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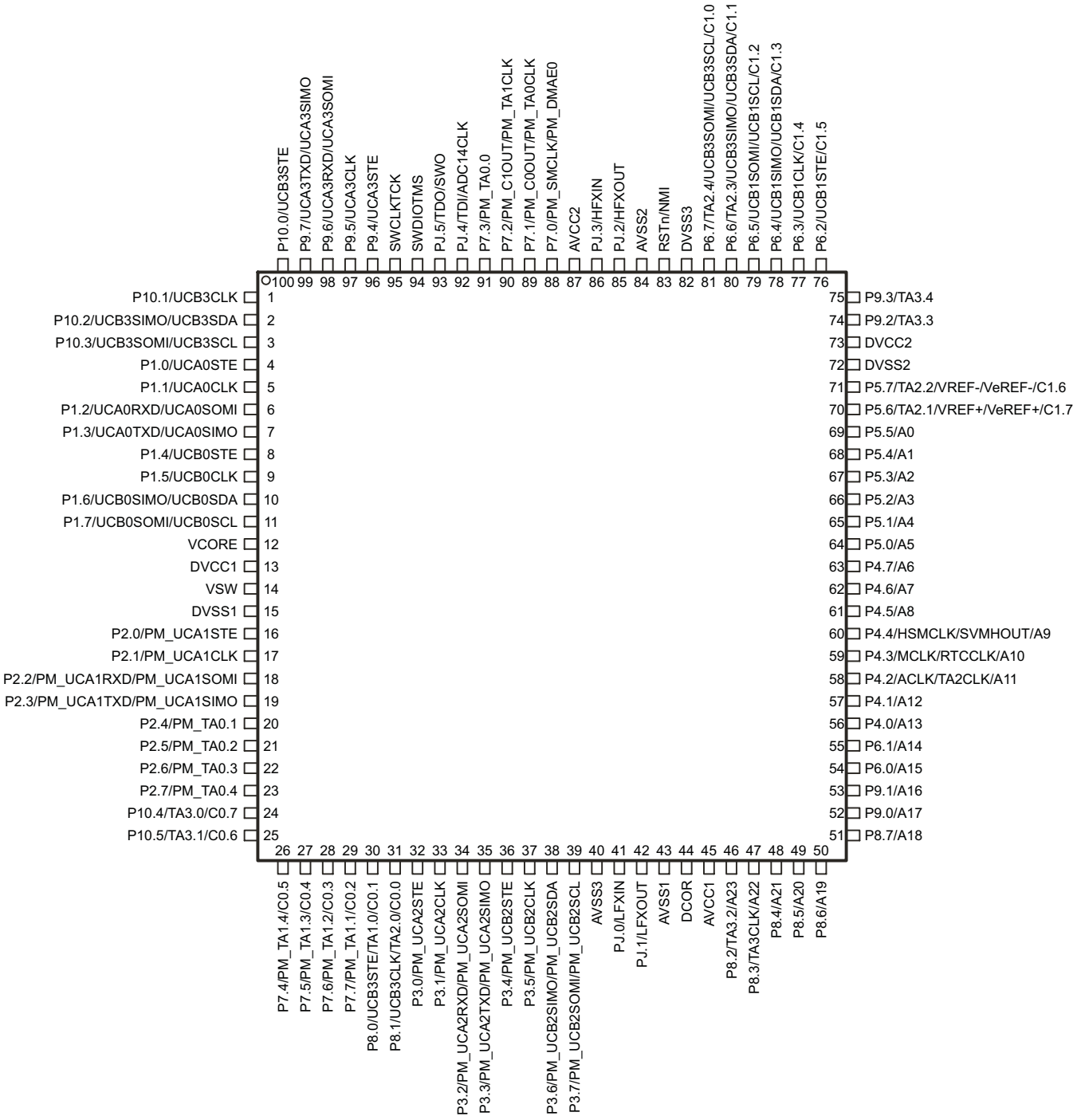
4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 100-pin PZ package.

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Notes:
1. The secondary digital functions on Ports P2, P3, and P7 are fully mappable. The pin designation shows only the default mapping. See Table 6-19 for details.
2. Glitch filter is implemented on the following 8 digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
3. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
4. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
5. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-1. 100-Pin PZ Package (Top View)

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Figure 4-2 shows the pinout of the 80-pin ZXH package.

P1.0 A1	SWCLKTCK A2	PJ.5 A3	P7.3 A4	PJ.3 A5	PJ.2 A6	P6.5 A7	P6.4 A8	P6.2 A9
P1.1 B1	SWDIOTMS B2	PJ.4 B3	P7.2 B4	P7.0 B5	RSTn/NMI B6	P6.7 B7	P6.6 B8	P6.3 B9
P1.5 C1	VCORE C2		P1.2 C4	P7.1 C5	DVCC2 C6	DVSS3 C7	P5.5 C8	P5.7 C9
P1.6 D1	DVCC1 D2	P1.4 D3	P1.3 D4	AVCC2 D5	AVSS2 D6	P5.3 D7	P5.4 D8	P5.6 D9
P1.7 E1	VSW E2	P2.2 E3	P2.0 E4	AVSS3 E5	DVSS2 E6	P5.0 E7	P5.1 E8	P5.2 E9
P2.1 F1	DVSS1 F2	P2.4 F3	P2.3 F4	AVSS1 F5	AVCC1 F6	P4.5 F7	P4.6 F8	P4.7 F9
P2.5 G1	P2.6 G2	P7.7 G3	P8.1 G4	P3.2 G5	P3.5 G6	P4.2 G7	P4.3 G8	P4.4 G9
P2.7 H1	P7.5 H2	P8.0 H3	P3.1 H4	P3.4 H5	P3.7 H6	P6.1 H7	P4.1 H8	P4.0 H9
P7.4 J1	P7.6 J2	P3.0 J3	P3.3 J4	P3.6 J5	PJ.0 J6	PJ.1 J7	DCOR J8	P6.0 J9

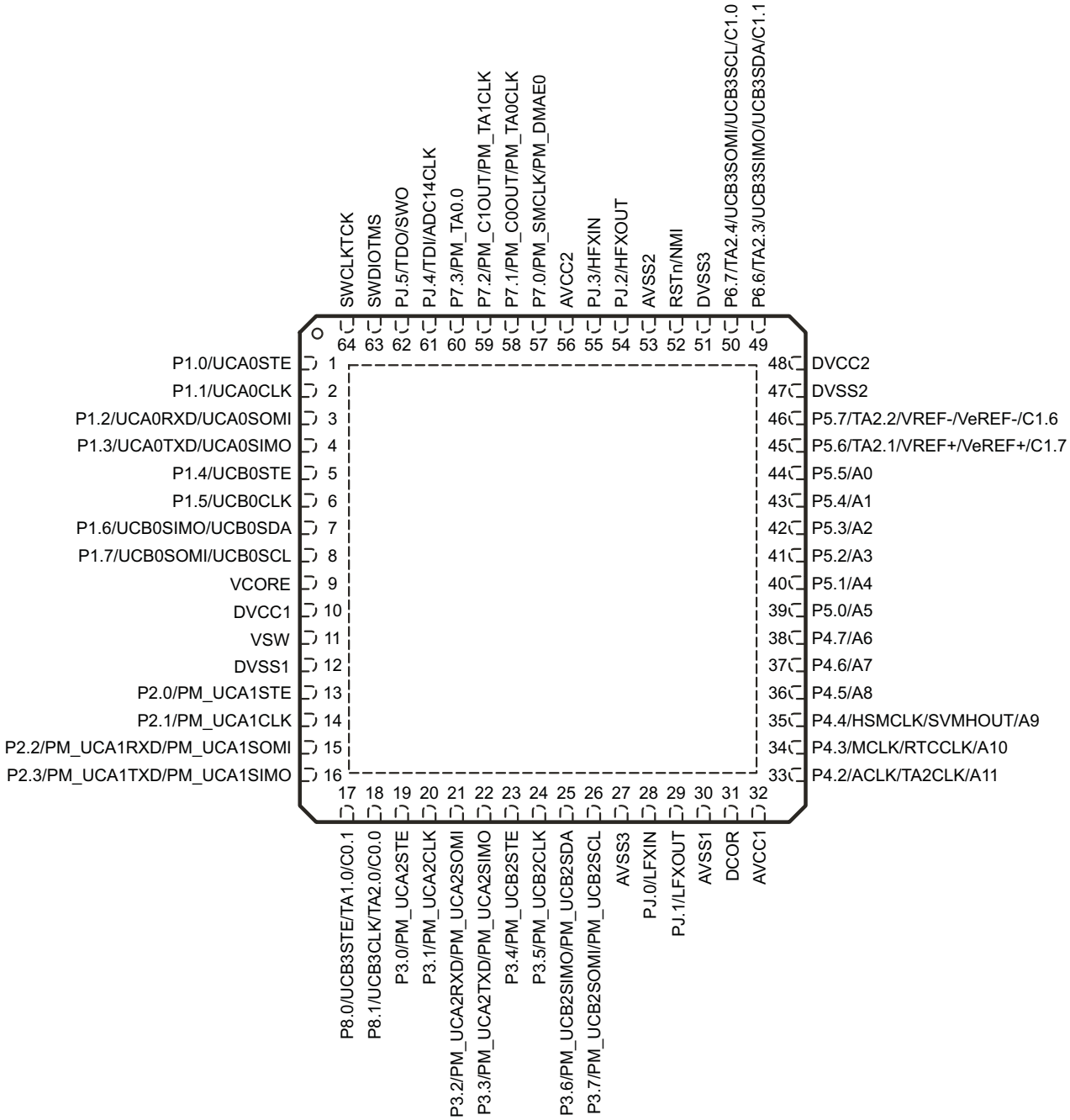
Notes:
1. Glitch filter is implemented on the following 8 digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
2. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
3. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
4. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-2. 80-Pin ZXH Package (Top View)

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Figure 4-3 shows the pinout of the 64-pin RGC package.



Notes:
1. The secondary digital functions on Ports P2, P3, and P7 are fully mappable. The pin designation shows only the default mapping. See Table 6-19 for details.
2. Glitch filter is implemented on the following 8 digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
TI recommends connecting the thermal pad on the QFN package to DVSS.
4. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
5. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
6. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-3. 64-Pin RGC Package (Top View)

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4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

TERMINAL				I/O(1)	DESCRIPTION
NAME	NO.(2)				
	PZ	ZXH	RGC		
P10.1/ UCB3CLK	1	N/A	N/A	I/O	General-purpose digital I/O Clock signal input – eUSCI_B3 SPI slave mode Clock signal output – eUSCI_B3 SPI master mode
P10.2/ UCB3SIMO/UCB3SDA	2	N/A	N/A	I/O	General-purpose digital I/O Slave in, master out – eUSCI_B3 SPI mode I^2C data – eUSCI_B3 I^2C mode
P10.3/ UCB3SOMI/UCB3SCL	3	N/A	N/A	I/O	General-purpose digital I/O Slave out, master in – eUSCI_B3 SPI mode I^2C clock – eUSCI_B3 I^2C mode
P1.0/ UCA0STE	4	A1	1	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability Slave transmit enable – eUSCI_A0 SPI mode
P1.1/ UCA0CLK	5	B1	2	I/O	General-purpose digital I/O with port interrupt and wake-up capability Clock signal input – eUSCI_A0 SPI slave mode Clock signal output – eUSCI_Ao0 SPI master mode
P1.2/ UCA0RXD/UCA0SOMI	6	C4	3	I/O	General-purpose digital I/O with port interrupt and wake-up capability Receive data – eUSCI_A0 UART mode Slave out, master in – eUSCI_A0 SPI mode
P1.3/ UCA0TXD/UCA0SIMO	7	D4	4	I/O	General-purpose digital I/O with port interrupt and wake-up capability Transmit data – eUSCI_A0 UART mode Slave in, master out – eUSCI_A0 SPI mode
P1.4/ UCB0STE	8	D3	5	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability Slave transmit enable – eUSCI_B0 SPI mode
P1.5/ UCB0CLK	9	C1	6	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
P1.6/ UCB0SIMO/UCB0SDA	10	D1	7	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave in, master out – eUSCI_B0 SPI mode I^2C data – eUSCI_B0 I^2C mode
P1.7/ UCB0SOMI/UCB0SCL	11	E1	8	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave out, master in – eUSCI_B0 SPI mode I^2C clock – eUSCI_B0 I^2C mode
VCORE(3)	12	C2	9		Regulated core power supply (internal use only, no external current loading)
DVCC1	13	D2	10		Digital power supply
VSW	14	E2	11		DC-to-DC converter switching output.
DVSS1	15	F2	12		Digital ground supply
P2.0/ PM_UCA1STE	16	E4	13	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave transmit enable – eUSCI_A1 SPI mode
P2.1/ PM_UCA1CLK	17	F1	14	I/O	General-purpose digital I/O with port interrupt and wake-up capability Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode
P2.2/ PM_UCA1RXD/ PM_UCA1SOMI	18	E3	15	I/O	General-purpose digital I/O with port interrupt and wake-up capability Receive data – eUSCI_A1 UART mode Slave out, master in – eUSCI_A1 SPI mode

(1) I = input, O = output
(2) N/A = not available
(3) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	PZ	ZXH	RGC		
P2.3/ PM_UCA1TXD/ PM_UCA1SIMO	19	F4	16	I/O	General-purpose digital I/O with port interrupt and wake-up capability Transmit data – eUSCI_A1 UART mode Slave in, master out – eUSCI_A1 SPI mode
P2.4/ PM_TA0.1	20	F3	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability TA0 CCR1 capture: CCI1A input, compare: Out1
P2.5/ PM_TA0.2	21	G1	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability TA0 CCR2 capture: CCI2A input, compare: Out2
P2.6/ PM_TA0.3	22	G2	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability TA0 CCR3 capture: CCI3A input, compare: Out3
P2.7/ PM_TA0.4	23	H1	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability TA0 CCR4 capture: CCI4A input, compare: Out4
P10.4/ TA3.0/ C0.7	24	N/A	N/A	I/O	General-purpose digital I/O TA3 CCR0 capture: CCI0A input, compare: Out0 Comparator_E0 input 7
P10.5/ TA3.1/ C0.6	25	N/A	N/A	I/O	General-purpose digital I/O TA3 CCR1 capture: CCI1A input, compare: Out1 Comparator_E0 input 6
P7.4/ PM_TA1.4/ C0.5	26	J1	N/A	I/O	General-purpose digital I/O TA1 CCR4 capture: CCI4A input, compare: Out4 Comparator_E0 input 5
P7.5/ PM_TA1.3/ C0.4	27	H2	N/A	I/O	General-purpose digital I/O TA1 CCR3 capture: CCI3A input, compare: Out3 Comparator_E0 input 4
P7.6/ PM_TA1.2/ C0.3	28	J2	N/A	I/O	General-purpose digital I/O TA1 CCR2 capture: CCI2A input, compare: Out2 Comparator_E0 input 3
P7.7/ PM_TA1.1/ C0.2	29	G3	N/A	I/O	General-purpose digital I/O TA1 CCR1 capture: CCI1A input, compare: Out1 Comparator_E0 input 2
P8.0/ UCB3STE/ TA1.0/ C0.1	30	H3	17	I/O	General-purpose digital I/O Slave transmit enable – eUSCI_B3 SPI mode TA1 CCR0 capture: CCI0A input, compare: Out0 Comparator_E0 input 1
P8.1/ UCB3CLK/ TA2.0/ C0.0	31	G4	18	I/O	General-purpose digital I/O Clock signal input – eUSCI_B3 SPI slave mode Clock signal output – eUSCI_B3 SPI master mode TA2 CCR0 capture: CCI0A input, compare: Out0 Comparator_E0 input 0
P3.0/ PM_UCA2STE	32	J3	19	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability Slave transmit enable – eUSCI_A2 SPI mode
P3.1/ PM_UCA2CLK	33	H4	20	I/O	General-purpose digital I/O with port interrupt and wake-up capability Clock signal input – eUSCI_A2 SPI slave mode Clock signal output – eUSCI_A2 SPI master mode
P3.2/ PM_UCA2RXD/ PM_UCA2SOMI	34	G5	21	I/O	General-purpose digital I/O with port interrupt and wake-up capability Receive data – eUSCI_A2 UART mode Slave out, master in – eUSCI_A2 SPI mode
P3.3/ PM_UCA2TXD/ PM_UCA2SIMO	35	J4	22	I/O	General-purpose digital I/O with port interrupt and wake-up capability Transmit data – eUSCI_A2 UART mode Slave in, master out – eUSCI_A2 SPI mode
P3.4/ PM_UCB2STE	36	H5	23	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability Slave transmit enable – eUSCI_B2 SPI mode
P3.5/ PM_UCB2CLK	37	G6	24	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability Clock signal input – eUSCI_B2 SPI slave mode Clock signal output – eUSCI_B2 SPI master mode

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	PZ	ZXH	RGC		
P3.6/ PM_UCB2SIMO/ PM_UCB2SDA	38	J5	25	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave in, master out – eUSCI_B2 SPI mode I^2C data – eUSCI_B2 I^2C mode
P3.7/ PM_UCB2SOMI/ PM_UCB2SCL	39	H6	26	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave out, master in – eUSCI_B2 SPI mode I^2C clock – eUSCI_B2 I^2C mode
AVSS3	40	E5	27		Analog ground supply
PJ.0/ LFXIN	41	J6	28	I/O	General-purpose digital I/O Input for low-frequency crystal oscillator LFXT
PJ.1/ LFXOUT	42	J7	29	I/O	General-purpose digital I/O Output of low-frequency crystal oscillator LFXT
AVSS1	43	F5	30		Analog ground supply
DCOR	44	J8	31		DCO external resistor pin
AVCC1	45	F6	32		Analog power supply
P8.2/ TA3.2/ A23	46	N/A	N/A	I/O	General-purpose digital I/O TA3 CCR2 capture: CCI2A input, compare: Out2 ADC analog input A23
P8.3/ TA3CLK/ A22	47	N/A	N/A	I/O	General-purpose digital I/O TA3 input clock ADC analog input A22
P8.4/ A21	48	N/A	N/A	I/O	General-purpose digital I/O ADC analog input A21
P8.5/ A20	49	N/A	N/A	I/O	General-purpose digital I/O ADC analog input A20
P8.6/ A19	50	N/A	N/A	I/O	General-purpose digital I/O ADC analog input A19
P8.7/ A18	51	N/A	N/A	I/O	General-purpose digital I/O ADC analog input A18
P9.0/ A17	52	N/A	N/A	I/O	General-purpose digital I/O ADC analog input A17
P9.1/ A16	53	N/A	N/A	I/O	General-purpose digital I/O ADC analog input A16
P6.0/ A15	54	J9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability. ADC analog input A15
P6.1/ A14	55	H7	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability. ADC analog input A14
P4.0/ A13	56	H9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability. ADC analog input A13
P4.1/ A12	57	H8	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability. ADC analog input A12
P4.2/ ACLK/ TA2CLK/ A11	58	G7	33	I/O	General-purpose digital I/O with port interrupt and wake-up capability. ACLK clock output TA2 input clock ADC analog input A11
P4.3/ MCLK/ RTCCLK/ A10	59	G8	34	I/O	General-purpose digital I/O with port interrupt and wake-up capability. MCLK clock output RTC_C clock calibration output ADC analog input A10
P4.4/ HSMCLK/ SVMHOUT/ A9	60	G9	35	I/O	General-purpose digital I/O with port interrupt and wake-up capability HSMCLK clock output SVMH output ADC analog input A9
P4.5/ A8	61	F7	36	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A8

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	PZ	ZXH	RGC		
P4.6/ A7	62	F8	37	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A7
P4.7/ A6	63	F9	38	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A6
P5.0/ A5	64	E7	39	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A5
P5.1/ A4	65	E8	40	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A4
P5.2/ A3	66	E9	41	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A3
P5.3/ A2	67	D7	42	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A2
P5.4/ A1	68	D8	43	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A1
P5.5/ A0	69	C8	44	I/O	General-purpose digital I/O with port interrupt and wake-up capability ADC analog input A0
P5.6/ TA2.1/ VREF+/ VeREF+/ C1.7	70	D9	45	I/O	General-purpose digital I/O with port interrupt and wake-up capability TA2 CCR1 capture: CCI1A input, compare: Out1 Internal shared reference voltage positive terminal Positive terminal of external reference voltage to ADC Comparator_E1 input 7
P5.7/ TA2.2/ VREF-/ VeREF-/ C1.6	71	C9	46	I/O	General-purpose digital I/O with port interrupt and wake-up capability TA2 CCR2 capture: CCI2A input, compare: Out2 Internal shared reference voltage negative terminal Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground) Comparator_E1 input 6
DVSS2	72	E6	47		Digital ground supply
DVCC2	73	C6	48		Digital power supply
P9.2/ TA3.3	74	N/A	N/A	I/O	General-purpose digital I/O TA3 CCR3 capture: CCI3A input, compare: Out3
P9.3/ TA3.4	75	N/A	N/A	I/O	General-purpose digital I/O TA3 CCR4 capture: CCI4A input, compare: Out4
P6.2/ UCB1STE/ C1.5	76	A9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave transmit enable – eUSCI_B1 SPI mode Comparator_E1 input 5
P6.3/ UCB1CLK/ C1.4	77	B9	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability Clock signal input – eUSCI_B1 SPI slave mode Clock signal output – eUSCI_B1 SPI master mode Comparator_E1 input 4
P6.4/ UCB1SIMO/UCB1SDA/ C1.3	78	A8	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave in, master out – eUSCI_B1 SPI mode I^2C data – eUSCI_B1 I^2C mode Comparator_E1 input 3
P6.5/ UCB1SOMI/UCB1SCL/ C1.2	79	A7	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability Slave out, master in – eUSCI_B1 SPI mode I^2C clock – eUSCI_B1 I^2C mode Comparator_E1 input 2
P6.6/ TA2.3/ UCB3SIMO/UCB3SDA/ C1.1	80	B8	49	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability TA2 CCR3 capture: CCI3A input, compare: Out3 Slave in, master out – eUSCI_B3 SPI mode I^2C data – eUSCI_B3 I^2C mode Comparator_E1 input 1

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	PZ	ZXH	RGC		
P6.7/ TA2.4/ UCB3SOMI/UCB3SCL/ C1.0	81	B7	50	I/O	General-purpose digital I/O with port interrupt, wake-up and glitch filtering capability TA2 CCR4 capture: CCI4A input, compare: Out4 Slave out, master in – eUSCI_B3 SPI mode I^2C clock – eUSCI_B3 I^2C mode Comparator_E1 input 0
DVSS3	82	C7	51		Digital ground supply
RSTn/ NMI	83	B6	52	I	External reset (active low) External nonmaskable interrupt
AVSS2	84	D6	53		Analog ground supply
PJ.2/ HFXOUT	85	A6	54	I/O	General-purpose digital I/O Output for high-frequency crystal oscillator HFXT
PJ.3/ HFXIN	86	A5	55	I/O	General-purpose digital I/O Input for high-frequency crystal oscillator HFXT
AVCC2	87	D5	56		Analog power supply
P7.0/ PM_SMCLK/ PM_DMAE0	88	B5	57	I/O	General-purpose digital I/O SMCLK clock output DMA external trigger input
P7.1/ PM_C0OUT/ PM_TA0CLK	89	C5	58	I/O	General-purpose digital I/O Comparator_E0 output TA0 input clock
P7.2/ PM_C1OUT/ PM_TA1CLK	90	B4	59	I/O	General-purpose digital I/O Comparator_E1 output TA1 input clock
P7.3/ PM_TA0.0	91	A4	60	I/O	General-purpose digital I/O TA0 CCR0 capture: CCI0A input, compare: Out0
PJ.4/ TDI/ ADC14CLK	92	B3	61	I/O	General-purpose digital I/O JTAG test data input ADC14 clock output
PJ.5/ TDO/ SWO	93	A3	62	I/O	General-purpose digital I/O JTAG test data output Serial wire trace output
SWDIOTMS	94	B2	63	I/O	Serial wire data input/output (SWDIO)/JTAG test mode select (TMS)
SWCLKTCK	95	A2	64	I	Serial wire clock input (SWCLK)/JTAG clock input (TCK)
P9.4/ UCA3STE	96	N/A	N/A	I/O	General-purpose digital I/O Slave transmit enable – eUSCI_A3 SPI mode
P9.5/ UCA3CLK	97	N/A	N/A	I/O	General-purpose digital I/O Clock signal input – eUSCI_A3 SPI slave mode Clock signal output – eUSCI_A3 SPI master mode
P9.6/ UCA3RXD/UCA3SOMI	98	N/A	N/A	I/O	General-purpose digital I/O Receive data – eUSCI_A3 UART mode Slave out, master in – eUSCI_A3 SPI mode
P9.7/ UCA3TXD/UCA3SIMO	99	N/A	N/A	I/O	General-purpose digital I/O Transmit data – eUSCI_A3 UART mode Slave in, master out – eUSCI_A3 SPI mode
P10.0/ UCB3STE	100	N/A	N/A	I/O	General-purpose digital I/O Slave transmit enable – eUSCI_B3 SPI mode
QFN Pad	N/A	N/A	Pad		QFN package exposed thermal pad. Connection to VSS is recommended.

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5 Specifications

5.1 Absolute Maximum Ratings (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3	4.17	V
Voltage difference between DVCC and AVCC pins (2)		±0.3	V
Voltage applied to any pin (3)	–0.3	V_{CC} + 0.3 V (4.17 V MAX)	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (4)	–40	125	°C
Maximum junction temperature, T_J		95	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device.
(3) All voltages referenced to V_{SS}.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

TYP data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range at all DVCC and AVCC pins (1) (2) (3)	At power-up (with internal V_{CC} supervision)	1.65		3.7	V
		Normal operation, Flash not active (with internal V_{CC} supervision)	1.62		3.7	
		Normal operation, Flash active (with internal V_{CC} supervision)	1.71		3.7	
		Normal operation, Flash active (without internal V_{CC} supervision)	1.62		3.7	
V_{SS}	Supply voltage on all DVSS and AVSS pins			0		V
I_{INRUSH}	Inrush current into the V_{CC} pins (4)				100	mA
f_{MCLK}	Frequency of the CPU and AHB clock in the system (5)		0		48	MHz
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		95	°C

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of ±0.1 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation. Refer to section Section 5.4 for decoupling capacitor recommendations.
(2) Supply voltage must not change faster than TBD. Faster changes can cause the VCCDET to trigger a reset even within the recommended supply voltage range.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) Does not include I/O currents (driven by application requirements)
(5) Operating frequency may require the flash to be accessed with wait states. Refer to Section 5.8 for further details

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5.4 Recommended External Components (1) (2) (3)

			MIN	TYP	MAX	UNIT
C_{DVCC}	Capacitor on DVCC pin	For DC-DC operation (4)	3.3	4.7		µF
		For LDO-only operation	3.3	4.7		
C_{VCORE}	Capacitor on VCORE pin	For DC-DC operation, including capacitor tolerance	1.54	4.7	9	µF
		For LDO-only operation, including capacitor tolerance	70	100	9000	nF
C_{AVCC}	Capacitor on AVCC pin		3.3	4.7		µF
L_{VSW}	Inductor between VSW and VCORE pins for DC-DC		3.3	4.7	13	µH
$R_{LVSW-DCR}$	Allowed DCR for L_{VSW}			150	350	mΩ
$I_{SAT-LVSW}$	L_{VSW} saturation current		700			mA

(1) For optimum performance, select the component value to match the typical value given in the table.
(2) Refer to the section on board guidelines for further details on component selection, placement as well as related PCB design guidelines.
(3) Tolerance of the capacitance/inductance values should be taken into account when choosing a component, in order to ensure that the Min/Max ranges are never exceeded
(4) C_{DVCC} should not be smaller than C_{VCORE}

5.5 Operating Mode V_{CC} Ranges

over operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC_LDO_VCORE0}$	AM_LDO_VCORE0 (1) (2) AM_LF_VCORE0 LPM0_LDO_VCORE0 LPM0_LF_VCORE0 LPM3_VCORE0 LPM4_VCORE0 LPM3.5	LDO active, SVSMH enabled, Flash not active	1.62	3.7	V
		LDO active, SVSMH enabled, Flash active	1.71	3.7	
		LDO active, SVSMH disabled, Flash active	1.62	3.7	
$V_{CC_LDO_VCORE1}$	AM_LDO_VCORE1 (1) (2) AM_LF_VCORE1 LPM0_LDO_VCORE1 LPM0_LF_VCORE1 LPM3_VCORE1 LPM4_VCORE1	LDO active, SVSMH enabled, Flash active	1.71	3.7	V
		LDO active, SVSMH disabled, Flash active	1.62	3.7	
$V_{CC_DCDC_VCORE0}$	AM_DCDC_VCORE0 (3) (4) LPM0_DCDC_VCORE0	DC-DC active, SVSMH enabled or disabled	2.18	3.7	V
$V_{CC_DCDC_VCORE1}$	AM_DCDC_VCORE1 (3) (4) LPM0_DCDC_VCORE1	DC-DC active, SVSMH enabled or disabled	2.18	3.7	V
$V_{CC_VCORE_OFF}$	LPM4.5 (5)	LDO disabled, SVSMH enabled or disabled	1.62	3.7	V

(1) LPM0 mode associated with each active mode will have a similar V_{CC} range restriction.
(2) Flash remains active **only** in active modes and LPM0 modes.
(3) Low frequency active, Low frequency LPM0, LPM3, LPM4, and LPM3.5 modes are based on LDO **only**.
(4) When V_{CC} falls below the specified Min value, the DC-DC operation will switch to LDO automatically, as long as the V_{CC} drop is slower than the rate that is reliably detected. Refer to <ref> for more details.
(5) Core voltage is switched off in LPM4.5 mode.

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5.6 Operating Mode CPU Frequency Ranges(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	f_{MCLK}		UNIT
			MIN	MAX	
$f_{AM_LDO_VCORE0}$	AM_LDO_VCORE0	Medium-performance mode with LDO as the active regulator	0	24	MHz
$f_{AM_LDO_VCORE1}$	AM_LDO_VCORE1	High-performance mode with LDO as the active regulator	0	48	MHz
$f_{AM_DCDC_VCORE0}$	AM_DCDC_VCORE0	Medium-performance mode with DC-DC as the active regulator	0	24	MHz
$f_{AM_DCDC_VCORE1}$	AM_DCDC_VCORE1	High-performance mode with DC-DC as the active regulator	0	48	MHz
$f_{AM_LF_VCORE0}$	AM_LF_VCORE0	Low-frequency low-leakage mode with LDO as the active regulator	0	128	kHz
$f_{AM_LF_VCORE1}$	AM_LF_VCORE1	Low-frequency low-leakage mode with LDO as the active regulator	0	128	kHz

(1) DMA can be operated at the same frequency as CPU.

5.7 Operating Mode Peripheral Frequency Ranges

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	MIN	MAX	UNIT
$f_{AM_LPM0_VCORE0}$	AM_LDO_VCORE0	Peripheral frequency range in LDO or DC-DC based active or LPM0 modes for VCORE0	0	12	MHz
	AM_DCDC_VCORE0				
	LPM0_LDO_VCORE0				
	LPM0_DCDC_VCORE0				
$f_{AM_LPM0_VCORE1}$	AM_LDO_VCORE1	Peripheral frequency range in LDO or DC-DC based active or LPM0 modes for VCORE1	0	24	MHz
	AM_DCDC_VCORE1				
	LPM0_LDO_VCORE1				
	LPM0_DCDC_VCORE1				
$f_{AM_LPM0_LF}$	AM_LF_VCORE0	Peripheral frequency range in low-frequency active or low frequency LPM0 modes for VCORE0 and VCORE1	0	128	kHz
	AM_LF_VCORE1				
	LPM0_LF_VCORE0				
	LPM0_LF_VCORE1				
f_{LPM3} (1)	LPM3_VCORE0	Peripheral frequency in LPM3 mode for VCORE0 and VCORE1	0	32.768	kHz
	LPM3_VCORE1				
$f_{LPM3.5}$ (1)	LPM3.5	Peripheral frequency in LPM3.5 mode	0	32.768	kHz

(1) Only RTC and WDT can be active.

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5.8 Operating Mode Execution Frequency vs Flash Wait-State Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	NUMBER OF FLASH WAIT STATES	FLASH READ MODE	MAXIMUM SUPPORTED MCLK FREQUENCY(1), (2)		UNIT
			AM_LDO_VCORE0, AM_DCDC_VCORE0	AM_LDO_VCORE1, AM_DCDC_VCORE1	
$f_{MAX_NRM_FLWAIT0}$	0	Normal read mode	12	16	MHz
$f_{MAX_NRM_FLWAIT1}$	1	Normal read mode	24	32	MHz
$f_{MAX_NRM_FLWAIT2}$	2	Normal read mode	24	48	MHz
$f_{MAX_ORM_FLWAIT0}$	0	Other read modes(3)	6	8	MHz
$f_{MAX_ORM_FLWAIT1}$	1	Other read modes(3)	12	16	MHz
$f_{MAX_ORM_FLWAIT2}$	2	Other read modes(3)	18	24	MHz
$f_{MAX_ORM_FLWAIT3}$	3	Other read modes(3)	24	32	MHz
$f_{MAX_ORM_FLWAIT4}$	4	Other read modes(3)	24	40	MHz
$f_{MAX_ORM_FLWAIT5}$	5	Other read modes(3)	24	48	MHz

(1) Violation of the maximum frequency limitation for a given wait-state configuration results in nondeterministic data or instruction fetches from the flash memory.
(2) In low-frequency active modes, the flash can always be accessed in zero wait-state because the maximum MCLK frequency is limited to 128 kHz.
(3) Other read modes refer to Read Margin 0/1, Read Margin 0B/1B, Program Verify, Erase Verify, and Leakage Verify.

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5.9 Current Consumption

Table 5-1. Current Consumption During Device Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)(2)(3)

PARAMETER	V_{CC}	TYP	MAX	UNIT
I_{RESET}	2.2 V			µA
	3.0 V	540	1300	

(1) Device held in reset through RSTn/NMI pin.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.

Table 5-2. Current Consumption in LDO-Based Active Modes

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM_LDO_VCORE0,Flash}$ (6) (7)	Flash	3.0 V					3950	4700							µA
$I_{AM_LDO_VCORE1,Flash}$ (6) (7)	Flash	3.0 V											7600	8500	µA
$I_{AM_LDO_VCORE0,SRAM}$ (8)	SRAM	3.0 V													µA
$I_{AM_LDO_VCORE1,SRAM}$ (8)	SRAM	3.0 V													µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks kept active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 algorithm. Code execution from Flash, stack and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Device executing the Dhrystone 2.1 algorithm. Code execution from SRAM, stack and data in SRAM.

Table 5-3. Current Consumption in DC-DC-Based Active Modes

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM_DCDC_VCORE0,Flash}$ (6) (7)	Flash	3.0 V					2200	2800							µA
$I_{AM_DCDC_VCORE1,Flash}$ (6) (7)	Flash	3.0 V											4600	5400	µA
$I_{AM_DCDC_VCORE0,SRAM}$ (8)	SRAM	3.0 V													µA
$I_{AM_DCDC_VCORE1,SRAM}$ (8)	SRAM	3.0 V													µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks kept active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 algorithm. Code execution from Flash, stack and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Device executing the Dhrystone 2.1 algorithm. Code execution from SRAM, stack and data in SRAM.

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Table 5-4. Current Consumption in Low-Frequency Active Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5)

PARAMETER	EXECUTION MEMORY	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM_LF_VCORE0,\ Flash}$ (6) (7)	Flash	2.2 V									µA
		3.0 V			90					570	
$I_{AM_LF_VCORE1,\ Flash}$ (6) (7)	Flash	2.2 V									µA
		3.0 V			95					680	
$I_{AM_LF_VCORE0,\ SRAM}$ (8)	SRAM	2.2 V									µA
		3.0 V									
$I_{AM_LF_VCORE1,\ SRAM}$ (8)	SRAM	2.2 V									µA
		3.0 V									

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) MCLK sourced by REFO at 128 kHz.
(4) All peripherals are inactive.
(5) SRAM banks 0,1 enabled for execution from flash and SRAM banks 0 to 3 enabled for execution from SRAM.
(6) Flash configured to 0 wait states.
(7) Device executing the Dhrystone 2.1 algorithm. Code execution from Flash, stack and data in SRAM.
(8) Device executing the Dhrystone 2.1 algorithm. Code execution from SRAM, stack and data also in SRAM.

Table 5-5. Current Consumption in LDO-Based LPM0 Modes

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5)(6)

PARAMETER	V_{CC}	MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0_LDO_VCORE0}$	2.2 V													µA
	3.0 V					700	1350							
$I_{LPM0_LDO_VCORE1}$	2.2 V													µA
	3.0 V											1130	1900	

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) CPU is OFF, Flash or SRAM not being accessed.
(5) All SRAM banks kept active.
(6) All peripherals are inactive.

Table 5-6. Current Consumption in DC-DC-Based LPM0 Modes

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5)(6)

PARAMETER	V_{CC}	MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0_DCDC_VCORE0}$	2.2 V													µA
	3.0 V					500	950							
$I_{LPM0_DCDC_VCORE1}$	2.2 V													µA
	3.0 V											800	1350	

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) CPU is OFF, Flash or SRAM not being accessed.
(5) All SRAM banks kept active.
(6) All peripherals are inactive.

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Table 5-7. Current Consumption in Low-Frequency LPM0 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5)(6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0_LF_VCORE0}$	2.2 V									µA
	3.0 V			70					530	
$I_{LPM0_LF_VCORE1}$	2.2 V									µA
	3.0 V			70					625	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) MCLK sourced by REFO at 128 kHz.
(4) All peripherals are inactive.
(5) Bank-0 of SRAM kept active. Rest of the banks are powered down.
(6) CPU is OFF, Flash or SRAM not being accessed.

Table 5-8. Current Consumption in LPM3, LPM4 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)(3)(4)(5) (6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3_VCORE0_RTCLF}$ (7)(8)	2.2 V									µA
	3.0 V			0.85					17	
$I_{LPM3_VCORE0_RTCREFO}$ (9)(8)	2.2 V									µA
	3.0 V			1.35					18	
$I_{LPM3_VCORE1_RTCLF}$ (7)(8)	2.2 V									µA
	3.0 V			1.16					24	
$I_{LPM3_VCORE1_RTCREFO}$ (9)(8)	2.2 V									µA
	3.0 V			1.67					25	
I_{LPM4_VCORE0} (10)	2.2 V									µA
	3.0 V									
I_{LPM4_VCORE1} (10)	2.2 V									µA
	3.0 V									

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU is OFF, Flash powered down.
(4) Bank-0 of SRAM retained, all other banks powered down.
(5) Refer to Table 5-54 for details on additional current consumed for each extra Bank that is enabled for retention.
(6) SVSMH and SVSL are disabled.
(7) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(8) WDT module is disabled.
(9) RTC sourced by REFO.
(10) RTC and WDT modules disabled.

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Table 5-9. Current Consumption in LPM3.5, LPM4.5 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5_RTCLF}$(3)(4)(5)(6)(7)	2.2 V									µA
	3.0 V			0.8					17	
$I_{LPM3.5_RTCREFO}$(3)(4)(8)(6)(7)	2.2 V									µA
	3.0 V			1.3					18	
$I_{LPM4.5}$(9)(10)	2.2 V									µA
	3.0 V			0.1					7	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU and Flash are powered down.
(4) Bank-0 of SRAM retained, all other banks powered down.
(5) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(6) WDT module is disabled.
(7) SVSMH and SVSL are disabled.
(8) RTC sourced by REFO.
(9) No core voltage. CPU, Flash and all banks of SRAM are powered down.
(10) SVSMH is disabled.

Table 5-10. Current Consumption of Digital Peripherals

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I_{TIMER_A0}	Timer_A0 configured as PWM timer with 50% duty cycle	TBD	TBD	µA/MHz
$I_{TIMER32}$	Timer32 enabled	TBD	TBD	µA/MHz
I_{UART}	eUSCI_A configured in UART mode.	TBD	TBD	µA/MHz
I_{SPI}	eUSCI_A configured in SPI master mode	TBD	TBD	µA/MHz
I_{I2C}	eUSCI_B configured in I^2C master mode	TBD	TBD	µA/MHz
I_{WDT_A}	WDT_A configured in interval timer mode	TBD	TBD	µA/MHz
I_{RTC_C}	RTC_C enabled and sourced from 32-kHz LFXT	TBD	TBD	nA
I_{AES256}	AES256 active.	TBD	TBD	µA/MHz
I_{CRC32}	CRC32 active.	TBD	TBD	µA/MHz

(1) Measured with VCORE = 1.2 V.

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5.10 Timing and Switching Characteristics

5.10.1 Mode Transition Timing

Table 5-11. Active Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	LATENCY		UNIT
				TYP	MAX	
$t_{OFF_AMLDO0,100\ nF}$	Power Off	AM_LDO_VCORE0	From V_{CC} reaching 1.65 V to start of application code. C_{VCORE} = 100 nF.	4.5	5.2	ms
$t_{OFF_AMLDO0,4.7\ \mu F}$	Power Off	AM_LDO_VCORE0	From V_{CC} reaching 1.65 V to start of application code. C_{VCORE} = 4.7 µF.	4.7	5.8	ms
t_{AMLDO0_AMLDO1}	AM_LDO_VCORE0	AM_LDO_VCORE1	Transition from AM_LDO_VCORE0 to AM_LDO_VCORE1. MCLK frequency = 24 MHz.	285	340	µs
t_{AMLDO1_AMLDO0}	AM_LDO_VCORE1	AM_LDO_VCORE0	Transition from AM_LDO_VCORE1 to AM_LDO_VCORE0. MCLK frequency = 24 MHz.	4	5	µs
$t_{AMLDO0_AMDCDC0}$	AM_LDO_VCORE0	AM_DCDC_VCORE0	Transition from AM_LDO_VCORE0 to AM_DCDC_VCORE0. MCLK frequency = 24 MHz	15	32	µs
$t_{AMDCDC0_AMLDO0}$	AM_DCDC_VCORE0	AM_LDO_VCORE0	Transition from AM_DCDC_VCORE0 to AM_LDO_VCORE0. MCLK frequency = 24 MHz	15	27	µs
$t_{AMLDO1_AMDCDC1}$	AM_LDO_VCORE1	AM_DCDC_VCORE1	Transition from AM_LDO_VCORE1 to AM_DCDC_VCORE1. MCLK frequency = 48 MHz	15	32	µs
$t_{AMDCDC1_AMLDO1}$	AM_DCDC_VCORE1	AM_LDO_VCORE1	Transition from AM_DCDC_VCORE1 to AM_LDO_VCORE1. MCLK frequency = 48 MHz	15	27	µs
t_{AMLDO0_AMLF0}	AM_LDO_VCORE0	AM_LF_VCORE0	Transition from AM_LDO_VCORE0 to AM_LF_VCORE0. All high frequency clock sources (DCO, HFXT, MODOSC) disabled. SELM = 2, REFO frequency = 128 kHz	115	125	µs
t_{AMLF0_AMLDO0}	AM_LF_VCORE0	AM_LDO_VCORE0	Transition from AM_LF_VCORE0 to AM_LDO_VCORE0. All high frequency clock sources (DCO, HFXT, MODOSC) disabled. SELM = 2, REFO frequency = 128 kHz.	115	130	µs
t_{AMLDO1_AMLF1}	AM_LDO_VCORE1	AM_LF_VCORE1	Transition from AM_LDO_VCORE1 to AM_LF_VCORE1. All high frequency clock sources (DCO, HFXT, MODOSC) disabled. SELM = 2, REFO frequency = 128 kHz.	110	115	µs
t_{AMLF1_AMLDO1}	AM_LF_VCORE1	AM_LDO_VCORE1	Transition from AM_LF_VCORE1 to AM_LDO_VCORE1. All high frequency clock sources (DCO, HFXT, MODOSC) disabled. SELM = 2, REFO frequency = 128 kHz.	110	120	µs

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Table 5-12. LPM0 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	LATENCY		UNIT
				TYP	MAX	
$t_{AMLDO0_LPM0LDO0}$ (1)	AM_LDO_VCORE0	LPM0_LDO_VCORE0	Transition from AM_LDO_VCORE0 to LPM0_LDO_VCORE0	1		MCLK cycles
$t_{LPM0LDO0_AMLDO0}$ (2)	LPM0_LDO_VCORE0	AM_LDO_VCORE0	Transition from LPM0_LDO_VCORE0 to AM_LDO_VCORE0 through I/O interrupt	3	4	MCLK cycles
$t_{AMDCDC0_LPM0DCDC0}$ (1)	AM_DCDC_VCORE0	LPM0_DCDC_VCORE0	Transition from AM_DCDC_VCORE0 to LPM0_DCDC_VCORE0	1		MCLK cycles
$t_{LPM0DCDC0_AMDCDC0}$ (2)	LPM0_DCDC_VCORE0	AM_DCDC_VCORE0	Transition from LPM0_DCDC_VCORE0 to AM_DCDC_VCORE0 through I/O interrupt	3	4	MCLK cycles
$t_{AMLF0_LPM0LF0}$ (1)	AM_LF_VCORE0	LPM0_LF_VCORE0	Transition from AM_LF_VCORE0 to LPM0_LF_VCORE0, All high frequency clock sources (DCO, HFXT, MODOSC) disabled	1		MCLK cycles
$t_{LPM0LF0_AMLF0}$ (2)	LPM0_LF_VCORE0	AM_LF_VCORE0	Transition from LPM0_LF_VCORE0 to AM_LF_VCORE0 through I/O interrupt, All high frequency clock sources (DCO, HFXT, MODOSC) disabled	3	4	MCLK cycles
$t_{AMLDO1_LPM0LDO1}$ (1)	AM_LDO_VCORE1	LPM0_LDO_VCORE1	Transition from AM_LDO_VCORE1 to LPM0_LDO_VCORE1	1		MCLK cycles
$t_{LPM0LDO1_AMLDO1}$ (2)	LPM0_LDO_VCORE1	AM_LDO_VCORE1	Transition from LPM0_LDO_VCORE1 to AM_LDO_VCORE1 through I/O interrupt	3	4	MCLK cycles
$t_{AMDCDC1_LPM0DCDC1}$ (1)	AM_DCDC_VCORE1	LPM0_DCDC_VCORE1	Transition from AM_DCDC_VCORE1 to LPM0_DCDC_VCORE1	1		MCLK cycles
$t_{LPM0DCDC1_AMDCDC1}$ (2)	LPM0_DCDC_VCORE1	AM_DCDC_VCORE1	Transition from LPM0_DCDC_VCORE1 to AM_DCDC_VCORE1 through I/O interrupt	3	4	MCLK cycles
$t_{AMLF1_LPM0LF1}$ (1)	AM_LF_VCORE1	LPM0_LF_VCORE1	Transition from AM_LF_VCORE1 to LPM0_LF_VCORE1. All high frequency clock sources (DCO, HFXT, MODOSC) disabled	1		MCLK cycles
$t_{LPM0LF1_AMLF1}$ (2)	LPM0_LF_VCORE1	AM_LF_VCORE1	Transition from LPM0_LF_VCORE1 to AM_LF_VCORE1 through I/O interrupt. All high frequency clock sources (DCO, HFXT, MODOSC) disabled	3	4	MCLK cycles

(1) This is the latency between execution of WFI instruction by CPU to assertion of SLEEPING signal at CPU output.
(2) This is the latency between I/O interrupt event to deassertion of SLEEPING signal at CPU output.

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Table 5-13. LPM3, LPM4 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS		LATENCY		UNIT
					TYP	MAX	
t_{AMLDO0_LPMx0} (1)	AM_LDO_VCORE0	LPM3_LPM4_VCORE0	Transition from AM_LDO_VCORE0 to LPM3 or LPM4 at VCORE0.	SELM = 3, DCO frequency = 16 MHz	TBD	TBD	µs
				SELM = 3, DCO frequency = 24 MHz	22	24	
$t_{LPMx0_AMLDO0_NORIO}$ (2)	LPM3_LPM4_VCORE0	AM_LDO_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from nonglitch filter type I/O.	SELM = 3, DCO frequency = 16 MHz	TBD	TBD	µs
				SELM = 3, DCO frequency = 24 MHz	10	15	
$t_{LPMx0_AMLDO0_GFLTIO}$ (2)	LPM3_LPM4_VCORE0	AM_LDO_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1	SELM = 3, DCO frequency = 16 MHz	TBD	TBD	µs
				SELM = 3, DCO frequency = 24 MHz	10	16	
t_{AMLDO1_LPMx1} (1)	AM_LDO_VCORE1	LPM3_LPM4_VCORE1	Transition from AM_LDO_VCORE1 to LPM3 or LPM4 at VCORE1.	SELM = 3, DCO frequency = 32 MHz	TBD	TBD	µs
t_{AMLDO1_LPMx1} (1)	AM_LDO_VCORE1	LPM3_LPM4_VCORE1	Transition from AM_LDO_VCORE1 to LPM3 or LPM4 at VCORE1	SELM = 3, DCO frequency = 48 MHz	21	23	µs
$t_{LPMx1_AMLDO1_NORIO}$ (2)	LPM3_LPM4_VCORE1	AM_LDO_VCORE1	Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from nonglitch filter type I/O.	SELM = 3, DCO frequency = 32 MHz	TBD	TBD	µs
$t_{LPMx1_AMLDO1_NORIO}$ (2)	LPM3_LPM4_VCORE1	AM_LDO_VCORE1	Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from nonglitch filter type I/O.	SELM = 3, DCO frequency = 48 MHz	10	15	µs
$t_{LPMx1_AMLDO1_GFLTIO}$ (2)	LPM3_LPM4_VCORE1	AM_LDO_VCORE1	Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1.	SELM = 3, DCO frequency = 32 MHz	TBD	TBD	µs
$t_{LPMx1_AMLDO1_GFLTIO}$ (2)	LPM3_LPM4_VCORE1	AM_LDO_VCORE1	Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1	SELM = 3, DCO frequency = 48 MHz	10	16	µs

(1) This is the latency from WFI instruction execution by CPU to LPM3 or LPM4 entry.
(2) This is the latency from I/O wake-up event to MCLK clock start at device pin.

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Table 5-14. LPM3.5, LPM4.5 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	LATENCY		UNIT
				TYP	MAX	
$t_{AMLDO0_LPM3.5}$ (1)	AM_LDO_VCORE0	LPM3.5	Transition from AM_LDO_VCORE0 to LPM3.5	22	25	µs
$t_{AMDCDC0_LPM3.5}$ (1)	AM_DCDC_VCORE0	LPM3.5	Transition from AM_DCDC_VCORE0 to LPM3.5	34	47	µs
$t_{AMLF0_LPM3.5}$ (1)	AM_LF_VCORE0	LPM3.5	Transition from AM_LF_VCORE0 to LPM3.5	225	240	µs
$t_{AMLDO1_LPM3.5}$ (1)	AM_LDO_VCORE1	LPM3.5	Transition from AM_LDO_VCORE1 to LPM3.5	22	25	µs
$t_{AMDCDC1_LPM3.5}$ (1)	AM_DCDC_VCORE1	LPM3.5	Transition from AM_DCDC_VCORE1 to LPM3.5	32	45	µs
$t_{AMLF1_LPM3.5}$ (1)	AM_LF_VCORE1	LPM3.5	Transition from AM_LF_VCORE1 to LPM3.5	225	240	µs
$t_{AMLDO0_LPM4.5}$ (2)	AM_LDO_VCORE0	LPM4.5	Transition from AM_LDO_VCORE0 to LPM4.5	22	25	µs
$t_{AMDCDC0_LPM4.5}$ (2)	AM_DCDC_VCORE0	LPM4.5	Transition from AM_DCDC_VCORE0 to LPM4.5	32	45	µs
$t_{AMLF0_LPM4.5}$ (2)	AM_LF_VCORE0	LPM4.5	Transition from AM_LF_VCORE0 to LPM4.5	180	195	µs
$t_{AMLDO1_LPM4.5}$ (2)	AM_LDO_VCORE1	LPM4.5	Transition from AM_LDO_VCORE1 to LPM4.5	22	25	µs
$t_{AMDCDC1_LPM4.5}$ (2)	AM_DCDC_VCORE1	LPM4.5	Transition from AM_DCDC_VCORE1 to LPM4.5	22	25	µs
$t_{AMLF1_LPM4.5}$ (2)	AM_LF_VCORE1	LPM4.5	Transition from AM_LF_VCORE1 to LPM4.5	180	195	µs
$t_{LPM3.5_AMLDO0}$ (3)	LPM3.5	AM_LDO_VCORE0	Transition from LPM3.5 to AM_LDO_VCORE0	0.9	0.95	ms
$t_{LPM4.5_AMLDO0_SVSMON,100\ nF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, C_{VCORE} = 100 nF	1	TBD	ms
$t_{LPM4.5_AMLDO0_SVSMON,4.7\ µF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, C_{VCORE} = 4.7 µF	TBD	TBD	ms
$t_{LPM4.5_AMLDO0_SVSMOFF,100\ nF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, C_{VCORE} = 100 nF	1.7	TBD	ms
$t_{LPM4.5_AMLDO0_SVSMOFF,4.7\ µF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, C_{VCORE} = 4.7 µF	TBD	TBD	ms

(1) This is the latency from WFI instruction execution by CPU to LPM3.5 mode entry.
(2) This is the latency from WFI instruction execution by CPU to LPM4.5 mode entry.
(3) This is the latency from I/O wake-up event to start of application code.

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5.10.2 Reset Timing

Table 5-15. Reset Recovery Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{SOFT}	Latency from release of soft reset to first CPU instruction fetch		5		MCLK cycles
t_{HARD}	Latency from release of hard reset to release of soft reset		25		MCLK cycles
t_{POR}	Latency from release of device POR to release of hard reset		15	25	µs
$t_{COLDPWR,100\ nF}$	Latency from a cold power-up condition to release of device POR, C_{VCORE} = 100 nF		410	1000	µs
$t_{COLDPWR,4.7\ µF}$	Latency from a cold power-up condition to release of device POR, C_{VCORE} = 4.7 µF		530	1600	µs

(1) Refer to Section 6.7.1 for details on the various classes of resets on the device

Table 5-16. External Reset (RSTn) Recovery Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{AMLDO0_RSTn,\ 16MHz}$	External reset applied on RSTn pin while the device is in AM_LDO_VCORE0 mode with MCLK = 16 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMLDO1_RSTn,\ 32MHz}$	External reset applied on RSTn pin while the device is in AM_LDO_VCORE1 mode with MCLK = 32 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMLDO1_RSTn,\ 48MHz}$	External reset applied on RSTn pin while the device is in AAM_LDO_VCORE1 mode with MCLK = 48 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMDCDC0_RSTn,\ 16MHz}$	External reset applied on RSTn pin while the device is in AM_DCDC_VCORE0 mode with MCLK = 16 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMDCDC1_RSTn,\ 48MHz}$	External reset applied on RSTn pin while the device is in AM_DCDC_VCORE1 mode with MCLK = 48 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMLF0_RSTn,\ 128kHz}$	External reset applied on RSTn pin while the device is in AM_LF_VCORE0 mode with MCLK = 128 kHz from REFO, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMLF0_RSTn,\ 32kHz}$	External reset applied on RSTn pin while the device is in AM_LF_VCORE0 mode with MCLK = 32 kHz from LFXT, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{AMLF1_RSTn,\ 128kHz}$	External reset applied on RSTn pin while the device is in AM_LF_VCORE1 mode with MCLK = 128 kHz from REFO, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM0LDO0_RSTn,\ 16MHz}$	External reset applied on RSTn pin while the device is in LPM0_LDO_VCORE0 mode with MCLK = 16 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM0LDO1_RSTn,\ 48MHz}$	External reset applied on RSTn pin while the device is in LPM0_LDO_VCORE1 mode with MCLK = 48 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM0DCDC0_RSTn,\ 16MHz}$	External reset applied on RSTn pin while the device is in LPM0_DCDC_VCORE0 mode with MCLK = 16 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM0DCDC1_RSTn,\ 48MHz}$	External reset applied on RSTn pin while the device is in LPM0_DCDC_VCORE1 mode with MCLK = 48 MHz, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM0LF0_RSTn,\ 128kHz}$	External reset applied on RSTn pin while the device is in LPM0_LF_VCORE0 mode with MCLK = 128 kHz from REFO, The latency is from release of external reset to start of application code		TBD	4	ms

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External Reset (RSTn) Recovery Latencies *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LPM0LF0_RSTn,\ 32kHz}$	External reset applied on RSTn pin while the device is in LPM0_LF_VCORE0 mode with MCLK = 32 kHz from LFXT, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM0LF1_RSTn,\ 128kHz}$	External reset applied on RSTn pin while the device is in LPM0_LF_VCORE1 mode with MCLK = 128 kHz from REFO, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM3_LPM4_VCORE0_RSTn}$	External reset applied on RSTn pin while the device is in LPM3 or LPM4 modes at VCORE0, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM3_LPM4_VCORE1_RSTn}$	External reset applied on RSTn pin while the device is in LPM3 or LPM4 modes at VCORE1, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM3.5_RSTn}$	External reset applied on RSTn pin while the device is in LPM3.5 mode, The latency is from release of external reset to start of application code		TBD	4	ms
$t_{LPM4.5_RSTn}$	External reset applied on RSTn pin while the device is in LPM4.5 mode, The latency is from release of external reset to start of application code		TBD	4	ms

5.10.3 Clock Specifications

Table 5-17. Low-Frequency Crystal Oscillator, LFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal equivalent series resistance	f_{OSC} = 32.768 kHz	16	40	65	kΩ
C_{LFXT}	Capacitance from LFXT input to ground and from LFXT output to ground(1)		7.4	12	24	pF
C_{SHUNT}	Crystal shunt capacitance		0.6	0.8	1.6	pF
C_m	Crystal motional capacitance		1	2	10	fF

(1) Does not include board parasitics. Package and board will add additional capacitance to C_{LFXT}.

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Table 5-18. Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC,LFXT}$	Current consumption(1)	f_{OSC} = 32.768 kHz LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF Typical ESR, C_{SHUNT}	3.0 V		100		nA
		f_{OSC} = 32.768 kHz LFXTBYPASS = 0, LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF Typical ESR, C_{SHUNT}	3.0 V		200		
		f_{OSC} = 32.768 kHz LFXTBYPASS = 0, LFXTDRIVE = {2}, $C_{L,eff}$ = 9 pF, Typical ESR, C_{SHUNT}	3.0 V		300		
		f_{OSC} = 32.768 kHz LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR, C_{SHUNT}	3.0 V		500		
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0(2)			32.768		kHz
DC_{LFXT}	LFXT oscillator duty cycle	f_{LFXT} = 32.768 kHz(2)		30%		70%	
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1(3) (4)		10	32.768	50	kHz
$DC_{LFXT,SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA_{LFXT}	Oscillation allowance for LF crystals(5)	LFXTBYPASS = 0, LFXTDRIVE = {1}, f_{LFXT} = 32.768 kHz, $C_{L,eff}$ = 6 pF			TBD		kΩ
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32.768 kHz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance(6) (7)				1		pF
$t_{START,LFXT}$	Start-up time(8)	f_{OSC} = 32.768 kHz LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF Typical ESR, C_{SHUNT} FCNTLF_EN = 0(2)	3.0 V		0.6		s
		f_{OSC} = 32.768 kHz LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF Typical ESR, C_{SHUNT} FCNTLF_EN = 0(2)			2		
$f_{Fault,LFXT}$	Oscillator fault frequency(9) (10)			1		8	kHz

(1) Total current measured on both AVCC and DVCC supplies.
(2) Measured at ACLK pin.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF.
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF.
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
(7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 3.7 pF, 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF. Because the PCB adds additional capacitance, it must be considered, and TI recommends verifying proper oscillator performance.
(8) Does not include programmable startup counter.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition will set the fault flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-19. High-Frequency Crystal Oscillator, HFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal Equivalent Series Resistance	f_{OSC} = 1 MHz to ≤ 4 MHz		75	150	Ω
		f_{OSC} = > 4 MHz to ≤ 8 MHz		75	150	
		f_{OSC} = > 8 MHz to ≤ 16 MHz		40	80	
		f_{OSC} = > 16 MHz to ≤ 24 MHz		30	60	
		f_{OSC} = > 24 MHz to ≤ 32 MHz		20	40	
		f_{OSC} = > 32 MHz to ≤ 48 MHz		15	30	
C_{HFXT}	Capacitance from HFXT input to ground and from HFXT output to ground.	f_{OSC} = 1 MHz to 48 MHz	28	32	36	pF
C_{SHUNT}	Crystal shunt capacitance	f_{OSC} = 1 MHz to 48 MHz	1	3	7	pF
C_m	Crystal motional capacitance	f_{OSC} = 1 MHz to 48 MHz	3	7	30	fF

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Table 5-20. High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC,HFXT}$	HFXT oscillator crystal current HF mode at typical ESR	f_{OSC} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}	3.0 V		40		µA
		f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			60		
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			120		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			200		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			260		
		f_{OSC} = 32 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			330		
		f_{OSC} = 40 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			460		
		f_{OSC} = 48 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT}			530		
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 0 (1)		1		4	MHz
		HFXTBYPASS = 0, HFFREQ = 1 (1)		4.01		8	
		HFXTBYPASS = 0, HFFREQ = 2 (1)		8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3 (1)		16.01		24	
		HFXTBYPASS = 0, HFFREQ = 4 (1)		24.01		32	
		HFXTBYPASS = 0, HFFREQ = 5 (1)		32.01		40	
		HFXTBYPASS = 0, HFFREQ = 6 (1)		40.01		48	
DC_{HFXT}	HFXT oscillator duty cycle	Measured at MCLK or HSMCLK. f_{HFXT} = 1 MHz - 48 MHz		40%	50%	60%	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1 (2) (1)		0.8		48	MHz

(1) Maximum frequency of operation of the entire device cannot be exceeded.
(2) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.

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High-Frequency Crystal Oscillator, HFXT *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$DC_{HFXT,SW}$	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1 External clock used as a direct source to MCLK or HSMCLK with no divider (DIVM = 0 or DIVHS = 0).		45%		55%	
		HFXTBYPASS = 1 External clock used as a direct source to MCLK or HSMCLK with divider (DIVM > 0 or DIVHS > 0) or not used as a direct source to MCLK or HSMCLK.		40%		60%	
OA_{HFXT}	Oscillation allowance for HFXT crystals(3)	HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0 $f_{HFXT,HF}$ = 1 MHz, $C_{L,eff}$ = 16 pF			5000		Ω
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0 $f_{HFXT,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF			1250		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1 $f_{HFXT,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF			750		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2 $f_{HFXT,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF			425		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3 $f_{HFXT,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF			275		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4 $f_{HFXT,HF}$ = 32 MHz, $C_{L,eff}$ = 16 pF			225		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5 $f_{HFXT,HF}$ = 40 MHz, $C_{L,eff}$ = 16 pF			160		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6 $f_{HFXT,HF}$ = 48 MHz, $C_{L,eff}$ = 16 pF			140		

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(3) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

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High-Frequency Crystal Oscillator, HFXT *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,HFXT}$	Start-up time(4)	f_{OSC} = 1 MHz HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0	3.0 V		3.57		ms
		f_{OSC} = 4 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			0.89		
		f_{OSC} = 8 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			0.66		
		f_{OSC} = 16 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			0.53		
		f_{OSC} = 24 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			470		µs
		f_{OSC} = 32 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			435		
		f_{OSC} = 40 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			425		
		f_{OSC} = 48 MHz HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6 $C_{L,eff}$ = 16 pF Typical ESR , C_{SHUNT} FCNTHF_EN = 0			420		
$C_{L,eff}$	Integrated effective load capacitance(5) (6)				1		pF
$f_{Fault,HFXT}$	Oscillator fault frequency(7) (8)			400		700	kHz

(4) Does not include programable startup counter.
(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, TI recommeds verifying the correct load by measuring the oscillator frequency through MCLK or SMCLK. For a correct setup, the effective load capacitance should always match the specification of the crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
(7) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX might set the flag. A static condition or stuck at fault condition will set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-21. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} , T_A	MIN	TYP	MAX	UNIT
f_{RSEL0_CTR}	DCO frequency center range 0 initial accuracy , with trimmed factory settings	Internal resistor option DCORSEL = 0, DCOTUNE = 0	3.0 V 25°C	1.4925	1.5	1.5075	MHz
		External resistor option DCORSEL = 0, DCOTUNE = 0	3.0 V 25°C	1.4925	1.5	1.5075	
f_{RSEL1_CTR}	DCO frequency center range 1 initial accuracy , with trimmed factory settings	Internal resistor option DCORSEL = 1, DCOTUNE = 0	3.0 V 25°C	2.985	3	3.015	MHz
		External resistor option DCORSEL = 1, DCOTUNE = 0	3.0 V 25°C	2.985	3	3.015	
f_{RSEL2_CTR}	DCO frequency center range 2 initial accuracy , with trimmed factory settings	Internal resistor option DCORSEL = 2, DCOTUNE = 0	3.0 V 25°C	5.97	6	6.03	MHz
		External resistor option DCORSEL = 2, DCOTUNE = 0	3.0 V 25°C	5.97	6	6.03	
f_{RSEL3_CTR}	DCO frequency center range 3 initial accuracy , with trimmed factory settings	Internal resistor option DCORSEL = 3, DCOTUNE = 0	3.0 V 25°C	11.94	12	12.06	MHz
		External resistor option DCORSEL = 3, DCOTUNE = 0	3.0 V 25°C	11.94	12	12.06	
f_{RSEL4_CTR}	DCO frequency center range 4 initial accuracy , with trimmed factory settings	Internal resistor option DCORSEL = 4, DCOTUNE = 0	3.0 V 25°C	23.88	24	24.12	MHz
		External resistor option DCORSEL = 4, DCOTUNE = 0	3.0 V 25°C	23.88	24	24.12	
f_{RSEL5_CTR}	DCO frequency center range 5 initial accuracy , with trimmed factory settings	Internal resistor option DCORSEL = 5, DCOTUNE = 0	3.0 V 25°C	47.76	48	48.24	MHz
		External resistor option DCORSEL = 5, DCOTUNE = 0	3.0 V 25°C	47.76	48	48.24	
df_{DCO}/dT (1)	DCO frequency drift with temperature	Internal resistor option At fixed voltage.	1.62 V to 3.7 V	–250		250	ppm/°C
		External resistor option (2) At fixed voltage.	1.62 V to 3.7 V	–35		35	
df_{DCO}/dV_{CC}	DCO frequency voltage drift with voltage	At fixed temperature.	–40°C to 85 °C	–0.10		0.10	%/V
f_{RSEL0}	DCO frequency range 0	DCORSEL = 0, DCOTUNE = value **TBD** in the negative scale to value **TBD** in the positive scale	1.62 V to 3.7 V –40°C to 85°C	0.98		2.7	MHz
f_{RSEL1}	DCO frequency range 1	DCORSEL = 1, DCOTUNE = value **TBD** in the negative scale to value **TBD** in the positive scale	1.62 V to 3.7 V –40°C to 85°C	1.96		5.4	MHz
f_{RSEL2}	DCO frequency range 2	DCORSEL = 2, DCOTUNE = value **TBD** in the negative scale to value **TBD** in the positive scale	1.62 V to 3.7 V –40°C to 85°C	3.92		10.8	MHz
f_{RSEL3}	DCO frequency range 3	DCORSEL = 3, DCOTUNE = value **TBD** in the negative scale to value **TBD** in the positive scale	1.62 V to 3.7 V –40°C to 85°C	7.84		21.6	MHz
f_{RSEL4}	DCO frequency range 4	DCORSEL = 4, DCOTUNE = value **TBD** in the negative scale to value **TBD** in the positive scale	1.62 V to 3.7 V –40°C to 85°C	15.68		43.2	MHz
f_{RSEL5}	DCO frequency range 5	DCORSEL = 5, DCOTUNE = value **TBD** in the negative scale to value **TBD** in the positive scale	1.62 V to 3.7 V –40°C to 85°C	31.36		86.5	MHz
f_{DCO_DC}	Duty cycle	No external divide, all DCO settings	1.62 V to 3.7 V –40°C to 85°C	48%	50%	52%	
t_{DCO_JITTER}	DCO jitter		1.62 V to 3.7 V –40°C to 85°C		120	200	ps
T_{DCO_STEP}	Step size	Step size of the DCO.	1.62 V to 3.7 V –40°C to 85°C		0.2%		

(1) Average calculated using the box method, (f_{DCO_MAX} - f_{DCO_MIN}) / (T_{MAX} - T_{MIN}).
(2) Does not include temperature coefficient of external resistor.
The recommended value of External Resistor at DCOR pin: 91kΩ, 0.1%, ±25 ppm/°C.

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DCO *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} , T_A	MIN	TYP	MAX	UNIT
$t_{DCO_SETTLE_RANGE}$	DCO settling from worst case DCORSELn to DCORSELm	DCO settled to within 0.5% of steady state frequency See Figure 5-1.	1.62 V to 3.7 V –40°C to 85°C			5	µs
$t_{DCO_SETTLE_TUNE_LSB}$	DCO settling LSB change of DCOTUNE within any DCORSEL setting	DCO settled to within 0.5% of steady state frequency See Figure 5-1.	1.62 V to 3.7 V –40°C to 85°C			2.2	µs
$t_{DCO_SETTLE_TUNE}$	DCO settling worst case DCOTUNEn to DCOTUNEm within any DCORSEL setting	DCO settled to within 0.5% of steady state frequency See Figure 5-1.	1.62 V to 3.7 V –40°C to 85°C			5	µs
$DCO_{OVERSHOOT}$	DCO overshoot	Worst case DCO frequency change See Figure 5-1.	1.62 V to 3.7 V –40°C to 85°C	–10%		5%	
t_{START}	DCO startup time(3)	DCO settled to within 0.5% of steady state frequency.	1.62 V to 3.7 V –40°C to 85°C		5		µs

(3) The maximum parasitic capacitance at the DCO External Resistance pin (DCOR) should not exceed 5pF to guarantee the specified DCO startup time.

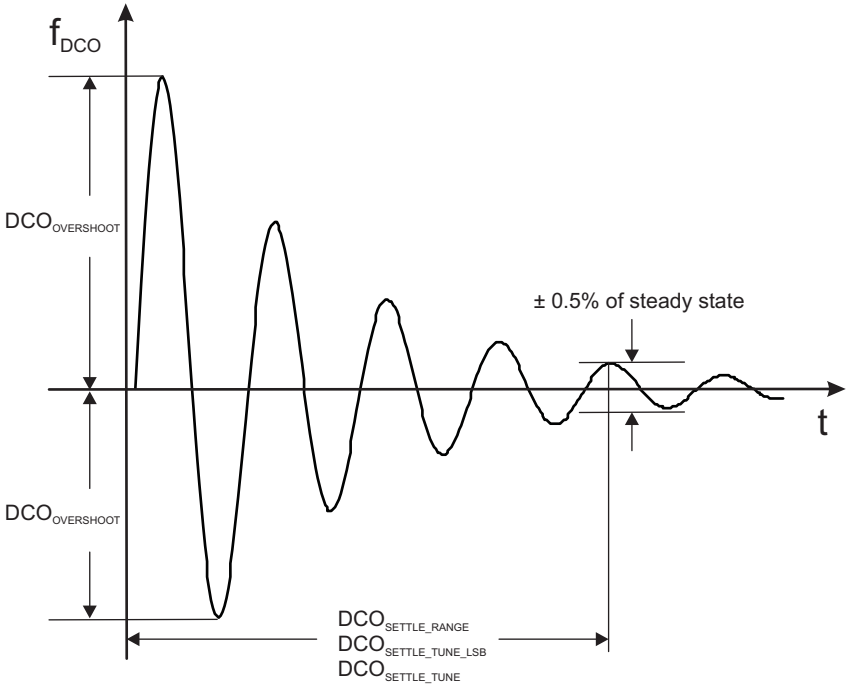


Figure 5-1. DCO Settling

Table 5-22. DCO Overall Tolerance

over operating free-air temperature range (unless otherwise noted)

RESISTOR OPTION	TEMPERATURE CHANGE	TEMPERATURE DRIFT (%)	VOLTAGE CHANGE	VOLTAGE DRIFT (%)	OVERALL DRIFT (%)	OVERALL ACCURACY (%)
Internal resistor	–40°C to 85 °C	±3.125	1.62 V to 3.7 V	±0.2	±3.325	±3.825
	0°C	0	1.62 V to 3.7 V	±0.2	±0.2	±0.7
	–40°C to 85 °C	±3.125	0 V	0	±3.125	±3.625
External resistor with 25-ppm TCR	–40°C to 85 °C	±0.438	1.62 V to 3.7 V	±0.2	±0.638	±1.138
	0°C	0	1.62 V to 3.7 V	±0.2	±0.2	±0.7
	–40°C to 85 °C	±0.438	0 V	0	±0.438	±0.938

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Table 5-23. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{VLO}	Current consumption(1)		1.62 V to 3.7 V		100		nA
f_{VLO}	VLO frequency	(2)	1.62 V to 3.7 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift(3)	(2)	1.62 V to 3.7 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(4)	(2)	1.62 V to 3.7 V		4		%/V
DC_{VLO}	Duty cycle	(2)	1.62 V to 3.7 V	40%	50%	60%	

(1) Current measured on DVCC supply
(2) Measured at ACLK pin
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-24. Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO current consumption(1)	REFOFSEL = 0	1.62 V to 3.7 V		0.6		µA
		REFOFSEL = 1	1.62 V to 3.7 V		1		
f_{REFO}	REFO frequency calibrated	REFOFSEL = 0(2)	1.62 V to 3.7 V		32.768		kHz
		REFOFSEL = 1(2)	1.62 V to 3.7 V		128		
	REFO absolute tolerance calibrated	Full temperature range REFOFSEL = 0(2)	1.62 V to 3.7 V	–3%		3%	
		Full temperature range REFOFSEL = 1(2)	1.62 V to 3.7 V	–6%		6%	
		T_A = 25°C REFOFSEL = 0,1(2)	3 V	–1.5%		1.5%	
df_{REFO}/d_T	REFO frequency temperature drift(3)	(2)	1.62 V to 3.7 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift(4)	(2)	1.62 V to 3.7 V		1.0		%/V
DC_{REFO}	REFO duty cycle	(2)	1.62 V to 3.7 V	40%	50%	60%	

(1) Total current measured on both AVCC and DVCC supplies.
(2) Measured at ACLK pin
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-25. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption(1)		1.62 V to 3.7 V		50		µA
f_{MODOSC}	MODOSC frequency		(2)1.62 V to 3.7 V	23	25	27	MHz
df_{MODOSC}/dT	MODOSC frequency temperature drift(3)	(2)	1.62 V to 3.7 V		0.017		%/°C
df_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift(4)	(2)	1.62 V to 3.7 V		0.36		%/V
DC_{MODOSC}	Duty cycle	(2)	1.62 V to 3.7 V	40%	50%	60%	

(1) Total current measured on both AVCC and DVCC supplies.
(2) Measured at SMCLK pin with divide by 2 setting for MODOSC clock.
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62V to 3.7V) – MIN(1.62V to 3.7V)) / MIN(1.62V to 3.7V) / (3.7V – 1.62V)

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Table 5-26. System Oscillator (SYSOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SYSOSC}	Current consumption (1)		1.62 V to 3.7 V		25		µA
f_{SYSOSC}	SYSOSC frequency		1.62 V to 3.7 V	4.25	5.0	5.75	MHz
df_{SYSOSC}/ dT	SYSOSC frequency temperature drift (2)		1.62 V to 3.7 V		0.03		%/°C
df_{SYSOSC}/ dVCC	SYSOSC frequency supply voltage drift (3)		1.62 V to 3.7 V		0.6		%/V
DC_{SYSOSC}	Duty cycle		1.62 V to 3.7 V	40%	50%	60%	

(1) Total current measured on both AVCC and DVCC supplies.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-27. Recommended Parts for L_{VSW}

PART NAME	VALUE	TOLERANCE	FOOTPRINT	DCR (1)	CURRENT RATING	TEMPERATURE RATING
LQM2MPN4R7NG0	4.7 µH	±30%	0806	140 mΩ ± 25%	1100 mA	–55°C to +125°C
LQM21PN4R7NGR	4.7 µH	±30%	0806	230 mΩ ± 25%	800 mA	–55°C to +125°C
LQM2HPN4R7MGC	4.7 µH	±20%	1008	180 mΩ ± 25%	800 mA	–55°C to +125°C
VLS252010ET4R7M	4.7 µH	±20%	1008	398 mΩ max	890 mA	–40°C to +105°C
VLS252010ET6R8M	6.8 µH	±20%	1008	532 mΩ max	760 mA	–40°C to +105°C
VLS252015ET100M	10 µH	±20%	1008	588 mΩ max	800 mA	–40°C to +105°C

(1) Higher DCR will result in lower DC-DC efficiency

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5.10.4 Voltage Regulators

Table 5-28. V_{CORE} Regulator (LDO) Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CORE0-HP}$	Static VCORE voltage Level 0 in active and LPM0 modes	Device power modes AM_LDO_VCORE0, LPM0_LDO_VCORE0	1.07	1.2	1.27	V
$V_{CORE1-HP}$	Static VCORE voltage Level 1 in active and LPM0 modes	Device power modes AM_LDO_VCORE1, LPM0_LDO_VCORE1	1.25	1.4	1.48	V
$V_{CORE0-LF}$	Static VCORE voltage Level 0 in low-frequency active and low frequency LPM0 modes	Device power modes AM_LF_VCORE0	1.07	1.2	1.27	V
$V_{CORE1-LF}$	Static VCORE voltage Level 1 in low-frequency active and low frequency LPM0 modes	Device power modes AM_LF_VCORE1	1.25	1.4	1.48	V
$V_{CORE0-LPM34}$	Static VCORE voltage Level 0 in LPM3 and LPM4 modes	Device power modes LPM3, LPM4	0.98	1.2	1.31	V
$V_{CORE1-LPM34}$	Static VCORE voltage Level 1 in LPM3 and LPM4 modes	Device power modes LPM3, LPM4	1.14	1.4	1.52	V
$V_{CORE0-LPM35}$	Static VCORE voltage Level 0 in LPM3.5 mode	Device power mode LPM3.5	0.98	1.2	1.31	V
$I_{INRUSH-ST}$	Inrush current at startup	Device power-up			200	mA
$I_{PEAK-LDO}$	Peak current drawn by LDO from DV_{CC}	Highest peak current expected during TBD			350	mA
T_{LPMLDO_RDY}	Time taken by LPM LDO (LDO in LPM3, LPM4, or LPM3.5) to get ready after a cold powerup or LPM4.5, before it may be enabled.(1)				650	µs
$I_{SC-coreLDO}$	Short circuit current limit for core LDO	Measured when output is shorted to ground			350	mA

(1) If LPM LDO is attempted to be enabled before this time, the active mode LDO automatically remains ON at the expense of system power to allow the SOC operations to continue smoothly.

Table 5-29. V_{CORE} Regulator (DC-DC) Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC-DCDC}$	Allowed DV_{CC} range for DC-DC operation		2.0		3.7	V
$V_{CORE0-DCDC}$	Static VCORE voltage Level 0 in DC-DC high-performance modes	Device power modes AM_DCDC_VCORE0, LPM0_DCDC_VCORE0	1.07	1.2	1.27	V
$V_{CORE1-DCDC}$	Static VCORE voltage Level 1 in DC-DC high-performance modes	Device power modes AM_DCDC_VCORE1, LPM0_DCDC_VCORE1	1.25	1.4	1.48	V
$I_{PEAK-DCDC}$	Peak current drawn by DC-DC from DVCC				500	mA
$I_{SC-DCDC}$	Short circuit current limit for DC-DC	Measured when output is shorted to ground			700	mA

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Table 5-30. PSS, VCCDET

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCC_VCCDET-}$	VCCDET power-down level - trip point with falling V_{CC}	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s (1)	0.64	1.1	1.62	V
$V_{VCC_VCCDET+}$	VCCDET power-up level - trip point with rising V_{CC}	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s (1)	0.70	1.165	1.65	V
$V_{VCC_VCC_hys}$	VCCDET hysteresis		40	65	100	mV

(1) The VCCDET levels are measured with a slow-changing supply. Faster slopes can result in different levels.

Table 5-31. PSS, SVSMH

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SVSMH}	$SVSM_H$ leakage current consumption, power down	SVSMHOFF = 1		0.05	15	nA
	$SVSM_H$ current consumption, low-power mode	SVSMHOFF = 0, SVSMHLP = 1		300	500	
	$SVSM_H$ current consumption, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0		4.5	8	µA
$V_{SVSMH+,ST}$	$SVSM_H$ threshold level during start up [(rising DV_{CC})	*untrimmed (at initial powerup),* DC (dDV_{CC}/dt < 1V/s)	1.47	1.565	1.65	V
$V_{SVSMH-,HP}$	$SVSM_H$ threshold level during high-performance mode (falling DV_{CC})	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.54	1.58	1.62	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.57	1.61	1.65	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.0	2.05	2.12	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.2	2.25	2.32	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.4	2.46	2.54	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.7	2.77	2.86	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.92	3.0	3.1	
$V_{SVSMH+,HP}$	$SVSM_H$ threshold level; High Performance Mode [rising DV_{CC}]	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.555	1.595	1.635	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.585	1.625	1.665	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.605	1.655	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.015	2.065	2.12	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.215	2.265	2.32	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.415	2.475	2.54	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.715	2.785	2.86	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.935	3.015	3.1	

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PSS, SVSMH *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SVSMH-,LP}$	$SVSM_H$ threshold level; Low Power Mode [falling DV_{CC}]	SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.47	1.54	1.62	V
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.5	1.57	1.65	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s) *trimmed*	1.55	1.62	1.71	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2	2.09	2.18	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.2	2.3	2.4	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.4	2.51	2.62	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.7	2.82	2.94	
		SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s) *trimmed*	2.87	3.0	3.13	
V_{SVSMH_hys}	$SVSM_H$ hysteresis			15		mV
$t_{PD,SVSMH}$	SVS_H propagation delay, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0, very fast dV_{DVCC}/dt		2	10	µs
	SVS_H propagation delay, low-power mode	SVSMHOFF = 0, SVSMHLP = 1, very fast dV_{DVCC}/dt		15	100	
$t_{(SVSMH)}$	$SVSM_H$ on or off delay time	SVSMHOFF = 1 → 0 SVSMHLP = 0 (1)		17	40	µs

(1) If the SVSMH is kept disabled in active mode and is enabled before entering a low-power mode of the device (LPM3, LPM4, LPM3.5, or LPM4.5) care should be taken that sufficient time has elapsed since enabling of the module before entry into the device low-power mode to allow for successful wakeup of SVSMH module as per the SVSMH on or off delay time specification. Otherwise, SVSMH may trip, causing device to get a Reset & wakeup from the Low Power Mode.

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Table 5-32. PSS, SVSL

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SVSL,leak}$	SVS_L leakage current consumption, power down	SVSLOFF = 1		0.1	10	nA
$I_{SVSL-DVCC,LP}$	SVS_L current consumption, low-power mode, from DV_{CC}	SVSLOFF = 0, SVSLLP = 1		110	200	nA
$I_{SVSL-VCORE,LP}$	SVS_L current consumption, low-power mode, from V_{CORE}			95	200	
$I_{SVSL-DVCC,HP}$	SVS_L current consumption, high-performance mode, from DV_{CC}	SVSLOFF = 0, SVSLLP = 0		1.5	2	µA
$I_{SVSL-VCORE,HP}$	SVS_L current consumption, high-performance mode, from V_{CORE}			1.5	3	
$t_{PD,SVSL,\ AM}$	SVS_L propagation delay, high-performance mode	SVSLOFF = 0, SVSLLP = 0, very fast dV_{VCORE}/dt		2	10	µs
	SVS_L propagation delay, low-power mode	SVSLOFF = 0, SVSLLP = 1, very fast dV_{VCORE}/dt		16	100	
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLOFF = 0 → 1, SVSLLP = 0		16	40	µs

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5.10.5 Digital I/Os

Table 5-33. Digital Inputs (Applies to Both Normal and High-Drive I/Os)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	0.99		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.21	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2.2 V	0.32		0.84	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins shared with analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg,ndio}$	Normal I/O high-impedance input leakage current (refer also to and)	(1) (2)	2.2 V, 3 V	–20		+20	nA
$I_{lkg,hdio}$	High-drive I/O high-impedance input leakage current (refer also to and)	(1) (2)	2.2 V, 3 V	–20		+20	nA
t_{int}	External interrupt timing (external trigger pulse duration to set interrupt flag)(3)	Ports with interrupt capability and without glitch filter	2.2 V, 3 V	20			ns
		Ports with interrupt capability and with glitch filter but glitch filter disabled (GLTFLT_EN = 0)	2.2 V, 3 V	20			ns
		Ports with interrupt capability and with glitch filter, Glitch filter enabled (GLTFTL_EN = 1)	2.2 V, 3 V	2			µs
t_{RST}	External reset pulse duration on RSTn pin(4)		2.2 V, 3 V	2			µs

(1) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_{int} is met. It may be set by trigger signals shorter than t_{int}.
(4) Not applicable if RSTn/NMI pin configured as NMI.

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Table 5-34. Digital Outputs, Normal I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(1)	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with RC load)(3)	VCORE = 1.4 V, C_L = 20 pF, R_L (4) (5)	1.62 V	20		MHz
			2.2 V	24		
			3.0 V	24		
$d_{Px.y}$	Port output duty cycle (with RC Load)	VCORE = 1.4 V, C_L = 20 pF, R_L (4) (5)	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency(3)	VCORE = 1.4 V, C_L = 20 pF(5)	1.62 V	20		MHz
			2.2 V	24		
			3.0 V	24		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.4 V, C_L = 20 pF(5)	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit - it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 3.2kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 20% and 80% V_{CC} at the specified toggle frequency.
(6) Measured between 20% of V_{CC} to 80% of V_{CC}.
(7) Measured between 80% of V_{CC} to 20% of V_{CC}.

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Table 5-35. Digital Outputs, High-Drive I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –5 mA(1)	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –10 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –20 mA(2)		V_{CC} – 0.30	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 5 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 10 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 20 mA(2)		V_{SS}	V_{SS} + 0.30	
$f_{Px.y}$	Port output frequency (with RC load)(3)	VCORE = 1.4 V, C_L = 20 pF, R_L (4) (5)	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
$d_{Px.y}$	Port output duty cycle (with RC Load)	VCORE = 1.4 V, C_L = 20 pF, R_L (4) (5)	1.62 V	40%	60%	
			2.2 V	45%	55%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency(3)	VCORE = 1.4 V, C_L = 20 pF(5)	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.4 V, C_L = 20 pF(5)	1.62 V	40%	60%	
			2.2 V	45%	55%	
			3.0 V	45%	55%	
t_{rise}	Port output rise time	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
t_{fall}	Port output fall time	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit - it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 3.2kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 20% and 80% V_{CC} at the specified toggle frequency.
(6) Measured between 20% of V_{CC} to 80% of V_{CC}.
(7) Measured between 80% of V_{CC} to 20% of V_{CC}.

Table 5-36. Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{Px.y}$	Pin-Oscillator Frequency	Px.y, C_L = 10 pF(1)	3.0 V		2000		kHz
		Px.y, C_L = 20 pF(1)	3.0 V		1300		kHz

(1) CL is the external load capacitance connected from the output to VSS and includes all parasitic effects such as PCB traces.

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5.10.6 14-Bit ADC

Table 5-37. 14-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 2		1.62		3.7	V
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 0		1.8		3.7	V
V(Ax)	Analog input voltage range(1)	All ADC14 analog input pins Ax		0		AVCC	V
I(ADC14) single-ended mode	Operating supply current into AVCC plus DVCC terminal(2)	$f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 1110(3), REFON = 0, ADC14SHT0x = 0, ADC14SHT1x = 0	3.0 V		375	TBD	µA
			2.2 V		355	TBD	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 1110(3), REFON = 0, ADC14SHT0x = 0, ADC14SHT1x = 0	3.0 V		175	TBD	
			2.2 V		170	TBD	
I(ADC14) differential mode	Operating supply current into AVCC plus DVCC terminal(2)	$f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 1110(3), REFON = 0, ADC14SHT0x = 0, ADC14SHT1x = 0	3.0 V		535	TBD	µA
			2.2 V		495	TBD	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 1110(3), REFON = 0, ADC14SHT0x = 0, ADC14SHT1x = 0	3.0 V		215	TBD	
			2.2 V		210	TBD	
	Resolution				14		bits
C_I	Input capacitance into a single terminal				10	15	pF
R_I	Input MUX ON-resistance	0 V ≤ V(Ax)≤ AVCC	1.8V - 3.7V		0.135	1	kΩ
			1.62V - 1.8V		0.15	1.5	kΩ

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter I(ADC14).
(3) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 1110.

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Table 5-38. 14-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC14CLK}$	For specified performance of ADC14 linearity parameters	1 Msps, ADC14PWRMD = 0	1.8 V to 3.7 V		25		MHz
		200 ksps, ADC14PWRMD = 2	1.62 V to 3.7 V		5		
$N_{CONVERT}$	Clock cycles for conversion	ADC14RES = 11			16		cycles
		ADC14RES = 10			14		
		ADC14RES = 01			11		
		ADC14RES = 00			9		
$t_{ADC14ON}$	Turnon settling time of the ADC	See (1)				100	ns
t_{Sample}	Sampling time(2)	R_S = 200 Ω, C_S = 10pF		0.215			µs

(1) The condition is that the error in a conversion started after $t_{ADC14ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(2) Sampling time should be at-least 4x $1/f_{ADC14CLK}$.

Table 5-39. 14-Bit ADC, Linearity Parameters, LDO Operation

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SINAD	With single-ended input	1Msps, ADC14DIF = 0, ADC14VRSEL = 1110(1), 2.5-V reference, 20-kHz input sine	1.8 V to 3.7 V	*TBD*	75		dB
	With differential input	1Msps, ADC14DIF = 1, ADC14VRSEL = 1110(1), 2.5-V reference, 20-kHz input sine	1.8 V to 3.7 V	*TBD*	80		
ENOB	With single-ended input	1Msps, ADC14DIF = 0, ADC14VRSEL = 1110(1), 2.5-V reference, 20-kHz input sine	1.8 V to 3.7 V	*TBD*	12.1		bit
	With differential input	1Msps, ADC14DIF = 1, ADC14VRSEL = 1110(1), 2.5-V reference, 20-kHz input sine	1.8 V to 3.7 V	*TBD*	13		
E_I	Integral linearity error (INL)	1.45 V≤ V_{R+} - V_{R-}≤ AVCC		–2.0		2.0	LSB
		1.2 V < V_{R+} - V_{R-}< 1.45		TBD		TBD	
E_D	Differential linearity error (DNL)			–0.99		1.0	LSB
E_O	Offset error			–0.7	±0.35	0.7	mV
E_G	Gain error			–2.0	±1	2.0	LSB
E_T	Total unadjusted error			–10	±TBD	10	LSB

(1) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 1110.

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Table 5-40. 14-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1) (2)	ADC14ON = 1, ADC14TCMAP = 1, T_A = 0°C			730		mV
TC_{SENSOR}	See (2)	ADC14ON = 1, ADC14TCMAP = 1			1.9		mV/°C
$t_{SENSOR(sample)}$	Sample time required if ADCTCMAP = 1 and channel MAX-1 is selected(3)	ADC14ON = 1, ADC14TCMAP = 1, Error of conversion result ≤ 1 LSB		5			µs
$V_{1/2}$	AVCC voltage divider for ADC14BATMAP = 1 on MAX input channel	ADC14ON = 1, ADC14BATMAP = 1		48%	50%	52%	
$t_{V\ 1/2\ (sample)}$	Sample time required if ADC14BATMAP = 1 and channel MAX is selected(4)	ADC14ON = 1, ADC14BMAP = 1		1			µs

(1) The temperature sensor offset can be as much as ±20°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The TLV structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (Temperature,°C) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V\ 1/2\ (sample)}$. No additional on time is needed.

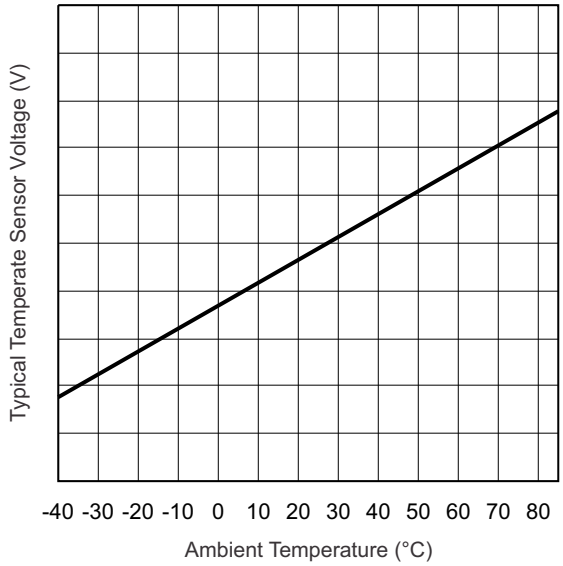


Figure 5-2. Typical Temperature Sensor Voltage

Table 5-41. 14-Bit ADC, Internal Reference Buffers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REF+}	Operating supply current into AVCC terminal(1)	ADC ON, REFOUT = 0, ADC14PWRMD = 0, REFVSEL = {0, 1, 3}	3 V		600	1000	µA
		ADC ON, REFOUT = 0, ADC14PWRMD = 2, REFVSEL = {0, 1, 3}	3 V		200	360	
		ADC ON, REFOUT = 1, ADC14PWRMD = 2, REFVSEL = {0, 1, 3}	3 V		560	870	
t_{on}	Time to turn on		3V			5	µs

(1) The internal reference current is supplied via terminal AV_{CC}.

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Table 5-42. 14-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{eREF-}$ (1)	1.45		AV_{CC}	V
V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{eREF-}$ (2)	0		AV_{CC} – 1.45	V
(V_{eREF+} - V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{eREF-}$ (3)	1.45		AV_{CC}	V
I_{VeREF+} I_{VeREF-}	Static input current single ended input mode	1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 25 MHz, ADC14SHTx = 1h, ADC14DIF = 0, Conversion rate 1 Msps	–45		45	uA
		1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 5 MHz, ADC14SHTx = 1h, ADC14DIF = 0, Conversion rate 200 ksps	–9		9	µA
I_{VeREF+} I_{VeREF-}	Static input current differential input mode	1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 25 MHz, ADC14SHTx = 1h, ADC14DIF = 1, Conversion rate 1Msps	–90		90	uA
		1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC14CLK}$ = 5 MHz, ADC14SHTx = 1h, ADC14DIF = 1 Conversion rate 200ksps	–18		18	uA
I_{VeREF+}	Peak input current single ended input mode	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC14DIF = 0			TBD	mA
I_{VeREF+}	Peak input current differential input mode	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC14DIF = 1			TBD	mA
$C_{VeREF±}$	Capacitance at VeREF± terminal		(4)5			µF
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC\ (min)}$ – $AV_{CC(max)}$ T_A = 25°C			TBD	µV/V
PSRR_AC	Power supply rejection ratio (AC)	dAV_{CC} = 0.1V at 1 kHz		TBD		mV/V

(1) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels down to 1.2 V may be applied with reduced accuracy requirements for DNL, INL and SNR at 1 Msps or for ≤500-ksps specified accuracy can still be achieved.
(2) The accuracy limits the maximum negative external reference voltage. For 1-Msps, higher reference voltage levels up to AVCC – 1.2 V may be applied with reduced speed and accuracy, or for ≤500 ksps, specified accuracy can still be achieved.
(3) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(4) Two decoupling capacitors, 5 µF and 50 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC14. See also the *MSP432P4xx Family Technical Reference Manual* (SLAU356).

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5.10.7 REF_A

Table 5-43. REF_A, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {0} for 1.2 V REFON = 1	1.62 V		1.2	±1%	V
		REFVSEL = {1} for 1.45 V REFON = 1	1.75 V		1.45	±1%	
		REFVSEL = {2} for 2.0 V REFON = 1	2.3 V		2.0	±1%	
		REFVSEL = {3} for 2.5 V REFON = 1	2.8 V		2.5	±1%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.62			V
		REFVSEL = {1} for 1.45 V		1.75			
		REFVSEL = {2} for 2.0 V		2.3			
		REFVSEL = {3} for 2.5 V		2.8			
I_{REF+}	Operating supply current into AVCC terminal (1)	REFON = 1	3 V		12	20	µA
$I_{L(VREF+)}$	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2, 3}, I(VREF+) = +10 µA/–1000 µA, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1				2500	µV/mA
$C_{VREF±}$	Capacitance at VREF+, VREF- terminals	REFON = REFOUT = 1		0		100	pF
$PSRR_DC_{REFOUT0}$	Power supply rejection ratio (DC) after ADC buffer	AVCC = AVCC(min) for each reference level, REFVSEL = {0,1,2, 3}, REFON = 1, REFOUT = 0			120	300	µV/V
$PSRR_DC_{REFOUT1}$	Power supply rejection ratio (DC) after ADC buffer	AVCC = AVCC(min) for each reference level, REFVSEL = {0,1,2, 3}, REFON = 1, REFOUT = 1			50	100	µV/V
$PSRR_AC_{REFOUT0}$	Power supply rejection ratio (AC) after ADC buffer	AVCC = AVCC(min) for each reference level, dAVCC = 0.1V at 1 kHz, REFVSEL = {0,1,2, 3}, REFON = 1, REFOUT = 0			6.4	10	mV/V
$PSRR_AC_{REFOUT1}$	Power supply rejection ratio (AC) after ADC buffer	AVCC = AVCC(min) for each reference level, dAVCC = 0.1V at 1 kHz, REFVSEL = {0,1,2, 3}, REFON = 1, REFOUT = 1			2	5	mV/V
TC_{REF+} (2)	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2, 3}, REFON = 1, T_A = –40°C to 85°C			<10	20	ppm/°C
TC_{REF+} (2)	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2, 3}, REFON = 1, T_A = 0°C to 50°C			<5	15	ppm/°C
t_{SETTLE}	Settling time of reference voltage (3)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$ REFVSEL = {0, 1, 2, 3}, REFON = 0 → 1			75	90	µs

(1) The internal reference current is supplied from terminal AVCC.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(3) The condition is that the error in a ADC conversion started after t_{SETTLE} is less than ±0.5 LSB.

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5.10.8 Comparator_E

Table 5-44. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VCC	Supply voltage			1.62		3.7	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CMPPWRMD = 00, CMPON = 1, CMPRSx = 00 (fast)	2.2 V, 3 V		11	15	µA
		CMPPWRMD = 01, CMPON = 1, CMPRSx = 00 (medium)	2.2 V, 3 V		6.5	10	
		CMPPWRMD = 10, CMPON = 1, CMPRSx = 00 (slow), TA = 30°C	2.2 V, 3 V			0.5	
		CMPPWRMD = 10, CMPON = 1, CMPRSx = 00 (slow), T_A = 85°C	2.2 V, 3 V			1.2	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Includes REF_A module current	CMPREFACC = 0, CMPREFLx = 01, CMPRSx = 10, REFON = 0, CMPON = 0	2.2 V, 3 V		15	26	µA
		CMPREFACC = 1, CMPREFLx = 01, CMPRSx = 10, REFON = 0, CMPON = 0	2.2 V, 3 V		7	10	
V_{REF}	Reference voltage level	CMPRSx = 11, CMPREFLx = 01, CMPREFACC = 0	1.62 V	1.17	1.2	1.23	V
		CMPRSx = 11, CMPREFLx = 10, CMPREFACC = 0	2.2 V	1.95	2.0	2.05	
		CMPRSx = 11, CMPREFLx = 11, CMPREFACC = 0	2.7 V	2.40	2.5	2.60	
		CMPRSx = 11, CMPREFLx = 01, CMPREFACC = 1	1.62 V	1.10	1.2	1.23	
		CMPRSx = 11, CMPREFLx = 10, CMPREFACC = 1	2.2 V	1.90	2.0	2.05	
		CMPRSx = 11, CMPREFLx = 11, CMPREFACC = 1	2.7 V	2.4	2.5	2.6	
V_{IC}	Common mode input range			0		VCC–1	V
V_{OFFSET}	Input offset voltage	CMPPWRMD = 00		–10		+10	mV
		CMPPWRMD = 01		–20		+20	
		CMPPWRMD = 10		–20		+20	
C_{IN}	Input capacitance	CMPPWRMD = 00 or CMPPWRMD = 01			5		pF
		CMPPWRMD = 10			5		pF
R_{SIN}	Series input resistance	ON (switch closed)			2	4	kΩ
		OFF (switch opened)		50			MΩ
t_{PD}	Propagation delay, response time	CMPPWRMD = 00, CMPF = 0, Overdrive = 20 mV			150	300	ns
		CMPPWRMD = 01, CMPF = 0, Overdrive = 20 mV			200	400	
		CMPPWRMD = 10, CMPF = 0, Overdrive = 20 mV			5	10	µs
		CMPPWRMD = 00, CMPF = 0, Overdrive = 100 mV			150	300	ns
		CMPPWRMD = 01, CMPF = 0, Overdrive = 100 mV			200	400	
		CMPPWRMD = 10, CMPF = 0, Overdrive = 100 mV			5	10	µs
$t_{PD,filter}$	Propagation delay with filter active	CMPPWRMD = 00 or 01, CMPF = 1, Overdrive = 20 mV, CMPFDLY = 00			1.1	1.8	µs
		CMPPWRMD = 00 or 01, CMPF = 1, Overdrive = 20 mV, CMPFDLY = 01			1.4	2.6	
		CMPPWRMD = 00 or 01, CMPF = 1, Overdrive = 20 mV, CMPFDLY = 10			2	3.5	
		CMPPWRMD = 00 or 01, CMPF = 1, Overdrive = 20 mV, CMPFDLY = 11			3	5	

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Comparator_E *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{EN_CMP}	Comparator enable time	CMPON = 0 to CMPON = 1, CMPPWRMD = 00, VIN+, VIN- from pins, Overdrive = 20 mV			0.6	1	µs
		CMPON = 0 to CMPON = 1, CMPPWRMD = 01, VIN+, VIN- from pins, Overdrive = 20 mV			0.7	1	
		CMPON = 0 to CMPON = 1, CMPPWRMD = 10, VIN+, VIN- from pins, Overdrive = 20 mV			20	30	
$t_{EN_CMP_VREF}$	Comparator and reference ladder and reference voltage enable time	CMPON = 0 to CMPON = 1, CMPPWRMD = 00, CMPREFLx = 10, CMPRSx = 11, REFON = 0, Overdrive = 20 mV			2	3	µs
		CMPON = 0 to CMPON = 1, CMPPWRMD = 01, CMPREFLx = 10, CMPRSx = 11, REFON = 0, Overdrive = 20 mV			2	3	
		CMPON = 0 to CMPON = 1, CMPPWRMD = 10, CMPREFLx = 10, CMPRSx = 11, REFON = 0, Overdrive = 20 mV			20	30	
		CMPON = 0 to CMPON = 1, CMPPWRMD = 00, CMPREFLx = 10, CMPRSx = 10, REFON = 0, CMPREF0/1 = 0x0F, Overdrive = 20 mV			2.5	5	
		CMPON = 0 to CMPON = 1, CMPPWRMD = 01, CMPREFLx = 10, CMPRSx = 10, REFON = 0, CMPREF0/1 = 0x0F, Overdrive = 20 mV			2.5	5	
		CMPON = 0 to CMPON = 1, CMPPWRMD = 10, CMPREFLx = 10, CMPRSx = 10, REFON = 0, CMPREF0/1 = 0x0F, Overdrive = 20 mV			20	30	
$t_{EN_CMP_RL}$	Comparator and reference ladder enable time	CMPON = 0 to CMPON = 1, CMPPWRMD = 00, CMPREFLx = 10, CMPRSx = 10, REFON = 1, CMPREF0/1 = 0x0F			1	2	µs
		CMPON = 0 to CMPON = 1, CMPPWRMD = 01, CMPREFLx = 10, CMPRSx = 10, REFON = 1, CMPREF0/1 = 0x0F			1	2	
		CMPON = 0 to CMPON = 1, CMPPWRMD = 10, CMPREFLx = 10, CMPRSx = 10, REFON = 1, CMPREF0/1 = 0x0F			20	30	
V_{CMP_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n+0.9) / 32	VIN × (n+1) / 32	VIN × (n+1.1) / 32	V

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5.10.9 eUSCI

Table 5-45. eUSCI (UART Mode), Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	VCORE	VCC	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK External: UCLK Duty cycle = 50% ± 10%	1.2 V				12	MHz
			1.4 V				24	
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		1.2 V				1	MHz
			1.4 V				3	

Table 5-46. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0		10		40	ns
		UCGLITx = 1		25		90	
		UCGLITx = 2		45		140	
		UCGLITx = 3		60		190	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the max. useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-47. eUSCI (SPI Master Mode), Recommended Operating Conditions

PARAMETER		CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	SMCLK Duty cycle = 50% ± 10%	VCORE = 1.2 V				12	MHz
			VCORE = 1.4 V				24	

Table 5-48. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10			1			UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10			1			
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	1.2 V	1.62 V			90	ns
			1.4 V	3.7 V			50	
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	1.2 V	1.62 V			35	ns
			1.4 V	3.7 V			10	
$t_{SU,MI}$	SOMI input data setup time		1.2 V	1.62 V	50			ns
			1.4 V	3.7 V	25			
$t_{HD,MI}$	SOMI input data hold time		1.2 V	1.62 V	0			ns
			1.4 V	3.7 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	1.2 V	1.62 V			5	ns
			1.4 V	3.7 V			1	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	1.2 V	1.62 V	0			ns
			1.4 V	3.7 V	0			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 5-3 and Figure 5-4.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 5-3 and Figure 5-4.

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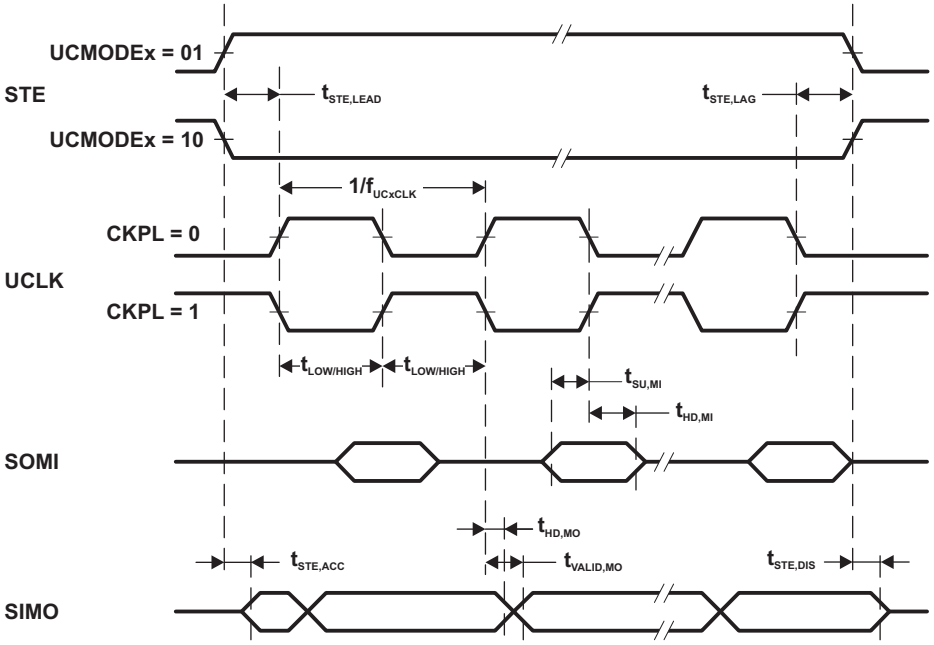


Figure 5-3. SPI Master Mode, CKPH = 0

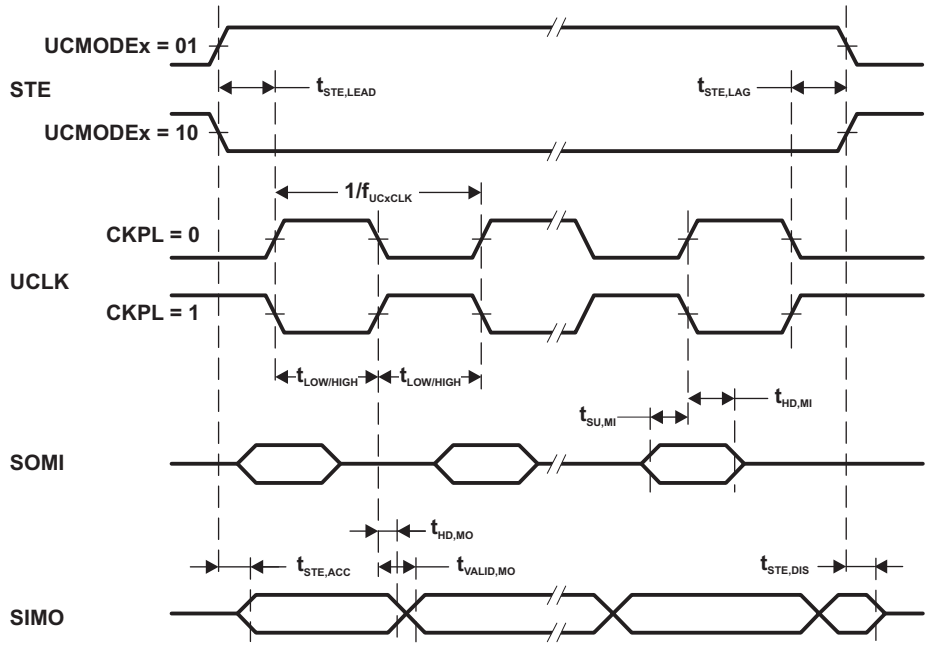


Figure 5-4. SPI Master Mode, CKPH = 1

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Table 5-49. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note (1))

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		1.2 V	1.62 V	65			ns
			1.4 V	3.7 V	45			
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		1.2 V	1.62 V	5			ns
			1.4 V	3.7 V	5			
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		1.2 V	1.62 V			90	ns
			1.4 V	3.7 V			50	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		1.2 V	1.62 V			30	ns
			1.4 V	3.7 V			10	
$t_{SU,SI}$	SIMO input data setup time		1.2 V	1.62 V	8			ns
			1.4 V	3.7 V	4			
$t_{HD,SI}$	SIMO input data hold time		1.2 V	1.62 V	7			ns
			1.4 V	3.7 V	6			
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	1.2 V	1.62 V			50	ns
			1.4 V	3.7 V			10	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	1.2 V	1.62 V	0			ns
			1.4 V	3.7 V	0			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 5-5 and Figure 5-6.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 5-5 and Figure 5-6.

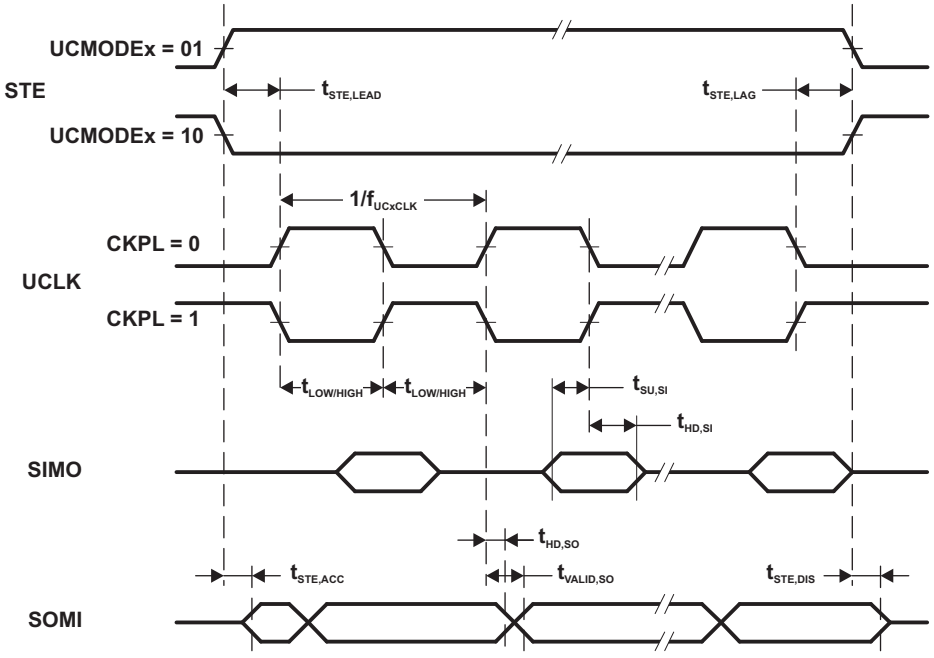


Figure 5-5. SPI Slave Mode, CKPH = 0

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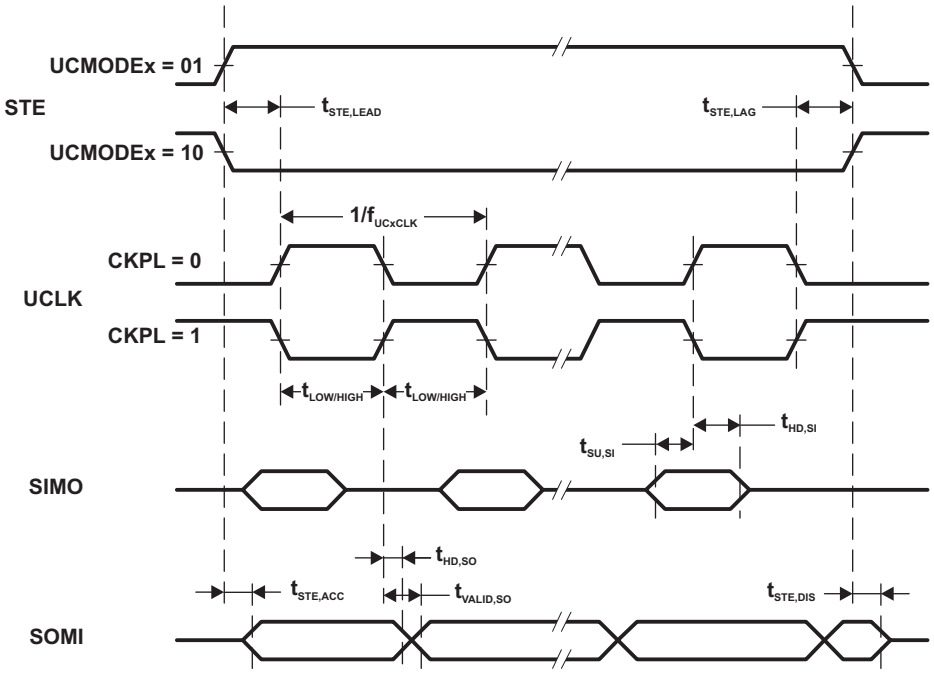


Figure 5-6. SPI Slave Mode, CKPH = 1

Table 5-50. eUSCI (I^2C Mode), Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK External: UCLK Duty cycle = 50% ± 10%	1.2 V				12	MHz
			1.4 V				24	
f_{SCL}	SCL clock frequency						1	MHz

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Table 5-51. eUSCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-7)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	5.0			µs
		f_{SCL} = 400 kHz		1.25			
		f_{SCL} = 1 MHz		500			ns
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	5.0			µs
		f_{SCL} = 400 kHz		1.25			
		f_{SCL} = 1 MHz		500			ns
$t_{HD,DAT}$	Data hold time	f_{SCL} = 100 kHz	2.2 V, 3.0 V	0			ns
		f_{SCL} = 400 kHz		0			
		f_{SCL} = 1 MHz		0			
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100 kHz	2.2 V, 3.0 V	250			ns
		f_{SCL} = 400 kHz		100			
		f_{SCL} = 1 MHz		50			
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.2 V, 3.0 V	5.0			µs
		f_{SCL} = 400 kHz		1.25			
		f_{SCL} = 1 MHz		500			ns
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.2 V, 3.0 V	60		200	ns
		UCGLITx = 1		35		110	
		UCGLITx = 2		20		65	
		UCGLITx = 3		10		45	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2.2 V, 3.0 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

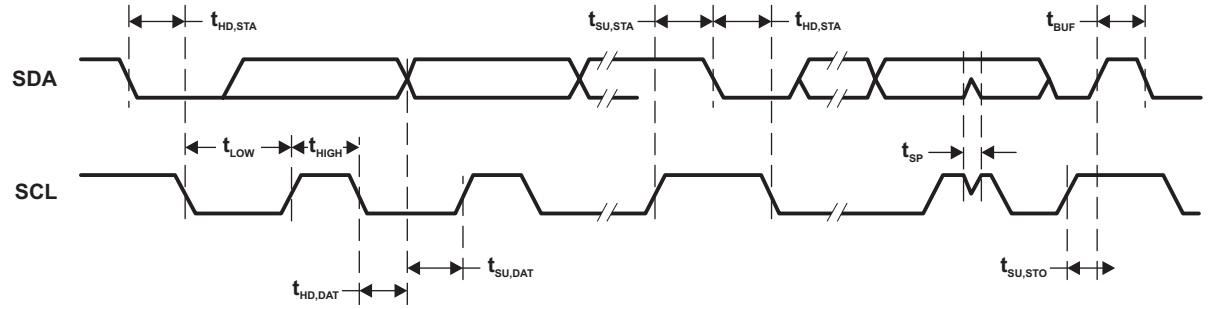


Figure 5-7. I^2C Mode Timing

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5.10.10 Timer_A

Table 5-52. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK External: TACLK Duty cycle = 50% ± 10%	1.2V				12	MHz
			1.4V				24	
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture			20			ns

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5.10.11 Memories

Table 5-53. Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DVCC_{PGM/ERS}$	Supply voltage for program or erase		1.62		3.7	V
$I_{PGM/ERS, AVG}$	Average supply current from DVCC during program or erase			TBD	35	mA
$I_{PGM/ERS, PEAK}$	Peak supply current from DVCC during program or erase				50	mA
$N_{Endurance}$	Program or erase endurance		20000			cycles
$t_{Retention}$	Data retention duration	T_J = TBD	20			years
t_{word}	Word program time without preverify (VER_PRE = 0)(1)			37	39	µs
$t_{word, ver}$	Word program time with preverify (VER_PRE = 1)(1)			62	63	µs
$t_{block, 0}$	Block program time for the first data			11	12	µs
$t_{block, 1-(N-1)}$	Block program time for each additional data, except for last data			8	9	µs
$t_{block, N}$	Block program time for the last data			13	14	µs
t_{ERS}	Segment or mass erase time			2.5	3	ms
$t_{ers2ersver}$	Erase to erase verify mode transition time			2	3	µs
$t_{nrd2ersver}$	Normal read to erase verify mode transition time			11	12	µs
$t_{pgm2pgmver}$	Program to program verify mode transition time			13.5	15	µs
$t_{nrd2pgmver}$	Normal read to program verify mode transition time			13.5	15	µs

(1) After verify enabled (VER_PST = 1).

Table 5-54. SRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SRAM_EN}	Current consumption of one SRAM bank when enabled	VCORE = 1.2 V		80		nA
		VCORE = 1.4 V		290		
I_{SRAM_RET}	Current consumption of one SRAM bank under retention	VCORE = 1.2 V		27		nA
		VCORE = 1.4 V		31		
$t_{SRAM_EN, one}$	Time taken to enable one SRAM bank			4	5	µs
$t_{SRAM_DIS, one}$	Time taken to disable one SRAM bank			4	5	µs
$t_{SRAM_EN, all}$	Time taken to enable all SRAM banks except Bank-0			7	8	µs
$t_{SRAM_DIS, all}$	Time taken to disable all SRAM banks except Bank-0			4	5	µs

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5.10.12 Emulation and Debug

Table 5-55. JTAG

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{TCK}	TCK clock frequency	0		10	MHz
t_{TCK}	TCK clock period	100			ns
t_{TCK_LOW}	TCK clock low time		$t_{TCK}/2$		ns
t_{TCK_HIGH}	TCK clock high time		$t_{TCK}/2$		ns
t_{TCK_RISE}	TCK rise time	0		10	ns
t_{TCK_FALL}	TCK fall time	0		10	ns
t_{TMS_SU}	TMS setup time to TCK rise	28			ns
t_{TMS_HLD}	TMS hold time from TCK rise	4			ns
t_{TDI_SU}	TDI setup time to TCK rise	18			ns
t_{TDI_HLD}	TDI hold time from TCK rise	4			ns
t_{TDO_ZDV}	TCK fall to data valid from high impedance		TBD	42	ns
t_{TDO_DV}	TCK fall to data valid from data valid		TBD	40	ns
t_{TDO_DVZ}	TCK fall to high impedance from data valid		TBD	33	ns

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6 Detailed Description

6.1 Processor and Execution Features

The ARM Cortex-M4 processor provides a high-performance low-cost platform that meets system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts. The Thumb-2 mixed 16- and 32-bit instruction set of the processor delivers the high performance that is expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices (typically in the range of a few kilobytes of memory needed for microcontroller-class applications).

In the MSP432P401x devices, the Cortex-M4 processor can run up to 48 MHz, delivering high performance for the targeted class of applications, while at the same time maintaining ultra-low active power consumption.

6.1.1 Floating Point Unit

The Cortex-M4 processor on the MSP432P401x devices includes a tightly coupled Floating Point Unit (FPU). The FPU is an IEEE754 compliant single precision floating point module supporting add, subtract, multiply, divide, accumulate, and square-root operations. It also provides conversion between fixed-point and floating-point data formats and floating point constant instructions.

6.1.2 Memory Protection Unit

The Cortex-M4 processor on the MSP432P401x devices includes a tightly coupled Memory Protection Unit (MPU) that supports up to eight protection regions. Applications can use this to enforce memory privilege rules, thus allowing isolation of processes from each other, or enforce memory access rules. These features are typically required for operating system handling purposes.

6.1.3 Nested Vectored Interrupt Controller

The MSP432P401x devices include a Nested Vectored Interrupt Controller (NVIC) that supports up to 64 interrupts with eight levels of interrupt priority. The Cortex-M4 NVIC architecture allows for low latency, efficient interrupt/event handling, and seamless integration to device-level power-control strategies.

6.1.4 SYSTICK

The Cortex-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, and is typically deployed either for Operating System related purposes or as a general purpose alarm mechanism.

6.1.5 Debug and Trace Features

The Cortex-M4 processor implements a complete hardware debug solution, providing high system visibility of the processor and memory through either a traditional 4-pin JTAG port or a 2-pin Serial Wire Debug (SWD) port, typically ideal for microcontrollers and other small package devices. The SWJ-DP interface combines the SWD and JTAG debug ports into one module, allowing a seamless switch between the 2-pin and 4-pin modes of operation, depending on application needs.

For system trace, the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system trace events, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

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NOTE

For detailed specifications and information on the programmers model for the Cortex-M4 CPU as well as the associated peripherals mentioned throughout Section 6.1, see the appropriate reference manual at www.arm.com.

6.2 Memory Map

The device supports a 4-GB address space that is divided into eight 512-MB zones (see Figure 6-1).

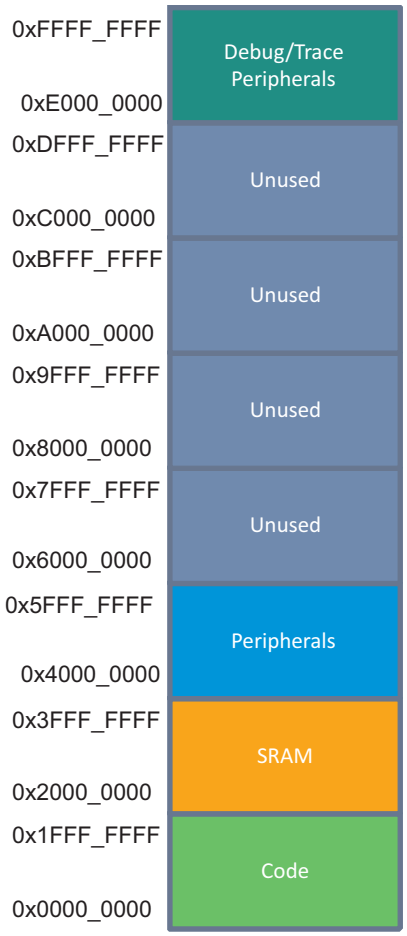


Figure 6-1. Device Memory Zones

6.2.1 CODE Zone Memory Map

The region from 0x0000_0000 to 0x1FFF_FFFF is defined as the Code zone, and is accessible through the ICODE and DCODE buses of the Cortex-M4 processor as well as through the system DMA. This region maps the flash, the ROM as well as the internal SRAM (permitting optimal single cycle execution from the SRAM).

The MSP432P401x specific memory map of the Code Zone, as visible to the user code (see Figure 6-2).

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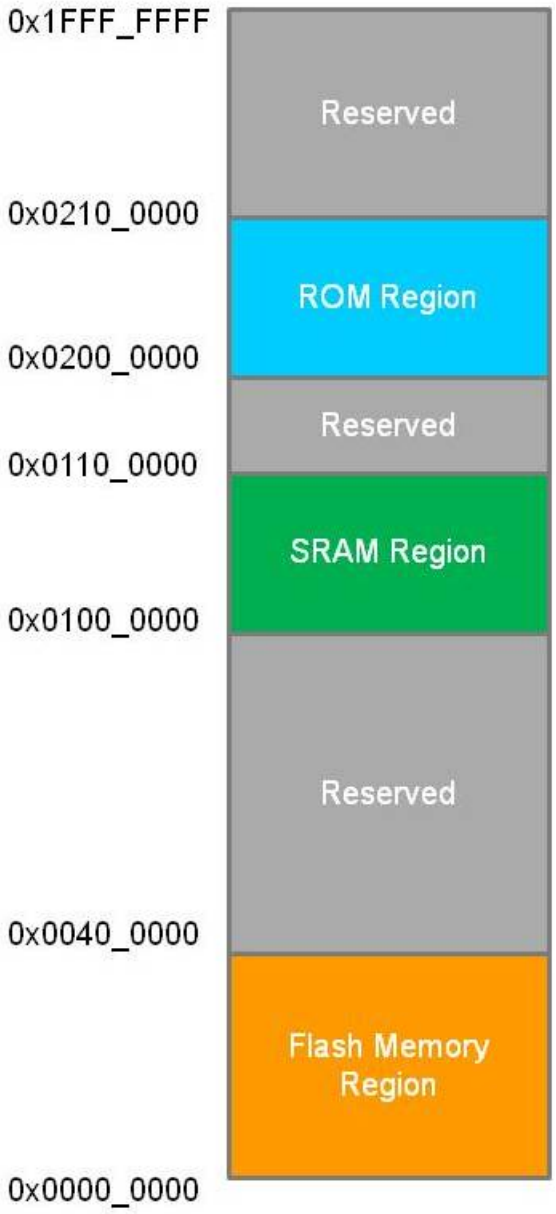


Figure 6-2. CODE Zone Memory Map

6.2.1.1 Flash Memory Region

The 4-MB region from 0x0000_0000 to 0x003F_FFFF is defined as the flash memory region. This region is further divided into different types of flash memory regions which are explained in Section 6.3.1.

6.2.1.2 SRAM Memory Region

The 1-MB region from 0x0100_0000 to 0x010F_FFFF is defined as the SRAM region. This region is also aliased in the SRAM *zone* of the device, thereby allowing efficient access to the SRAM, both for instruction fetches as well as data reads. Refer to Section 6.3.2 for more details.

6.2.1.3 ROM Memory Region

The 1-MB region from 0x0200_0000 to 0x020F_FFFF is defined as the ROM memory region. Details about the ROM memory can be found in Section 6.3.3.

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6.2.2 SRAM Zone Memory Map

The SRAM Zone of the device lies in the address range of 0x2000_0000 to 0x3FFF_FFFF. This is further divided as shown in Figure 6-3.

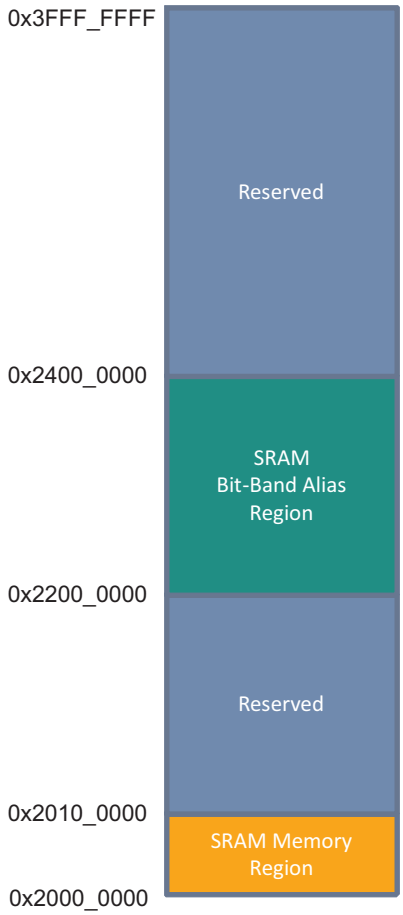


Figure 6-3. SRAM Zone Memory Map

6.2.2.1 SRAM Memory Region

The 1-MB region from 0x2000_0000 to 0x200F_FFFF is defined as the SRAM region. The SRAM memory accessible in this region is also aliased in the Code zone of the device, thereby allowing efficient access to the SRAM, both for instruction fetches as well as data reads. Refer to Section 6.3.2 for details about the SRAM memory.

6.2.2.2 SRAM Bit Band Alias Region

The 32-MB region from 0x2200_0000 through 0x23FF_FFFF forms the bit-band alias region for the 1-MB SRAM region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set or clear individual bits throughout the SRAM memory space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

6.2.3 Peripheral Zone Memory Map

The Peripheral Zone of the device lies in the address range of 0x4000_0000 to 0x5FFF_FFFF. This is further divided as shown in Figure 6-4.

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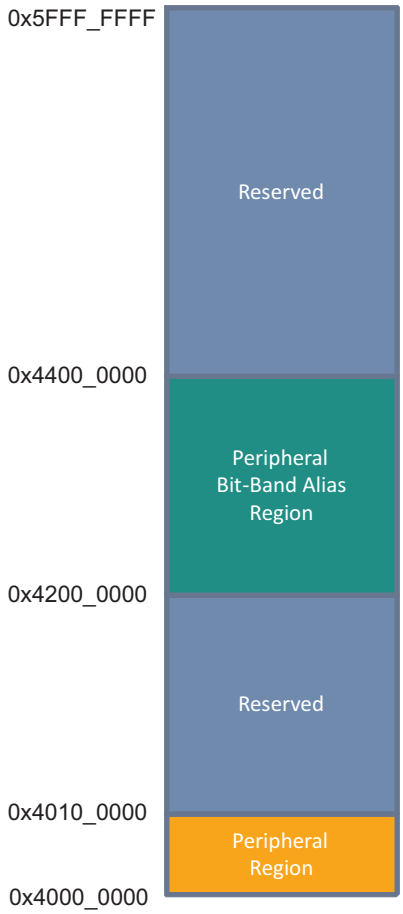


Figure 6-4. Peripheral Zone Memory Map

6.2.3.1 Peripheral Region

The 1-MB region from 0x4000_0000 to 0x400F_FFFF is dedicated to the system and application control peripherals of the device. On the MSP432P401x devices, a total of 128KB of this region is dedicated for peripherals, while the rest is marked as reserved. The peripheral allocation within this 128-KB space is listed in Table 6-1. Note that all peripherals may not be available in all devices of the family (details in the Remarks column). If a peripheral is listed as NA for a particular device, the corresponding address space must be treated as reserved.

NOTE

Peripherals that are marked as 16-bit should be accessed through byte or half-word size read/write only. Any 32-bit access to these peripherals results in a bus error response.

Table 6-1. Peripheral Address Offsets

ADDRESS RANGE	PERIPHERAL	REMARKS
0x4000_0000–0x4000_03FF	Timer_A0	16-bit peripheral
0x4000_0400–0x4000_07FF	Timer_A1	16-bit peripheral
0x4000_0800–0x4000_0BFF	Timer_A2	16-bit peripheral
0x4000_0C00–0x4000_0FFF	Timer_A3	16-bit peripheral
0x4000_1000–0x4000_13FF	eUSCI_A0	16-bit peripheral
0x4000_1400–0x4000_17FF	eUSCI_A1	16-bit peripheral
0x4000_1800–0x4000_1BFF	eUSCI_A2	16-bit peripheral

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Table 6-1. Peripheral Address Offsets (continued)

ADDRESS RANGE	PERIPHERAL	REMARKS
0x4000_1C00–0x4000_1FFF	eUSCI_A3	16-bit peripheral
0x4000_2000–0x4000_23FF	eUSCI_B0	16-bit peripheral
0x4000_2400–0x4000_27FF	eUSCI_B1	16-bit peripheral
0x4000_2800–0x4000_2BFF	eUSCI_B2	16-bit peripheral
0x4000_2C00–0x4000_2FFF	eUSCI_B3	16-bit peripheral
0x4000_3000–0x4000_33FF	REF_A	16-bit peripheral
0x4000_3400–0x4000_37FF	COMP_E0	16-bit peripheral
0x4000_3800–0x4000_3BFF	COMP_E1	16-bit peripheral
0x4000_3C00–0x4000_3FFF	AES256	16-bit peripheral
0x4000_4000–0x4000_43FF	CRC32	16-bit peripheral
0x4000_4400–0x4000_47FF	RTC_C	16-bit peripheral
0x4000_4800–0x4000_4BFF	WDT_A	16-bit peripheral
0x4000_4C00–0x4000_4FFF	Port Module	16-bit peripheral
0x4000_5000–0x4000_53FF	Port Mapping Controller	16-bit peripheral
0x4000_5400–0x4000_57FF	Capacitive Touch I/O 0	16-bit peripheral
0x4000_5800–0x4000_5BFF	Capacitive Touch I/O 1	16-bit peripheral
0x4000_5C00–0x4000_8FFF	Reserved	Read only, always reads 0h
0x4000_9000–0x4000_BFFF	Reserved	Read only, always reads 0h
0x4000_C000–0x4000_CFFF	Timer32	
0x4000_D000–0x4000_DFFF	Reserved	Read only, always reads 0h
0x4000_E000–0x4000_FFFF	DMA	
0x4001_0000–0x4001_03FF	PCM	
0x4001_0400–0x4001_07FF	CS	
0x4001_0800–0x4001_0FFF	PSS	
0x4001_1000–0x4001_17FF	Flash Controller	
0x4001_1800–0x4001_1BFF	Reserved	Read only, always reads 0h
0x4001_1C00–0x4001_1FFF	Reserved	Read only, always reads 0h
0x4001_2000–0x4001_23FF	ADC14	
0x4001_2400–0x4001_FFFF	Reserved	Read only, always reads 0h

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6.2.3.2 Peripheral Bit Band Alias Region

The 32-MB region from 0x4200_0000 through 0x43FF_FFFF forms the bit-band alias region for the 1MB Peripheral region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set/clear individual bits throughout the peripheral memory space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

NOTE

The restriction of accessing 16-bit peripherals only through byte or half-word accesses also applies to the corresponding bit-band region of these peripherals. In other words, writes to the bit-band alias region for these peripherals must be in the form of byte or half-word accesses only.

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6.2.4 Debug and Trace Peripheral Zone

This zone maps the internal as well as external PPB regions of the Cortex-M4. The following peripherals are mapped to this zone

- Core and System debug control registers (internal PPB)
- NVIC and other registers in the System Control space of the Cortex-M4 (internal PPB)
- FPB, DWT, ITM (internal PPB)
- TPIU, Debug ROM table (external PPB)
- Reset Controller (external PPB)
- System Controller (external PPB)

Table 6-2. Debug Zone Memory Map

ADDRESS RANGE	MODULE OR PERIPHERAL	REMARKS
0xE000_0000–0xE000_0FFF	ITM	Internal PPB
0xE000_1000–0xE000_1FFF	DWT	Internal PPB
0xE0000_2000–0xE000_2FFF	FPB	Internal PPB
0xE000_3000–0xE000_DFFF	Reserved	Internal PPB
0xE000_E000–0xE000_EFFF	Cortex-M4 System Control Space	Internal PPB
0xE000_F000–0xE003_FFFF	Reserved	Internal PPB
0xE004_0000–0xE004_0FFF	TPIU	External PPB
0xE004_1000–0xE004_1FFF	Reserved	External PPB
0xE004_2000–0xE004_23FF	Reset Controller	External PPB
0xE004_2400–0xE004_2FFF	Reserved	External PPB
0xE004_3000–0xE004_33FF	System Controller	External PPB
0xE004_3400–0xE004_3FFF	Reserved	External PPB
0xE004_4000–0xE004_43FF	System Controller	External PPB
0xE004_4400–0xE00F_EFFF	Reserved	External PPB
0xE00F_F000–0xE00F_FFFF	ROM Table (External PPB)	External PPB
0xE010_0000–0xFFFF_FFFF	Reserved	Vendor Space

NOTE

Refer to the Cortex-M4 TRM for the address maps of the ARM modules listed above

NOTE

The region from 0xE004_4000–0xE004_43FF is reserved for System Controller registers. These registers are detailed in various sections of this data sheet

6.3 Memories on the MSP432P401x

The MSP432P401x devices include flash and SRAM memories for general application purposes. In addition, the devices include a backup memory (a portion of total available SRAM) that is retained in low-power modes.

6.3.1 Flash Memory

The MSP432P401x devices include a high-endurance low-power flash memory that supports up to 20000 write and erase cycles. The flash memory is 128 bits wide thereby enabling high code execution performance by virtue of each fetch returning up to four 32-bit instructions (or up to eight 16-bit instructions). The flash is further divided into two types of subregions: Main Memory and Information Memory.

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From a physical perspective the flash memory comprises of two banks, with the main and information memory regions divided equally between the two banks. This permits application to carry out a simultaneous read or execute operation from one bank while the other bank may be undergoing a program or erase operation.

The memory map of flash on MSP432P401x devices is shown in Figure 6-5.

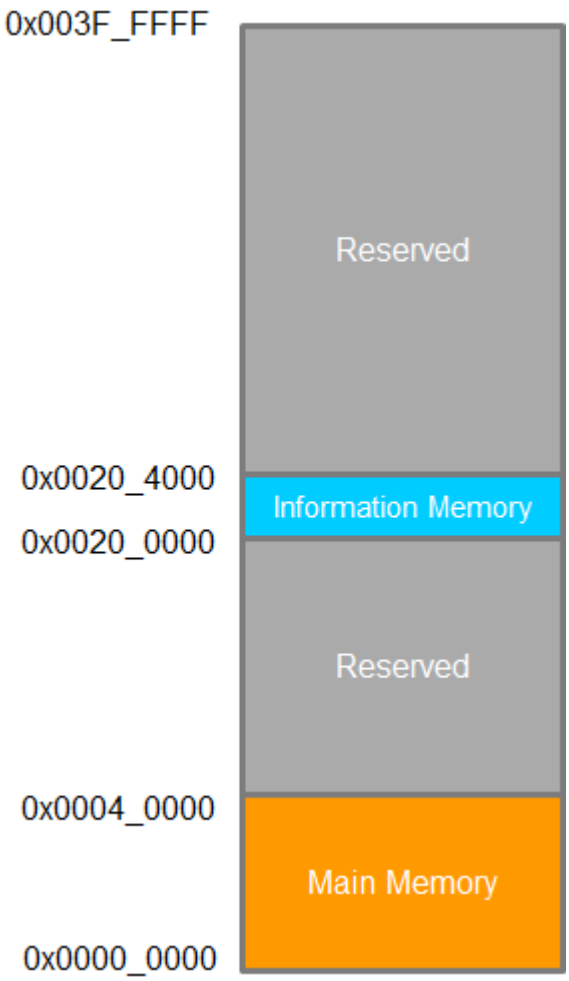


Figure 6-5. Flash Memory Map

6.3.1.1 Flash Main Memory (0x0000_0000 to 0x0003_FFFF)

The flash main memory on MSP432P401x devices can be up to 256KB. Flash main memory consists of up to 64 sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). The main memory can be viewed as two independent, identical banks of up to 128KB each, allowing simultaneous read/execute from one bank while the other bank is undergoing program/erase operation.

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6.3.1.1.1 Flash Size Register (Address = 0xE004_3020h)

This register reflects the size of flash main memory available on the device.

Figure 6-6. SYS_FLASH_SIZE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIZE															
r	r	r	r	r	r	r	r	r	r	r	r	r	r-1	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Table 6-3. SYS_FLASH_SIZE Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-0	SIZE	R	Variable	Indicates the size (in bytes) of the flash main memory on the device. This is divided equally between the two banks.

6.3.1.2 Flash Information Memory (0x0020_0000 to 0x0020_3FFF)

The flash information memory region is 16KB. Flash information memory consists of four sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). The information memory can be viewed as two independent blocks of 8KB each, which allows read or execute from one block while the other block is undergoing a program or erase operation. Table 6-4 describes different regions of flash information memory and the contents of each of the regions. The flash information memory region that contains the device descriptor (TLV) is factory configured for protection again write or erase operations.

Table 6-4. Flash Information Memory Regions

REGION	ADDRESS RANGE	CONTENTS	WRITE AND ERASE PROTECTED?
Bank 0, Sector 0	0x0020_0000–0x0020_0FFF	Flash Boot-override Mailbox	No
Bank 0, Sector 1	0x0020_1000–0x0020_1FFF	Device Descriptor (TLV)	Yes
Bank 1, Sector 0	0x0020_2000–0x0020_2FFF	TI BSL	No
Bank 1, Sector 1	0x0020_3000–0x0020_3FFF	TI BSL	No

6.3.1.3 Flash Operation

The flash memory provides multiple read and program modes of operation that the application can deploy. Up to 128 bits (memory word width) can be programmed (set from 1 to 0) in a single program operation. Although the CPU data buses are 32 bits wide, the flash can buffer 128-bit write data before initiating flash programming, thereby making it more seamless and power efficient for software to program large blocks of data at a time. In addition, the flash memory also supports a burst write mode that takes less time when compared to programming words individually. Refer to *Flash Memory* for information on timing parameters.

The flash main and information memory regions offer write/erase protection control at a sector granularity to enable software to optimize operations like mass erase while protecting certain regions of the flash. In low-power modes of operation, the flash memory is disabled and put in a power-down state to minimize leakage.

For details on the flash memory and its various modes of operation and configuration, refer to the *Flash Controller* chapter in the *MSP432P4xx Family Technical Reference Manual* (SLAU356).

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NOTE

Depending on the CPU (MCLK) frequency and the active mode in use, the flash may need to be accessed with single/multiple wait states. Whenever there is a change required in the operating frequency, it is the responsibility of the application to ensure that the flash access wait states are configured correctly before the frequency change is effected. Refer to electrical specification for details on flash wait state requirements.

6.3.2 SRAM

The MSP432P401x devices support up to 64KB of SRAM memory, with the rest of the 1MB SRAM memory region treated as reserved. The SRAM memory is aliased in *both* Code as well as SRAM memory zones. This enables fast, single cycle execution of code from the SRAM, as the Cortex-M4 processor pipelines instruction fetches to memory zones other than the Code space. As with the flash memory, the SRAM can be powered down or placed in a low leakage retention state in low-power modes of operation.

The memory map of SRAM on MSP432P401x devices is shown in Figure 6-7.

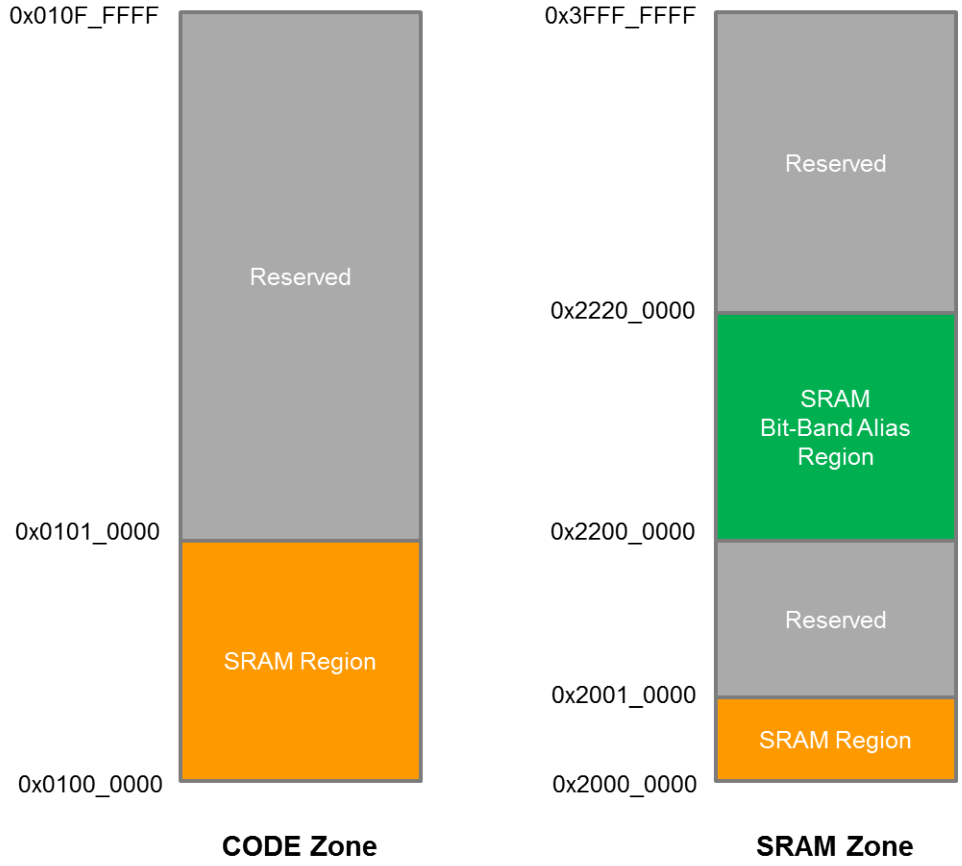


Figure 6-7. SRAM Memory Map

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6.3.2.1 SRAM Bank Enable Configuration

The application can choose to optimize the power consumption of the SRAM. In order to enable this, the SRAM memory is divided into 8KB banks that can individually be powered down. Banks that are powered down remain powered down in both active as well as low-power modes of operation, thereby limiting any unnecessary inrush current when the device transitions between active and retention based low-power modes. The application can also choose to disable one (or more) banks for a certain stage in the processing and re-enable it for another stage. Refer to Section 6.3.2.3 for details on how individual banks can be controlled by the application.

Whenever a particular bank is disabled, reads to its address space return 0h, and writes are discarded. To prevent 'holes' in the memory map, if a particular bank is enabled, all the lower banks are forced to enabled state as well. This ensures a contiguous memory map through the set of enabled banks instead of a possible disabled bank appearing between enabled banks.

NOTE

Bank0 is **always** enabled and cannot be powered down.

NOTE

When any SRAM bank is enabled or disabled, accesses to the SRAM are temporarily stalled to prevent spurious reads. This is handled transparently and does not require any code intervention. Refer to SRAM characteristics in the electrical specification for the SRAM bank enable or disable latency.

6.3.2.2 SRAM Bank Retention Configuration and Backup Memory

The application can choose to optimize the leakage power consumption of the SRAM in LPM3 and LPM4 modes of operation as well. In order to enable this, each SRAM bank can be individually configured for retention. Banks that are enabled for retention retain their data through the LPM3 and LPM4 modes. The application can also choose to retain a subset of the enabled banks.

For example, the application may need 32KB of SRAM for its processing needs (4 banks are kept enabled). However, of these four banks, only one bank may contain critical data that must be retained in LPM3 or LPM4 modes while the rest are powered off completely to minimize power consumption. Refer to Section 6.3.2.3 for details on how individual banks can be controlled by the application.

Bank0 of SRAM is **always** retained and cannot be powered down. Therefore, it also operates up as a possible backup memory in the LPM3, LPM4, and LPM3.5 modes of operation.

6.3.2.3 SRAM Status and Configuration Registers

This section lists the registers that can be used to configure and/or monitor status regarding the SRAM.

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6.3.2.3.1 SRAM Size Register (Address = 0xE004_3010h)

This register reflects the size of the SRAM available on the device.

Figure 6-8. SYS_SRAM_SIZE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIZE															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Table 6-5. SYS_SRAM_SIZE Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-0	SIZE	R	Variable	Indicates the size (in bytes) of SRAM present on the device.

NOTE

The SRAM on the MSP432P401x devices is divided into equal size banks of 8KB each. For example, if the total SRAM available is 32KB, the device contains 4 SRAM banks.

6.3.2.3.2 SRAM Bank Enable Register (Address = E004_3014h)

This register configures which bank of the SRAM is powered up and available for the application. The application can choose to enable or disable SRAM banks on the fly. While the SRAM banks are being powered up or down, accesses to the SRAM space is temporarily stalled and is completed when the SRAM banks are ready. Accesses to the rest of the memory map remain unaffected.

Figure 6-9. SYS_SRAM_BANKEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															SRAM_RDY
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r-0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BNK7_EN	BNK6_EN	BNK5_EN	BNK4_EN	BNK3_EN	BNK2_EN	BNK1_EN	BNK0_EN
r	r	r	r	r	r	r	r	rw-<1>	rw-<1>	rw-<1>	rw-<1>	rw-<1>	rw-<1>	rw-<1>	r-1

Table 6-6. SYS_SRAM_BANKEN Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-17	Reserved	R	0h	Reserved. Reads return 0h
16	SRAM_RDY(1)	R	0h	1b = SRAM is ready for accesses. All SRAM banks are enabled or disabled according to values of bits 7:0 of this register 0b = SRAM is not ready for accesses. Banks are undergoing the enable/disable sequence, and reads/Writes to SRAM will be stalled until the banks are ready
15-8	Reserved	R	0h	Reserved. Reads return 0h

(1) This bit will automatically be set to 0 whenever any of the Bank Enable bits in this register are changed, which will in turn trigger off a power up/down of the impacted SRAM blocks. It will set back to 1 after the power sequence is complete and the SRAM blocks are ready for subsequent read/write accesses

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Table 6-6. SYS_SRAM_BANKEN Register Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BNK7_EN (2)	RW	1h	0b = Disables Bank7 of the SRAM 1b = enables Bank7 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
6	BNK6_EN (2)	RW	1h	0b = Disables Bank6 of the SRAM 1b = enables Bank6 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
5	BNK5_EN (2)	RW	1h	0b = Disables Bank5 of the SRAM 1b = enables Bank5 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
4	BNK4_EN (2)	RW	1h	0b = Disables Bank4 of the SRAM 1b = enables Bank4 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
3	BNK3_EN (2)	RW	1h	0b = Disables Bank3 of the SRAM 1b = enables Bank3 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
2	BNK2_EN (2)	RW	1h	0b = Disables Bank2 of the SRAM 1b = enables Bank2 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
1	BNK1_EN (2)	RW	1h	0b = Disables Bank1 of the SRAM 1b = enables Bank1 of the SRAM When set to 1, bank enable bits for all banks below this bank are set to 1 as well.
0	BNK0_EN	R	1h	When 1, enables Bank0 of the SRAM

(2) Writes to this bit are allowed ONLY when the SRAM_RDY bit is set to 1. If the bit is 0, it indicates that the SRAM banks are not ready, and writes to this bit will be ignored

The SRAM Bank Enable Register controls which banks of the SRAM are enabled for read/write accesses. There is one bit for each available bank (unused bits are reserved). Banks that are not enabled are powered down to minimize power consumption. Each bit in this register corresponds to one bank of the SRAM. Banks may **only** be enabled in a contiguous form. For example:

- If there are eight banks in the device, values of 00111111 and 00000111 are acceptable.
- Values like 00010111 are not valid, and the resultant bank configuration will be set to 00011111.
- For exmaple, for a 4-bank SRAM, the only allowed values are 0001, 0011, 0111, and 1111

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NOTE

Bank0 is **always** enabled and cannot be disabled. In the case of all other banks, any enable/disable change will result in the SRAM_RDY bit of the SYS_SRAM_BANKEN register being set to 0 until the configuration change is effective. Any accesses to the SRAM will be stalled during this time frame, and resumed only after the SRAM banks are ready for read or write operations.

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6.3.2.3.3 SRAM Bank Retention Control Register (Address = E004_3018h)

This register controls which bank of the SRAM is retained when the device enters LPM3 or LPM4 modes. Any bank that is not enabled for retention will be completely powered down in these modes and will lose its data

Figure 6-10. SYS_SRAM_BANKRET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															SRAM_RDY
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BNK7_RET	BNK6_RET	BNK5_RET	BNK4_RET	BNK3_RET	BNK2_RET	BNK1_RET	BNK0_RET
r	r	r	r	r	r	r	r	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-1

Table 6-7. SYS_SRAM_BANKRET Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-17	Reserved	R	0h	Reserved. Reads return 0h
16	SRAM_RDY (1)	R	0h	1b = SRAM is ready for accesses. All SRAM banks are enabled or disabled for retention according to values of bits 7:0 of this register 0b = SRAM banks are being set up for retention. Entry into LPM3, LPM4 should not be attempted until this bit is set to 1.
15-8	Reserved	R	0h	Reserved. Reads return 0h
7	BNK7_RET (2)(3)	RW	0h	0b = Bank7 of the SRAM is not retained in LPM3 or LPM4 1b = Bank7 of the SRAM is retained in LPM3 or LPM4
6	BNK6_RET (2), (3)	RW	0h	0b = Bank6 of the SRAM is not retained in LPM3 or LPM4 1b = Bank6 of the SRAM is retained in LPM3 or LPM4
5	BNK5_RET (2)(3)	RW	0h	0b = Bank5 of the SRAM is not retained in LPM3 or LPM4 1b = Bank5 of the SRAM is retained in LPM3 or LPM4
4	BNK4_RET (2)(3)	RW	0h	0b = Bank4 of the SRAM is not retained in LPM3 or LPM4 1b = Bank4 of the SRAM is retained in LPM3 or LPM4
3	BNK3_RET (2), (3)	RW	0h	0b = Bank3 of the SRAM is not retained in LPM3 or LPM4 1b = Bank3 of the SRAM is retained in LPM3 or LPM4
2	BNK2_RET (2)(3)	RW	0h	0b = Bank2 of the SRAM is not retained in LPM3 or LPM4 1b = Bank2 of the SRAM is retained in LPM3 or LPM4
1	BNK1_RET (2)(3)	RW	0h	0b = Bank1 of the SRAM is not retained in LPM3 or LPM4 1b = Bank1 of the SRAM is retained in LPM3 or LPM4
0	BNK0_RET	R	1h	Bank0 is always retained in LPM3, LPM4 and LPM3.5 modes of operation

(1) This bit will automatically be set to 0 whenever any of the BNKx_RET bits in this register are changed. It will set back to 1 after the SRAM controller has recognized the new BNKx_RET values.
(2) Value of this bit is a don't care when the device enters LPM3.5 or LPM4.5 modes of operation. It will always get reset and the SRAM block associated with this bit will not retain its contents.
(3) Writes to this bit are allowed ONLY when the SRAM_RDY bit of this register is set to 1. If the SRAM_RDY bit is 0, writes to this bit will be ignored.

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6.3.3 ROM

The MSP432P401x devices support 32KB of ROM memory, with the rest of the 1-MB region treated as reserved (for future upgrades). The lower 1KB of the ROM is reserved for TI internal purposes and accesses to this space will return an error response. The rest of the ROM is used for driver libraries.

NOTE

The entire ROM region returns an error response for write accesses. The lower 1KB of the ROM always returns an error response for any access.

6.4 DMA

The MSP432P401x devices implement an 8-channel ARM uDMA. This allows eight simultaneously active channels for data transfer between memory and peripherals without needing to use the bandwidth of the CPU (thereby reducing power by idling the CPU when there is no data processing required). In addition, the DMA remains active in multiple low-power modes of operation, allowing for a very low power state in which data can be transferred at low rates.

For maximum flexibility, up to eight DMA event sources can map to any of the eight channels. This is controlled through configuration registers in the DMA. In addition, the DMA can generate up to four interrupt requests (described in Section 6.4.2). For details regarding configuration of the DMA, refer to the DMA chapter in the *MSP432P4xx Family Technical Reference Manual*.

Figure 6-11 shows the block diagram of the DMA.

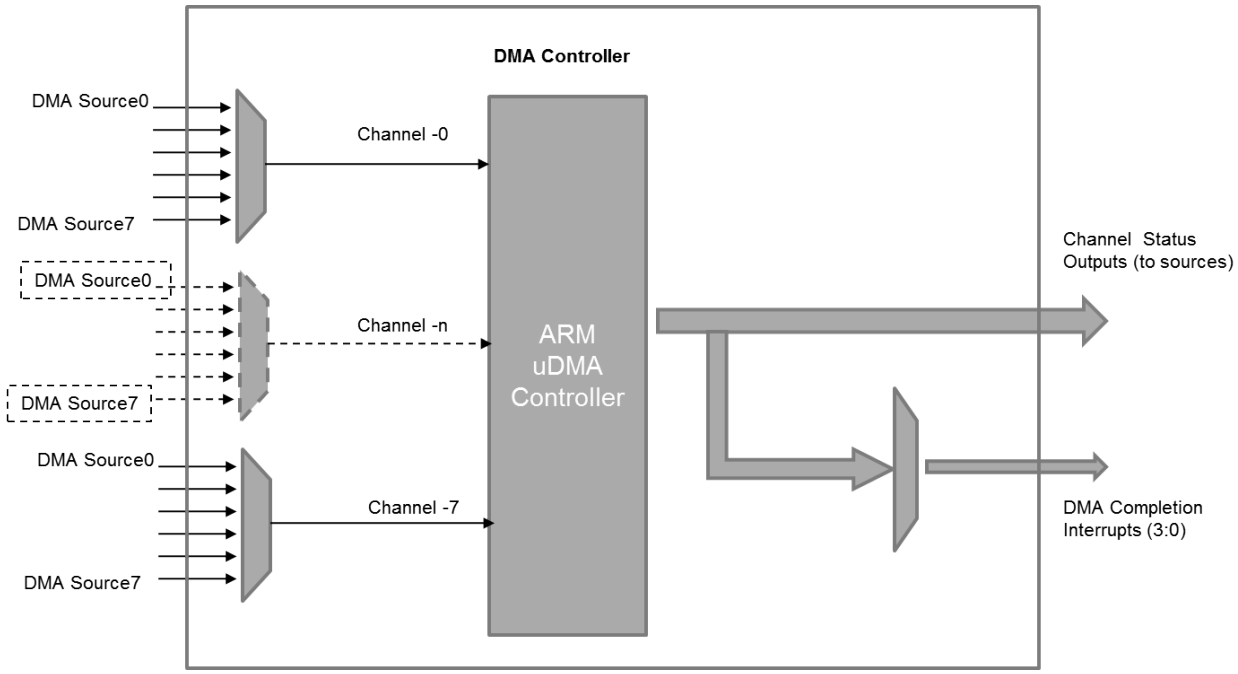


Figure 6-11. DMA Block Diagram

6.4.1 DMA Source Mapping

Each channel of the eight available channels has a control register that can select any of the device level DMA sources as the final source for that corresponding channel. Table 6-8 lists the sources available for mapping to each channel, based on the value of the Source Config Register (SRCCFG).

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Table 6-8. DMA Sources

	SRCCFG = 0	SRCCFG = 1	SRCCFG = 2	SRCCFG = 3	SRCCFG = 4	SRCCFG = 5	SRCCFG = 6	SRCCFG = 7
Channel 0	Reserved	eUSCI_A0 TX	eUSCI_B0 TX0	eUSCI_B3 TX1	eUSCI_B2 TX2	eUSCI_B1 TX3	TA0CCR0	AES256_Trigger0
Channel 1	Reserved	eUSCI_A0 RX	eUSCI_B0 RX0	eUSCI_B3 RX1	eUSCI_B2 RX2	eUSCI_B1 RX3	TA0CCR2	AES256_Trigger1
Channel 2	Reserved	eUSCI_A1 TX	eUSCI_B1 TX0	eUSCI_B0 TX1	eUSCI_B3 TX2	eUSCI_B2 TX3	TA1CCR0	AES256_Trigger2
Channel 3	Reserved	eUSCI_A1 RX	eUSCI_B1 RX0	eUSCI_B0 RX1	eUSCI_B3 RX2	eUSCI_B2 RX3	TA1CCR2	Reserved
Channel 4	Reserved	eUSCI_A2 TX	eUSCI_B2 TX0	eUSCI_B1 TX1	eUSCI_B0 TX2	eUSCI_B3 TX3	TA2CCR0	Reserved
Channel 5	Reserved	eUSCI_A2 RX	eUSCI_B2 RX0	eUSCI_B1 RX1	eUSCI_B0 RX2	eUSCI_B3 RX3	TA2CCR2	Reserved
Channel 6	Reserved	eUSCI_A3 TX	eUSCI_B3 TX0	eUSCI_B2 TX1	eUSCI_B1 TX2	eUSCI_B0 TX3	TA3CCR0	DMAE0 (External Pin)
Channel 7	Reserved	eUSCI_A3 RX	eUSCI_B3 RX0	eUSCI_B2 RX1	eUSCI_B1 RX2	eUSCI_B0 RX3	TA3CCR2	ADC14

NOTE

Any source marked as Reserved is unused. It may be used for software-controlled DMA tasks, but typically it is reserved for enhancement purposes on future devices.

6.4.2 DMA Completion Interrupts

In the case of the ARM µDMA controller, it is usually the responsibility of software to maintain a list of channels that have completed their operation. In order to provide further flexibility, the MSP432P401x DMA supports four DMA completion interrupts, which are mapped in the following way:

- DMA_INT0: Logical OR of all completion events **except** those that are already mapped to DMA_INT1, DMA_INT2, or DMA_INT3.
- DMA_INT1, DMA_INT2, DMA_INT3: Can be mapped to the DMA completion event of any of the eight channels

NOTE

Software must ensure that DMA_INT1, DMA_INT2, and DMA_INT3 are mapped to different channels, so that the same channel does not result in multiple interrupts at the NVIC.

6.4.3 DMA Access Privileges

The DMA has access to all the memories and peripheral configuration interfaces of the device. In the event the device is configured for IP protection, DMA access to the flash is restricted to only the lower half (second bank) of the flash main and information memory regions. This prevents the DMA from being used as an unauthorized access source into the top half (first bank) of the flash, where secure data regions are housed.

6.5 Memory Map Access Details

The bus system on the MSP432P401x devices incorporates 4 masters, which can initiate various types of transactions

- ICODE: Cortex-M4 instruction fetch bus. Accesses the Code Zone only
- DCODE: Cortex-M4 data and literal fetch bus. Accesses the Code Zone only. Debugger accesses to Code Zone also appear on this bus.
- SBUS: Cortex-M4 data read and write bus. Accesses to all zones except Code Zones and PPB memory space only. Debugger accesses to this space also appear on this bus.
- DMA: Access to all zones except the PPB memory space

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NOTE

The PPB space is dedicated only to the Cortex-M4 Private Peripheral Bus.

6.5.1 Master and Slave Access Priority Settings

Table 6-9 lists all the available masters (rows) and their access permissions to slaves (columns). If multiple masters can access one slave, the table lists access priorities if arbitration is required. A lower number in the table indicates a higher arbitration priority (the priority is always fixed).

Table 6-9. Master and Slave Access Priority

	FLASH MEMORY	ROM	SRAM	PERIPHERALS
ICODE	3	2	4	NA
DCODE	2 (1)	1	2	NA
SBUS	NA	NA	3	2
DMA	1 (2)	NA	1 (3)	1

(1) Access from the DCODE to flash memory may be restricted if the device is operating in a secure mode
(2) Access from DMA to flash memory will be restricted to Bank 1 if the device is operating in a secure mode with IP protection enabled. In such cases, access to Bank0 will return an error response
(3) Although the SRAM is mapped to both Code and System spaces, accesses from DMA to SRAM must use the System space addressing ONLY.

6.5.2 Memory Map Access Response

The following table consolidates the access responses to the entire memory map of the MSP432P401x devices.

Table 6-10. Memory Map Access Response

ADDRESS RANGE	DESCRIPTION	READ (1)	WRITE (1)	INSTRUCTION FETCH (1)
0x0000_0000–0x0003_FFFF	Flash Main Memory	OK	OK (2), (3)	OK
0x0004_0000–0x001F_FFFF	Reserved	Error	Error	Error
0x0020_0000–0x0020_3FFF	Flash Information Memory	OK	OK (3)	OK
0x0020_4000–0x00FF_FFFF	Reserved	Error	Error	Error
0x0100_0000–0x0100_FFFF	SRAM	OK	OK	OK
0x0101_0000–0x01FF_FFFF	Reserved	Error	Error	Error
0x0200_0000–0x0200_03FF	ROM (Reserved)	Error	Error	Error
0x0200_0400–0x0200_7FFF	ROM	OK	Error	OK
0x0200_8000–0x1FFF_FFFF	Reserved	Error	Error	Error
0x2000_0000–0x2000_FFFF	SRAM	OK	OK	OK
0x2001_0000–0x21FF_FFFF	Reserved	Error	Error	Error
0x2200_0000–0x23FF_FFFF	SRAM bit-band alias	OK (4)	OK	Error
0x2400_0000–0x3FFF_FFFF	Reserved	Error	Error	Error
0x4000_0000–0x4001_FFFF	Peripheral	OK	OK	Error
0x4002_0000–0x41FF_FFFF	Reserved	Error	Error	Error
0x4200_0000–0x43FF_FFFF	Peripheral bit-band alias	OK (4)	OK	Error
0x4400_0000–0xDFFF_FFFF	Reserved	Error	Error	Error

(1) A 'reserved' memory region returns 0h on reads and instruction fetches. Writes to this region are ignored.
(2) If the User memory address is part of a secure region, this access returns an error if it is initiated by an unauthorized source. For more details, refer to the device security application note.
(3) Writes to this address are ignored if the concerned sector has write protection enabled.
(4) Reads from the bit-band region return 00h if the bit is clear and 01h if the bit is set.

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Table 6-10. Memory Map Access Response (continued)

ADDRESS RANGE	DESCRIPTION	READ (1)	WRITE (1)	INSTRUCTION FETCH (1)
0xE000_0000–0xE003_FFFF	Internal PPB (5)	OK	OK	Error
0xE004_0000–0xE004_0FFF	TPIU (External PPB)	OK	OK	Error
0xE004_1000–0xE004_1FFF	Reserved	Reserved	Reserved	Error
0xE004_2000–0xE004_23FF	Reset Controller (External PPB)	OK	OK	Error
0xE004_2400–0xE004_2FFF	Reserved	Reserved	Reserved	Error
0xE004_3000–0xE004_33FF	SYSCTL (External PPB)	OK	OK	Error
0xE004_3400–0xE004_3FFF	Reserved	Reserved	Reserved	Error
0xE004_4000–0xE004_43FF	SYSCTL (External PPB)	OK	OK	Error
0xE004_4400–0xE00F_EFFF	Reserved	Reserved	Reserved	Error
0xE00F_F000–0xE00F_FFFF	ROM Table (External PPB)	OK	OK	Error
0xE010_0000–0xFFFF_FFFF	Reserved	Error	Error	Error

(5) Refer to the Cortex®-M4 TRM for details of the memory map of the internal PPB.

6.6 Interrupts

The Cortex-M4 processor on MSP432P401x devices implements an NVIC with 64 external interrupt lines and 8 levels of priority. From an application perspective, the interrupt sources at the device level are divided into two classes, the NMI and the User Interrupts. Internally, the CPU exception model handles the various exceptions (internal and external events including CPU instruction, memory, and bus fault conditions) in a fixed and configurable order of priority. For details on the handling of various exception priorities (including CPU reset and fault models), see the ARM-V7M architecture reference manual at www.arm.com.

6.6.1 NMI

The NMI input of the NVIC has the following possible sources

- External NMI pin (if configured in NMI mode)
- Oscillator fault condition
- Power Supply System (PSS) generated interrupts
- Power Control Manager (PCM) generated interrupts

The source that finally feeds the NMI of the NVIC is configured through the NMI Control register, explained in Section 6.6.1.1.

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6.6.1.1 NMI Control and Status Register [Address = E004_3004h]

Figure 6-12. SYS_NMI_CTLSTAT Register

31	30	29	28	27	26	25	24
Reserved							
r	r	r	r	r	r	r	r
23	22	21	20	19	18	17	16
Reserved				PIN_FLG	PCM_FLG	PSS_FLG	CS_FLG
r	r	r	r	rw-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
Reserved				PIN_SRC	PCM_SRC	PSS_SRC	CS_SRC
r	r	r	r	rw-0	rw-1	rw-1	rw-1

Table 6-11. SYS_NMI_CTLSTAT Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-20	Reserved	R	0h	Reserved. Reads return 0h
19	PIN_FLG	RW	0h	0b = Indicates the RSTn/NMI pin was not the source of NMI 1b = Indicates the RSTn/NMI pin was the source of NMI
18	PCM_FLG	R	0h	0b = Indicates the PCM interrupt was not the source of NMI 1b = Indicates the PCM interrupt was the source of NMI This flag gets auto-cleared when the corresponding source flag in the PCM is cleared
17	PSS_FLG	R	0h	0b = Indicates the PSS interrupt was not the source of NMI 1b = Indicates the PSS interrupt was the source of NMI This flag gets auto-cleared when the corresponding source flag in the PSS is cleared
16	CS_FLG	R	0h	0b = Indicates CS interrupt was not the source of NMI 1b = Indicates CS interrupt was the source of NMI This flag gets auto-cleared when the corresponding source flag in the CS is cleared
15-4	Reserved	R	0h	Reserved. Reads return 0h
3	PIN_SRC(1)(2)	RW	0h	0b = Configures the RSTn/NMI pin as a source of POR Class Reset 1b = Configures the RSTn/NMI pin as a source of NMI **Note:** Setting this bit to 1 prevents the RSTn pin from being used as a reset. An NMI is triggered by the pin only if a negative edge is detected.
2	PCM_SRC	RW	1h	0b = Disbles the PCM interrupt as a source of NMI 1b = Enables the PCM interrupt as a source of NMI
1	PSS_SRC	RW	1h	0b = Disables the PSS interrupt as a source of NMI 1b = Enables the PSS interrupt as a source of NMI

(1) When the device enters LPM3/LPM4 modes of operation, the functionality selected by this bit will be retained. If selected as an NMI, activity on this pin in LPM3/LPM4 will wake the device and process the interrupt, without causing a POR. If selected as a Reset, activity on this pin in LPM3/LPM4 will cause a device level POR

(2) When the device enters LPM3.5/LPM4.5 modes of operation, this bit will *always* be cleared to 0. In other words, the RSTn/NMI pin will always assume a reset functionality in LPM3.5/LPM4.5 modes.

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Table 6-11. SYS_NMI_CTLSTAT Register Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	CS_SRC	RW	1h	0b = Disables CS interrupt as a source of NMI 1b = Enables CS interrupt as a source of NMI

6.6.2 Device-Level User Interrupts

Table 6-12 lists the various interrupt sources and their connection to the NVIC inputs

NOTE

Some sources may have multiple interrupt conditions, in which case the appropriate interrupt status/flag register of the source must be examined to differentiate between the generating conditions.

Table 6-12. NVIC Interrupts

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[0]	PSS (1)	
INTISR[1]	CS (1)	
INTISR[2]	PCM (1)	
INTISR[3]	WDT_A	
INTISR[4]	FPU_INT (2)	Combined interrupt from flags in the FPSCR (part of Cortex-M4 FPU)
INTISR[5]	Flash Controller	Flash Controller interrupt flags
INTISR[6]	COMP_E0	Comparator_E0 interrupt flags
INTISR[7]	COMP_E1	Comparator_E1 interrupt flags
INTISR[8]	Timer_A0	TA0CCTL0.CCIFG
INTISR[9]	Timer_A0	TA0CCTLx.CCIFG (x = 1 through 4), TA0CTL.TAIFG
INTISR[10]	Timer_A1	TA1CCTL0.CCIFG
INTISR[11]	Timer_A1	TA1CCTLx.CCIFG (x = 1 through 4), TA1CTL.TAIFG
INTISR[12]	Timer_A2	TA2CCTL0.CCIFG
INTISR[13]	Timer_A2	TA2CCTLx.CCIFG (x = 1 through 4), TA2CTL.TAIFG
INTISR[14]	Timer_A3	TA3CCTL0.CCIFG
INTISR[15]	Timer_A3	TA3CCTLx.CCIFG (x = 1 through 4), TA3CTL.TAIFG
INTISR[16]	eUSCI_A0	UART/SPI mode Tx/Rx/Status Flags
INTISR[17]	eUSCI_A1	UART/SPI mode Tx/Rx/Status Flags
INTISR[18]	eUSCI_A2	UART/SPI mode Tx/Rx/Status Flags
INTISR[19]	eUSCI_A3	UART/SPI mode Tx/Rx/Status Flags
INTISR[20]	eUSCI_B0	SPI/I^2C mode Tx/Rx/Status Flags (I^2C in multi-slave mode)
INTISR[21]	eUSCI_B1	SPI/I^2C mode Tx/Rx/Status Flags (I^2C in multi-slave mode)
INTISR[22]	eUSCI_B2	SPI/I^2C mode Tx/Rx/Status Flags (I^2C in multi-slave mode)
INTISR[23]	eUSCI_B3	SPI/I^2C mode Tx/Rx/Status Flags (I^2C in multi-slave mode)
INTISR[24]	ADC14	IFG[0-31], LO/IN/HI-IFG, RDYIFG, OVIFG, TOVIFG
INTISR[25]	Timer32_INT1	Timer32 Interrupt for Timer1
INTISR[26]	Timer32_INT2	Timer32 Interrupt for Timer2
INTISR[27]	Timer32_INTC	Timer32 Combined Interrupt
INTISR[28]	AES256	AESRDYIFG
INTISR[29]	RTC_C	OFIFG, RDYIFG, TEVIFG, AIFG, RT0PSIFG, RT1PSIFG
INTISR[30]	DMA_ERR	DMA error interrupt

(1) This source can also be mapped to the system NMI. Refer to the *MSP432P4xx Family Technical Reference Manual* for more details.
(2) The FPU of the Cortex-M4 can generate interrupts due to multiple floating point exceptions. It is the responsibility of software to process and clear the interrupt flags in the FPSCR.

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Table 6-12. NVIC Interrupts (continued)

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[31]	DMA_INT3	DMA completion interrupt3
INTISR[32]	DMA_INT2	DMA completion interrupt2
INTISR[33]	DMA_INT1	DMA completion interrupt1
INTISR[34]	DMA_INT0(3)	DMA completion interrupt0
INTISR[35]	I/O Port P1	P1IFG.x (x = 0 through 7)
INTISR[36]	I/O Port P2	P2IFG.x (x = 0 through 7)
INTISR[37]	I/O Port P3	P3IFG.x (x = 0 through 7)
INTISR[38]	I/O Port P4	P4IFG.x (x = 0 through 7)
INTISR[39]	I/O Port P5	P5IFG.x (x = 0 through 7)
INTISR[40]	I/O Port P6	P6IFG.x (x = 0 through 7)
INTISR[41]	Reserved	
INTISR[42]	Reserved	
INTISR[43]	Reserved	
INTISR[44]	Reserved	
INTISR[45]	Reserved	
INTISR[46]	Reserved	
INTISR[47]	Reserved	
INTISR[48]	Reserved	
INTISR[49]	Reserved	
INTISR[50]	Reserved	
INTISR[51]	Reserved	
INTISR[52]	Reserved	
INTISR[53]	Reserved	
INTISR[54]	Reserved	
INTISR[55]	Reserved	
INTISR[56]	Reserved	
INTISR[57]	Reserved	
INTISR[58]	Reserved	
INTISR[59]	Reserved	
INTISR[60]	Reserved	
INTISR[61]	Reserved	
INTISR[62]	Reserved	
INTISR[63]	Reserved	

(3) DMA_INT0 has a different functionality from DMA_INT1/2/3. Refer to Section 6.4.2 for more details.

NOTE

The Interrupt Service Routine (ISR) **must** ensure that the relevant interrupt flag in the source peripheral is cleared before returning from the ISR. If this is not done, the same interrupt may get incorrectly pended again as a new event, even though the event has already been processed by the ISR. As there may be a few cycles of delay between the execution of the write command and the actual write reflecting in the peripheral's interrupt flag register, the recommendation is to carry out the write and wait for a few cycles before exiting the ISR. Alternatively, the application can do an explicit read to ensure that the flag was cleared before exiting the ISR.

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6.7 System Control

System Control comprises the modules that govern the overall behavior of the device, including power management, operating modes, clocks, reset handling, and user configuration settings.

6.7.1 Device Resets

The MSP432P401x devices support multiple classes of reset. Each class results in a different level of initiation of device logic, thus offering the application developer the capability of initiating different resets based reset requirements during code development and debug. The following subsections cover the classes of reset in the device

6.7.1.1 Power On/Off Reset (POR)

The POR initiates a complete initialization of the application settings and device configuration information. This class of reset may be initiated either by the PSS, the PCM, the RSTn pin, the Clock System upon DCO external resistor short circuit fault or the device emulation logic (through the debugger). From an application perspective, all sources of POR return the device to the same state of initialization.

NOTE

Depending on the source of the reset, the device may exhibit different wake-up latencies from the POR. This implementation enables optimization of the reset recovery time.

6.7.1.2 Reboot Reset

The Reboot Reset is identical to the POR, and allows the application to emulate a POR class reset without needing to power cycle the device or activating the RSTn pin. It can also be initiated through the debugger, and hence does not affect the debug connection to the device. On the other hand, a POR will result in a debug disconnect.

6.7.1.2.1 Reboot Control Register (Address = E004_3000h)

Figure 6-13. SYS_REBOOT_CTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKEY								Reserved							REBOOT
w	w	w	w	w	w	w	w	r	r	r	r	r	r	r	w

Table 6-13. SYS_REBOOT_CTL Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-16	Reserved	R	0h	Reserved. Reads return 0h
15-8	WKEY	W	0h	Key to enable writes to bit 0. Bit 0 is written only if WKEY is 69h in the same write cycle
7-1	Reserved	R	0h	Reserved. Reads return 0h
0	REBOOT	W	0h	Write 1 initiates a Reboot of the device

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6.7.1.3 Hard Reset

The Hard Reset resets all modules that are set up or modified by the application. This includes all peripherals as well as the non debug logic of the Cortex-M4. The MSP432P401x devices support up to 16 sources of Hard Reset. The following table lists the reset source allocation. The Reset Controller registers can be used to identify the possible source of reset in the device. For further details, refer to Reset Controller chapter in the *MSP432P4xx Family Technical Reference Manual* (SLAU356).

Table 6-14. MSP432P401x Hard Reset Sources

RESET SOURCE NUMBER	SOURCE
0	SYSRESETREQ (System reset output of Cortex-M4)
1	WDT_A Time-out (1)
2	WDT_A Password Violation (1)
3	Flash Controller (2)
4	Reserved (3)
5	Reserved (3)
6	Reserved (3)
7	Reserved (3)
8	Reserved (3)
9	Reserved (3)
10	Reserved (3)
11	Reserved (3)
12	Reserved (3)
13	Reserved (3)
14	CS (4)
15	PCM (5)

(1) The WDT_A generated resets can be mapped either as a Hard Reset or a Soft Reset.
(2) The Flash Controller can generate a reset if a voltage anomaly is detected that can corrupt only flash reads, and not the rest of the system.
(3) 'Reserved' indicates that this source of Hard Reset is currently unused and left for future expansion.
(4) The CS is technically not a true source of a Hard Reset, but if a Hard Reset occurs during clock source/frequency changes, it may extend the reset to allow the clocks to settle before releasing the system. This prevents chances of nondeterministic behavior.
(5) The PCM is technically not a true source of a Hard Reset, but if a Hard Reset causes power mode changes, it may extend the reset to allow the system to settle before releasing the Reset. This prevents chances of nondeterministic behavior.

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6.7.1.4 Soft Reset

The Soft Reset resets only the execution component of the system, which is the non debug logic in the Cortex-M4 and the WDT_A. This reset remains nonintrusive to all other peripherals and system components. The MSP432P401x devices support up to 16 sources of Soft Reset. The following table lists the reset source allocation. The Reset Controller registers can be used to identify the possible source of reset in the design. For further details, refer to Reset Controller chapter in the *MSP432P4xx Family Technical Reference Manual* (SLAU356).

Table 6-15. MSP432P401x Soft Reset Sources

RESET SOURCE NUMBER	SOURCE
0	CPU LOCKUP Condition (LOCKUP output of Cortex-M4)
1	WDT_A Time-out (1)
2	WDT_A Password Violation (1)
3	Reserved (2)
4	Reserved (2)
5	Reserved (2)
6	Reserved (2)
7	Reserved (2)
8	Reserved (2)
9	Reserved (2)
10	Reserved (2)
11	Reserved (2)
12	Reserved (2)
13	Reserved (2)
14	Reserved (2)
15	Reserved (2)

(1) The WDT_A generated resets can be mapped either as a Hard Reset or a Soft Reset.
(2) 'Reserved' indicates that this source of Soft Reset is currently unused and left for future expansion.

NOTE

To support and enhance debug of reset conditions, the Reset Controller is located on the PPB of the device. This allows the Reset Controller to remain accessible even if the device is stuck in a Hard or Soft reset state. The Reset Controller permits overrides for Hard and Soft resets, thereby allowing regaining control of the device and isolating the cause of the stuck reset.

6.7.2 Power Supply System (PSS)

The PSS controls all the power supply related functionality of the device. It consists of the following components

6.7.2.1 VCCDET

The VCCDET monitors the input voltage applied at the DVCC and AVCC pins of the device. When the V_{CC} is found to be below the operating range of the VCCDET trip points, it generates a brownout condition, thereby initiating a device reset (POR class reset).

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6.7.2.2 Supply Supervisor and Monitor for High Side (SVSMH)

The SVSMH supervises and monitors the V_{CC}. SVSMH has a programmable threshold setting and can be used by the application to generate a reset or an interrupt if the V_{CC} dips below the desired threshold. In supervisor mode, the SVSMH generates a device reset (POR class reset). In monitor mode, the SVSMH generates an interrupt. The SVSMH can also be disabled if monitoring and supervision of the supply voltage are not required (offers further power savings).

6.7.2.3 Core Voltage Regulator

The MSP432P401x devices can be programmed to operate either with an LDO or with a DC-DC as the voltage regulator for the digital logic in the core domain of the device. The DC-DC offers significant boost in power efficiency for high-current high-performance applications. The LDO is a highly efficient regulator that offers power advantages at lower V_{CC} ranges and in the ultra-low-power modes of operation.

The core operating voltage (output of the LDO or DC-DC) is automatically set by the device depending on the selected operating mode of the device (refer to Table 6-16 for further details). The device offers seamless switching between LDO and DC-DC operating modes and also implements a seamless DC-DC fail-safe mechanism.

6.7.2.4 Supply Supervisor for Low Side (SVSL)

The SVSL monitors the low-side (core domain) voltage of the device (also available at the VCORE pin). If the core voltage drops below the trip threshold of the SVSL, the SVSL generates a device reset (POR class reset). The SVSL can also be disabled if supervision of the core voltage is not required (offers further power savings).

6.7.3 Power Control Manager (PCM)

The PCM controls the operating modes of the device and the switching between the modes. This is controlled by the application, which can choose modes to meet its power and performance requirements. Table 6-16 lists the operating modes of the device.

Table 6-16. MSP432P401x Operating Modes

OPERATING MODE	DESCRIPTION
AM_LDO_VCORE0	LDO based active mode, medium performance, core voltage level 0
LPM0_LDO_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_LDO_VCORE1	LDO based active mode, maximum performance, core voltage level 1
LPM0_LDO_VCORE1	Same as above, except that CPU is OFF (no code execution)
AM_DCDC_VCORE0	DC-DC based active mode, medium performance, core voltage level 0
LPM0_DCDC_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_DCDC_VCORE1	DC-DC based active mode, maximum performance, core voltage level 1
LPM0_DCDC_VCORE1	Same as above, except that CPU is OFF (no code execution)
AM_LF_VCORE0	LDO based low frequency active mode, core voltage level 0
LPM0_LF_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_LF_VCORE1	LDO based low frequency active mode, core voltage level 1
LPM0_LF_VCORE1	Same as above, except that CPU is OFF (no code execution)
LPM3_VCORE0	LDO based low-power mode with full state retention, core voltage level 0, RTC and WDT can be active
LPM3_VCORE1	LDO based low-power mode with full state retention, core voltage level 1, RTC and WDT can be active
LPM4_VCORE0	LDO based low-power mode with full state retention, core voltage level 0, all peripherals disabled.
LPM4_VCORE1	LDO based low-power mode with full state retention, core voltage level 1, all peripherals disabled
LPM3.5	LDO based low-power mode, core voltage level 0, no retention of peripheral registers, RTC and WDT can be active
LPM4.5	Core voltage turned off, wake-up only through Pin Reset or Wake-up capable I/O's

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6.7.4 Clock System (CS)

The CS contains the sources of the various clocks in the device and also controls the mapping between sources and the clock domains in the device.

6.7.4.1 LFXT

The LFXT supports 32.768-kHz low-frequency crystals.

6.7.4.2 HFXT

The HFXT supports high-frequency crystals up to 48 MHz.

6.7.4.3 DCO

The DCO is a power-efficient tunable internal oscillator that generates up to 48 MHz. It also supports a high-precision mode when using an external precision resistor.

6.7.4.4 Very Low-Power Low-Frequency Oscillator (VLO)

The VLO is an ultra-low-power internal oscillator that generates a low-accuracy clock at typical frequency of 9.4 kHz.

6.7.4.5 Low Frequency Reference Oscillator (REFO)

The REFO can be used as an alternate low-power lower-accuracy source of a 32.768-kHz clock instead of the LFXT. REFO can also be programmed to generate a 128-kHz clock.

6.7.4.6 Module Oscillator (MODOSC)

The MODOSC is an internal clock source that has a very low latency wake-up time. MODOSC is factory-calibrated to a frequency of 25 MHz. It is typically used to supply a 'clock on request' to modules like the ADC (when in 1-Msps conversion mode).

6.7.4.7 System Oscillator (SYSOSC)

The SYSOSC is a lower-frequency version of the MODOSC and is factory calibrated to a frequency of 5 MHz. It drives the ADC sampling clock in the 200-ksps conversion mode. In addition, it is also used for timing of various system-level control and management operations.

6.7.4.8 Fail-Safe Mechanisms

All clock sources that operate with external components have a built-in fail-safe mechanism that automatically switches to the relevant backup source, thereby ensuring that spurious or unstable clocks never impact the device behavior.

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6.7.5 System Controller (SYSCTL)

The SYSCTL is a set of various miscellaneous features of the device, including SRAM bank configuration, RSTn/NMI function selection, and peripheral halt control. In addition, the SYSCTL enables device security features like JTAG and SWD lock and IP protection, which can be used to protect unauthorized accesses either to the entire device memory map or to certain selected regions of the flash. Table 6-17 lists the registers that are part of SYSCTL. Only the offsets of the registers are listed—the entire addresses are listed with the complete register definitions elsewhere this data sheet.

Table 6-17. SYSCTL Registers

OFFSET	ACRONYM	REGISTER NAME	SECTION
000h	SYS_REBOOT_CTL	Reboot Control Register	Section 6.7.1.2.1
004h	SYS_NMI_CTLSTAT	NMI Control and Status Register	Section 6.6.1.1
008h	SYS_WDTRESET_CTL	Watchdog Reset Control Register	Section 6.8.7.1
00Ch	SYS_PERIHALT_CTL	Peripheral Halt Control Register	Section 6.9.2
010h	SYS_SRAM_SIZE	SRAM Size Register	Section 6.3.2.3.1
014h	SYS_SRAM_BANKEN	SRAM Bank Enable Register	Section 6.3.2.3.2
018h	SYS_SRAM_BANKRET	SRAM Bank Retention Control Register	Section 6.3.2.3.3
020h	SYS_FLASH_SIZE	Flash Size Register	Section 6.3.1.1.1
030h	SYS_DIO_GLTFLT_CTL	Digital I/O Glitch Filter Control Register	Section 6.8.1.1.1

NOTE

As is the case with the Cortex-M4 system control registers (housed on the internal PPB space), the System Controller module registers are mapped to the Cortex-M4 external PPB. This keeps the System Controller module accessible even when the Hard and/or Soft resets are active.

6.8 Peripherals

6.8.1 Digital I/O

There are up to 10 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt capability is available on ports P1 through P6.
- Wake-up capability from LPM3, LPM4, LPM3.5, and LPM4.5 modes over ports P1 through P6.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or in pairs (16bit widths).
- Capacitive Touch functionality is supported on all pins of ports P1 through P10 and PJ.
- Glitch filtering capability on selected digital I/Os.

6.8.1.1 Glitch Filtering on Digital I/Os

Some of the interrupt and wake-up capable digital I/Os have the capability to suppress glitches through the use of analog glitch filter to prevent unintentional interrupt or wake-up during device operation. The analog filter will suppress a minimum of 250ns wide glitches. The glitch filter on these selected digital I/Os is enabled by default. If the glitch filtering capability is not required in the application there is a provision to bypass them by programming the SYS_DIO_GLTFLT_CTL register. When GLTFLT_EN bit in this register is cleared then glitch filters on all the digital I/Os are bypassed at once. The glitch filter is automatically bypassed on a digital I/O when it is configured for peripheral or analog functionality by programming the respective PySEL0.x, PySEL1.x registers.

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NOTE

The glitch filter is implemented on the following digital I/Os on MSP432P401x devices: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.

6.8.1.1.1 Digital I/O Glitch Filter Control Register [Address = E004_0030h]

Figure 6-14. SYS_DIO_GLTFLT_CTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															GLTFLT_EN
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	rw-1

Table 6-18. SYS_DIO_GLTFLT_CTL Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-1	Reserved	R	0h	Reserved. Always reads 0h.
0	GLTFLT_EN	RW	1h	0b = Disables glitch filter on the digital I/Os. 1b = Enables glitch filter on the digital I/Os.

6.8.2 Port Mapping Controller (PMAPCTL)

The port mapping controller allows flexible and reconfigurable mapping of digital functions.

6.8.2.1 Port Mapping Definitions

The port mapping controller on MSP432P401x devices allows reconfigurable mapping of digital functions over ports P2, P3, and P7.

Table 6-19. Port Mapping, Mnemonics, and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_UCA0CLK	eUSCI_A0 clock input/output (direction controlled by eUSCI)	
2	PM_UCA0RXD	eUSCI_A0 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA0SOMI	eUSCI_A0 SPI slave out master in (direction controlled by eUSCI)	
3	PM_UCA0TXD	eUSCI_A0 UART TXD (direction controlled by eUSCI – Output)	
	PM_UCA0SIMO	eUSCI_A0 SPI slave in master out (direction controlled by eUSCI)	
4	PM_UCB0CLK	eUSCI_B0 clock input/output (direction controlled by eUSCI)	
5	PM_UCB0SDA	eUSCI_B0 I^2C data (open drain and direction controlled by eUSCI)	
	PM_UCB0SIMO	eUSCI_B0 SPI slave in master out (direction controlled by eUSCI)	
6	PM_UCB0SCL	eUSCI_B0 I^2C clock (open drain and direction controlled by eUSCI)	
	PM_UCB0SOMI	eUSCI_B0 SPI slave out master in (direction controlled by eUSCI)	
7	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
8	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
9	PM_UCA1RXD	eUSCI_A1 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA1SOMI	eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
10	PM_UCA1TXD	eUSCI_A1 UART TXD (direction controlled by eUSCI – Output)	
	PM_UCA1SIMO	eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
11	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	

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Table 6-19. Port Mapping, Mnemonics, and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
12	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
13	PM_UCA2RXD	eUSCI_A2 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA2SOMI	eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
14	PM_UCA2TXD	eUSCI_A2 UART TXD (direction controlled by eUSCI – Output)	
	PM_ UCA2SIMO	eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
15	PM_UCB2STE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
16	PM_UCB2CLK	eUSCI_B2 clock input/output (direction controlled by eUSCI)	
17	PM_UCB2SDA	eUSCI_B2 I^2C data (open drain and direction controlled by eUSCI)	
	PM_UCB2SIMO	eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)	
18	PM_UCB2SCL	eUSCI_B2 I^2C clock (open drain and direction controlled by eUSCI)	
	PM_UCB2SOMI	eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)	
19	PM_TA0.0	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
20	PM_TA0.1	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
21	PM_TA0.2	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
22	PM_TA0.3	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
23	PM_TA0.4	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
24	PM_TA1.1	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
25	PM_TA1.2	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
26	PM_TA1.3	TA1 CCR3 capture input CCI3A	TA1 CCR3 compare output Out3
27	PM_TA1.4	TA1 CCR4 capture input CCI4A	TA1 CCR4 compare output Out4
28	PM_TA0CLK	Timer_A0 external clock input	None
	PM_C0OUT	None	Comparator-E0 output
29	PM_TA1CLK	Timer_A1 external clock input	None
	PM_C1OUT	None	Comparator-E1 output
30	PM_DMAE0	DMAE0 input	None
	PM_SMCLK	None	SMCLK
31 (0FFh)(1)	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 31. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

Table 6-20. Default Mapping

PIN NAME	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P2.0/PM_UCA1STE	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
P2.1/PM_UCA1CLK	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
P2.2/PM_UCA1RXD/ PM_UCA1SOMI	PM_UCA1RXD/ PM_UCA1SOMI	eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
P2.3/PM_UCA1TXD/ PM_UCA1SIMO	PM_UCA1TXD/ PM_UCA1SIMO	eUSCI_A1 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
P2.4/PM_TA0.1(1)	PM_TA0.1	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
P2.5/PM_TA0.2(1)	PM_TA0.2	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
P2.6/PM_TA0.3(1)	PM_TA0.3	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
P2.7/PM_TA0.4(1)	PM_TA0.4	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
P3.0/PM_UCA2STE	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.1/PM_UCA2CLK	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
P3.2/PM_UCA2RXD/ PM_UCA2SOMI	PM_UCA2RXD/ PM_UCA2SOMI	eUSCI_A2 UART RXD (direction controlled by eUSCI – input)/ eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	

(1) Not available on the 64-pin RGC package.

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Table 6-20. Default Mapping (continued)

PIN NAME	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P3.3/PM_UCA2TXD/ PM_UCA2SIMO	PM_UCA2TXD/ PM_UCA2SIMO	eUSCI_A2 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
P3.4/PM_UCB2STE	PM_UCB2STE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.5/PM_UCB2CLK	PM_UCB2CLK	eUSCI_B2 clock input/output (direction controlled by eUSCI)	
P3.6/PM_UCB2SIMO/ PM_UCB2SDA	PM_UCB2SIMO/ PM_UCB2SDA	eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)/ eUSCI_B2 I^2C data (open drain and direction controlled by eUSCI)	
P3.7/PM_UCB2SOMI/ PM_UCB2SCL	PM_UCB2SOMI/ PM_UCB2SCL	eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)/ eUSCI_B2 I^2C clock (open drain and direction controlled by eUSCI)	
P7.0/PM_SMCLK/ PM_DMAE0	PM_SMCLK/ PM_DMAE0	DMAE0 input	SMCLK
P7.1/PM_C0OUT/ PM_TA0CLK	PM_C0OUT/ PM_TA0CLK	Timer_A0 external clock input	Comparator-E0 output
P7.2/PM_C1OUT/ PM_TA1CLK	PM_C1OUT/ PM_TA1CLK	Timer_A1 external clock input	Comparator-E1 output
P7.3/PM_TA0.0	PM_TA0.0	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
P7.4/PM_TA1.4/C0.5 (1)	PM_TA1.4	TA1 CCR4 capture input CCI4A	TA1 CCR4 compare output Out4
P7.5/PM_TA1.3/C0.4 (1)	PM_TA1.3	TA1 CCR3 capture input CCI3A	TA1 CCR3 compare output Out3
P7.6/PM_TA1.2/C0.3 (1)	PM_TA1.2	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
P7.7/PM_TA1.1/C0.2 (1)	PM_TA1.1	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1

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6.8.3 Timer_A

Timers TA0, TA1, TA2 and TA3 are 16-bit timers/counters (Timer_A type) with five capture/compare registers each. Each timer supports multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

6.8.3.1 Timer_A Signal Connection Tables

Table 6-21 through Table 6-24 list the interface signals of the Timer_A modules on the device and connections of the interface signals to the corresponding pins or internal signals. The following rules apply to the naming conventions used.

- The first column lists the device level pin or internal signal that sources the clocks and/or triggers into the Timer. The default assumption is that these are pins, unless specifically marked as (internal). Nomenclature used for internal signals is as follows:
  - CxOUT: output from Comparator 'x'.
  - TAx_Cy: Output from Timer 'x', Capture/Compare module 'y'.
- The second column lists the input signals of the Timer module.
- The third column lists the submodule of the Timer and also implies the functionality (Timer, Capture (Inputs or Triggers), or Compare (Outputs or PWM)).
- The fourth column lists the output signals of the Timer module.
- The fifth column lists the device level pin or internal signal that is driven by the outputs of the Timer. The default assumption is that these are pins, unless specifically marked as (internal).

NOTE

The pin names listed in the tables are the complete names. It is the responsibility of the software to ensure that the pin is used in the intended mode for the targeted Timer functionality.

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NOTE

Internal signals that are sourced by the Timer outputs may connect to other modules (other Timers, ADC, etc) in the device (as trigger sources).

Table 6-21. TA0 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.1/PM_C0OUT/PM_TA0CLK	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
C0OUT (internal)	INCLK			
P7.3/PM_TA0.0	CCI0A	CCR0	TA0	P7.3/PM_TA0.0 TA0_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.4/PM_TA0.1	CCI1A	CCR1	TA1	P2.4/PM_TA0.1 TA0_C1 (internal) ADC14 (internal) ADC14SHSx = {1}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.5/PM_TA0.2	CCI2A	CCR2	TA2	P2.5/PM_TA0.2 TA0_C2 (internal) ADC14 (internal) ADC14SHSx = {2}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.6/PM_TA0.3	CCI3A	CCR3	TA3	P2.6/PM_TA0.3 TA0_C3 (internal)
C1OUT (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.7/PM_TA0.4	CCI4A	CCR4	TA4	P2.7/PM_TA0.4 TA0_C4 (internal)
TA1_C4 (Internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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Table 6-22. TA1 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.2/PM_C1OUT/PM_TA1CLK	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
C1OUT (internal)	INCLK			
P8.0/UCB3STE/TA1.0/C0.1	CCI0A	CCR0	TA0	P8.0/UCB3STE/TA1.0/C0.1 TA1_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.7/PM_TA1.1/C0.2	CCI1A	CCR1	TA1	P7.7/PM_TA1.1/C0.2 TA1_C1 (internal) ADC14 (internal) ADC14SHSx = {3}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.6/PM_TA1.2/C0.3	CCI2A	CCR2	TA2	P7.6/PM_TA1.2/C0.3 TA1_C2 (internal) ADC14 (internal) ADC14SHSx = {4}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.5/PM_TA1.3/C0.4	CCI3A	CCR3	TA3	P7.5/PM_TA1.3/C0.4 TA1_C3 (internal)
C1OUT (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.4/PM_TA1.4/C0.5	CCI4A	CCR4	TA4	P7.4/PM_TA1.4/C0.5 TA1_C4 (internal)
TA0_C4 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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Table 6-23. TA2 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P4.2/ACLK/TA2CLK/A11	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 0 (internal)	INCLK			
P8.1/UCB3CLK/TA2.0/C0.0	CCI0A	CCR0	TA0	P8.1/UCB3CLK/TA2.0/C0.0 TA2_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P5.6/TA2.1/VREF+/VeREF+/C1.7	CCI1A	CCR1	TA1	P5.6/TA2.1/VREF+/VeREF+/C1.7 TA2_C1 (internal) ADC14 (internal) ADC14SHSx = {5}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P5.7/TA2.2/VREF-/VeREF-/C1.6	CCI2A	CCR2	TA2	P5.7/TA2.2/VREF-/VeREF-/C1.6 TA2_C2 (internal) ADC14 (internal) ADC14SHSx = {6}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1	CCI3A	CCR3	TA3	P6.6/TA2.3/UCB3SIMO/ UCB3SDA/C1.1 TA2_C3 (internal)
TA3_C3 (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0	CCI4A	CCR4	TA4	P6.7/TA2.4/UCB3SOMI/ UCB3SCL/C1.0 TA2_C4 (internal)
From Capacitive Touch I/O 0 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

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Table 6-24. TA3 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P8.3/TA3CLK/A22	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 1 (internal)	INCLK			
P10.4/TA3.0/C0.7	CCI0A	CCR0	TA0	P10.4/TA3.0/C0.7 TA3_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P10.5/TA3.1/C0.6	CCI1A	CCR1	TA1	P10.5/TA3.1/C0.6 TA3_C1 (internal) ADC14 (internal) ADC14SHSx = {7}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P8.2/TA3.2/A23	CCI2A	CCR2	TA2	P8.2/TA3.2/A23 TA3_C2 (internal)
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P9.2/TA3.3	CCI3A	CCR3	TA3	P9.2/TA3.3 TA3_C3 (internal)
TA2_C3 (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P9.3/TA3.4	CCI4A	CCR4	TA4	P9.3/TA3.4 TA3_C4 (internal)
From Capacitive Touch I/O 1 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

6.8.4 Timer32

Timer32 is an ARM dual 32-bit timer module. It contains two 32-bit timers, each of which can be configured as two independent 16-bit timers. The two timers can generate independent events or a combined event, which can be processed according to application requirements.

6.8.5 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I^2C.

The MSP432P401x devices offer up to four eUSCI_A and four eUSCI_B modules.

6.8.6 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock. It integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset-calibration and temperature compensation. The RTC_C operation is available in LPM3 and LPM3.5 modes to minimize power consumption.

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6.8.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

The watchdog can generate a reset either on a time-out or a password violation. This reset can be configured to generate either a Hard Reset or a Soft Reset into the system. Refer to the *MSP432P4xx Family Technical Reference Manual* for more details.

Table 6-25. WDT_A Clocks

WDTSSELx	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	BCLK

CAUTION

The WDT **must** be set to interval mode before transitioning into the LPM3 or LPM3.5 modes of operation. This allows the WDT event to wake the device and return it to active modes of operation. Using the WDT in watchdog mode may result in nondeterministic behavior due to the generated reset.

6.8.7.1 Watchdog Reset Control Register [Address = E004_3008h]

Figure 6-15. SYS_WDTRESET_CTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														VIOLATION	TIMEOUT
r	r	r	r	r	r	r	r	r	r	r	r	r	r	rw-1	rw-1

Table 6-26. SYS_WDTRESET_CTL Register Description

Bit	Field	Type	Reset	Description
31-2	Reserved	R	0h	Reserved. Reads return 0h
1	VIOLATION	RW	1h	0b = WDT password violation event generates Soft reset 1b = WDT password violation event generates Hard reset
0	TIMEOUT	RW	1h	0b = WDT time-out event generates Soft reset 1b = WDT time-out event generates Hard reset

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CAUTION

The WDT should ideally be configured to generate a Hard Reset into the system. A Soft Reset will reset the CPU, but leave the rest of the system and peripherals unaffected. As a result if the WDT is configured to generate a Soft Reset, the application should assume responsibility for the fact that a Soft Reset can corrupt an ongoing transaction from the CPU into the system.

6.8.8 ADC14

The ADC14 module supports fast, 14-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 14-bit SAR core, sample select control, reference generator and a conversion result buffer. The window comparators with a lower and upper limit allow CPU independent result monitoring through different window comparator interrupt flags.

The available ADC14 external trigger sources are summarized in Table 6-27.

The available multiplexing between internal and external analog inputs of ADC14 is listed in Table 6-28,Table 6-29,Table 6-30.

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Table 6-27. ADC14 Trigger Signal Connections

ADC14SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC14SC)
001	1	TA0_C1
010	2	TA0_C2
011	3	TA1_C1
100	4	TA1_C2
101	5	TA2_C1
110	6	TA2_C2
111	7	TA3_C1

Table 6-28. ADC14 Channel Mapping on 100PZ Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 23	A23	Battery Monitor	ADC14BATMAP
Channel 22	A22	Temperature Sensor	ADC14TCMAP
Channel 21	A21	NA (Reserved)	ADC14CH0MAP
Channel 20	A20	NA (Reserved)	ADC14CH1MAP
Channel 19	A19	NA (Reserved)	ADC14CH2MAP
Channel 18	A18	NA (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as NA or Reserved, it indicates that only the external source is available for that channel.
(2) Refer to theADC14 chapter in the *MSP432P4xx Family Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

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Table 6-29. ADC14 Channel Mapping on 80ZXH Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 15	A15	Battery Monitor	ADC14BATMAP
Channel 14	A14	Temperature Sensor	ADC14TCMAP
Channel 13	A13	NA (Reserved)	ADC14CH0MAP
Channel 12	A12	NA (Reserved)	ADC14CH1MAP
Channel 11	A11	NA (Reserved)	ADC14CH2MAP
Channel 10	A10	NA (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as NA or Reserved, it indicates that only the external source is available for that channel.
(2) Refer to the ADC14 chapter in the *MSP432P4xx Family Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

Table 6-30. ADC14 Channel Mapping on 64RGC Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 11	A11	Battery Monitor	ADC14BATMAP
Channel 10	A10	Temperature Sensor	ADC14TCMAP
Channel 9	A9	NA (Reserved)	ADC14CH0MAP
Channel 8	A8	NA (Reserved)	ADC14CH1MAP
Channel 7	A7	NA (Reserved)	ADC14CH2MAP
Channel 6	A6	NA (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as NA or Reserved, it indicates that only the external source is available for that channel.
(2) Refer to the ADC14 chapter in the *MSP432P4xx Family Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

6.8.9 Comparator_E (COMP_E)

The primary function of the COMP_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

There are two COMP_E modules available on the MSP432P401x devices.

6.8.10 Shared Reference (REF_A)

The REF_A is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. The reference voltage from REF_A can also be switched on to device pin for external use.

6.8.11 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. It supports both a CRC32 and a CRC16 computation.

- The CRC16 computation signature is based on the CRC16-CCITT standard.
- The CRC32 computation signature is based on the CRC32-ISO3309 standard.

6.8.12 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit, 192-bit, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

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6.8.13 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

6.9 Code Development and Debug

The MSP432P401x devices support various methods through which the user can carry out code development and debug on the device.

6.9.1 JTAG and Serial Wire Debug (SWD) Based Development, Debug and Trace

The device supports both 4-pin JTAG and the 2-pin SWD modes of operation. The device is compatible with all standard Cortex-M4 debuggers available in the market today. The debug logic in the device has been designed to remain minimally intrusive to the application state. In low-power modes, the user can enable the debugger to override the state of the PSS, thereby gaining access to debug and trace features.

In 2-pin SWD mode, the TDO pin can be used to export serial wire trace output (SWO) data. In addition, the TDI and TDO pins of the device can be reassigned as user I/Os. Refer to sections Section 6.10.22 and Section 6.10.23 for more details.

NOTE

If the device has activated debug security, debugger accesses into the device is completely disabled. The debugger, however, is still be able to scan the run/halt state of the CPU. Further control of and visibility into the device is possible only after initiating a mass erase of the device flash contents.

6.9.2 Peripheral Halt Control Register [Address = E004_300Ch]

This register allows the user independent control over the functionality of device peripherals during code development and debug. When the CPU is halted, the bits in this register can control whether the corresponding peripheral freezes its operation (such as incrementing, transmit, and receive) or continues its operation (debug remains nonintrusive). The registers of the peripheral remain accessible irrespective of the values in the Halt Control Register

Figure 6-16. SYS_PERIHALT_CTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA	WDTA	ADC14	eUB3	eUB2	eUB1	eUB0	eUA3	eUA2	eUA1	eUA0	T32	TA3	TA2	TA1	TA0
rw-0	rw-1	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 6-31. SYS_PERIHALT_CTL Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-16	Reserved	R	0h	Reserved. Reads return 0h
15	DMA	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
14	WDTA	RW	1h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
13	ADC14	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted

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Table 6-31. SYS_PERIHALT_CTL Register Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
12	eUB3	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
11	eUB2	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
10	eUB1	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
9	eUB0	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
8	eUA3	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
7	eUA2	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
6	eUA1	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
5	eUA0	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
4	T32	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
3	TA3	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
2	TA2	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
1	TA1	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted
0	TA0	RW	0h	0b = IP operation unaffected when CPU is halted 1b = freezes IP operation when CPU is halted

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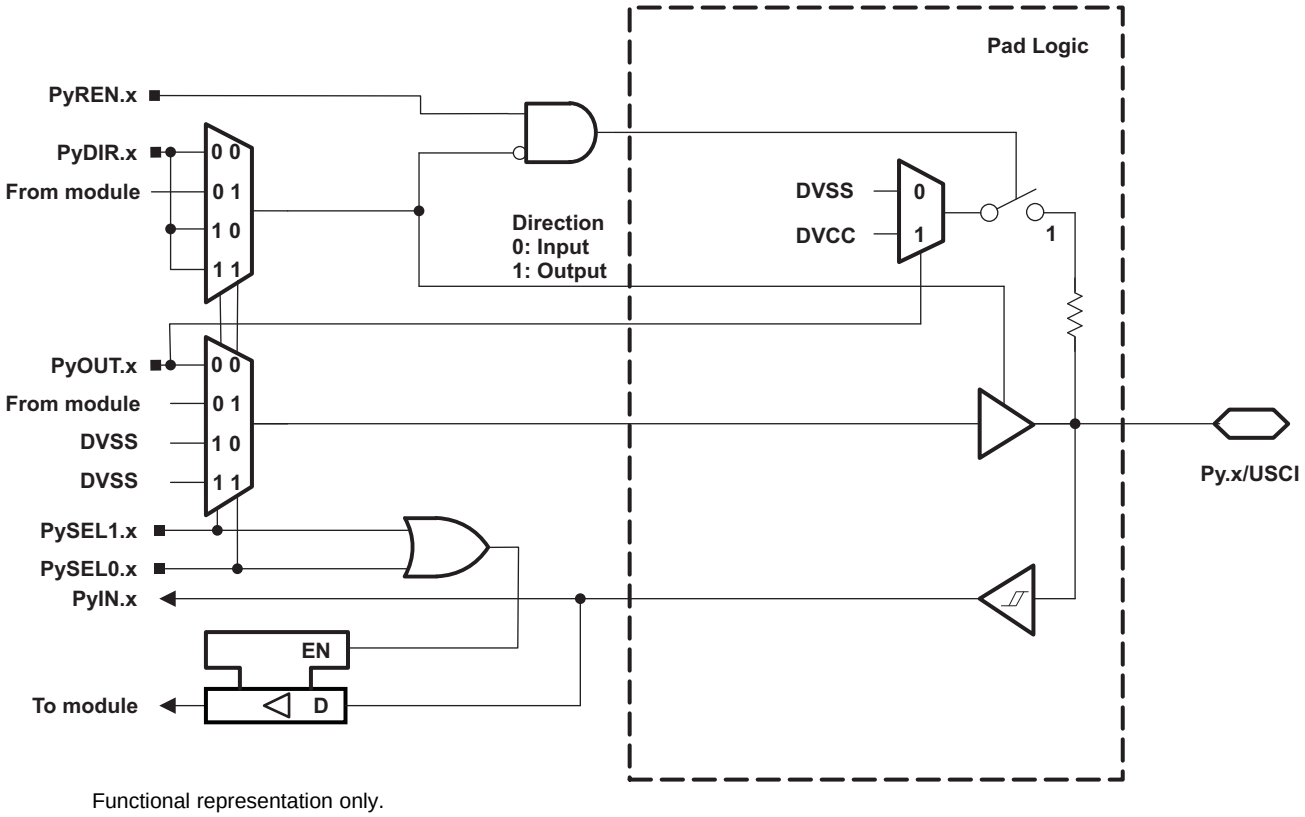
6.9.3 Bootstrap Loader (BSL)

After any POR class reset, the MSP432P401x devices automatically check for presence of user code in the flash. If the user code is not present, the BSL routine is invoked.

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6.10 Input/Output Schematics

6.10.1 Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger



Functional representation only.

Figure 6-17. Py.x/USCI Pin Schematic

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Table 6-32. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA0STE	0	P1.0 (I/O)	I: 0; O: 1	0	0
		UCA0STE	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.1/UCA0CLK	1	P1.1 (I/O)	I: 0; O: 1	0	0
		UCA0CLK	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.2/UCA0RXD/UCA0SOMI	2	P1.2 (I/O)	I: 0; O: 1	0	0
		UCA0RXD/UCA0SOMI	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.3/UCA0TXD/UCA0SIMO	3	P1.3 (I/O)	I: 0; O: 1	0	0
		UCA0TXD/UCA0SIMO	X(2)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.4/UCB0STE	4	P1.4 (I/O)	I: 0; O: 1	0	0
		UCB0STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.5/UCB0CLK	5	P1.5 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.6/UCB0SIMO/UCB0SDA	6	P1.6 (I/O)	I: 0; O: 1	0	0
		UCB0SIMO/UCB0SDA	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_B0 module.

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Table 6-32. Port P1 (P1.0 to P1.7) Pin Functions (continued)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.7/UCB0SOMI/UCB0SCL	7	P1.7 (I/O)	I: 0; O: 1	0	0
		UCB0SOMI/UCB0SCL	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

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6.10.2 Port P2, P2.0 to P2.3, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-17

Table 6-33. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.0/PM_UCA1STE	0	P2.0 (I/O)	I: 0; O: 1	0	0	X
		UCA1STE	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.1/PM_UCA1CLK	1	P2.1 (I/O)	I: 0; O: 1	0	0	X
		UCA1CLK	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.2/PM_UCA1RXD/PM_UCA1SOMI	2	P2.2 (I/O)	I: 0; O: 1	0	0	X
		UCA1RXD/UCA1SOMI	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.3/PM_UCA1TXD/PM_UCA1SIMO	3	P2.3 (I/O)	I: 0; O: 1	0	0	X
		UCA1TXD/UCA1SIMO	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.

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6.10.3 Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-17

Table 6-34. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.0/PM_UCA2STE	0	P3.0 (I/O)	I: 0; O: 1	0	0	X
		UCA2STE	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.1/PM_UCA2CLK	1	P3.1 (I/O)	I: 0; O: 1	0	0	X
		UCA2CLK	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.2/PM_UCA2RXD/PM_UCA2SOMI	2	P3.2 (I/O)	I: 0; O: 1	0	0	X
		UCA2RXD/UCA2SOMI	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.3/PM_UCA2TXD/PM_UCA2SIMO	3	P3.3 (I/O)	I: 0; O: 1	0	0	X
		UCA2TXD/UCA2SIMO	X(2)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.4/PM_UCB2STE	4	P3.4 (I/O)	I: 0; O: 1	0	0	X
		UCB2STE	X(3)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.5/PM_UCB2CLK	5	P3.5 (I/O)	I: 0; O: 1	0	0	X
		UCB2CLK	X(3)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Direction controlled by eUSCI_A2 module.
(3) Direction controlled by eUSCI_B2 module.

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Table 6-34. Port P3 (P3.0 to P3.7) Pin Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.6/PM_UCB2SIMO/PM_UCB2SDA	6	P3.6 (I/O)	I: 0; O: 1	0	0	X
		UCB2SIMO/UCB2SDA	X(3)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P3.7/PM_UCB2SOMI/PM_UCB2SCL	7	P3.7 (I/O)	I: 0; O: 1	0	0	X
		UCB2SOMI/UCB2SCL	X(3)	0	1	default
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

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6.10.4 Port P9, P9.4 to P9.7, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-17

Table 6-35. Port P9 (P9.4 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.4/UCA3STE(2)	4	P9.4 (I/O)	I: 0; O: 1	0	0
		UCA3STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.5/UCA3CLK(2)	5	P9.5 (I/O)	I: 0; O: 1	0	0
		UCA3CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.6/UCA3RXD/UCA3SOMI(2)	6	P9.6 (I/O)	I: 0; O: 1	0	0
		UCA3RXD/UCA3SOMI	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.7/UCA3TXD/UCA3SIMO(2)	7	P9.7 (I/O)	I: 0; O: 1	0	0
		UCA3TXD/UCA3SIMO	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Direction controlled by eUSCI_A3 module.

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6.10.5 Port P10, P10.0 to P10.3, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-17

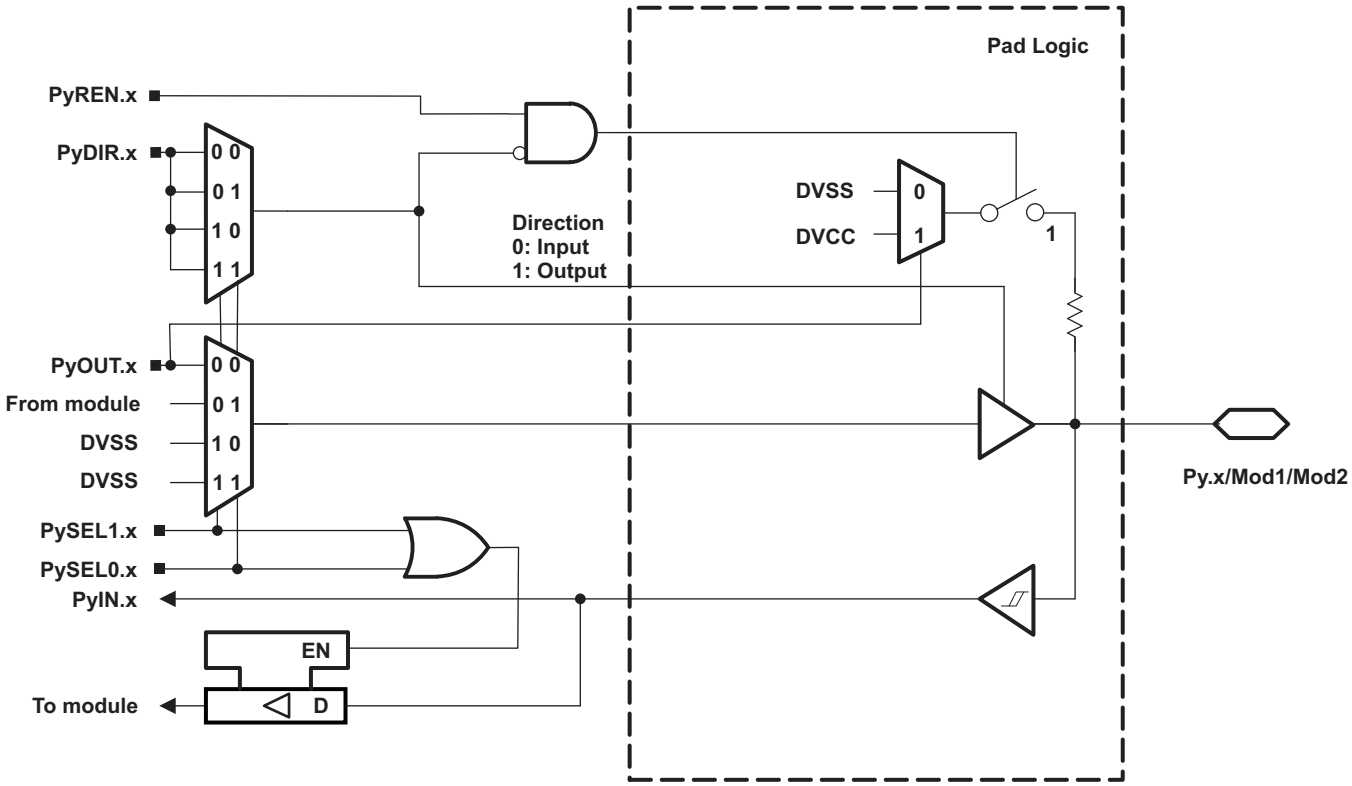
Table 6-36. Port P10 (P10.0 to P10.3) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.0/UCB3STE(2)	0	P10.0 (I/O)	I: 0; O: 1	0	0
		UCB3STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P10.1/UCB3CLK(2)	1	P10.1 (I/O)	I: 0; O: 1	0	0
		UCB3CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P10.2/UCB3SIMO/UCB3SDA(2)	2	P10.2 (I/O)	I: 0; O: 1	0	0
		UCB3SIMO/UCB3SDA	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P10.3/UCB3SOMI/UCB3SCL(2)	3	P10.3 (I/O)	I: 0; O: 1	0	0
		UCB3SOMI/UCB3SCL	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Direction controlled by eUSCI_B3 module.

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6.10.6 Port P2, P2.4 to P2.7, Input/Output With Schmitt Trigger



Functional representation only.

Figure 6-18. Py.x/Mod1/Mod2 Pin Schematic

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Table 6-37. Port P2 (P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.4/PM_TA0.1(2)	4	P2.4 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI1A	0	0	1	default
		TA0.1	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.5/PM_TA0.2(2)	5	P2.5 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI2A	0	0	1	default
		TA0.2	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.6/PM_TA0.3(2)	6	P2.6 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI3A	0	0	1	default
		TA0.3	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.7/PM_TA0.4(2)	7	P2.7 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI4A	0	0	1	default
		TA0.4	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Not available on the 64-pin RGC package.

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6.10.7 Port P7, P7.0 to P7.3, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-18

Table 6-38. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.0/PM_SMCLK/ PM_DMAE0	0	P7.0 (I/O)	I: 0; O: 1	0	0	X
		DMAE0	0	0	1	default
		SMCLK	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P7.1/PM_C0OUT/ PM_TA0CLK	1	P7.1 (I/O)	I: 0; O: 1	0	0	X
		TA0CLK	0	0	1	default
		C0OUT	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P7.2/PM_C1OUT/ PM_TA1CLK	2	P7.2 (I/O)	I: 0; O: 1	0	0	X
		TA1CLK	0	0	1	default
		C1OUT	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P7.3/PM_TA0.0	3	P7.3 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI0A	0	0	1	default
		TA0.0	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care

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6.10.8 Port P9, P9.2 and P9.3, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-18

Table 6-39. Port P9 (P9.2 and P9.3) Pin Functions

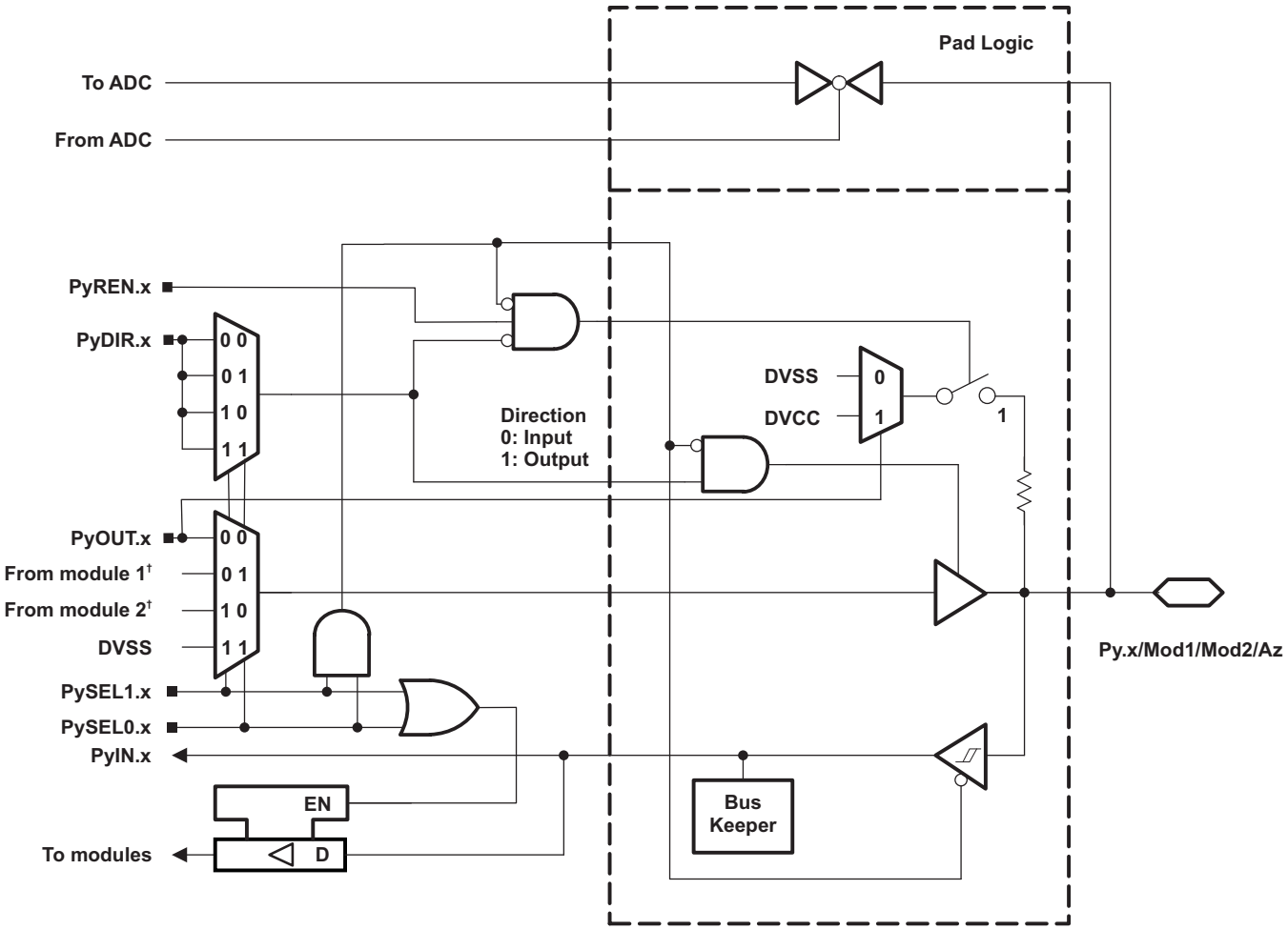
PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.2/TA3.3 (1)	2	P9.2 (I/O)	I: 0; O: 1	0	0
		TA3.CCI3A	0	0	1
		TA3.3	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P9.3/TA3.4 (1)	3	P9.3 (I/O)	I: 0; O: 1	0	0
		TA3.CCI4A	0	0	1
		TA3.4	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) Not available on 80ZXH and 64RGC packages.

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6.10.9 Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger



† Output will be DVSS if module 1 or module 2 function is not available. Refer to pin function tables.
Functional representation only.

Figure 6-19. Py.x/Mod1/Mod2/Az Pin Schematic

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Table 6-40. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/A13(2)	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A13(3)	X	1	1
P4.1/A12(2)	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A12(3)	X	1	1
P4.2/ACLK/TA2CLK/A11	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		ACLK	1		
		TA2CLK	0	1	0
		DVSS	1		
		A11(3)	X	1	1
P4.3/MCLK/RTCCLK/A10	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		MCLK	1		
		N/A	0	1	0
		RTCCLK	1		
		A10(3)	X	1	1
P4.4/HSMCLK/SVMHOUT/ A9	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		HSMCLK	1		
		N/A	0	1	0
		SVMHOUT	1		
		A9(3)	X	1	1
P4.5/A8	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A8(3)	X	1	1
P4.6/A7	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A7(3)	X	1	1

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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Table 6-40. Port P4 (P4.0 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.7/A6	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A6(3)	X	1	1

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6.10.10 Port P5, P5.0 to P5.5, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-19

Table 6-41. Port P5 (P5.0 to P5.5) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.0/A5	0	P5.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A5(2)	X	1	1
P5.1/A4	1	P5.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A4(2)	X	1	1
P5.2/A3	2	P5.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A3(2)	X	1	1
P5.3/A2	3	P5.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A2(2)	X	1	1
P5.4/A1	4	P5.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A1(2)	X	1	1
P5.5/A0	5	P5.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A0(2)	X	1	1

(1) X = Don't care
(2) Setting P5SEL1.x and P5SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.10.11 Port P6, P6.0 and P6.1, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-19

Table 6-42. Port P6 (P6.0 and P6.1) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.0/A15(2)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A15(3)	X	1	1
P6.1/A14(2)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A14(3)	X	1	1

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.10.12 Port P8, P8.2 to P8.7, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-19

Table 6-43. Port P8 (P8.2 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.2/TA3.2/A23(2)	2	P8.2 (I/O)	I: 0; O: 1	0	0
		TA3.CCI2A	0	0	1
		TA3.2	1		
		N/A	0	1	0
		DVSS	1		
		A23(3)	X	1	1
P8.3/TA3CLK/A22(2)	3	P8.3 (I/O)	I: 0; O: 1	0	0
		TA3CLK	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A22(3)	X	1	1
P8.4/A21(2)	4	P8.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A21(3)	X	1	1
P8.5/A20(2)	5	P8.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A20(3)	X	1	1
P8.6/A19(2)	6	P8.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A19(3)	X	1	1
P8.7/A18(2)	7	P8.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A18(3)	X	1	1

(1) X = Don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.10.13 Port P9, P9.0 and P9.1, Input/Output With Schmitt Trigger

Pin Schematic: see Figure 6-19

Table 6-44. Port P9 (P9.0 and P9.1) Pin Functions

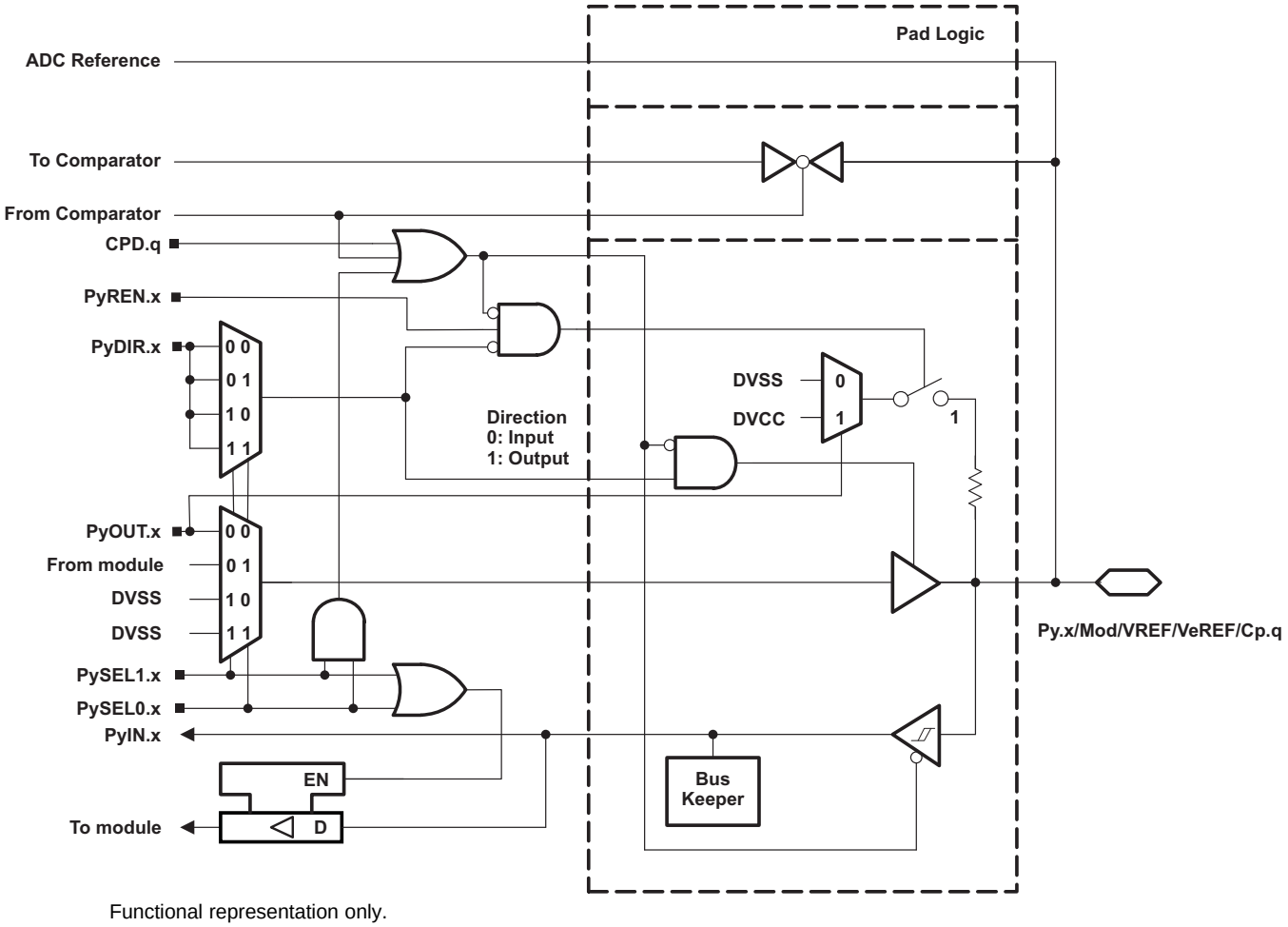
PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.0/A17(2)	0	P9.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A17(3)	X	1	1
P9.1/A16(2)	1	P9.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A16(3)	X	1	1

(1) X = Don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.10.14 Port P5, P5.6 and P5.7, Input/Output With Schmitt Trigger



Functional representation only.

Figure 6-20. Py.x/Mod/VREF/VeREF/Cp.q Pin Schematic

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Table 6-45. Port P5 (P5.6 and P5.7) Pin Functions

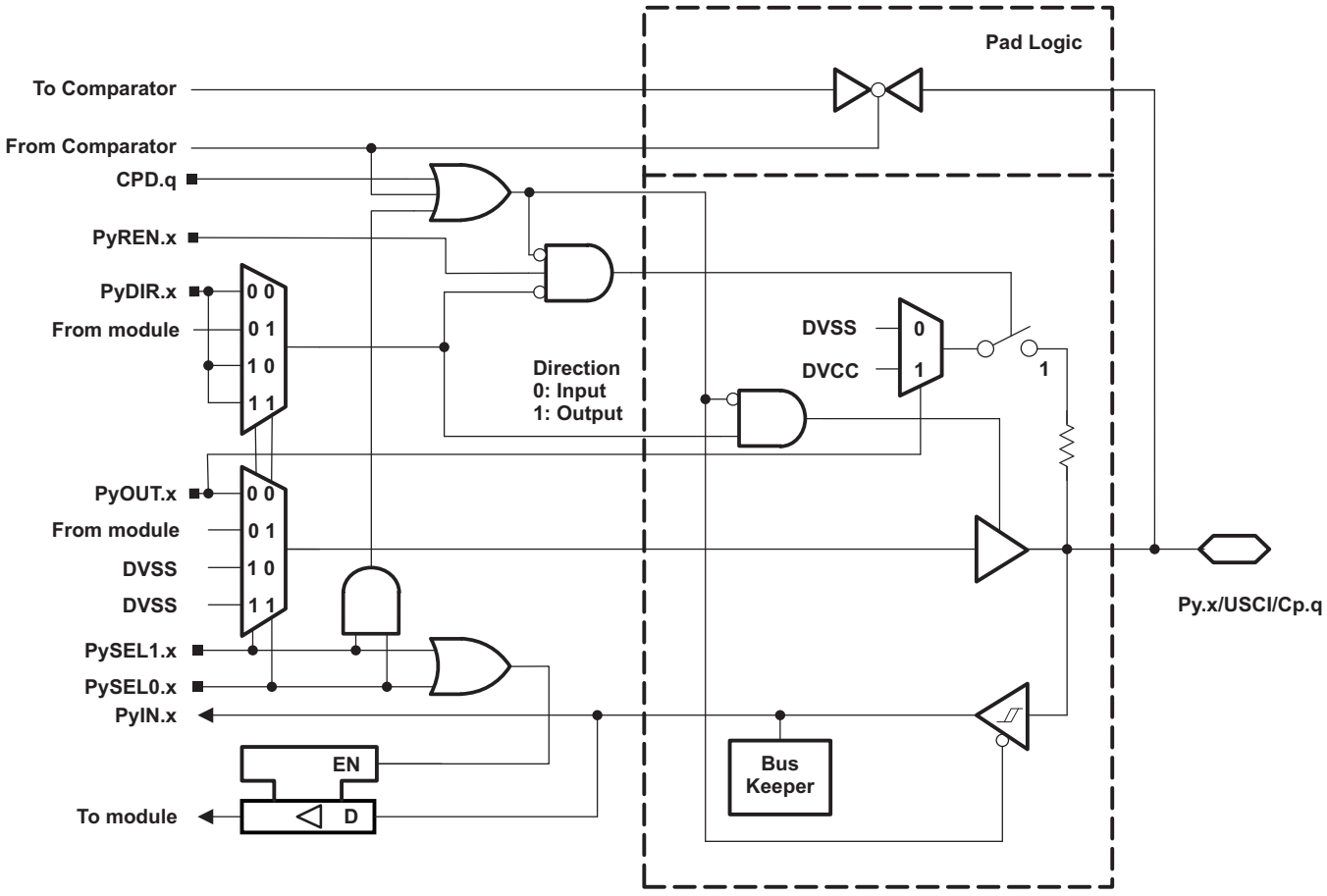
PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.6/TA2.1/VREF+/VeREF+/C1.7	6	P5.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI1A	0	0	1
		TA2.1	1		
		N/A	0	1	0
		DVSS	1		
		VREF+, VeREF+, C1.7(2)(3)	X	1	1
P5.7/TA2.2/VREF-/VeREF-/C1.6	7	P5.7 (I/O)	I: 0; O: 1	0	0
		TA2.CCI2A	0	0	1
		TA2.2	1		
		N/A	0	1	0
		DVSS	1		
		VREF-, VeREF-, C1.6(2)(3)	X	1	1

(1) X = Don't care
(2) Setting P5SEL1.x and P5SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.10.15 Port P6, P6.2 to P6.5, Input/Output With Schmitt Trigger



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Figure 6-21. Py.x/USCI/Cp.q Pin Schematic

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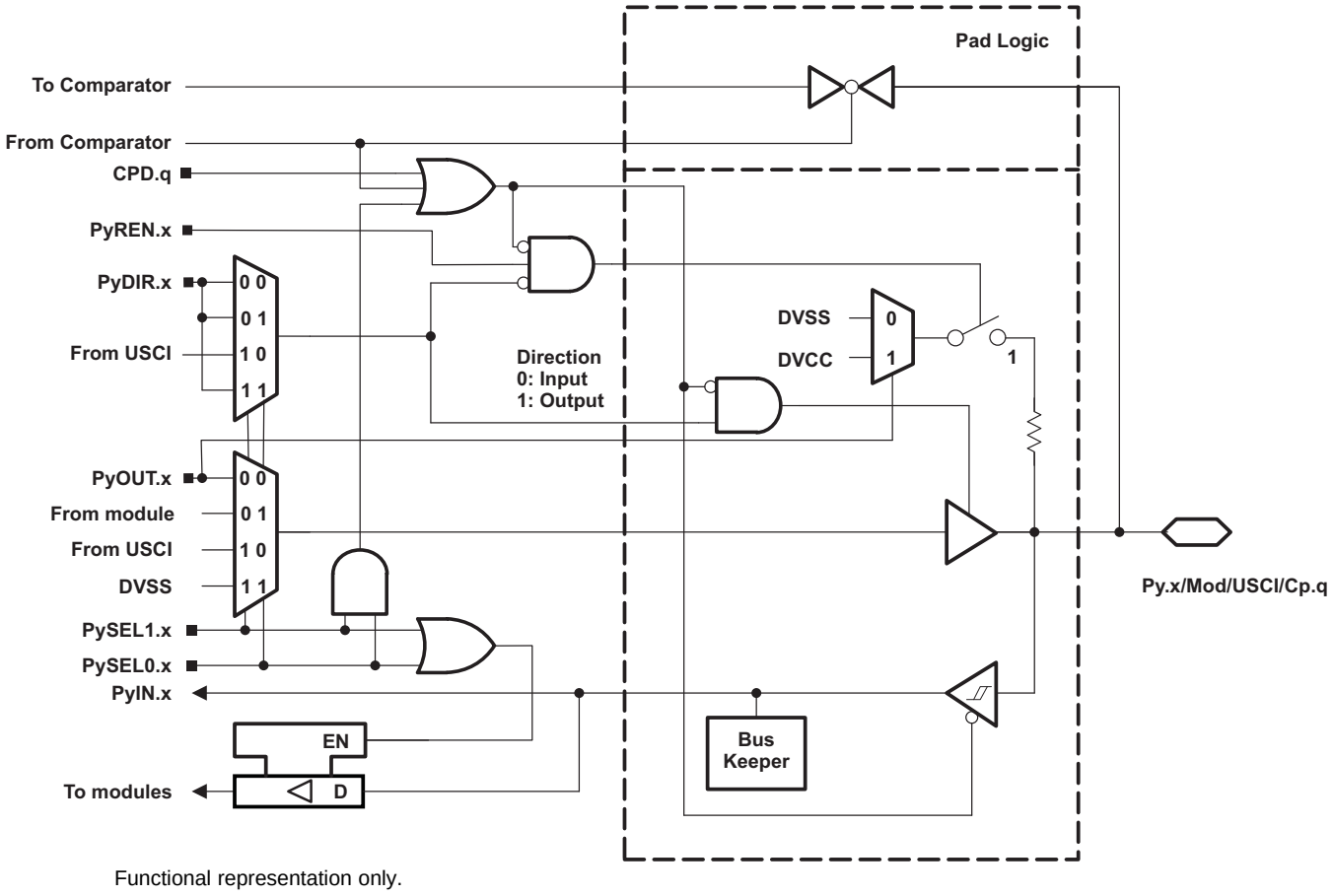
Table 6-46. Port P6 (P6.2 to P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.2/UCB1STE/C1.5(2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		UCB1STE	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.5(4)(5)	X	1	1
P6.3/UCB1CLK/C1.4(2)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		UCB1CLK	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.4(4)(5)	X	1	1
P6.4/UCB1SIMO/UCB1SDA/C1.3(2)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		UCB1SIMO/UCB1SDA	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.3(4)(5)	X	1	1
P6.5/UCB1SOMI/UCB1SCL/C1.2(2)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		UCB1SOMI/UCB1SCL	X(3)	0	1
		N/A	0	1	0
		DVSS	1		
		C1.2(4)(5)	X	1	1

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Direction controlled by eUSCI_B1 module.
(4) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.10.16 Port P6, P6.6 and P6.7, Input/Output With Schmitt Trigger



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Figure 6-22. Py.x/Mod/USCI/Cp.q Pin Schematic

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Table 6-47. Port P6 (P6.6 and P6.7) Pin Functions

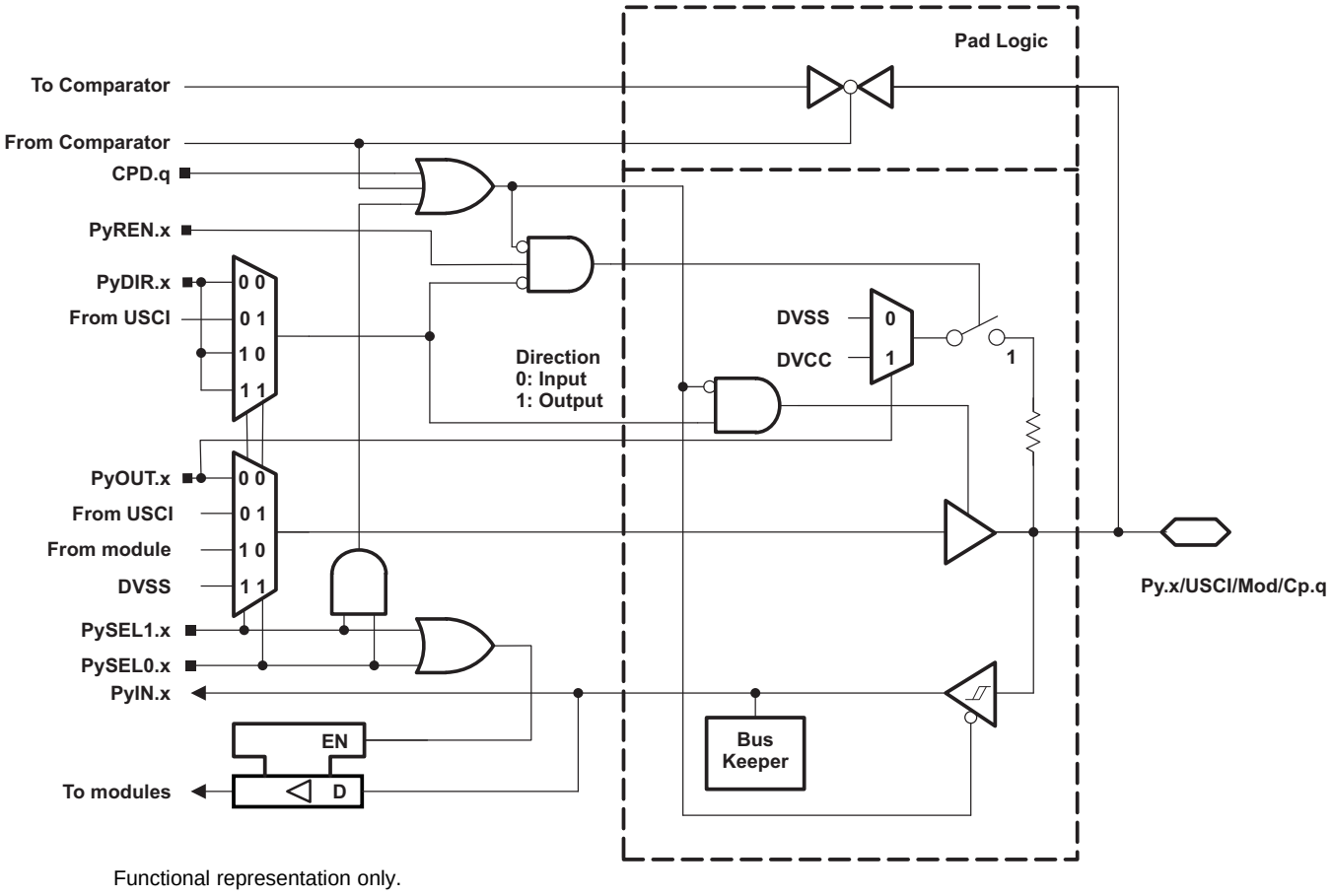
PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1	6	P6.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI3A	0	0	1
		TA2.3	1		
		UCB3SIMO/UCB3SDA	X(2)	1	0
		C1.1(3)(4)	X	1	1
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0	7	P6.7 (I/O)	I: 0; O: 1	0	0
		TA2.CCI4A	0	0	1
		TA2.4	1		
		UCB3SOMI/UCB3SCL	X(2)	1	0
		C1.0(3)(4)	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B3 module.
(3) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.10.17 Port P8, P8.0 and P8.1, Input/Output With Schmitt Trigger



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Figure 6-23. Py.x/USCI/Mod/Cp.q Pin Schematic

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Table 6-48. Port P8 (P8.0 and P8.1) Pin Functions

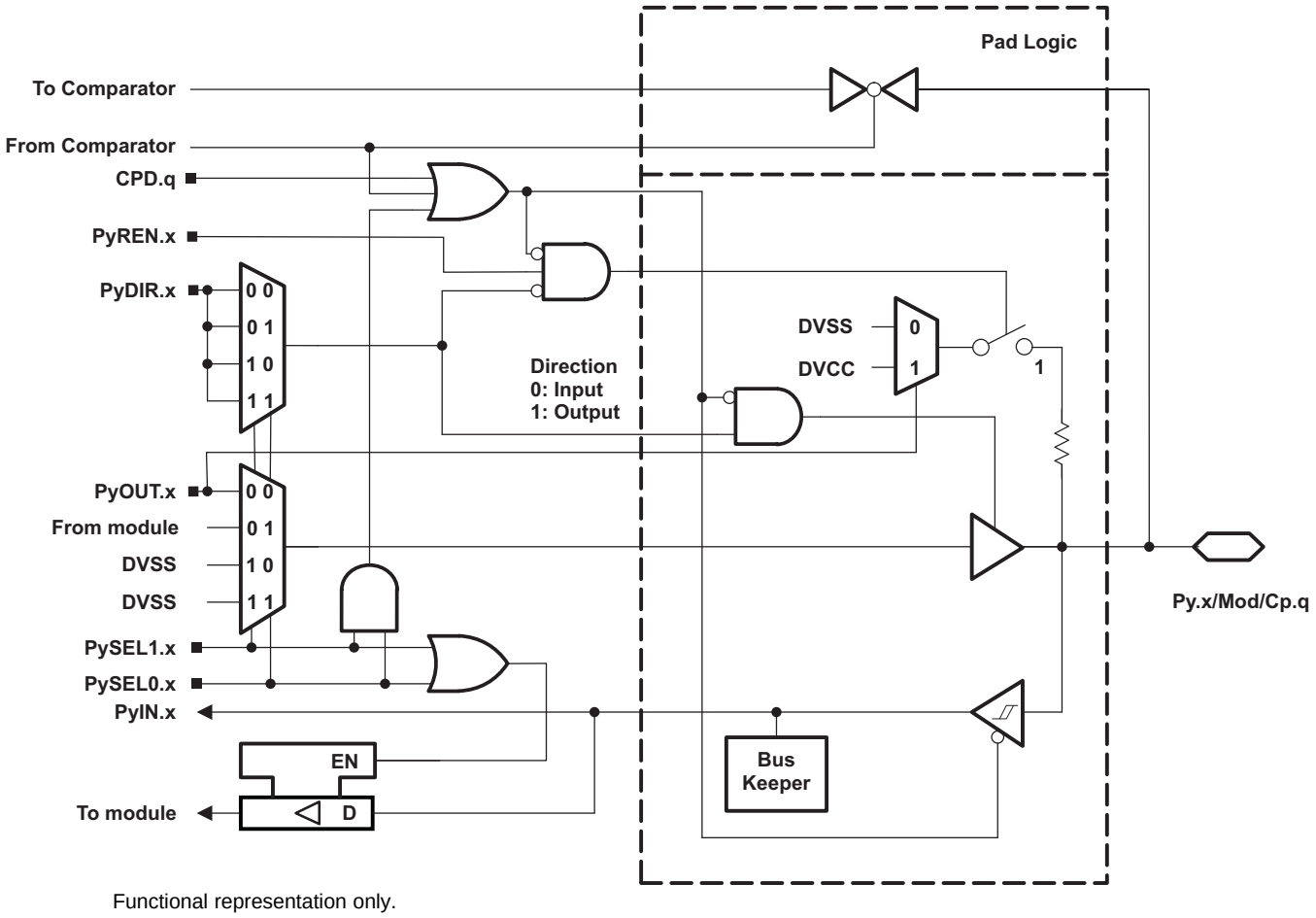
PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.0/UCB3STE/TA1.0/C0.1	0	P8.0 (I/O)	I: 0; O: 1	0	0
		UCB3STE	X(2)	0	1
		TA1.CCI0A	0	1	0
		TA1.0	1		
		C0.1(3)(4)	X	1	1
P8.1/UCB3CLK/TA2.0/C0.0	1	P8.1 (I/O)	I: 0; O: 1	0	0
		UCB3CLK	X(2)	0	1
		TA2.CCI0A	0	1	0
		TA2.0	1		
		C0.0(3)(4)	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B3 module.
(3) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.10.18 Port P10, P10.4 and P10.5, Input/Output With Schmitt Trigger



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Figure 6-24. Py.x/Mod/Cp.q Pin Schematic

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Table 6-49. Port P10 (P10.4 and P10.5) Pin Functions

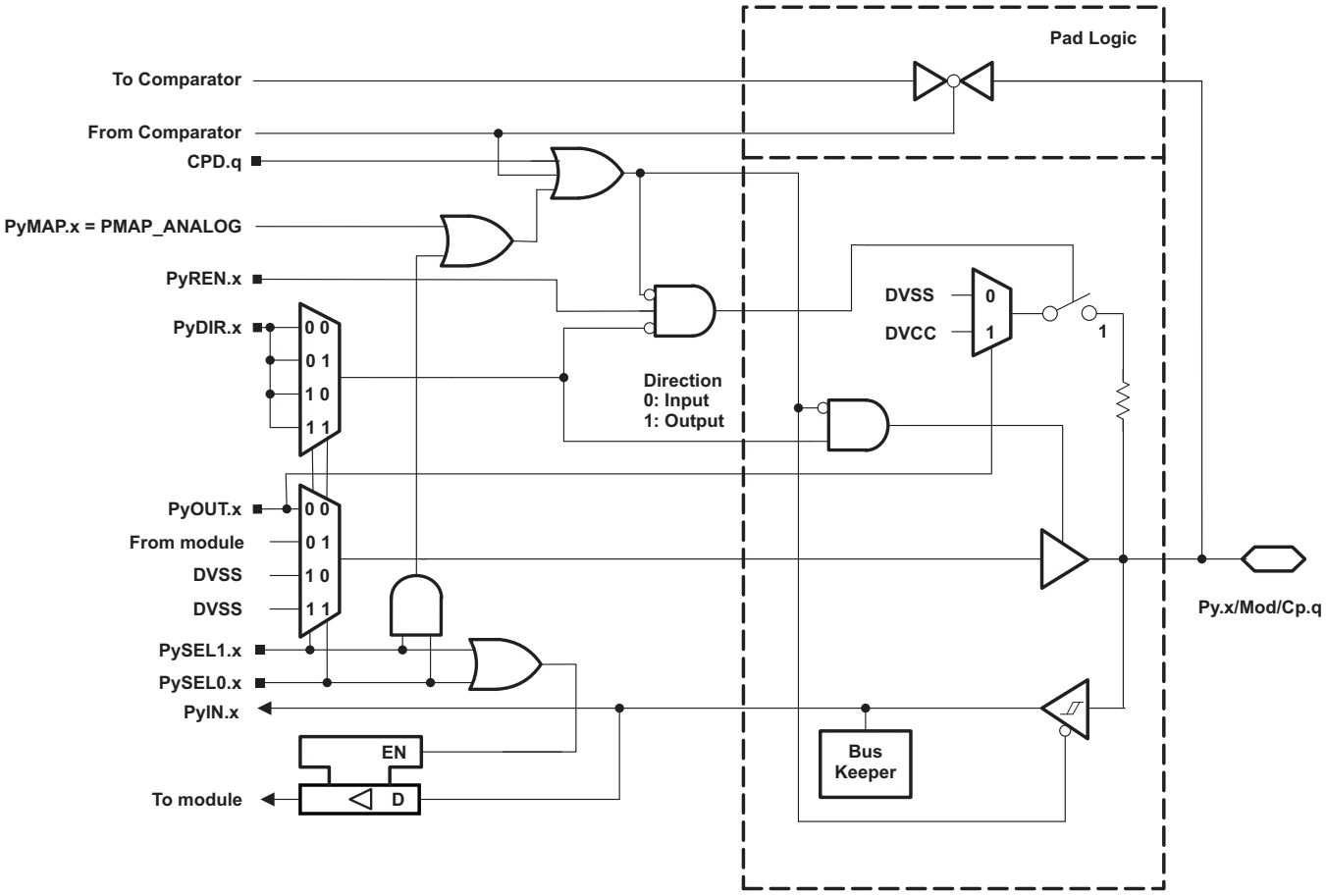
PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.4/TA3.0/C0.7(2)	4	P10.4 (I/O)	I: 0; O: 1	0	0
		TA3.CCI0A	0	0	1
		TA3.0	1		
		N/A	0	1	0
		DVSS	1		
		C0.7(3)(4)	X	1	1
P10.5/TA3.1/C0.6(2)	5	P10.5 (I/O)	I: 0; O: 1	0	0
		TA3.CCI1A	0	0	1
		TA3.1	1		
		N/A	0	1	0
		DVSS	1		
		C0.6(3)(4)	X	1	1

(1) X = Don't care
(2) Not available on 80ZXH and 64RGC packages.
(3) Setting P10SEL1.x and P10SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

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6.10.19 Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger



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Figure 6-25. Py.x/Mod/Cp.q Pin Schematic

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Table 6-50. Port P7 (P7.4 to P7.7) Pin Functions

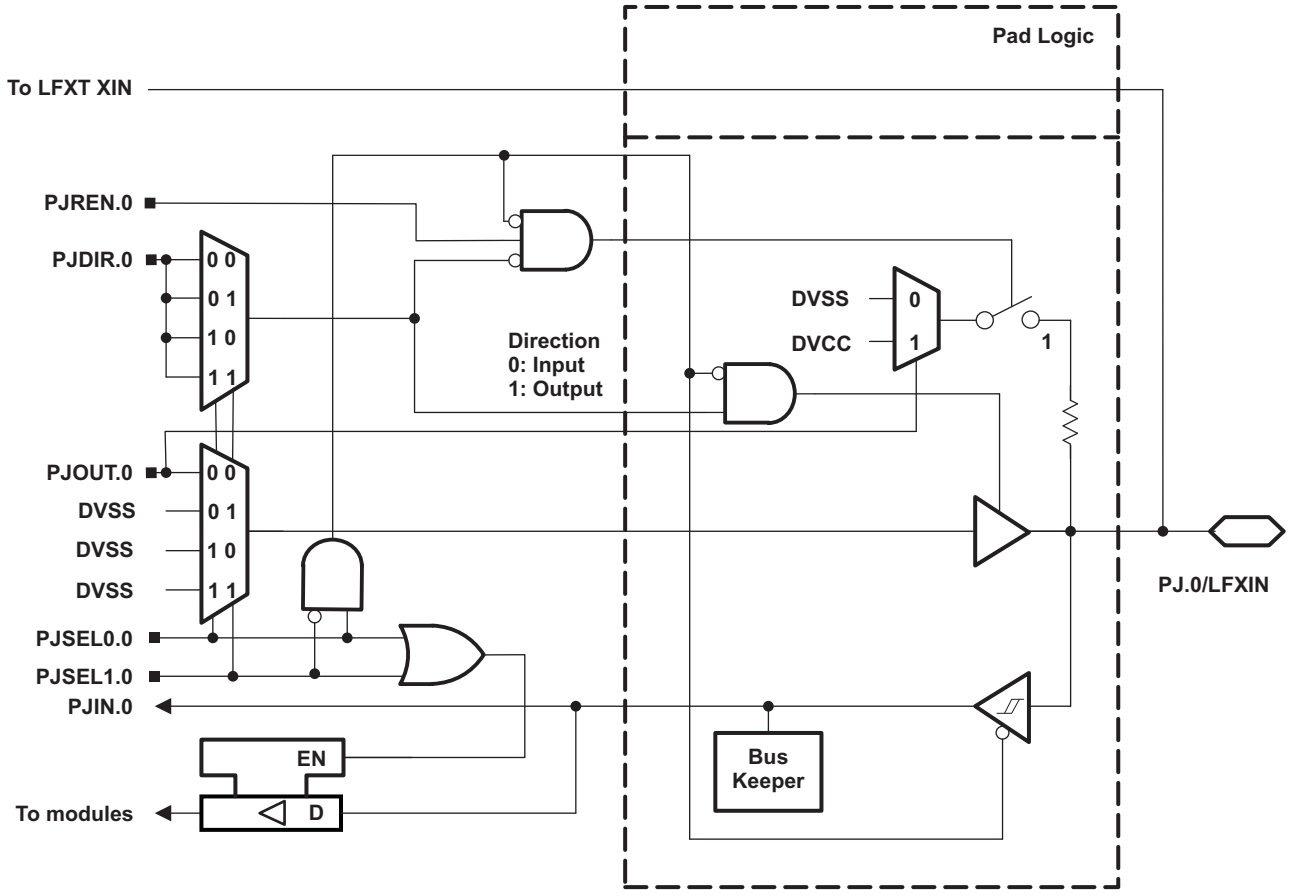
PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.4/PM_TA1.4/C0.5(2)	4	P7.4 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI4A	0	0	1	default
		TA1.4	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.5(3)(4)(5)	X	1	1	X
P7.5/PM_TA1.3/C0.4(2)	5	P7.5 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI3A	0	0	1	default
		TA1.3	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.4(3)(4)(5)	X	1	1	X
P7.6/PM_TA1.2/C0.3(2)	6	P7.6 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI2A	0	0	1	default
		TA1.2	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.3(3)(4)(5)	X	1	1	X
P7.7/PM_TA1.1/C0.2(2)	7	P7.7 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI1A	0	0	1	default
		TA1.1	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.2(3)(4)(5)	X	1	1	X

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting P7SEL1.x and P7SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.
(5) Setting P7MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger independent of P7SEL1.x and P7SEL0.x settings.

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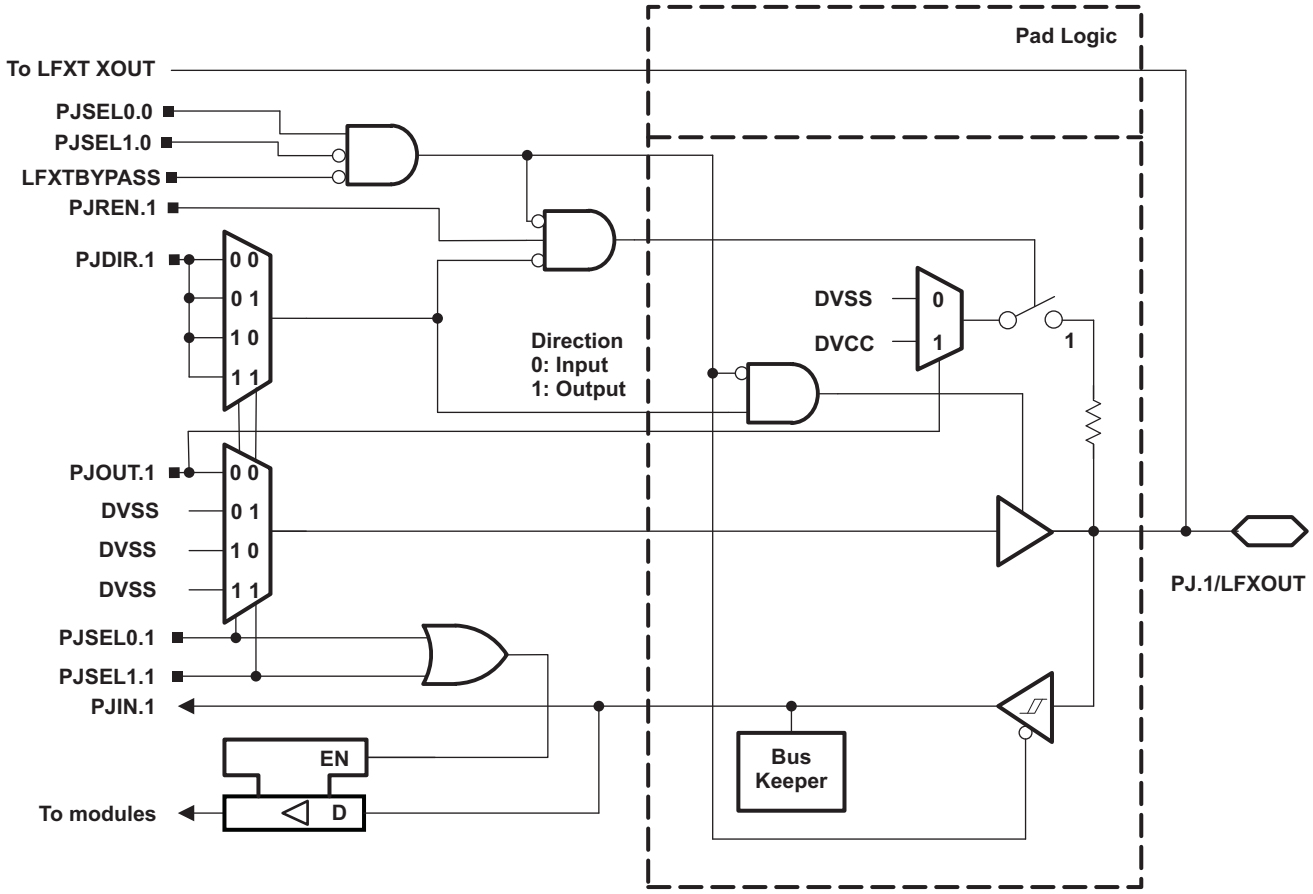
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6.10.20 Port PJ, PJ.0 and PJ.1 Input/Output With Schmitt Trigger



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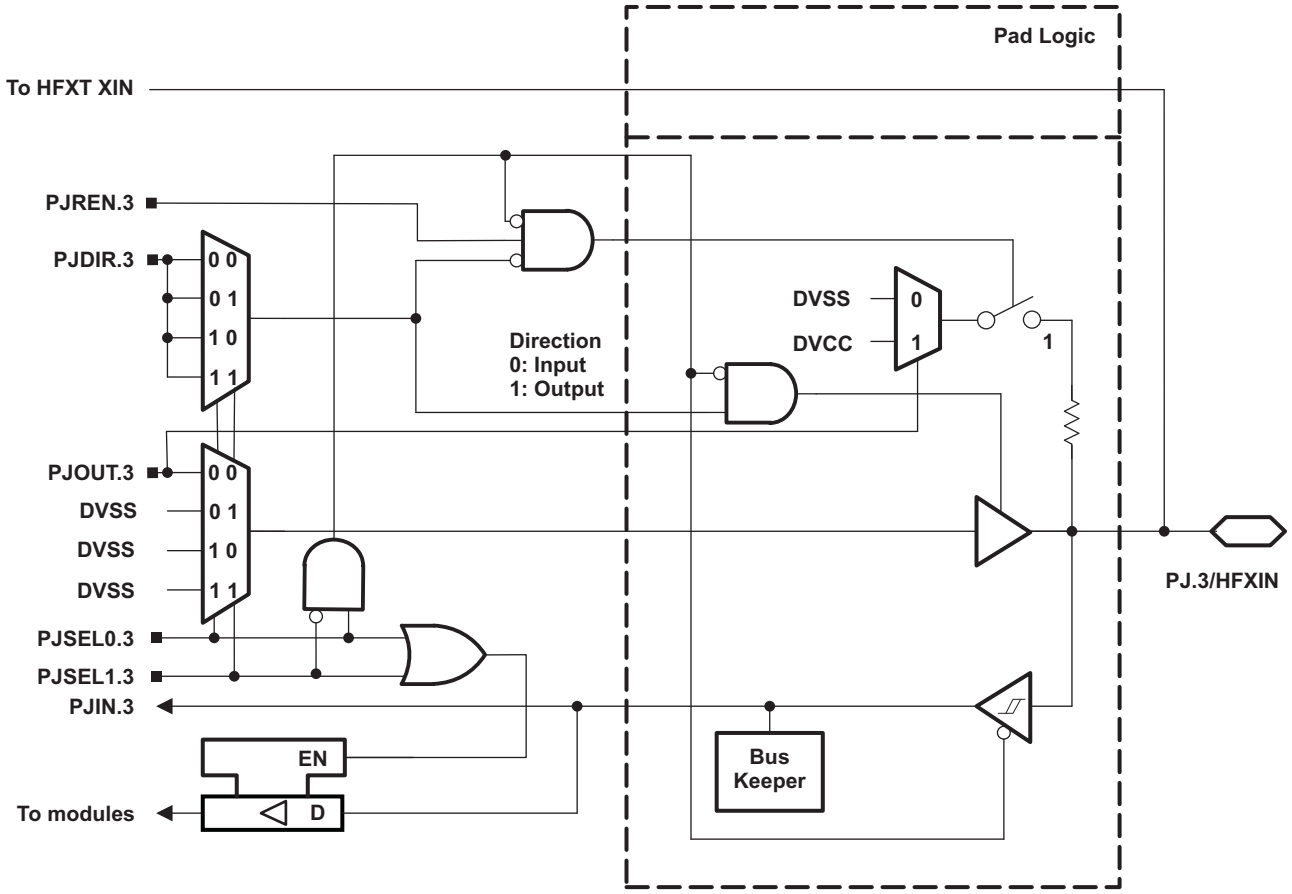
Table 6-51. Port PJ (PJ.0 and PJ.1) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.1	PJSEL0.1	PJSEL1.0	PJSEL0.0	LFXT BYPASS
PJ.0/LFXIN	0	PJ.0 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		DVSS	1					
		LFXIN crystal mode (2)	X	X	X	0	1	0
		LFXIN bypass mode (2)	X	X	X	0	1	1
PJ.1/LFXOUT	1	PJ.1 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		LFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.0 = 0 and PJSEL0.0 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.0 and PJ.1 are configured for crystal operation and PJSEL1.1 and PJSEL0.1 are do not care. When LFXTBYPASS = 1, PJ.0 is configured for bypass operation and PJ.1 is configured as general-purpose I/O.
(3) When PJ.0 is configured in bypass mode, PJ.1 is configured as general-purpose I/O.
(4) With PJSEL0.1 = 1 or PJSEL1.1 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

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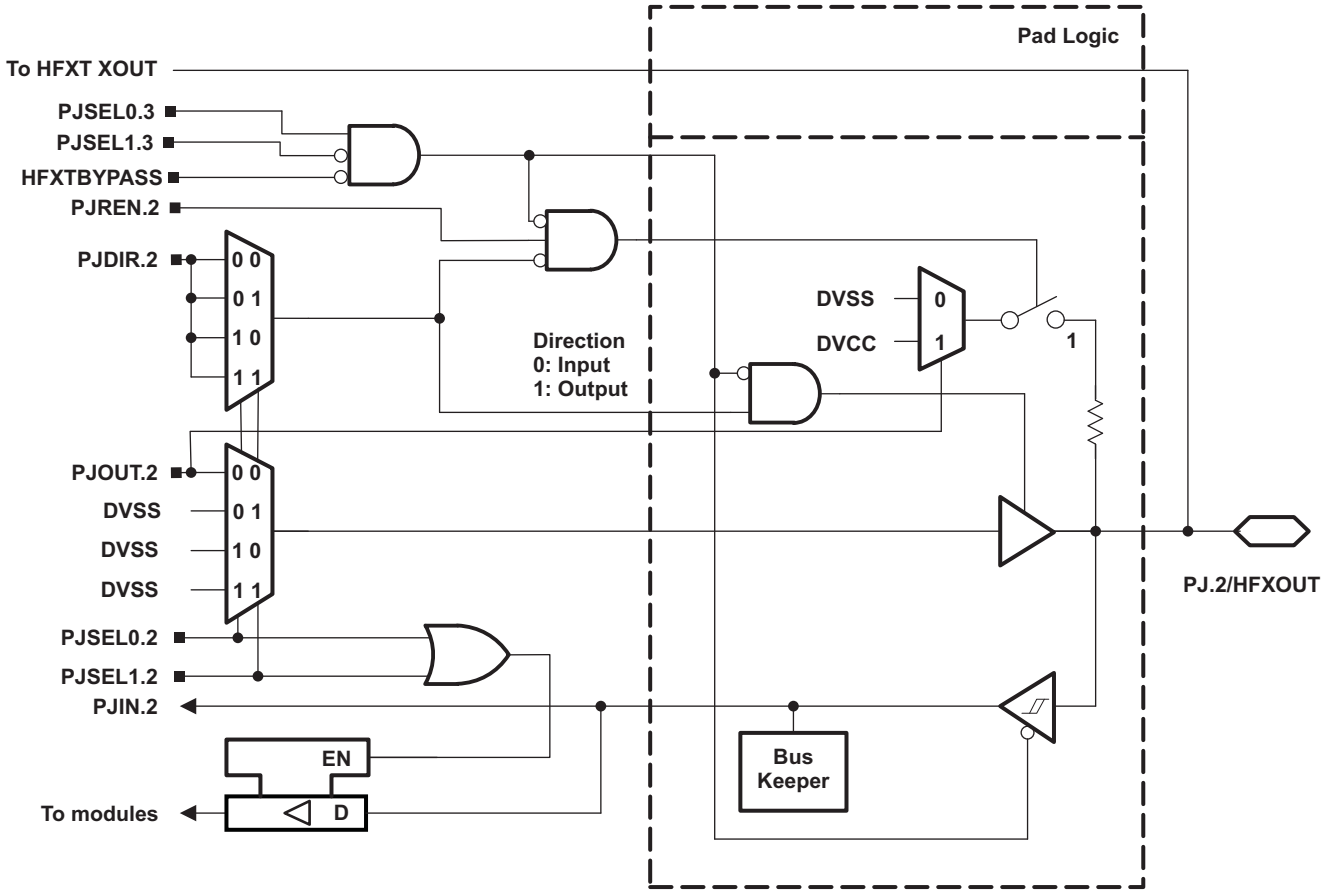
6.10.21 Port PJ, PJ.2 and PJ.3 Input/Output With Schmitt Trigger



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Table 6-52. Port PJ (PJ.2 and PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.2	PJSEL0.2	PJSEL1.3	PJSEL0.3	HFXT BYPASS
PJ.3/HFXIN	3	PJ.3 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		DVSS	1					
		HFXIN crystal mode (2)	X	X	X	0	1	0
		HFXIN bypass mode (2)	X	X	X	0	1	1
PJ.2/HFXOUT	2	PJ.2 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		HFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.3 = 0 and PJSEL0.3 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.2 and PJ.3 are configured for crystal operation and PJSEL1.2 and PJSEL0.2 are do not care. When HFXTBYPASS = 1, PJ.3 is configured for bypass operation and PJ.2 is configured as general-purpose I/O.
(3) When PJ.3 is configured in bypass mode, PJ.2 is configured as general-purpose I/O.
(4) With PJSEL0.2 = 1 or PJSEL1.2 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

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6.10.22 Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger

Table 6-53. Port PJ (PJ.4 to PJ.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)				SWJ MODE OF OPERATION (1)
			PJDIR.x	PJSEL1.x	PJSEL0.x	PJMAPx	
PJ.4/TDI/ADC14CLK (2),	4	PJ.4 (I/O)	I: 0; O: 1	0	0	X	X
		TDI	X	0	1	default (3)	JTAG (4 wire)
		DVcc					SWD (2 wire)
		ADC12CLK	1	1	0	X	X
		DVcc	X	1	1	X	X
PJ.5/TDO/SWO (4), (5)	5	PJ.5 (I/O)	I: 0; O: 1	0	0	X	X
		TDO	X	0	1	default (3)	JTAG (4 wire)
		SWO					SWD (2 wire)
		Hi-Z	X	1	X	X	X

(1) X indicates that the value of the control signal or mode of operation has no effect on the functionality.
(2) This pin is internally pulled up if PJSEL0 is 1.
(3) The 'default' value in the table indicates the functionality that is selected whenever a Hard Reset (or higher class reset) occurs.
(4) This pin is has NO internal pull feature. If used in User IO mode or left unused, it must be pulled to GND through an external pulldown resistor.
(5) After any Hard Reset (or higher class reset), this pin returns to TDO functionality with the SWJ in JTAG (4 wire) mode of operation. If used as a User IO, it reflects the value of the external pullup until the PJSELx bits are reconfigured to the value 00.

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6.10.23 Ports SWCLKTCK and SWDIOTMS With Schmitt Trigger

Table 6-54. Ports SWCLKTCK and SWDIOTMS Pin Functions

PIN NAME	FUNCTION	SWJ MODE OF OPERATION
SWCLKTCK (1)	TCK (input)	JTAG (4 wire)
	SWCLK (input)	SWD (2 wire)
SWDIOTMS (2)	TMS (input)	JTAG (4 wire)
	SWDIO (I/O)	SWD (2 wire)

(1) This pin is internally pulled to DV_{SS}.
(2) This pin is internall pulled to DV_{CC}.

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6.11 Device Descriptors (TLV)

Table 6-56 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP432P401xx devices. Table 6-55 summarizes the Device IDs of the corresponding MSP432P401xx devices.

Table 6-55. Device IDs

DEVICE	DEVICE ID
MSP432P401RIPZ	0000A000h
MSP432P401MIPZ	0000A001h
MSP432P401RIZXH	0000A002h
MSP432P401MIZXH	0000A003h
MSP432P401RIRGC	0000A004h
MSP432P401MIRGC	0000A005h

Table 6-56. Device Descriptor Table(1)

	DESCRIPTION	ADDRESS	VALUE
	TLV checksum	00201000h	per unit
Info Block	Device Info Tag	00201004h	0000000Bh
	Device Info Length	00201008h	00000004h
	Device ID	0020100Ch	See Table 6-55
	HW Revision	00201010h	00000042h
	Boot-code Revision	00201014h	00410042h
	ROM Driver Library Revision	00201018h	01010022h
Die Record	Die Record Tag	0020101Ch	0000000Ch
	Die Record Length	00201020h	00000008h
	Die X Position	00201024h	per unit
	Die Y Position	00201028h	per unit
	Wafer ID	0020102Ch	per unit
	Lot ID	00201030h	per unit
	Reserved	00201034h	per unit
	Reserved	00201038h	per unit
	Reserved	0020103Ch	per unit
	Test Results	00201040h	FFFFFFFFh
Clock System Calibration	Clock System Calibration Tag	00201044h	00000003h
	Clock System Calibration Length	00201048h	00000010h
	DCO IR mode: Frequency calibration	0020104Ch	per unit
	Reserved	00201050h	FFFFFFFFh
	DCO IR mode: Max Positive Tune for DCORSEL 0 to 4	00201054h	00000600h
	DCO IR mode: Max Negative Tune for DCORSEL 0 to 4	00201058h	00001600h
	DCO IR mode: Max Positive Tune for DCORSEL 5	0020105Ch	00000150h
	DCO IR mode: Max Negative Tune for DCORSEL 5	00201060h	00001600h
	DCO IR mode: DCO Constant (K) for DCORSEL 0 to 4	00201064h	3BA20147h
	DCO IR mode: DCO Constant (K) for DCORSEL 5	00201068h	3B9DF117h
	DCO ER mode: Frequency calibration	0020106Ch	per unit
	Reserved	00201070h	FFFFFFFFh
	DCO ER mode: Max Positive Tune for DCORSEL 0 to 4	00201074h	000005A0h
	DCO ER mode: Max Negative Tune for DCORSEL 0 to 4	00201078h	00001600h
	DCO ER mode: Max Positive Tune for DCORSEL 5	0020107Ch	00000140h
	DCO ER mode: Max Negative Tune for DCORSEL 5	00201080h	00001600h
	DCO ER mode: DCO Constant (K) for DCORSEL 0 to 4	00201084h	3BA47ED0h
	DCO ER mode: DCO Constant (K) for DCORSEL 5	00201088h	3B9FE868h

(1) per unit = the contents can differ from device to device

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Table 6-56. Device Descriptor Table[1] (continued)

	DESCRIPTION	ADDRESS	VALUE
ADC14 Calibration	ADC14 Calibration Tag	0020108Ch	00000005h
	ADC14 Calibration Length	00201090h	00000018h
	Reserved	00201094h	FFFFFFFFh
	Reserved	00201098h	FFFFFFFFh
	Reserved	0020109Ch	FFFFFFFFh
	Reserved	002010A0h	FFFFFFFFh
	Reserved	002010A4h	FFFFFFFFh
	Reserved	002010A8h	FFFFFFFFh
	Reserved	002010ACh	FFFFFFFFh
	Reserved	002010B0h	FFFFFFFFh
	Reserved	002010B4h	FFFFFFFFh
	Reserved	002010B8h	FFFFFFFFh
	Reserved	002010BCh	FFFFFFFFh
	Reserved	002010C0h	FFFFFFFFh
	Reserved	002010C4h	FFFFFFFFh
	Reserved	002010C8h	FFFFFFFFh
	Reserved	002010CCh	FFFFFFFFh
	Reserved	002010D0h	FFFFFFFFh
	Reserved	002010D4h	FFFFFFFFh
	Reserved	002010D8h	FFFFFFFFh
	Reserved	002010DCh	FFFFFFFFh
	Reserved	002010E0h	FFFFFFFFh
	Reserved	002010E4h	FFFFFFFFh
	Reserved	002010E8h	FFFFFFFFh
	Reserved	002010ECh	FFFFFFFFh
	Reserved	002010F0h	FFFFFFFFh
REF Calibration	REF Calibration Tag	002010F4h	00000008h
	REF Calibration Length	002010F8h	00000003h
	Reserved	002010FCh	FFFFFFFFh
	Reserved	00201100h	FFFFFFFFh
	Reserved	00201104h	FFFFFFFFh
Random Number	128-bit Random Number Tag	00201108h	0000000Dh
	128-bit Random Number Length	0020110Ch	00000004h
	32-bit Random Number 1	00201110h	per unit
	32-bit Random Number 2	00201114h	per unit
	32-bit Random Number 3	00201118h	per unit
	32-bit Random Number 4	0020111Ch	per unit
BSL Configuration	BSL Configuration Tag	00201120h	0000000Fh
	BSL Configuration Length	00201124h	00000004h
	BSL Peripheral Interface Selection	00201128h	FFC2D0C0h
	BSL Port Interface Configuration for UART	0020112Ch	FCFFFDA0h
	BSL Port Interface Configuration for SPI	00201130h	F0FF9770h
	BSL Port Interface Configuration for I2C	00201134h	FCFFFF72h
TLV End	TLV End Word	00201138h	0BD0E11Dh
	Reserved	0020113Ch-00201FFFh	FFFFFFFFh

PRODUCT PREVIEW

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7 Applications, Implementation, and Layout

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP432™ microcontrollers. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 4.7-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommended for better noise isolation from digital to analog circuits on the board and are especially recommended to achieve high analog accuracy.

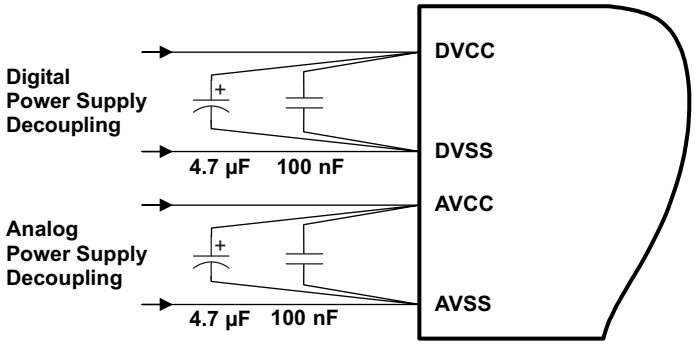


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

The device supports a low-frequency crystal (32.768 kHz) on the LFXT pins and a high-frequency crystal on the HFXT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes.

Figure 7-2 shows a typical connection diagram.

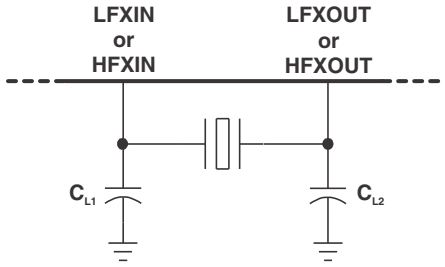


Figure 7-2. Typical Crystal Connection

See the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322) for more information on selecting, testing, and designing a crystal oscillator with the MSP432 devices.

PRODUCT PREVIEW

7.1.3 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Refer to the *Circuit Board Layout Techniques* design guide (SLOA089) for a detailed discussion of printed-circuit-board (PCB) layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See the application report *MSP430 System-Level ESD Considerations* (SLAA530) for guidelines.

7.1.4 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the Absolute Maximum Ratings section. Exceeding the specified limits may cause malfunction of the device.

PRODUCT PREVIEW

7.2 Peripheral and Interface-Specific Design Information

7.2.1 ADC14 Peripheral

7.2.1.1 Partial Schematic

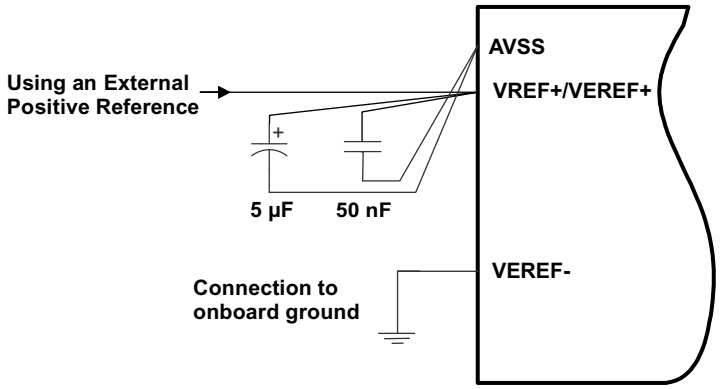


Figure 7-3. ADC14 Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Section 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.

Figure 7-3 shows the recommended decoupling circuit when an external voltage reference is used.

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The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 5-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 50-nF bypass capacitor is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Component that are shown in the partial schematic (see Figure 7-3) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC14, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Tools Support

All MSP432 microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp432.

8.1.1.1 Hardware Features

FAMILY	JTAG	SWD	NUMBER OF BREAKPOINTS	ITM	DWT	FPB
MSP432P4xx	Yes	Yes	4	Yes	Yes	Yes

8.1.1.2 Recommended Hardware Options

8.1.1.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG or SWD. They also feature header pin outs for prototyping. The following table shows the compatible target boards and the supported packages.

DEVICE	PACKAGE	TARGET BOARD
MSP432P401RPZ	100-pin QFP (PZ100)	MSP-TS432PZ100

8.1.1.2.2 Evaluation Kits

Evaluation kits are available for some MSP432 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp432 for details.

8.1.1.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from third party suppliers. See a comprehensive list of available tools at www.ti.com/msp432.

8.1.1.2.4 Production Programmers

Production programmers expedite loading firmware to devices by programming several devices simultaneously. See a comprehensive list of available tools at www.ti.com/msp432.

8.1.1.3 Recommended Software Options

8.1.1.3.1 Integrated Development Environments

Software development tools are available from TI or from third party suppliers. Open source solutions are also available. The MSP432 Family is supported by Code Composer Studio™ IDE (CCS) Version 6 or higher. See a comprehensive list of available tools at www.ti.com/msp432.

8.1.1.3.2 MSPWare

MSPWare is a collection of code examples, data sheets, and other design resources for all MSP430 and MSP432 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 and MSP432 design resources, MSPWare also includes a high-level API called Driver Library. This library makes it easy to program MSP430 or MSP432 hardware. MSPWare is available as a component of CCS or as a stand-alone package. Visit www.ti.com/msp432 to download the stand-alone package.

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8.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP432 MCU devices and support tools. Each MSP432 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP432P401R). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

PMS – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

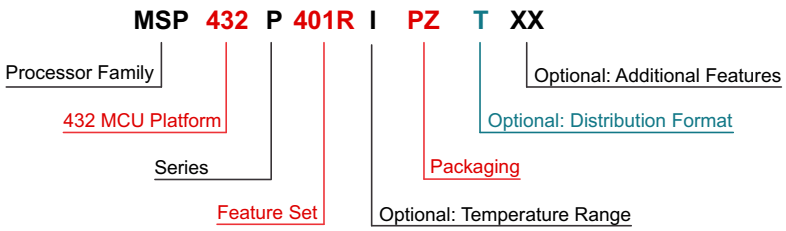
"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). Figure 8-1 provides a legend for reading the complete device name for any family member.

PRODUCT PREVIEW



Processor Family	MSP = Mixed Signal Processor XMS = Experimental Silicon			
432 MCU Platform	TI's 32-bit Low-Power Microcontroller Platform			
Series	P = Performance and Low-Power Series			
Feature Set	**First Digit** 4 = Flash based devices up to 48 MHz	**Second Digit** 0 = General Purpose	**Third Digit** 1 = ADC14	**Fourth Digit** R = 256KB of Flash 64KB of SRAM M = 128KB of Flash 32KB of SRAM
Optional: Temperature Range	S = 0°C to 50°C I = –40°C to 85°C T = –40°C to 105°C			
Packaging	http://www.ti.com/packaging			
Optional: Distribution Format	T = Small Reel R = Large Reel No Markings = Tube or Tray			
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified			

Figure 8-1. Device Nomenclature

8.2 Documentation Support

The following documents describe the MSP432P401x MCUs. Copies of these documents are available on the Internet at www.ti.com.

SLAU356 ***MSP432P4xx Family Technical Reference Manual.*** Detailed information on all of the modules and peripherals available in this device family.

SLAZ610 ***MSP432P401R Device Erratasheet.*** Describes the known exceptions to the functional specifications.

8.2.1 Related Links

Table 8-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP432P401R	Click here	Click here	Click here	Click here	Click here
MSP432P401M	Click here	Click here	Click here	Click here	Click here

PRODUCT PREVIEW

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8.2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.3 Trademarks

MSP430, MSP432, E2E are trademarks of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Ltd.
ULPBench is a registered trademark of Embedded Microprocessor Benchmark Consortium.
All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

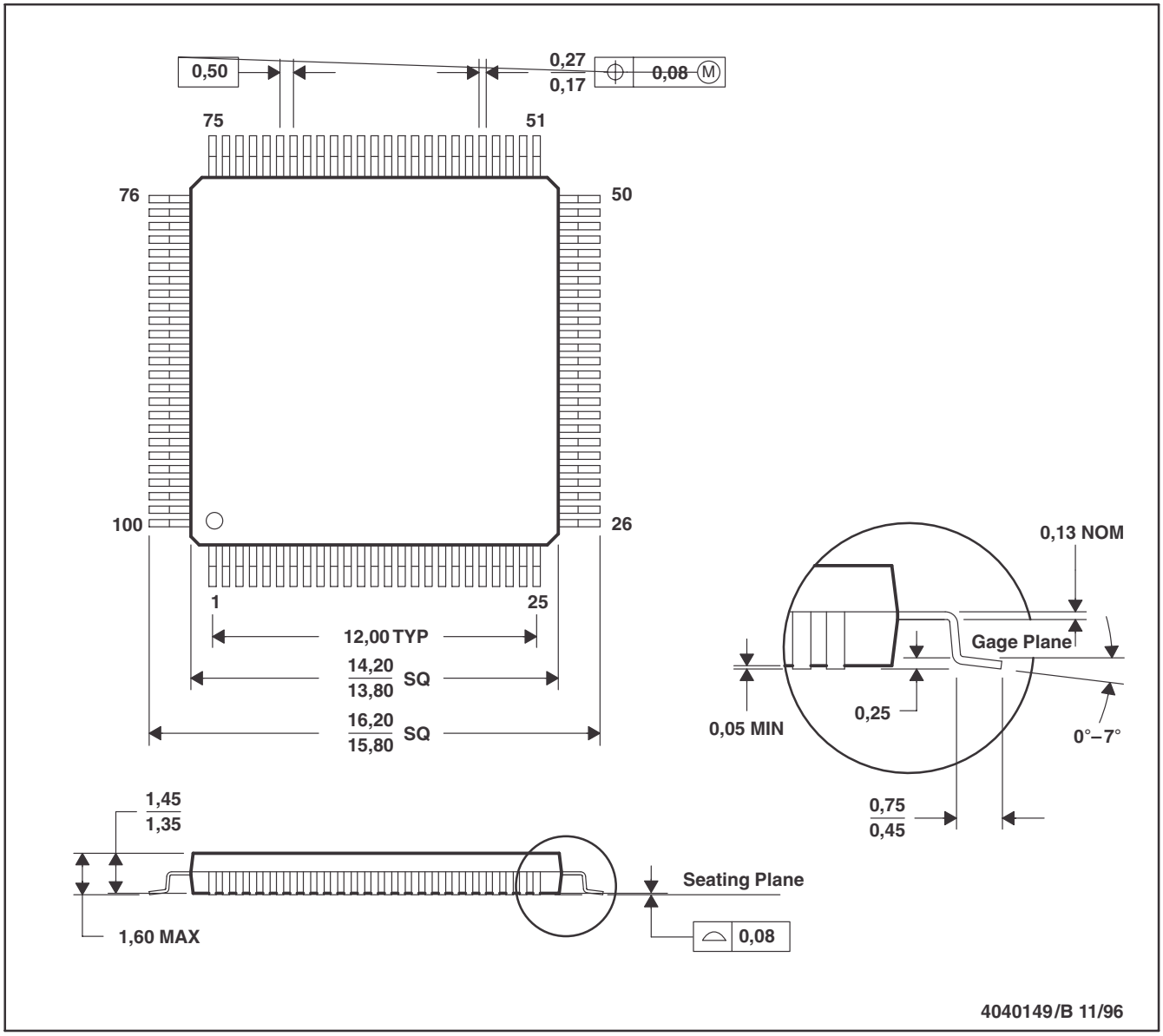
PRODUCT PREVIEW

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**

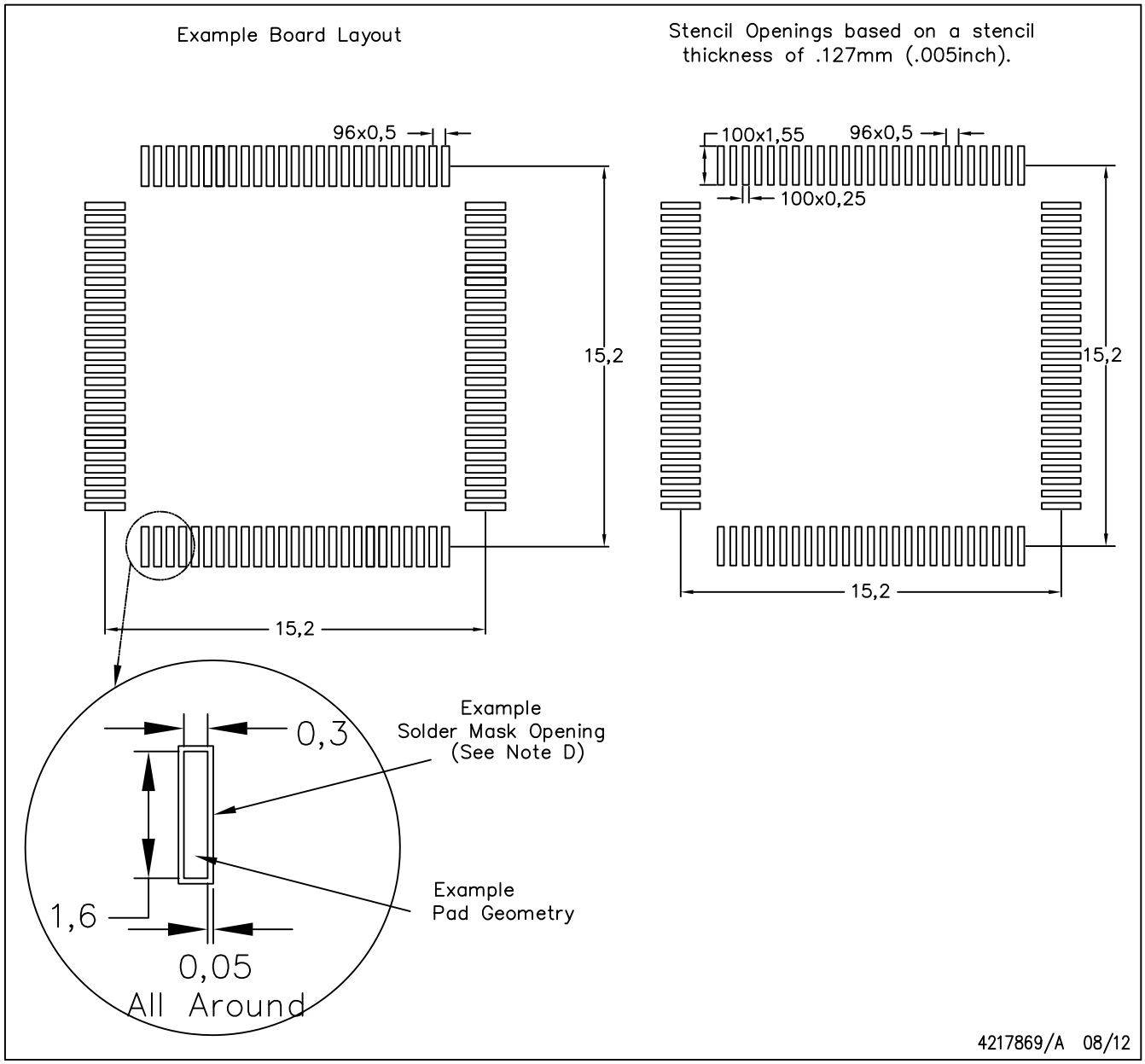


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

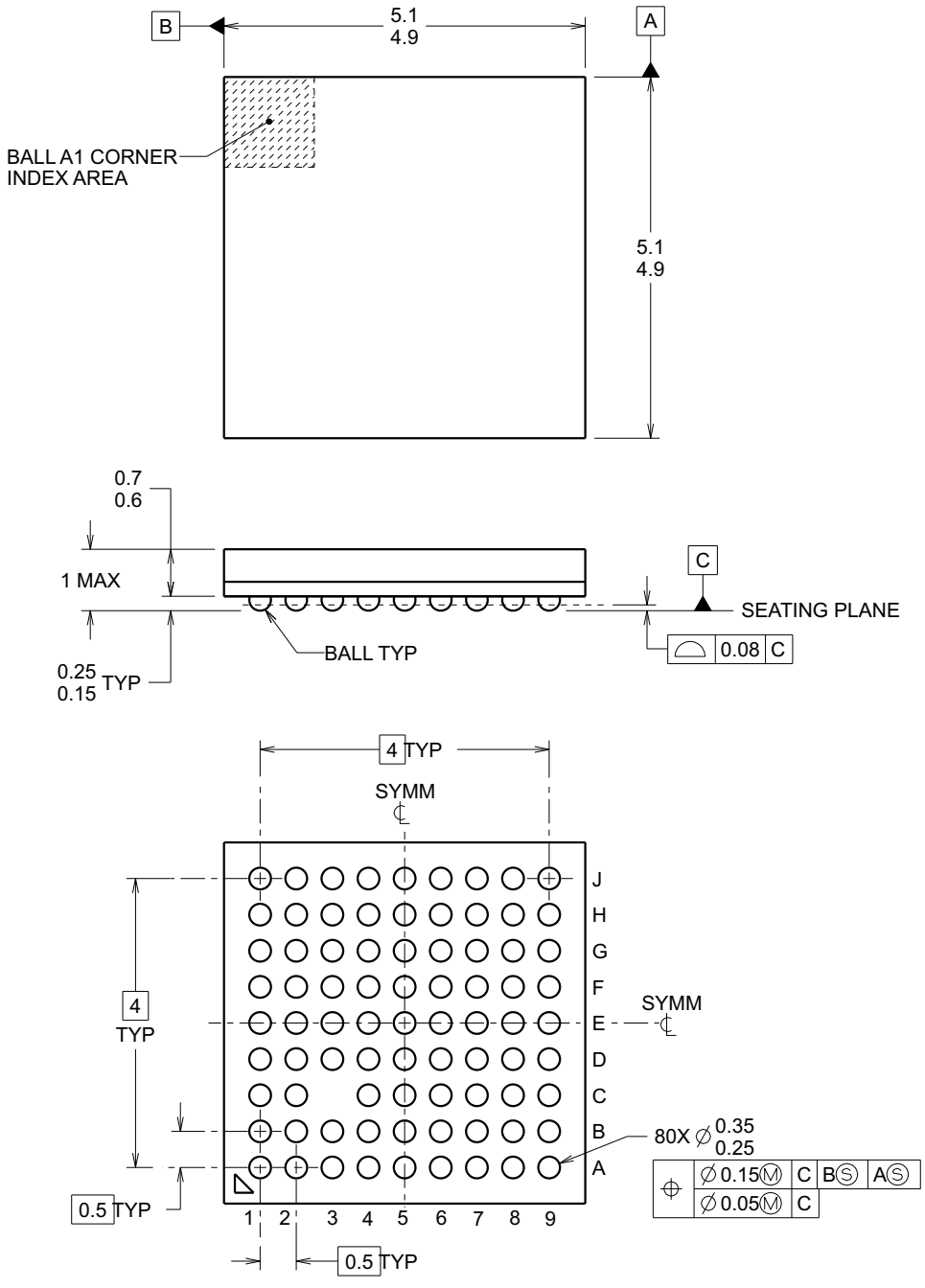
PRODUCT PREVIEW

PRODUCT PREVIEW

PACKAGE OUTLINE

ZXH 80 (NFBGA - 1 mm max height)

BALL GRID ARRAY



NOTES:

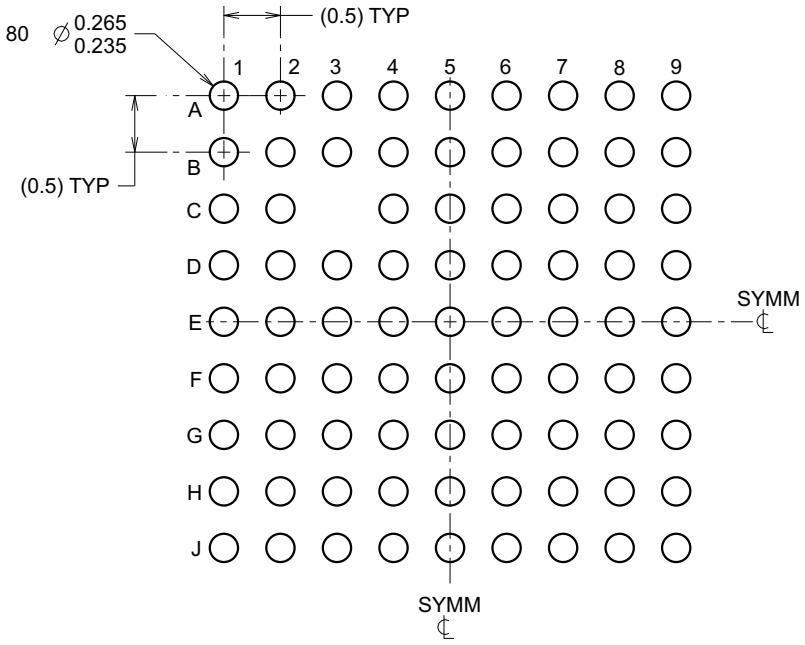
1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.

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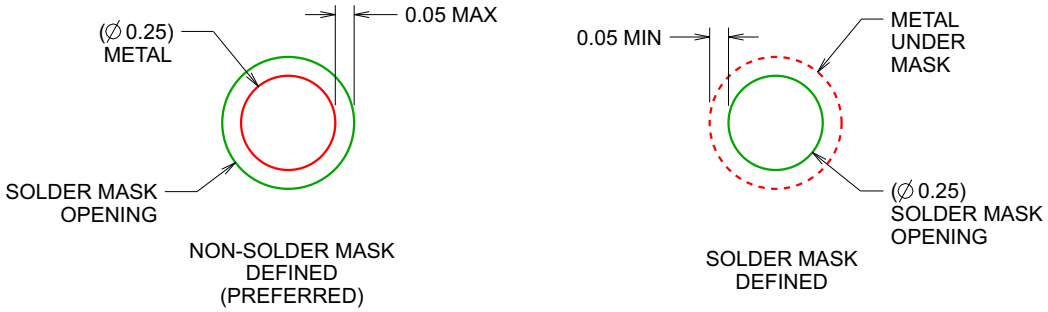
EXAMPLE BOARD LAYOUT

ZXH 80 (NFBGA - 1 mm max height)

BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

4221325/A 01/2014

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).

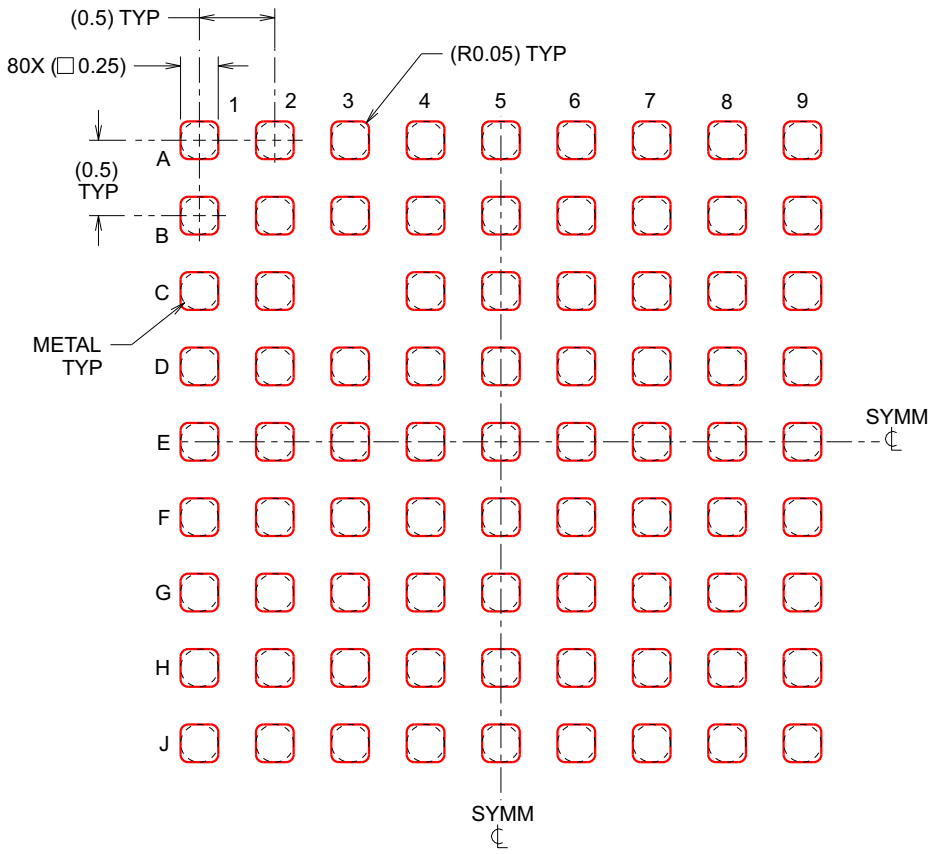
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PRODUCT PREVIEW

EXAMPLE STENCIL DESIGN

ZXH 80 (NFBGA - 1 mm max height)

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

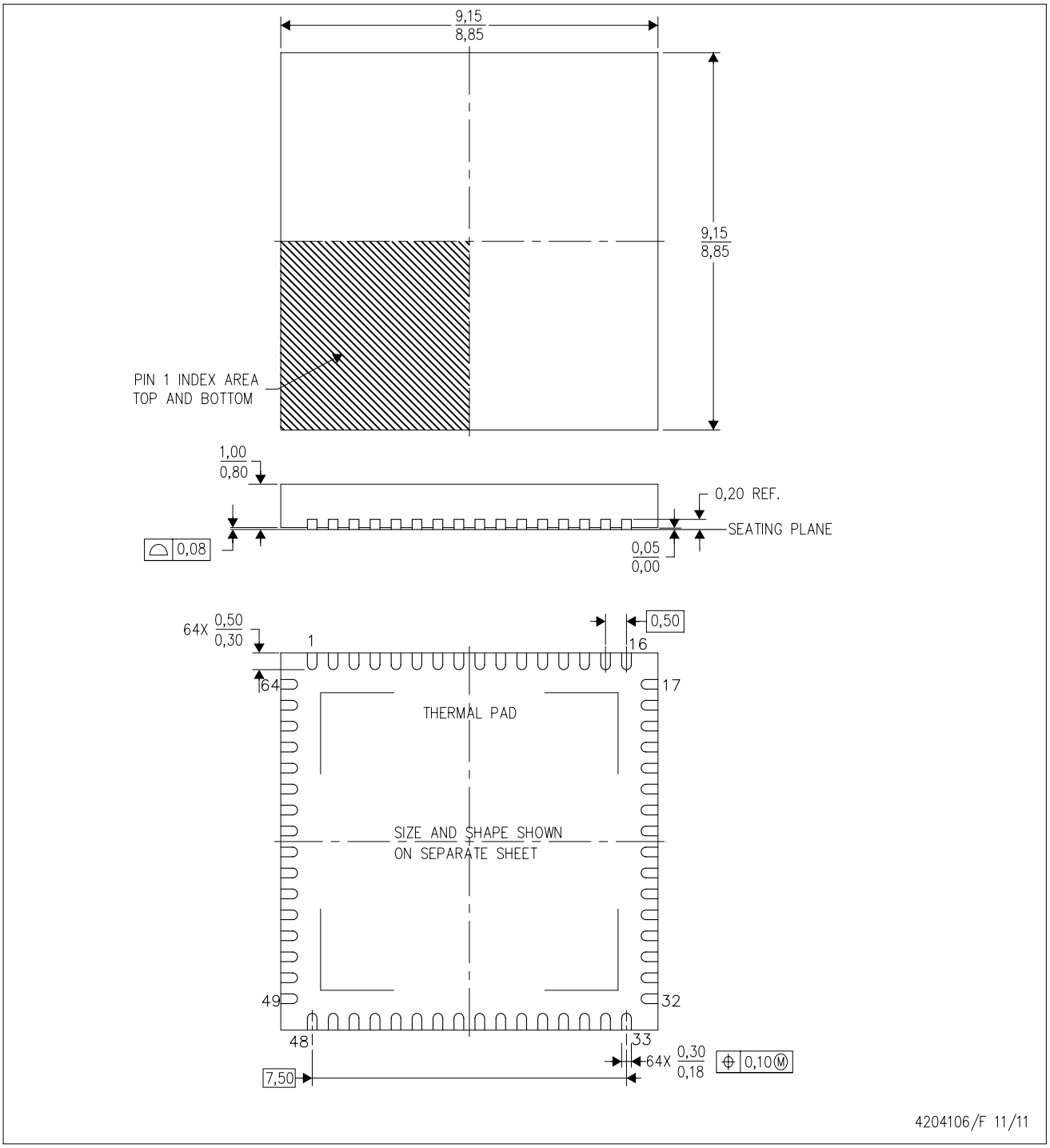
4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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THERMAL PAD MECHANICAL DATA

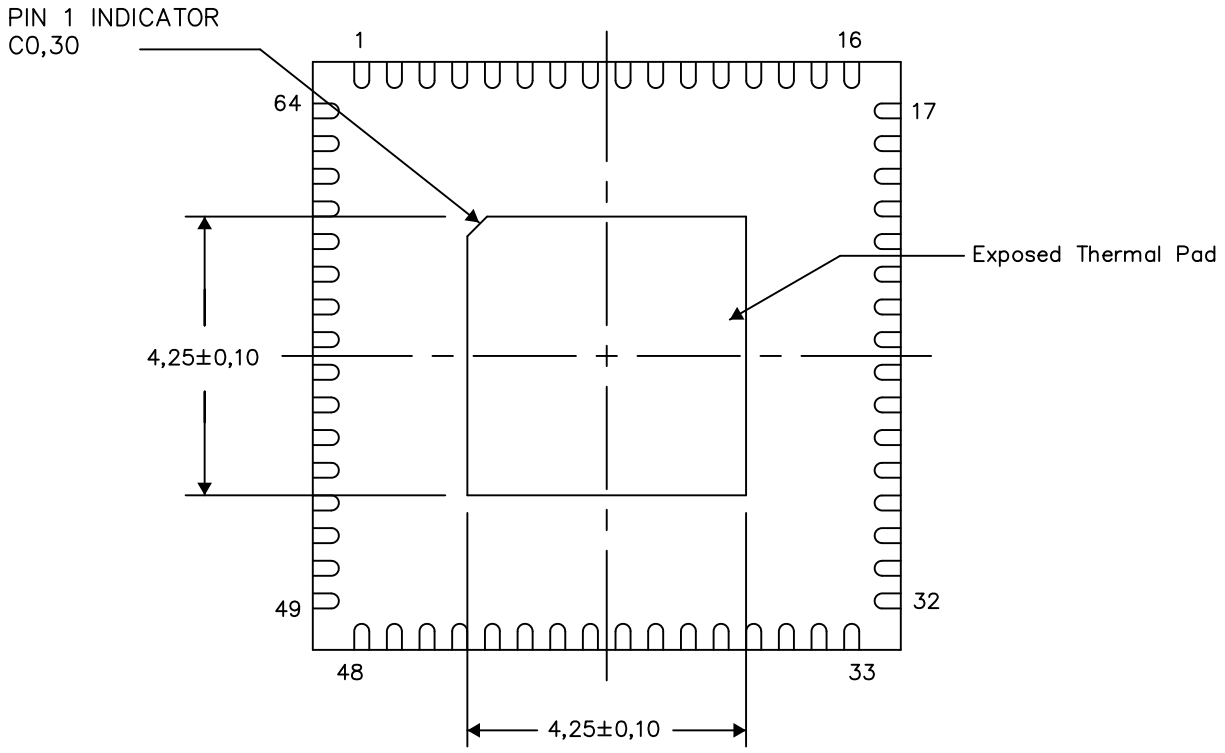
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206192–3/AD 10/14

NOTE: A. All linear dimensions are in millimeters

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XMS432P401MIPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI	-40 to 85		
XMS432P401RIPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

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