SSM-2120/SSM-2122

DYNAMIC RANGE
PROCESSOR / DUAL VCA

Precision Monolithics Inc.

FEATURES

- 0.01% THD at +10dBV In/Out
- 100dB VCA Dynamic Range
- Low VCA Control Feedthrough
- 100dB Level Detection Range
- Log/Antilog Control Paths
- Low External Component Count

APPLICATIONS

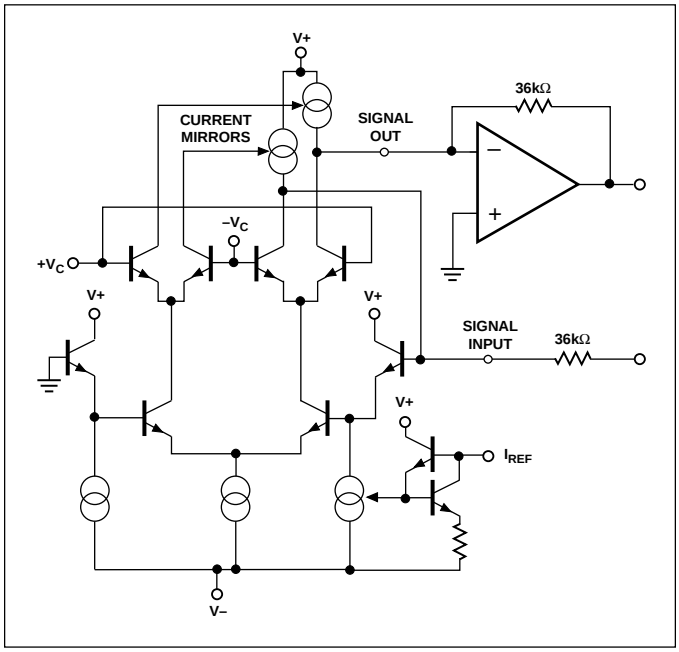
- Compressors
- Expanders
- Limiters
- AGC Circuits
- Voltage-Controlled Filters
- Noise Reduction Systems
- Stereo Noise Gates

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ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	PLASTIC 22-PIN	
SSM2122P	SSM2120P	–10°C to +50°C

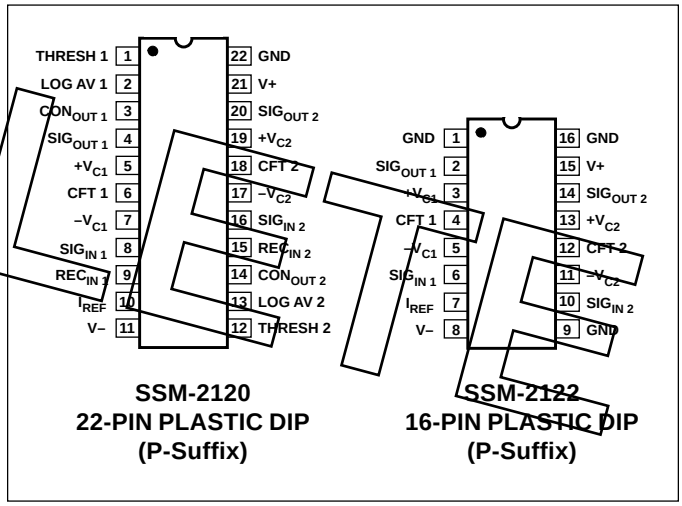
SIMPLIFIED SCHEMATIC (VCA Section Only)



GENERAL DESCRIPTION

The SSM-2120 is a monolithic integrated circuit designed for the purpose of processing dynamic signals in various analog systems including audio. This “dynamic range processor” consists of two VCAs and two level detectors (the SSM-2122 consists of two VCAs only). These circuit blocks allow the user to logarithmically control the gain or attenuation of the signals presented to the level detectors depending on their magnitudes. This allows the compression, expansion or limiting of AC signals, some of the primary applications for the SSM-2120.

PIN CONNECTIONS



SSM-2120
22-PIN PLASTIC DIP
(P-Suffix)

SSM-2122
16-PIN PLASTIC DIP
(P-Suffix)

The SSM-2120/SSM-2122 is mask work protected under the Semiconductor Chip Protection Act of 1983.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Operating Temperature Range ..... –10° to +55°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65° to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
16-Pin Plastic DIP (P)	86	10	°C/W
22-Pin Plastic DIP (P)	70	7	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, I_{REF} = 200µA, A_V = 1, unless otherwise noted.

		SSM-2120/SSM-2122			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY					
Supply Voltage Range		±5	–	±18	V
Positive Supply Current		–	8	10	mA
Negative Supply Current		–	6	8	mA
VCAs					
Max I_{SIGNAL} (In/Out)		±387	±400	±413	µA
Output Offset		–	±1	±2	µA
Control Feedthrough (Trimmed)	$R_{IN} = R_{OUT}$ = 36kΩ, $A_V \leq$ 0dB ≤ –30dB	–	750	–	µV
Gain Control Range	Unity-Gain	–100	–	+40	dB
Control Sensitivity		–	6	–	mV/dB
Gain Scale Factor Drift		–	–3300	–	ppm/°C
Frequency Response	Unity-Gain or Less	–	250	–	kHz
Off Isolation	At 1kHz	–	100	–	dB
Current Gain	$+V_C = -V_C$ = 0V	–0.25	0	+0.25	dB
THD (Unity-Gain)	+10dBV IN/OUT	–	0.005	0.02	%
Noise (20kHz Bandwidth)	RE: 0dBV	–	–80	–	dB
LEVEL DETECTORS (SSM-2120 ONLY)					
Dynamic Range		100	110	–	dB
Input Current Range		0.03	–	3000	μA_{p-p}
Rectifier Input Bias Current		–	4	16	nA
Output Sensitivity (At LOG AV Pin)		–	3	–	mV/dB
Output Offset Voltage		–	±0.5	±2	mV
Frequency Response					
$I_{IN} = 1mA_{p-p}$		–	1000	–	
$I_{IN} = 10\mu A_{p-p}$		–	50	–	kHz
$I_{IN} = 1\mu A_{p-p}$		–	7.5	–	
CONTROL AMPLIFIERS (SSM-2120 ONLY)					
Input Bias Current		–	85	175	nA
Output Drive (Max Sink Current)		5.0	7.5	–	mA
Input Offset Voltage		–	±0.5	±2	mV

NOTE:
1. Specifications are subject to change; consult latest data sheet.

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VOLTAGE-CONTROLLED AMPLIFIERS

The two voltage-controlled amplifiers are full Class A current in/current out devices with complementary dB/V gain control ports. The control sensitivities are +6mV/dB and –6mV/dB. A resistor divider (attenuator) is used to adapt the sensitivity of an external control voltage to the range of the control port. It is best to use 200Ω or less for the attenuator resistor to ground.

VCA INPUTS

The signal inputs behave as virtual grounds. The input current compliance range is determined by the current into the reference current pin.

REFERENCE PIN

The reference current determines the input and output current compliance range of the VCAs. The current into the reference pin is set by connecting a resistor to V+. The voltage at the reference pin is about two volts above V– and the current will be

$$I_{REF} = \frac{[(V+) - ((V-) + 2V)]}{R_{REF}}$$

The current consumption of the VCAs will be directly proportional to I_{REF} which is nominally 200µA. The device will operate at lower current levels which will reduce the effective dynamic range of the VCAs. With a 200µA reference current, the input and output clip points will be ±400µA. In general:

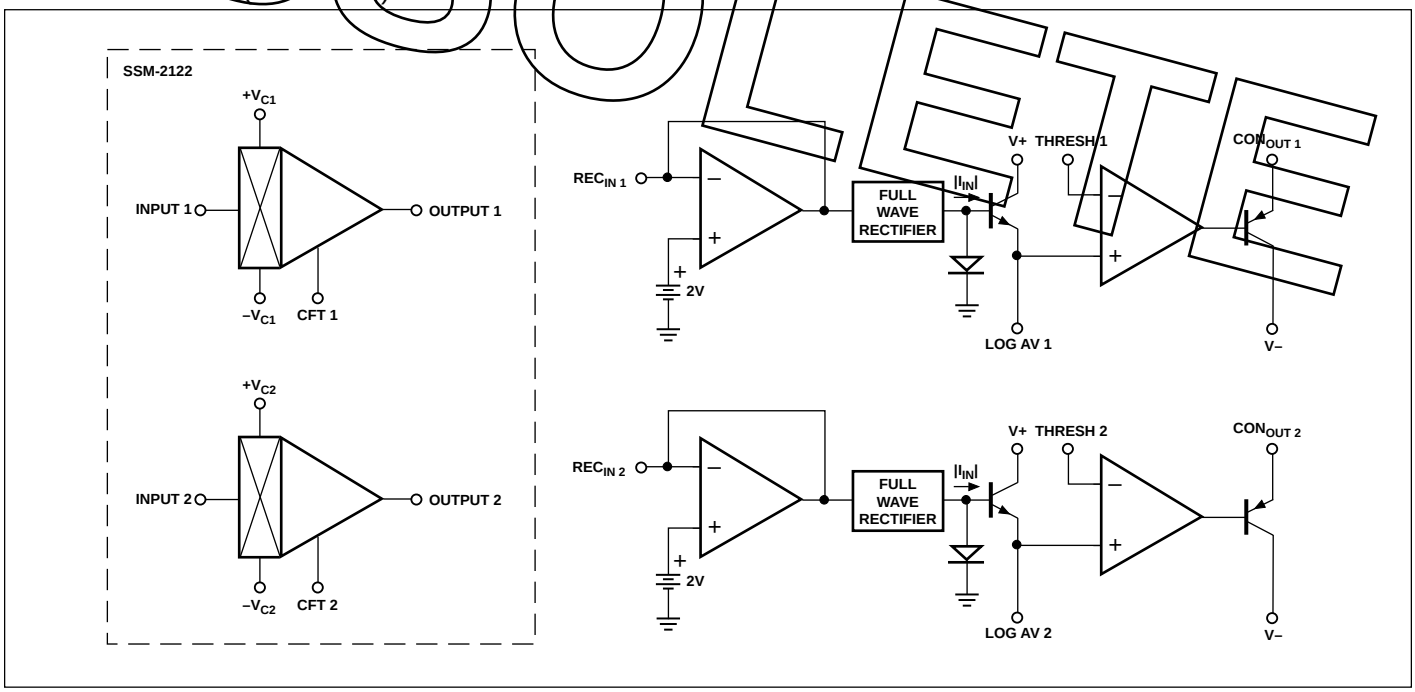
$$I_{CLIP} = \pm 2I_{REF}$$

VCA OUTPUTS

The VCA outputs are designed to interface directly with the virtual ground inputs of external operational amplifiers configured as current-to-voltage converters. The outputs must operate at virtual ground because of the output stage's finite output impedance. The power supplies and selected compliance range determines the values of input and output resistors needed. As an example, with ±15V supplies and ±400µA maximum input and output current, choose $R_{IN} = R_{OUT} = 36k\Omega$ for an output compliance range of ±14.4 V. Note that the signal path through the VCA including the output current-to-voltage converter is noninverting.

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BLOCK DIAGRAM (SSM-2120)



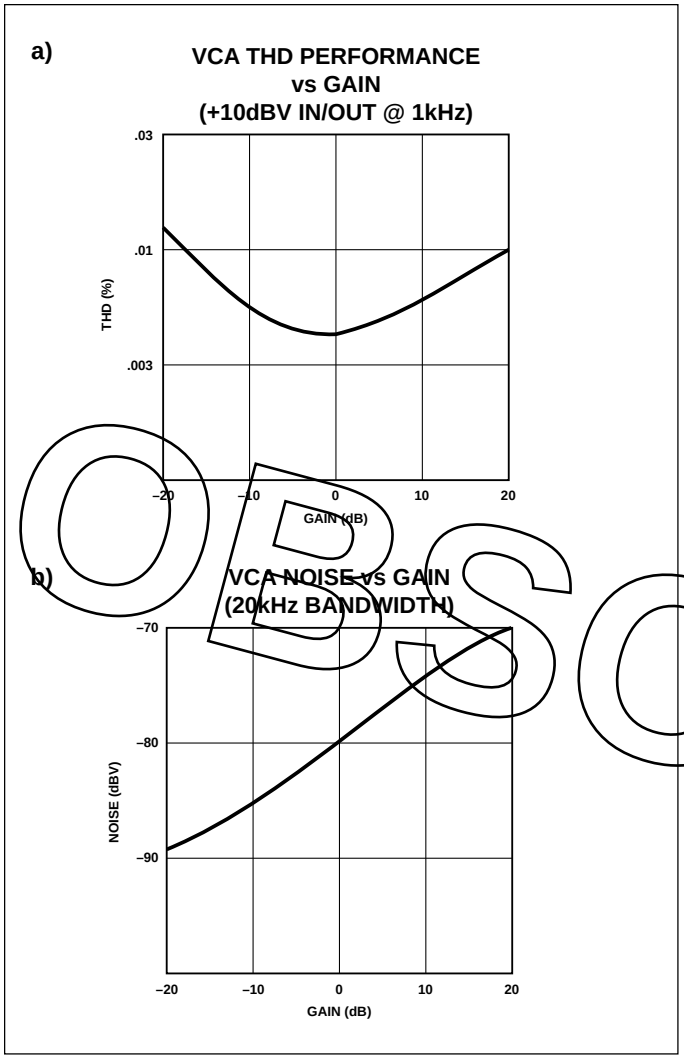


FIGURE 1: *Typical THD and Noise Performance*

VCA PERFORMANCE

Figures 1a and 1b show the typical THD and noise performance of the VCAs over ±20dB gain/attenuation. Full Class A operation provides very low THD.

TRIMMING THE VCAs

The control feedthrough (CFT) pins are optional control feedthrough null points. CFT nulling is usually required in applications such as noise gating and downward expansion. If trimming is not used, leave the CFT pins open.

Trim Procedure

1) Apply a 100Hz sine wave to the control point attenuator. The signal peaks should correspond to the control voltages which induce the VCAs maximum intended gain and at least 30dB of attenuation.

2) Adjust the 50kΩ potentiometer for the minimum feedthrough.

(Trimmed control feedthrough is typically well under $1mV_{RMS}$ when the maximum gain is unity using 36kΩ input and output resistors.)

Applications such as compressor/limiters typically do not require control feedthrough trimming because the VCA operates at unity-gain unless the signal is large enough to initiate gain reduction. In this case the signal masks control feedthrough.

This trim is ineffective for voltage-controlled filter applications.

LEVEL DETECTION CIRCUITS

The SSM-2120 contains two independent level detection circuits. Each circuit contains a wide dynamic range full-wave rectifier, logging circuit and a unipolar drive amplifier. These circuits will accurately detect the input signal level over a 100dB range from 30nA to 3mA peak-to-peak.

LEVEL DETECTOR THEORY OF OPERATION

Referring to the level detector block diagram of Figure 2, the $RE-C_{IN}$ input is an AC virtual ground. The next block implements the full-wave rectification of the input current. This current is then fed into a logging transistor (Q_1) whose pair transistor (Q_2) has a fixed collector current of I_{REF}. The LOG AV output is then:

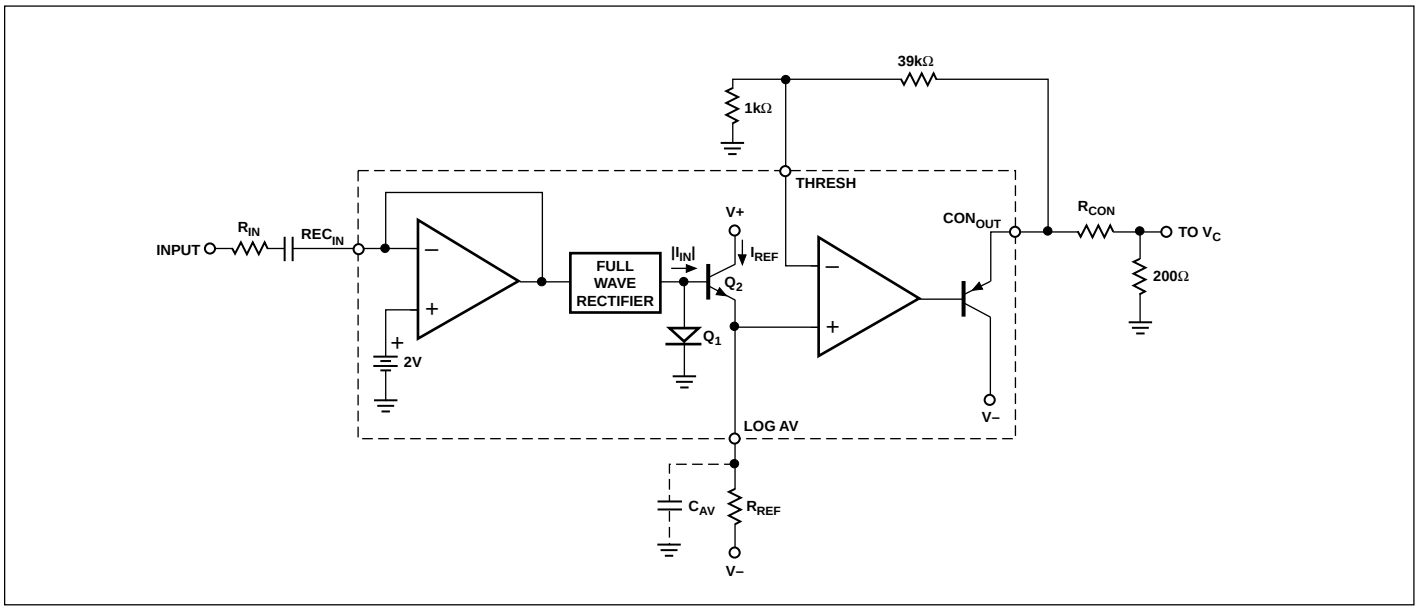


FIGURE 2: *Level Detector*

$$V_{LOG\ AV} = \frac{kT}{q} \ln\left(\frac{|I_{IN}|}{I_{REF}}\right)$$

With the use of the LOG AV capacitor the output is then the log of the average of the absolute value of I_{IN}.

(The unfiltered LOG AV output has broad flat plateaus with sharp negative spikes at the zero crossing. This reduces the "work" that the averaging capacitor must do, particularly at low frequencies.)

Note: It is natural to assume that with the addition of the averaging capacitor, the LOG AV output would become the **average of the log of the absolute value of I_{IN}**. However, since the capacitor forces an AC ground at the emitter of the output transistor, the capacitor charging currents are proportional to the **antilog** of the voltage at the base of the output transistor. Since the base voltage of the output transistor is the log of the absolute value of I_{IN}, the log and antilog terms cancel, so the capacitor becomes a linear integrator with a charging current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging functions. The signal at the output therefore is the **log of the average of the absolute value of I_{IN}**.

USING DETECTOR PINS REC_{IN}, LOG_{AV}, THRESH AND CON_{OUT}

When applying signals to REC_{IN} (rectifier input) an input series resistor should be followed by a low leakage blocking capacitor since REC_{IN} has a DC voltage of approximately 2.1V above ground. Choose R_{IN} for a ±1.5mA peak signal. For ±15V operation this corresponds to a value of 10kΩ.

A 1.5MΩ value of R_{REF} from log average to –15V will establish a 10µA reference current in the logging transistor (Q_1). This will bias the transistor in the middle of the detector's dynamic current range in dB to optimize dynamic range and accuracy. The LOG AV outputs are buffered and amplified by unipolar drive op amps. The 39kΩ, 1kΩ resistor network at the THRESH pin provides a gain of 40.

An attenuator from the CON_{OUT} (control output) to the appropriate VCA control port establishes the control sensitivity. Use 200Ω for the attenuator resistor to ground and choose R_{CON} for the desired sensitivity. Care should be taken to minimize capacitive loads on the control outputs CON_{OUT}. If long lines or capacitive loads are present, it is best to connect the series resistor R_{CON} as closely to the CON_{OUT} pin as possible.

DYNAMIC LEVEL DETECTOR CHARACTERISTICS

Figures 3 and 4 show the dynamic performance of the level detector to a change in signal level. The input to the detector (not shown) is a series of 500ms tone bursts at 1kHz in successive 10dBV steps. The tone bursts start at a level of –60dBV (with R_{IN} =10k) and return to –60dBV after each successive 10dB step. Tone bursts range from –60dBV to +10dBV. Figure 3 shows the logarithmic level detector output. The output of the detector is 3mV/dB at LOG AV and the amplifier gain is 40 which yields 120mV/dB. Thus, the output at CON_{OUT} is seen to increase by 1.2V for each 10dBV increase in input level.

DYNAMIC ATTACK AND DECAY RATES

Figure 4 shows the output levels overlayed using a storage scope. The attack rate is determined by the step size and the value of

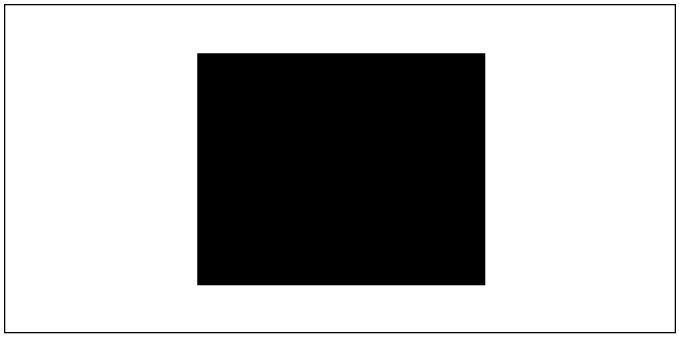


FIGURE 3: *Detector Output*

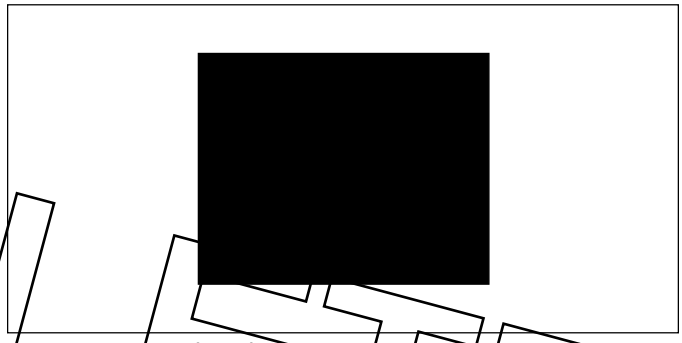


FIGURE 4: *Overlayed Detector Output*

C_{AV}. The attack time to final value is a function of the step size increase. The chart of Figure 5 shows the values of total settling times to within 5, 3, 2 and 1dB of final value with C_{AV} = 10µF. When step sizes exceed 40dB, the increase in settling time for larger steps is negligible. To calculate the attack time to final value for any value of C_{AV}, simply multiply the value in the chart by C_{AV} / 10µF.

The decay rates are linear ramps that are dependent on the current out of the LOG AV pin (set by R_{REF}) and the value of C_{AV}. The integration or decay time of the circuit is derived from the formula:

$$\text{Decrementation Rate (in dB/s)} = \frac{I_{REF} \times 333}{C_{AV}}$$

	5dB	3dB	2dB	1dB
10dB Step	11.28ms	21.46	30.19	46.09
20dB Step	16.65	26.83	35.56	51.46
30dB Step	18.15	28.33	37.06	52.96
40dB Step	18.61	27.79	37.52	53.42
50dB Step			(+144µs)	
60dB Step			(+46µs)	

FIGURE 5: *Settling Time (t_S) for C_{AV} = 10µF, $t_S' = t_S$ (C_{AV}/ 10µF)*

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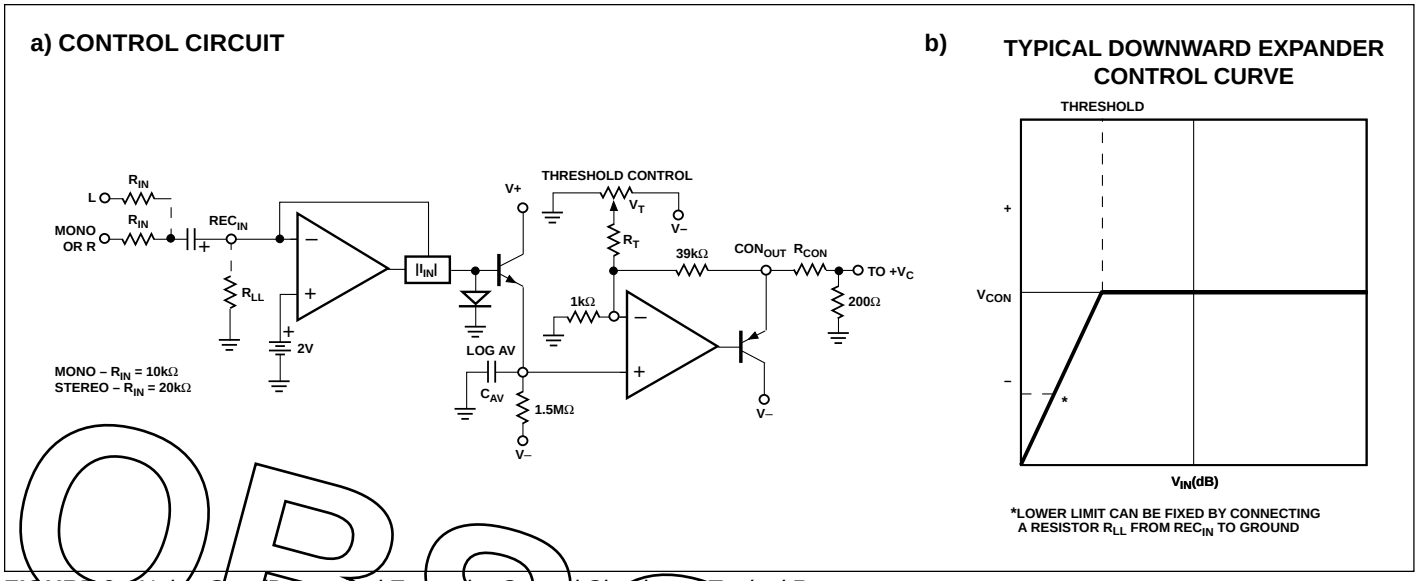


FIGURE 6: *Noise Gate/Downward Expander Control Circuit and Typical Response.*

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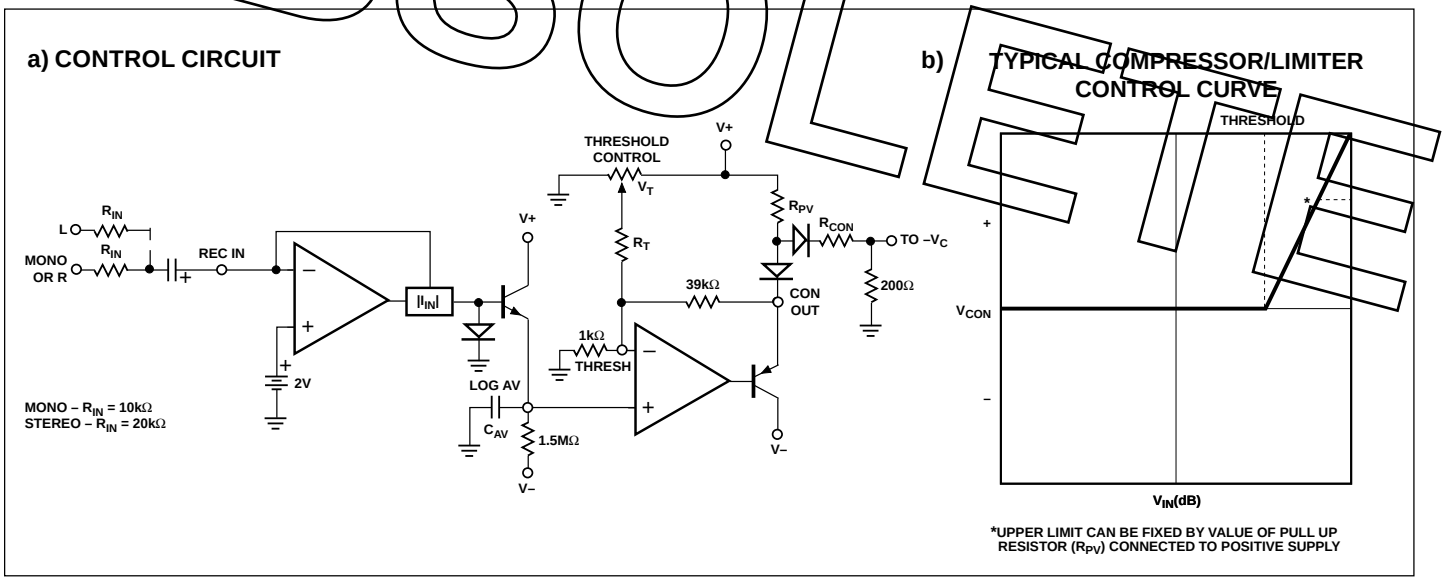


FIGURE 7: *Compressor/Limiter Control Circuit and Typical Response.*

APPLICATIONS

The following applications for the SSM-2120 use both the VCAs and level detectors in conjunction to assimilate a variety of functions.

The first section describes the arrangement of the threshold control in each control circuit configuration. These control circuits form the foundation for the applications to follow which include the downward expander, compressor/limiter and compandor.

THRESHOLD CONTROL

Figure 6a shows the control circuit for a typical downward expander while Figure 6b shows a typical control curve. Here, the threshold potentiometer adjusts V_T to provide a negative unipolar control output. This is typically used in noise gate, downward expander, and dynamic filter applications. This potentiometer is used in all applications to control the signal level versus control voltage characteristics.

In the noise gate, downward expander and compressor/limiter applications, this potentiometer will establish the onset of the control action. The sensitivity of the control action depends on the value of R_T.

For a positive unipolar control output add two diodes as shown in Figure 7a. This is useful in compressor/limiter applications. Figure 7b shows a typical response.

Bipolar control outputs can be realized by adding a resistor from the op amp output to V+. This is useful in compandor circuits as

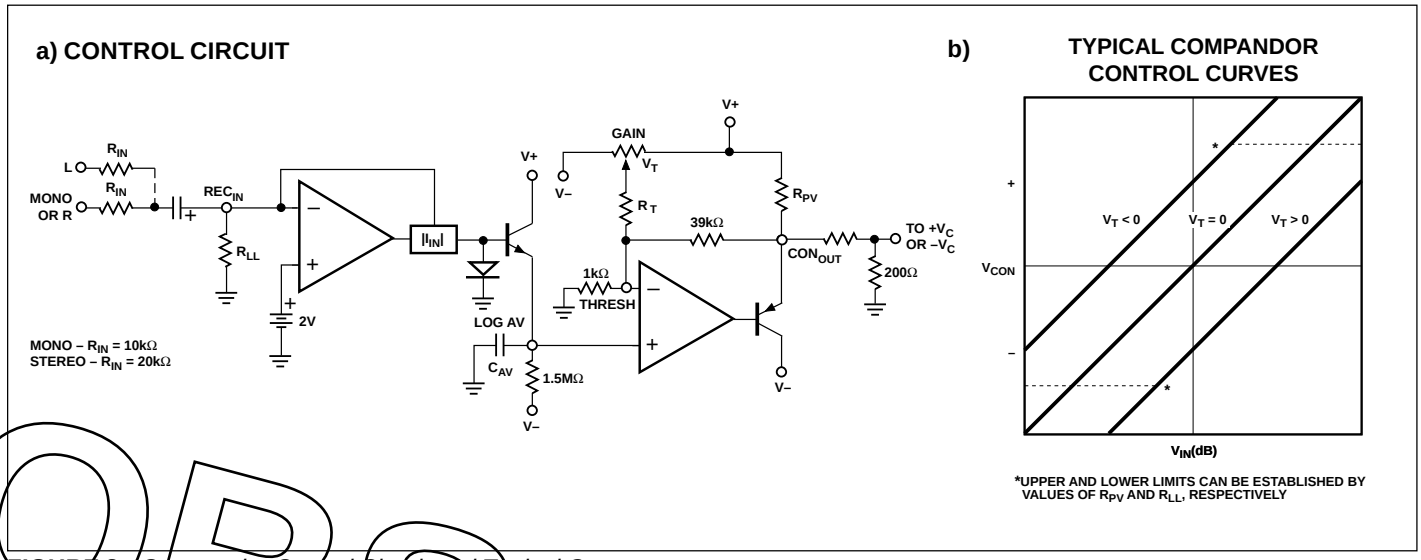


FIGURE 8: *Compandor Control Circuit and Typical Curves.*

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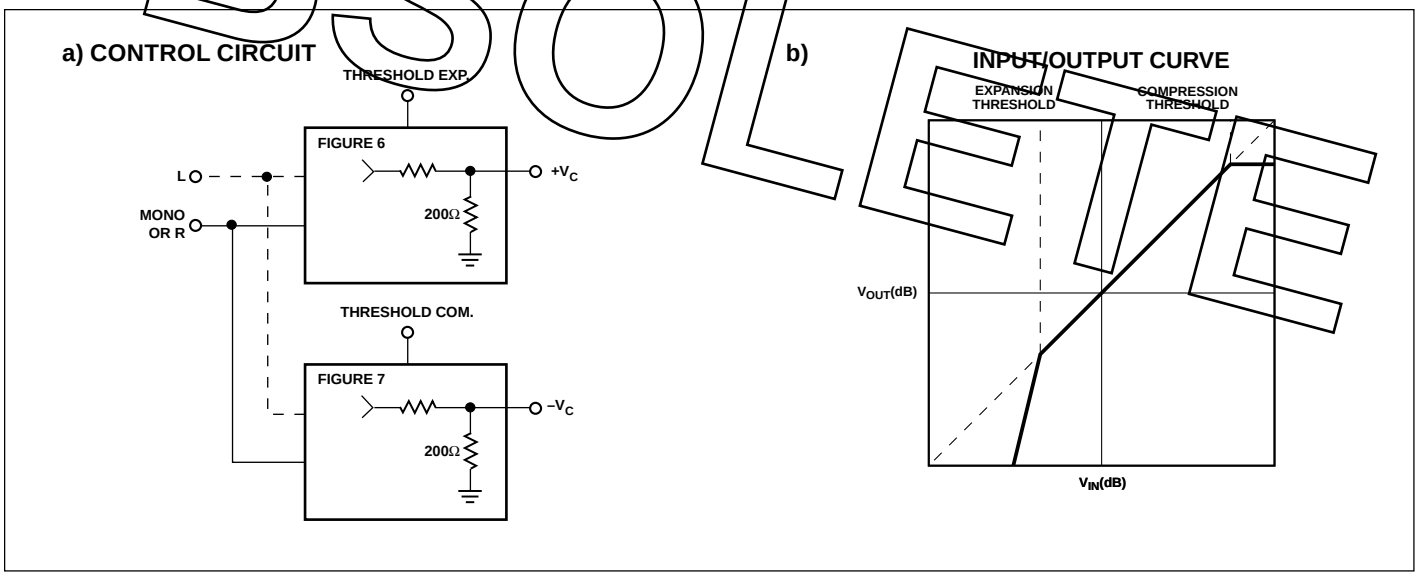


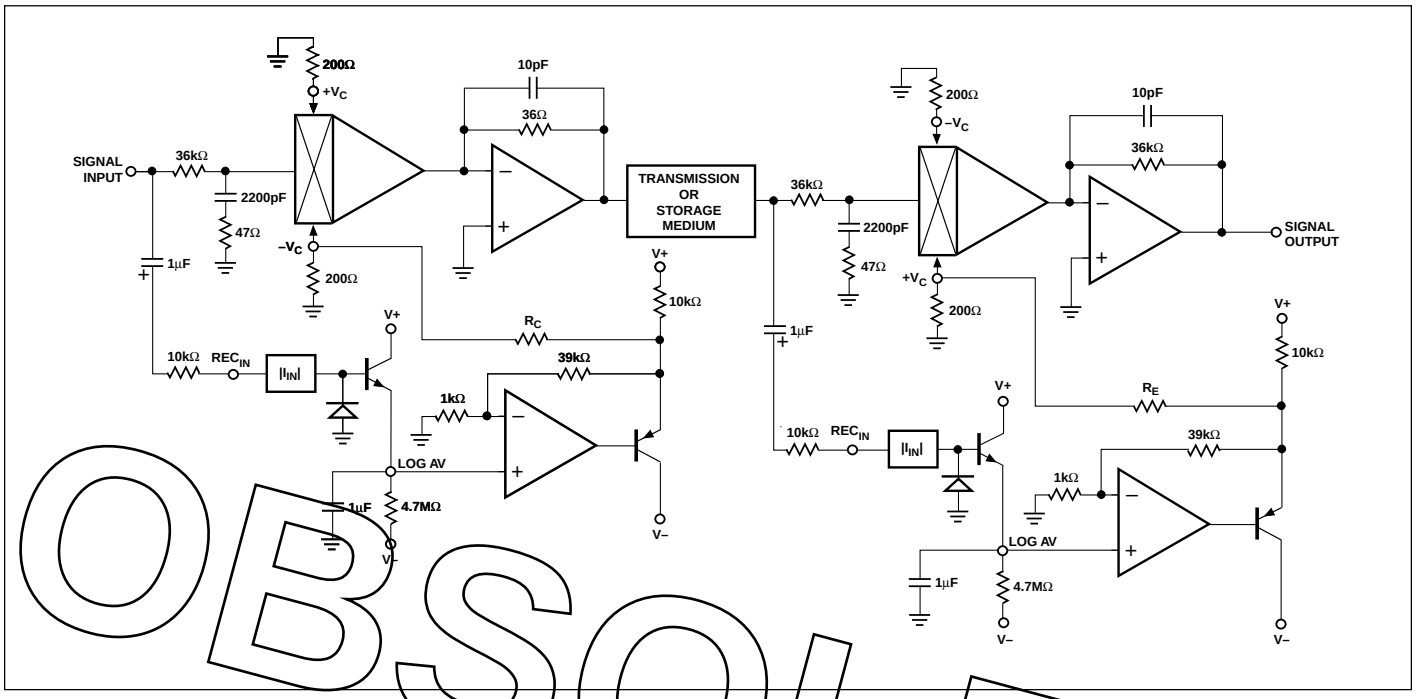
FIGURE 9: *Control Circuit for Stereo Compressor/Limiter with Noise Gating and Input/Output Curve*

shown in Figure 8a, with its response in Figure 8b. The value of the resistor R_{PV} will determine the maximum output from the control amplifier.

STEREO COMPRESSOR/LIMITER

The two control circuits of Figures 6 and 7 can be used in conjunction to produce composite control voltages. Figures 9a and 9b show this type of circuit and transfer function for a stereo compressor/limiter which also acts as a downward expander for noise gating. The output noise in the absence of a signal will be dependent on the noise of the current-to-voltage converter amplifier if the expansion ratio is high enough.

As discussed in the Threshold Control section, the use of the control circuit of Figure 5, including the R_{PV} to V+ and two diodes, yields positive unipolar control outputs.



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FIGURE 10: *Companding Noise Reduction System*

COMPANDING NOISE REDUCTION SYSTEM

A complete companding noise reduction system is shown in Figure 10. Normally, to obtain an overall gain of unity, the value of R_C is equal to R_E. The values of $R_{C/E}$ will determine the compression/expansion ratio.

Table 1 shows compression/expansion ratios ranging from 1.5:1 to full limiting with the corresponding values of $R_{C/E}$.

An example of a 2:1 compression/expansion ratio is plotted in Figure 11. Note that signal compression increases gain for low level signals and reduces gain for high levels while expansion does the reverse. The net result for the system is the same as the original input signal except that it has been compressed before being sent to a given medium and expanded after recovery. The compression/expansion ratio needed depends on the medium being used. As an extreme example, a household tape player would require a higher compression/expansion ratio than a professional stereo system.

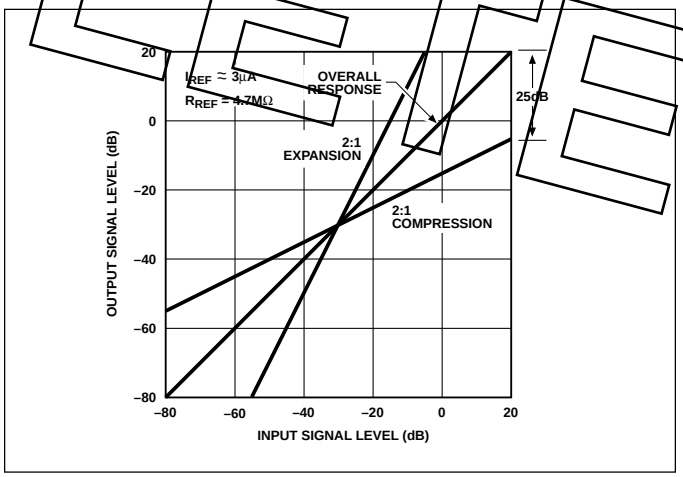
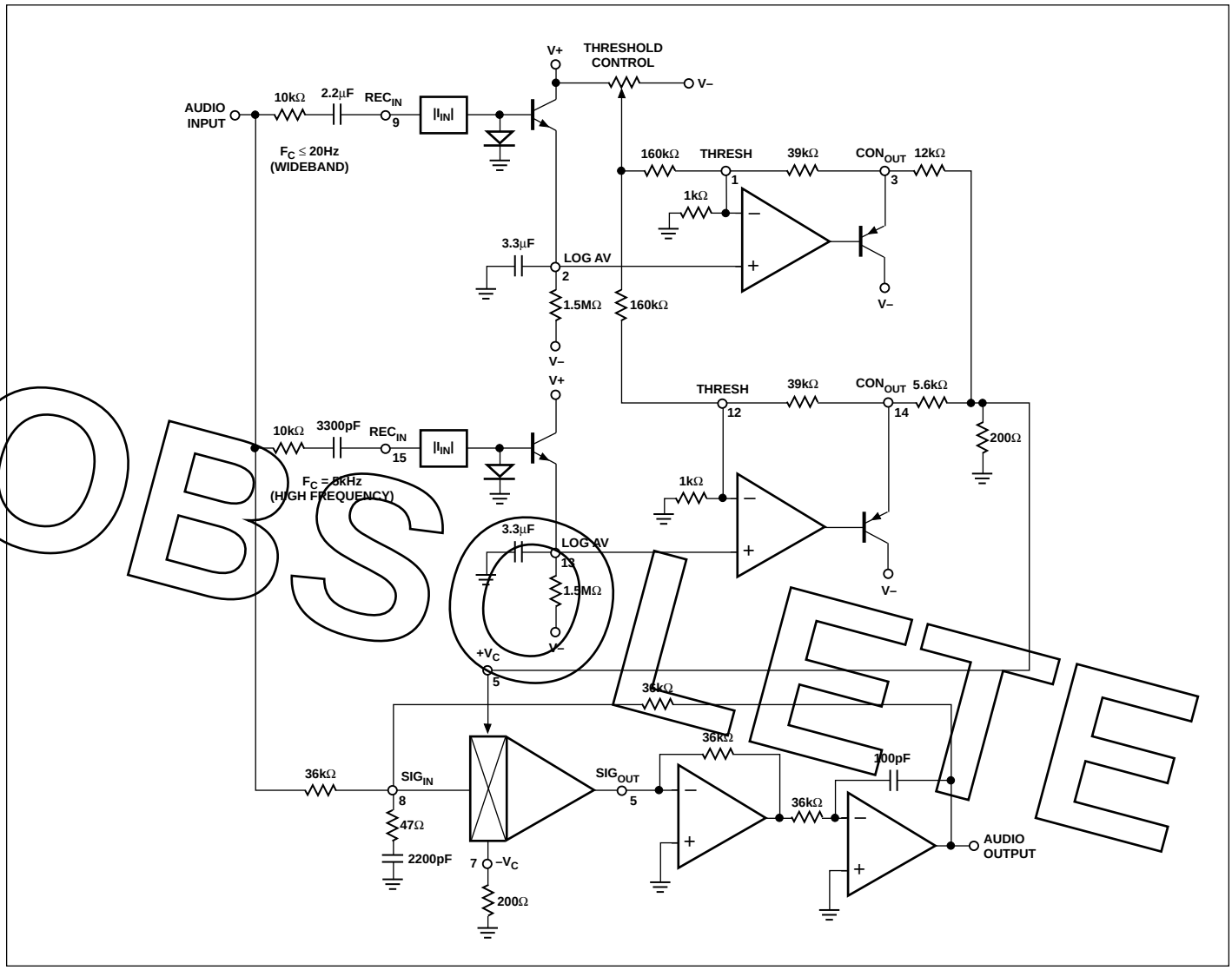


FIGURE 11: *Companding Noise Reduction with 2:1 Compression/Expansion Ratio*

TABLE 1

INPUT SIGNAL INCREASE (dB)	GAIN (REDUCTION OR INCREASE) (dB)	COMPRESSOR ONLY OUTPUT SIGNAL INCREASE (dB)	EXPANDER ONLY OUTPUT SIGNAL INCREASE (dB)	COMPRESSION/ EXPANSION RATIO	$R_{C/E}$ Ω	$\Delta V_{CONTROL}$– (mV/dB)
20	6.67	13.33	22.67	1.5:1	11,800	2.0
20	10.00	10.00	30.00	2:1	7,800	3.0
20	13.33	6.67	33.33	3:1	5,800	4.0
20	15.00	5.00	35.00	4:1	5,133	4.5
20	16.00	4.00	36.00	5:1	4,800	4.8
20	17.33	2.67	37.33	7.5:1	4,415	5.2
20	18.00	2.00	38.00	10:1	4,244	5.4
20	20.00	0	40.00	AGC*/Limiter	3,800	6.0

*AGC for Compression Only



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FIGURE 12: *Dynamic Noise Filter Circuit*

DYNAMIC FILTER

Figure 12 shows a control circuit for a dynamic filter capable of single ended (non-encode/decode) noise reduction. Such circuits usually suffer from a loss of high-frequency content at low signal levels because their control circuits detect the absolute amount of highs present in the signal. This circuit, however, measures wideband level as well as high-frequency band level to produce a composite control signal combined in a 1:2 ratio respectively. The upper detector senses wideband signals with a cutoff of 20Hz while the lower detector has a 5kHz cutoff to sense only high-frequency band signals. This approach allows very good noise masking with a minimum loss of “highs” when the signal level goes below the threshold.

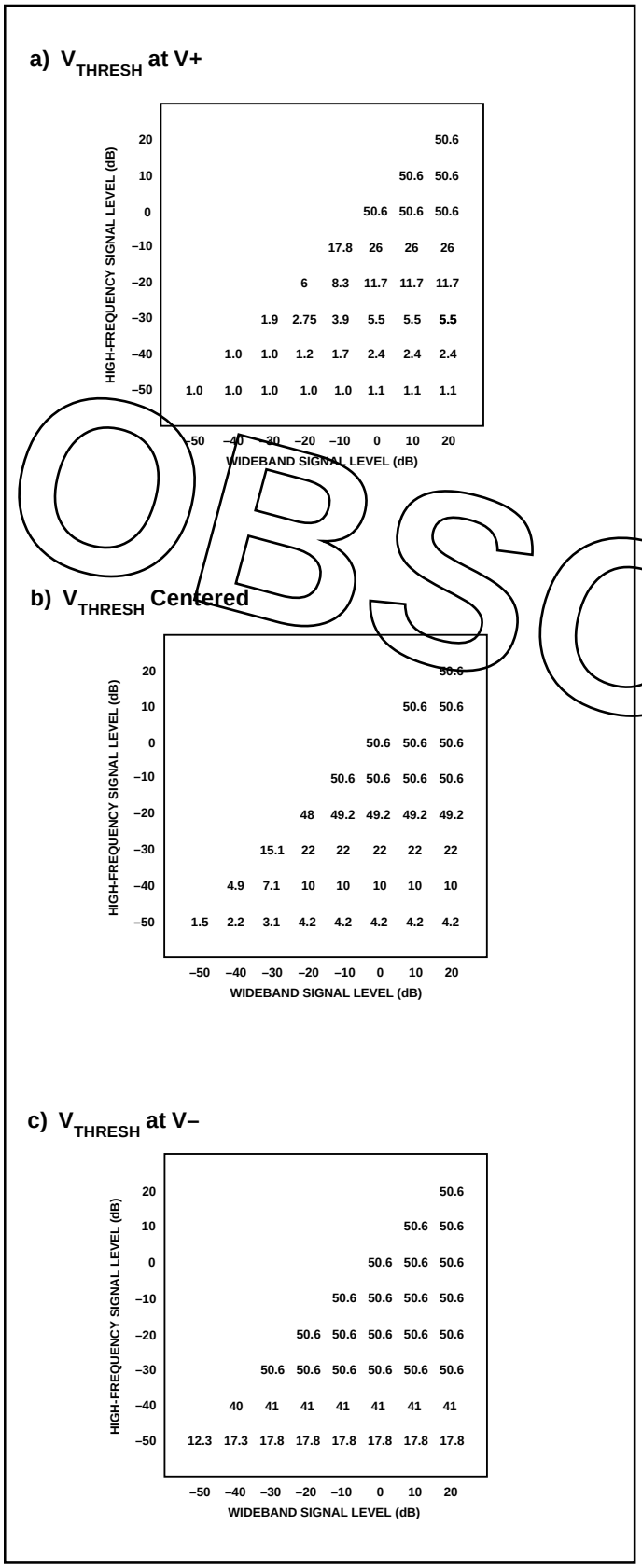


FIGURE 13: *3dB Filter Response*

Figures 13a-c show the filter's 3dB frequency response with the threshold potentiometer at V+, centered, and V–. Data was taken by applying a 300Hz signal to the wideband detector and a 20kHz signal to the high-frequency band detector simultaneously. These figures correspond to filter characteristics for 50dB, 70dB and 90dB dynamic range program source material, respectively. The system could thus treat signals from anything ranging from 1/4" magnetic tape to high-performance compact disc players.

Note that in Figure 13a the control circuit is designed so that the minimum cutoff frequency is about 1kHz. This occurs as the control circuit detects the noise floor of the source material.

Dynamic filtering limits the signal bandwidth to less than 1kHz unless enough highs are detected in the signal to cover the noise floor in the mid- and high-frequency range. In this case the filter opens to pass more of the audio band as more highs are detected. The filter's bandwidth can extend to 50kHz with a nominal signal level at the input. At other signal levels with varying high-frequency content, the filter will close to the required bandwidth. Here, noise outside the band is removed while the perceived noise is masked by other signals within the band. Even in this system, however, a certain amount of mid- and high-frequency components will be lost, especially during transients at very low signal levels. This circuit does not address low frequency noise such as "hum" and "rumble."

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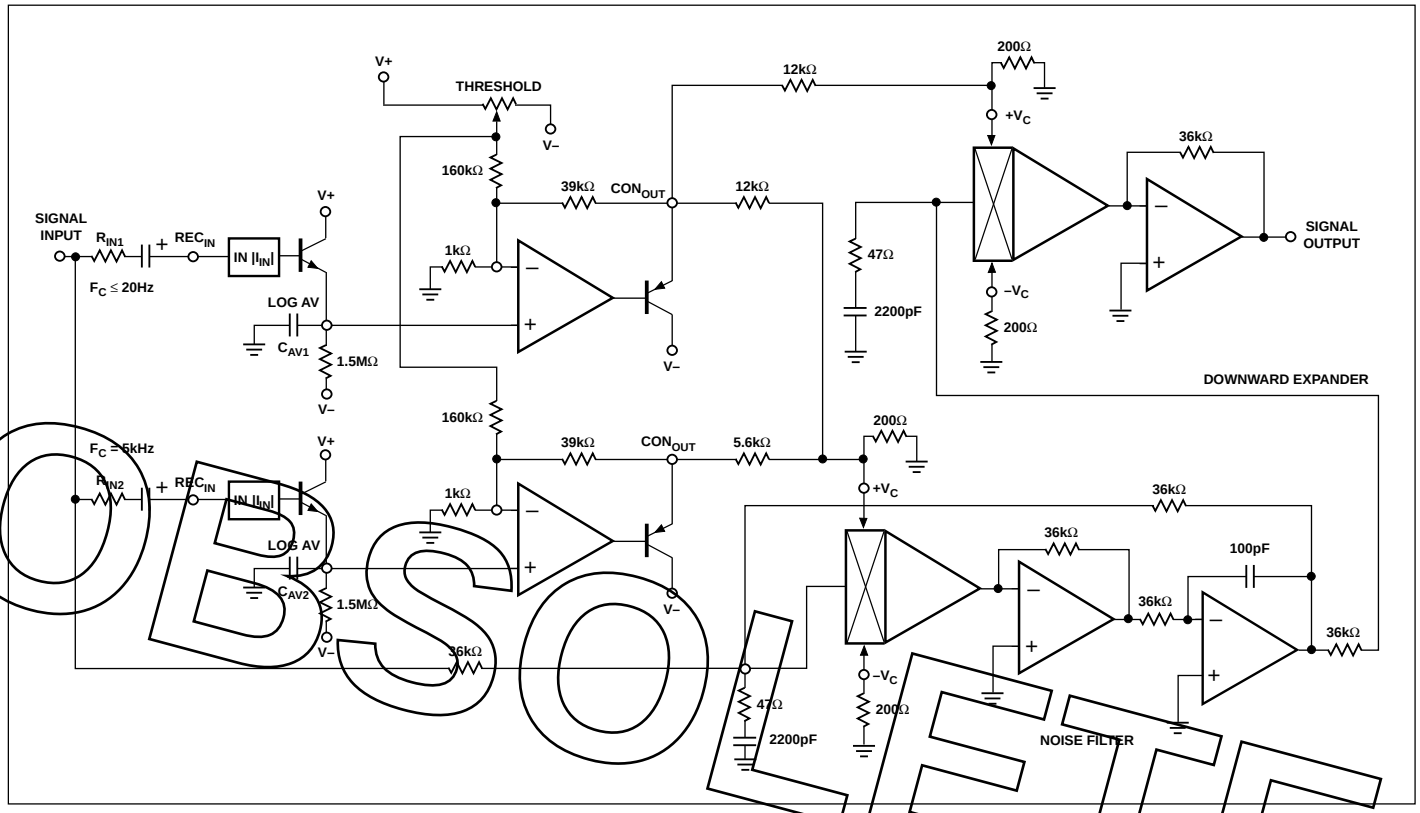


FIGURE 14: *Dynamic Filter with Downward Expander*

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DYNAMIC FILTER WITH DOWNWARD EXPANDER

A composite single-ended noise reduction system can be realized by a combination of dynamic filtering and a downward expander. As shown in Figure 14, the output from the wideband detector can also be connected to the $+V_C$ control port of the second VCA which is connected in series with the sliding filter. This will act as a downward expander with a threshold that tracks that of the filter. Although both of these techniques are used for noise reduction, each alone will pass appreciable amounts of noise under some conditions. When used together, both contribute distinct advantages while compensating for each other's deficiencies.

Downward expansion uses a VCA controlled by the level detector. This section maintains dynamic range integrity for all levels above the user adjustable threshold level. As the input level decreases below the threshold, gain reduction occurs at an increasing rate (see Figure 15). This technique reduces audible noise in fade outs or low level signal passages by keeping the standing noise floor well below the program material.

This technique by itself is less effective for signals with predominantly low frequency content such as a bass solo where wideband frequency noise would be heard at full level. Also, since the level detector has a time constant for signal averaging, percussive material can modulate the noise floor causing a "pumping" or "breathing" effect.

The dynamic filter and downward expander techniques used together can be employed more subtly to achieve a given level of noise reduction than would be required if used individually. Up to 30dB of noise reduction can be realized while preserving the crisp highs with a minimum of transient side effects.

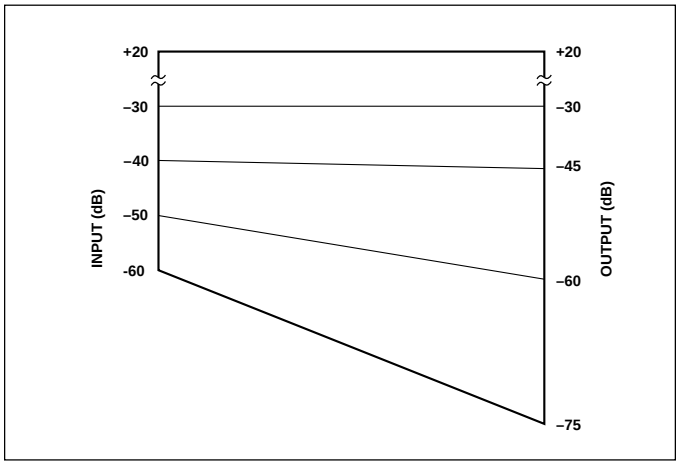


FIGURE 15: *Typical Downward Expander I/O Characteristics at –30dB Threshold Level (1:1.5 Ratio)*

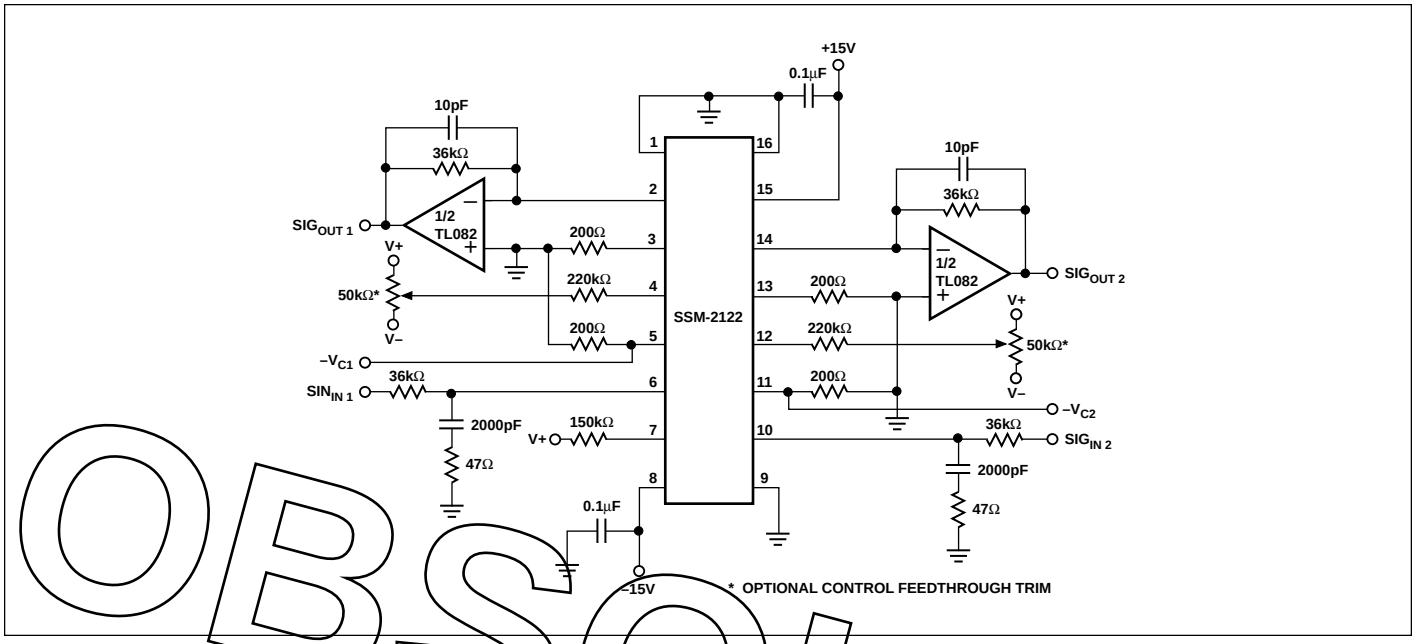


FIGURE 16: *SSM-2122 Basic Connection (Control Ports at 0V)*

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FADER AUTOMATION

The SSM-2120 can be used in fader automation systems to serve two channels. The inverting control port is connected through an attenuator to the VCA control voltage source. The noninverting control port is connected to a control circuit (such as Figure 6) which senses the input signal level to the VCA. Above the threshold voltage, which can be set quite low (for example –60dBV), the VCA operates at its programmed gain. Below this threshold the VCA will downward expand at a rate determined by the $+V_C$ control port attenuator. By keeping the release time constant in the 10 to 25ms range, the modulation of the VCA standing noise floor (–80dB at unity-gain), can be kept inaudibly low.

The SSM-2300 8-channel multiplexed sample-and-hold IC makes an excellent controller for VCAs in automation systems.

Figure 16 shows the basic connection for the SSM-2122 operating as a unity-gain VCA with its noninverting control ports grounded and access to the inverting control ports. This is typical for fader automation applications. Since this device is a pinout option of the SSM-2120, the VCAs will behave exactly as described earlier in the VCA section.

The SSM-2122 can also be used with two or more op amps to implement complex voltage-controlled filter functions. Biquad and state-variable two-pole filters offering lowpass, bandpass and highpass outputs can be realized. Higher order filters can also be formed by connecting two or more such stages in series.

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