DATA SHEET

GPC3LXXXX

Low Power 3-Channel Sound Controller

Jun. 02, 2017

Version 1.2

GENERALPLUS TECHNOLOGY INC. reserves the right to change this documentation without prior notice. Information provided by GENERALPLUS TECHNOLOGY INC. is believed to be accurate and reliable. However, GENERALPLUS TECHNOLOGY INC. makes no warranty for any errors which may appear in this document. Contact GENERALPLUS TECHNOLOGY INC. to obtain the latest version of device specifications before placing your order. No responsibility is assumed by GENERALPLUS TECHNOLOGY INC. for any infringement of patent or other rights of third parties which may result from its use. In addition, GENERALPLUS products are not authorized for use as critical components in life support devices/systems or aviation devices/systems, where a malfunction or failure of the product may reasonably be expected to result in significant injury to the user, without the express written approval of Generalplus.

Table of Contents

PAGE

TABLE OF CONTENTS 2
LOW POWER 3-CHANNEL SOUND CONTROLLER 4
1. GENERAL DESCRIPTION 4
2. BLOCK DIAGRAM 4
3. FEATURES 4
4. APPLICATION FIELD 4
5. GPC3LXXXX FAMILY AND FEATURE LIST 5
6. SIGNAL DESCRIPTIONS 6
6.1. SIGNAL DESCRIPTIONS FOR GPC3L170A~GPC3L096A 6
6.2. LQFP128 PIN MAP FOR GPC3L170A~GPC3L096A 7
7. FUNCTIONAL DESCRIPTIONS 8
7.1. CPU 8
7.2. RAM AREA 8
7.3. ROM AREA 8
7.4. MAP OF MEMORY AND I/OS 8
7.5. I/O PORT 8
7.6. DC-DC 8
7.7. POWER SAVING MODE 8
7.8. RTC (REAL TIME CLOCK) 9
7.9. WATCHDOG 9
7.10. LOW VOLTAGE RESET 9
7.11. INTERRUPT 9
7.12. TIMER/COUNTER 9
7.13. SPEECH AND MELODY 9
7.14. BATTERY VOLTAGE DETECT FUNCTION 9
8. ELECTRICAL SPECIFICATIONS 10
8.1. ABSOLUTE MAXIMUM RATINGS 10
8.2. POWER CHARACTERISTICS (ONE-BATTERY , TA = 25℃) 10
8.3. POWER CHARACTERISTICS (TWO-BATTERY , TA = 25℃) 10
8.4. DC CHARACTERS (TA = 25℃) 11
8.5. PUMP EFFICIENCY (ONE-BATTERY , T_A = 25℃) 11
8.6. PUMP EFFICIENCY (TWO-BATTERY , T_A = 25℃) 12
8.7. VDD15 V.S. MAX. SUPPLIED CURRENT (I(VDD)) (ONE-BATTERY , TA = 25℃) 12
8.8. VDD15 V.S. MAX. SUPPLIED CURRENT (I(VDD)) (TWO-BATTERY , TA = 25℃) 12
8.9. (3VOLT) EXTERNAL OSCILLATOR R RELATIVE F_{OSC} (THE TABLE IS FOR REFERENCE ONLY). 12
8.10. THE RELATIONSHIP BETWEEN THE FOSC AND VDD 13
9. APPLICATION CIRCUITS 14
9.1. LIGHT LOADING AND CIRCUIT WITHOUT NOISE FOR GPC3L170A~GPC3L096A 14
9.2. HEAVY LOADING OR CIRCUIT WITH NOISE FOR GPC3L170A~GPC3L096A 15
10. PACKAGE/PAD LOCATIONS 16
10.1. ORDERING INFORMATION 16
10.2. PACKAGE LQFP128 INFORMATION 16

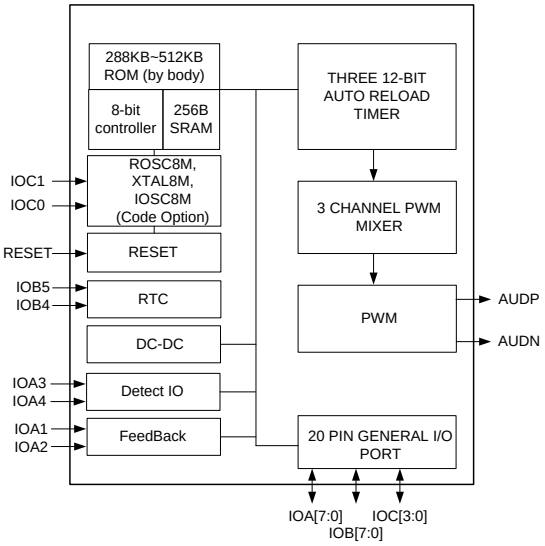
11. DISCLAIMER 17
12. REVISION HISTORY 18

LOW POWER 3-CHANNEL SOUND CONTROLLER

1. GENERAL DESCRIPTION

GPC3LXXXX is embedded with an 8-bit processor, 288K~512K bytes ROM and 256-byte working SRAM, three 12-bit timer/counters, 20 general I/Os, a 3-channel mixer, a pair of 12-bit PWM outputs and a Real Time Clock(RTC). GPC3LXXXX is designed for wide input voltage (1.0V~1.8V; 1.3V~3.6V), and the circuit works at a programmable pumped voltage (2.7V~4.5V). In audio processing, both melody and speech is capable of being mixed together into one output. Furthermore, it contains a Low Voltage Reset to assure system operating appropriately under low voltage condition and a sleep mode to save power while system is standing by. With a high cost/performance ratio characteristic, GPC3LXXXX is one of the most suitable engines in the industry for vocal applications.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 288K ~ 512K bytes ROM (by body).
- 256-byte working SRAM
- Wide input voltage (Code Option) : 1.0V~1.8V (one-battery)
  1.3V~3.6V (two-battery)
  *Lower input voltage can drive lighter loading only.
- Pumped voltage (DC-DC) for core power:2.7V~4.5V;Step:0.3V
  *The output pumped voltage is greater than or equal to input voltage
- Operating clock : 8.0MHz
- Three system clock sources: IOSC(8MHz), ROSC and XTAL (Code option)
- Standby mode (Clock Stop mode) for power savings.
  Max. 5.0μA @1.5V (one-battery)
  Max. 10.0μA @ 3.0V (two-battery)
- 20 general I/Os
- Low Voltage Reset (LVR) function
- Three 12-bit timer/counters
- 9 IRQs & 1 NMI interrupts
- Three wake-up sources
- Watchdog function
- RTC function
- IR function
- Four sets of 256-level PWMIO outputs
- Feedback function
- Detect IO function
- A 3-channel mixer with melody or ADPCM/PCM input
- A pair of PWM outputs with volume control
- BVD (battery voltage detection) function.

4. APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- High-end toy controller
- Intelligent education toys
- And more

5. GPC3LXXXX FAMILY AND FEATURE LIST

Body	GPC3L170A	GPC3L128A	GPC3L112A	GPC3L096A
Voice Duration	170 Sec.	128 Sec.	112 Sec.	96 Sec.
Working Voltage (Code Option)	1.0V~1.8V (one-battery) 1.3V~3.6V (two-battery)	1.0V~1.8V (one-battery) 1.3V~3.6V (two-battery)	1.0V~1.8V (one-battery) 1.3V~3.6V (two-battery)	1.0V~1.8V (one-battery) 1.3V~3.6V (two-battery)
RAM Size	256B	256B	256B	256B
ROM Size	512KB	384KB	352KB	288KB
Clock Source (Code Option)	IROSC(8MHz) ROSC XTAL	IROSC(8MHz) ROSC XTAL	IROSC(8MHz) ROSC XTAL	IROSC(8MHz) ROSC XTAL
IO Pin	20 (IOA/B/C)	20 (IOA/B/C)	20 (IOA/B/C)	20 (IOA/B/C)
Hardware PWMIO	V	V	V	V
IR	V	V	V	V
RTC	V	V	V	V
PWM Volume control	V	V	V	V
Feedback function	V	V	V	V
IRQ Interrupt	9	9	9	9
NMI interrupt	1	1	1	1
Wakeup source	3	3	3	3

6. SIGNAL DESCRIPTIONS

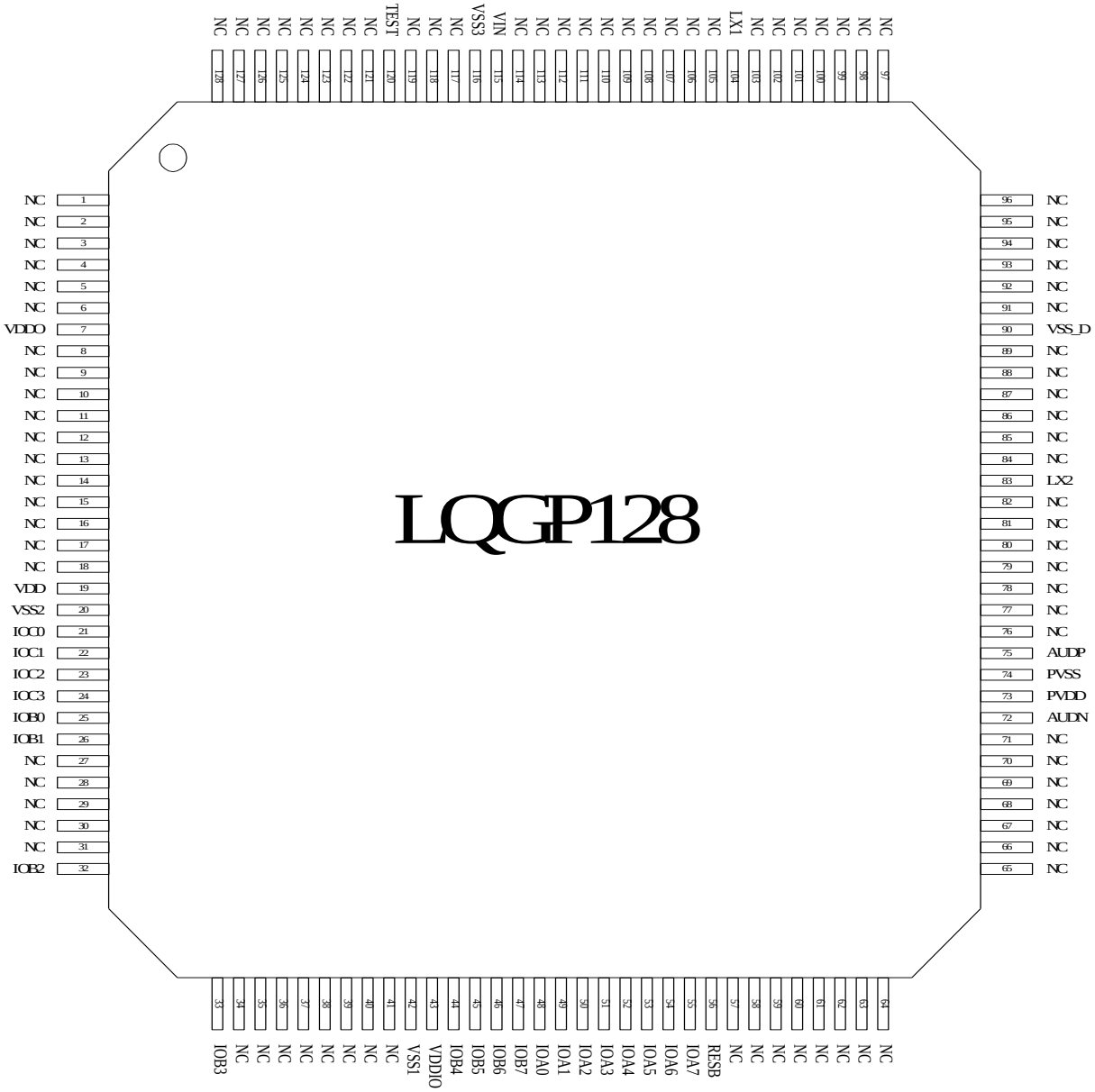
6.1. Signal Descriptions for GPC3L170A~GPC3L096A

PIN Name	Type	Description
IOA[7:0]	I/O	IOA[7:0] is a bi-directional I/O port, which can be software programmed as a wakeup I/O with 1Mohm or 100Kohm pull low resistor. IOA7 shares its pad with IR output. IOA[4:3]shares its pad with detecting IO function. IOA[2:1] shares its pad with feedback function. IOA1 shares its pad with external clock input. IOA0 shares its pad with external interrupt input.
IOB[7:0]	I/O	IOB[7:0] is a bi-directional I/O port, which can be software programmed as a wakeup I/O with 1Mohm or 100Kohm pull low resistor. IOB5 shares its pad with XTAL 32KHz inputs IOB4 shares its pad with XTAL 32KHz outputs IOB[3:0] shares its pad with 256-level PWM outputs
IOC[3:0]	I/O	IOC[3:0] is a bi-directional I/O port, which can be software programmed as wakeup I/O with 1Mohm or 100Kohm pull low resistor. IOC1 shares its pad with XTAL8M output. IOC0 shares its pad with ROSC8M or XTAL8M input.
VDD15	P	Power PAD for DC-DC .
VSS15	G	Ground PAD for DC-DC.
LX1	I	This pin must short with LX2 externally. Inductance input of DC-DC(Inductance must be connected to VDD15)
LX2	I	This pin must short with LX1 externally. Inductance input of DC-DC(Inductance must be connected to VDD15)
VDDO	O	DC-DC Pumped voltage output
VDD	P	Power supply voltage input for logic circuit
VSS2	G	Ground reference for logic circuit
VSS3	G	Ground reference for logic circuit
VDDIO	P	Power supply voltage input for IO PAD
VSS1	G	Ground reference for IO PAD
PVDD	P	PWM driver power
PVSS	G	PWM driver ground reference
RESB	I	System reset input, low active (with pull high)
TEST	I	Test pin, high active (with pull low)
AUDP, AUDN	O	PWM output

Total: 36 pins

Legend: I=Input, O=Output, P=Power, G=Ground

6.2. LQFP128 pin map for GPC3L170A~GPC3L096A



7. FUNCTIONAL DESCRIPTIONS

7.1. CPU

The microprocessor inside the GPC3LXXXX is an 8-bit high performance processor equipped with Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as CPU6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of generating clearer speech, pleasant music as well as achieving the best performance.

7.2. RAM Area

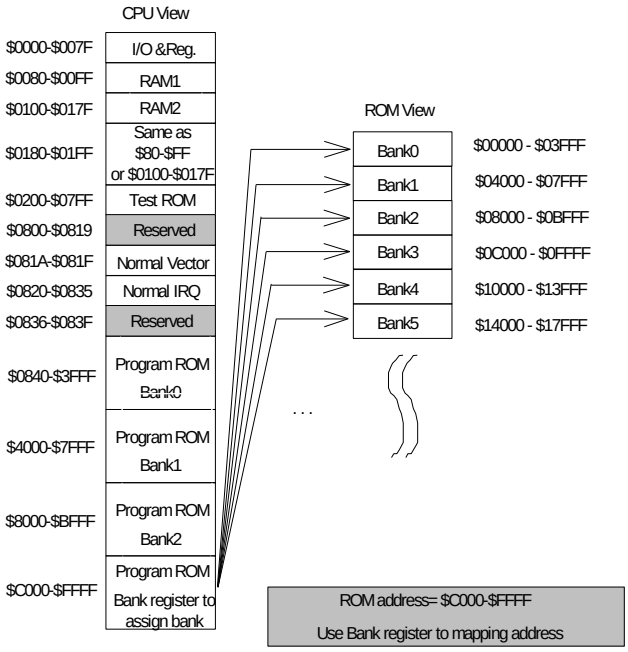
The RAM size in GPC3LXXXX is **256-byte** (including Stack), in which address starts from $0080 through $017F ($0100 - $017F mapping to $0180 - $01FF).

7.3. ROM Area

GPC3LXXXX builds a 288K~512K bytes of ROM, which can be defined as the program area, audio data area, or both. To access ROM, users shall program the BANK SELECT register, choose bank, and access address to fetch data.

Body	ROM size	ROM Address
GPC3L170A	512KB	0x00840~0x07FFFF
GPC3L128A	384KB	0x00840~0x05FFFF
GPC3L112A	352KB	0x00840~0x057FFF
GPC3L096A	288KB	0x00840~0x047FFF

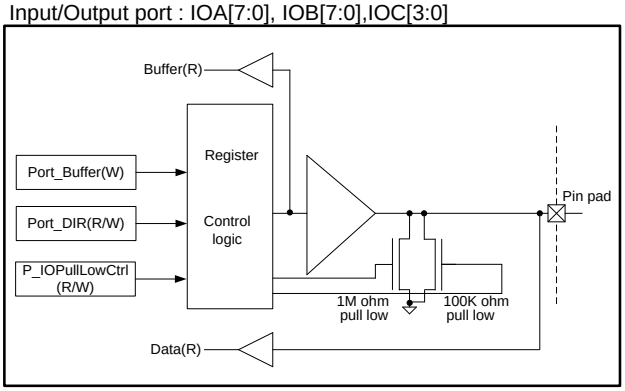
7.4. Map of Memory and I/Os



7.5. I/O Port

There are 20 IOs (IOA[7:0], IOB[7:0] and IOC[3:0] in GPC3LXXXX, which are bit-control IOs. They can be programmed as input (pure input or pull-low) or output buffer. As pull-low input, they keep a less impedance to get better noise immunity. While pressing the key (IOs to VDD), a less or large impedance can be selected at different conditions. IOA7 can be programmed as an IR transmitter. IOA[4:3] can be programmed as Detect IO. IOA[2:1] can also be programmed as feedback function with IOA2 connecting to the input of inverter and IOA1 connecting to the output of inverter. With feedback function, RC or XTAL oscillation can be implemented. For more flexible application, IO wakeup and ECK as TMA clock source are also available when feedback function enable. Please refer to programming guide for more detailed information about feedback function. IOA1 can be programmed as an external clock source. IOA0 is programmable as an external interrupt source. IOB5 and IOB4 can be programmed as a 32KHz crystal clock generator by adding external components. IO port configuration:

Input/Output port : IOA[7:0], IOB[7:0],IOC[3:0]



7.6. DC-DC

GPC3LXXXX can work with wide input voltage (1.0V~1.8V; 1.3V~3.6V). Inside the chip, it is implemented with a high efficient DC-DC circuit. The DC-DC circuits pump input voltage to programmed voltage that supplies chip as working voltage.

7.7. Power Saving Mode

GPC3LXXXX features a power saving mode (standby mode) for those applications requiring low standby current. To enter standby mode, the Wake-up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their prior states until being awakened. All 20 IOs, RTC (8Hz/2Hz), and external interrupt (IOA0) are wake-up sources in GPC3LXXXX. After GPC3LXXXX wakes up, the internal CPU will proceed to execute the program.

7.8. RTC (Real Time Clock)

GPC3LXXXX provides two RTC (real time clock) sources: 2Hz, 8Hz. The RTC sources can be used for time counting or system awaking function. Each RTC occurs, system wakes up and users can use this signal for time counting. In addition, GPC3LXXXX supports 32768Hz OSC in auto mode; the first one second, it runs at strong mode (consumes the highest power) and then switches to weak mode automatically to save power.

7.9. Watchdog

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog must be cleared. It prevents system from incorrect code execution by generating a system reset when software fails to clear watchdog flag within 1 second. Watchdog function can be removed by option in GPC3LXXXX series.

7.10. Low Voltage Reset

GPC3LXXXX has a Low Voltage Reset (LVR) function. In general, CPU becomes unstable and abnormal under low voltage condition. With the unique design of Low Voltage Reset in GPC3LXXXX, it is able to reset all functions to the initial operational (stable) state if the power voltage drops below certain operation voltage.

7.11. Interrupt

GPC3LXXXX has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller provides 9 IRQs and 1 NMI. A NMI cannot be interrupted by any other IRQs.

Interrupt Source	Priority
TIMER A	NMI
TIMER A	IRQ1
TIMER B	IRQ2
TIMER C	IRQ3
TB1	IRQ4
TB2	IRQ5
RTC	IRQ6
KEY	IRQ7
EXT	IRQ8
DETIO	IRQ9

7.12. Timer/Counter

GPC3LXXXX has three 12-bit timer/counters: TMA, TMB, and TMC respectively. In timer mode, TMA, TMB, and TMC are re-loadable up-counters. When timer overflows from $0FFF to $0000, the carry (overflow) signal will make the user's pre-set value to be loaded into timer automatically and count up again. At the same time, the carry signal will generate an INT signal if the corresponding bit in the INT ENABLE Register is enabled. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter is activated, the counter value can also be read at the same time. The read instruction will not affect the counter value nor reset it.

7.13. Speech and Melody

In speech synthesis, the GPC3LXXXX can use NMI for accurate sampling frequency. User can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, ADPCM, SACMA3400 and A3400Pro.

7.14. Battery voltage detect function

GPC3LXXXX has Battery Voltage Detection (BVD) function. There are four detecting levels can be chosen for 1-battery and 2-battery application respectively. Please refer to programming guide for more detailed information about BVD function.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	(VSS-0.3V) to (V_+ + 0.3V)
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-65℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device.

8.2. Power Characteristics (One-Battery , TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VDD15	1.0	-	-	V	I(VDD)=40mA@VDD=3.3V, L=22uH/0.5W , ESR =1 ohm (Color Code Inductance)
Input Voltage (Max.)	VDD15	-	-	1.8	V	-
Operating Voltage**	VDD	V_{LVR} ***	-	3.9	V	-
Low Voltage Reset Level	V_{LVR}	2.3	2.4	2.5	V	-
Operating Current	I_{OP}	-	10	-	mA	F_{OSC}=8.0MHz @ VDD=3.3V(no load) VDD15=1.5V
Halt Current	I_{HALT}	-	5	-	μA	VDD15=1.5V
Standby Current	I_{STBY}	-	-	5.0	μA	VDD15=1.5V

*As I(VDD) is larger than the value of test condition; VDD can be observed voltage drop.

**VDD is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating condition.

*** V_{LVR} is 2.4V +/- 5%.

8.3. Power Characteristics (Two-Battery , TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VDD15	1.3	-	-	V	I(VDD)=40mA@VDD=3.3V, L=22uH/0.5W , ESR =1 ohm (Color Code Inductance)
Input Voltage (Max.)	VDD15	-	-	3.6	V	-
Operating Voltage**	VDD	V_{LVR} ***	-	4.5	V	-
Low Voltage Reset Level	V_{LVR}	2.3	2.4	2.5	V	-
Operating Current	I_{OP}	-	5	-	mA	F_{OSC}=8.0MHz @ VDD=3.3V(no load) VDD15=3.0V
		-	10	-	mA	F_{OSC}=8.0MHz @ VDD=4.5V(no load) VDD15=3.0V
Halt Current	I_{HALT}	-	15	-	μA	VDD15=3.0V
Standby Current	I_{STBY}	-	-	10.0	μA	VDD15=3.0V

*As I(VDD) is larger than the value of test condition; VDD can be observed voltage drop.

**VDD is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating condition.

*** V_{LVR} is 2.4V +/- 5%.

8.4. DC Characters (TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
GPIO Input High Level (IOA, IOB, IOC)	V_{IH}	0.7VDD	-	-	V	VDD = 3.3V
		0.7VDD	-	-	V	VDD = 4.5V
GPIO Input Low Level (IOA, IOB, IOC)	V_{IL}	-	-	0.3VDD	V	VDD = 3.3V
		-	-	0.3VDD	V	VDD = 4.5V
Output High Current (IOA, IOB, IOC)	I_{OH}	-	5	-	mA	VDD = 3.3V, V_{OH} = 0.7*VDD
		-	10	-	mA	VDD = 4.5V, V_{OH} = 0.7*VDD
Output Low Current (IOA, IOB, IOC)	I_{OL}	-	10	-	mA	VDD = 3.3V, V_{OL} = 0.3*VDD
		-	20	-	mA	VDD =4.5V, V_{OL} = 0.3*VDD
Input 1M Ohm Pull Low Resistor (IOA, IOB, IOC)	R_{PLM}**	-	1000	-	Kohm	VDD = 1.5V, IO = 1.5V
		-	200	-	Kohm	VDD = 3.3V, IO = 3.3V
		-	120	-	Kohm	VDD = 4.5V, IO = 4.5V
Input 100K Ohm Pull Low Resistor(IOA, IOB, IOC)	R_{PL100K}***	-	100	-	Kohm	VDD = 3.3V, IO = 0V or VDD
		-	100	-	Kohm	VDD = 4.5V, IO = 0V or VDD
PWM Driver Current	I_{PWM}	-	200	-	mA	VDD = 3.3V, 8 Ohms load (bypass DC-DC)
		-	300	-	mA	VDD = 4.5V, 8 Ohms load (bypass DC-DC)
Frequency deviation by voltage drop	⊿F/F	-2	-	2	%	$\frac{Fosc(4.5v) - Fosc(3.0v)}{Fosc(4.5v)}$ F_{CPU} = 8MHz, For IOSC
		-2	-	2	%	$\frac{Fosc(4.5v) - Fosc(3.0v)}{Fosc(4.5v)}$ F_{CPU} = 8MHz, For ROSC
Frequency lot deviation	⊿F/F	-3	-	3	%	$\frac{Fmax(3.6v) - Fmin(3.6v)}{Fmax(3.6v)}$ F_{CPU} = 8MHz @ 3.6V,For IOSC
		-7	-	7	%	$\frac{Fmax(3.6v) - Fmin(3.6v)}{Fmax(3.6v)}$ F_{CPU} = 8MHz @ 3.6V,For ROSC

***** VDD is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating condition.

**R_{PLM} increases enormously while VDD drops.

***RPL100K keeps remain while VDD drops.

8.5. Pump Efficiency (One-Battery , T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (Color Code Inductance L=22uH/0.5W , ESR =1 ohm)	Eff.	-	86	-	%	I(VDD)=30mA;VDD15=1.5V; VDD=3.3V
		-	78	-	%	I(VDD)=60mA;VDD15=1.5V; VDD=3.3V
		-	86	-	%	I(VDD)=30mA;VDD15=1.5V; VDD=3.9V
		-	76	-	%	I(VDD)=60mA;VDD15=1.5V; VDD=3.9V

8.6. Pump Efficiency (Two-Battery , T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (Color Code Inductance L=22uH/0.5W , ESR =1 ohm)	Eff.	-	91	-	%	I(VDD)=50mA;VDD15=3.0V; VDD=3.9V
		-	88	-	%	I(VDD)=100mA;VDD15=3.0V; VDD=3.9V
		-	92	-	%	I(VDD)=50mA;VDD15=3.0V; VDD=4.5V
		-	87	-	%	I(VDD)=100mA;VDD15=3.0V; VDD=4.5V

8.7. VDD15 v.s. Max. Supplied Current (I(VDD)) (One-Battery , TA = 25℃)

VIN (V)	I(VDD) (mA)	Condition
1.0	50	VDD=3.3V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductor)
	30	VDD=3.9V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductor)
1.2	70	VDD=3.3V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductor)
	50	VDD=3.9V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductor)
1.5	110	VDD=3.3V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductor)
	90	VDD=3.9V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductor)

***** VDD drops about 0.3V in max supplied current condition.

8.8. VDD15 v.s. Max. Supplied Current (I(VDD)) (Two-Battery , TA = 25℃)

VIN (V)	I(VDD) (mA)	Condition
1.5	40	VDD=3.9V ; L=22uH/0.5W, ESR = 1 ohm (Color Code Inductance)
	10	VDD=4.5V ; L=22uH/0.5W, ESR = 1 ohm (Color Code Inductance)
1.8	90	VDD=3.9V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductance)
	70	VDD=4.5V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductance)
2.4	140	VDD=3.9V ; L=22uH/0.5W , ESR = 1 ohm (Color Code Inductance)
	140	VDD=4.5V ; L=22uH/0.5W, ESR = 1 ohm (Color Code Inductance)
3.0	250	VDD=3.9V ; L=22uH/0.5W, ESR = 1 ohm (Color Code Inductance)
	190	VDD=4.5V ; L=22uH/0.5W, ESR = 1 ohm (Color Code Inductance)

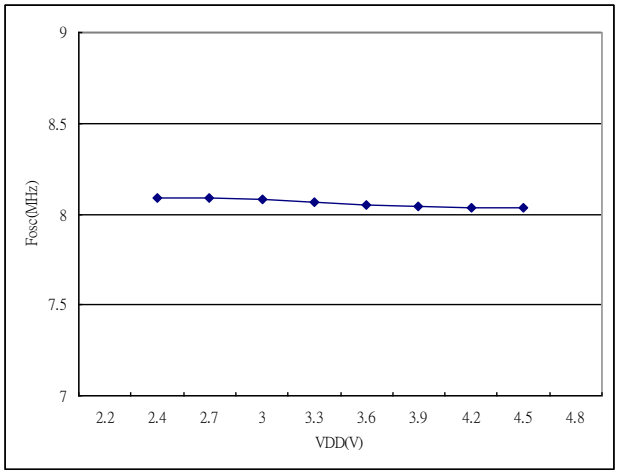
***** VDD drops about 0.3V in max supplied current condition.

8.9. (3volt) External Oscillator R Relative F_{osc} (the table is for reference only).

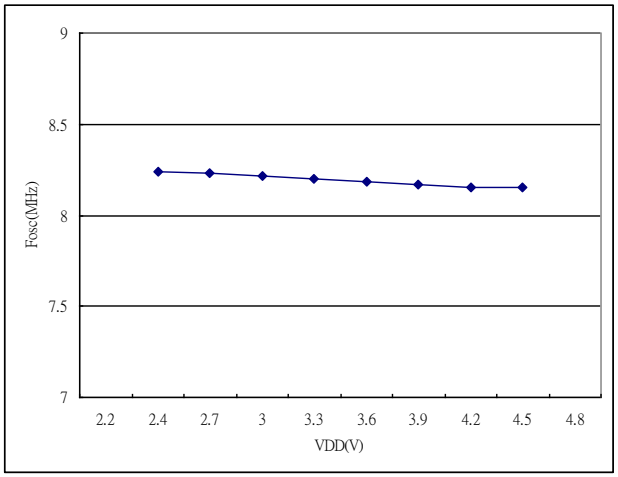
R(Kohm)	39	51	75
F_{osc} (MHz)	8	6	4

8.10. The Relationship between the FOSC and VDD

8.10.1. Frequency vs. VDD (external R_{OSC})

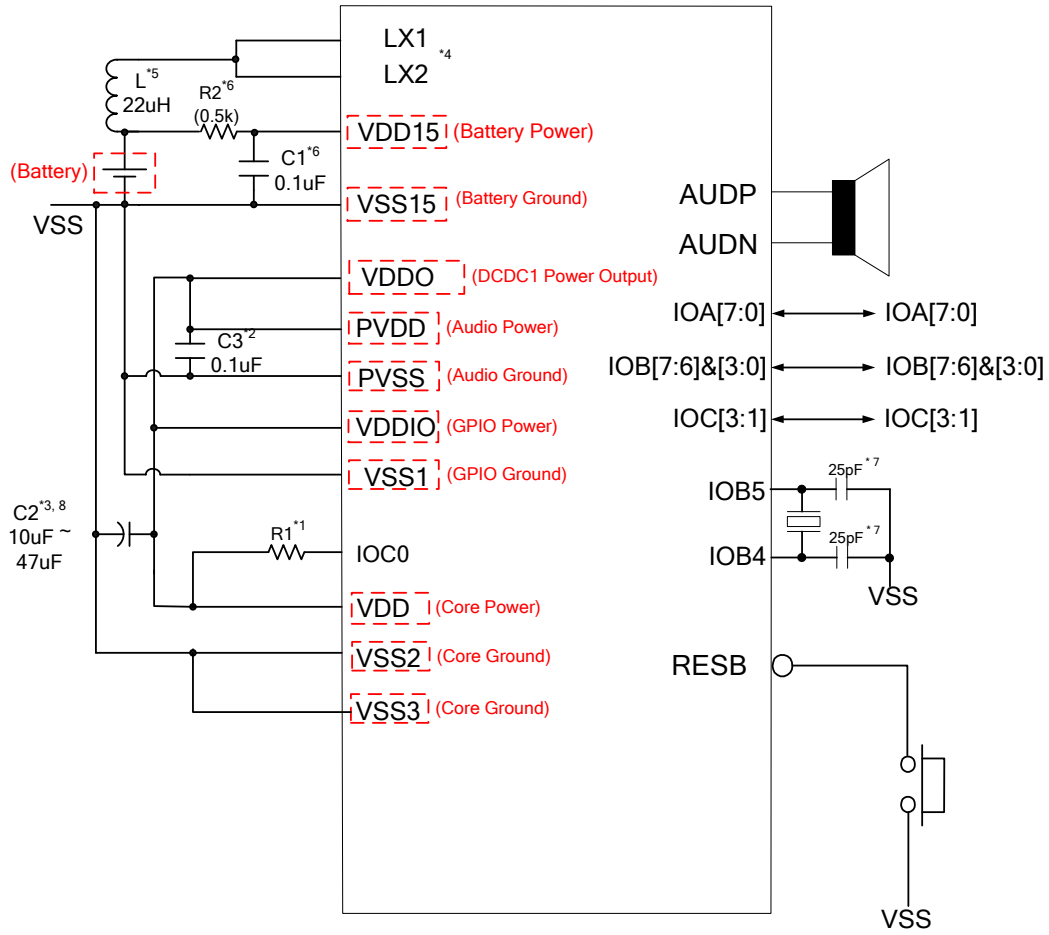


8.10.2. Frequency vs. VDD (build-in 8MHz ROSC)



9. APPLICATION CIRCUITS

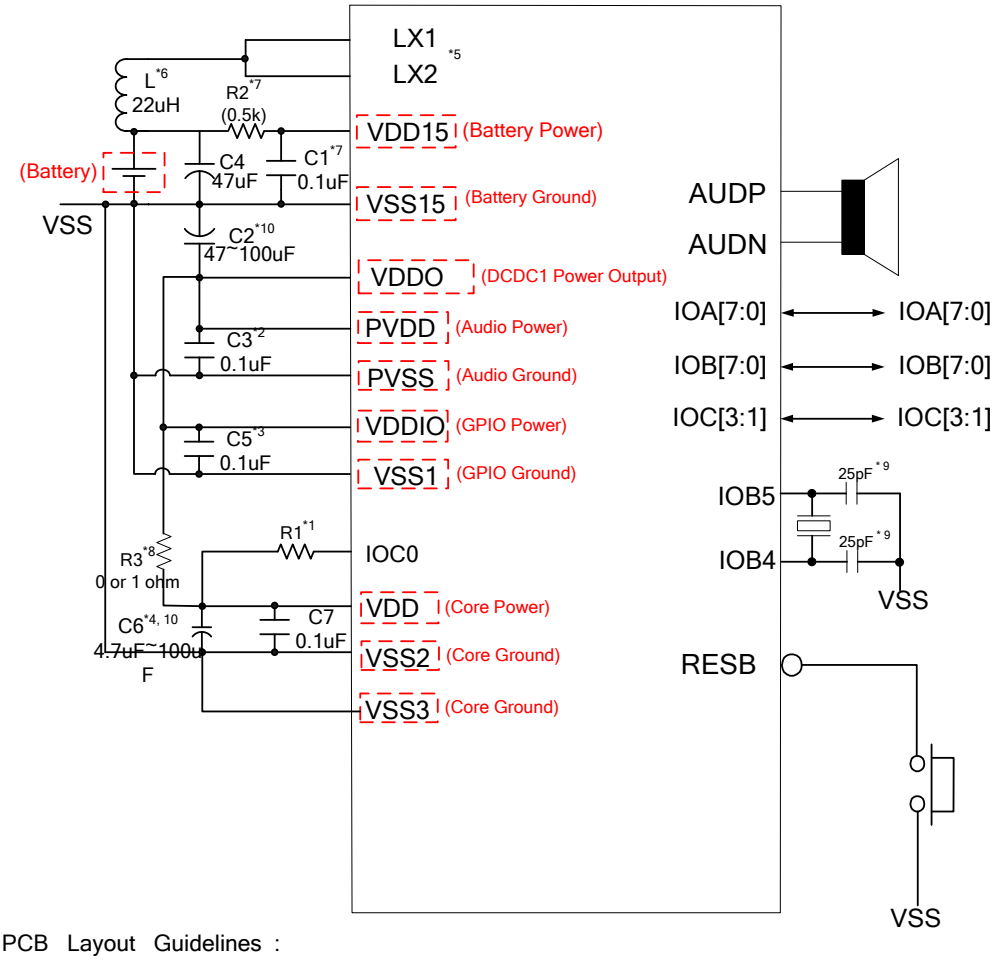
9.1. Light Loading and Circuit without Noise for GPC3L170A~GPC3L096A



PCB Layout Guidelines :

1. R1 (used for ROSC) should be as close as possible to IOC0 pin.
2. C3 should be as close as possible to PVDD/PVSS, and C3 can be removed if there is good power line layout on PCB that no harm to sound quality.
3. The value of C2 depends on the loading. 10uF~47uF is the suggested value range. One end of C2 should be placed between VSS1, VSS2, VSS3 and VSS15. The other end of C2 should be placed between VDDO, VDDIO and VDD. C2 should be as close as possible to VDDO/VDDIO/VDD
4. Net between LX1 and LX2 should be as short as possible.
5. L should be as close as possible to VDD15/LX1/LX2. **Please use inductance with lower resistance to gain higher efficiency, 22uH/0.5W@IDC(max)>250mA, DCR<1 ohm is the suggested inductance spec.**
6. R2 and C1 could be removed if do not care BVD flag vibration due to VDD15 bouncing.
7. These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).
8. **Please use capacitor (C2) with lower resistance to reduce noise, ESR<2 ohm in 0~70C is suggested.**

9.2. Heavy Loading or Circuit with Noise for GPC3L170A~GPC3L096A



PCB Layout Guidelines :

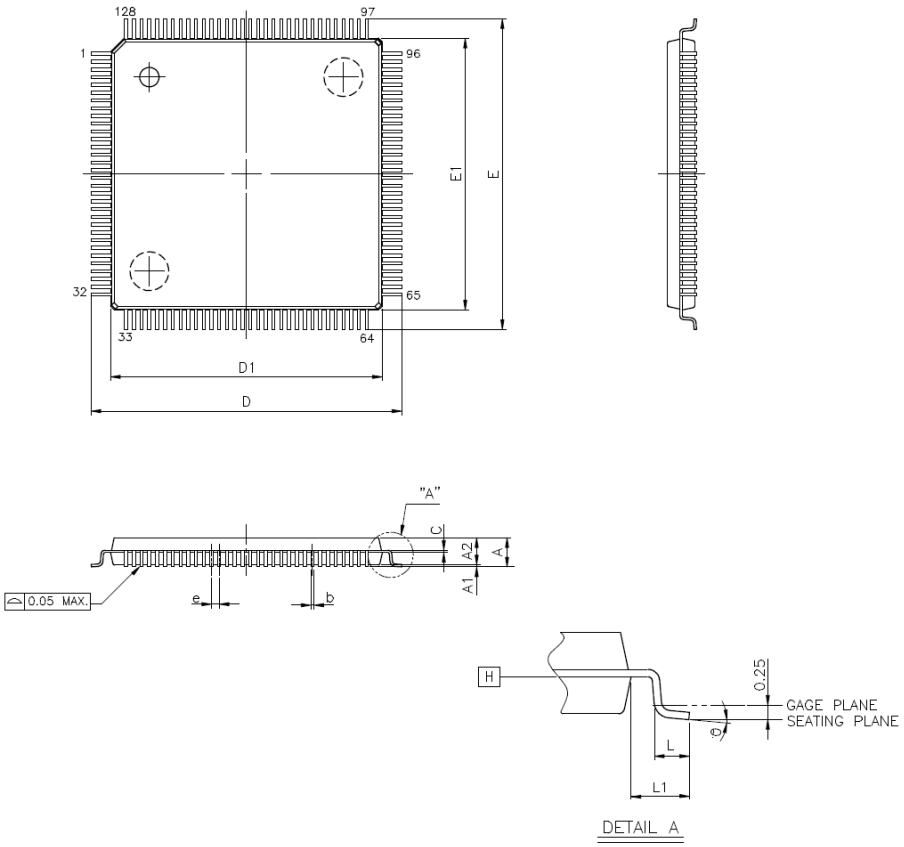
1. R1 (used for ROSC) should be as close as possible to IOC0 pin.
2. C3 should be as close as possible to PVDD/PVSS, and C3 can be removed if there is good power line layout on PCB that no harm to sound quality.
3. C5 should be as close as possible to VDDIO/VSS1, and C5 can be removed if there is good power line layout on PCB that the power stable enough.
4. The value of C6 depends on the loading. 4.7uF~100uF is the suggested value range. C6 should be as close as possible to VDD/VSS2, and C6 can be smaller if there is good power line layout on PCB that the power stable enough.
5. Net between LX1 and LX2 should be as short as possible.
6. L should be as close as possible to VDD15/LX1/LX2. **Please use inductance with lower resistance to gain higher efficiency, 22uH/0.5W@IDC(max)>250mA ,DCR<1 ohm is the suggested inductance spec.**
7. R2 and C1 could be removed if do not care BVD flag vibration due to VDD15 bouncing.
8. R3 with 0 Ohm is suggested for 2 batteries or C6 > 10uF and with 1 Ohm is suggested for 1 battery and C6 < 10uF.
9. These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).
10. **Please use capacitors (C2 and C6) with lower resistance to reduce noise, ESR<2 ohm in 0~70C is suggested.**

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPC3LXXXX - C	Chip form
GPC3LXXXX - NnnV – QL09X	Halogen free LQFP128 package

10.2. Package LQFP128 Information



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:

1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

11. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

12. REVISION HISTORY

Date	Revision #	Description	Page
Jun. 02, 2017	1.2	1.Add LQFP128 information.	7, 16
Dec. 20, 2013	1.1	1.Add notice to capacitors in application circuits. 2.Modify “ESR” to “DCR” for inductor impedance. 3.Modify VDD max supplied current.	10, 11, 12, 14, 15
Oct. 07, 2013	1.0	Original	