MSP430™ SoC With RF Core

Check for Samples: CC430F6137, CC430F6135, CC430F6127, CC430F6126, CC430F6125, CC430F5137, CC430F5135, CC430F5133

FEATURES

- **True System-on-Chip (SoC) for Low-Power Wireless Communication Applications**
- **Wide Supply Voltage Range: 3.6 V Down to 1.8 V**
- **Ultralow-Power Consumption:**
  - **CPU Active Mode (AM): 160 µA/MHz**
  - **Standby Mode (LPM3 RTC Mode): 2.0 µA**
  - **Off Mode (LPM4 RAM Retention): 1.0 µA**
  - **Radio in RX: 15 mA, 250 kbps, 915 MHz**
- **MSP430 System and Peripherals**
  - **16-Bit RISC Architecture, Extended Memory, up to 20-MHz System Clock**
  - **Wake Up From Standby Mode in Less Than 6 µs**
  - **Flexible Power-Management System With SVS and Brownout**
  - **Unified Clock System With FLL**
  - **16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers**
  - **16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers**
  - **Hardware Real-Time Clock (RTC)**
  - **Two Universal Serial Communication Interfaces**
    - **USCI_A0 Supports UART, IrDA, SPI**
    - **USCI_B0 Supports I^2C, SPI**
  - **12-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold, and Autoscan Features (CC430F613x and CC430F513x Only)**
  - **Comparator**
  - **Integrated LCD Driver With Contrast Control for up to 96 Segments (CC430F61xx Only)**
  - **128-Bit AES Security Encryption and Decryption Coprocessor**
  - **32-Bit Hardware Multiplier**
  - **Three-Channel Internal DMA**
  - **Serial Onboard Programming, No External Programming Voltage Needed**
  - **Embedded Emulation Module (EEM)**
- **High-Performance Sub-1-GHz RF Transceiver Core**
  - **Same as in CC1101**
  - **Wide Supply Voltage Range: 2.0 V to 3.6 V**
  - **Frequency Bands: 300 MHz to 348 MHz, 389 MHz to 464 MHz, and 779 MHz to 928 MHz**
  - **Programmable Data Rate From 0.6 kBaud to 500 kBaud**
  - **High Sensitivity (–117 dBm at 0.6 kBaud, –111 dBm at 1.2 kBaud, 315 MHz, 1% Packet Error Rate)**
  - **Excellent Receiver Selectivity and Blocking Performance**
  - **Programmable Output Power Up to +12 dBm for All Supported Frequencies**
  - **2-FSK, 2-GFSK, and MSK Supported as Well as OOK and Flexible ASK Shaping**
  - **Flexible Support for Packet-Oriented Systems: On-Chip Support for Sync Word Detection, Address Check, Flexible Packet Length, and Automatic CRC Handling**
  - **Support for Automatic Clear Channel Assessment (CCA) Before Transmitting (for Listen-Before-Talk Systems)**
  - **Digital RSSI Output**
  - **Suited for Systems Targeting Compliance With EN 300 220 (Europe) and FCC CFR Part 15 (US)**
  - **Suited for Systems Targeting Compliance With Wireless M-Bus Standard EN 13757-4:2005**
  - **Support for Asynchronous and Synchronous Serial Receive or Transmit Mode for Backward Compatibility With Existing Radio Communication Protocols**
- **Table 1 Summarizes Family Members**
- **For Complete Module Descriptions, See the *CC430 Family User's Guide* (SLAU259)**

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APPLICATIONS

- **Wireless Analog and Digital Sensor Systems**
- **Heat Cost Allocators**
- **Thermostats**
- **AMR or AMI Metering**
- **Smart Grid Wireless Networks**

DESCRIPTION

The Texas Instruments CC430 family of ultralow-power microcontroller system-on-chip (SoC) with integrated RF transceiver cores consists of several devices featuring different sets of peripherals targeted for a wide range of applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features the powerful MSP430 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The CC430 family provides a tight integration between the microcontroller core, its peripherals, software, and the RF transceiver, making these true SoC solutions easy to use as well as improving performance.

The CC430F61xx series are microcontroller SoC configurations that combine the excellent performance of the state-of-the-art CC1101 sub-1-GHz RF transceiver with the MSP430 CPUXV2, up to 32KB of in-system programmable flash memory, up to 4KB of RAM, two 16-bit timers, a high-performance 12-bit analog-to-digital converter (ADC) with eight external inputs plus internal temperature and battery sensors on CC430F613x devices, a comparator, universal serial communication interfaces (USCIs), a 128-bit AES security accelerator, a hardware multiplier, a DMA, a real-time clock (RTC) module with alarm capabilities, an LCD driver, and up to 44 I/O pins.

The CC430F513x series are microcontroller SoC configurations that combine the excellent performance of the state-of-the-art CC1101 sub-1-GHz RF transceiver with the MSP430 CPUXV2, up to 32KB of in-system programmable flash memory, up to 4KB of RAM, two 16-bit timers, a high performance 12-bit ADC with six external inputs plus internal temperature and battery sensors, a comparator, universal serial communication interfaces (USCIs), a 128-bit AES security accelerator, a hardware multiplier, a DMA, an RTC module with alarm capabilities, and up to 30 I/O pins.

Typical applications for these devices include wireless analog and digital sensor systems, heat cost allocators, thermostats, metering (AMR or AMI), and smart grid wireless networks.

Table 1 summarizes the available family members.

For complete module descriptions, see the *CC430 Family User's Guide* (SLAU259).

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Table 1. Family Members(1)(2)

Device	Program (KB)	SRAM (KB)	Timer_A(3)	LCD_B(4)	USCI		ADC12_A(4)	Comp_B	I/O	Package Type
					Channel A: UART, LIN, IrDA, SPI	Channel B: SPI, I^2C				
CC430F6137	32	4	5, 3	96 seg	1	1	8 ext, 4 int ch.	8 ch.	44	64 RGC
CC430F6135	16	2	5, 3	96 seg	1	1	8 ext, 4 int ch.	8 ch.	44	64 RGC
CC430F6127	32	4	5, 3	96 seg	1	1	n/a	8 ch.	44	64 RGC
CC430F6126	32	2	5, 3	96 seg	1	1	n/a	8 ch.	44	64 RGC
CC430F6125	16	2	5, 3	96 seg	1	1	n/a	8 ch.	44	64 RGC
CC430F5137	32	4	5, 3	n/a	1	1	6 ext, 4 int ch.	6 ch.	30	48 RGZ
CC430F5135	16	2	5, 3	n/a	1	1	6 ext, 4 int ch.	6 ch.	30	48 RGZ
CC430F5133	8	2	5, 3	n/a	1	1	6 ext, 4 int ch.	6 ch.	30	48 RGZ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 5, 3 would represent two instantiations of Timer_A, the first instantiation having 5 and the second instantiation having 3 capture compare registers and PWM output generators, respectively.
(4) n/a = not available

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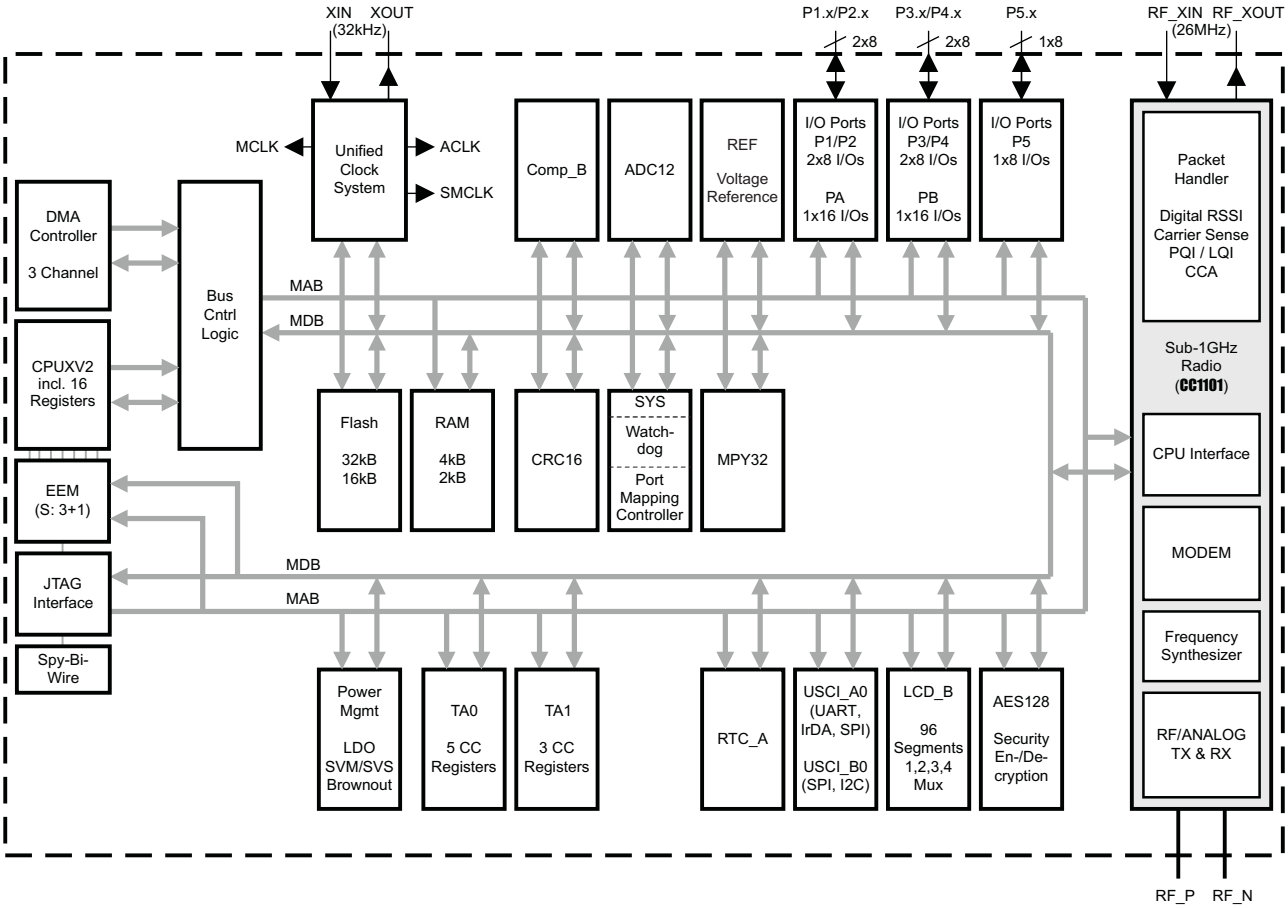
CC430F613x Functional Block Diagram



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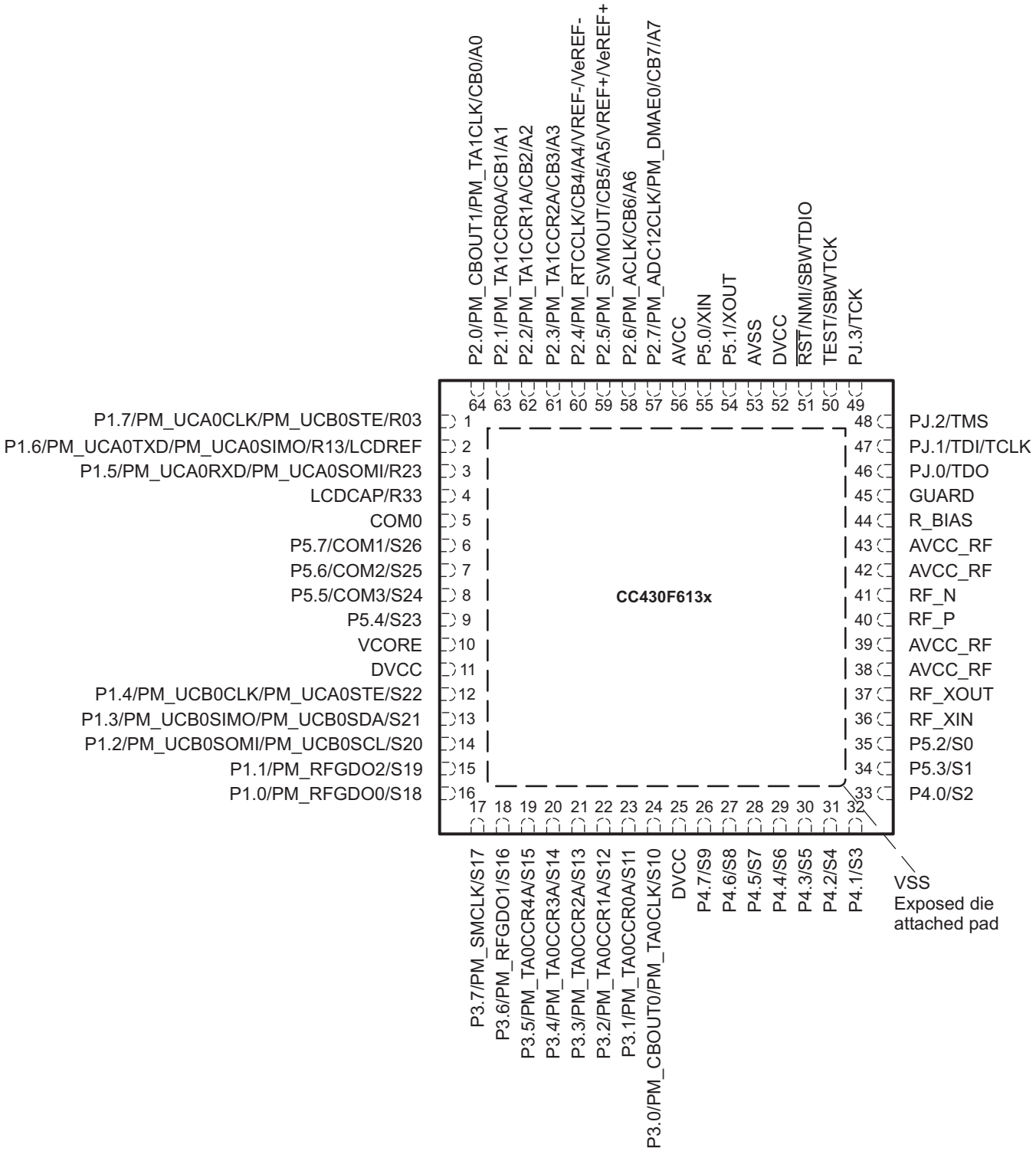
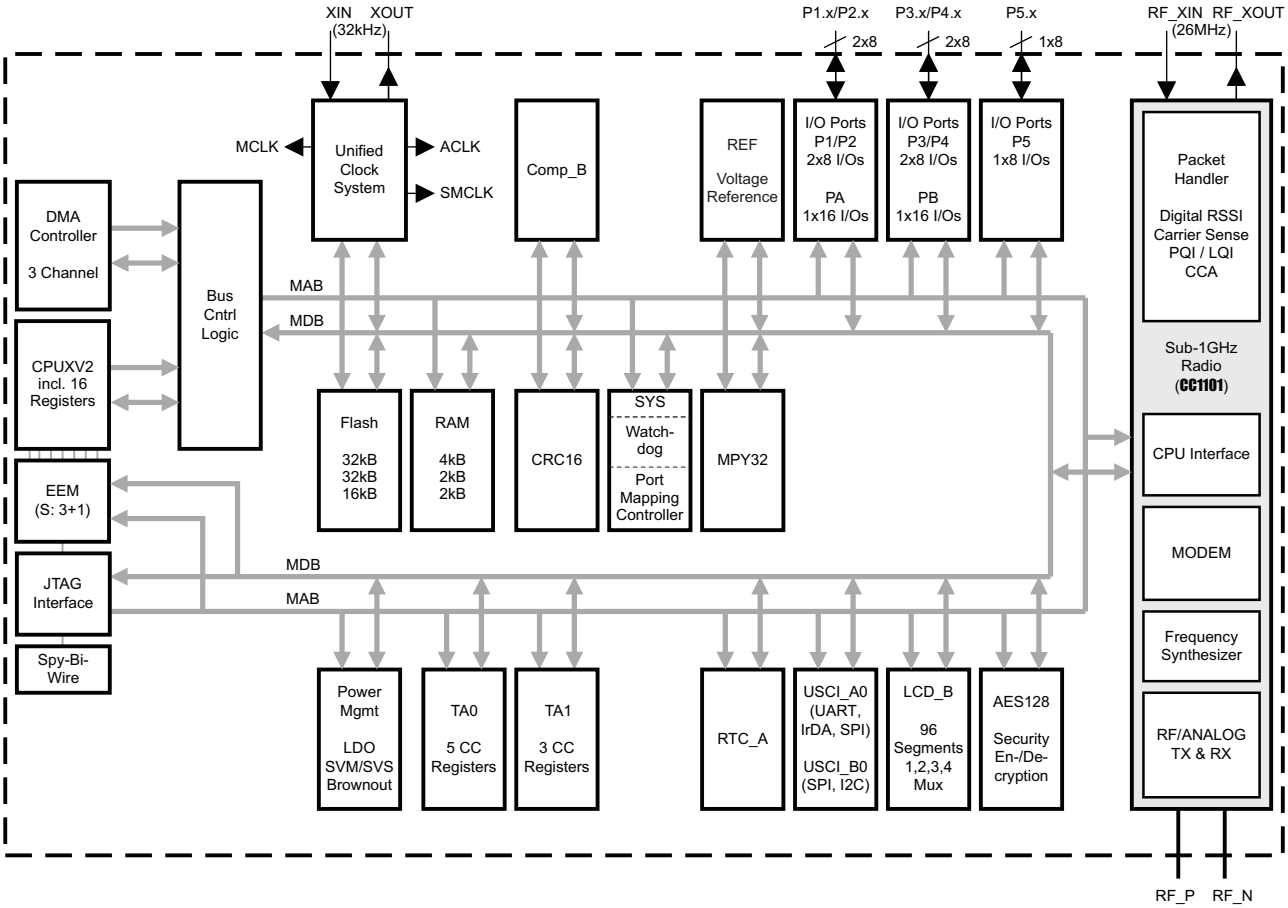
RGC PACKAGE
(TOP VIEW)



NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. This pinout shows only the default mapping. See Table 9 for details.

CAUTION: The LCDCAP/R33 must be connected to VSS if not used.

CC430F612x Functional Block Diagram



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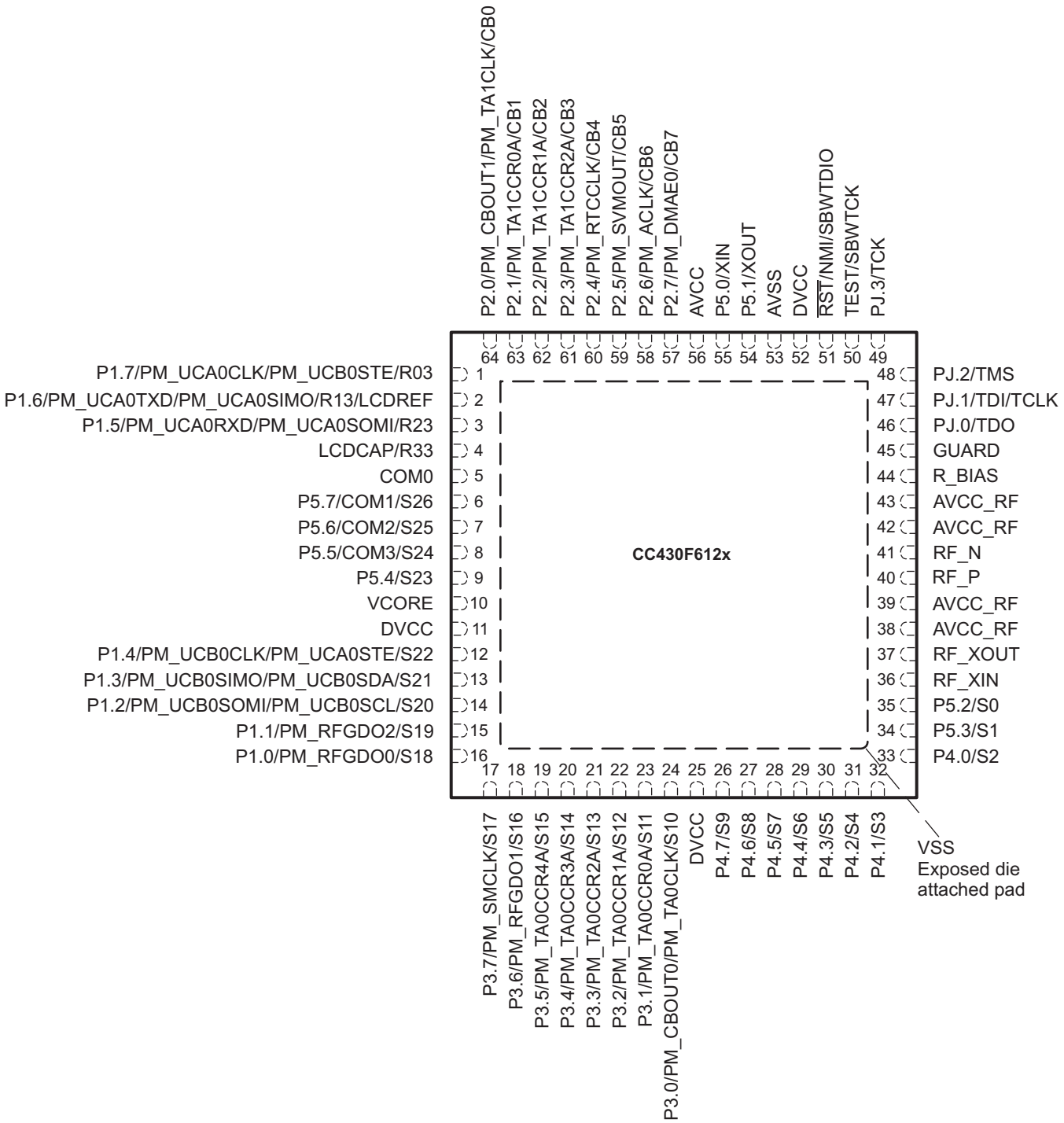
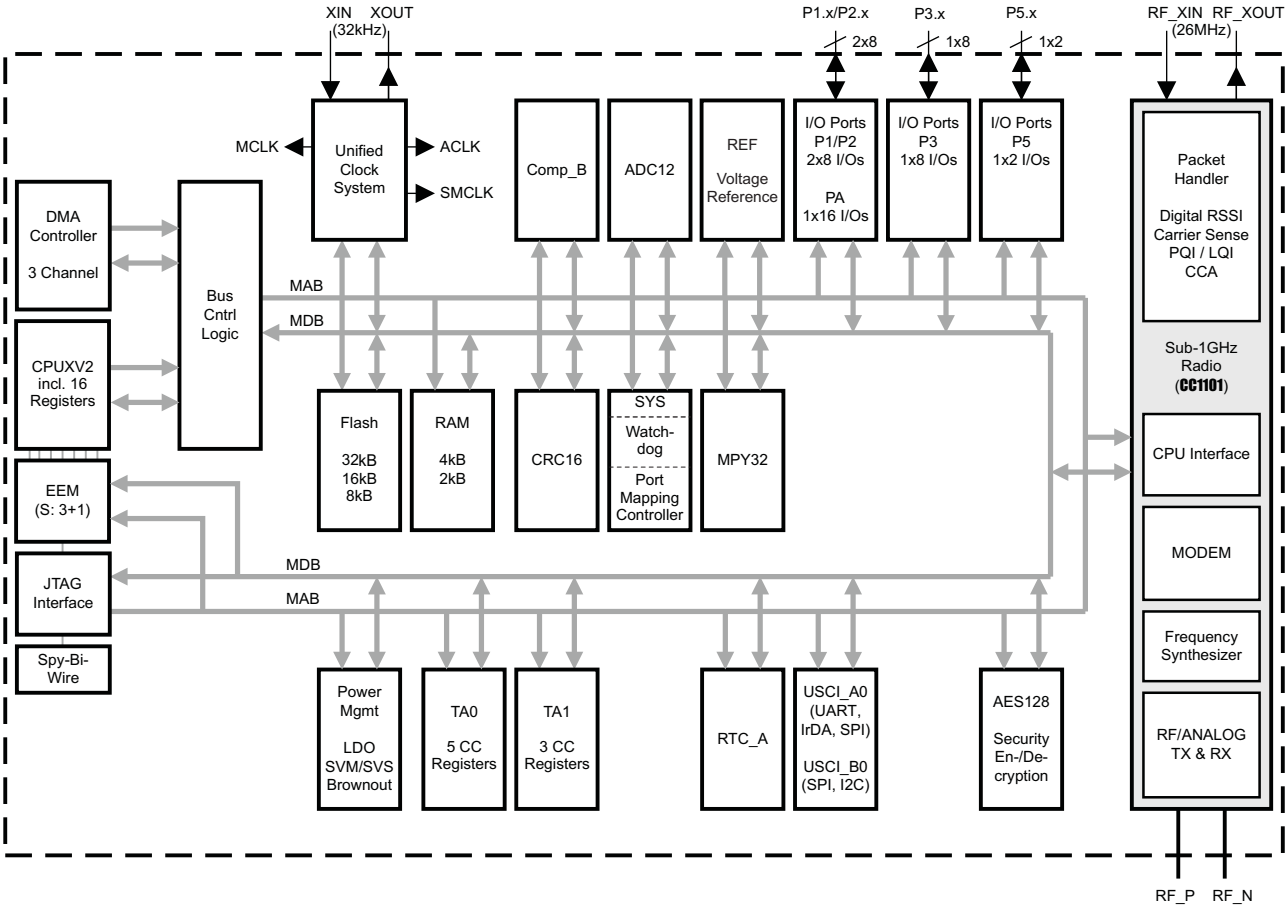
RGC PACKAGE
(TOP VIEW)



NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. This pinout shows only the default mapping. See Table 9 for details.

CAUTION: The LCDCAP/R33 must be connected to VSS if not used.

CC430F513x Functional Block Diagram



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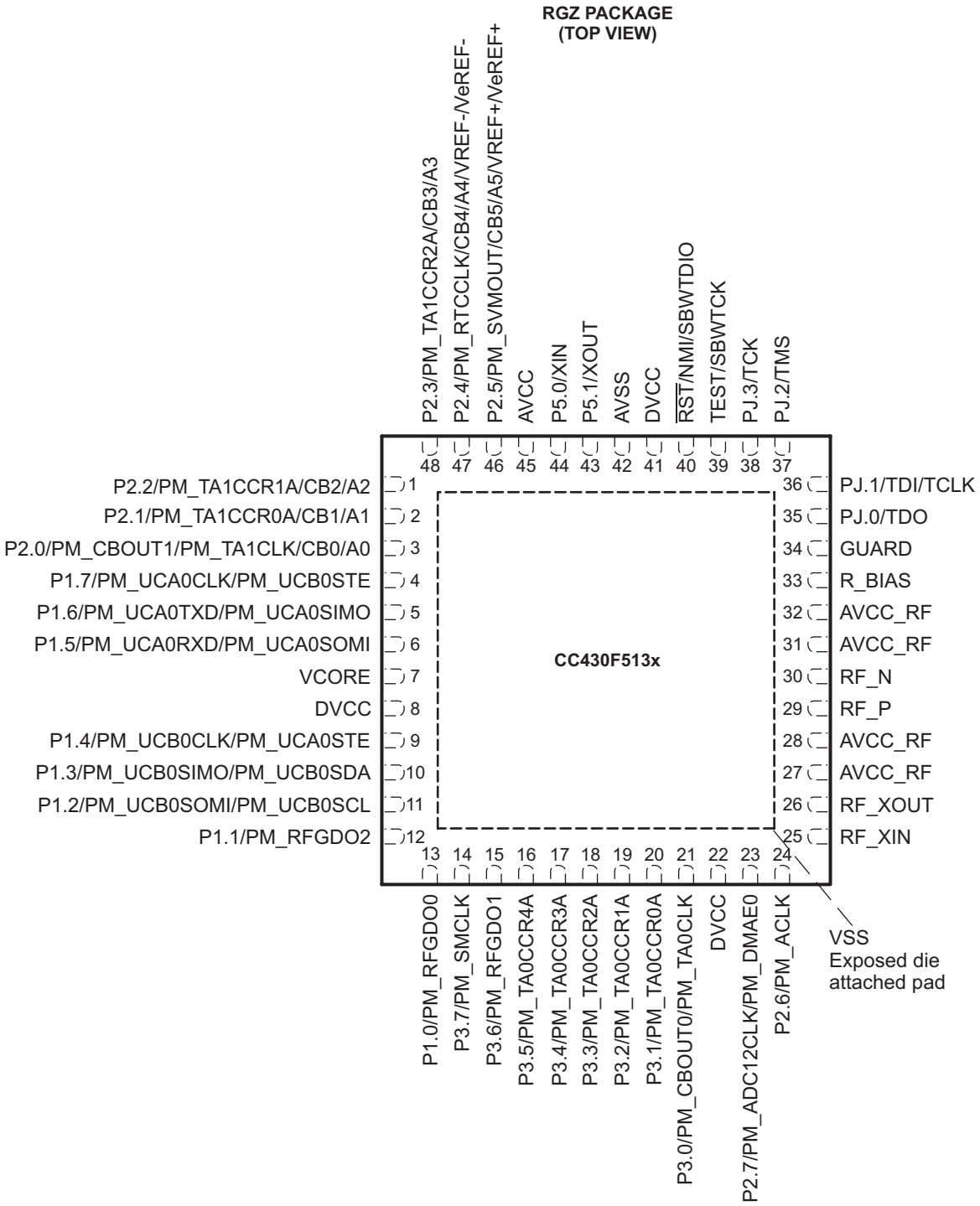
RGZ PACKAGE
(TOP VIEW)



NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. This pinout shows only the default mapping. See Table 9 for details.

Table 2. CC430F613x and CC430F612x Terminal Functions

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
P1.7/ PM_UCA0CLK/ PM_UCB0STE/ R03	1	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 clock input/output; USCI_B0 SPI slave transmit enable Input/output port of lowest analog LCD voltage (V5)
P1.6/ PM_UCA0TXD/ PM_UCA0SIMO/ R13/LCDREF	2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in master out Input/output port of third most positive analog LCD voltage (V3 or V4) External reference voltage input for regulated LCD voltage
P1.5/ PM_UCA0RXD/ PM_UCA0SOMI/ R23	3	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART receive data; USCI_A0 SPI slave out master in Input/output port of second most positive analog LCD voltage (V2)
LCDCAP/ R33	4	I/O	LCD capacitor connection Input/output port of most positive analog LCD voltage (V1) **CAUTION:** Must be connected to VSS if not used.
COM0	5	O	LCD common output COM0 for LCD backplane
P5.7/ COM1/ S26	6	I/O	General-purpose digital I/O LCD common output COM1 for LCD backplane LCD segment output S26
P5.6/ COM2/ S25	7	I/O	General-purpose digital I/O LCD common output COM2 for LCD backplane LCD segment output S25
P5.5/ COM3/ S24	8	I/O	General-purpose digital I/O LCD common output COM3 for LCD backplane LCD segment output S24
P5.4/ S23	9	I/O	General-purpose digital I/O LCD segment output S23
VCORE	10		Regulated core power supply
DVCC	11		Digital power supply
P1.4/ PM_UCB0CLK/ PM_UCA0STE/ S22	12	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable LCD segment output S22
P1.3/ PM_UCB0SIMO/ PM_UCB0SDA/ S21	13	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave in master out; USCI_B0 I2C data LCD segment output S21
P1.2/ PM_UCB0SOMI/ PM_UCB0SCL/ S20	14	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave out master in; UCSI_B0 I2C clock LCD segment output S20
P1.1/ PM_RFGDO2/ S19	15	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO2 output LCD segment output S19
P1.0/ PM_RFGDO0/ S18	16	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO0 output LCD segment output S18
P3.7/ PM_SMCLK/ S17	17	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SMCLK output LCD segment output S17
P3.6/ PM_RFGDO1/ S16	18	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Radio GDO1 output LCD segment output S16
P3.5/ PM_TA0CCR4A/ S15	19	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR4 compare output or capture input LCD segment output S15
P3.4/ PM_TA0CCR3A/ S14	20	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR3 compare output or capture input LCD segment output S14
P3.3/ PM_TA0CCR2A/ S13	21	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR2 compare output or capture input LCD segment output S13

(1) I = input, O = output

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Table 2. CC430F613x and CC430F612x Terminal Functions (continued)

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
P3.2/ PM_TA0CCR1A/ S12	22	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR1 compare output or capture input LCD segment output S12
P3.1/ PM_TA0CCR0A/ S11	23	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR0 compare output or capture input LCD segment output S11
P3.0/ PM_CBOUT0/PM_TA0CLK/ S10	24	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Comparator_B output; TA0 clock input LCD segment output S10
DVCC	25		Digital power supply
P4.7/ S9	26	I/O	General-purpose digital I/O LCD segment output S9
P4.6/ S8	27	I/O	General-purpose digital I/O LCD segment output S8
P4.5/ S7	28	I/O	General-purpose digital I/O LCD segment output S7
P4.4/ S6	29	I/O	General-purpose digital I/O LCD segment output S6
P4.3/ S5	30	I/O	General-purpose digital I/O LCD segment output S5
P4.2/ S4	31	I/O	General-purpose digital I/O LCD segment output S4
P4.1/ S3	32	I/O	General-purpose digital I/O LCD segment output S3
P4.0/ S2	33	I/O	General-purpose digital I/O LCD segment output S2
P5.3/ S1	34	I/O	General-purpose digital I/O LCD segment output S1
P5.2/ S0	35	I/O	General-purpose digital I/O LCD segment output S0
RF_XIN	36	I	Input terminal for RF crystal oscillator, or external clock input
RF_XOUT	37	O	Output terminal for RF crystal oscillator
AVCC_RF	38		Radio analog power supply
AVCC_RF	39		Radio analog power supply
RF_P	40	RF I/O	Positive RF input to LNA in receive mode Positive RF output from PA in transmit mode
RF_N	41	RF I/O	Negative RF input to LNA in receive mode Negative RF output from PA in transmit mode
AVCC_RF	42		Radio analog power supply
AVCC_RF	43		Radio analog power supply
RBIAS	44		External bias resistor for radio reference current
GUARD	45		Power supply connection for digital noise isolation
PJ.0/ TDO	46	I/O	General-purpose digital I/O Test data output port
PJ.1/ TDI/ TCLK	47	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/ TMS	48	I/O	General-purpose digital I/O Test mode select
PJ.3/ TCK	49	I/O	General-purpose digital I/O Test clock
TEST/ SBWTCK	50	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock

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Table 2. CC430F613x and CC430F612x Terminal Functions (continued)

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
$\overline{\text{RST}}$/NMI/ SBWTDIO	51	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output
DVCC	52		Digital power supply
AVSS	53		Analog ground supply for ADC12
P5.1/ XOUT	54	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
P5.0/ XIN	55	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
AVCC	56		Analog power supply
P2.7/ PM_ADC12CLK/ PM_DMAE0/ CB7 (/A7)	57	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ADC12CLK output; DMA external trigger input Comparator_B input CB7 Analog input A7 – 12-bit ADC (CC430F613x only)
P2.6/ PM_ACLK/ CB6 (/A6)	58	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ACLK output Comparator_B input CB6 Analog input A6 – 12-bit ADC (CC430F613x only)
P2.5/ PM_SVMOUT/ CB5 (/A5/ VREF+/ VeREF+)	59	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: SVM output Comparator_B input CB5 Analog input A5 – 12-bit ADC (CC430F613x only) Output of reference voltage to the ADC (CC430F613x only) Input for an external reference voltage to the ADC (CC430F613x only)
P2.4/ PM_RTCCLK/ CB4 (/A4/ VREF-/ VeREF-)	60	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: RTCCLK output Comparator_B input CB4 Analog input A4 – 12-bit ADC (CC430F613x only) Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage (CC430F613x only)
P2.3/ PM_TA1CCR2A/ CB3 (/A3)	61	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR2 compare output or capture input Comparator_B input CB3 Analog input A3 – 12-bit ADC (CC430F613x only)
P2.2/ PM_TA1CCR1A/ CB2 (/A2)	62	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR1 compare output or capture input Comparator_B input CB2 Analog input A2 – 12-bit ADC (CC430F613x only)
P2.1/PM_TA1CCR0A/CB1(/A1)	63	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR0 compare output or capture input Comparator_B input CB1 Analog input A1 – 12-bit ADC (CC430F613x only)
P2.0/ PM_CBOUT1/ PM_TA1CLK/ CB0 (/A0)	64	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Comparator_B output; TA1 clock input Comparator_B input CB0 Analog input A0 – 12-bit ADC (CC430F613x only)
VSS - Exposed die attach pad			Ground supply **The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.**

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Table 3. CC430F513x Terminal Functions

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
P2.2/ PM_TA1CCR1A/ CB2/ A2	1	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR1 compare output or capture input Comparator_B input CB2 Analog input A2 – 12-bit ADC
P2.1/ PM_TA1CCR0A/ CB1/ A1	2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR0 compare output or capture input Comparator_B input CB1 Analog input A1 – 12-bit ADC
P2.0/ PM_CBOUT1/ PM_TA1CLK/ CB0/ A0	3	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Comparator_B output; TA1 clock input Comparator_B input CB0 Analog input A0 – 12-bit ADC
P1.7/ PM_UCA0CLK/ PM_UCB0STE	4	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 clock input/output / USCI_B0 SPI slave transmit enable
P1.6/ PM_UCA0TXD/ PM_UCA0SIMO	5	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in master out
P1.5/ PM_UCA0RXD/ PM_UCA0SOMI	6	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART receive data; USCI_A0 SPI slave out master in
VCORE	7		Regulated core power supply
DVCC	8		Digital power supply
P1.4/ PM_UCB0CLK/ PM_UCA0STE	9	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 clock input/output / USCI_A0 SPI slave transmit enable
P1.3/ PM_UCB0SIMO/ PM_UCB0SDA	10	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave in master out/USCI_B0 I2C data
P1.2/ PM_UCB0SOMI/ PM_UCB0SCL	11	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave out master in/UCSI_B0 I2C clock
P1.1/ PM_RFGDO2	12	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO2 output
P1.0/ PM_RFGDO0	13	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO0 output
P3.7/ PM_SMCLK	14	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SMCLK output
P3.6/ PM_RFGDO1	15	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Radio GDO1 output
P3.5/ PM_TA0CCR4A	16	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR4 compare output or capture input
P3.4/ PM_TA0CCR3A	17	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR3 compare output or capture input
P3.3/ PM_TA0CCR2A	18	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR2 compare output or capture input
P3.2/ PM_TA0CCR1A	19	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR1 compare output or capture input
P3.1/ PM_TA0CCR0A	20	I/O	General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR0 compare output or capture input
P3.0/ PM_CBOUT0/ PM_TA0CLK	21	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Comparator_B output; TA0 clock input
DVCC	22		Digital power supply
P2.7/ PM_ADC12CLK/ PM_DMAE0	23	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ADC12CLK output; DMA external trigger input
P2.6/ PM_ACLK	24	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ACLK output
RF_XIN	25	I	Input terminal for RF crystal oscillator, or external clock input
RF_XOUT	26	O	Output terminal for RF crystal oscillator
AVCC_RF	27		Radio analog power supply

(1) I = input, O = output

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Table 3. CC430F513x Terminal Functions (continued)

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
AVCC_RF	28		Radio analog power supply
RF_P	29	RF I/O	Positive RF input to LNA in receive mode Positive RF output from PA in transmit mode
RF_N	30	RF I/O	Negative RF input to LNA in receive mode Negative RF output from PA in transmit mode
AVCC_RF	31		Radio analog power supply
AVCC_RF	32		Radio analog power supply
RBIAS	33		External bias resistor for radio reference current
GUARD	34		Power supply connection for digital noise isolation
PJ.0/ TDO	35	I/O	General-purpose digital I/O Test data output port
PJ.1/ TDI/ TCLK	36	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/ TMS	37	I/O	General-purpose digital I/O Test mode select
PJ.3/ TCK	38	I/O	General-purpose digital I/O Test clock
TEST/ SBWTCK	39	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
$\overline{\text{RST}}$/NMI/ SBWTDIO	40	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output
DVCC	41		Digital power supply
AVSS	42		Analog ground supply for ADC12
P5.1/ XOUT	43	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
P5.0/ XIN	44	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
AVCC	45		Analog power supply
P2.5/ PM_SVMOUT/ CB5/ A5/ VREF+/ VeREF+	46	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: SVM output Comparator_B input CB5 Analog input A5 – 12-bit ADC Output of reference voltage to the ADC Input for an external reference voltage to the ADC
P2.4/ PM_RTCCLK/ CB4/ A4/ VREF-/ VeREF-	47	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: RTCCLK output Comparator_B input CB4 Analog input A4 – 12-bit ADC Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
P2.3/ PM_TA1CCR2A/ CB3/ A3	48	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR2 compare output or capture input Comparator_B input CB3 Analog input A3 – 12-bit ADC
VSS - Exposed die attach pad			Ground supply **The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.**

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Short-Form Description

Sub-1-GHz Radio

The implemented sub-1-GHz radio module is based on the industry-leading CC1101, requiring very few external components. Figure 1 shows a high-level block diagram of the implemented radio.

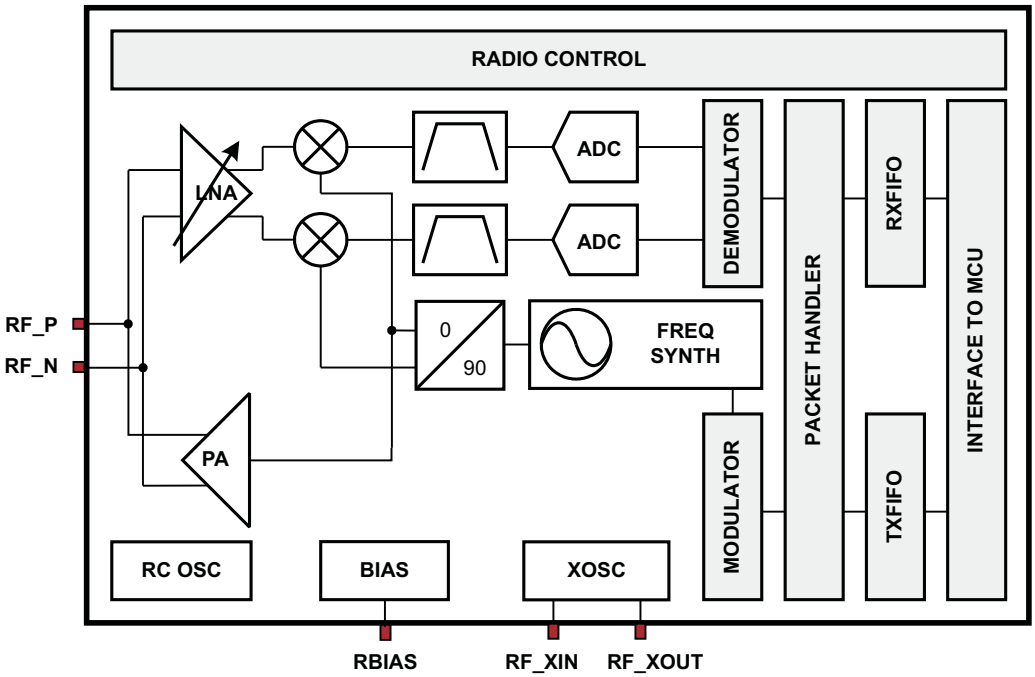

Figure 1. Sub-1-GHz Radio Block Diagram

The radio features a low-IF receiver. The received RF signal is amplified by a low-noise amplifier (LNA) and down-converted in quadrature to the intermediate frequency (IF). At IF, the I/Q signals are digitized. Automatic gain control (AGC), fine channel filtering, demodulation bit and packet synchronization are performed digitally.

The transmitter part is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90° phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

The 26-MHz crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A memory mapped register interface is used for data access, configuration, and status request by the CPU.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

For complete module descriptions, see the *CC430 Family User's Guide* (SLAU259).

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Operating Modes

The CC430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention

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Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Password Violation Flash Memory Password Violation	WDTIFG, KEYV (SYSRSTIV)(1)(2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)(3)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG (SYSUNIV)(1)(3)	(Non)maskable	0FFFAh	61
Comparator_B	Comparator_B Interrupt Flags (CBIV)(1)	Maskable	0FFF8h	60
Watchdog Interval Timer Mode	WDTIFG	Maskable	0FFF6h	59
USCI_A0 Receive or Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)	Maskable	0FFF4h	58
USCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG, I2C Status Interrupt Flags (UCB0IV)(1)	Maskable	0FFF2h	57
ADC12_A (Reserved on CC430F612x)	ADC12IFG0 ... ADC12IFG15 (ADC12IV)(1)	Maskable	0FFF0h	56
TA0	TA0CCR0 CCIFG0	Maskable	0FFEEh	55
TA0	TA0CCR1 CCIFG1 ... TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1)	Maskable	0FFECh	54
RF1A CC1101-based Radio	Radio Interface Interrupt Flags (RF1AIFIV) Radio Core Interrupt Flags (RF1AIV)	Maskable	0FFEAh	53
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1)	Maskable	0FFE8h	52
TA1	TA1CCR0 CCIFG0	Maskable	0FFE6h	51
TA1	TA1CCR1 CCIFG1 ... TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1)	Maskable	0FFE4h	50
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)	Maskable	0FFE2h	49
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)	Maskable	0FFE0h	48
LCD_B (Reserved on CC430F513x)	LCD_B Interrupt Flags (LCDBIV)(1)	Maskable	0FFDEh	47
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1)	Maskable	0FFDCh	46
AES	AESRDYIFG	Maskable	0FFDAh	45
Reserved	Reserved(4)		0FFD8h	44
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space.
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

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Memory Organization

Table 5. Memory Organization

		CC430F6137 CC430F6127 CC430F5137(1)	CC430F6126(1)	CC430F6135 CC430F6125 CC430F5135(1)	CC430F5133(1)
Main Memory (flash)	Total Size	32kB	32kB	16kB	8kB
Main: Interrupt vector		00FFFFh to 00FF80h	00FFFFh to 00FF80h	00FFFFh to 00FF80h	00FFFFh to 00FF80h
Main: code memory	Bank 0	32kB 00FFFFh to 008000h	32kB 00FFFFh to 008000h	16kB 00FFFFh to 00C000h	8kB 00FFFFh to 00E000h
RAM	Total Size	4kB	2kB	2kB	2kB
	Sect 1	2kB 002BFFh to 002400h	not available	not available	not available
	Sect 0	2kB 0023FFh to 001C00h	2kB 0023FFh to 001C00h	2kB 0023FFh to 001C00h	2kB 0023FFh to 001C00h
Device Descriptor		128 B 001AFFh to 001A80h	128 B 001AFFh to 001A80h	128 B 001AFFh to 001A80h	128 B 001AFFh to 001A80h
		128 B 001A7Fh to 001A00h	128 B 001A7Fh to 001A00h	128 B 001A7Fh to 001A00h	128 B 001A7Fh to 001A00h
Information memory (flash)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootstrap loader (BSL) memory (flash)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals		4 KB 000FFFh to 0h	4 KB 000FFFh to 0h	4 KB 000FFFh to 0h	4 KB 000FFFh to 0h

(1) All memory regions not specified here are vacant memory, and any access to them causes a Vacant Memory Interrupt.

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory via the BSL is protected by an user-defined password. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 6. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.6	Data transmit
P1.5	Data receive
VCC	Power supply
VSS	Ground supply

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JTAG Operation

JTAG Standard Interface

The CC430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 7. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 7. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the CC430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 8. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 8. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (Info A to Info D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments Info A to Info D can be erased individually, or as a group with the main memory segments. Segments Info A to Info D are also called *information memory*.
- Segment A can be locked separately.

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RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however, all data is lost. Features of the RAM memory include:

- RAM memory has n sectors of 2k bytes each.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *CC430 Family User's Guide* (SLAU259).

Oscillator and System Clock

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The UCS module is designed to meet the requirements of both low system cost and low-power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Digital I/O

There are up to five 8-bit I/O ports implemented: ports P1 through P5.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P5) or word-wise in pairs (PA and PB).

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Port Mapping Controller

The port mapping controller allows the flexible and re-configurable mapping of digital functions to port pins of ports P1 through P3.

Table 9. Port Mapping, Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION (PxDIR.y = 0)	OUTPUT PIN FUNCTION (PxDIR.y = 1)
0	PM_NONE	None	DVSS
1 (1)	PM_CBOUT0		Comparator_B output (on TA0 clock input)
	PM_TA0CLK	TA0 clock input	-
2 (1)	PM_CBOUT1	-	Comparator_B output (on TA1 clock input)
	PM_TA1CLK	TA1 clock input	-
3	PM_ACLK	None	ACLK output
4	PM_MCLK	None	MCLK output
5	PM_SMCLK	None	SMCLK output
6	PM_RTCCLK	None	RTCCLK output
7 (1)	PM_ADC12CLK	-	ADC12CLK output
	PM_DMAE0	DMA external trigger input	-
8	PM_SVMOUT	None	SVM output
9	PM_TA0CCR0A	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
10	PM_TA0CCR1A	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
11	PM_TA0CCR2A	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
12	PM_TA0CCR3A	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
13	PM_TA0CCR4A	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
14	PM_TA1CCR0A	TA1 CCR0 capture input CCI0A	TA1 CCR0 compare output Out0
15	PM_TA1CCR1A	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
16	PM_TA1CCR2A	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
17 (2)	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI - input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
18 (2)	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI - output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
19 (3)	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI - input)	
20 (4)	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I2C clock (open drain and direction controlled by USCI)	
21 (4)	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I2C data (open drain and direction controlled by USCI)	
22 (5)	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI - input)	
23	PM_RFGDO0	Radio GDO0 (direction controlled by Radio)	
24	PM_RFGDO1	Radio GDO1 (direction controlled by Radio)	
25	PM_RFGDO2	Radio GDO2 (direction controlled by Radio)	
26	Reserved	None	DVSS

(1) Input or output function is selected by the corresponding setting in the port direction register PxDIR.
(2) UART or SPI functionality is determined by the selected USCI mode.
(3) UCA0CLK function takes precedence over UCB0STE function. If the mapped pin is required as UCA0CLK input or output USCI_B0 will be forced to 3-wire SPI mode even if 4-wire mode is selected.
(4) SPI or I2C functionality is determined by the selected USCI mode. In case the I2C functionality is selected the output of the mapped pin drives only the logical 0 to V_{SS} level.
(5) UCB0CLK function takes precedence over UCA0STE function. If the mapped pin is required as UCB0CLK input or output USCI_A0 will be forced to 3-wire SPI mode even if 4-wire mode is selected.

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Table 9. Port Mapping, Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION (PxDIR.y = 0)	OUTPUT PIN FUNCTION (PxDIR.y = 1)
27	Reserved	None	DVSS
28	Reserved	None	DVSS
29	Reserved	None	DVSS
30	Reserved	None	DVSS
31 (0FFh) (6)	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(6) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

Table 10. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION (PxDIR.y = 0)	OUTPUT PIN FUNCTION (PxDIR.y = 1)
P1.0/P1MAP0	PM_RFGDO0	None	Radio GDO0
P1.1/P1MAP1	PM_RFGDO2	None	Radio GDO2
P1.2/P1MAP2	PM_UCB0SOMI/PM_UCB0SCL	USCI_B0 SPI slave out master in (direction controlled by USCI), USCI_B0 I2C clock (open drain and direction controlled by USCI)	
P1.3/P1MAP3	PM_UCB0SIMO/PM_UCB0SDA	USCI_B0 SPI slave in master out (direction controlled by USCI), USCI_B0 I2C data (open drain and direction controlled by USCI)	
P1.4/P1MAP4	PM_UCB0CLK/PM_UCA0STE	USCI_B0 clock input/output (direction controlled by USCI), USCI_A0 SPI slave transmit enable (direction controlled by USCI - input)	
P1.5/P1MAP5	PM_UCA0RXD/PM_UCA0SOMI	USCI_A0 UART RXD (Direction controlled by USCI - input), USCI_A0 SPI slave out master in (direction controlled by USCI)	
P1.6/P1MAP6	PM_UCA0TXD/PM_UCA0SIMO	USCI_A0 UART TXD (Direction controlled by USCI - output), USCI_A0 SPI slave in master out (direction controlled by USCI)	
P1.7/P1MAP7	PM_UCA0CLK/PM_UCB0STE	USCI_A0 clock input/output (direction controlled by USCI), USCI_B0 SPI slave transmit enable (direction controlled by USCI - input)	
P2.0/P2MAP0	PM_CBOUT1/PM_TA1CLK	TA1 clock input	Comparator_B output
P2.1/P2MAP1	PM_TA1CCR0A	TA1 CCR0 capture input CCI0A	TA1 CCR0 compare output Out0
P2.2/P2MAP2	PM_TA1CCR1A	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
P2.3/P2MAP3	PM_TA1CCR2A	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
P2.4/P2MAP4	PM_RTCCLK	None	RTCCLK output
P2.5/P2MAP5	PM_SVMOUT	None	SVM output
P2.6/P2MAP6	PM_ACLK	None	ACLK output
P2.7/P2MAP7	PM_ADC12CLK/PM_DMAE0	DMA external trigger input	ADC12CLK output
P3.0/P3MAP0	PM_CBOUT0/PM_TA0CLK	TA0 clock input	Comparator_B output
P3.1/P3MAP1	PM_TA0CCR0A	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
P3.2/P3MAP2	PM_TA0CCR1A	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
P3.3/P3MAP3	PM_TA0CCR2A	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
P3.4/P3MAP4	PM_TA0CCR3A	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
P3.5/P3MAP5	PM_TA0CCR4A	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
P3.6/P3MAP6	PM_RFGDO1	None	Radio GDO1
P3.7/P3MAP7	PM_SMCLK	None	SMCLK output

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System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 11. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RST/NMI (POR)	04h	
		DoBOR (BOR)	06h	
		Reserved	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		DoPOR (POR)	14h	
		WDT timeout (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		DLYLIFG	06h	
		DLYHIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		VLRLIFG	10h	
		VLRHIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h to 1Eh	Lowest

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DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 12. DMA Trigger Assignments(1)

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	Reserved	Reserved	Reserved
6	Reserved	Reserved	Reserved
7	Reserved	Reserved	Reserved
8	Reserved	Reserved	Reserved
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	Reserved	Reserved	Reserved
21	Reserved	Reserved	Reserved
22	Reserved	Reserved	Reserved
23	Reserved	Reserved	Reserved
24	ADC12IFGx(2)	ADC12IFGx(2)	ADC12IFGx(2)
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers will not cause any DMA trigger event when selected.
(2) Only on CC430F613x and CC430F513x. Reserved on CC430F612x.

Watchdog Timer (WDT_A)

The primary function of the watchdog timer is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

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CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

AES128 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

Universal Serial Communication Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The USCI_Bn module provides support for SPI (3 or 4 pin) and I2C.

A USCI_A0 and USCI_B0 module are implemented.

TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 13. TA0 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
PM_TA0CLK	TACLK	Timer	NA	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
RFCLK/192 (1)	INCLK			
PM_TA0CCR0A	CCI0A	CCR0	TA0	PM_TA0CCR0A
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
PM_TA0CCR1A	CCI1A	CCR1	TA1	PM_TA0CCR1A
CBOUT (internal)	CCI1B			ADC12 (internal) (2) ADC12SHSx = {1}
DV_{SS}	GND			
DV_{CC}	V_{CC}			
PM_TA0CCR2A	CCI2A	CCR2	TA2	PM_TA0CCR2A
ACLK (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
PM_TA0CCR3A	CCI3A	CCR3	TA3	PM_TA0CCR3A
GDO1 from Radio (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
PM_TA0CCR4A	CCI4A	CCR4	TA4	PM_TA0CCR4A
GDO2 from Radio (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

(1) If a different RFCLK divider setting is selected for a radio GDO output, this divider setting is also used for the Timer_A INCLK.
(2) Only on CC430F613x and CC430F513x

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TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing. TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 14. TA1 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
				PZ
PM_TA1CLK	TACLK	Timer	NA	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
RFCLK/192[(1)]	INCLK			
PM_TA1CCR0A	CCI0A	CCR0	TA0	PM_TA1CCR0A
RF Async. Output (internal)	CCI0B			RF Async. Input (internal)
DV_{SS}	GND			
DV_{CC}	V_{CC}			
PM_TA1CCR1A	CCI1A	CCR1	TA1	PM_TA1CCR1A
CBOUT (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
PM_TA1CCR2A	CCI2A	CCR2	TA2	PM_TA1CCR2A
ACLK (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

(1) If a different RFCLK divider setting is selected for a radio GDO output, this divider setting is also used for the Timer_A INCLK.

Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

REF Voltage Reference

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC12_A, LCD_B, and COMP_B modules.

LCD_B (Only CC430F613x and CC430F612x)

The LCD_B driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_B controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments.

Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

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ADC12_A (Only CC430F613x and CC430F513x)

The ADC12_A module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

Embedded Emulation Module (EEM) (S Version)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

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Peripheral File Map

Table 15. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 16)	0100h	000h-01Fh
PMM (see Table 17)	0120h	000h-00Fh
Flash Control (see Table 18)	0140h	000h-00Fh
CRC16 (see Table 19)	0150h	000h-007h
RAM Control (see Table 20)	0158h	000h-001h
Watchdog (see Table 21)	015Ch	000h-001h
UCS (see Table 22)	0160h	000h-01Fh
SYS (see Table 23)	0180h	000h-01Fh
Shared Reference (see Table 24)	01B0h	000h-001h
Port Mapping Control (see Table 25)	01C0h	000h-007h
Port Mapping Port P1 (see Table 26)	01C8h	000h-007h
Port Mapping Port P2 (see Table 27)	01D0h	000h-007h
Port Mapping Port P3 (see Table 28)	01D8h	000h-007h
Port P1, P2 (see Table 29)	0200h	000h-01Fh
Port P3, P4 (see Table 30) (P4 not available on CC430F513x)	0220h	000h-01Fh
Port P5 (see Table 31)	0240h	000h-01Fh
Port PJ (see Table 32)	0320h	000h-01Fh
TA0 (see Table 33)	0340h	000h-03Fh
TA1 (see Table 34)	0380h	000h-03Fh
RTC_A (see Table 35)	04A0h	000h-01Fh
32-Bit Hardware Multiplier (see Table 36)	04C0h	000h-02Fh
DMA Module Control (see Table 37)	0500h	000h-00Fh
DMA Channel 0 (see Table 38)	0510h	000h-00Fh
DMA Channel 1 (see Table 39)	0520h	000h-00Fh
DMA Channel 2 (see Table 40)	0530h	000h-00Fh
USCI_A0 (see Table 41)	05C0h	000h-01Fh
USCI_B0 (see Table 42)	05E0h	000h-01Fh
ADC12 (see Table 43) (only CC430F613x and CC430F513x)	0700h	000h-03Fh
Comparator_B (see Table 44)	08C0h	000h-00Fh
AES Accelerator (see Table 45)	09C0h	000h-00Fh
LCD_B (see Table 46) (only CC430F613x and CC430F612x)	0A00h	000h-05Fh
Radio Interface (see Table 47)	0F00h	000h-03Fh

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Table 16. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 17. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 18. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 19. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC initialization and result	CRCINIRES	04h

Table 20. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 21. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 22. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

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Table 23. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 24. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 25. Port Mapping Control Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key register	PMAPKEYID	00h
Port mapping control register	PMAPCTL	02h

Table 26. Port Mapping Port P1 Registers (Base Address: 01C8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1.0 mapping register	P1MAP0	00h
Port P1.1 mapping register	P1MAP1	01h
Port P1.2 mapping register	P1MAP2	02h
Port P1.3 mapping register	P1MAP3	03h
Port P1.4 mapping register	P1MAP4	04h
Port P1.5 mapping register	P1MAP5	05h
Port P1.6 mapping register	P1MAP6	06h
Port P1.7 mapping register	P1MAP7	07h

Table 27. Port Mapping Port P2 Registers (Base Address: 01D0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2.0 mapping register	P2MAP0	00h
Port P2.1 mapping register	P2MAP1	01h
Port P2.2 mapping register	P2MAP2	02h
Port P2.3 mapping register	P2MAP3	03h
Port P2.4 mapping register	P2MAP4	04h
Port P2.5 mapping register	P2MAP5	05h
Port P2.6 mapping register	P2MAP6	06h
Port P2.7 mapping register	P2MAP7	07h

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Table 28. Port Mapping Port P3 Registers (Base Address: 01D8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3.0 mapping register	P3MAP0	00h
Port P3.1 mapping register	P3MAP1	01h
Port P3.2 mapping register	P3MAP2	02h
Port P3.3 mapping register	P3MAP3	03h
Port P3.4 mapping register	P3MAP4	04h
Port P3.5 mapping register	P3MAP5	05h
Port P3.6 mapping register	P3MAP6	06h
Port P3.7 mapping register	P3MAP7	07h

Table 29. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 30. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

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Table 31. Port P5 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah

Table 32. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 33. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 34. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

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Table 35. Real Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 36. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

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Table 37. DMA Module Control Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

Table 38. DMA Channel 0 Registers (Base Address: 0510h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah

Table 39. DMA Channel 1 Registers (Base Address: 0520h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah

Table 40. DMA Channel 2 Registers (Base Address: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah

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Table 41. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 42. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

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Table 43. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

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Table 44. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control register 0	CBCTL0	00h
Comp_B control register 1	CBCTL1	02h
Comp_B control register 2	CBCTL2	04h
Comp_B control register 3	CBCTL3	06h
Comp_B interrupt register	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 45. AES Accelerator Registers (Base Address: 09C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
AES accelerator control register 0	AESACTL0	00h
Reserved		02h
AES accelerator status register	AESASTAT	04h
AES accelerator key register	AESAKEY	06h
AES accelerator data in register	AESADIN	008h
AES accelerator data out register	AESADOUT	00Ah

Table 46. LCD_B Registers (Base Address: 0A00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD_B control register 0	LCDBCTL0	000h
LCD_B control register 1	LCDBCTL1	002h
LCD_B blinking control register	LCDBBLKCTL	004h
LCD_B memory control register	LCDBMEMCTL	006h
LCD_B voltage control register	LCDBVCTL	008h
LCD_B port control register 0	LCDBPCTL0	00Ah
LCD_B port control register 1	LCDBPCTL1	00Ch
LCD_B charge pump control register	LCDBCTL0	012h
LCD_B interrupt vector word	LCDBIV	01Eh
LCD_B memory 1	LCDM1	020h
LCD_B memory 2	LCDM2	021h
...		
LCD_B memory 14	LCDM14	02Dh
LCD_B blinking memory 1	LCDBM1	040h
LCD_B blinking memory 2	LCDBM2	041h
...		
LCD_B blinking memory 14	LCDBM14	04Dh

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Table 47. Radio Interface Registers (Base Address: 0F00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Radio interface control register 0	RF1AIFCTL0	00h
Radio interface control register 1	RF1AIFCTL1	02h
Radio interface error flag register	RF1AIFERR	06h
Radio interface error vector word	RF1AIFERRV	0Ch
Radio interface interrupt vector word	RF1AIFIV	0Eh
Radio instruction word register	RF1AINSTRW	10h
Radio instruction word register, 1-byte auto-read	RF1AINSTR1W	12h
Radio instruction word register, 2-byte auto-read	RF1AINSTR2W	14h
Radio data in register	RF1ADINW	16h
Radio status word register	RF1ASTATW	20h
Radio status word register, 1-byte auto-read	RF1ASTAT1W	22h
Radio status word register, 2-byte auto-read	RF1AISTAT2W	24h
Radio data out register	RF1ADOUTW	28h
Radio data out register, 1-byte auto-read	RF1ADOUT1W	2Ah
Radio data out register, 2-byte auto-read	RF1ADOUT2W	2Ch
Radio core signal input register	RF1AIN	30h
Radio core interrupt flag register	RF1AIFG	32h
Radio core interrupt edge select register	RF1AIES	34h
Radio core interrupt enable register	RF1AIE	36h
Radio core interrupt vector word	RF1AIV	38h

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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE, RF_P, RF_N, and R_BIAS)[2]	–0.3 V to (V_{CC} + 0.3 V), 4.1 V Max
Voltage applied to VCORE, RF_P, RF_N, and R_BIAS[2]	–0.3 V to 2.0 V
Input RF level at pins RF_P and RF_N	10 dBm
Diode current at any device terminal	±2 mA
Storage temperature range[3], T_{stg}	–55°C to 150°C
Maximum junction temperature, T_J	95°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Thermal Packaging Characteristics CC430F51xx

θ_{JA}	Junction-to-ambient thermal resistance, still air	Low-K board	48 QFN (RGZ)	98°C/W
		High-K board	48 QFN (RGZ)	28°C/W

Thermal Packaging Characteristics CC430F61xx

θ_{JA}	Junction-to-ambient thermal resistance, still air	Low-K board	64 QFN (RGC)	83°C/W
		High-K board	64 QFN (RGC)	26°C/W

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins[1] during program execution and flash programming with PMM default settings, Radio is not operational with PMMCOREVx = 0 or 1[2][3]	PMMCOREVx = 0 (default after POR)	1.8		3.6	V
		PMMCOREVx = 1	2.0		3.6	
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins[1] during program execution, flash programming, and radio operation with PMM default settings[2][3]	PMMCOREVx = 2	2.2		3.6	V
		PMMCOREVx = 3	2.4		3.6	
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins[1] during program execution, flash programming and radio operation with PMMCOREVx = 2, high-side SVS level lowered (SVSHRVL = SVSMHRRL = 1) or high-side SVS disabled (SVSHE = 0)[2][3][4]	PMMCOREVx = 2, SVSHRVLx = SVSHRRRLx = 1 or SVSHE = 0	2.0		3.6	V
V_{SS}	Supply voltage applied at the exposed die attach VSS and AVSS pin			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{VCORE}	Recommended capacitor at VCORE[5]			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of capacitor at DVCC to capacitor at VCORE		10			

(1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the PMM, SVS High Side threshold parameters for the exact values and further details.
(4) Lowering the high-side SVS level or disabling the high-side SVS might cause the LDO to operate out of regulation, but the core voltage will still stay within its limits and is still supervised by the low-side SVS ensuring reliable operation.
(5) A capacitor tolerance of ±20% or better is required.

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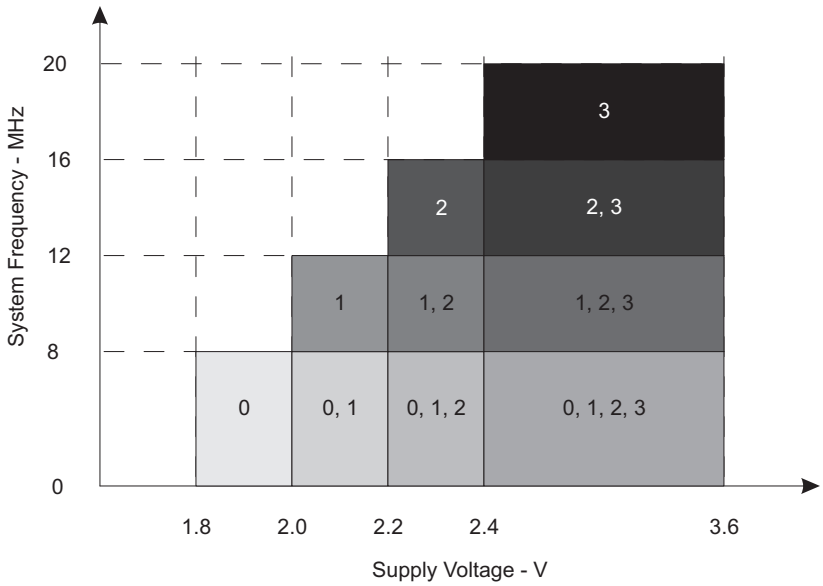
Recommended Operating Conditions (continued)

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SYSTEM}	Processor (MCLK) frequency(6) (see Figure 2)	PMMCOREVx = 0 (default condition)	0		8	MHz
		PMMCOREVx = 1	0		12	
		PMMCOREVx = 2	0		16	
		PMMCOREVx = 3	0		20	
P_{INT}	Internal power dissipation		$V_{CC} \times I_{(DVCC)}$			W
P_{IO}	I/O power dissipation of I/O pins powered by DVCC		$(V_{CC} - V_{IOH}) \times I_{IOH} + V_{IOL} \times I_{IOL}$			W
P_{MAX}	Maximum allowed power dissipation, $P_{MAX} > P_{IO} + P_{INT}$		$(T_J - T_A) / \theta_{JA}$			W

(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 2. Maximum System Frequency

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		16 MHz		20 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM,\ Flash}$(4)	Flash	3.0 V	0	0.23	0.26	1.35	1.60							mA
			1	0.25	0.28	1.55		2.30	2.65					
			2	0.27	0.30	1.75		2.60		3.45	3.90			
			3	0.28	0.32	1.85		2.75		3.65		4.55	5.10	
$I_{AM,\ RAM}$(5)	RAM	3.0 V	0	0.18	0.20	0.95	1.10							mA
			1	0.20	0.22	1.10		1.60	1.85					
			2	0.21	0.24	1.20		1.80		2.40	2.70			
			3	0.22	0.25	1.30		1.90		2.50		3.10	3.60	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.
(4) Active mode supply current when program executes in flash at a nominal supply voltage of 3.0 V.
(5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3.0 V.

Typical Characteristics - Active Mode Supply Currents

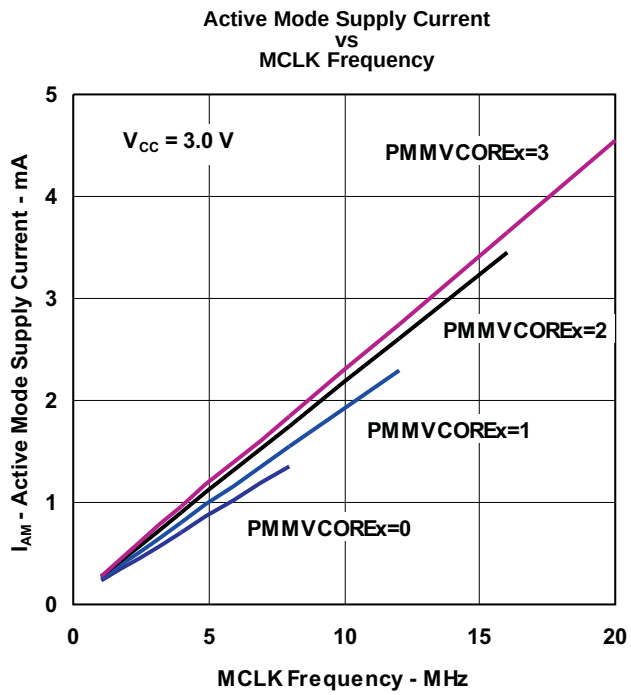


Figure 3.

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Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	Temperature (T_A)								UNIT
				-40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3) (4)	2.2 V	0	80	100	80	100	80	100	80	100	µA
		3.0 V	3	90	110	90	110	90	110	90	110	
I_{LPM2}	Low-power mode 2(5) (4)	2.2 V	0	6.5	11	6.5	11	6.5	11	6.5	11	µA
		3.0 V	3	7.5	12	7.5	12	7.5	12	7.5	12	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6) (4)	3.0 V	0	1.8		2.0	2.6	3.0	4.0	4.4	5.9	µA
			1	1.9		2.1		3.2		4.8		
			2	2.0		2.2		3.4		5.1		
			3	2.0		2.2	2.9	3.5	4.8	5.3	7.4	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(7) (4)	3.0 V	0	0.9		1.1	2.3	2.1	3.7	3.5	5.6	µA
			1	1.0		1.2		2.3		3.9		
			2	1.1		1.3		2.5		4.2		
			3	1.1		1.3	2.6	2.6	4.5	4.4	7.1	
I_{LPM4}	Low-power mode 4(8) (4)	3.0 V	0	0.8		1.0	2.2	2.0	3.6	3.4	5.5	µA
			1	0.9		1.1		2.2		3.8		
			2	1.0		1.2		2.4		4.1		
			3	1.0		1.2	2.5	2.5	4.4	4.3	7.0	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
(4) Current for brownout, high side supervisor (SVS_H) normal mode included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

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Typical Characteristics - Low-Power Mode Supply Currents

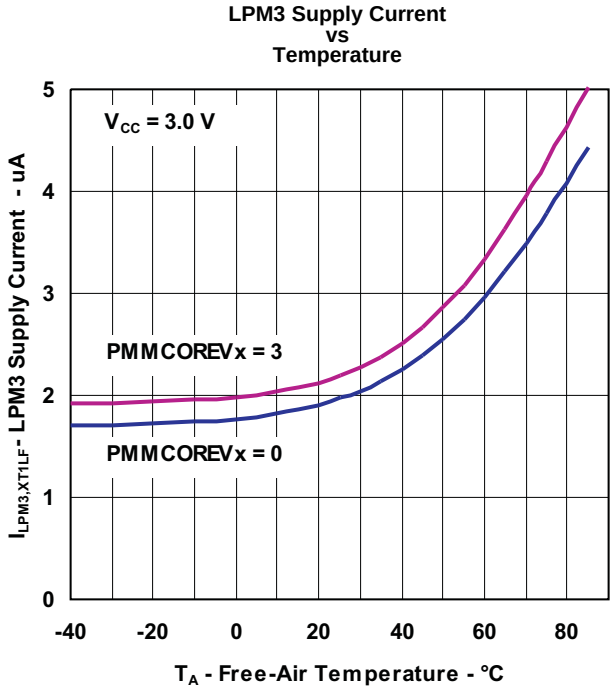

Figure 4.

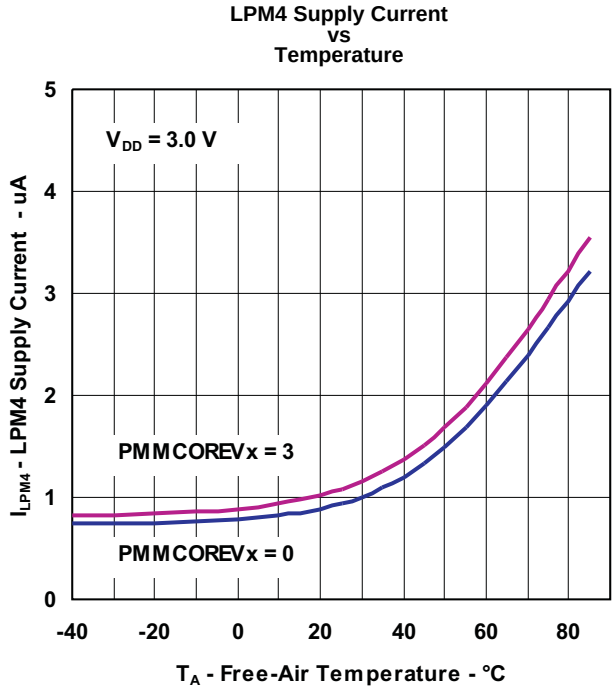

Figure 5.

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Low-Power Mode with LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	Temperature (T_A)								UNIT
				-40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM3} LCD, ext. bias	Low-power mode 3 (LPM3) current, LCD 4-mux mode, external biasing(3) (4)	3.0 V	0	2.2		2.4		3.5		4.9		µA
			1	2.3		2.5		3.7		5.3		
			2	2.4		2.6		3.9		5.6		
			3	2.4		2.6		4.0		5.8		
I_{LPM3} LCD, int. bias	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled(3) (5)	3.0 V	0	3.1		3.3	4.0	4.3		5.8	7.4	µA
			1	3.2		3.4		4.5		6.2		
			2	3.3		3.5		4.7		6.5		
			3	3.3		3.5	4.3	4.8		6.7	8.9	
I_{LPM3} LCD,CP	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled(3) (6)	2.2 V	0			4.0						µA
			1			4.1						
			2			4.2						
		3.0 V	0			4.2						
			1			4.3						
			2			4.5						
			3			4.5						

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
Current for brownout, high side supervisor (SVS_H) normal mode included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.
(4) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL=0, LCDPREx=101, LCDDIVx=00011 (f_{LCD} = 32768 Hz/32/4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0, S2,...=0, odd segments S1, S3,...=1. No LCD panel load.
(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL=0, LCDPREx=101, LCDDIVx=00011 (f_{LCD} = 32768 Hz/32/4 = 256 Hz)
Even segments S0, S2,...=0, odd segments S1, S3,...=1. No LCD panel load.
(6) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 (V_{LCD}= 3 V typ.), LCDSSEL=0, LCDPREx=101, LCDDIVx=00011 (f_{LCD} = 32768 Hz/32/4 = 256 Hz)
Even segments S0, S2,...=0, odd segments S1, S3,...=1. No LCD panel load.

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Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	1.8 V, 3 V			±50	nA
$t_{(int)}$	External interrupt timing (External trigger pulse duration to set interrupt flag)(3)	Ports with interrupt capability (see block diagram and terminal function descriptions).	1.8 V, 3 V	20			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

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Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage, Reduced Drive Strength(1)	$I_{(OHmax)}$ = –1 mA, PxDS.y = 0(2)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA, PxDS.y = 0(3)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA, PxDS.y = 0(2)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA, PxDS.y = 0(3)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage, Reduced Drive Strength(1)	$I_{(OLmax)}$ = 1 mA, PxDS.y = 0(2)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA, PxDS.y = 0(3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA, PxDS.y = 0(2)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA, PxDS.y = 0(3)		V_{SS}	V_{SS} + 0.60	
V_{OH}	High-level output voltage, Full Drive Strength	$I_{(OHmax)}$ = –3 mA, PxDS.y = 1(2)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA, PxDS.y = 1(3)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA, PxDS.y = 1(2)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA, PxDS.y = 1(3)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage, Full Drive Strength	$I_{(OLmax)}$ = 3 mA, PxDS.y = 1(2)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA, PxDS.y = 1(3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA, PxDS.y = 1(2)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA, PxDS.y = 1(3)		V_{SS}	V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with load)	C_L = 20 pF, R_L (4) (5)	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 2		25	
f_{Port_CLK}	Clock output frequency	C_L = 20 pF(5)	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 2		25	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(4) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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Typical Characteristics - Outputs, Reduced Drive Strength (PxDS.y = 0)

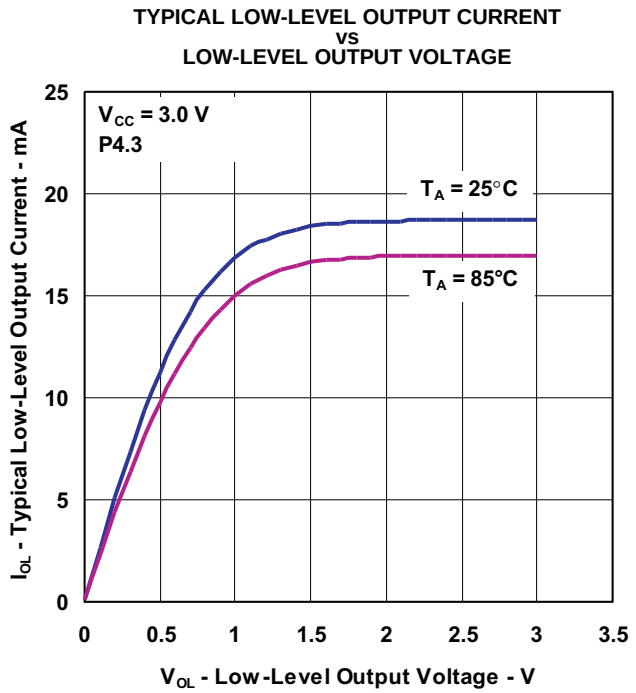

Figure 6.

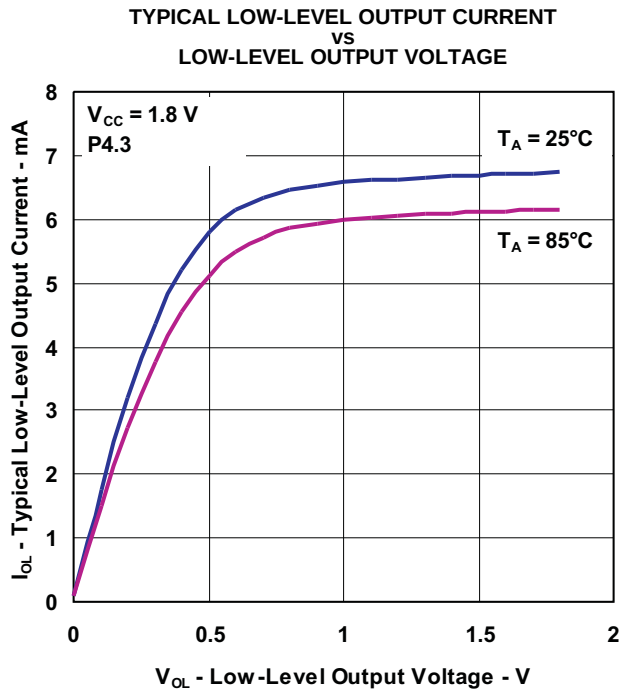

Figure 7.

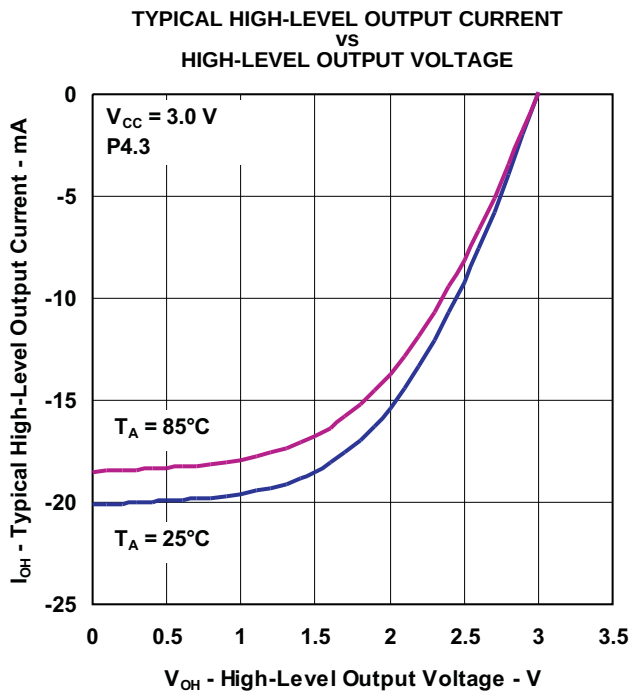

Figure 8.

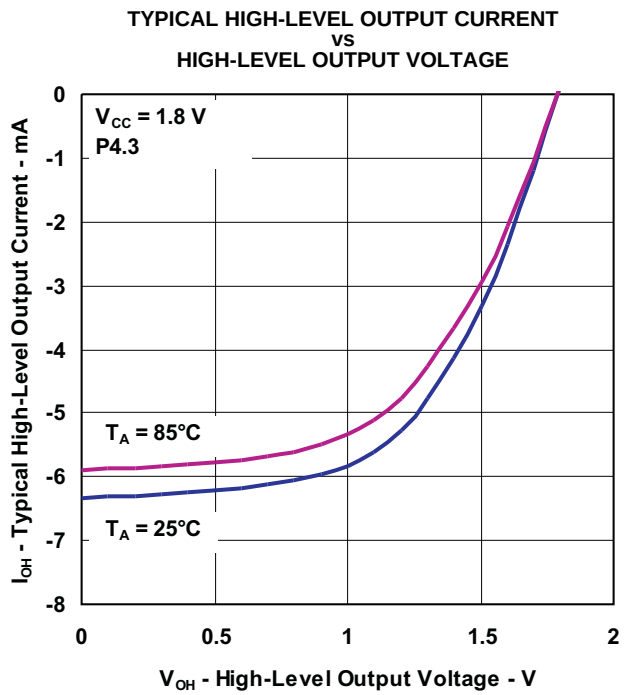

Figure 9.

Typical Characteristics - Outputs, Full Drive Strength (PxDS.y = 1)

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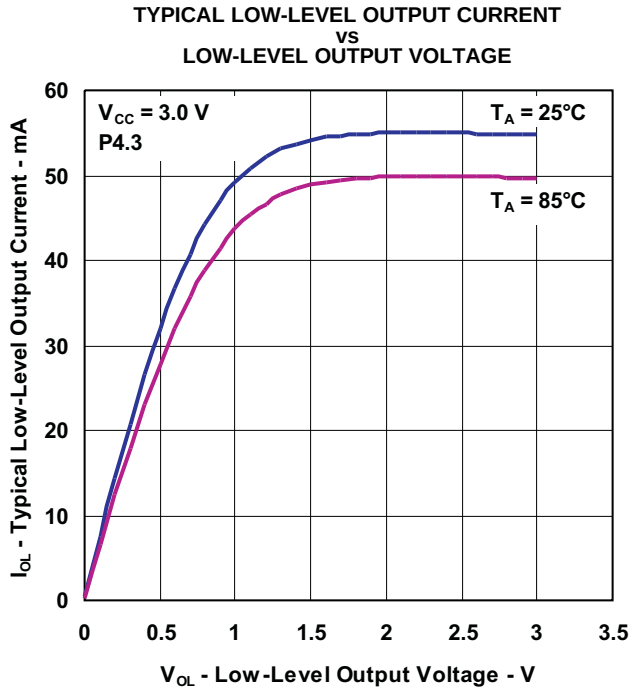

Figure 10.

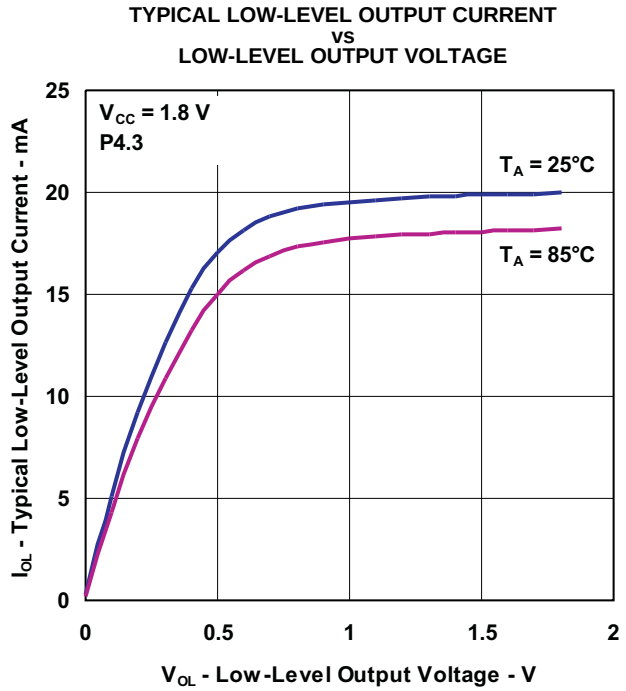

Figure 11.

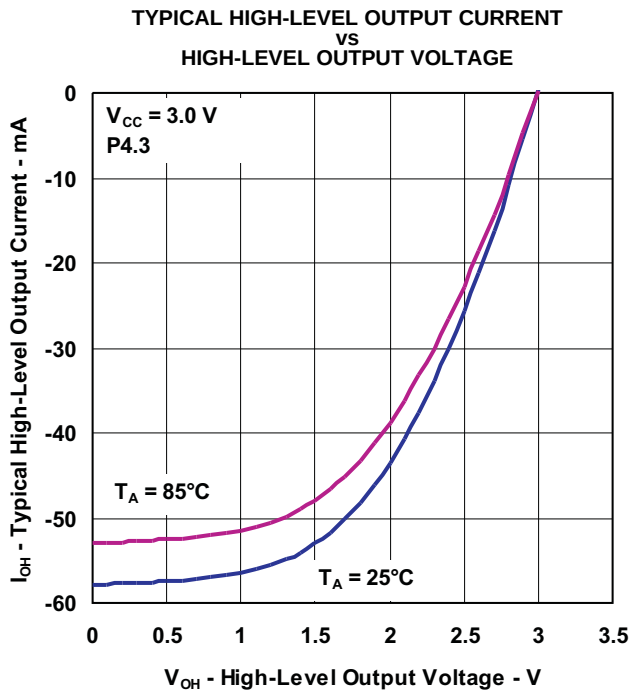

Figure 12.

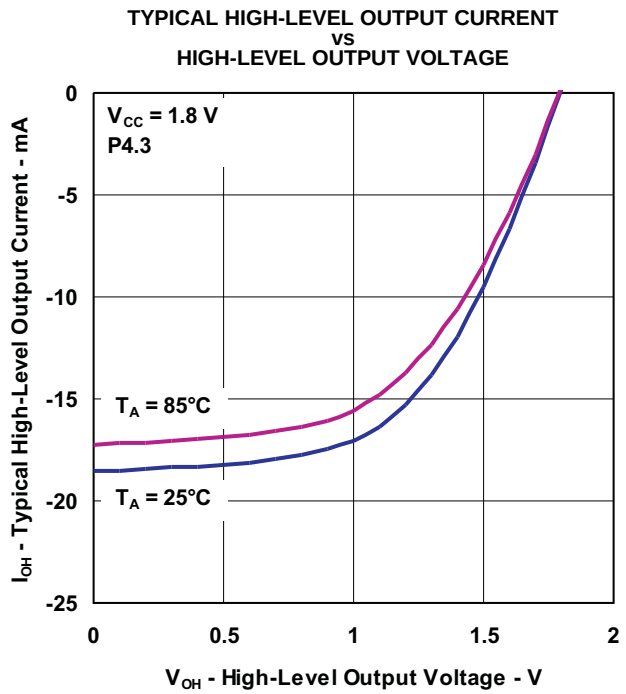

Figure 13.

Crystal Oscillator, XT1, Low-Frequency Mode[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3.0 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1[2] [3]		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals[4]	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode[5]	XTS = 0, XCAPx = 0[6]			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode[7]	XTS = 0[8]		10		10000	Hz
$t_{START,LF}$	Startup time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3.0 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  (a) Keep the trace between the device and the crystal as short as possible.
  (b) Design a good ground plane around the oscillator pins.
  (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  (e) Use assembly materials and techniques that avoid any parasitic load on the oscillator XIN and XOUT pins.
  (f) If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  (a) For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF
  (b) For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le$ 9 pF
  (c) For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le$ 10 pF
  (d) For XT1DRIVEx = 3, $C_{L,eff} \ge 6$ pF
(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
  Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag
(8) Measured with logic-level input frequency but also applies to operation with crystals.

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Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK (1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK (2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5	%
		T_A = 25°C	3 V			±1.5	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK (1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK (2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t_{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

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DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40	50	60	%
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n,\ 0),MAX} \le f_{DCO} \le f_{DCO(n,\ 31),MIN}$, where $f_{DCO(n,\ 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

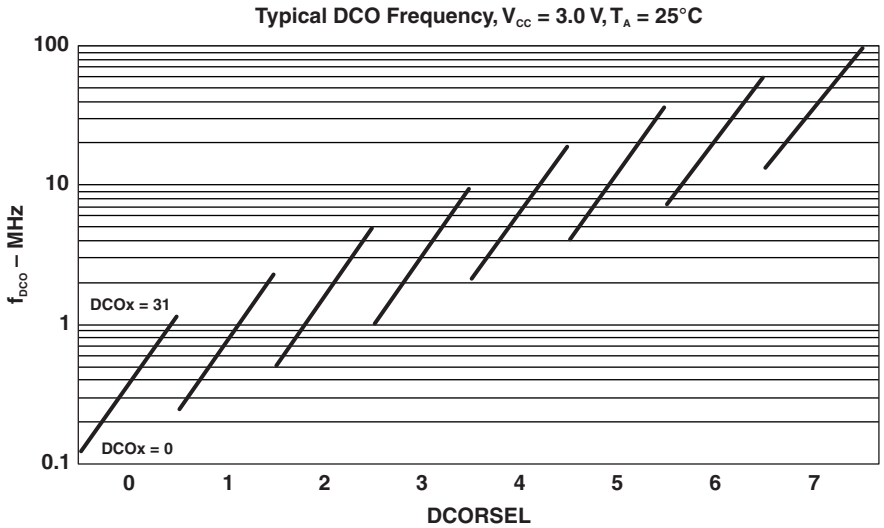

Figure 14. Typical DCO frequency

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PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(DV_{CC}_BOR_IT–)$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s			1.45	V
$V(DV_{CC}_BOR_IT+)$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s	0.80	1.30	1.50	V
$V(DV_{CC}_BOR_hys)$	BOR_H hysteresis		60		250	mV
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CORE3}(AM)$	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.90		V
$V_{CORE2}(AM)$	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.80		V
$V_{CORE1}(AM)$	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.60		V
$V_{CORE0}(AM)$	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.40		V
$V_{CORE3}(LPM)$	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.94		V
$V_{CORE2}(LPM)$	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.84		V
$V_{CORE1}(LPM)$	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.64		V
$V_{CORE0}(LPM)$	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.44		V

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
$V_{(SVSH_IT–)}$	SVS_H on voltage level (1)	SVSHE = 1, SVSHRVL = 0	1.53	1.60	1.67	V
		SVSHE = 1, SVSHRVL = 1	1.73	1.80	1.87	V
		SVSHE = 1, SVSHRVL = 2	1.93	2.00	2.07	V
		SVSHE = 1, SVSHRVL = 3	2.03	2.10	2.17	V
$V_{(SVSH_IT+)}$	SVS_H off voltage level (1)	SVSHE = 1, SVSMHRRL = 0	1.60	1.70	1.80	V
		SVSHE = 1, SVSMHRRL = 1	1.80	1.90	2.00	V
		SVSHE = 1, SVSMHRRL = 2	2.00	2.10	2.20	V
		SVSHE = 1, SVSMHRRL = 3	2.10	2.20	2.30	V
		SVSHE = 1, SVSMHRRL = 4	2.25	2.35	2.50	V
		SVSHE = 1, SVSMHRRL = 5	2.52	2.65	2.78	V
		SVSHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	V
		SVSHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	V
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		µs
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0 → 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		100		µs
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide* (SLAU259) on recommended settings and usage.

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PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE= 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
$V_{(SVMH)}$	SVM_H on or off voltage level(1)	SVMHE = 1, SVSMHRRL = 0	1.60	1.70	1.80	V
		SVMHE = 1, SVSMHRRL = 1	1.80	1.90	2.00	
		SVMHE = 1, SVSMHRRL = 2	2.00	2.10	2.20	
		SVMHE = 1, SVSMHRRL = 3	2.10	2.20	2.30	
		SVMHE = 1, SVSMHRRL = 4	2.25	2.35	2.50	
		SVMHE = 1, SVSMHRRL = 5	2.52	2.65	2.78	
		SVMHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0 → 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide* (SLAU259) on recommended settings and usage.

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PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		100		

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		100		

Wake Up From Low Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	f_{MCLK} ≥ 4.0 MHz			5	µs
			f_{MCLK} < 4.0 MHz			6	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode(2)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	165	µs
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode(3)				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wake-up times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide* (SLAU259).

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide* (SLAU259).

(3) This value represents the time from the wake-up event to the reset vector execution.

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Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK, External: TACLK, Duty cycle = 50% ± 10%	1.8 V, 3 V			25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture.	1.8 V, 3 V	20			ns

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USCI (UART Mode) Recommended Operating Conditions

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					1	MHz

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_τ	UART receive deglitch time (1)		2.2 V	50		600	ns
			3 V	50		600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode) Recommended Operating Conditions

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Note (1), Figure 15 and Figure 16)

PARAMETER		TEST CONDITIONS	PMMCOREVx	V_{CC}	MIN	TYP	MAX	UNIT
$t_{SU,MI}$	SOMI input data setup time		0	1.8 V	55			ns
				3.0 V	38			
			3	2.4 V	30			ns
				3.0 V	25			
$t_{HD,MI}$	SOMI input data hold time		0	1.8 V	0			ns
				3.0 V	0			
			3	2.4 V	0			ns
				3.0 V	0			
$t_{VALID,MO}$	SIMO output data valid time (2)	UCLK edge to SIMO valid, C_L = 20 pF	0	1.8 V			20	ns
				3.0 V			18	
			3	2.4 V			16	ns
				3.0 V			15	
$t_{HD,MO}$	SIMO output data hold time (3)	C_L = 20 pF	0	1.8 V	-10			ns
				3.0 V	-8			
			3	2.4 V	-10			ns
				3.0 V	-8			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 15 and Figure 16.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 15 and Figure 16.

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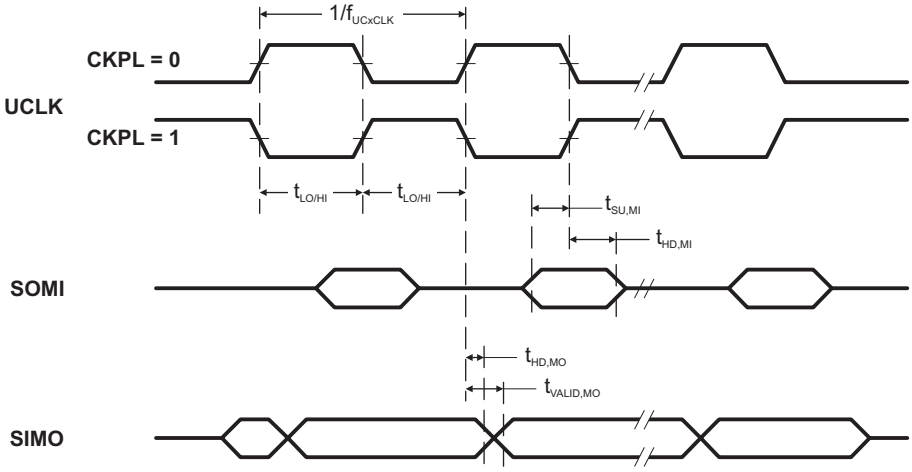

Figure 15. SPI Master Mode, CKPH = 0

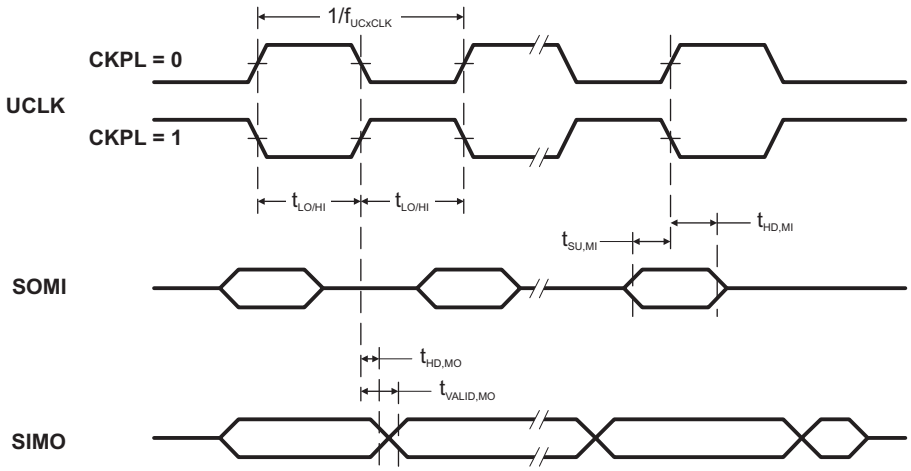

Figure 16. SPI Master Mode, CKPH = 1

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USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Note (1), Figure 17 and Figure 18)

PARAMETER		TEST CONDITIONS	PMMCOREVx	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		0	1.8 V	11			ns
				3.0 V	8			
			3	2.4 V	7			
				3.0 V	6			
$t_{STE,LAG}$	STE lag time, Last clock to STE high		0	1.8 V	3			ns
				3.0 V	3			
			3	2.4 V	3			
				3.0 V	3			
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		0	1.8 V			66	ns
				3.0 V			50	
			3	2.4 V			36	
				3.0 V			30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		0	1.8 V			30	ns
				3.0 V			23	
			3	2.4 V			16	
				3.0 V			13	
$t_{SU,SI}$	SIMO input data setup time		0	1.8 V	5			ns
				3.0 V	5			
			3	2.4 V	2			ns
				3.0 V	2			
$t_{HD,SI}$	SIMO input data hold time		0	1.8 V	5			ns
				3.0 V	5			
			3	2.4 V	5			ns
				3.0 V	5			
$t_{VALID,SO}$	SOMI output data valid time (2)	UCLK edge to SOMI valid, C_L = 20 pF	0	1.8 V			76	ns
				3.0 V			60	
			3	2.4 V			44	ns
				3.0 V			40	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	0	1.8 V	18			ns
				3.0 V	12			
			3	2.4 V	10			ns
				3.0 V	8			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 15 and Figure 16.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 15 and Figure 16.

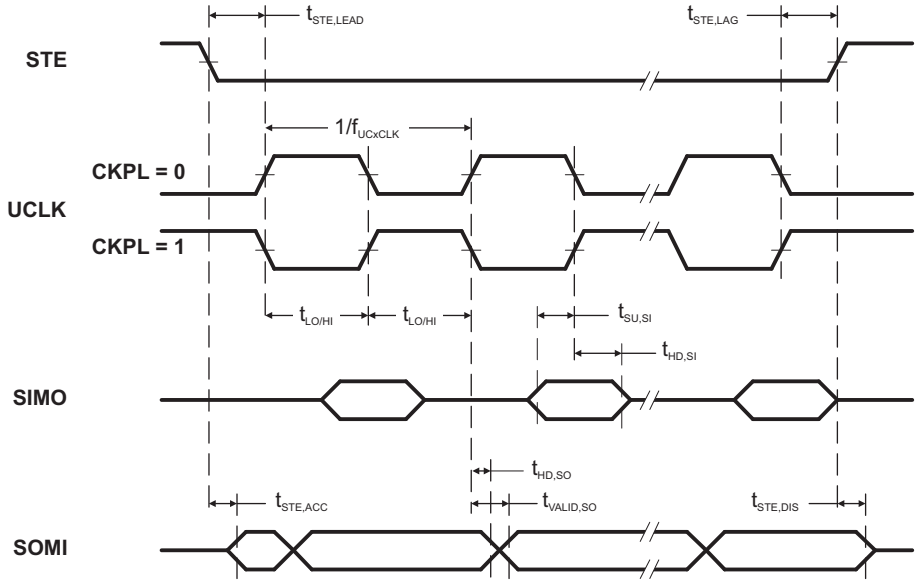

Figure 17. SPI Slave Mode, CKPH = 0

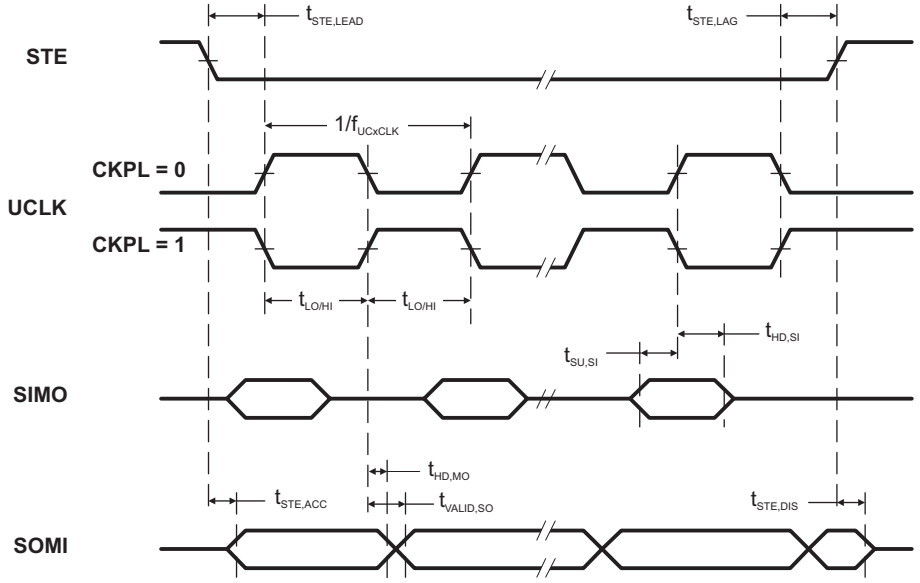

Figure 18. SPI Slave Mode, CKPH = 1

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USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50		600	ns
			3 V	50		600	

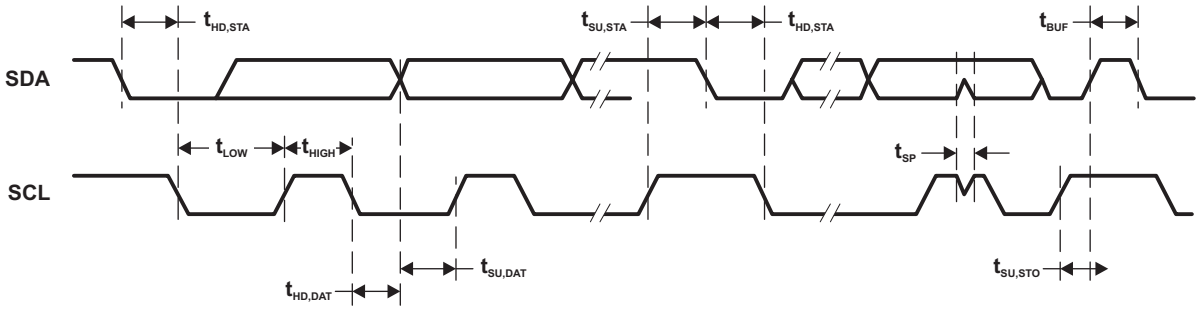

Figure 19. I2C Mode Timing

LCD_B Recommended Operating Conditions

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD_B,CP\ en,3.6}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.6 V	LCDCPEN = 1, 0000 < VLCDx ≤ 1111 (charge pump enabled, V_{LCD}≤ 3.6 V)	2.2		3.6	V
$V_{CC,LCD_B,CP\ en,3.3}$	Supply voltage range, charge pump enabled, V_{LCD}≤ 3.3 V	LCDCPEN = 1, 0000 < VLCDx ≤ 1100 (charge pump enabled, V_{LCD}≤ 3.3 V)	2.0		3.6	V
$V_{CC,LCD_B,int.\ bias}$	Supply voltage range, internal biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT=0	2.4		3.6	V
$V_{CC,LCD_B,ext.\ bias}$	Supply voltage range, external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT=0	2.4		3.6	V
$V_{CC,LCD_B,VLCDEXT}$	Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT=1	2.0		3.6	V
$V_{LCDCAP/R33}$	External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT=1	2.4		3.6	V
C_{LCDCAP}	Capacitor on LCDCAP when charge pump enabled	LCDCPEN = 1, VLCDx > 0000 (charge pump enabled)	4.7	4.7	10	µF
f_{Frame}	LCD frame frequency range	f_{LCD} = 2 × mux × f_{FRAME} with mux = 1 (static), 2, 3, 4	0		100	Hz
$f_{ACLK,in}$	ACLK input frequency range		30	32	40	kHz
C_{Panel}	Panel capacitance	100-Hz frame frequency			10000	pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, VLCDEXT=1	2.4		V_{CC}+0.2	V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R13}	V_{R03} + 2/3*(V_{R33} -V_{R03})	V_{R33}	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R03}	V_{R03} + 1/3*(V_{R33} -V_{R03})	V_{R23}	V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1	V_{R03}	V_{R03} + 1/2*(V_{R33} -V_{R03})	V_{R33}	V
V_{R03}	Analog input voltage at R03	R0EXT=1	V_{SS}			V
V_{LCD}-V_{R03}	Voltage difference between V_{LCD} and R03	LCDCPEN = 0, R0EXT=1	2.4		V_{CC}+0.2	V
$V_{LCDREF/R13}$	External LCD reference voltage applied at LCDREF/R13	VLCDREFx = 01	0.8	1.2	1.5	V

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LCD_B Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{LCD}	LCD voltage	VLCDx = 0000, VLCDEXT = 0	2.4 V to 3.6 V		V_{CC}		V
		LCDCPEN = 1, VLCDx = 0001	2.0 V to 3.6 V		2.54		V
		LCDCPEN = 1, VLCDx = 0010	2.0 V to 3.6 V		2.60		V
		LCDCPEN = 1, VLCDx = 0011	2.0 V to 3.6 V		2.66		V
		LCDCPEN = 1, VLCDx = 0100	2.0 V to 3.6 V		2.72		V
		LCDCPEN = 1, VLCDx = 0101	2.0 V to 3.6 V		2.78		V
		LCDCPEN = 1, VLCDx = 0110	2.0 V to 3.6 V		2.84		V
		LCDCPEN = 1, VLCDx = 0111	2.0 V to 3.6 V		2.90		V
		LCDCPEN = 1, VLCDx = 1000	2.0 V to 3.6 V		2.96		V
		LCDCPEN = 1, VLCDx = 1001	2.0 V to 3.6 V		3.02		V
		LCDCPEN = 1, VLCDx = 1010	2.0 V to 3.6 V		3.08		V
		LCDCPEN = 1, VLCDx = 1011	2.0 V to 3.6 V		3.14		V
		LCDCPEN = 1, VLCDx = 1100	2.0 V to 3.6 V		3.20		V
		LCDCPEN = 1, VLCDx = 1101	2.2 V to 3.6 V		3.26		V
		LCDCPEN = 1, VLCDx = 1110	2.2 V to 3.6 V		3.32		V
		LCDCPEN = 1, VLCDx = 1111	2.2 V to 3.6 V		3.38	3.6	V
$I_{CC,Peak,CP}$	Peak supply currents due to charge pump activities	LCDCPEN = 1, VLCDx = 1111	2.2 V		200		µA
$t_{LCD,CP,on}$	Time to charge C_{LCD} when discharged	C_{LCDCAP} = 4.7µF, LCDCPEN = 0→1, VLCDx = 1111	2.2 V		100	500	ms
$I_{CP,Load}$	Maximum charge pump load current	LCDCPEN = 1, VLCDx = 1111	2.2 V	50			µA
$R_{LCD,Seg}$	LCD driver output impedance, segment lines	LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ
$R_{LCD,COM}$	LCD driver output impedance, common lines	LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage, Full performance	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 analog input pins Ax		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AVCC terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		125	155	µA
			3 V		150	220	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON resistance	$0 V \le V_{Ax} \le AV_{CC}$		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See REF, External Reference and REF, Built-In Reference.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.

12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference.(1)	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference.(2)		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference.(3)		0.45	2.4	2.7	
$f_{ADC12OSC}$	Internal ADC12 oscillator(4)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12OSC}$ = 4.2 MHz to 5.4 MHz	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0			(5)		
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (6)	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) $13 \times ADC12DIV \times 1/f_{ADC12CLK}$
(6) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

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12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(1)	1.4 V ≤ dVREF ≤ 1.6 V(2)	2.2 V, 3 V			±2.0	LSB
		1.6 V < dVREF(2)				±1.7	
E_D	Differential linearity error(1)	(2)	2.2 V, 3 V			±1.0	LSB
E_O	Offset error(3)	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±1.0	±2.0	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.0	±2.0	
E_G	Gain error(3)	(2)	2.2 V, 3 V		±1.0	±2.0	LSB
E_T	Total unadjusted error	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±1.4	±3.5	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.4	±3.5	

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V_{R+} - V_{R-}, V_{R+} < AVCC, V_{R-} > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF+/VREF- to decouple the dynamic current. See also the *CC430 Family User's Guide* (SLAU259).
(3) Parameters are derived using a best fit curve.

12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V			±1.7	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±2.5	
E_D	Differential linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V	-1.0		+2.0	LSB
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 2.7 MHz		-1.0		+1.5	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz		-1.0		+2.5	
E_O	Offset error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.0	±2.0	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±1.0	±2.0	
E_G	Gain error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.0	±2.0	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1.5%(4)	VREF
E_T	Total unadjusted error	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.4	±3.5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1.5%(4)	VREF

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = V_{R+} - V_{R-}.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

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12-Bit ADC, Temperature Sensor and Built-In V_{MID} (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (2) (3)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		680		mV
			3 V		680		
TC_{SENSOR}	See (3)	ADC12ON = 1, INCH = 0Ah	2.2 V		2.25		mV/°C
			3 V		2.25		
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (4)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
V_{MID}	AV_{CC} divider at channel 11, V_{AVCC} factor	ADC12ON = 1, INCH = 0Bh		0.48	0.5	0.52	V_{AVCC}
	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh	2.2 V	1.06	1.1	1.14	V
			3 V	1.44	1.5	1.56	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns

(1) The temperature sensor is provided by the REF module. See the REF module parametric, I_{REF+}, regarding the current consumption of the temperature sensor.
(2) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(3) The device descriptor structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR}$ * (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

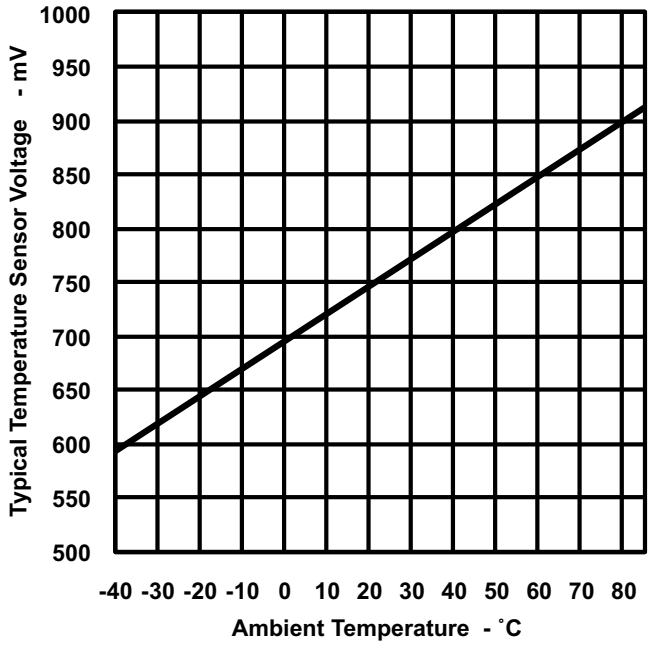

Figure 20. Typical Temperature Sensor Voltage

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REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ [2]		1.4		AV_{CC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ [3]		0		1.2	V
(V_{eREF+} – V_{REF-}/V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ [4]		1.4		AV_{CC}	V
I_{VeREF+} $I_{VREF-/VeREF-}$	Static input current	1.4 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz,ADC12SHTx = 1h, Conversion rate 200ksps	2.2 V, 3 V		±8.5	±26	µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz,ADC12SHTx = 8h, Conversion rate 20ksps	2.2 V, 3 V			±1	µA
$C_{VREF+/-}$	Capacitance at VREF+ or VREF- terminal, external reference[5]			10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *CC430 Family User's Guide* (SLAU259).

REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = 2 for 2.5 V, REFON = REFOUT = 1, I_{VREF+}= 0 A	3 V		2.41	±1.5%	V
		REFVSEL = 1 for 2.0 V, REFON = REFOUT = 1, I_{VREF+}= 0 A	3 V		1.93	±1.5%	
		REFVSEL = 0 for 1.5 V, REFON = REFOUT = 1, I_{VREF+}= 0 A	2.2 V, 3 V		1.45	±1.5%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = 0 for 1.5 V, reduced performance		1.8			V
		REFVSEL = 0 for 1.5 V		2.2			
		REFVSEL = 1 for 2.0 V		2.3			
		REFVSEL = 2 for 2.5 V		2.8			
I_{REF+}	Operating supply current into AVCC terminal[2][3]	REFON = 1, REFOUT = 0, REFBURST = 0	3 V		100	140	µA
		REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.9	1.5	mA
$I_{L(VREF+)}$	Load-current regulation, VREF+ terminal[4]	REFVSEL = 0, 1, or 2, I_{VREF+} = +10 µA or –1000 µA, AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1				2500	µV/mA
C_{VREF+}	Capacitance at VREF+ terminals, internal reference	REFON = REFOUT = 1		20		100	pF
TC_{REF+}	Temperature coefficient of built-in reference[5]	I_{VREF+} = 0 A, REFVSEL = 0, 1, or 2, REFON = 1, REFOUT = 0 or 1			30	50	ppm/ °C
PSRR_DC	Power supply rejection ratio (dc)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25 °C, REFVSEL = 0, 1, or 2, REFON = 1, REFOUT = 0 or 1			120	300	µV/V
PSRR_AC	Power supply rejection ratio (ac)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$ T_A = 25 °C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = 0, 1, or 2, REFON = 1, REFOUT = 0 or 1			6.4		mV/V
t_{SETTLE}	Settling time of reference voltage[6]	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, REFVSEL = 0, 1, or 2, REFOUT = 0, REFON = 0 → 1			75		µs
		AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, C_{VREF} = C_{VREF}(max), REFVSEL = 0, 1, or 2, REFOUT = 1, REFON = 0 → 1			75		

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal, as well as, used as the reference for the conversion and utilizes the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and utilizes the smaller buffer.
(2) The internal reference current is supplied from the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
(3) The temperature sensor is provided by the REF module. Its current is supplied from the AVCC terminal and is equivalent to I_{REF+} with REFON =1 and REFOUT = 0.
(4) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace or other causes.
(5) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C – (–40°C)).
(6) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

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Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00	1.8 V			40	µA
			2.2 V		30	50	
			3.0 V		40	65	
		CBPWRMD = 01	2.2 V, 3 V		10	30	
		CBPWRMD = 10	2.2 V, 3 V		0.1	0.5	
I_{AVCC_REF}	Quiescent current of local reference voltage amplifier into AVCC	CBREFACC = 1, CBREFLx = 01				22	µA
V_{IC}	Common mode input range			0		V_{CC}-1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01, 10				±10	mV
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	ON - switch closed			3	4	kΩ
		OFF - switch opened		30			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	ns
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.0	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	µs
t_{EN_CMP}	Comparator enable time, settling time	CBON = 0 to CBON = 1, CBPWRMD = 00, 01, 10			1	2	µs
t_{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			0.3	1.5	µs
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n+1) / 32			V

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Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DVCC during program			3	5	mA
I_{ERASE}	Average supply current from DVCC during erase			2	6.5	mA
I_{MERASE}, I_{BANK}	Average supply current from DVCC during mass erase or bank erase			2	6.5	mA
t_{CPT}	Cumulative program time(1)				16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
t_{Word}	Word or byte program time(2)		64		85	µs
$t_{Block, 0}$	Block program time for first byte or word(2)		49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word(2)		37		49	µs
$t_{Block, N}$	Block program time for last byte or word(2)		55		73	µs
t_{Erase}	Erase time for segment erase, mass erase, and bank erase when available(2)		23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word write, individual byte write, and block write modes.
(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency - 4-wire JTAG(2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface need to wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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RF1A CC1101-Based Radio Parameters

Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range during radio operation	2.0		3.6	V
PMMCOREVx	Core voltage range, PMMCOREVx setting during radio operation	2		3	
RF frequency range		300		348	MHz
		389 (1)		464	
		779		928	
Data rate	2-FSK	0.6		500	kBaud
	2-GFSK, OOK, and ASK	0.6		250	
	(Shaped) MSK (also known as differential offset QPSK) (2)	26		500	
RF crystal frequency		26	26	27	MHz
RF crystal tolerance	Total tolerance including initial tolerance, crystal loading, aging and temperature dependency. (3)		±40		ppm
RF crystal load capacitance		10	13	20	pF
RF crystal effective series resistance				100	Ω

(1) If using a 27-MHz crystal, the lower frequency limit for this band is 392 MHz.
(2) If using optional Manchester encoding, the data rate in kbps is half the baud rate.
(3) The acceptable crystal tolerance depends on frequency band, channel bandwidth, and spacing. Also see design note *DN005 -- CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy* (SWRA122).

RF Crystal Oscillator, XT2

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time (2)			150	810	µs
Duty cycle		45	50	55	%

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) The start-up time depends to a very large degree on the used crystal.

Current Consumption, Reduced-Power Modes

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption	RF crystal oscillator only (for example, SLEEP state with MCSM0.OSC_FORCE_ON = 1)		100		µA
	IDLE state (including RF crystal oscillator)		1.7		mA
	FSTXON state (only the frequency synthesizer is running) (2)		9.5		mA

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) This current consumption is also representative of other intermediate states when going from IDLE to RX or TX, including the calibration state.

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Current Consumption, Receive Mode

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1) (2)

PARAMETER	FREQ (MHz)	DATA RATE (kBaud)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current consumption, RX	315	1.2	Register settings optimized for reduced current	Input at -100 dBm (close to sensitivity limit)		17		mA
				Input at -40 dBm (well above sensitivity limit)		16		
		38.4		Input at -100 dBm (close to sensitivity limit)		17		
				Input at -40 dBm (well above sensitivity limit)		16		
		250		Input at -100 dBm (close to sensitivity limit)		18		
				Input at -40 dBm (well above sensitivity limit)		16.5		
	433	1.2	Register settings optimized for reduced current	Input at -100 dBm (close to sensitivity limit)		18		
				Input at -40 dBm (well above sensitivity limit)		17		
		38.4		Input at -100 dBm (close to sensitivity limit)		18		
				Input at -40 dBm (well above sensitivity limit)		17		
		250		Input at -100 dBm (close to sensitivity limit)		18.5		
				Input at -40 dBm (well above sensitivity limit)		17		
	868, 915	1.2	Register settings optimized for reduced current(3)	Input at -100 dBm (close to sensitivity limit)		16		
				Input at -40 dBm (well above sensitivity limit)		15		
		38.4		Input at -100 dBm (close to sensitivity limit)		16		
				Input at -40 dBm (well above sensitivity limit)		15		
		250		Input at -100 dBm (close to sensitivity limit)		16		
				Input at -40 dBm (well above sensitivity limit)		15		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) Reduced current setting (MDMCFG2.DEM_DCFILT_OFF = 1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See tables "RF Receive" for additional details on current consumption and sensitivity.
(3) For 868 or 915 MHz, see Figure 21 for current consumption with register settings optimized for sensitivity.

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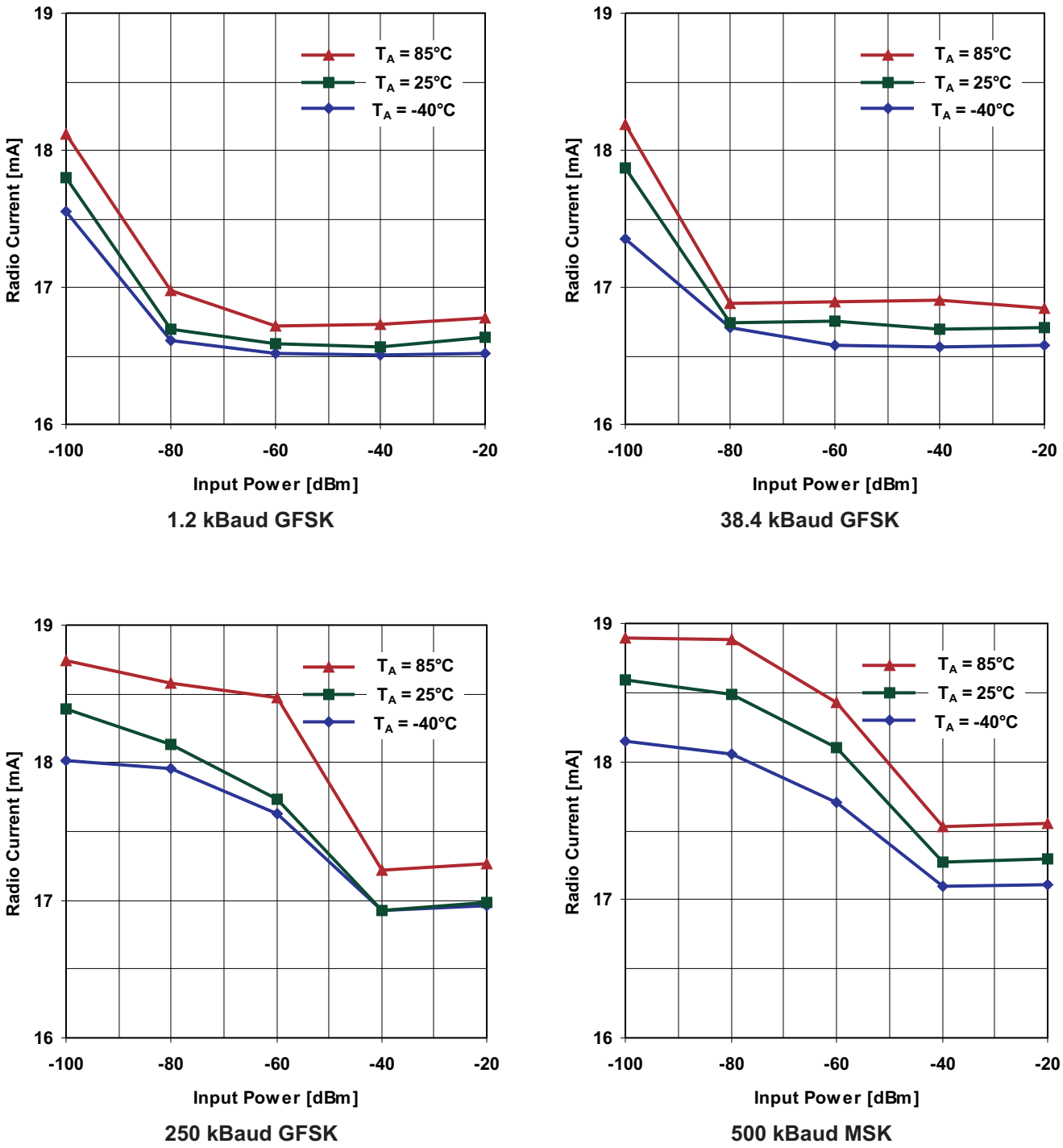

Figure 21. Typical RX Current Consumption Over Temperature and Input Power Level, 868 MHz, Sensitivity-Optimized Setting

Current Consumption, Transmit Mode

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1) (2)

PARAMETER	FREQUENCY [MHz}	PATABLE Setting	OUTPUT POWER (dBm)	MIN	TYP	MAX	UNIT
Current consumption, TX	315	0xC0	max.		26		mA
		0xC4	+10		25		mA
		0x51	0		15		mA
		0x29	-6		15		mA
	433	0xC0	max.		33		mA
		0xC6	+10		29		mA
		0x50	0		17		mA
		0x2D	-6		17		mA
	868	0xC0	max.		36		mA
		0xC3	+10		33		mA
		0x8D	0		18		mA
		0x2D	-6		18		mA
	915	0xC0	max.		35		mA
		0xC3	+10		32		mA
		0x8D	0		18		mA
		0x2D	-6		18		mA

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) Reduced current setting (MDMCFG2.DEM_DCFILT_OFF = 1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See tables "RF Receive" for additional details on current consumption and sensitivity.

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Typical TX Current Consumption, 315 MHz

PARAMETER	PATABLE Setting	Output Power (dBm)	V_{CC}	2.0 V	3.0 V	3.6 V	UNIT
			T_A	25°C	25°C	25°C	
Current consumption, TX	0xC0	max.		27.5	26.4	28.1	mA
	0xC4	+10		25.1	25.2	25.3	
	0x51	0		14.4	14.6	14.7	
	0x29	-6		14.2	14.7	15.0	

Typical TX Current Consumption, 433 MHz

PARAMETER	PATABLE Setting	Output Power (dBm)	V_{CC}	2.0 V	3.0 V	3.6 V	UNIT
			T_A	25°C	25°C	25°C	
Current consumption, TX	0xC0	max.		33.1	33.4	33.8	mA
	0xC6	+10		28.6	28.8	28.8	
	0x50	0		16.6	16.8	16.9	
	0x2D	-6		16.8	17.5	17.8	

Typical TX Current Consumption, 868 MHz

PARAMETER	PATABLE Setting	Output Power (dBm)	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
			T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Current consumption, TX	0xC0	max.		36.7	35.2	34.2	38.5	35.5	34.9	37.1	35.7	34.7	mA
	0xC3	+10		34.0	32.8	32.0	34.2	33.0	32.5	34.3	33.1	32.2	
	0x8D	0		18.0	17.6	17.5	18.3	17.8	18.1	18.4	18.0	17.7	
	0x2D	-6		17.1	17.0	17.2	17.8	17.8	18.3	18.2	18.1	18.1	

Typical TX Current Consumption, 915 MHz

PARAMETER	PATABLE Setting	Output Power (dBm)	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
			T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Current consumption, TX	0xC0	max.		35.5	33.8	33.2	36.2	34.8	33.6	36.3	35.0	33.8	mA
	0xC3	+10		33.2	32.0	31.0	33.4	32.1	31.2	33.5	32.3	31.3	
	0x8D	0		17.8	17.4	17.1	18.1	17.6	17.3	18.2	17.8	17.5	
	0x2D	-6		17.0	16.9	16.9	17.7	17.6	17.6	18.1	18.0	18.0	

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RF Receive, Overall

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital channel filter bandwidth(2)		58		812	kHz
Spurious emissions(3) (4)	25 MHz to 1 GHz		-68	-57	dBm
	Above 1 GHz		-66	-47	
RX latency	Serial operation(5)		9		bit

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
(3) Typical radiated spurious emission is -49 dBm measured at the VCO frequency
(4) Maximum figure is the ETSI EN 300 220 limit
(5) Time from start of reception until data is available on the receiver data output pin is equal to 9 bit.

RF Receive, 315 MHz

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)
2-FSK, 1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

PARAMETER	DATA RATE (kBaud)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	0.6	14.3kHz deviation, 58kHz digital channel filter bandwidth		-117		dBm
	1.2	5.2kHz deviation, 58kHz digital channel filter bandwidth(2)		-111		
	38.4	20kHz deviation, 100kHz digital channel filter bandwidth(3)		-103		
	250	127kHz deviation, 540kHz digital channel filter bandwidth (4)		-95		
	500	MSK, 812kHz digital channel filter bandwidth(4)		-86		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by about 2mA close to the sensitivity limit. The sensitivity is typically reduced to -109dBm.
(3) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by about 2mA close to the sensitivity limit. The sensitivity is typically reduced to -102dBm.
(4) MDMCFG2.DEM_DCFILT_OFF=1 can not be used for data rates ≥ 250kBaud.

RF Receive, 433 MHz

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)
2-FSK, 1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

PARAMETER	DATA RATE (kBaud)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	0.6	14.3kHz deviation, 58kHz digital channel filter bandwidth		-114		dBm
	1.2	5.2-kHz deviation, 58-kHz digital channel filter bandwidth(2)		-111		
	38.4	20-kHz deviation, 100-kHz digital channel filter bandwidth(3)		-104		
	250	127-kHz deviation, 540-kHz digital channel filter bandwidth (4)		-93		
	500	MSK, 812kHz digital channel filter bandwidth(4)		-85		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by about 2mA close to the sensitivity limit. The sensitivity is typically reduced to -109dBm.
(3) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by about 2mA close to the sensitivity limit. The sensitivity is typically reduced to -101dBm.
(4) MDMCFG2.DEM_DCFILT_OFF=1 can not be used for data rates ≥ 250kBaud.

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RF Receive, 868 or 915 MHz

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)
1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0.6-kBaud data rate, 2-FSK, 14.3-kHz deviation, 58-kHz digital channel filter bandwidth (unless otherwise noted)						
Receiver sensitivity				-115		dBm
1.2-kBaud data rate, 2-FSK, 5.2-kHz deviation, 58-kHz digital channel filter bandwidth (unless otherwise noted)						
Receiver sensitivity(2)				-109		dBm
	2-GFSK modulation by setting MDMCFG2.MOD_FORMAT=2, Gaussian filter with BT = 0.5			-109		
Saturation	FIFOTHR.CLOSE_IN_RX=0(3)			-28		dBm
Adjacent channel rejection	Desired channel 3 dB above the sensitivity limit, 100 kHz channel spacing(4)	-100-kHz offset		39		dB
		+100-kHz offset		39		
Image channel rejection	IF frequency 152 kHz, desired channel 3 dB above the sensitivity limit			29		dB
Blocking	Desired channel 3 dB above the sensitivity limit(5)	±2 MHz offset		-48		dBm
		±10 MHz offset		-40		dBm
38.4-kBaud data rate, 2-FSK, 20-kHz deviation, 100-kHz digital channel filter bandwidth (unless otherwise noted)						
Receiver sensitivity(6)				-102		dBm
	2-GFSK modulation by setting MDMCFG2.MOD_FORMAT = 2, Gaussian filter with BT = 0.5			-101		
Saturation	FIFOTHR.CLOSE_IN_RX=0(3)			-19		dBm
Adjacent channel rejection	Desired channel 3 dB above the sensitivity limit, 200 kHz channel spacing(5)	-200-kHz offset		20		dB
		+200-kHz offset		25		
Image channel rejection	IF frequency 152 kHz, Desired channel 3 dB above the sensitivity limit			23		dB
Blocking	Desired channel 3 dB above the sensitivity limit(5)	±2-MHz offset		-48		dBm
		±10-MHz offset		-40		dBm
250-kBaud data rate, 2-FSK, 127-kHz deviation, 540-kHz digital channel filter bandwidth (unless otherwise noted)						
Receiver sensitivity (7)				-90		dBm
	2-GFSK modulation by setting MDMCFG2.MOD_FORMAT = 2, Gaussian filter with BT = 0.5			-90		
Saturation	FIFOTHR.CLOSE_IN_RX=0(3)			-19		dBm
Adjacent channel rejection	Desired channel 3 dB above the sensitivity limit, 750-kHz channel spacing(8)	-750-kHz offset		24		dB
		+750-kHz offset		30		
Image channel rejection	IF frequency 304 kHz, Desired channel 3 dB above the sensitivity limit			18		dB
Blocking	Desired channel 3 dB above the sensitivity limit(8)	±2-MHz offset		-53		dBm
		±10-MHz offset		-39		dBm
500-kBaud data rate, MSK, 812-kHz digital channel filter bandwidth (unless otherwise noted)						
Receiver sensitivity(7)				-84		dBm
Image channel rejection	IF frequency 355 kHz, Desired channel 3 dB above the sensitivity limit			-2		dB
Blocking	Desired channel 3 dB above the sensitivity limit(9)	±2-MHz offset		-53		dBm
		±10-MHz offset		-38		dBm

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by about 2mA close to the sensitivity limit. The sensitivity is typically reduced to -107dBm
(3) See design note *DN010 Close-in Reception with CC1101* (SWRA147).
(4) See Figure 22 for blocking performance at other offset frequencies.
(5) See Figure 23 for blocking performance at other offset frequencies.
(6) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by about 2mA close to the sensitivity limit. The sensitivity is typically reduced to -100dBm.
(7) MDMCFG2.DEM_DCFILT_OFF = 1 cannot be used for data rates ≥ 250kBaud.
(8) See Figure 24 for blocking performance at other offset frequencies.
(9) See Figure 25 for blocking performance at other offset frequencies.

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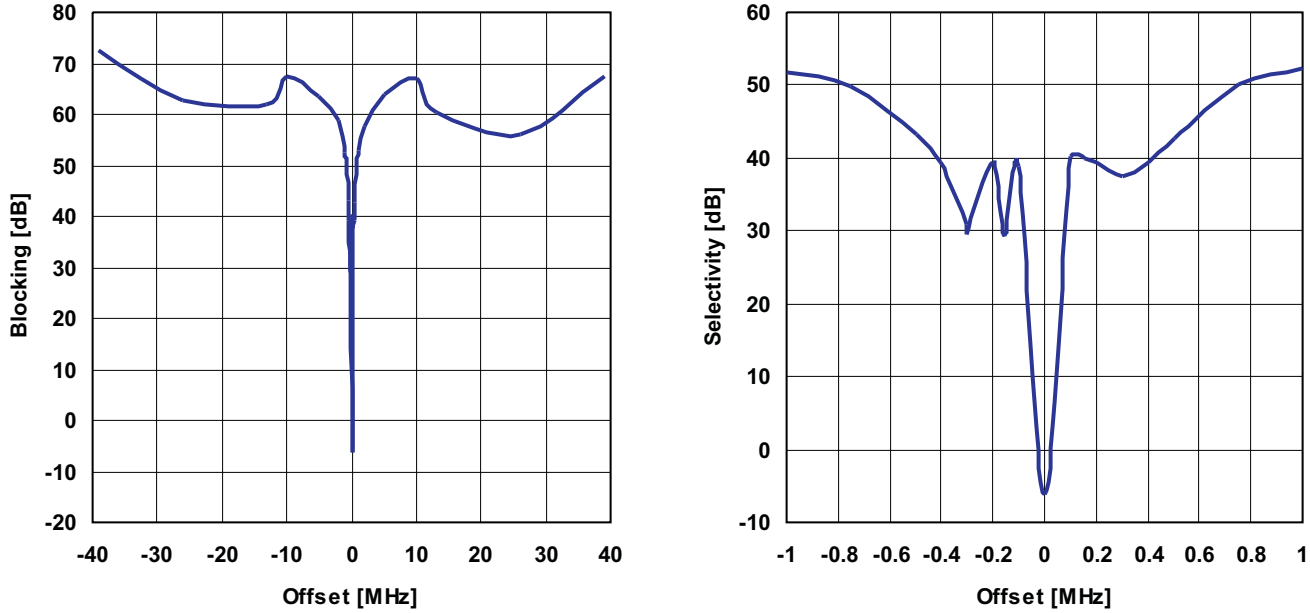
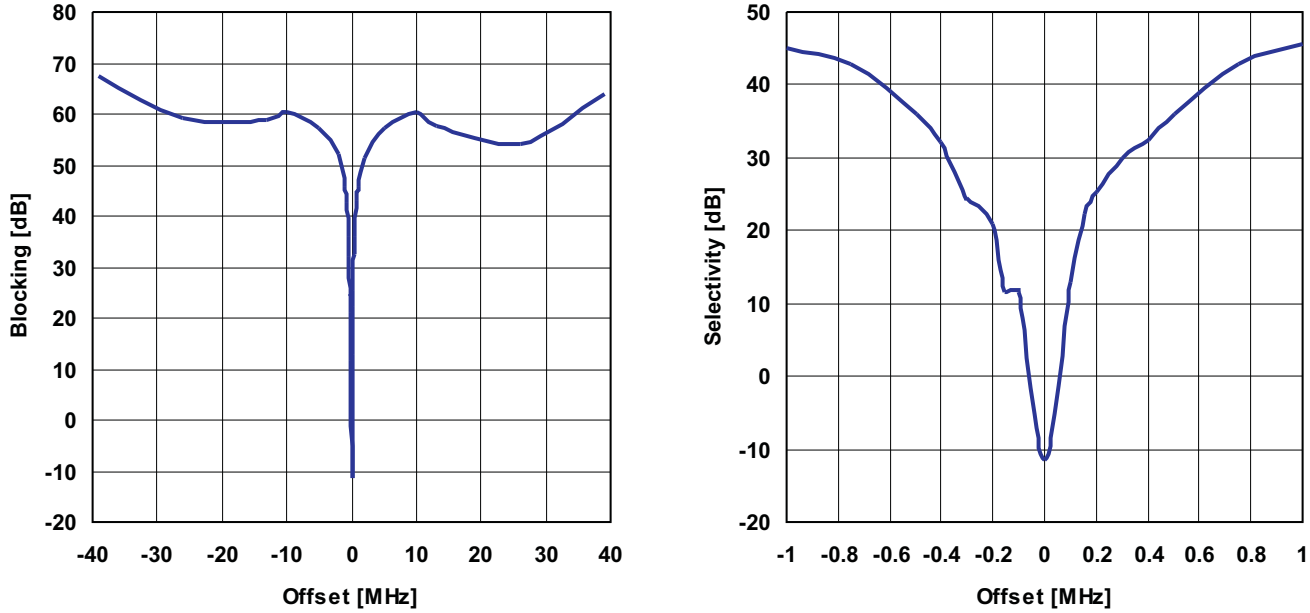


NOTE: 868.3 MHz, 2-FSK, 5.2-kHz deviation, IF frequency is 152.3 kHz, digital channel filter bandwidth is 58 kHz

Figure 22. Typical Selectivity at 1.2-kBaud Data Rate



NOTE: 868 MHz, 2-FSK, 20 kHz deviation, IF frequency is 152.3 kHz, digital channel filter bandwidth is 100 kHz

Figure 23. Typical Selectivity at 38.4-kBaud Data Rate

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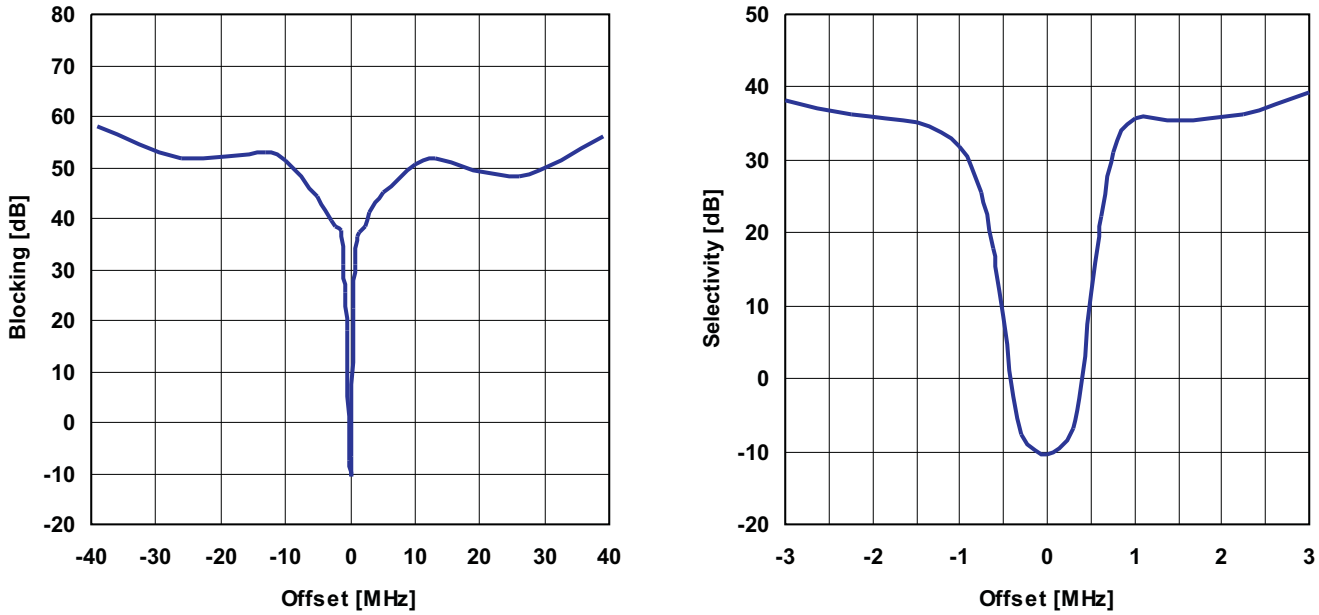
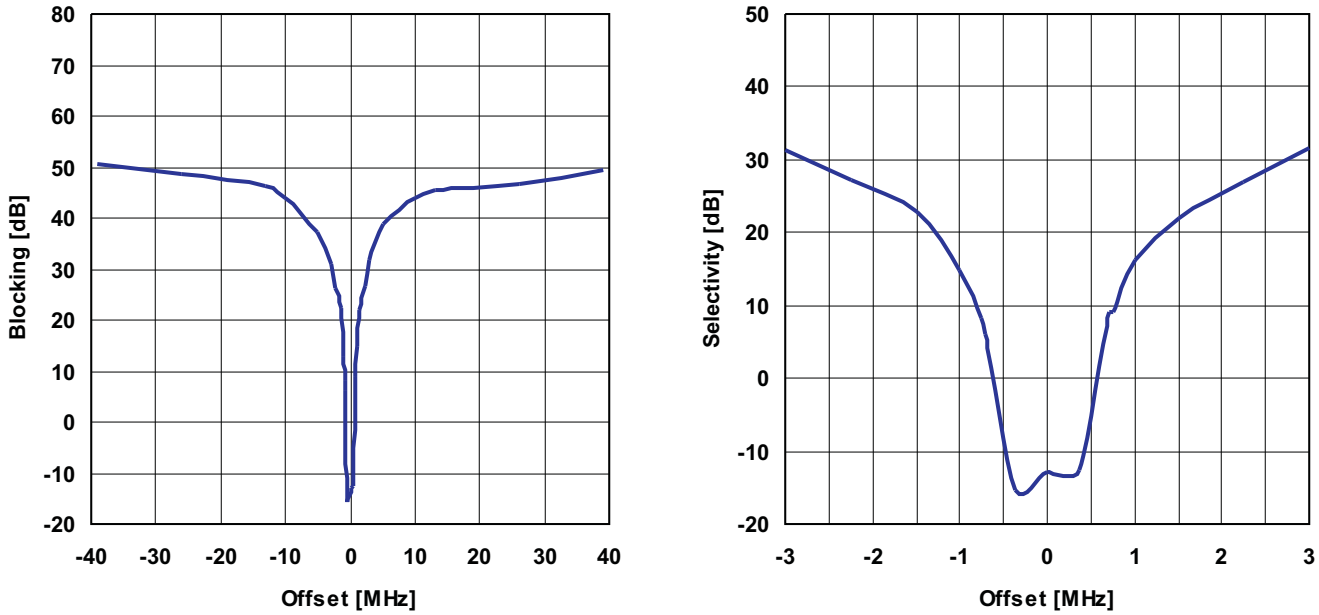


NOTE: 868 MHz, 2-FSK, IF frequency is 304 kHz, digital channel filter bandwidth is 540 kHz

Figure 24. Typical Selectivity at 250-kBaud Data Rate



NOTE: 868 MHz, 2-FSK, IF frequency is 355 kHz, digital channel filter bandwidth is 812 kHz

Figure 25. Typical Selectivity at 500-kBaud Data Rate

Typical Sensitivity, 315 MHz, Sensitivity Optimized Setting

PARAMETER	DATA RATE (kBaud)	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Sensitivity, 315MHz	1.2		-112	-112	-110	-112	-111	-109	-112	-111	-108	dBm
	38.4		-105	-105	-104	-105	-103	-102	-105	-104	-102	
	250		-95	-95	-92	-94	-95	-92	-95	-94	-91	

Typical Sensitivity, 433 MHz, Sensitivity Optimized Setting

PARAMETER	DATA RATE (kBaud)	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Sensitivity, 433MHz	1.2		-111	-110	-108	-111	-111	-108	-111	-110	-107	dBm
	38.4		-104	-104	-101	-104	-104	-101	-104	-103	-101	
	250		-93	-94	-91	-93	-93	-90	-93	-93	-90	

Typical Sensitivity, 868 MHz, Sensitivity Optimized Setting

PARAMETER	DATA RATE (kBaud)	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Sensitivity, 868MHz	1.2		-109	-109	-107	-109	-109	-106	-109	-108	-106	dBm
	38.4		-102	-102	-100	-102	-102	-99	-102	-101	-99	
	250		-90	-90	-88	-89	-90	-87	-89	-90	-87	
	500		-84	-84	-81	-84	-84	-80	-84	-84	-80	

Typical Sensitivity, 915 MHz, Sensitivity Optimized Setting

PARAMETER	DATA RATE (kBaud)	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Sensitivity, 915MHz	1.2		-109	-109	-107	-109	-109	-106	-109	-108	-105	dBm
	38.4		-102	-102	-100	-102	-102	-99	-103	-102	-99	
	250		-92	-92	-89	-92	-92	-88	-92	-92	-88	
	500		-87	-86	-81	-86	-86	-81	-86	-85	-80	

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RF Transmit

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)
P_{TX} = +10 dBm (unless otherwise noted)

PARAMETER	FREQUENCY (MHz)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Differential load impedance(2)	315				122 + j31		Ω
	433				116 + j41		
	868, 915				86.5 + j43		
Output power, highest setting(3)	315	Delivered to a 50Ω single-ended load via CC430 reference design's RF matching network			+12		dBm
	433				+13		
	868				+11		
	915				+11		
Output power, lowest setting(3)		Delivered to a 50Ω single-ended load via CC430 reference design's RF matching network			-30		dBm
Harmonics, radiated(4)(5)(6)	433	Second harmonic			-56		dBm
		Third harmonic			-57		
	868	Second harmonic			-50		
		Third harmonic			-52		
	915	Second harmonic			-50		
		Third harmonic			-54		
Harmonics, conducted	315	Frequencies below 960 MHz	+10 dBm CW		< -38		dBm
		Frequencies above 960 MHz			< -48		
	433	Frequencies below 1 GHz	+10 dBm CW		-45		
		Frequencies above 1 GHz			< -48		
	868	Second harmonic	+10 dBm CW		-59		
		Other harmonics			< -71		
	915	Second harmonic	+11 dBm CW(7)		-53		
		Other harmonics			< -47		
Spurious emissions, conducted, harmonics not included(8)	315	Frequencies below 960 MHz	+10 dBm CW		< -58		dBm
		Frequencies above 960 MHz			< -53		
	433	Frequencies below 1 GHz	+10 dBm CW		< -54		
		Frequencies above 1 GHz			< -54		
		Frequencies within 47 to 74, 87.5 to 118, 174 to 230, 470 to 862 MHz			< -63		
	868	Frequencies below 1 GHz	+10 dBm CW		< -46		
		Frequencies above 1 GHz			< -59		
		Frequencies within 47 to 74, 87.5 to 118, 174 to 230, 470 to 862 MHz			< -56		
	915	Frequencies below 960 MHz	+11 dBm CW		< -49		
		Frequencies above 960 MHz			< -63		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC430 reference designs available from the TI website.
(3) Output power is programmable, and full range is available in all frequency bands. Output power may be restricted by regulatory limits. See also application note *AN050 Using the CC1101 in the European 868MHz SRD Band* (SWRA146) and design note *DN013 Programming Output Power on CC1101* (SWRA168), which gives the output power and harmonics when using multi-layer inductors. The output power is then typically +10 dBm when operating at 868 or 915 MHz.
(4) The antennas used during the radiated measurements (SMAFF-433 from R.W.Badland and Nearson S331 868/915) play a part in attenuating the harmonics.
(5) Measured on EM430F6137RF900 with CW, maximum output power
(6) All harmonics are below -41.2 dBm when operating in the 902 to 928 MHz band.
(7) Requirement is -20 dBc under FCC 15.247
(8) All radiated spurious emissions are within the limits of ETSI. Also see design note *DN017 CC11xx 868/915 MHz RF Matching* (SWRA168).

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RF Transmit (continued)

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)
P_{TX} = +10 dBm (unless otherwise noted)

PARAMETER	FREQUENCY (MHz)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX latency(9)		Serial operation		8		bits

(9) Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports

Optimum PATABLE Settings for Various Output Power Levels and Frequency Bands

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)

Output Power (dBm)	PATABLE Setting			
	315 MHz	433 MHz	868 MHz	915 MHz
-30	0x12	0x05	0x03	0x03
-12	0x33	0x26	0x25	0x25
-6	0x29	0x2D	0x2D	0x2D
0	0x51	0x50	0x8D	0x8D
10	0xC4	0xC4	0xC3	0xC3
Maximum	0xC0	0xC0	0xC0	0xC0

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).

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Typical Output Power, 315 MHz(1)

PARAMETER	PATABLE Setting	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Output power, 315 MHz	0xC0 (max)			11.9			11.8			11.8		dBm
	0xC4 (10 dBm)			10.3			10.3			10.3		
	0xC6 (default)						9.3					
	0x51 (0 dBm)			0.7			0.6			0.7		
	0x29 (-6 dBm)			-6.8			-5.6			-5.3		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).

Typical Output Power, 433 MHz(1)

PARAMETER	PATABLE Setting	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Output power, 433 MHz	0xC0 (max)			12.6			12.6			12.6		dBm
	0xC4 (10 dBm)			10.3			10.2			10.2		
	0xC6 (default)						10.0					
	0x50 (0 dBm)			0.3			0.3			0.3		
	0x2D (-6 dBm)			-6.4			-5.4			-5.1		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).

Typical Output Power, 868 MHz(1)

PARAMETER	PATABLE Setting	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Output power, 868 MHz	0xC0 (max)		11.9	11.2	10.5	11.9	11.2	10.5	11.9	11.2	10.5	dBm
	0xC3 (10 dBm)		10.8	10.1	9.4	10.8	10.1	9.4	10.7	10.1	9.4	
	0xC6 (default)						8.8					
	0x8D (0 dBm)		1.0	0.3	-0.3	1.1	0.3	-0.3	1.1	0.3	-0.3	
	0x2D (-6 dBm)		-6.5	-6.8	-7.3	-5.3	-5.8	-6.3	-4.9	-5.4	-6.0	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).

Typical Output Power, 915 MHz(1)

PARAMETER	PATABLE Setting	V_{CC}	2.0 V			3.0 V			3.6 V			UNIT
		T_A	-40°C	25°C	85°C	-40°C	25°C	85°C	-40°C	25°C	85°C	
Output power, 915 MHz	0xC0 (max)		12.2	11.4	10.6	12.1	11.4	10.7	12.1	11.4	10.7	dBm
	0xC3 (10 dBm)		11.0	10.3	9.5	11.0	10.3	9.5	11.0	10.3	9.6	
	0xC6 (default)						8.8					
	0x8D (0 dBm)		1.9	1.0	0.3	1.9	1.0	0.3	1.9	1.1	0.3	
	0x2D (-6 dBm)		-5.5	-6.0	-6.5	-4.3	-4.8	-5.5	-3.9	-4.4	-5.1	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).

Frequency Synthesizer Characteristics

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)
MIN figures are given using a 27MHz crystal. TYP and MAX figures are given using a 26MHz crystal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmed frequency resolution(2)	26- to 27-MHz crystal	397	$f_{XOSC}/2^{16}$	412	Hz
Synthesizer frequency tolerance(3)			±40		ppm
RF carrier phase noise	50-kHz offset from carrier		–95		dBc/Hz
	100-kHz offset from carrier		–94		
	200-kHz offset from carrier		–94		
	500-kHz offset from carrier		–98		
	1-MHz offset from carrier		–107		
	2-MHz offset from carrier		–112		
	5-MHz offset from carrier		–118		
	10-MHz offset from carrier		–129		
PLL turn-on and hop time(4)	Crystal oscillator running	85.1	88.4	88.4	µs
PLL RX to TX settling time(5)		9.3	9.6	9.6	µs
PLL TX to RX settling time(6)		20.7	21.5	21.5	µs
PLL calibration time(7)		694	721	721	µs

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).
(2) The resolution (in Hz) is equal for all frequency bands.
(3) Depends on crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth and spacing.
(4) Time from leaving the IDLE state until arriving in the RX, FSTXON, or TX state, when not performing calibration.
(5) Settling time for the 1-IF frequency step from RX to TX
(6) Settling time for the 1-IF frequency step from TX to RX
(7) Calibration can be initiated manually or automatically before entering or after leaving RX or TX.

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Typical RSSI_offset Values

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)(1)

DATA RATE (kBaud)	RSSI_OFFSET (dB)	
	433 MHz	868 MHz
1.2	74	74
38.4	74	74
250	74	74
500	74	74

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 48).

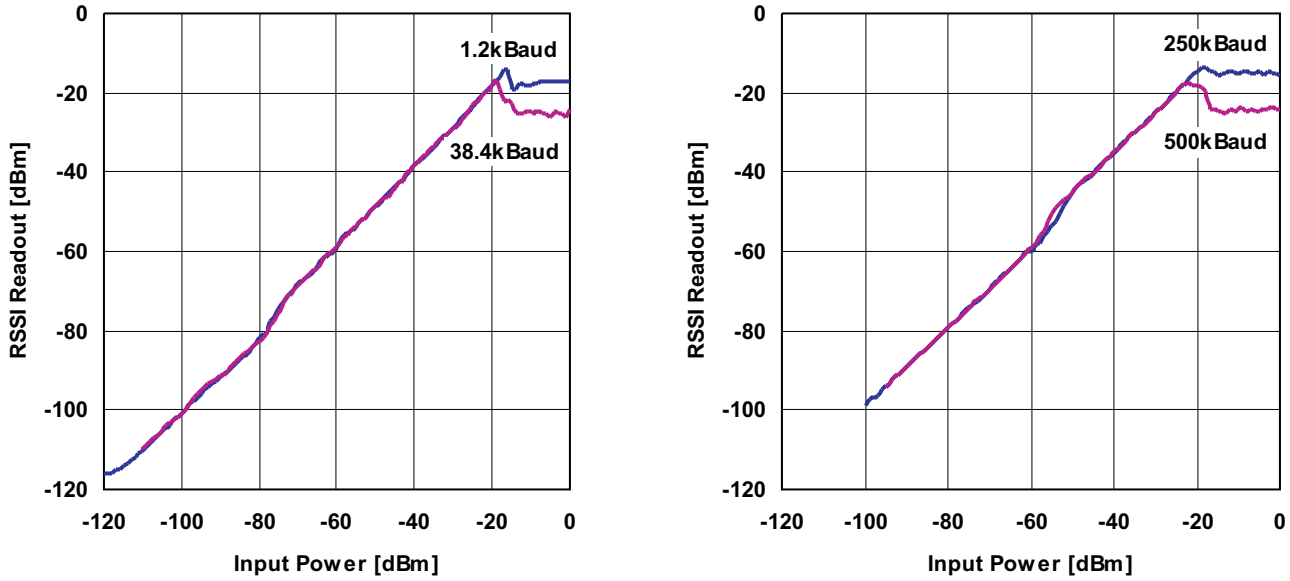
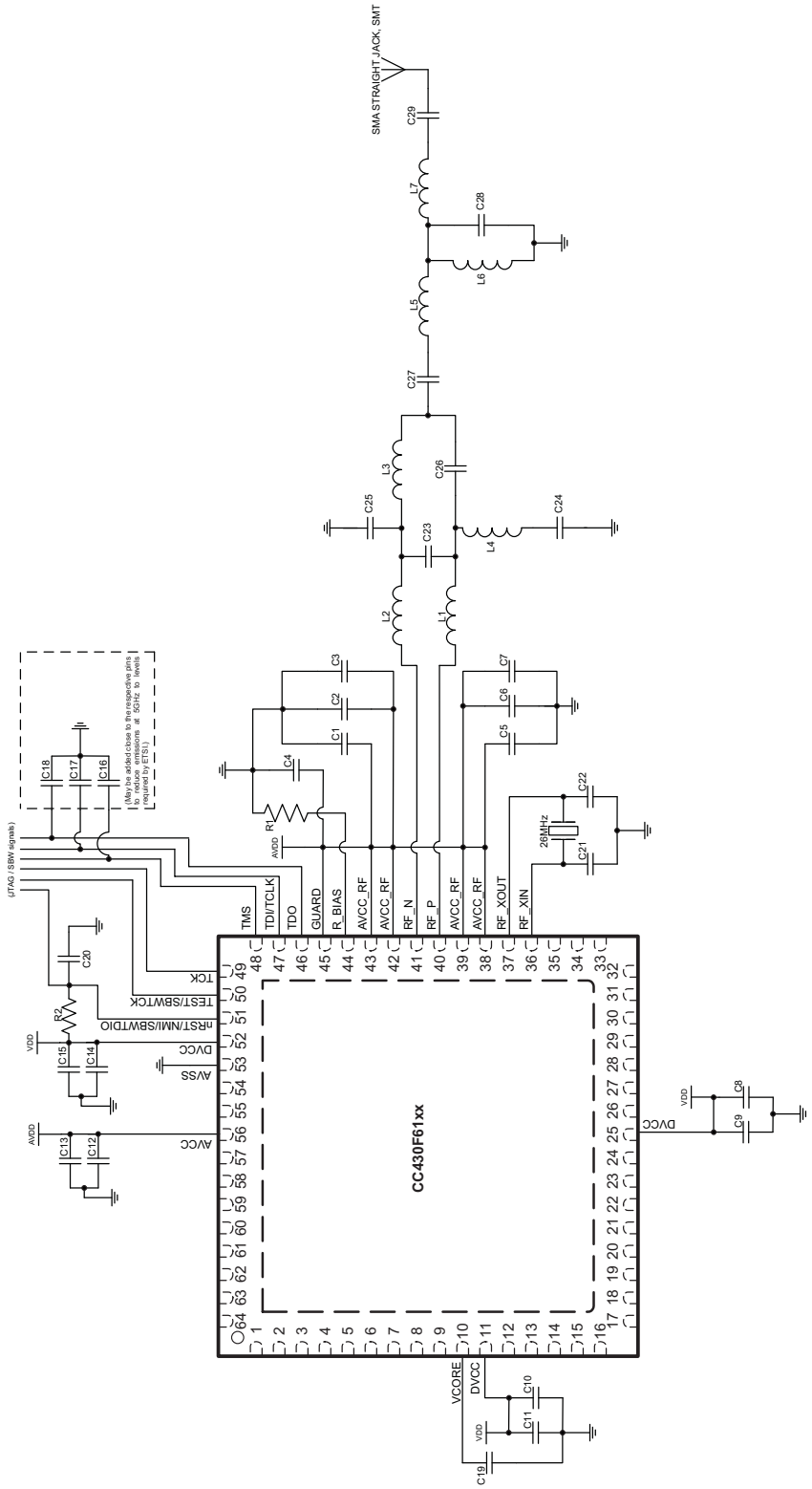


Figure 26. Typical RSSI Value vs Input Power Level for Different Data Rates at 868 MHz

APPLICATION CIRCUIT



For a complete reference design including layout see the CC430 Wireless Development Tools and related documentation [*MSP430 Hardware Tools User's Guide* (SLAU278)].

Figure 27. Typical Application Circuit CC430F61xx

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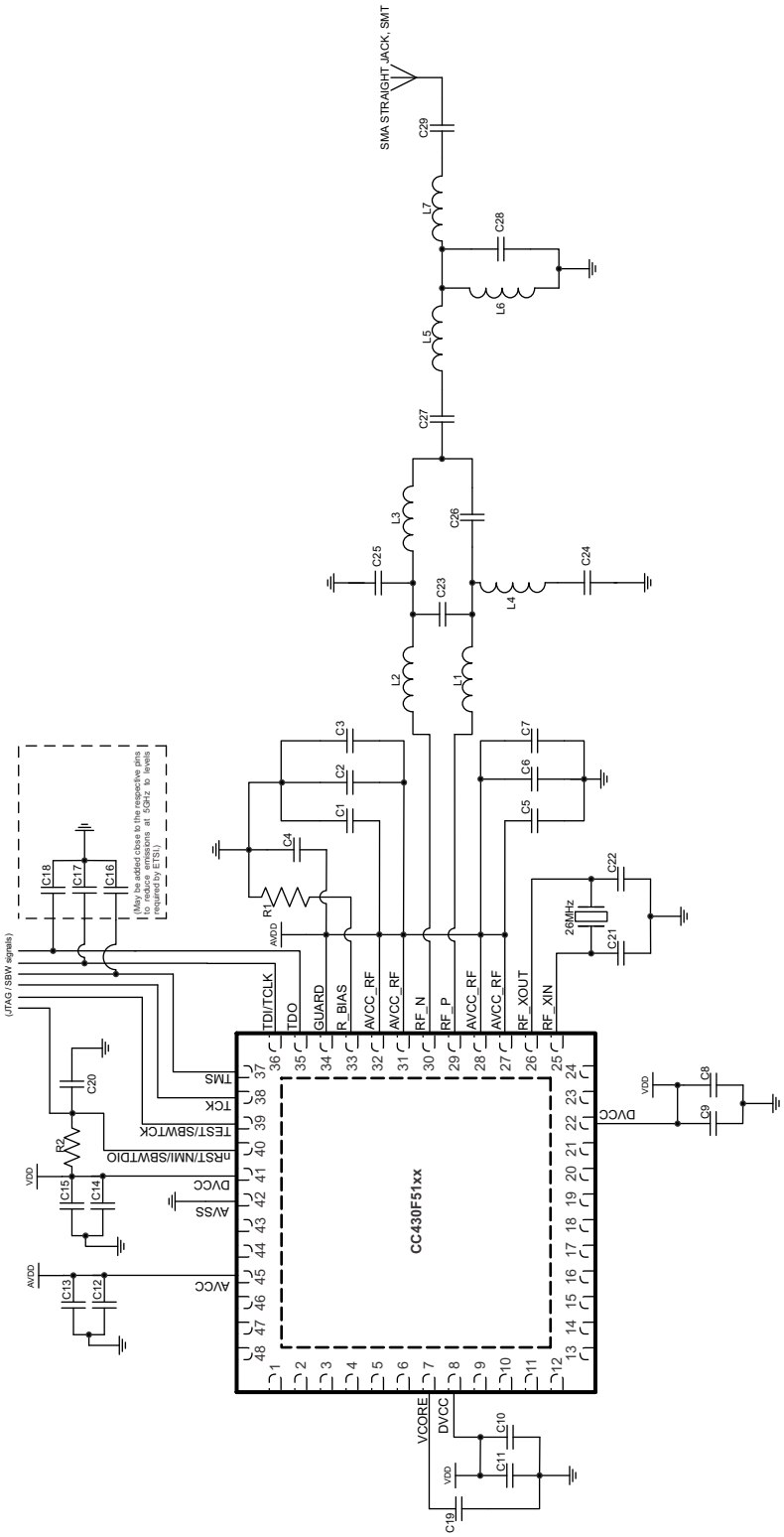

For a complete reference design including layout see the CC430 Wireless Development Tools and related documentation [*MSP430 Hardware Tools User's Guide* (SLAU278)].

Figure 28. Typical Application Circuit CC430F51xx

Table 48. Bill of Materials

Components	For 315 MHz	For 433 MHz	For 868, 915 MHz	Comment
C1,3,4,5,7,9,11,13,15	100 nF			Decoupling capacitors
C8,10,12,14	10 µF			Decoupling capacitors
C2,6,16,17,18	2 pF			Decoupling capacitors
C19	470 nF			V_{CORE} capacitor
C20	2.2 nF			$\overline{RST}$ decoupling cap (optimized for SBW)
C21,22	27 pF			Load capacitors for 26 MHz crystal(1)
R1	56 kΩ			R_BIAS (±1% required)
R2	47 kΩ			$\overline{RST}$ pullup
L1,2	Capacitors: 220 pF	0.016 µH	0.012 µH	
L3,4	0.033 µH	0.027 µH	0.018 µH	
L5	0.033 µH	0.047 µH	0.015 µH	
L6	dnp(2)	dnp(2)	0.0022 µH	
L7	0.033 µH	0.051 µH	0.015 µH	
C23	dnp(2)	2.7 pF	1 pF	
C24	220 pF	220 pF	100 pF	
C25	6.8 pF	3.9 pF	1.5 pF	
C26	6.8 pF	3.9 pF	1.5 pF	
C27	220 pF	220 pF	1.5 pF	
C28	10 pF	4.7 pF	8.2 pF	
C29	220 pF	220 pF	1.5 pF	

(1) The load capacitance C_L seen by the crystal is $C_L = 1/((1/C21)+(1/C22)) + C_{parasitic}$. The parasitic capacitance $C_{parasitic}$ includes pin capacitance and PCB stray capacitance. It can be typically estimated to be approximately 2.5 pF.
(2) dnp = do not populate

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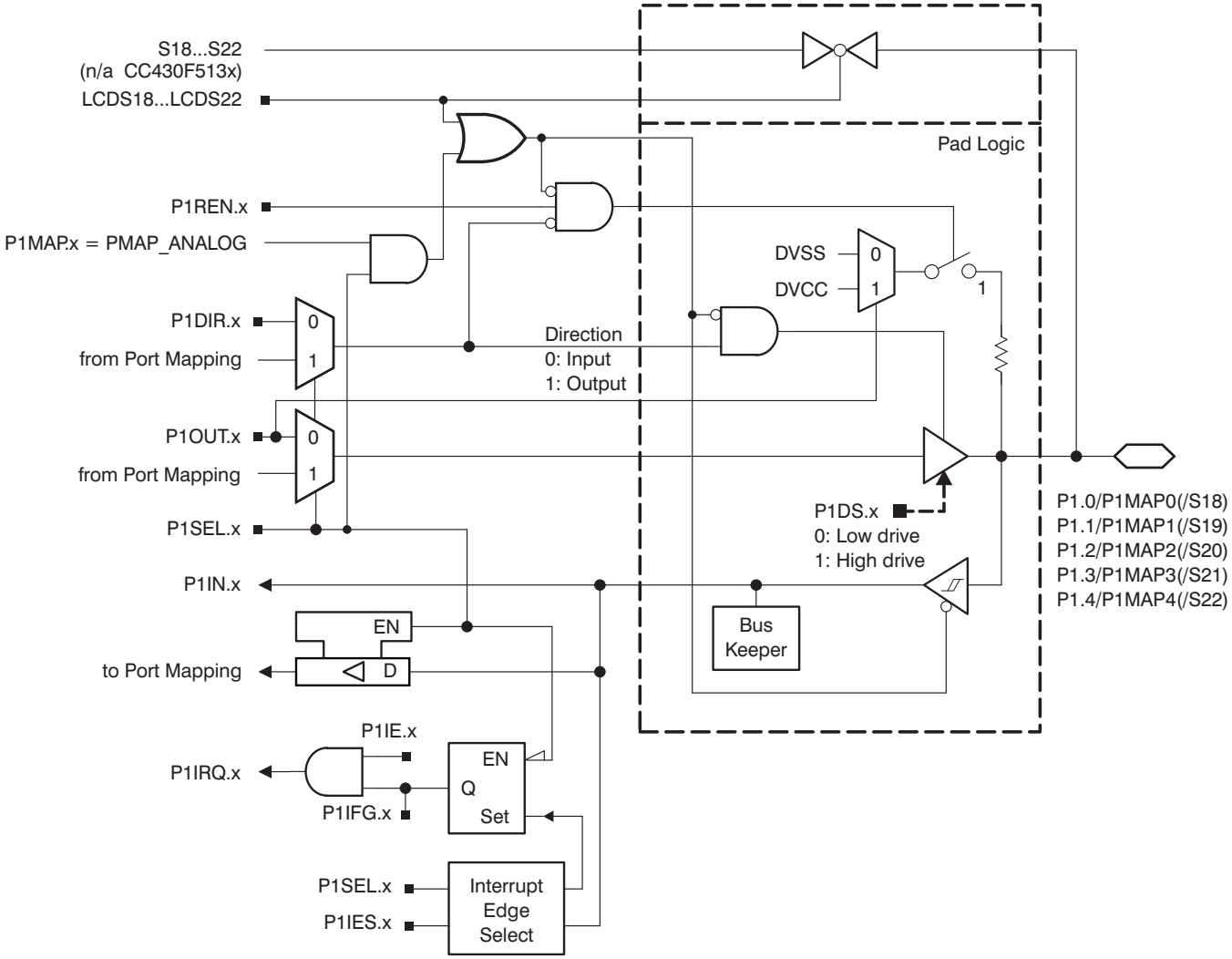
INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.4, Input/Output With Schmitt Trigger



CC430F513x devices don't provide LCD functionality on port P1 pins.

Table 49. Port P1 (P1.0 to P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P1DIR.x	P1SEL.x	P1MAPx	LCDS19...22[2]
P1.0/P1MAP/S18	0	P1.0 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S18 (not available on CC430F513x)	X	X	X	1
P1.1/P1MAP1/S19	1	P1.1 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S19 (not available on CC430F513x)	X	X	X	1
P1.2/P1MAP2/S20	2	P1.2 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S22 (not available on CC430F513x)	X	X	X	1
P1.3/P1MAP3/S21	3	P1.3 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S21 (not available on CC430F513x)	X	X	X	1
P1.4/P1MAP4/S22	4	P1.4 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S22 (not available on CC430F513x)	X	X	X	1

(1) X = don't care
(2) LCDSx not available in CC430F513x.
(3) According to mapped function - see Table 9.

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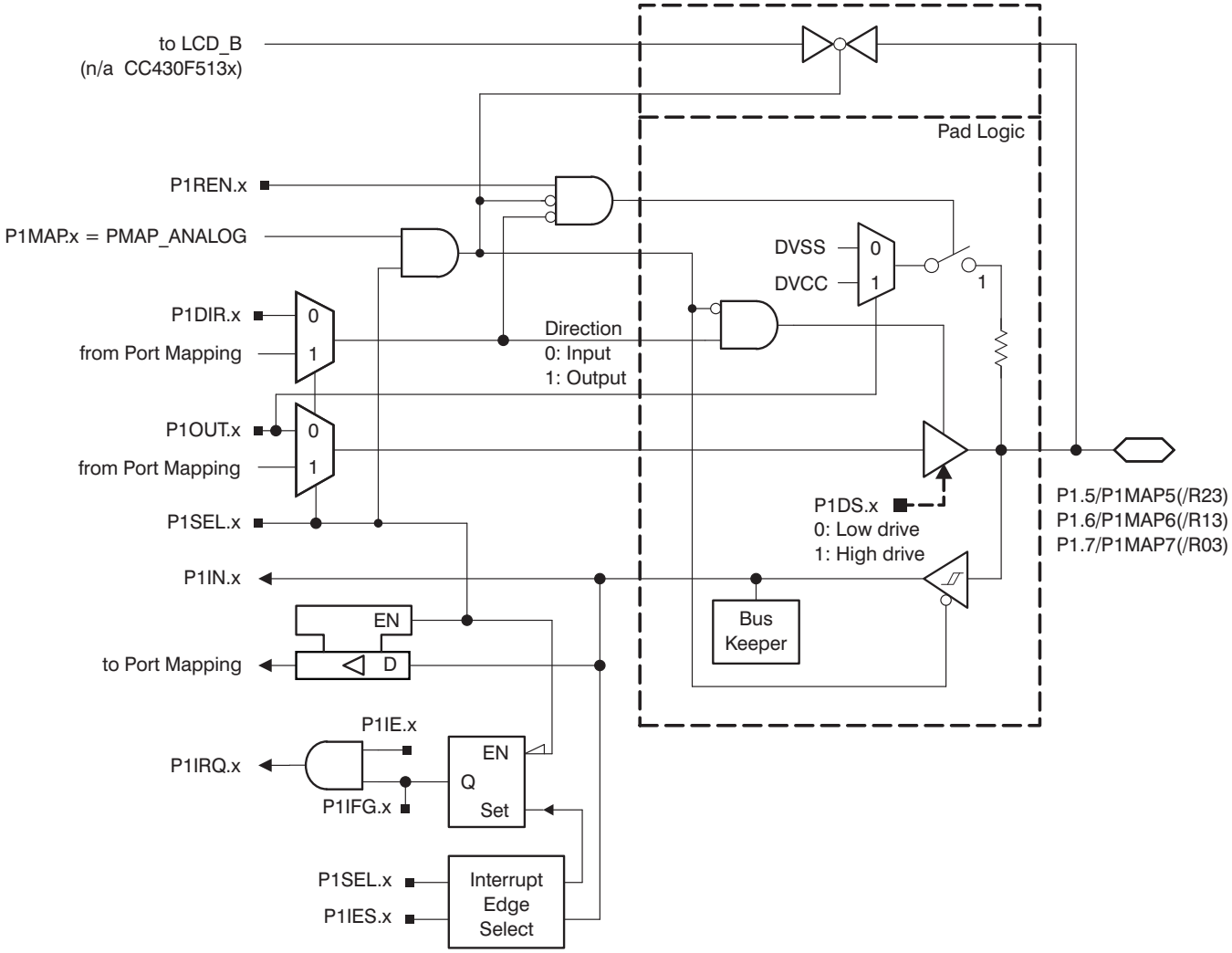
Port P1, P1.5 to P1.7, Input/Output With Schmitt Trigger



CC430F513x devices don't provide LCD functionality on port P1 pins.

Table 50. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P1DIR.x	P1SEL.x	P1MAPx
P1.5/P1MAP5/R23	5	P1.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]
		R23[3] (not available on CC430F513x)	X	1	= 31
P1.6/P1MAP6/R13/ LCDREF	6	P1.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]
		R13/LCDREF[3] (not available on CC430F513x)	X	1	= 31
P1.7/P1MAP7/R03	7	P1.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]
		R03[3] (not available on CC430F513x)	X	1	= 31

(1) X = don't care
(2) According to mapped function - see Table 9.
(3) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver as well as the input Schmitt trigger.

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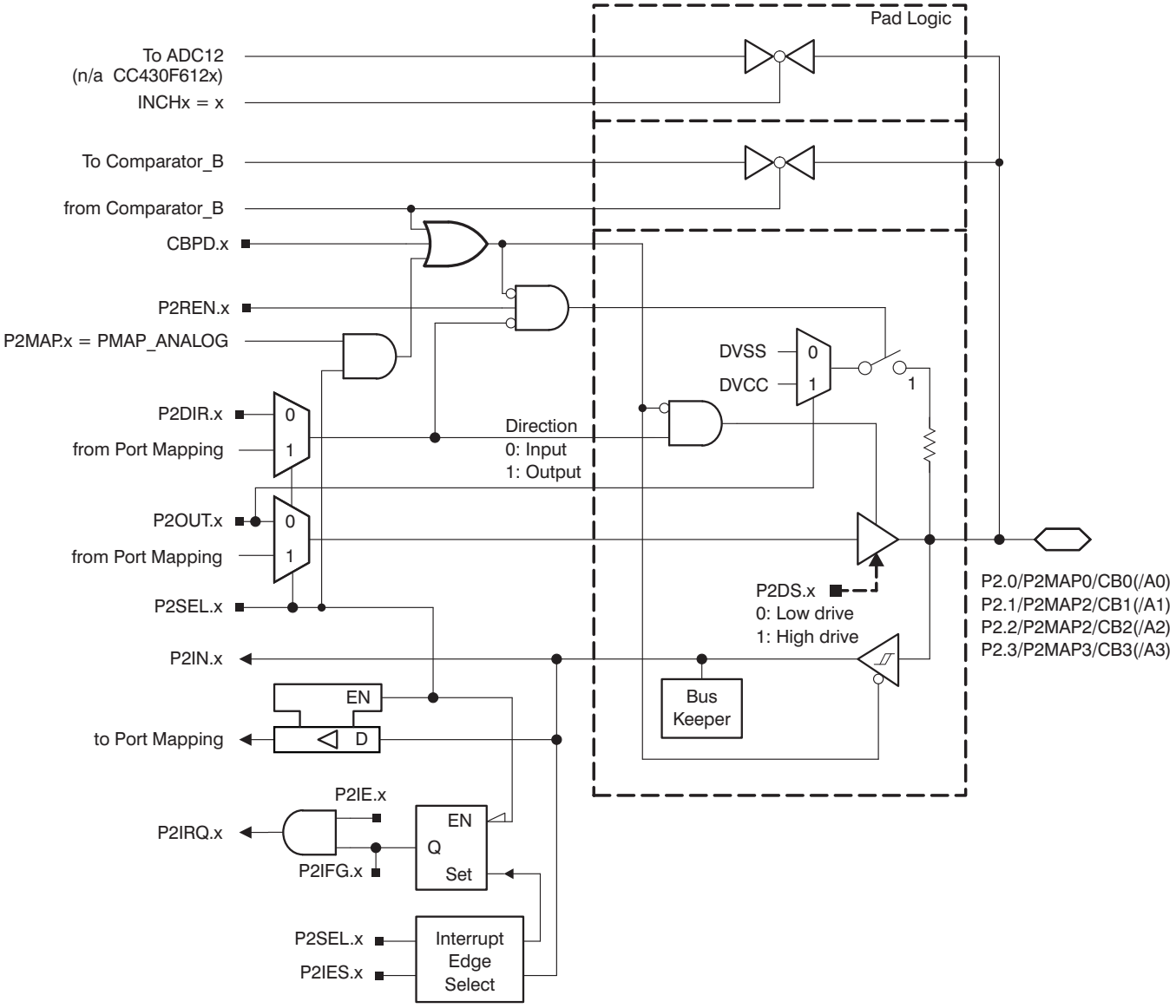
Port P2, P2.0 to P2.3, Input/Output With Schmitt Trigger



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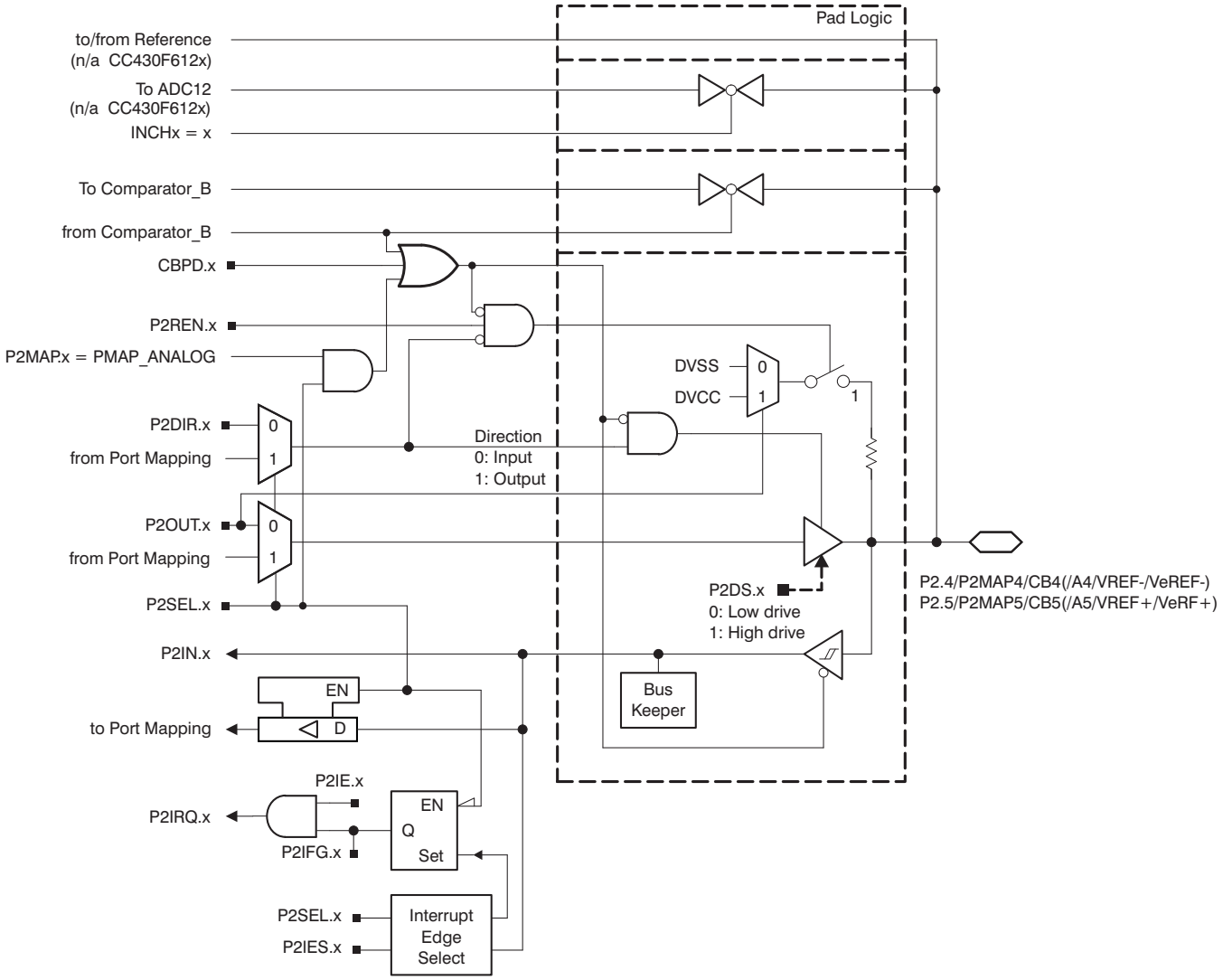
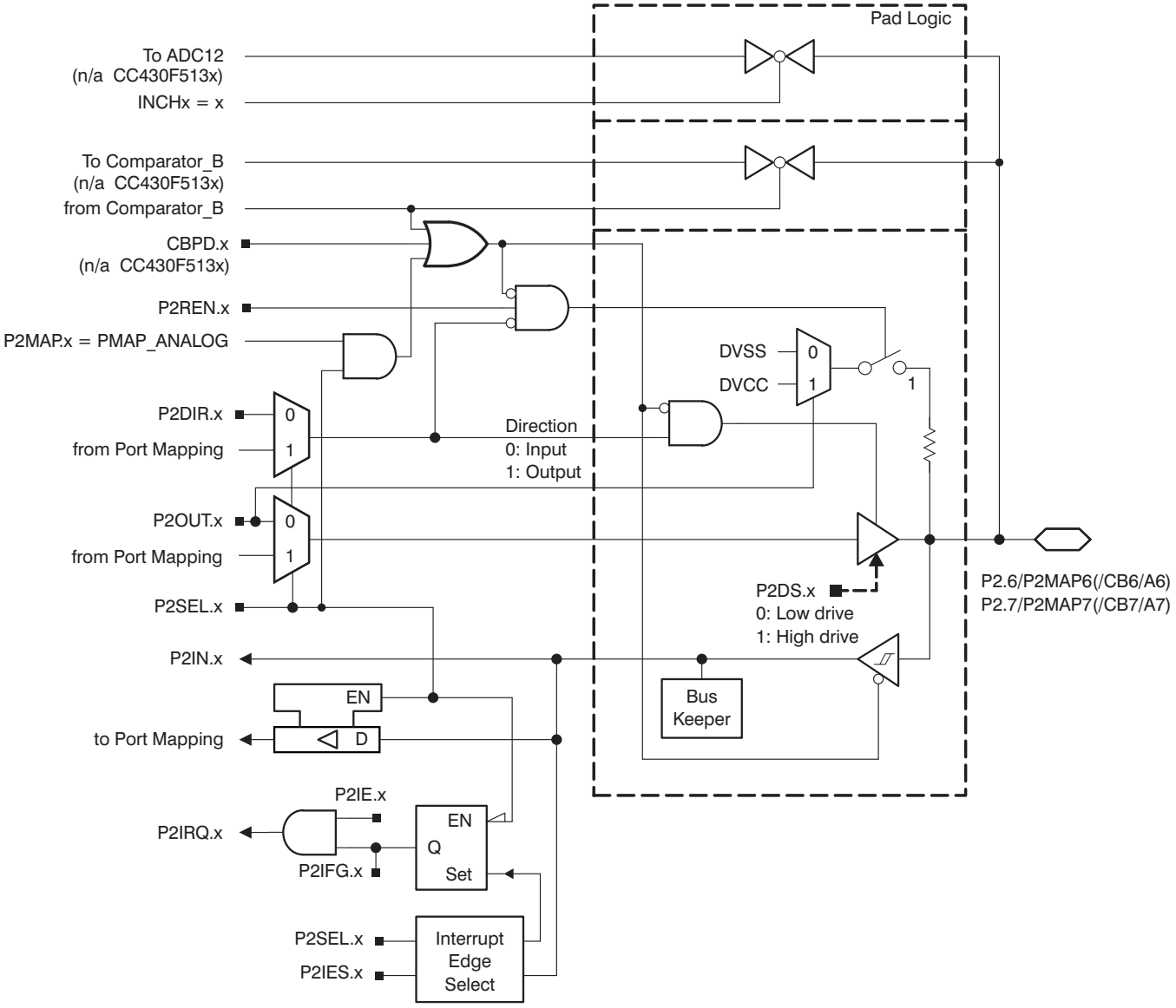
Port P2, P2.4 to P2.5, Input/Output With Schmitt Trigger



Port P2, P2.6 and P2.7, Input/Output With Schmitt Trigger



CC430F513x devices don't provide analog functionality on port P2.6 and P2.7 pins.

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Table 51. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P2DIR.x	P2SEL.x	P2MAPx	CBPD.x
P2.0/P2MAP0/CB0 (/A0)	0	P2.0 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A0 (not available on CC430F612x)[3]	X	1	= 31	X
		CB0[4]	X	X	X	1
P2.1/P2MAP1/CB1 (/A1)	1	P2.1 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A1 (not available on CC430F612x)[3]	X	1	= 31	X
		CB1[4]	X	X	X	1
P2.2/P2MAP2/CB2 (/A2)	2	P2.2 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A2 (not available on CC430F612x)[3]	X	1	= 31	X
		CB2[4]	X	X	X	1
P2.3/P2MAP3/CB3 (/A3)	3	P2.3 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A3 (not available on CC430F612x)[3]	X	1	= 31	X
		CB3[4]	X	X	X	1
P2.4/P2MAP4/CB4 (/A4/VREF-/VeREF-)	4	P2.4 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A4/VREF-/VeREF- (not available on CC430F612x)[3]	X	1	= 31	X
		CB4[4]	X	X	X	1
P2.5/P2MAP5/CB5 (/A5/VREF+/VeREF+)	5	P2.5 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A5/VREF+/VeREF+ (not available on CC430F612x)[3]	X	1	= 31	X
		CB5[4]	X	X	X	1
P2.6/P2MAP6(/CB6) (/A6)	6	P2.6 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A6 (not available on CC430F612x and CC430F513x)[3]	X	1	= 31	X
		CB6 (not available on CC430F513x)[4]	X	X	X	1
P2.7/P2MAP7(/CB7) (/A7)	7	P2.7 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[2]	1	≤ 30[2]	0
		A7 (not available on CC430F612x and CC430F513x)[3]	X	1	= 31	X
		CB7 (not available on CC430F513x)[4]	X	X	X	1

(1) X = don't care
(2) According to mapped function - see Table 9.
(3) Setting P2SEL.x bit together with P2MAPx = PM_ANALOG disables the output driver as well as the input Schmitt trigger.
(4) Setting the CBPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

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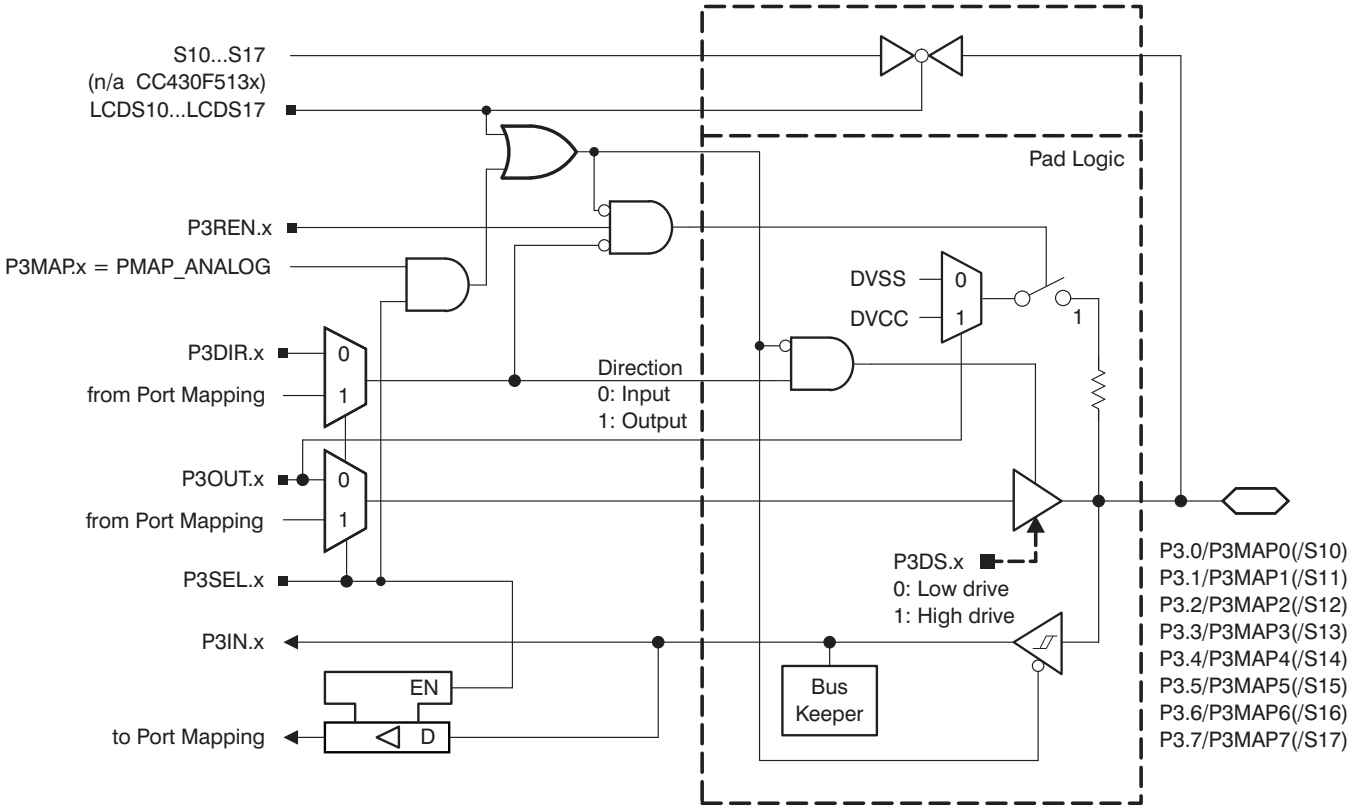
Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger



CC430F513x devices don't provide LCD functionality on port P3 pins.

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Table 52. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P3DIR.x	P3SEL.x	P3MAPx	LCDS10...17[2]
P3.0/P3MAP0/S10	0	P3.0 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S10 (not available on CC430F513x)	X	X	X	1
P3.1/P3MAP1/S11	1	P3.1 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S11 (not available on CC430F513x)	X	X	X	1
P3.2/P3MAP7/S12	2	P3.2 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S12 (not available on CC430F513x)	X	X	X	1
P3.3/P3MAP3/S13	3	P3.3 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S13 (not available on CC430F513x)	X	X	X	1
P3.4/P3MAP4/S14	4	P3.4 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S14 (not available on CC430F513x)	X	X	X	1
P3.5/P3MAP5/S15	5	P3.5 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S15 (not available on CC430F513x)	X	X	X	1
P3.6/P3MAP6/S16	6	P3.6 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S16 (not available on CC430F513x)	X	X	X	1
P3.7/P3MAP7/S17	7	P3.7 (I/O)	I: 0; O: 1	0	X	0
		Mapped secondary digital function - see Table 9	0; 1[3]	1	≤ 30[3]	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S17 (not available on CC430F513x)	X	X	X	1

(1) X = don't care
(2) LCDSx not available in CC430F513x.
(3) According to mapped function - see Table 9.

Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger (CC430F613x and CC430F612x only)

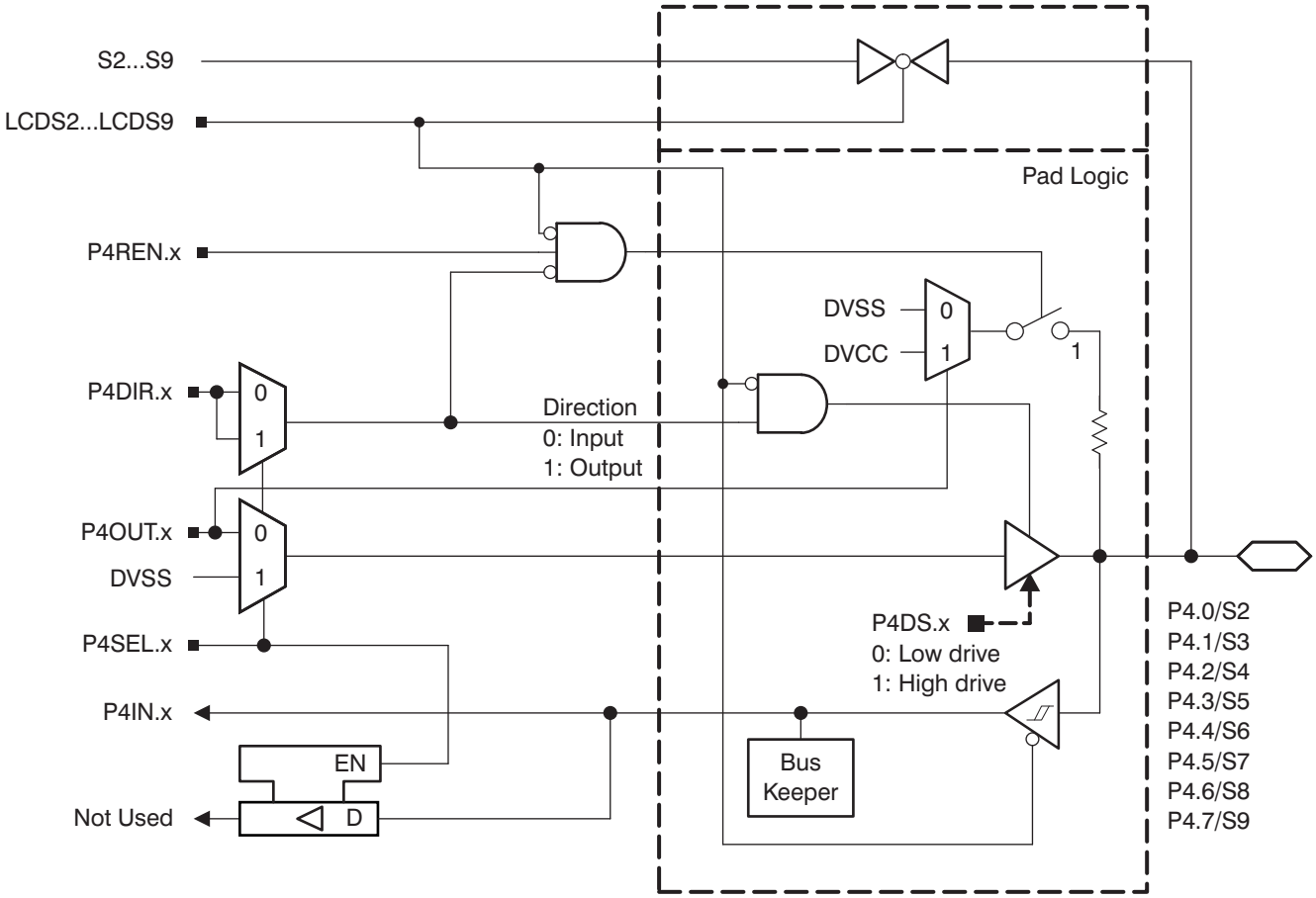

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Table 53. Port P4 (P4.0 to P4.7) Pin Functions (CC430F613x and CC430F612x only)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P4DIR.x	P4SEL.x	LCDS2...7
P4.0/P4MAP0/S2	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S2	X	X	1
P4.1/P4MAP1/S3	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S3	X	X	1
P4.2/P4MAP7/S4	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S4	X	X	1
P4.3/P4MAP3/S5	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S5	X	X	1
P4.4/P4MAP4/S6	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S6	X	X	1
P4.5/P4MAP5/S7	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S7	X	X	1
P4.6/P4MAP6/S8	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S8	X	X	1
P4.7/P4MAP7/S9	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S9	X	X	1

(1) X = don't care

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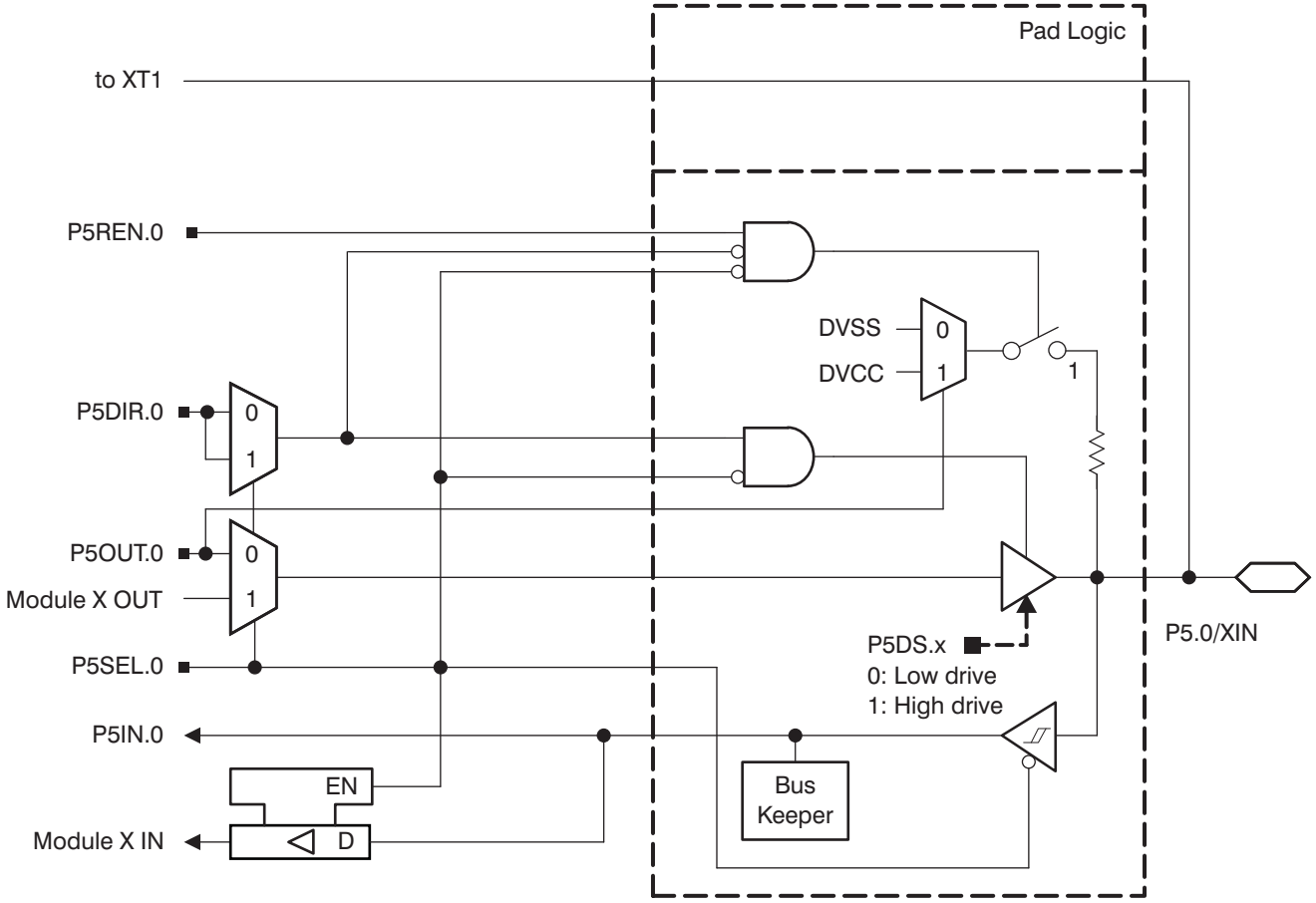
Port P5, P5.0, Input/Output With Schmitt Trigger



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Port P5, P5.1, Input/Output With Schmitt Trigger

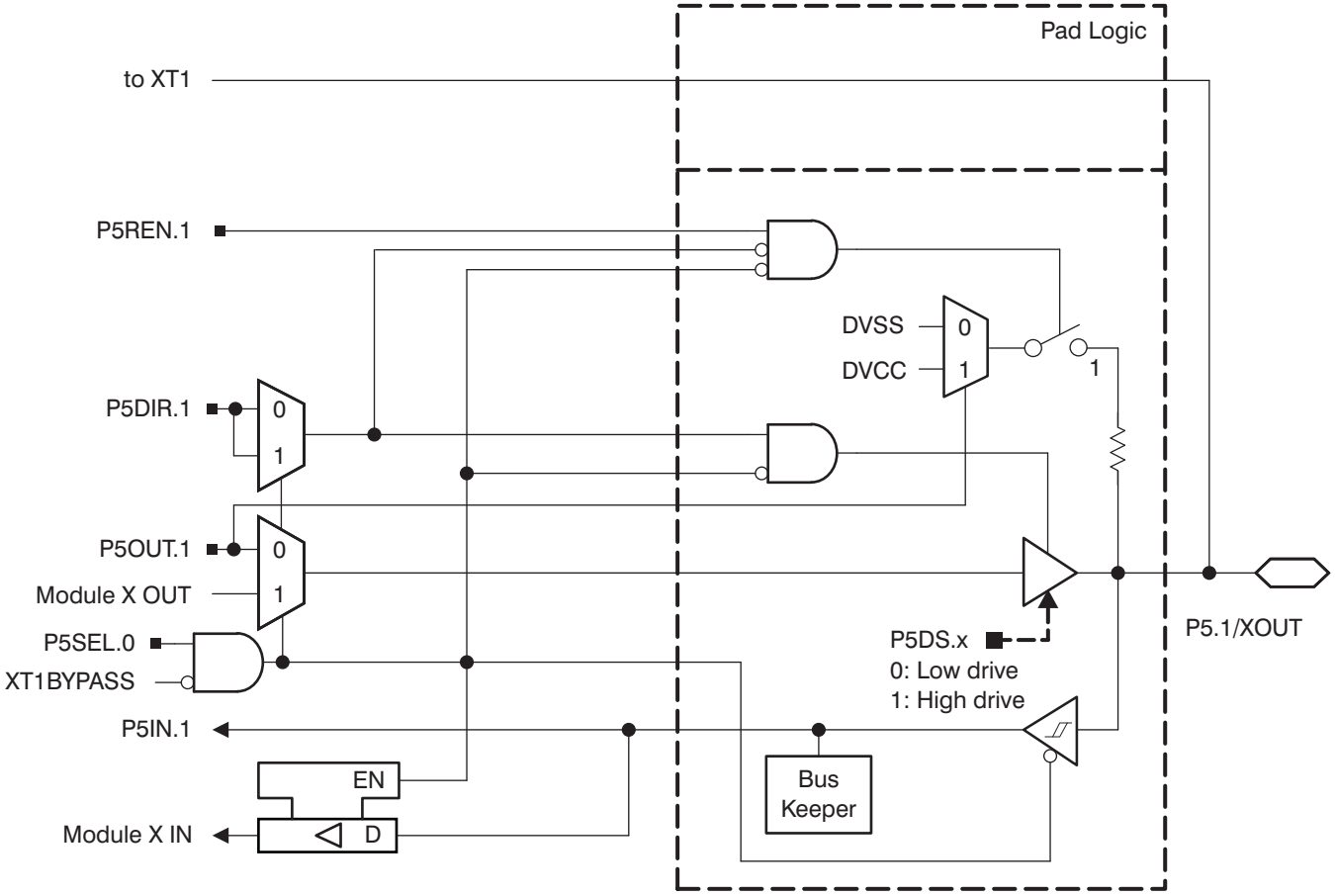

Table 54. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P5DIR.x	P5SEL.0	P5SEL.1	XT1BYPASS
P5.0/XIN	0	P5.0 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode[2]	X	1	X	0
		XIN bypass mode[2]	X	1	X	1
P5.1/XOUT	1	P5.1 (I/O)	I: 0; O: 1	0	X	X
		XOUT crystal mode[3]	X	1	X	0
		P5.1 (I/O)[3]	X	1	X	1

(1) X = don't care
(2) Setting P5SEL.0 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.0 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.0 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.1 can be used as general-purpose I/O.

Port P5, P5.2 to P5.4, Input/Output With Schmitt Trigger (CC430F613x and CC430F612x only)

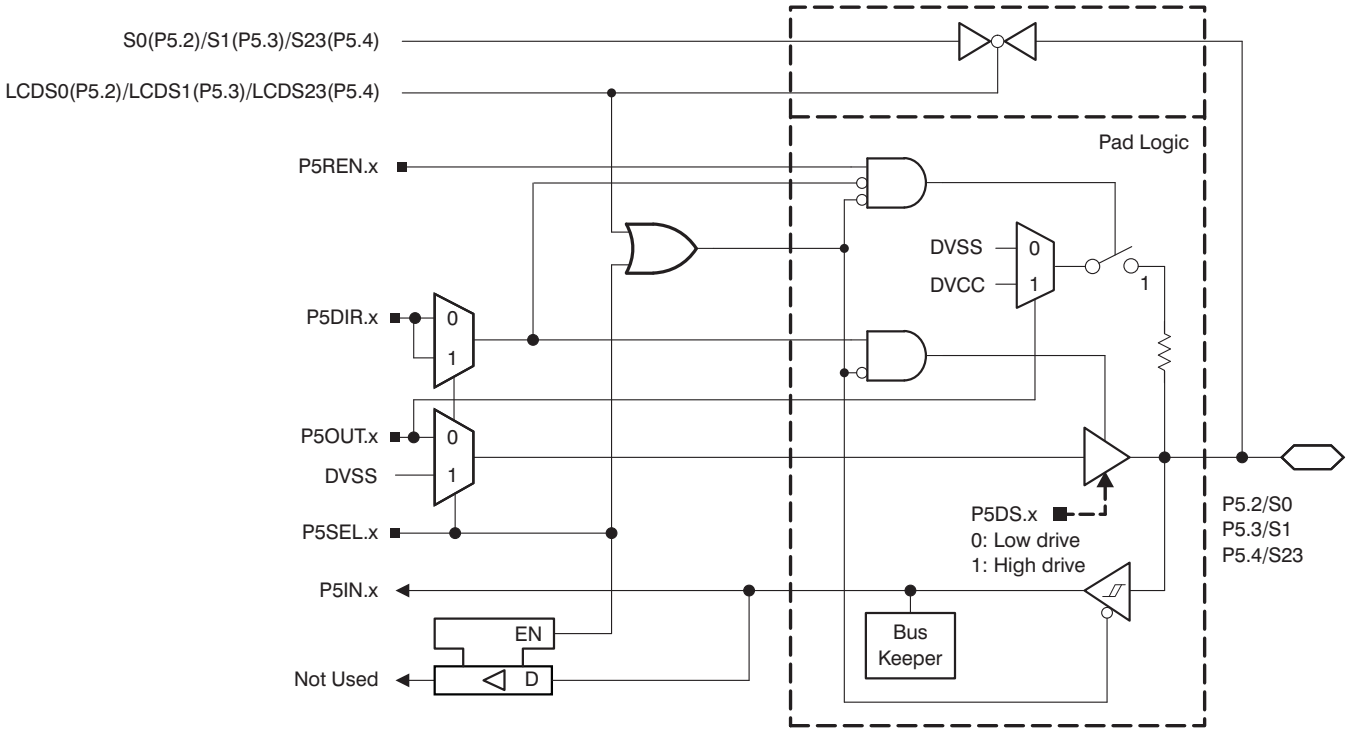

Table 55. Port P5 (P5.2 to P5.3) Pin Functions (CC430F613x and CC430F612x only)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P5DIR.x	P5SEL.x	LCDS0...1
P5.2/S0	2	P5.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S0	X	X	1
P5.3/S1	3	P5.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S1	X	X	1

(1) X = don't care

Table 56. Port P5 (P5.4) Pin Functions (CC430F613x and CC430F612x only)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P5DIR.x	P5SEL.x	LCDS23
P5.4/S23	4	P5.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S23	X	X	1

(1) X = don't care

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Port P5, P5.5 to P5.7, Input/Output With Schmitt Trigger (CC430F613x and CC430F612x only)

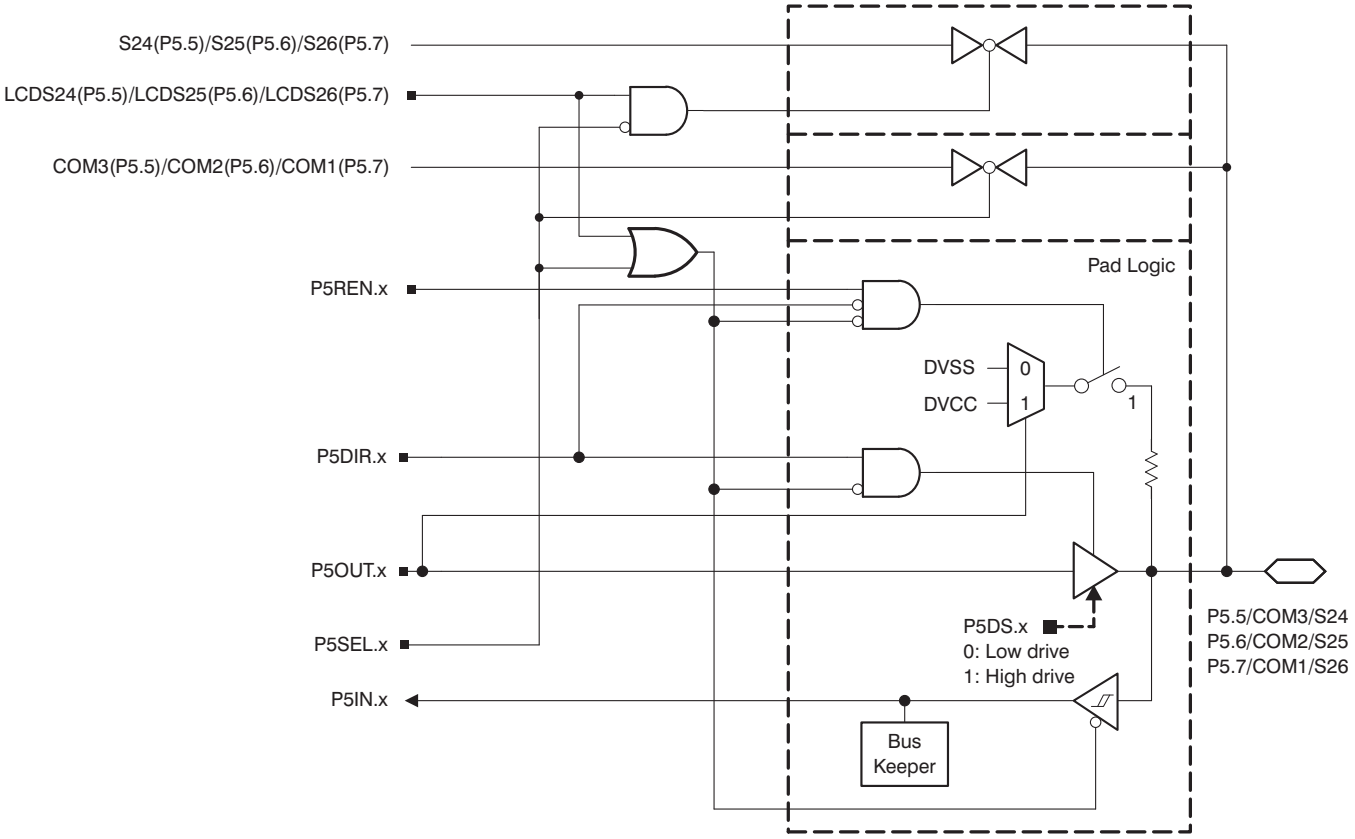
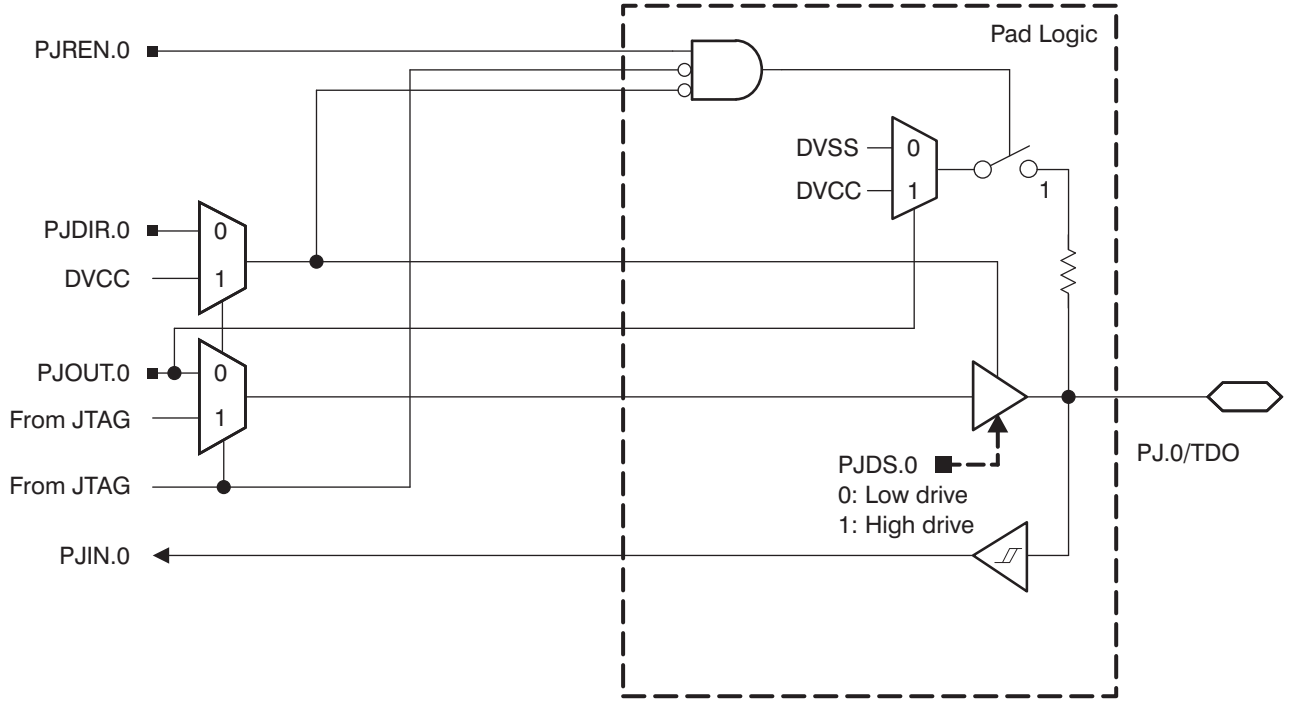


Table 57. Port P5 (P5.5 to P5.7) Pin Functions (CC430F613x and CC430F612x only)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P5DIR.x	P5SEL.x	LCDS24...26
P5.5/COM3/S24	5	P5.5 (I/O)	I: 0; O: 1	0	0
		COM3[2]	X	1	X
		S24[2]	X	0	1
P5.6/COM2/S25	6	P5.6 (I/O)	I: 0; O: 1	0	0
		COM2[2]	X	1	X
		S25[2]	X	0	1
P5.7/COM1/S26	7	P5.7 (I/O)	I: 0; O: 1	0	0
		COM1[2]	X	1	X
		S26[2]	X	0	1

(1) X = don't care
(2) Setting P5SEL.x bit disables the output driver as well as the input Schmitt trigger.

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

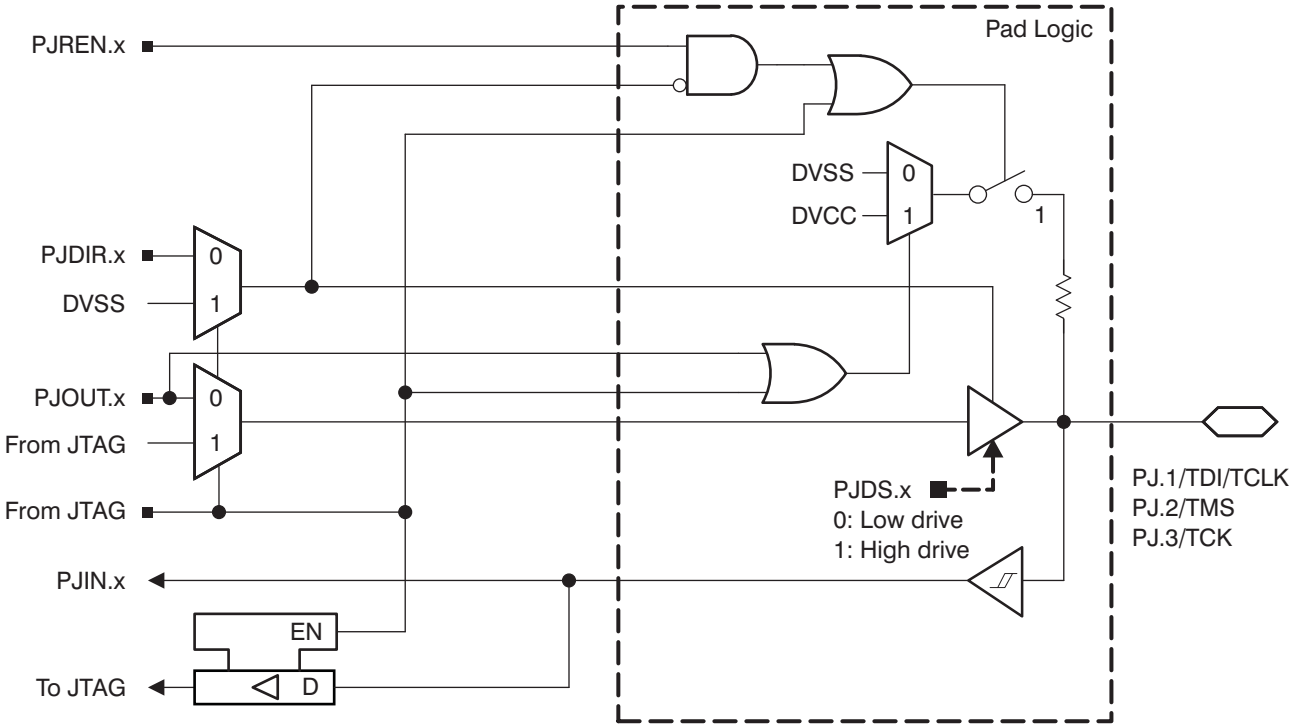


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Table 58. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)[2]	I: 0; O: 1
		TDO[3]	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)[2]	I: 0; O: 1
		TDI/TCLK[3] [4]	X
PJ.2/TMS	2	PJ.2 (I/O)[2]	I: 0; O: 1
		TMS[3] [4]	X
PJ.3/TCK	3	PJ.3 (I/O)[2]	I: 0; O: 1
		TCK[3] [4]	X

(1) X = don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

Device Descriptor Structures

Table 59 lists the content of the device descriptor tag-length-value (TLV) structure for CC430F613x and CC430F513x device types.

Table 60 lists the content of the device descriptor tag-length-value (TLV) structure for CC430F612x device types.

Table 59. Device Descriptor Table (CC430F613x and CC430F513x)

	Description	Address	Size bytes	'F6137	'F6135	'F5137	'F5135	'F5133
				Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	61h	61h	51h	51h	51h
	Device ID	01A05h	1	37h	35h	37h	35h	33h
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	11h	11h	11h	11h	11h
	ADC12 Calibration length	01A15h	1	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit	per unit	per unit
	ADC 1.5V Reference Temp. Sensor 30°C	01A1Ah	2	per unit	per unit	per unit	per unit	per unit
	ADC 1.5V Reference Temp. Sensor 85°C	01A1Ch	2	per unit	per unit	per unit	per unit	per unit
	ADC 2.0V Reference Temp. Sensor 30°C	01A1Eh	2	per unit	per unit	per unit	per unit	per unit
	ADC 2.0V Reference Temp. Sensor 85°C	01A20h	2	per unit	per unit	per unit	per unit	per unit
	ADC 2.5V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit	per unit	per unit
	ADC 2.5V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit	per unit	per unit
REF Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h	06h	06h

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Table 59. Device Descriptor Table (CC430F613x and CC430F513x) (continued)

	Description	Address	Size bytes	'F6137	'F6135	'F5137	'F5135	'F5133
				Value	Value	Value	Value	Value
	1.5V Reference Factor	01A28h	2	per unit	per unit	per unit	per unit	per unit
	2.0V Reference Factor	01A2Ah	2	per unit	per unit	per unit	per unit	per unit
	2.5V Reference Factor	01A2Ch	2	per unit	per unit	per unit	per unit	per unit
Peripheral Descriptor (PD)	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	57h	57h	55h	55h	55h
	Peripheral Descriptors	01A30h	PD Length	...	...	...	...	...

Table 60. Device Descriptor Table (CC430F612x)

	Description	Address	Size bytes	'F6127	'F6126	'F6125
				Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit
	Device ID	01A04h	1	61h	61h	61h
	Device ID	01A05h	1	27h	26h	25h
	Hardware revision	01A06h	1	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit
Empty Descriptor	Empty Tag	01A14h	1	05h	05h	05h
	Empty Tag Length	01A15h	1	10h	10h	10h
		01A16h	16	undefined	undefined	undefined
REF Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h
	1.5V Reference Factor	01A28h	2	per unit	per unit	per unit
	2.0V Reference Factor	01A2Ah	2	per unit	per unit	per unit
	2.5V Reference Factor	01A2Ch	2	per unit	per unit	per unit
Peripheral Descriptor (PD)	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	55h	55h	55h
	Peripheral Descriptors	01A30h	PD Length	...	...	...

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REVISION HISTORY

REVISION	DESCRIPTION
SLAS554	Product Preview data sheet release
SLAS554A	Product Preview data sheet updated with electrical parameters
SLAS554B	Production Data release data sheet for CC430F51xx devices. CC430F61xx devices are Product Preview.
SLAS554C	Production Data release data sheet for CC430F61xx devices.
SLAS554D	Added correct termination of LCDCAP/R33 if not used. Corrected unit in *Frequency Synthesizer Characteristics* from "ms" to "µs".
SLAS554E	Removed RFRXIFG (14) and RFTXIFG (15) from *DMA Trigger Assignments* table Corrected USCI control register location in *Peripheral File Map*. Changed T_{stg} maximum limit from 105°C to 150°C in *Absolute Maximum Ratings*. Replaced values for "Hardware revision" and "Firmware revision" in *Device Descriptor Tables* with "per unit".
SLAS554F	Table 3, Corrected USCI signal names for pins 5 and 6 (descriptions unchanged). 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage, ADC12 linearity parameter test conditions revised. 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage, linearity parameters with internal reference added.
SLAS554G	Table 11, Changed SYSRSTIV interrupt event at 1Ch to Reserved. Recommended Operating Conditions, Added test conditions for typical characteristics. Recommended Operating Conditions, Added note regarding relationship between SVS and MIN VCC. DCO Frequency, Added note (1). Flash Memory, Changed I_{ERASE} and I_{MERASE} values.
SLAS554H	Applications, Added section. Recommended Operating Conditions, Added note about C_{VCORE} tolerance. Peripheral File Map, Removed CRCRESR and CRCDIRB registers (do not apply).

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC430F5133IRGZ	ACTIVE	VQFN	RGZ	48	52	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		CC430 F5133	Samples
CC430F5133IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5133	Samples
CC430F5133IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5133	Samples
CC430F5135IRGZ	ACTIVE	VQFN	RGZ	48	52	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5135	Samples
CC430F5135IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5135	Samples
CC430F5135IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5135	Samples
CC430F5137IRGZ	ACTIVE	VQFN	RGZ	48	52	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5137	Samples
CC430F5137IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5137	Samples
CC430F5137IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430 F5137	Samples
CC430F6125IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6125	Samples
CC430F6125IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6125	Samples
CC430F6126IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6126	Samples
CC430F6126IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6126	Samples
CC430F6127IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6127	Samples
CC430F6127IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6127	Samples
CC430F6135IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6135	Samples
CC430F6135IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6135	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC430F6137IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6137	Samples
CC430F6137IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC430F6137	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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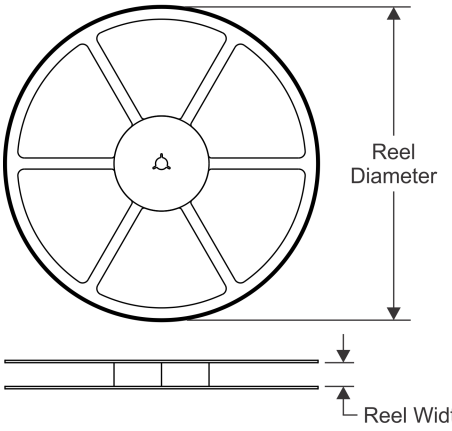
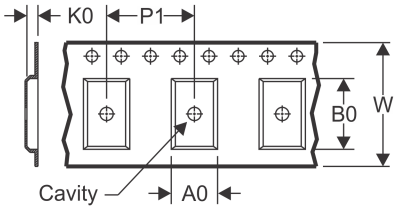
TAPE AND REEL INFORMATION

REEL DIMENSIONS

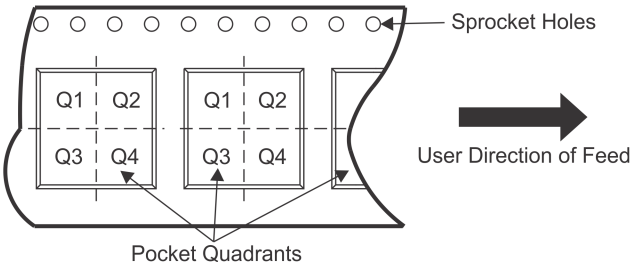


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

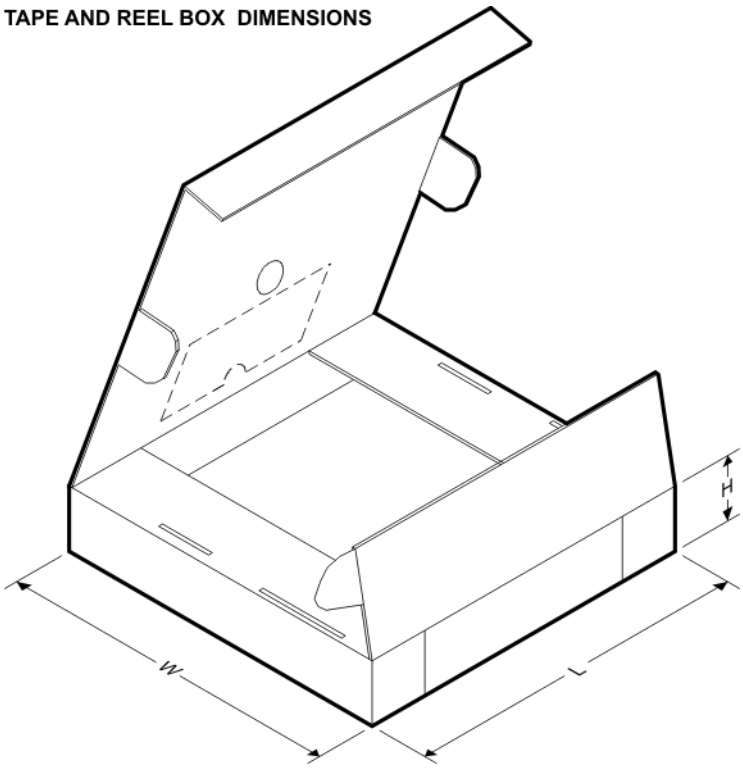
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC430F5133IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC430F5133IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC430F5135IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC430F5135IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC430F5137IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC430F5137IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC430F6125IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
CC430F6126IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
CC430F6127IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
CC430F6135IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
CC430F6137IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

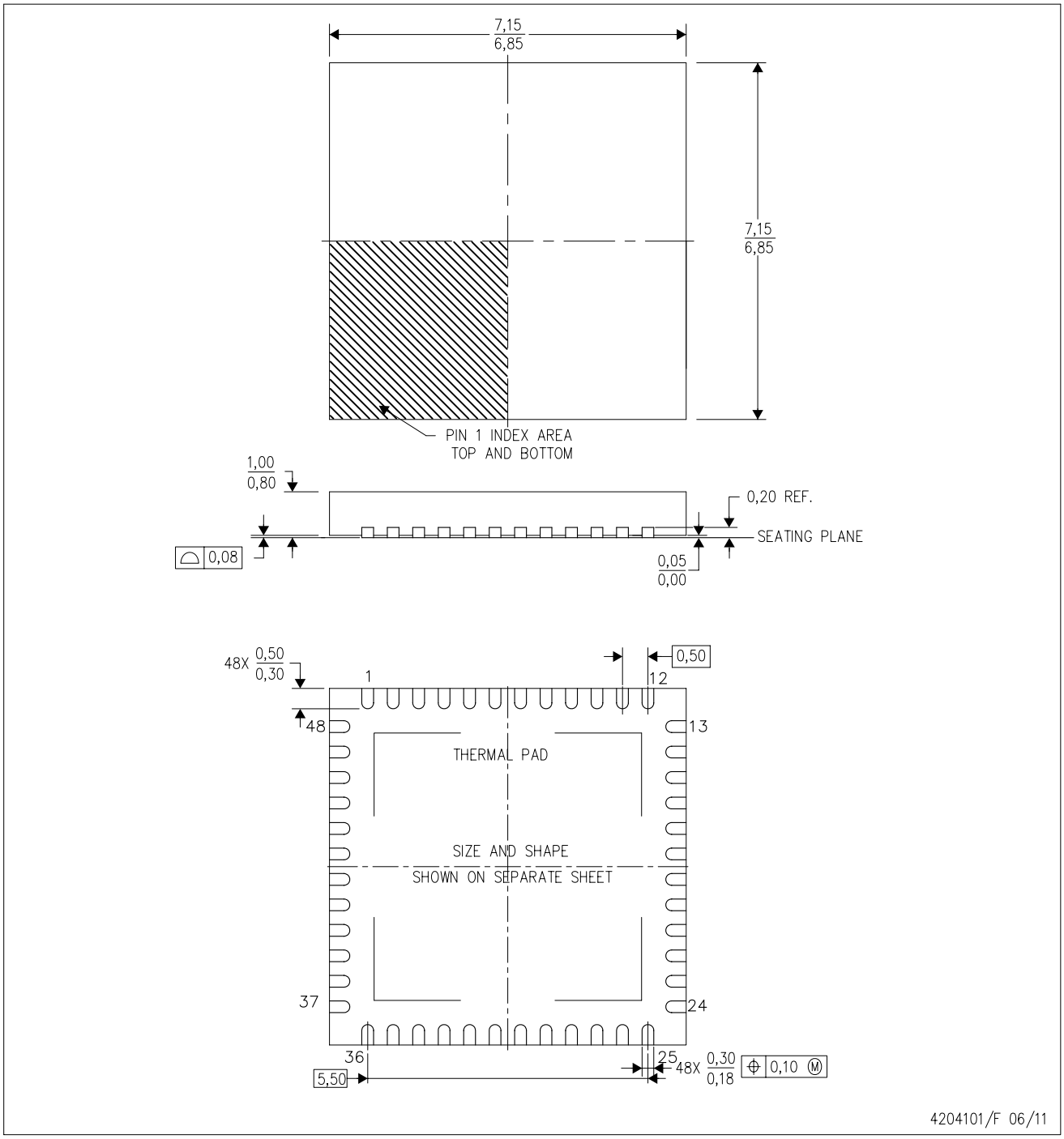
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC430F5133IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CC430F5133IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
CC430F5135IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CC430F5135IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
CC430F5137IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CC430F5137IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
CC430F6125IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
CC430F6126IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
CC430F6127IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
CC430F6135IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
CC430F6137IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

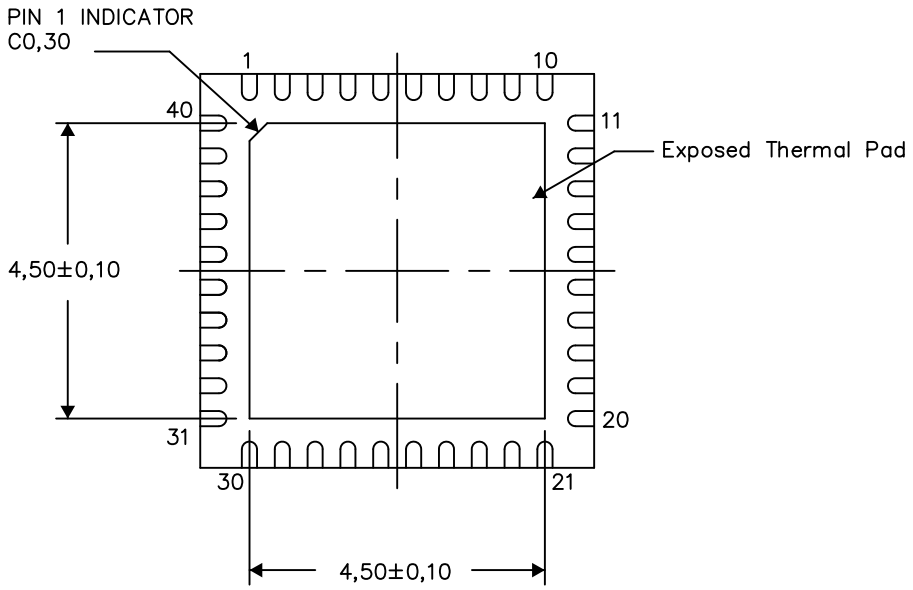
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



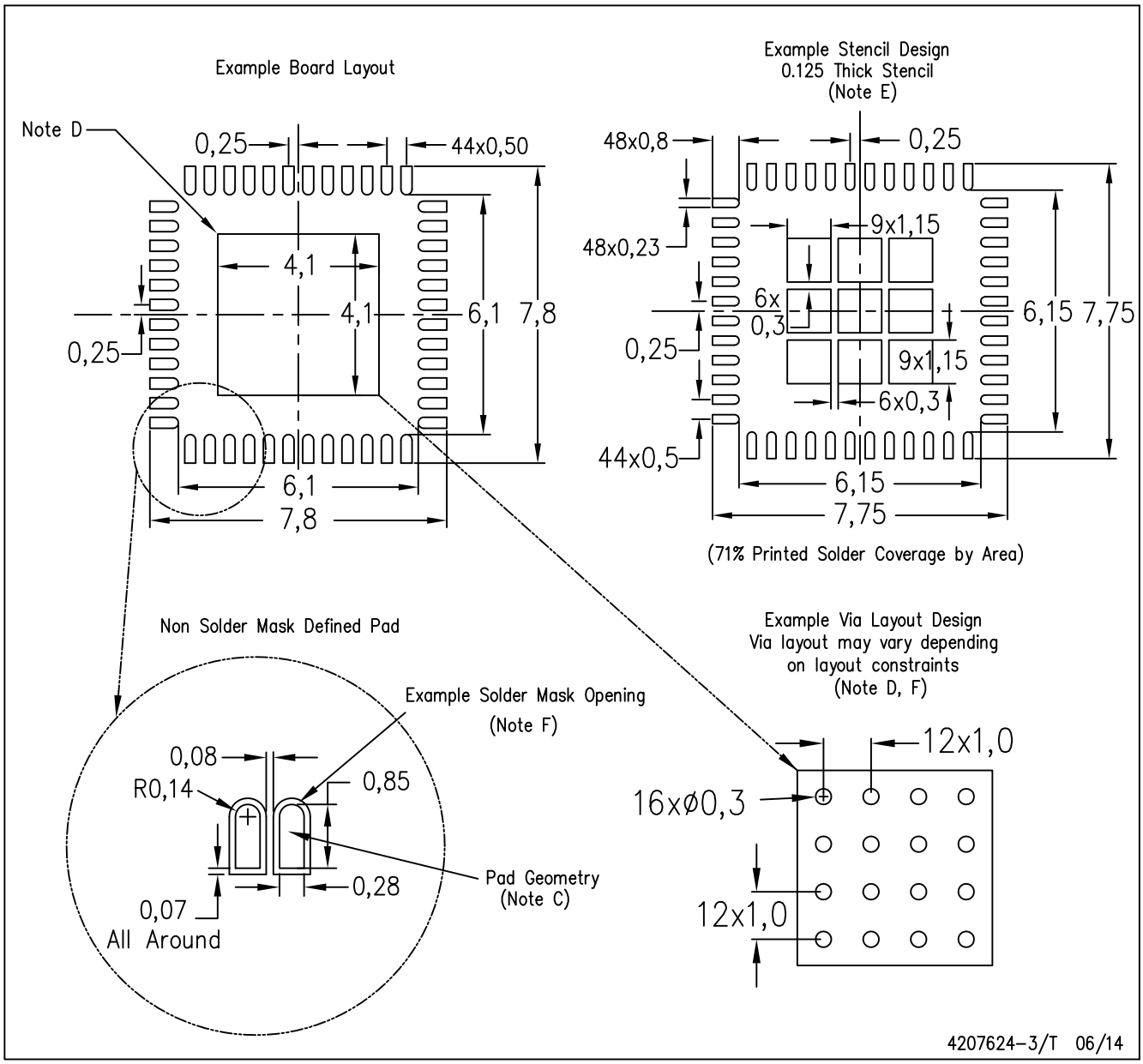
Bottom View

Exposed Thermal Pad Dimensions

4206355–4/W 06/14

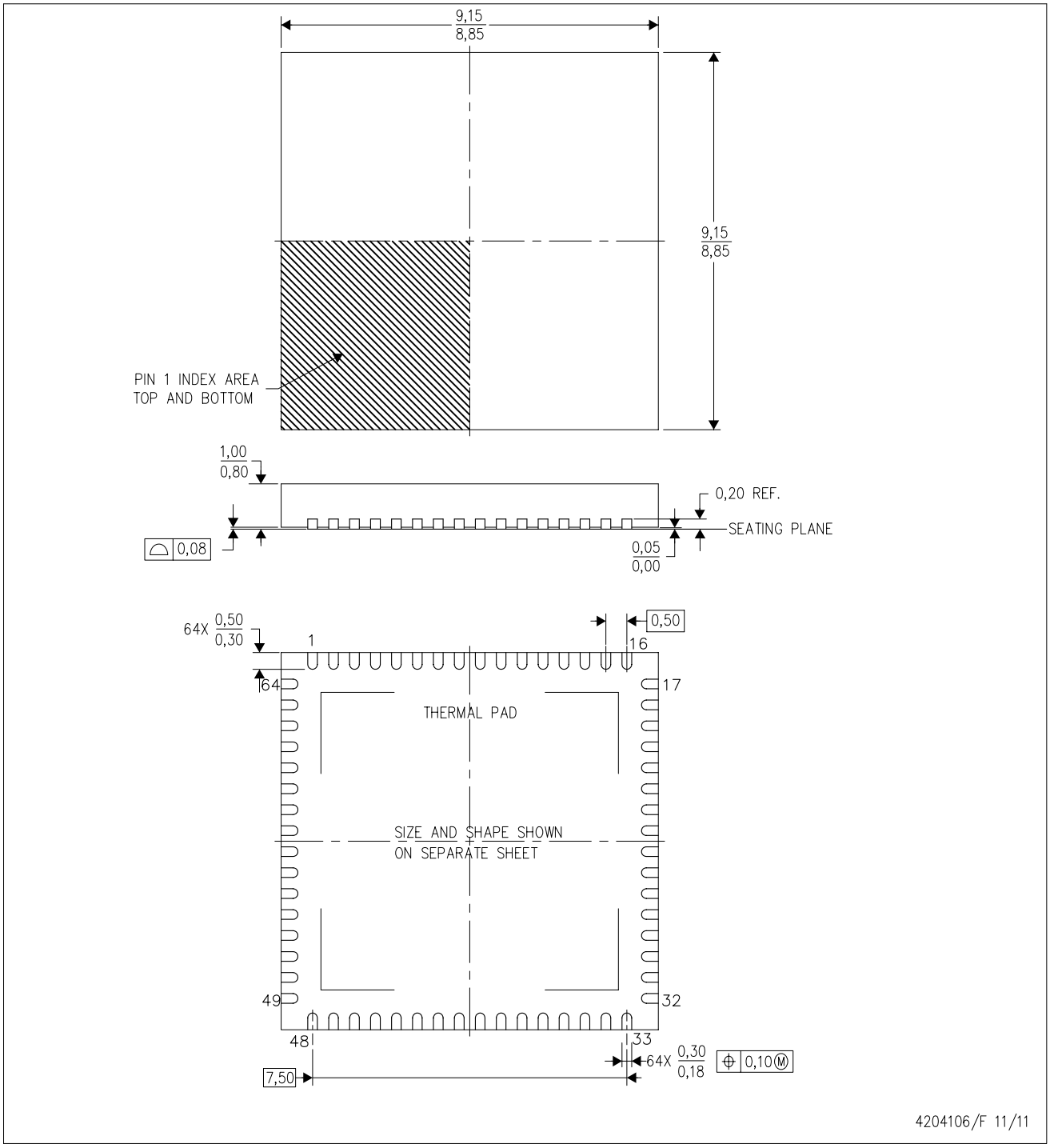
NOTES: A. All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

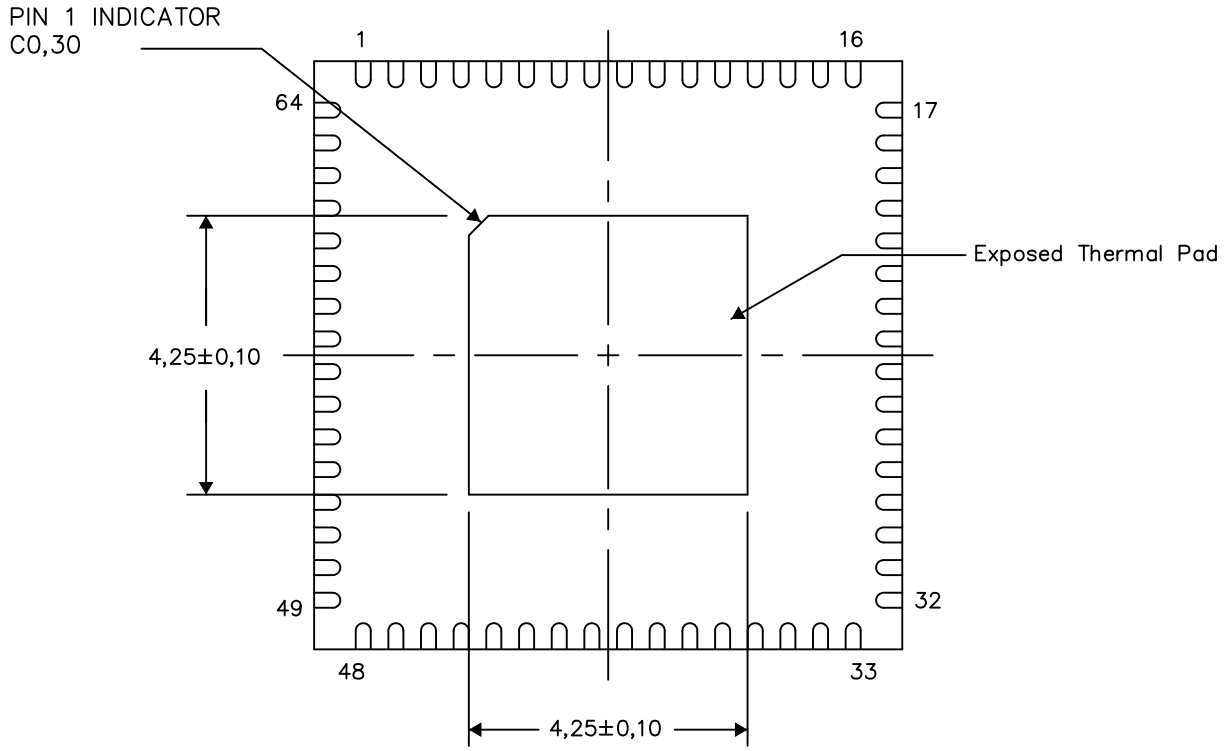
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



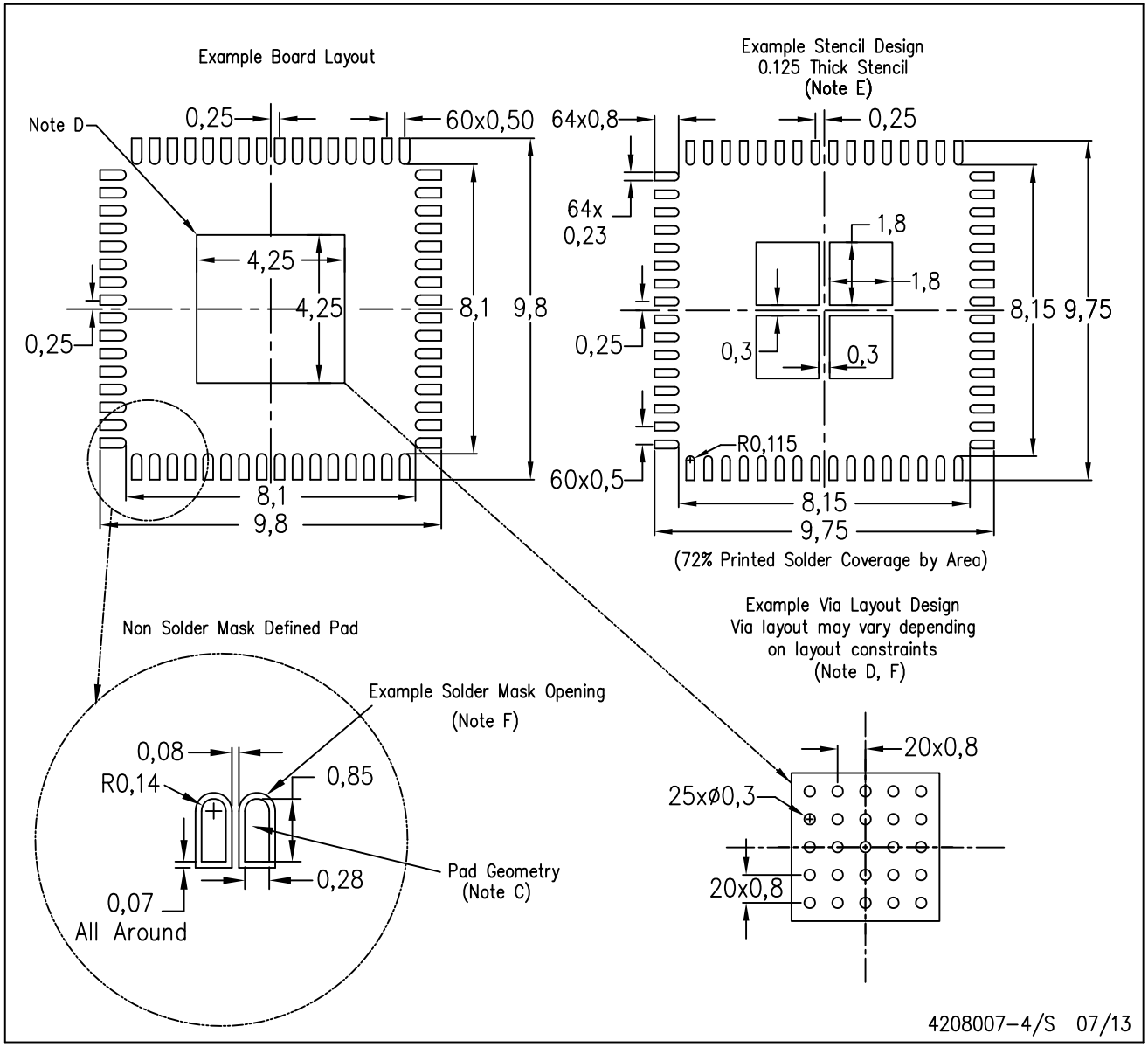
Bottom View

Exposed Thermal Pad Dimensions

4206192–3/AC 10/13

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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