NEC

MOS INTEGRATED CIRCUIT

μPD703100A-33, 703100A-40, 703101A-33, 703102A-33

V850E/MS1™
32/16-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD703101A-33 and μPD703102A-33 are members of the V850 Family™ of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU core, ROM, RAM, interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The μPD703100A-33 and μPD703100A-40 are ROM-less versions of the μPD703101A-33 and μPD703102A-33 products.

The μPD703100-33, μPD703100-40, μPD703101-33, and μPD703102-33 are also available as products having a 5.0-V power supply for external pins.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MS1 User's Manual Hardware: U12688E
V850E/MS1 User's Manual Architecture: U12197E

FEATURES

- Number of instructions: 81
- Minimum instruction execution time 25 ns (@ 40-MHz operation) ·····μPD703100A-40
  30 ns (@ 33-MHz operation) ·····μPD703100A-33, 703101A-33, 703102A-33
- General registers 32 bits × 32
- Instruction set optimized for control applications
- Internal memory ROM: None (μPD703100A-33, 703100A-40), 96 Kbytes (μPD703101A-33), 128 Kbytes (μPD703102A-33)
  RAM: 4 Kbytes
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power saving functions

APPLICATIONS

- Office automation equipment: printers, facsimile machines, PPCs, etc.
- Multimedia equipment: digital still cameras, video printers, etc.
- Consumer equipment: single-lens reflex cameras, etc.
- Industrial equipment: motor controllers, NC machine tools, etc.

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The mark ★ shows major revised points.

★ ORDERING INFORMATION

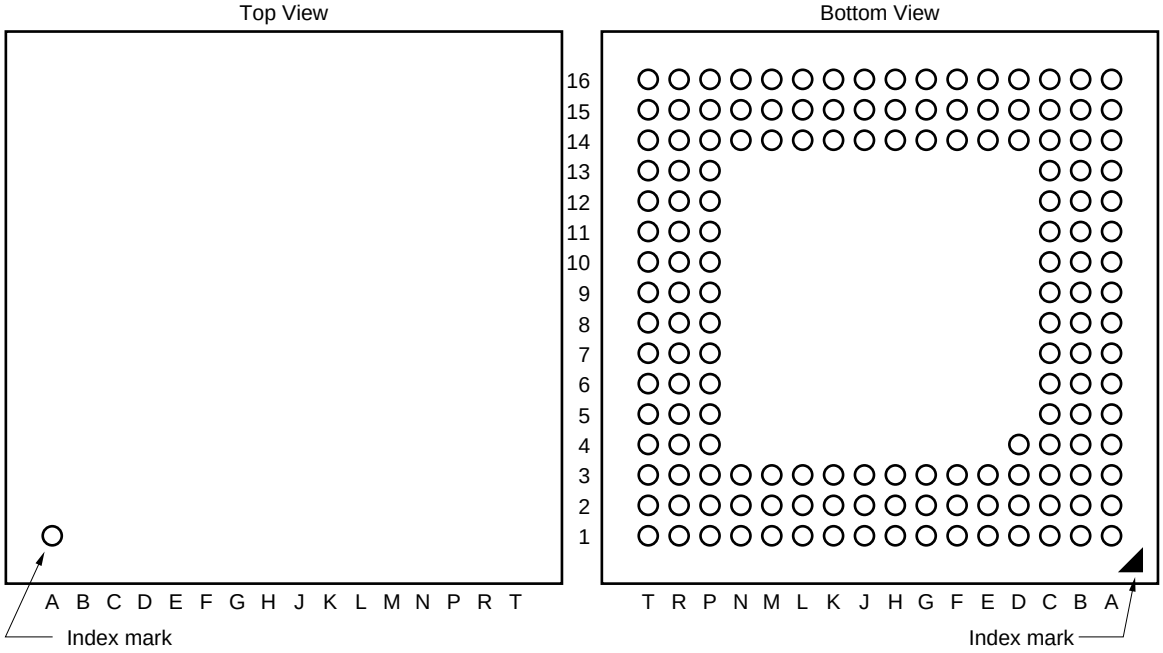
Part Number	Package	Maximum Operating Frequency	Internal ROM
μPD703100AF1-33-FA1	157-pin plastic FBGA (14 × 14 mm)	33 MHz	None
μPD703100AF1-40-FA1	157-pin plastic FBGA (14 × 14 mm)	40 MHz	None
μPD703100AGJ-33-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	33 MHz	None
μPD703100AGJ-40-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	40 MHz	None
μPD703101AF1-33-×××-FA1	157-pin plastic FBGA (14 × 14 mm)	33 MHz	96 Kbytes
μPD703101AGJ-33-×××-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	33 MHz	96 Kbytes
μPD703102AF1-33-×××-FA1	157-pin plastic FBGA (14 × 14 mm)	33 MHz	128 Kbytes
μPD703102AGJ-33-×××-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	33 MHz	128 Kbytes

Remark ××× indicates ROM code suffix.

PIN CONFIGURATION (Top view)

157-pin plastic FGBA (14 × 14 mm)

- μPD703100AF1-33-FA1
- μPD703100AF1-40- FA1
- μPD703101AF1-33-×××-FA1
- μPD703102AF1-33-×××-FA1



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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	—	B1	INTP103/$\overline{\text{DMARQ3}}$/P07	C1	INTP101/$\overline{\text{DMARQ1}}$/P05
A2	D0/P40	B2	D1/P41	C2	INTP102/$\overline{\text{DMARQ2}}$/P06
A3	D2/P42	B3	D3/P43	C3	V_{SS}
A4	D4/P44	B4	D5/P45	C4	V_{SS}
A5	D6/P46	B5	D7/P47	C5	HV_{DD}
A6	D8/P50	B6	D9/P51	C6	V_{SS}
A7	D10/P52	B7	D11/P53	C7	D12/P54
A8	D13/P55	B8	D14/P56	C8	D15/P57
A9	A0/PA0	B9	A1/PA1	C9	HV_{DD}
A10	A2/PA2	B10	A3/PA3	C10	A4/PA4
A11	A5/PA5	B11	A6/PA6	C11	A7/PA7
A12	A8/PB0	B12	A9/PB1	C12	V_{SS}
A13	A10/PB2	B13	A11/PB3	C13	A12/PB4
A14	A13/PB5	B14	A14/PB6	C14	A18/P62
A15	A15/PB7	B15	A17/P61	C15	A19/P63
A16	—	B16	A16/P60	C16	—

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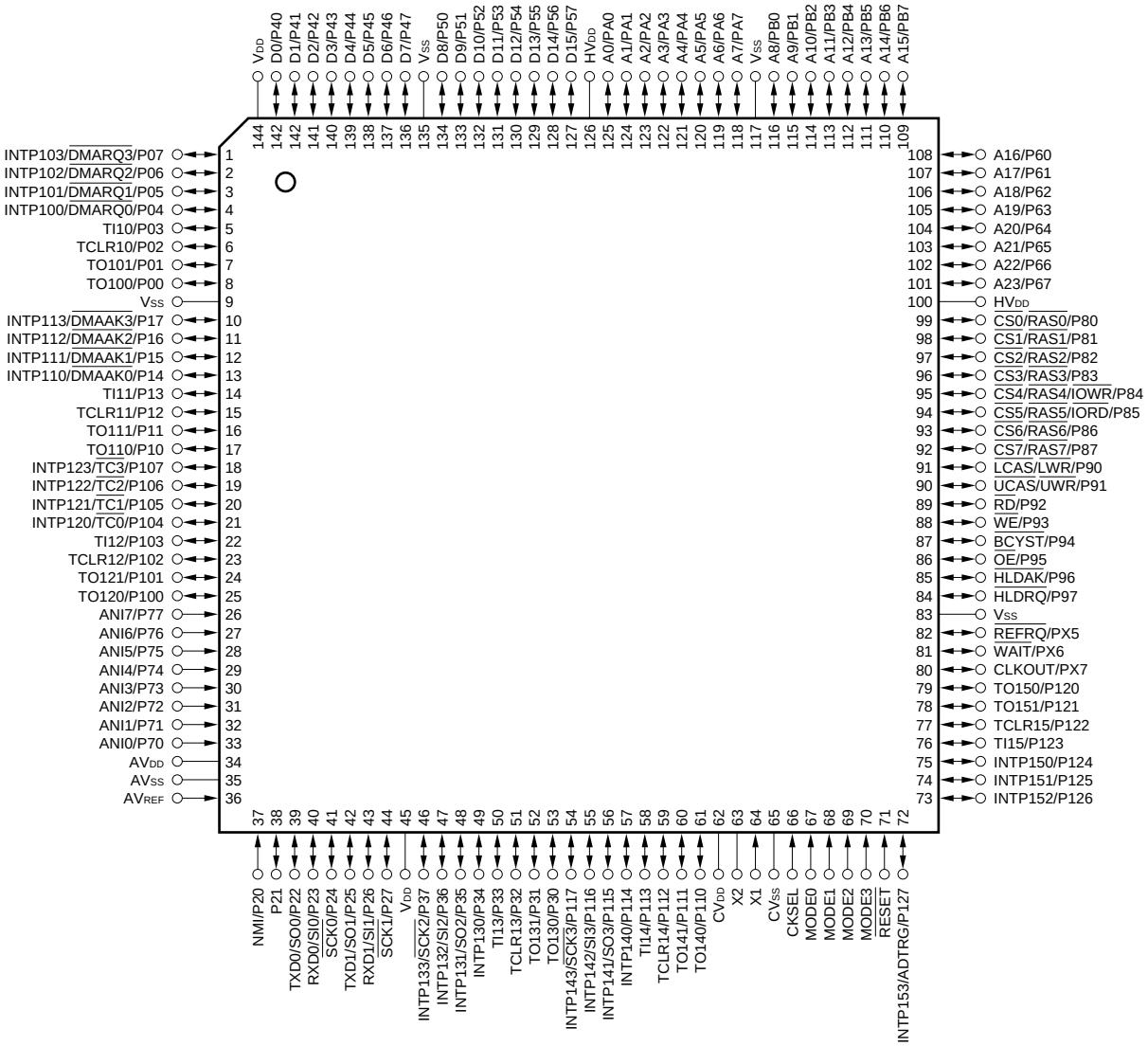
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
D1	TI10/P03	K1	TI12/P103	P14	$\overline{\text{RESET}}$
D2	INTP100/$\overline{\text{DMARQ0}}$/P04	K2	INTP120/$\overline{\text{TC0}}$/P104	P15	INTP151/P125
D3	HV_{DD}	K3	INTP121/$\overline{\text{TC1}}$/P105	P16	INTP150/P124
D4	—	K14	$\overline{\text{HLDAK}}$/P96	R1	AV_{SS}
D14	V_{SS}	K15	OE/P95	R2	ANI0/P70
D15	A21/P65	K16	$\overline{\text{BCYST}}$/P94	R3	P21
D16	A20/P64	L1	TO120/P100	R4	$\overline{\text{SCK0}}$/P24
E1	TO101/P01	L2	TO121/P101	R5	$\overline{\text{SCK1}}$/P27
E2	TCLR10/P02	L3	TCLR12/P102	R6	INTP132/SI2/P36
E3	V_{SS}	L14	V_{SS}	R7	TI13/P33
E14	HV_{DD}	L15	$\overline{\text{REFRQ}}$/PX5	R8	TO130/P30
E15	A23/P67	L16	$\overline{\text{HLDRQ}}$/P97	R9	INTP141/SO3/P115
E16	A22/P66	M1	ANI5/P75	R10	TCLR14/P112
F1	INTP113/$\overline{\text{DMAAK3}}$/P17	M2	ANI6/P76	R11	TO140/P110
F2	TO100/P00	M3	ANI7/P77	R12	MODE0
F3	V_{DD}	M14	TO150/P120	R13	MODE1
F14	$\overline{\text{CS2}}$/$\overline{\text{RAS2}}$/P82	M15	$\overline{\text{WAIT}}$/PX6	R14	MODE2
F15	$\overline{\text{CS1}}$/$\overline{\text{RAS1}}$/P81	M16	CLKOUT/PX7	R15	INTP153/ADTRG/P127
F16	$\overline{\text{CS0}}$/$\overline{\text{RAS0}}$/P80	N1	ANI2/P72	R16	INTP152/P126
G1	INTP110/$\overline{\text{DMAAK0}}$/P14	N2	ANI3/P73	T1	—
G2	INTP111/$\overline{\text{DMAAK1}}$/P15	N3	ANI4/P74	T2	AV_{REF}
G3	INTP112/$\overline{\text{DMAAK2}}$/P16	N14	TI15/P123	T3	NMI/P20
G14	$\overline{\text{CS5}}$/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$/P85	N15	TCLR15/P122	T4	RXD0/SI0/P23
G15	$\overline{\text{CS4}}$/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$/P84	N16	TO151/P121	T5	RXD1/SI1/P26
G16	$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$/P83	P1	AV_{DD}	T6	INTP131/SO2/P35
H1	TO111/P11	P2	ANI1/P71	T7	TCLR13/P32
H2	TCLR11/P12	P3	TXD0/SO0/P22	T8	INTP143/$\overline{\text{SCK3}}$/P117
H3	TI11/P13	P4	TXD1/SO1/P25	T9	INTP140/P114
H14	$\overline{\text{LCAS}}$/$\overline{\text{LWR}}$/P90	P5	V_{DD}	T10	CV_{DD}
H15	$\overline{\text{CS7}}$/$\overline{\text{RAS7}}$/P87	P6	INTP133/$\overline{\text{SCK2}}$/P37	T11	X2
H16	$\overline{\text{CS6}}$/$\overline{\text{RAS6}}$/P86	P7	INTP130/P34	T12	X1
J1	INTP122/$\overline{\text{TC2}}$/P106	P8	TO131/P31	T13	CV_{SS}
J2	INTP123/$\overline{\text{TC3}}$/P107	P9	INTP142/SI3/P116	T14	MODE3
J3	TO110/P10	P10	TI14/P113	T15	—
J14	$\overline{\text{WE}}$/P93	P11	TO141/P111	T16	—
J15	$\overline{\text{RD}}$/P92	P12	CKSEL	—	—
J16	$\overline{\text{UCAS}}$/$\overline{\text{UWR}}$/P91	P13	HV_{DD}	—	—

Remark Leave the A1, A16, C16, D4, T1, T15, and T16 pins open.

144-pin plastic LQFP (fine pitch) (20 × 20 mm)

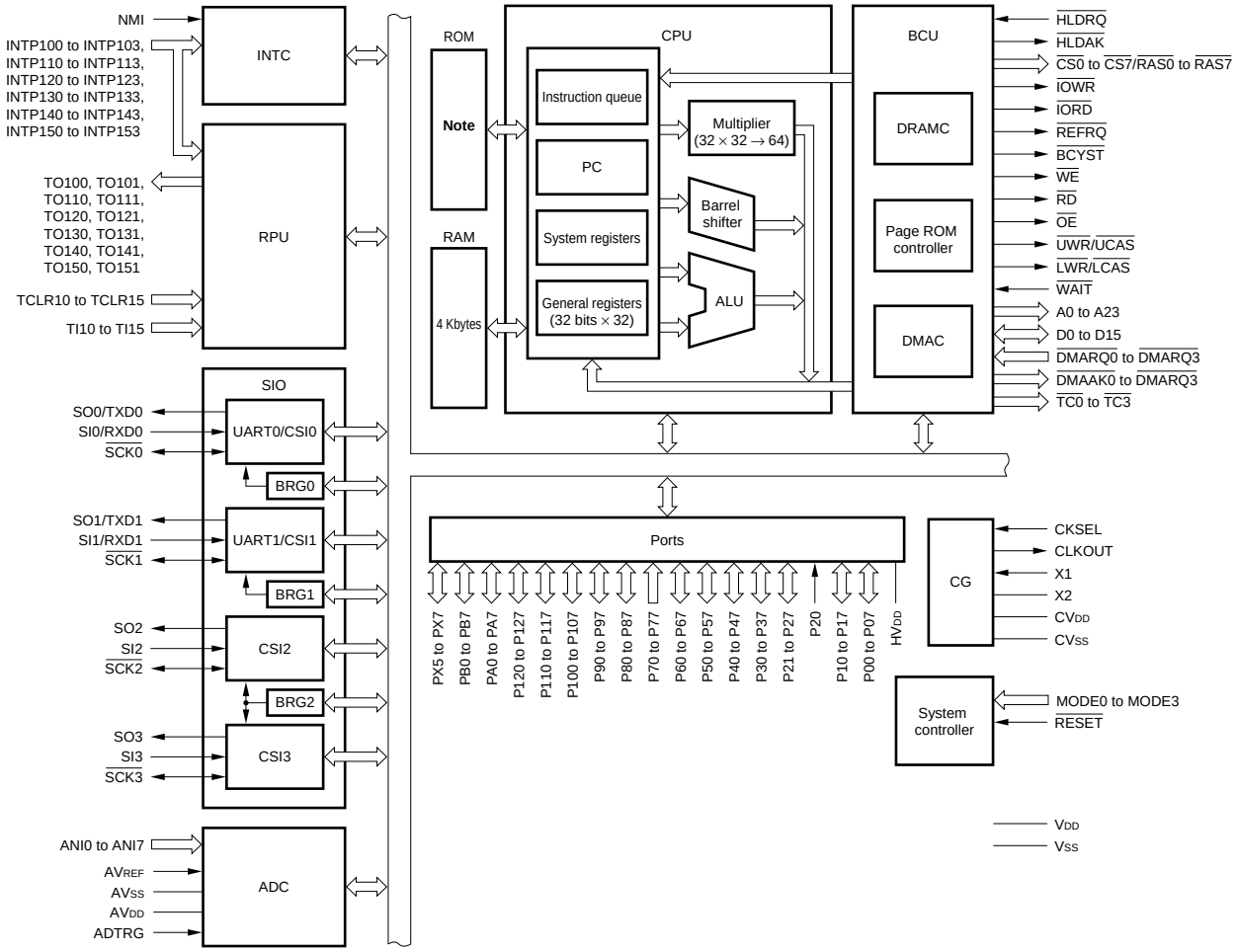
- μPD703100AGJ-33-8EU
- μPD703100AGJ-40-8EU
- μPD703101AGJ-33-×××-8EU
- μPD703102AGJ-33-×××-8EU



PIN IDENTIFICATION

A0 to A23:	Address Bus	P50 to P57:	Port 5
ADTRG:	AD Trigger Input	P60 to P67:	Port 6
ANI0 to ANI7:	Analog Input	P70 to P77:	Port 7
AV_{DD}:	Analog Power Supply	P80 to P87:	Port 8
AV_{REF}:	Analog Reference Voltage	P90 to P97:	Port 9
AV_{SS}:	Analog Ground	P100 to P107:	Port 10
$\overline{BCYST}$:	Bus Cycle Start Timing	P110 to P117:	Port 11
CKSEL:	Clock Generator Operating Mode Select	P120 to P127:	Port 12
CLKOUT:	Clock Output	PA0 to PA7:	Port A
$\overline{CS0}$ to $\overline{CS7}$:	Chip Select	PB0 to PB7:	Port B
CV_{DD}:	Clock Generator Power Supply	PX5 to PX7:	Port X
CV_{SS}:	Clock Generator Ground	$\overline{RAS0}$ to $\overline{RAS7}$:	Row Address Strobe
D0 to D15:	Data Bus	$\overline{RD}$:	Read
$\overline{DMAAK0}$ to $\overline{DMAAK3}$:	DMA Acknowledge	$\overline{REFRQ}$:	Refresh Request
$\overline{DMARQ0}$ to $\overline{DMARQ3}$:	DMA Request	$\overline{RESET}$:	Reset
$\overline{HLDAK}$:	Hold Acknowledge	RXD0, RXD1:	Receive Data
$\overline{HLDRQ}$:	Hold Request	$\overline{SCK0}$ to $\overline{SCK3}$:	Serial Clock
HV_{DD}:	Power Supply for External Pins	SI0 to SI3:	Serial Input
INTP100 to INTP103,	Interrupt Request from Peripherals	SO0 to SO3:	Serial Output
INTP110 to INTP113,		$\overline{TC0}$ to $\overline{TC3}$:	Terminal Count Signal
INTP120 to INTP123,		TCLR10 to TCLR15:	Timer Clear
INTP130 to INTP133,		TI10 to TI15:	Timer Input
INTP140 to INTP143,		TO100, TO101,	Timer Output
INTP150 to INTP153:		TO110, TO111,	
$\overline{IORD}$:	I/O Read Strobe	TO120, TO121,	
$\overline{IOWR}$:	I/O Write Strobe	TO130, TO131,	
$\overline{LCAS}$:	Lower Column Address Strobe	TO140, TO141,	
$\overline{LWR}$:	Lower Write Strobe	TO150, TO151:	
MODE0 to MODE3:	Mode	TXD0, TXD1:	Transmit Data
NMI:	Non-Maskable Interrupt Request	$\overline{UCAS}$:	Upper Column Address Strobe
$\overline{OE}$:	Output Enable	$\overline{UWR}$:	Upper Write Strobe
P00 to P07:	Port 0	V_{DD}:	Power Supply for Internal Unit
P10 to P17:	Port 1	V_{SS}:	Ground
P20 to P27:	Port 2	$\overline{WAIT}$:	Wait
P30 to P37:	Port 3	$\overline{WE}$:	Write Enable
P40 to P47:	Port 4	X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



Note μPD703100A-33, 703100A-40: None
μPD703101A-33: 96 Kbytes (mask ROM)
μPD703102A-33: 128 Kbytes (mask ROM)

CONTENTS

1. DIFFERENCES AMONG PRODUCTS

Item \ Part Number	μPD703100				μPD703101		μPD703102		μPD70F3102	
	-33	-40	A-33	A-40	-33	A-33	-33	A-33	-33	A-33
Internal ROM	None				96 Kbytes (mask ROM)		128 Kbytes (mask ROM)		128 Kbytes (flash memory)	
Maximum operating frequency	33 MHz	40 MHz	33 MHz	40 MHz	33 MHz					
HV_{DD}	4.5 to 5.5 V		3.0 to 3.6 V		4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V
Operation mode										
Single-chip mode 0, 1	None				Provided					
Flash memory programming mode	None								Provided	
Flash memory programming pin	None								Provided (V_{PP})	
Electrical specifications	Current consumption differs (refer to the data sheet of each product).									
Package	144LQFP		144LQFP 157FBGA		144LQFP	144LQFP 157FBGA	144LQFP	144LQFP 157FBGA	144LQFP	144LQFP 157FBGA
Others	Noise tolerance and noise radiation will differ due to the differences in circuit scale and mask layout.									

Remark 144LQFP: 144-pin plastic LQFP (fine pitch) (20 × 20 mm)
157FBGA: 157-pin plastic FBGA (14 × 14 mm)

2. PIN FUNCTIONS

2.1 Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output mode can be specified in 1-bit units	TO100
P01			TO101
P02			TCLR10
P03			TI10
P04			INTP100/$\overline{\text{DMARQ0}}$
P05			INTP101/$\overline{\text{DMARQ1}}$
P06			INTP102/$\overline{\text{DMARQ2}}$
P07			INTP103/$\overline{\text{DMARQ3}}$
P10	I/O	Port 1 8-bit I/O port Input/output mode can be specified in 1-bit units	TO110
P11			TO111
P12			TCLR11
P13			TI11
P14			INTP110/$\overline{\text{DMAAK0}}$
P15			INTP111/$\overline{\text{DMAAK1}}$
P16			INTP112/$\overline{\text{DMAAK2}}$
P17			INTP113/$\overline{\text{DMAAK3}}$
P20	I	Port 2 P20 is an input only port. When a valid edge is input, this pin operates as NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P21 to P27 are a 7-bit I/O port. Input/output mode can be specified in 1-bit units	NMI
P21	I/O		–
P22			TXD0/SO0
P23			RXD0/SI0
P24			$\overline{\text{SCK0}}$
P25			TXD1/SO1
P26			RXD1/SI1
P27			$\overline{\text{SCK1}}$
P30	I/O	Port 3 8-bit I/O port. Input/output mode can be specified in 1-bit units	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO2
P36			INTP132/SI2
P37			INTP133/$\overline{\text{SCK2}}$
P40 to P47	I/O	Port 4 8-bit I/O port Input/output mode can be specified in 1-bit units	D0 to D7

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Pin Name	I/O	Function	Alternate Function
P50 to P57	I/O	Port 5 8-bit I/O port Input/output mode can be specified in 1-bit units	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output mode can be specified in 1-bit units	A16 to A23
P70 to P77	I	Port 7 8-bit input only port	ANI0 to ANI7
P80	I/O	Port 8 8-bit I/O port Input/output mode can be specified in 1-bit units	$\overline{CS0}$/$\overline{RAS0}$
P81			$\overline{CS1}$/$\overline{RAS1}$
P82			$\overline{CS2}$/$\overline{RAS2}$
P83			$\overline{CS3}$/$\overline{RAS3}$
P84			$\overline{CS4}$/$\overline{RAS4}$/$\overline{IOWR}$
P85			$\overline{CS5}$/$\overline{RAS5}$/$\overline{IORD}$
P86			$\overline{CS6}$/$\overline{RAS6}$
P87			$\overline{CS7}$/$\overline{RAS7}$
P90	I/O	Port 9 8-bit I/O port Input/output mode can be specified in 1-bit units	$\overline{LCAS}$/$\overline{LWR}$
P91			$\overline{UCAS}$/$\overline{UWR}$
P92			$\overline{RD}$
P93			$\overline{WE}$
P94			$\overline{BCYST}$
P95			$\overline{OE}$
P96			$\overline{HLDAK}$
P97			$\overline{HLDRQ}$
P100	I/O	Port 10 8-bit I/O port Input/output mode can be specified in 1-bit units	TO120
P101			TO121
P102			TCLR12
P103			TI12
P104			INTP120/$\overline{TC0}$
P105			INTP121/$\overline{TC1}$
P106			INTP122/$\overline{TC2}$
P107			INTP123/$\overline{TC3}$
P110	I/O	Port 11 8-bit I/O port Input/output mode can be specified in 1-bit units	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141/SO3
P116			INTP142/SI3
P117			INTP143/$\overline{SCK3}$

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Pin Name	I/O	Function	Alternate Function
P120	I/O	Port 12 8-bit I/O port Input/output mode can be specified in 1-bit units	TO150
P121			TO151
P122			TCLR15
P123			TI15
P124			INTP150
P125			INTP151
P126			INTP152
P127			INTP153/ADTRG
PA0	I/O	Port A 8-bit I/O port Input/output mode can be specified in 1-bit units	A0
PA1			A1
PA2			A2
PA3			A3
PA4			A4
PA5			A5
PA6			A6
PA7			A7
PB0	I/O	Port B 8-bit I/O port Input/output mode can be specified in 1-bit units	A8
PB1			A9
PB2			A10
PB3			A11
PB4			A12
PB5			A13
PB6			A14
PB7			A15
PX5	I/O	Port X 3-bit I/O port Input/output mode can be specified in 1-bit units	$\overline{\text{REFRQ}}$
PX6			$\overline{\text{WAIT}}$
PX7			CLKOUT

2.2 Non-Port Pins

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Pin Name	I/O	Function	Alternate Function
TO100	O	Pulse signal output for timers 10 to 15	P00
TO101			P01
TO110			P10
TO111			P11
TO120			P100
TO121			P101
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TO150			P120
TO151			P121
TCLR10	I	External clear signal input for timers 10 to 15	P02
TCLR11			P12
TCLR12			P102
TCLR13			P32
TCLR14			P112
TCLR15			P122
TI10	I	External count clock input for timers 10 to 15	P03
TI11			P13
TI12			P103
TI13			P33
TI14			P113
TI15			P123
INTP100	I	External maskable interrupt request input, also used as external capture trigger input for timer 10	P04/$\overline{\text{DMARQ0}}$
INTP101			P05/$\overline{\text{DMARQ1}}$
INTP102			P06/$\overline{\text{DMARQ2}}$
INTP103			P07/$\overline{\text{DMARQ3}}$
INTP110	I	External maskable interrupt request input, also used as external capture trigger input for timer 11	P14/$\overline{\text{DMAAK0}}$
INTP111			P15/$\overline{\text{DMAAK1}}$
INTP112			P16/$\overline{\text{DMAAK2}}$
INTP113			P17/$\overline{\text{DMAAK3}}$
INTP120	I	External maskable interrupt request input, also used as external capture trigger input for timer 12	P104/$\overline{\text{TC0}}$
INTP121			P105/$\overline{\text{TC1}}$
INTP122			P106/$\overline{\text{TC2}}$
INTP123			P107/$\overline{\text{TC3}}$

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Pin Name	I/O	Function	Alternate Function
INTP130	I	External maskable interrupt request input, also used as external capture trigger input for timer 13	P34
INTP131			P35/SO2
INTP132			P36/SI2
INTP133			P37/$\overline{\text{SCK2}}$
INTP140	I	External maskable interrupt request input, also used as external capture trigger input for timer 14	P114
INTP141			P115/SO3
INTP142			P116/SI3
INTP143			P117/$\overline{\text{SCK3}}$
INTP150	I	External maskable interrupt request input, also used as external capture trigger input for timer 15	P124
INTP151			P125
INTP152			P126
INTP153			P127/ADTRG
SO0	O	Serial transmit data output (3-wire) for CSI0 to CSI3	P22/TXD0
SO1			P25/TXD1
SO2			P35/INTP131
SO3			P115/INTP141
SI0	I	Serial receive data input (3-wire) for CSI0 to CSI3	P23/RXD0
SI1			P26/RXD1
SI2			P36/INTP132
SI3			P116/INTP142
$\overline{\text{SCK0}}$	I/O	Serial clock I/O (3-wire) for CSI0 to CSI3	P24
$\overline{\text{SCK1}}$			P27
$\overline{\text{SCK2}}$			P37/INTP133
$\overline{\text{SCK3}}$			P117/INTP143
TXD0	O	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	I	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	P40 to P47
D8 to D15			P50 to P57
A0 to A7	O	24-bit address bus for external memory	PA0 to PA7
A8 to A15			PB0 to PB7
A16 to A23			P60 to P67
$\overline{\text{LWR}}$	O	Lower byte write-enable signal output for external data bus	P90/$\overline{\text{LCAS}}$
$\overline{\text{UWR}}$	O	Higher byte write-enable signal output for external data bus	P91/$\overline{\text{UCAS}}$
$\overline{\text{RD}}$	O	Read strobe signal output for external data bus	P92
$\overline{\text{WE}}$	O	Write enable signal output for DRAM	P93
$\overline{\text{OE}}$	O	Output enable signal output for DRAM	P95

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Pin Name	I/O	Function	Alternate Function
$\overline{\text{LCAS}}$	O	Column address strobe signal output for DRAM's lower data	P90/$\overline{\text{LWR}}$
$\overline{\text{UCAS}}$	O	Column address strobe signal output for DRAM's higher data	P91/$\overline{\text{UWR}}$
$\overline{\text{RAS0}}$ to $\overline{\text{RAS3}}$	O	Low address strobe signal output for DRAM	P80/$\overline{\text{CS0}}$ to P83/$\overline{\text{CS3}}$
$\overline{\text{RAS4}}$			P84/$\overline{\text{CS4}}$/$\overline{\text{IOWR}}$
$\overline{\text{RAS5}}$			P85/$\overline{\text{CS5}}$/$\overline{\text{IORD}}$
$\overline{\text{RAS6}}$			P86/$\overline{\text{CS6}}$
$\overline{\text{RAS7}}$			P87/$\overline{\text{CS7}}$
$\overline{\text{BCYST}}$	O	Strobe signal output indicating start of bus cycle	P94
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	Chip select signal output	P80/$\overline{\text{RAS0}}$ to P83/$\overline{\text{RAS3}}$
$\overline{\text{CS4}}$			P84/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$
$\overline{\text{CS5}}$			P85/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$
$\overline{\text{CS6}}$			P86/$\overline{\text{RAS6}}$
$\overline{\text{CS7}}$			P87/$\overline{\text{RAS7}}$
$\overline{\text{WAIT}}$	I	Control signal input for inserting waits in bus cycle	PX6
$\overline{\text{REFRQ}}$	O	Refresh request signal output for DRAM	PX5
$\overline{\text{IOWR}}$	O	DMA write strobe signal output	P84/$\overline{\text{RAS4}}$/$\overline{\text{CS4}}$
$\overline{\text{IORD}}$	O	DMA read strobe signal output	P85/$\overline{\text{RAS5}}$/$\overline{\text{CS5}}$
$\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$	I	DMA request signal input	P04/INTP100 to P07/INTP103
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$	O	DMA acknowledge signal output	P14/INTP110 to P17/INTP113
$\overline{\text{TC0}}$ to $\overline{\text{TC3}}$	O	DMA end (terminal count) signal output	P104/INTP120 to P107/INTP123
$\overline{\text{HLDAK}}$	O	Bus hold acknowledge output	P96
$\overline{\text{HLDRQ}}$	I	Bus hold request input	P97
ANI0 to ANI7	I	Analog input to A/D converter	P70 to P77
NMI	I	Non-maskable interrupt request input	P20
CLKOUT	O	System clock output	PX7
CKSEL	I	Input for specifying clock generator's operation mode	—
MODE0 to MODE3	I	Specify operation modes	—
$\overline{\text{RESET}}$	I	System reset input	—
X1	I	Oscillator connection for system clock. Input is via X1 when using an external clock.	—
X2	—		—
ADTRG	I	A/D converter external trigger input	P127/INTP153
AV_{REF}	I	Reference voltage input for A/D converter	—
AV_{DD}	—	Positive power supply for A/D converter	—
AV_{SS}	—	Ground potential for A/D converter	—

(4/4)

Pin Name	I/O	Function	Alternate Function
CV_{DD}	—	Positive power supply for dedicated clock generator	—
CV_{SS}	—	Ground potential for dedicated clock generator	—
V_{DD}	—	Positive power supply (power supply for internal units)	—
HV_{DD}	—	Positive power supply (power supply for external pins)	—
V_{SS}	—	Ground potential	—

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)

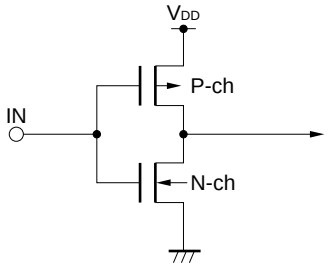
Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100, P01/TO101	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P02/TCLR10, P03/TI10	5-K	
P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$		
P10/TO110, P11/TO111	5	
P12/TCLR11, P13/TI11	5-K	
P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$		
P20/NMI	2	Connect directly to V_{SS}
P21	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P22/TXD0/SO0		
P23/RXD0/SI0	5-K	
P24/$\overline{\text{SCK0}}$		
P25/TXD1/SO1	5	
P26/RXD1/SI1	5-K	
P27/$\overline{\text{SCK1}}$		
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13	5-K	
P34/INTP130		
P35/INTP131/SO2		
P36/INTP132/SI2		
P37/INTP133/$\overline{\text{SCK2}}$		
P40/D0 to P47/D7	5	
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P77/ANI7	9	Connect directly to V_{SS}
P80/$\overline{\text{CS0}}$/$\overline{\text{RAS0}}$ to P83/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P84/$\overline{\text{CS4}}$/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$, P85/$\overline{\text{CS5}}$/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$		
P86/$\overline{\text{CS6}}$/$\overline{\text{RAS6}}$, P87/$\overline{\text{CS7}}$/$\overline{\text{RAS7}}$		
P90/$\overline{\text{LCAS}}$/$\overline{\text{LWR}}$		
P91/$\overline{\text{UCAS}}$/$\overline{\text{UWR}}$		

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

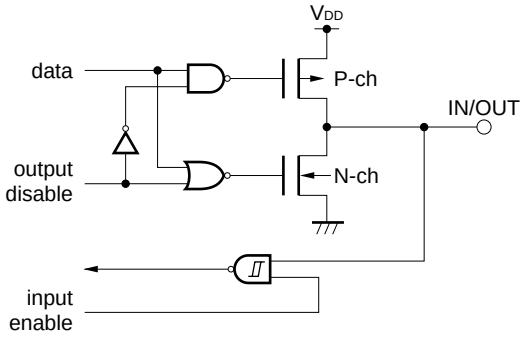
Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P92/$\overline{RD}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P93/$\overline{WE}$		
P94/$\overline{BCYST}$		
P95/$\overline{OE}$		
P96/$\overline{HLDAK}$		
P97/$\overline{HLDRQ}$		
P100/TO120, P101/TO121		
P102/TCLR12, P103/TI12	5-K	
P104/INTP120/$\overline{TC0}$ to P107/INTP123/$\overline{TC3}$		
P110/TO140, P111/TOI41	5	
P112/TCLR14, P113/TI14	5-K	
P114/INTP140		
P115/INTP141/SO3		
P116/INTP142/SI3		
P117/INTP143/$\overline{SCK3}$		
P120/TO150, P121/TO151	5	
P122/TCLR15, P123/TI15	5-K	
P124/INTP150 to P126/INTP152		
P127/INTP153/ADTRG		
PA0/A0 to PA7/A7	5	
PB0/A8 to PB7/A15		
PX5/$\overline{REFRQ}$		
PX6/$\overline{WAIT}$		
PX7/CLKOUT		
CKSEL	1	Connect directly to HV_{DD}
$\overline{RESET}$	2	—
MODE0 to MODE2		
MODE3		Connect to V_{SS} via a resistor (R_{VPP})
AV_{REF}, AV_{SS}	—	Connect directly to V_{SS}
AV_{DD}	—	Connect directly to HV_{DD}

Figure 2-1. Pin I/O Circuits

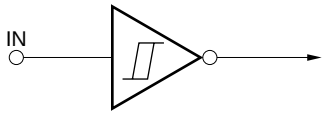
Type 1



Type 5-K

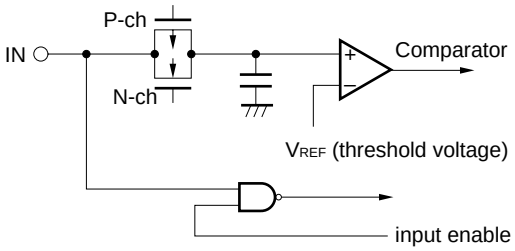


Type 2

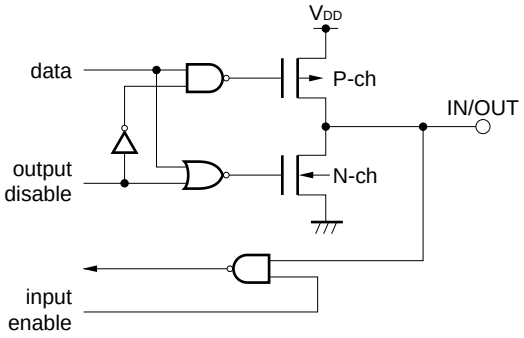


Schmitt trigger input with hysteresis characteristics

Type 9



Type 5



Caution Replace V_{DD} with HV_{DD} when referencing the circuit diagrams shown above.

3. FUNCTION BLOCKS

3.1 Internal Units

3.1.1 CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as the multiplier (16 bits × 16 bits → 32 bits, or 32 bits × 32 bits → 64 bits) and the barrel shifter (32 bits) help accelerate processing of complex instructions.

3.1.2 Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU. When an instruction is fetched from the external memory area and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in the internal instruction queue of the CPU.

The BCU contains a DRAM controller (DRAMC), page ROM controller, and DMA controller (DMAC).

(a) DRAM controller (DRAMC)

The DRAM controller generates the $\overline{RAS}$, $\overline{UCAS}$, and $\overline{LCAS}$ signals (2CAS control) and controls access to the DRAM.

It supports high-speed page DRAM and EDO DRAM, and has two types of cycles for accessing DRAM. These types of cycles are referred to as normal access (off-page) and page access (on-page).

The DRAM controller also has a refresh function that is associated with the CBR refresh cycle.

(b) Page ROM controller

The page ROM controller supports access to ROM that has the page access function.

It compares the address with that of the preceding bus cycle and controls the waits for normal access (off-page) and page access (on-page). The page ROM controller can support page sizes of 8 to 64 bytes.

(c) DMA controller (DMAC)

The DMA controller transfers data between memory and an I/O device in place of the CPU.

The two address modes are flyby (one-cycle) transfer and two-cycle transfer. The three bus modes are single transfer, single-step transfer, and block transfer.

3.1.3 ROM

The μPD703101A-33 contains 96 Kbytes of mask ROM, and the μPD703102A-33 contains 128 Kbytes of mask ROM.

The CPU can access ROM in one clock cycle when an instruction is fetched.

When single-chip mode 0 is set, ROM is mapped to the address space starting at 00000000H. When single-chip mode 1 is set, ROM is mapped to the address space starting at 00100000H. When ROM-less mode 0 or 1 is set, ROM cannot be accessed.

The μPD703100A-33 and μPD703100A-40 have no internal ROM.

3.1.4 RAM

RAM is mapped to the 4-Kbyte address space starting at FFFFE000H. The CPU can access RAM in one clock cycle when an instruction is fetched or data is accessed.

3.1.5 Ports

In addition to the 123 pins (ports 0 to 12, A, B, and X) constituting the I/O ports (of which nine pins constitute an input-only port), various port pin and control pin functions can be selected for these pins.

3.1.6 Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP100 to INTP103, INTP110 to INTP113, INTP120 to INTP123, INTP130 to INTP133, INTP140 to INTP143, and INTP150 to INTP153) from on-chip peripheral I/O and external hardware. Eight interrupt priority levels can be specified for these interrupt requests, and multiplexed servicing control can be performed for interrupt sources.

3.1.7 Clock generator (CG)

A frequency of five times (using an on-chip PLL) or one-half times (not using an on-chip PLL) that of the input clock (f_{XX}) is supplied as the internal system clock (ϕ). Either an external oscillator is connected to pins X1 and X2 (only when the on-chip PLL synthesizer is used) or an external clock is input from the X1 pin as the input clock.

3.1.8 Real-time pulse unit (RPU)

The RPU includes a six-channel 16-bit timer/event counter and a two-channel 16-bit interval timer, which enables measurement of pulse intervals and frequency as well as programmable pulse output.

3.1.9 Serial interface (SIO)

Four channels are comprised of two kinds of serial interfaces: an asynchronous serial interface (UART) and a clocked serial interface (CSI). Two of these four channels are switchable between the UART and CSI and the other two channels are fixed as CSI.

For UART, data is transferred via the TXD and RXD pins. For CSI, data is transferred via the SO, SI, and $\overline{SCK}$ pins.

The serial clock source can be selected from dedicated baud rate generator output or the internal system clock.

3.1.10 A/D converter (ADC)

This is a high-speed, high-resolution 10-bit A/D converter that includes eight analog input pins. It converts using the successive approximation method.

4. CPU FUNCTIONS

- RISC-based architecture
- Uses five-stage pipeline control to enable single-clock execution of almost all instructions
- Minimum instruction execution time 25 ns (@ 40-MHz operation) ... μPD703100A-40
  30 ns (@ 33-MHz operation) ... μPD703100A-33, 703101A-33, 703102A-33
- Memory space Program space: 64-Mbyte linear
  Data space: 4-Gbyte linear
- General registers 32 bits × 32
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiply/divide instructions
- Saturated operation instructions
- 32-bit shift instruction: 1 clock
- Long/short format
- Four types of bit manipulation instructions
  - Set
  - Clear
  - Not
  - Test

5. BUS CONTROL FUNCTIONS

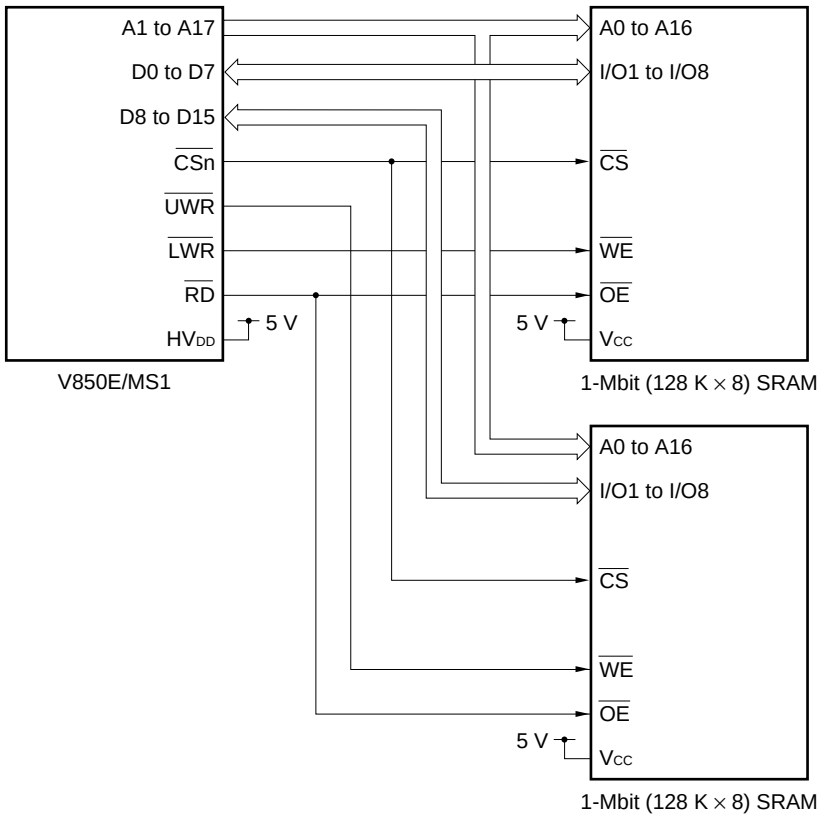
- 16-bit/8-bit data bus sizing function
- 8-space chip select output function
- Wait functions
  - Programmable wait function for up to seven states for each memory block
  - External wait function using $\overline{\text{WAIT}}$ pin
- Idle state insertion function
- Bus mastering arbitration function
- Bus hold function
- Alternate function port pins are connectable to external bus

6. MEMORY ACCESS CONTROL FUNCTIONS

6.1 SRAM Connection

The following figure shows an SRAM connection example.

Figure 6-1. SRAM Connection Example



Remark n = 0 to 7

6.2 Page ROM Controller (ROMC)

The page ROM controller (ROMC) supports access to ROM (page ROM) that has the page access function.

It compares the address with that of the preceding bus cycle and performs wait control for normal access (off-page) and page access (on-page). The page ROM controller can support page widths of 8 to 64 bytes.

6.2.1 Features

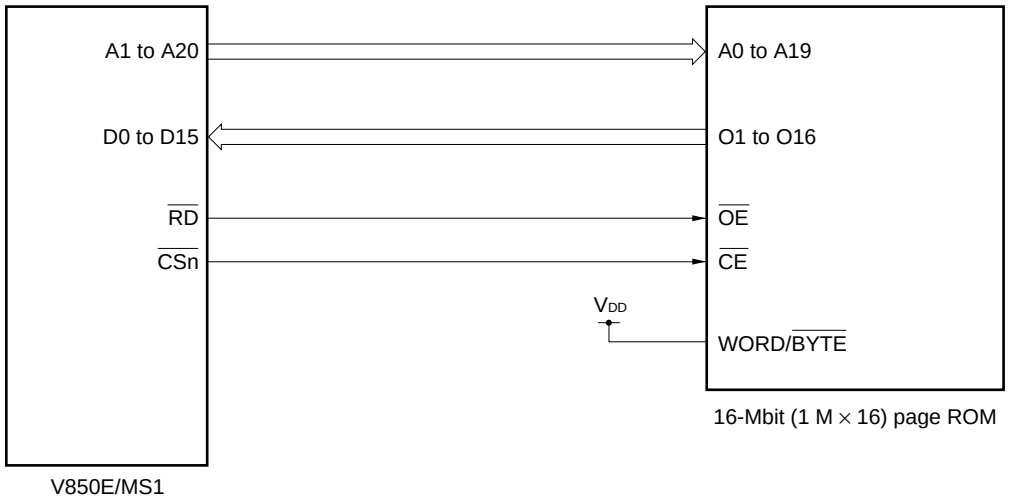
- Can be connected directly to 8-bit or 16-bit page ROM
- For 16-bit bus width, it supports 4-, 8-, 16-, or 32-word page access
  For 8-bit bus width, it supports 8-, 16-, 32-, or 64-word page access
- Enables waits to be set (0 to 7 waits) independently for off-page and on-page access

6.2.2 Page ROM connection

The following figure shows page ROM connection examples.

Figure 6-2. Page ROM Connection Examples (1/2)

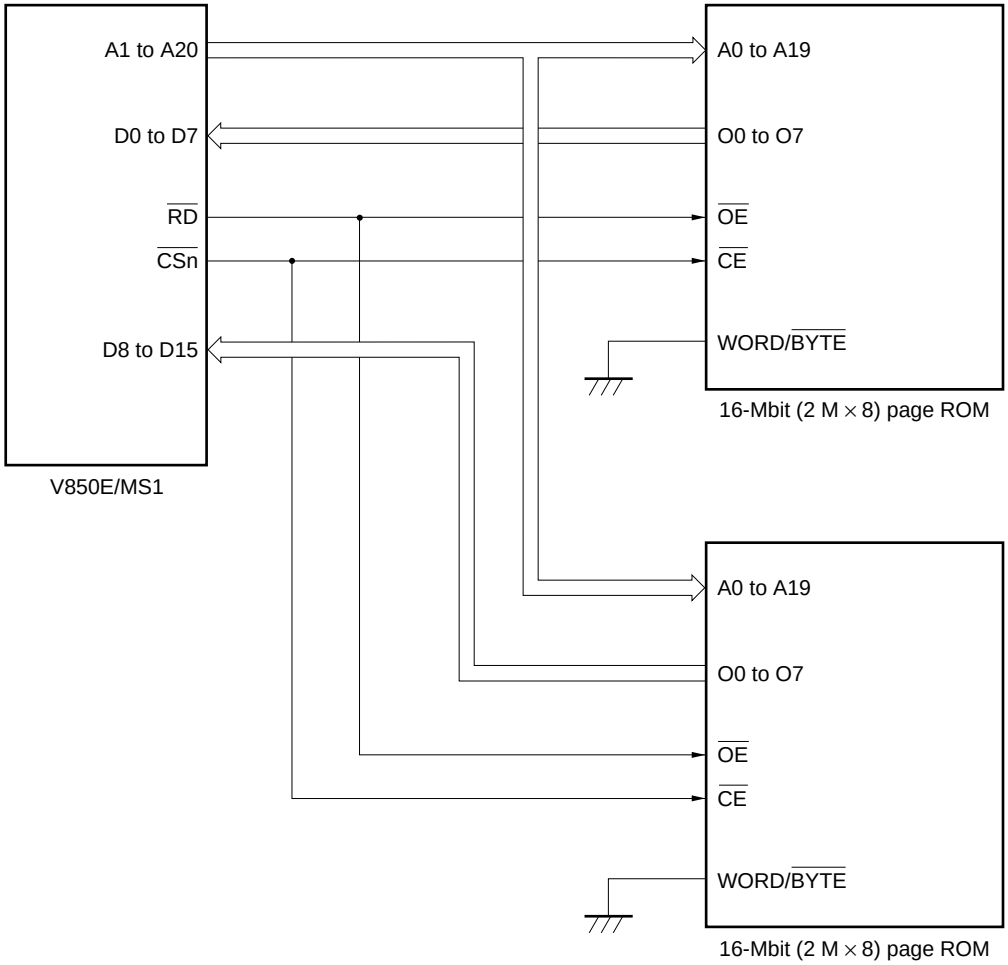
(a) 16-Mbit (1 M × 16) page ROM



Remark n = 0 to 7

Figure 6-2. Page ROM Connection Examples (2/2)

(b) 16-Mbit (2 M × 8) page ROM



Remark n = 0 to 7

6.3 DRAM Controller

6.3.1 Features

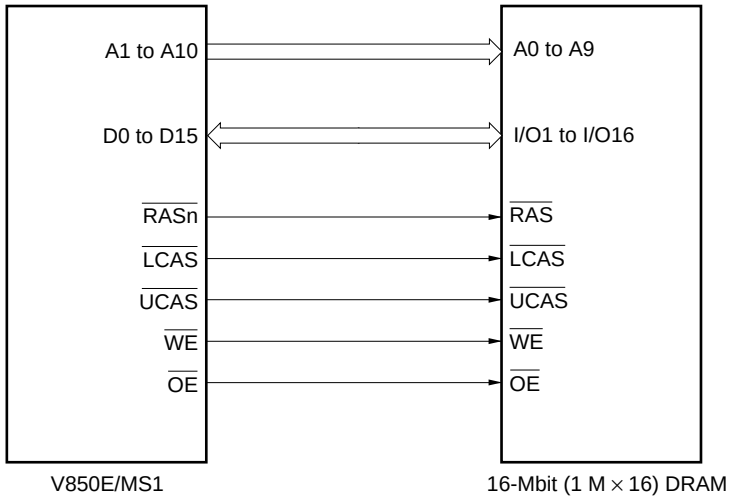
- Generates the $\overline{RAS}$, $\overline{UCAS}$, and $\overline{LCAS}$ signals
- Can be connected directly to high-speed page DRAM and EDO DRAM
- Supports RAS hold mode
- Can assign 4 types of DRAM to 8 memory block space
- Supports 2CAS type DRAM
- Can be switched between row and column address multiplex widths
- Can insert waits (0 to 3 waits) at each of the following timings
  - Row address pre-charge wait
  - Row address hold wait
  - Data access wait
  - Column address pre-charge wait
- Supports CBR refresh and CBR self refresh

6.3.2 DRAM connections

The following figure shows DRAM connection examples.

Figure 6-3. DRAM Connection Examples (1/2)

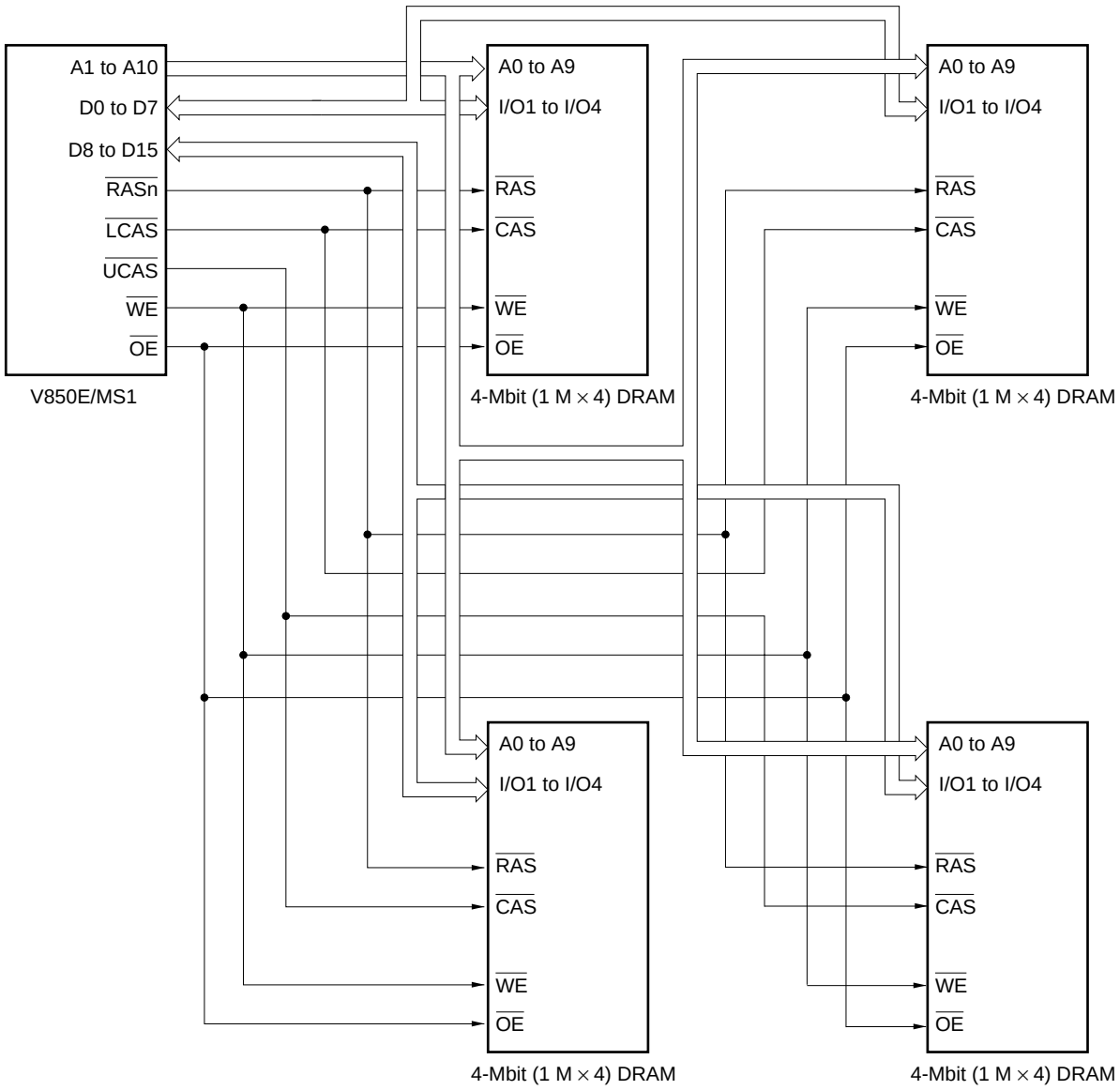
(a) 16-Mbit (1 M × 16) DRAM



Remark n = 0 to 7

Figure 6-3. DRAM Connection Examples (2/2)

(b) 4-Mbit (1 M × 4) DRAM

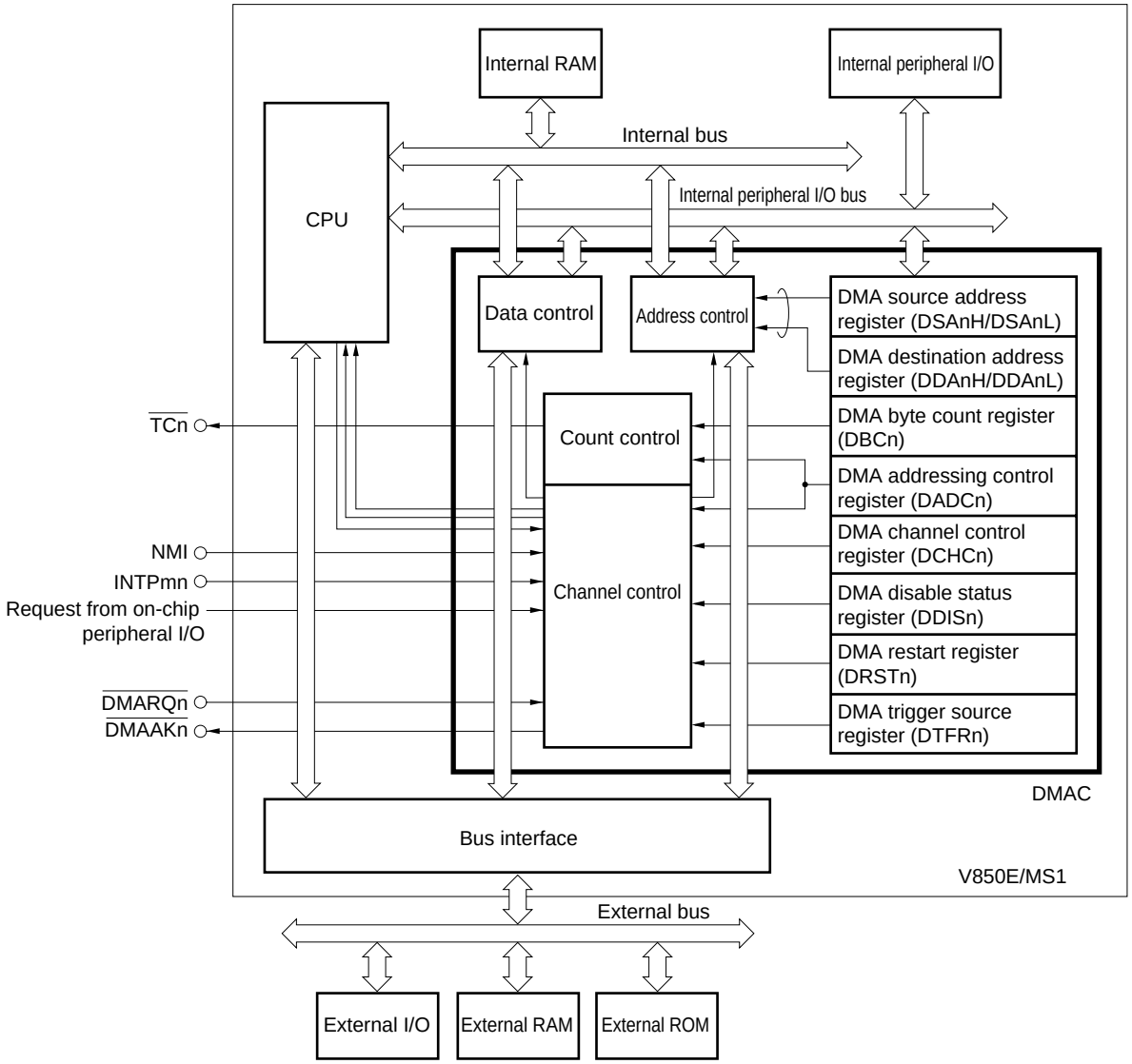


Remark n = 0 to 7

7. DMA FUNCTIONS (DMA CONTROLLER)

- 4 independent DMA channels
- Transfer units: 8 or 16 bits
- Maximum transfer count: 65536 (2^{16})
- Two types of transfer
  - Flyby (one-cycle) transfer
  - Two-cycle transfer
- Three transfer modes
  - Single transfer mode
  - Single-step transfer mode
  - Block transfer mode
- Transfer requests
  - $\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$ pin (× 4)
  - Requests from on-chip peripheral I/O (serial interface and real-time pulse unit)
  - Requests by software
- Transfer objects
  - Memory to I/O and vice versa
  - Memory to memory and vice versa
- DMA transfer end output signal ($\overline{\text{TC0}}$ to $\overline{\text{TC3}}$)

Figure 7-1. DMA Function Block Diagram



Remark m = 10 to 15, n = 0 to 3

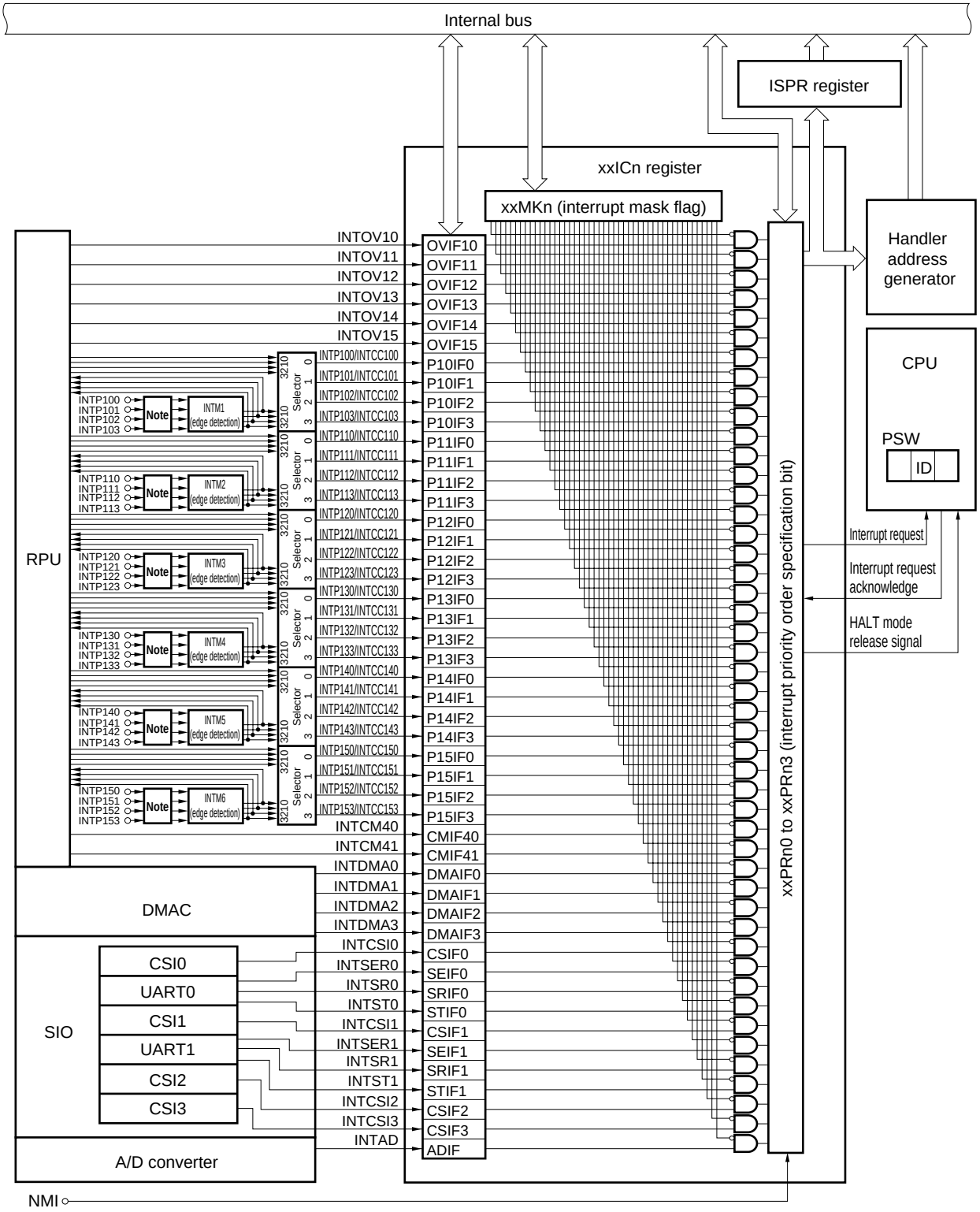
8. INTERRUPT/EXCEPTION PROCESSING FUNCTIONS

8.1 Features

○ Interrupts
- Non-maskable interrupt: 1 source
- Maskable interrupt: 47 sources
- 8-level programmable priority control
- Multiple interrupt control based on priority levels
- Mask specification for each maskable interrupt request
- Noise elimination, edge detection, and valid edge specification for external interrupt requests

○ Exceptions
- Software exceptions: 32 sources
- Exception trap: 1 source (invalid instruction code exception)

Figure 8-1. Interrupt Control Function Block Diagram



Note Noise elimination

Remark xx: OV, CM, P10 to P15, DMA, CS, SE, SR, ST, AD
n: None, or 10 to 15, 40, 41, 0 to 3

Table 8-1. List of Interrupts (1/3)

Type	Category	Interrupt/Exception Source				Default Priority	Exception Code	Handler Address	Restore PC
		Name	Control Register	Generation Source	Generating Unit				
Reset	Interrupt	RESET	—	$\overline{\text{RESET}}$ input	Pin	—	0000H	00000000H	Undefined
Non-maskable	Interrupt	NMI	—	NMI input	Pin	—	0010H	00000010H	nextPC
Software exception	Exception	TRAP0n[Note]	—	TRAP instruction	—	—	004n[Note]H	00000040H	nextPC
	Exception	TRAP1n[Note]	—	TRAP instruction	—	—	005n[Note]H	00000050H	nextPC
Exception trap	Exception	ILGOP	—	Illegal instruction code	—	—	0060H	00000060H	nextPC
Maskable	Interrupt	INTOV10	OVIC10	Timer 10 overflow	RPU	0	0080H	00000080H	nextPC
	Interrupt	INTOV11	OVIC11	Timer 11 overflow	RPU	1	0090H	00000090H	nextPC
	Interrupt	INTOV12	OVIC12	Timer 12 overflow	RPU	2	00A0H	000000A0H	nextPC
	Interrupt	INTOV13	OVIC13	Timer 13 overflow	RPU	3	00B0H	000000B0H	nextPC
	Interrupt	INTOV14	OVIC14	Timer 14 overflow	RPU	4	00C0H	000000C0H	nextPC
	Interrupt	INTOV15	OVIC15	Timer 15 overflow	RPU	5	00D0H	000000D0H	nextPC
	Interrupt	INTP100/ INTCC100	P10IC0	Match between INTP100 and CC100	Pin/RPU	6	0100H	00000100H	nextPC
	Interrupt	INTP101/ INTCC101	P10IC1	Match between INTP101 and CC101	Pin/RPU	7	0110H	00000110H	nextPC
	Interrupt	INTP102/ INTCC102	P10IC2	Match between INTP102 and CC102	Pin/RPU	8	0120H	00000120H	nextPC
	Interrupt	INTP103/ INTCC103	P10IC3	Match between INTP103 and CC103	Pin/RPU	9	0130H	00000130H	nextPC
	Interrupt	INTP110/ INTCC110	P11IC0	Match between INTP110 and CC110	Pin/RPU	10	0140H	00000140H	nextPC
	Interrupt	INTP111/ INTCC111	P11IC1	Match between INTP111 and CC111	Pin/RPU	11	0150H	00000150H	nextPC
	Interrupt	INTP112/ INTCC112	P11IC2	Match between INTP112 and CC112	Pin/RPU	12	0160H	00000160H	nextPC
	Interrupt	INTP113/ INTCC113	P11IC3	Match between INTP113 and CC113	Pin/RPU	13	0170H	00000170H	nextPC
	Interrupt	INTP120/ INTCC120	P12IC0	Match between INTP120 and CC120	Pin/RPU	14	0180H	00000180H	nextPC
	Interrupt	INTP121/ INTCC121	P12IC1	Match between INTP121 and CC121	Pin/RPU	15	0190H	00000190H	nextPC
	Interrupt	INTP122/ INTCC122	P12IC2	Match between INTP122 and CC122	Pin/RPU	16	01A0H	000001A0H	nextPC

Note n = 0 to FH

Table 8-1. List of Interrupts (2/3)

Type	Category	Interrupt/Exception Source				Default Priority	Exception Code	Handler Address	Restore PC
		Name	Control Register	Generation Source	Generating Unit				
Maskable	Interrupt	INTP123/ INTCC123	P12IC3	Match between INTP123 and CC123	Pin/RPU	17	01B0H	000001B0H	nextPC
	Interrupt	INTP130/ INTCC130	P13IC0	Match between INTP130 and CC130	Pin/RPU	18	01C0H	000001C0H	nextPC
	Interrupt	INTP131/ INTCC131	P13IC1	Match between INTP131 and CC131	Pin/RPU	19	01D0H	000001D0H	nextPC
	Interrupt	INTP132/ INTCC132	P13IC2	Match between INTP132 and CC132	Pin/RPU	20	01E0H	000001E0H	nextPC
	Interrupt	INTP133/ INTCC133	P13IC3	Match between INTP133 and CC133	Pin/RPU	21	01F0H	000001F0H	nextPC
	Interrupt	INTP140/ INTCC140	P14IC0	Match between INTP140 and CC140	Pin/RPU	22	0200H	00000200H	nextPC
	Interrupt	INTP141/ INTCC141	P14IC1	Match between INTP141 and CC141	Pin/RPU	23	0210H	00000210H	nextPC
	Interrupt	INTP142/ INTCC142	P14IC2	Match between INTP142 and CC142	Pin/RPU	24	0220H	00000220H	nextPC
	Interrupt	INTP143/ INTCC143	P14IC3	Match between INTP143 and CC143	Pin/RPU	25	0230H	00000230H	nextPC
	Interrupt	INTP150/ INTCC150	P15IC0	Match between INTP150 and CC150	Pin/RPU	26	0240H	00000240H	nextPC
	Interrupt	INTP151/ INTCC151	P15IC1	Match between INTP151 and CC151	Pin/RPU	27	0250H	00000250H	nextPC
	Interrupt	INTP152/ INTCC152	P15IC2	Match between INTP152 and CC152	Pin/RPU	28	0260H	00000260H	nextPC
	Interrupt	INTP153/ INTCC153	P15IC3	Match between INTP153 and CC153	Pin/RPU	29	0270H	00000270H	nextPC
	Interrupt	INTCM40	CMIC40	CM40 match signal	RPU	30	0280H	00000280H	nextPC
	Interrupt	INTCM41	CMIC41	CM41 match signal	RPU	31	0290H	00000290H	nextPC
	Interrupt	INTDMA0	DMAIC0	DMA channel 0 transfer completion	DMAC	32	02A0H	000002A0H	nextPC
	Interrupt	INTDMA1	DMAIC1	DMA channel 1 transfer completion	DMAC	33	02B0H	000002B0H	nextPC
	Interrupt	INTDMA2	DMAIC2	DMA channel 2 transfer completion	DMAC	34	02C0H	000002C0H	nextPC
	Interrupt	INTDMA3	DMAIC3	DMA channel 3 transfer completion	DMAC	35	02D0H	000002D0H	nextPC
	Interrupt	INTCSI0	CSIC0	CSI0 send/receive completion	SIO	36	0300H	000000300H	nextPC
	Interrupt	INTSER0	SEIC0	UART0 receive error	SIO	37	0310H	000000310H	nextPC

Note n = 0 to FH

Table 8-1. List of Interrupts (3/3)

Type	Category	Interrupt/Exception Source				Default Priority	Exception Code	Handler Address	Restore PC
		Name	Control Register	Generation Source	Generating Unit				
Maskable	Interrupt	INTSR0	SRIC0	UART0 receive completion	SIO	38	0320H	00000320H	nextPC
	Interrupt	INTST0	STIC0	UART0 send completion	SIO	39	0330H	00000330H	nextPC
	Interrupt	INTCSI1	CSIC1	CSI1 send/receive completion	SIO	40	0340H	00000340H	nextPC
	Interrupt	INTSER1	SEIC1	UART1 receive error	SIO	41	0350H	00000350H	nextPC
	Interrupt	INTSR1	SRIC1	UART1 receive completion	SIO	42	0360H	00000360H	nextPC
	Interrupt	INTST1	STIC1	UART1 send completion	SIO	43	0370H	00000370H	nextPC
	Interrupt	INTCSI2	CSIC2	CSI2 send/receive completion	SIO	44	0380H	00000380H	nextPC
	Interrupt	INTCSI3	CSIC3	CSI3 send/receive completion	SIO	45	03C0H	000003C0H	nextPC
	Interrupt	INTAD	ADIC	A/D conversion completion	ADC	46	0400H	00000400H	nextPC

Remarks 1. Default priority: The priority that takes precedence when two or more maskable interrupt requests having the same priority level are generated at the same time. The highest priority is 0.

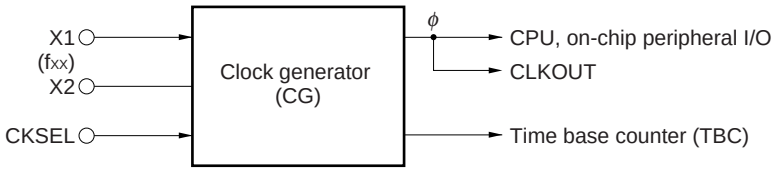
Restore PC: The PC value that is saved in EIPC or FEPC when the interrupt or exception processing is started. However, the restore PC value that is saved when an interrupt is acknowledged during the execution of a division instruction (DIV, DIVH, DIVU, or DIVHU) is the PC value of the current instruction (DIV, DIVH, DIVU, or DIVHU).

2. The execution address of the illegal instruction when an illegal opcode exception occurs is obtained according to the calculation “restore PC - 4.”

9. CLOCK GENERATION FUNCTIONS

- Multiplier function using a PLL (Phase locked loop) synthesizer
- Clock sources
  - Oscillation by connecting an oscillator: $f_{XX} = \phi/5$
  - External clock: $f_{XX} = 2 \times \phi$ or $\phi/5$
- Power saving modes
  - HALT mode
  - IDLE mode
  - Software STOP mode
  - Clock output inhibit mode
- Internal system clock output function

Figure 9-1. Block Diagram of Clock Generation Function

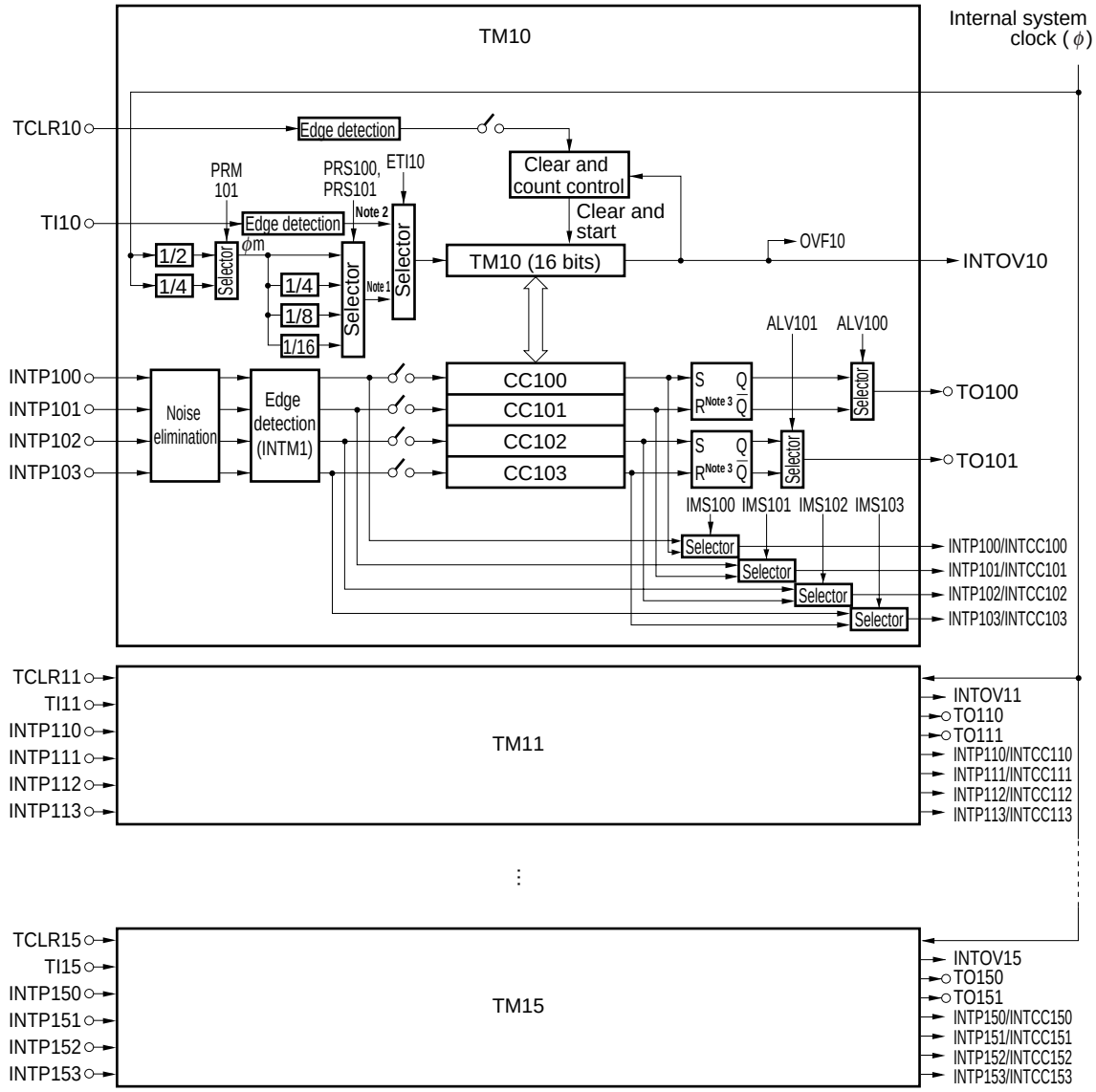


Remark ϕ: internal system clock frequency
F_{XX}: external oscillator or external clock frequency

10. TIMER/COUNTER FUNCTIONS (REAL-TIME PULSE UNIT)

- Measures the pulse interval and frequency, and outputs a programmable pulse
  - 16-bit measurements are possible
  - Can generate a variety of pulse patterns (interval pulse, one-shot pulse)
- Timer 1
  - 16-bit timer/event counter
  - Count clock sources: 2 types (division of internal system clock, and external pulse input)
  - Capture/compare common registers: 24
  - Count clear pins: TCLR10 to TCLR15
  - Interrupt sources: 30 types
  - External pulse outputs: 12
- Timer 4
  - 16-bit interval timer
  - Count clock can be selected from internal system clock divisions
  - Compare registers: 2
  - Interrupt sources: 2

Figure 10-1. Block Diagram of Timer 1 (16-bit Timer/Event Counter)

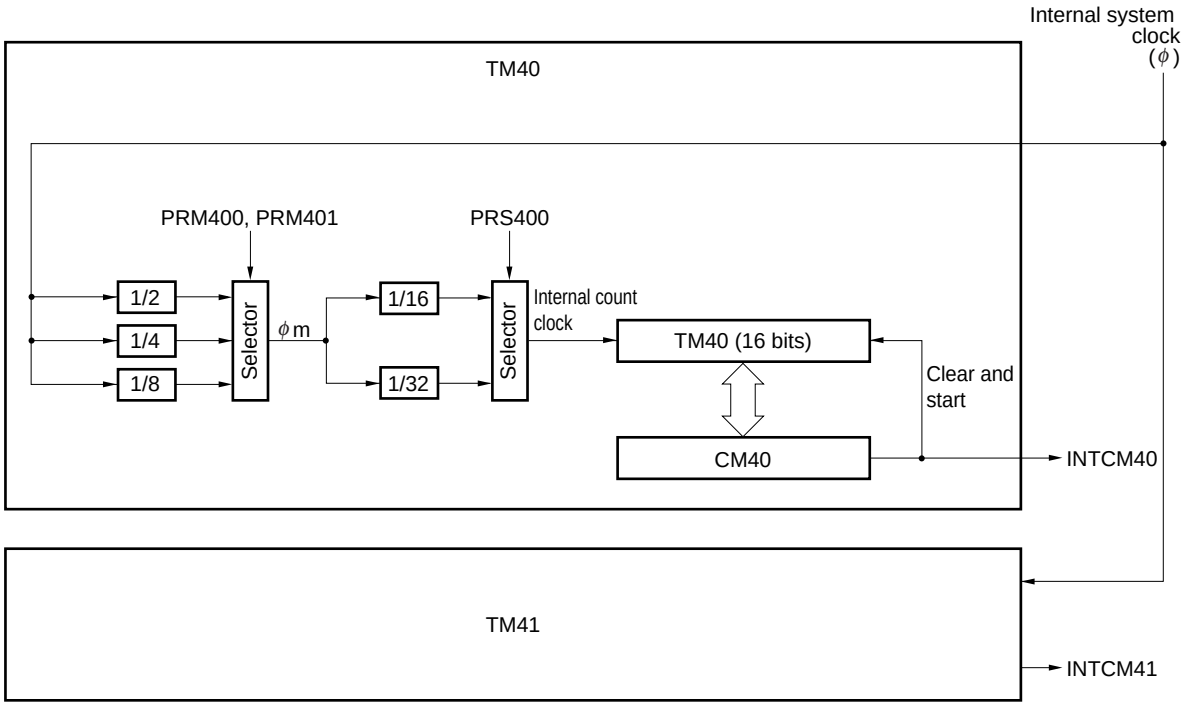


Notes 1. Internal count clock

2. External count clock

3. Reset priority

Figure 10-2. Block Diagram of Timer 4 (16-bit Interval Timer)



11. SERIAL INTERFACE FUNCTION

The serial interface function provides two 6-channel serial interfaces.
Up to four channels can be used at the same time.

(1) Asynchronous serial interface (UART0 and UART1): 2 channels
(2) Clocked serial interface (CSI0 to CSI3): 4 channels

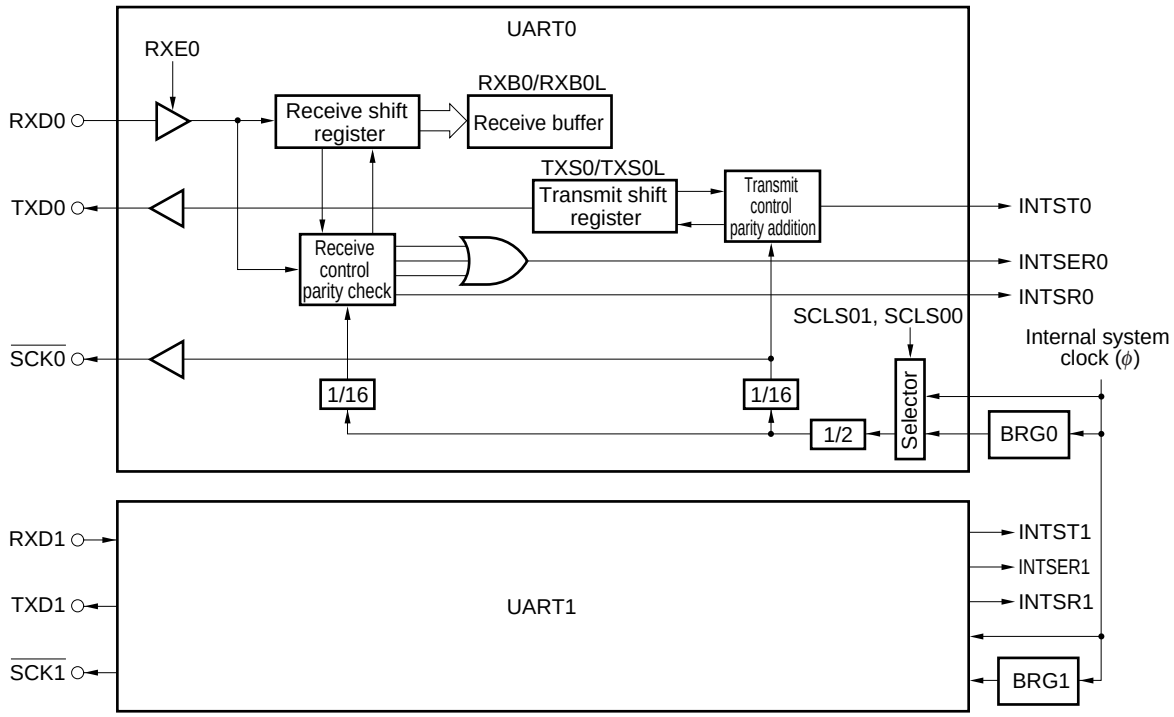
Caution UART0 and CSI0 share a pin, as do UART1 and CSI1. One or the other of each pair can be selected via a register (ASIM00, ASIM10).

11.1 Asynchronous Serial Interfaces 0, 1 (UART0, UART1)

- Transfer rate
  150 bps to 76800 bps (using the dedicated baud rate generator when the internal system clock is 33 MHz)
  Maximum 4.125 Mbps (using the ϕ/2 clock when the internal system clock is 33 MHz)
- Full duplex communications
  On-chip receive buffer (RXBn)
- 2-pin configuration
  TXDn: Transmit data output pin
  RXDn: Receive data input pin
- Receive error detection functions
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 3 types
  - Receive error interrupt (INTSERn)
  - Receive completion interrupt (INTSRn)
  - Transmission completion interrupt (INTSTn)
- The character length of transmission/reception data is specified by the ASIMn0 and ASIMn1 registers.
- Character length
  7, 8 bits
  9 bits (when adding an expansion bit)
- Parity function: odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- Serial clock ($\overline{\text{SCKn}}$) output function

Remark n = 0, 1

Figure 11-1. Block Diagram of Asynchronous Serial Interfaces 0, 1 (UART0, UART1)

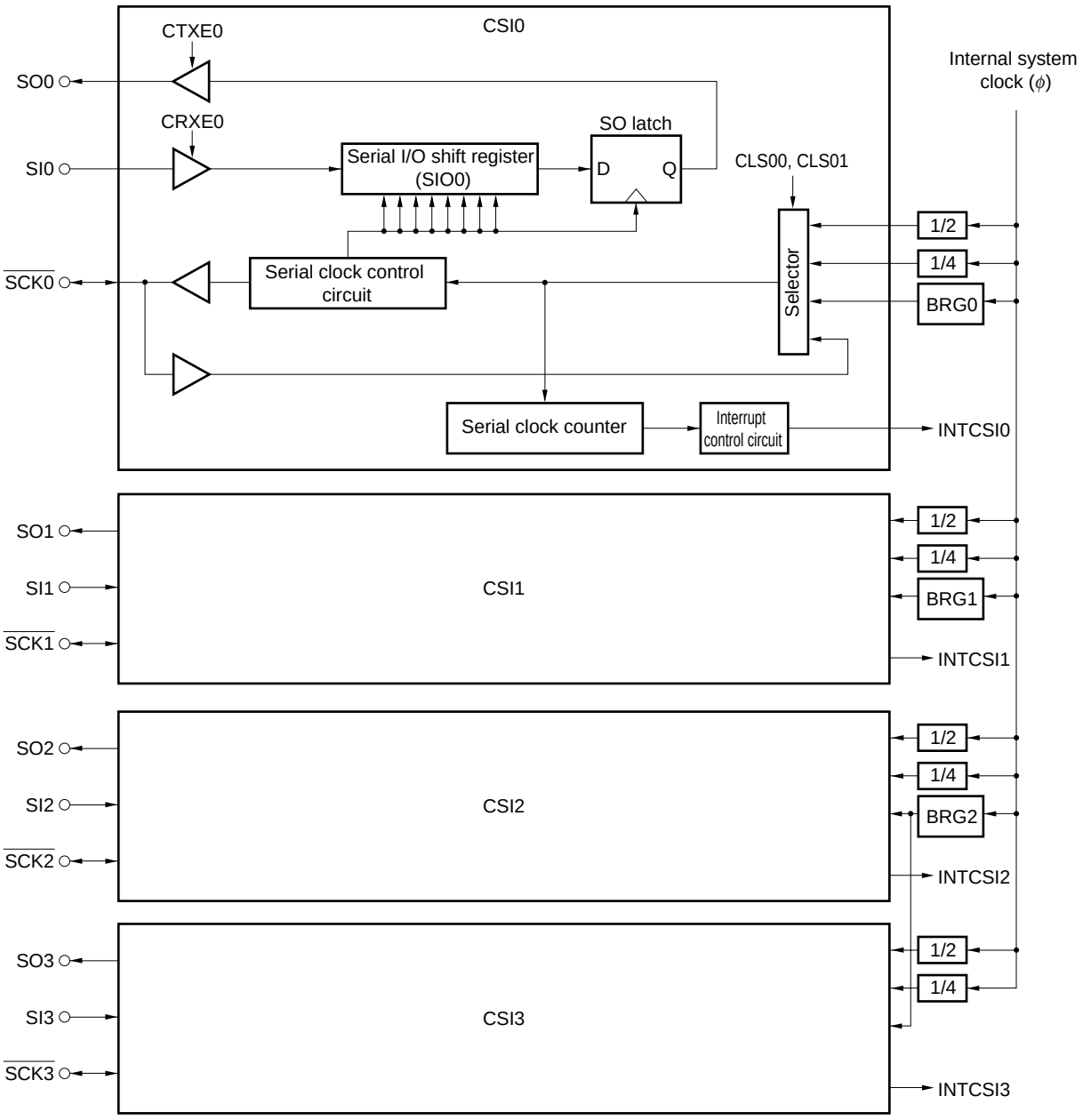


11.2 Clocked Serial Interfaces 0 to 3 (CSI0 to CSI3)

- High-speed transfer
  Maximum 10 Mbps (when the internal system clock is operating at 40 MHz) μPD703100A-40
  Maximum 8.25 Mbps (when the internal system clock is operating at 33 MHz) μPD703100A-33, μPD703101A-33, μPD703102A-33
- Half-duplex communications
- Character length: 8 bits
- Can switch between MSB first or LSB first for data
- Either external serial clock input or internal serial clock output can be selected
- 3-wire type
  SOn: Serial data output
  SIn: Serial data input
  $\overline{\text{SCK}}$n: Serial clock input/output
- Interrupt source: 1 type
  - Transmission/reception completion interrupt (INTCSIn)

Remark n = 0 to 3

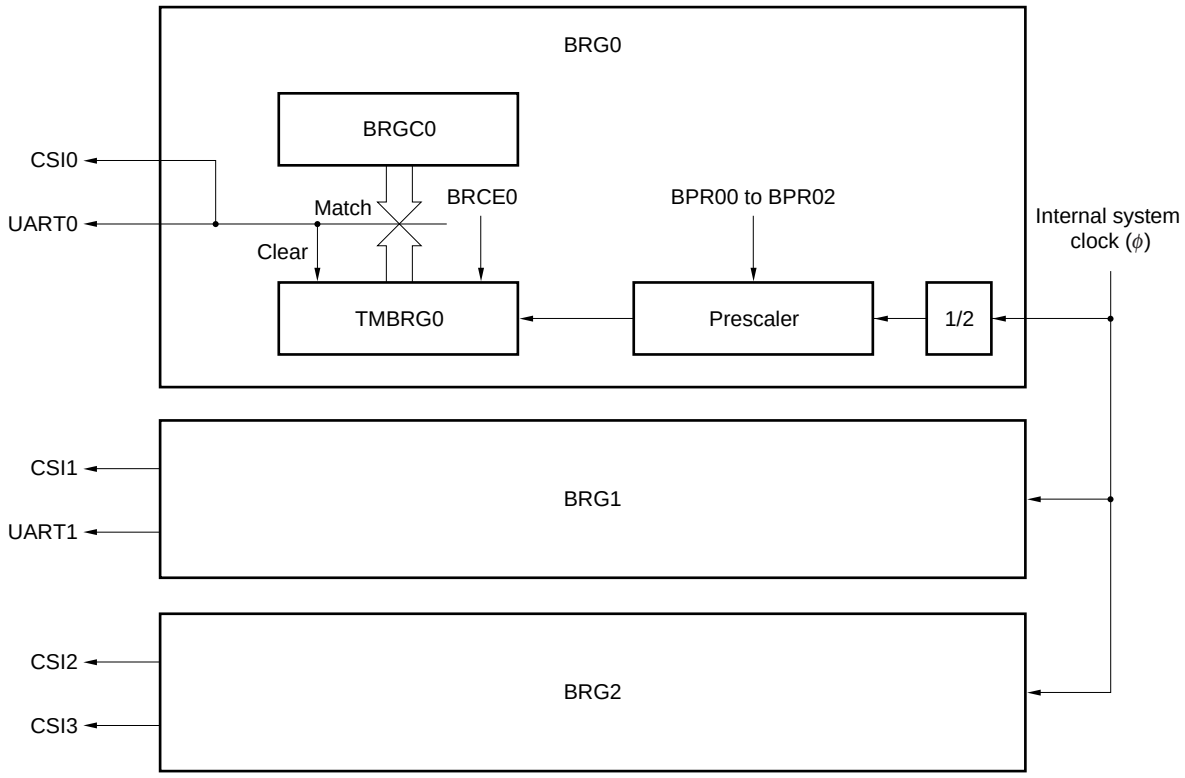
Figure 11-2. Block Diagram of Clocked Serial Interfaces 0 to 3 (CSI0 to CSI3)



11.3 Dedicated Baud Rate Generators 0 to 2 (BRG0 to BRG2)

- Serial clock can be selected via either dedicated baud rate generator output or internal system clock (ϕ)
- Identical baud rates during transmission and reception

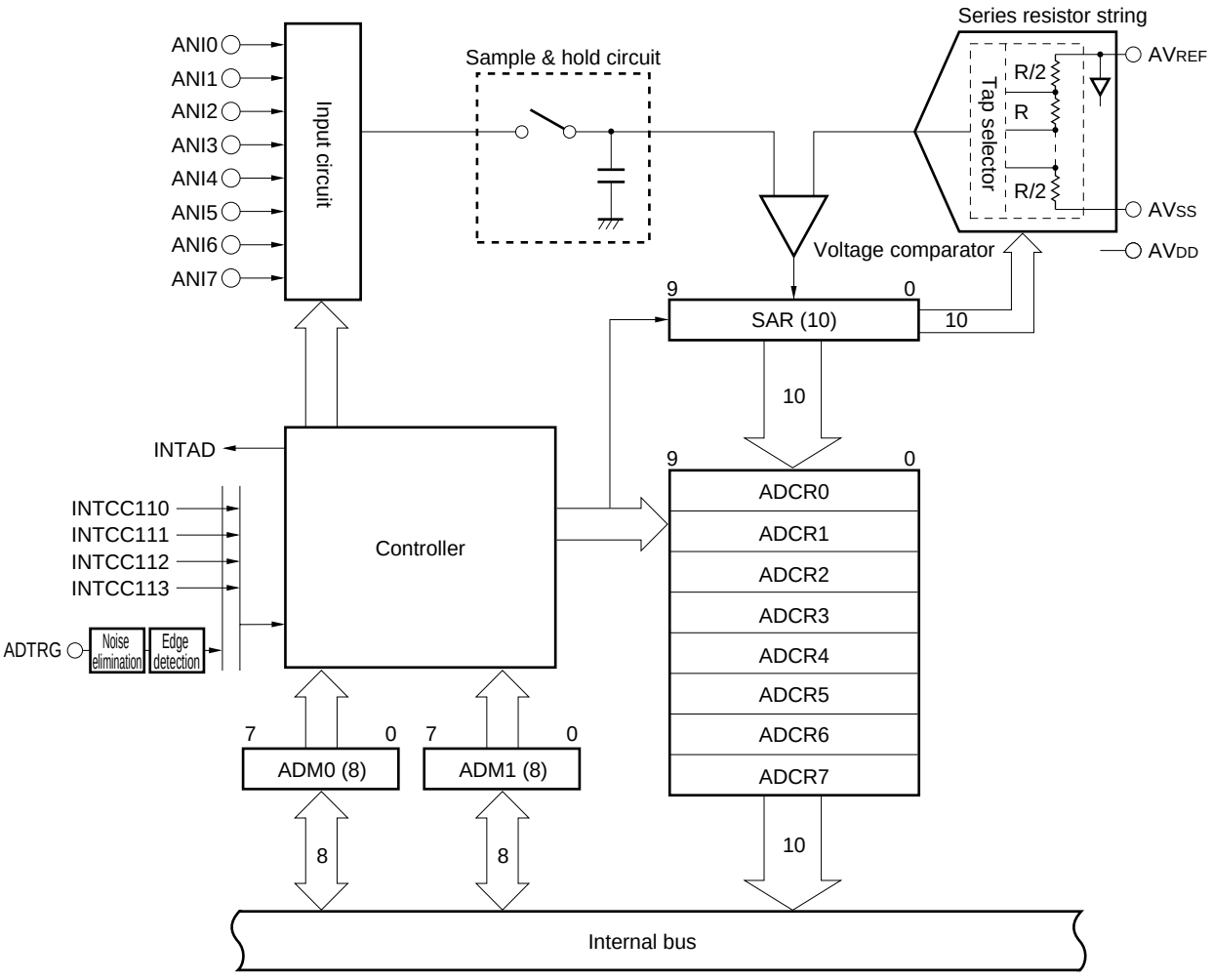
Figure 11-3. Block Diagram of Dedicated Baud Rate Generators 0 to 2 (BRG0 to BRG2)



12. A/D CONVERTER

- Analog input: 8 channels
- On-chip 10-bit A/D converter
- On-chip A/D conversion result registers (ADCR0 to ADCR7)
  10 bits × 8
- A/D conversion trigger modes
  A/D trigger mode
  Timer trigger mode
  External trigger mode
- Successive approximation method

Figure 12-1. A/D Converter Block Diagram



13. PORT FUNCTIONS

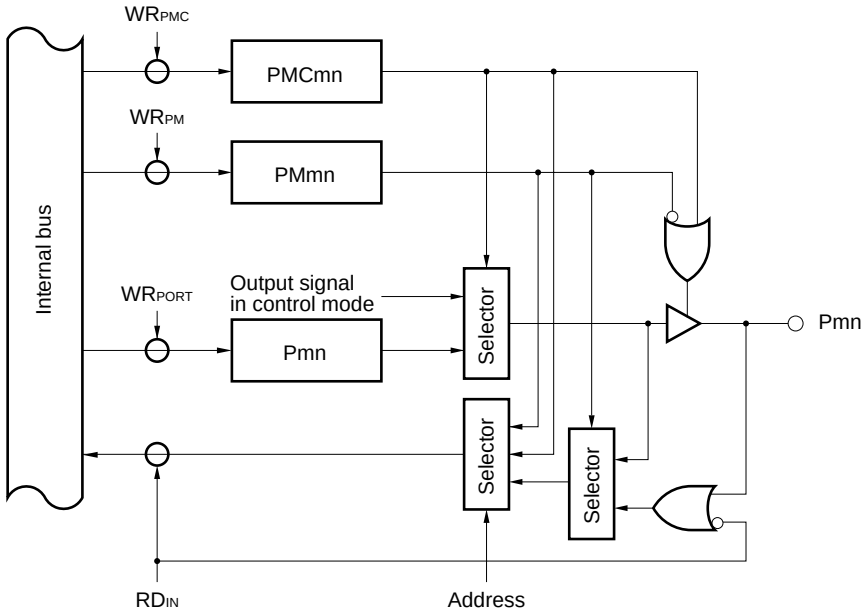
- Number of ports
  Dedicated input ports: 9
  Input/output ports: 114
- Shares pins with other peripheral function I/O
- Input and output can be specified in 1-bit units

The block diagrams of the various ports are divided into 16 block types identified by A to P as shown in Table 13-1. Figures 13-1 to 13-16 show the block diagrams of each type.

Table 13-1. List of Port Block Types

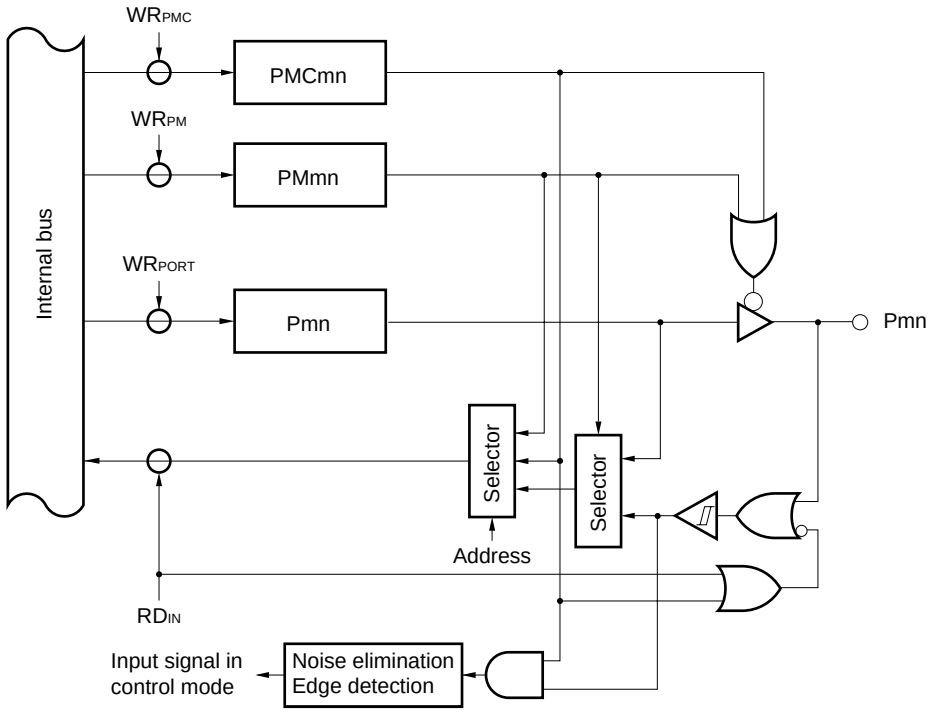
Port Name	Pin Name	Port Function	Function in Control Mode	Block Type
Port 0	P00 to P07	8-bit input/output	Input/output of real-time pulse unit (RPU), external interrupt input, DMA controller (DMAC) input	A, B, M
Port 1	P10 to P17	8-bit input/output	Input/output of real-time pulse unit (RPU), external interrupt input, DMA controller (DMAC) output	A, B, K
Port 2	P20 to P27	1-bit input, 7-bit input/output	NMI input, serial interface (UART0/CSI0, UART1/CSI1) input/output	A, C, D, I, J
Port 3	P30 to P37	8-bit input/output	Input/output of real-time pulse unit (RPU), external interrupt input, serial interface (CSI2) input/output	A, B, K, M, N
Port 4	P40 to P47	8-bit input/output	External data bus (D0 to D7)	E
Port 5	P50 to P57	8-bit input/output	External data bus (D8 to D15)	E
Port 6	P60 to P67	8-bit input/output	External address bus (A16 to A23)	F
Port 7	P70 to P77	8-bit input	A/D converter (ADC) analog input	G
Port 8	P80 to P87	8-bit input/output	External bus interface control signal output	O, P
Port 9	P90 to P97	8-bit input/output	External bus interface control signal input/output	H, O
Port 10	P100 to P107	8-bit input/output	Input/output of real-time pulse unit (RPU), external interrupt input, DMA controller (DMAC) output	A, B, K
Port 11	P110 to P117	8-bit input/output	Input/output of real-time pulse unit (RPU), external interrupt input, serial interface (CSI3) input/output	A, B, K, M, N
Port 12	P120 to P127	8-bit input/output	Input/output of real-time pulse unit (RPU), external interrupt input, A/D converter (ADC) external trigger input	A, B
Port A	PA0 to PA7	8-bit input/output	External address bus (A0 to A7)	F
Port B	PB0 to PB7	8-bit input/output	External address bus (A8 to A15)	F
Port X	PX5 to PX7	3-bit input/output	Refresh request signal output, wait insertion signal input, internal system clock output	A, L

Figure 13-1. Block Diagram of Type A



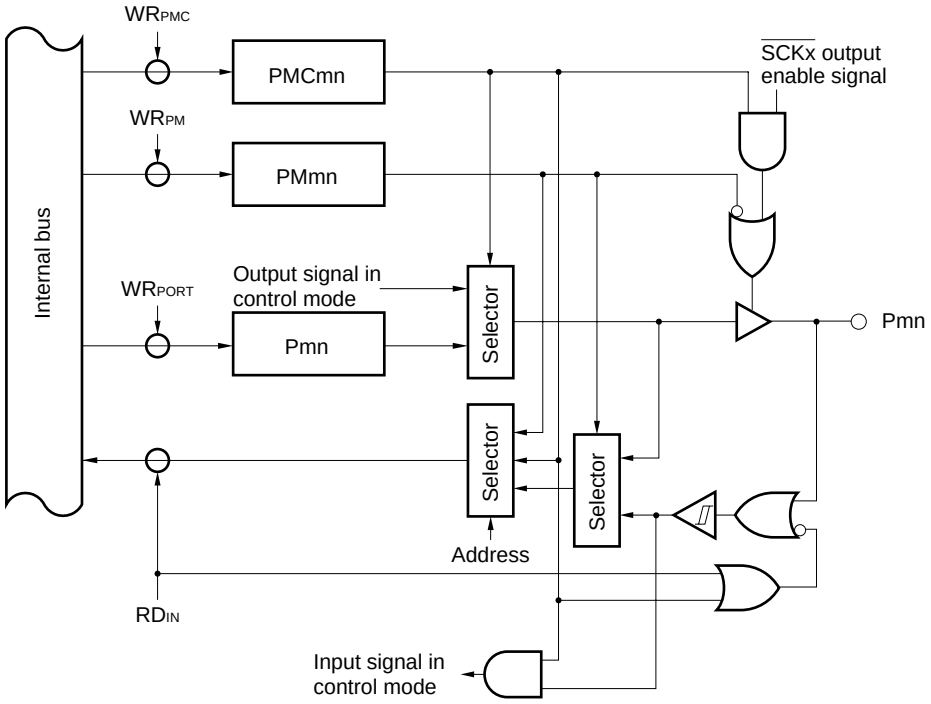
Remark m: port number
n: bit number

Figure 13-2. Block Diagram of Type B



Remark m: port number
n: bit number

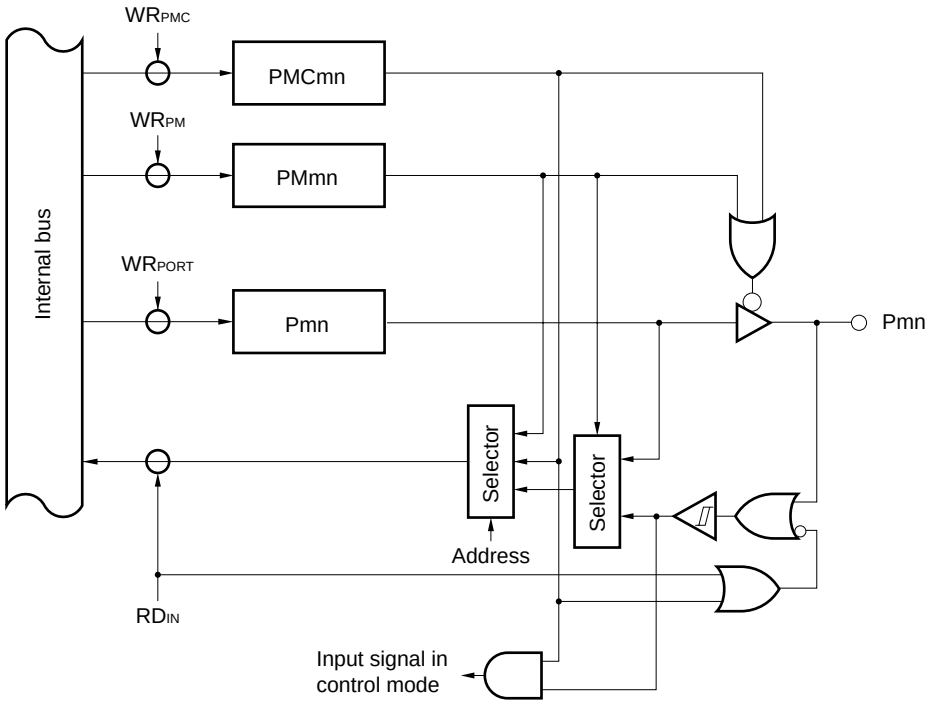
Figure 13-3. Block Diagram of Type C



Remark mn: 24, 27

x: 0 (when mn = 24), 1 (when mn = 27)

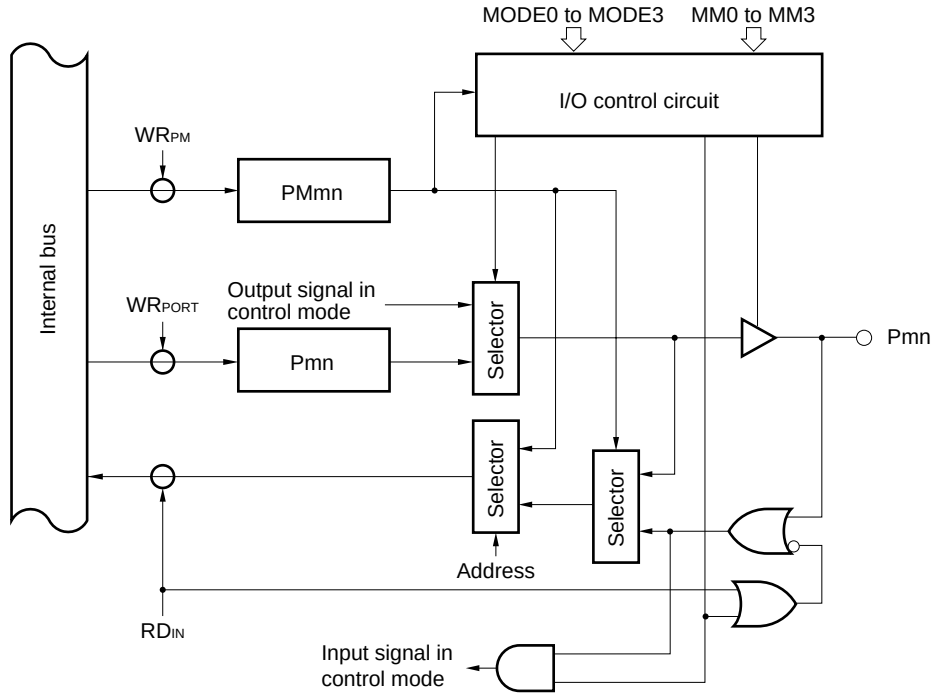
Figure 13-4. Block Diagram of Type D



Remark m: port number

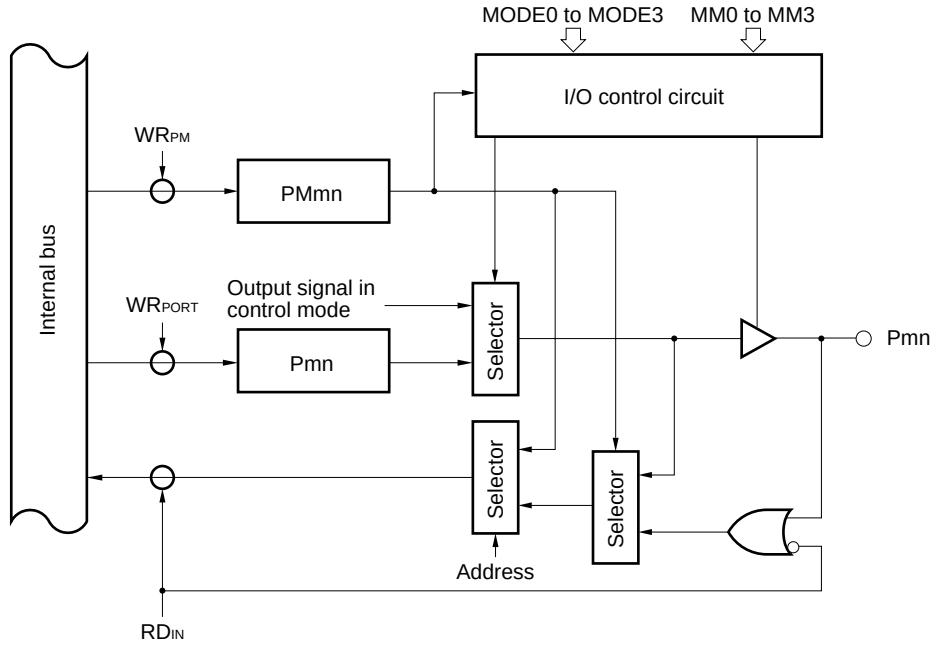
n: bit number

Figure 13-5. Block Diagram of Type E



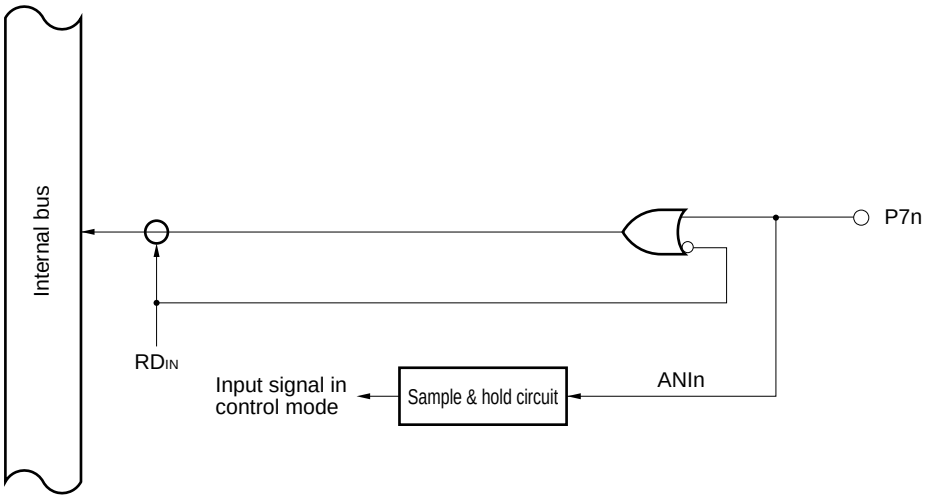
Remark m: port number
n: bit number

Figure 13-6. Block Diagram of Type F



Remark m: port number
n: bit number

Figure 13-7. Block Diagram of Type G



Remark n = 0 to 7

Figure 13-8. Block Diagram of Type H

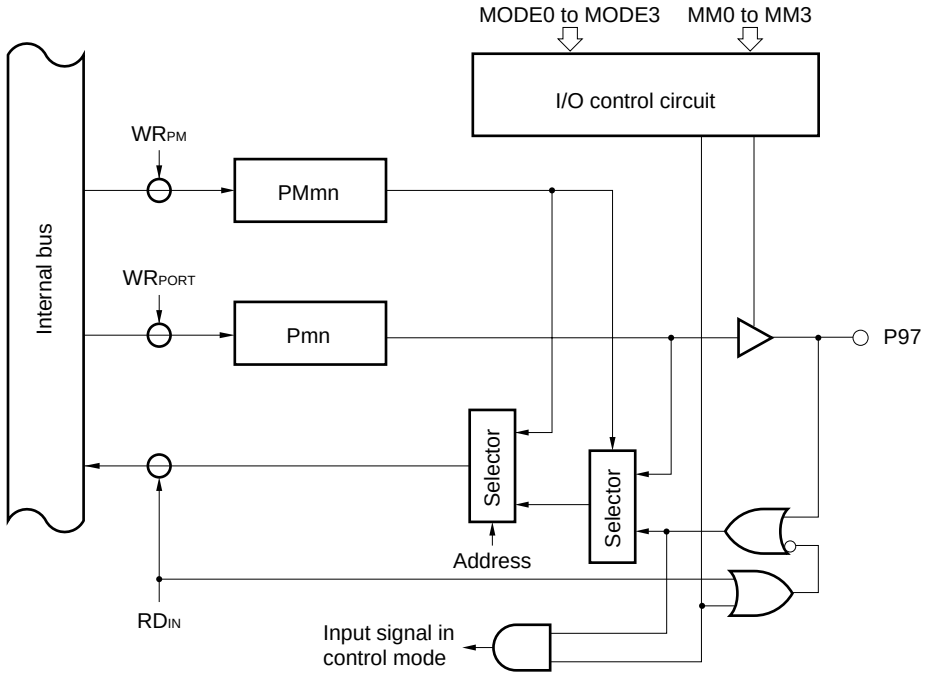


Figure 13-9. Block Diagram of Type I

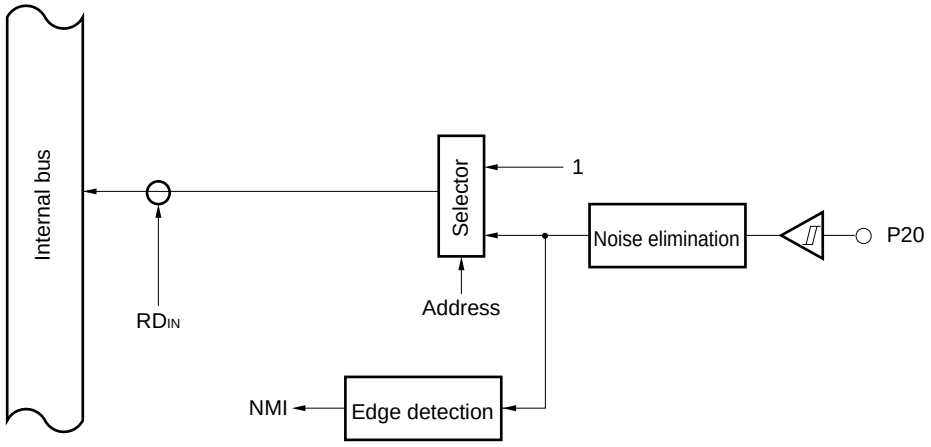
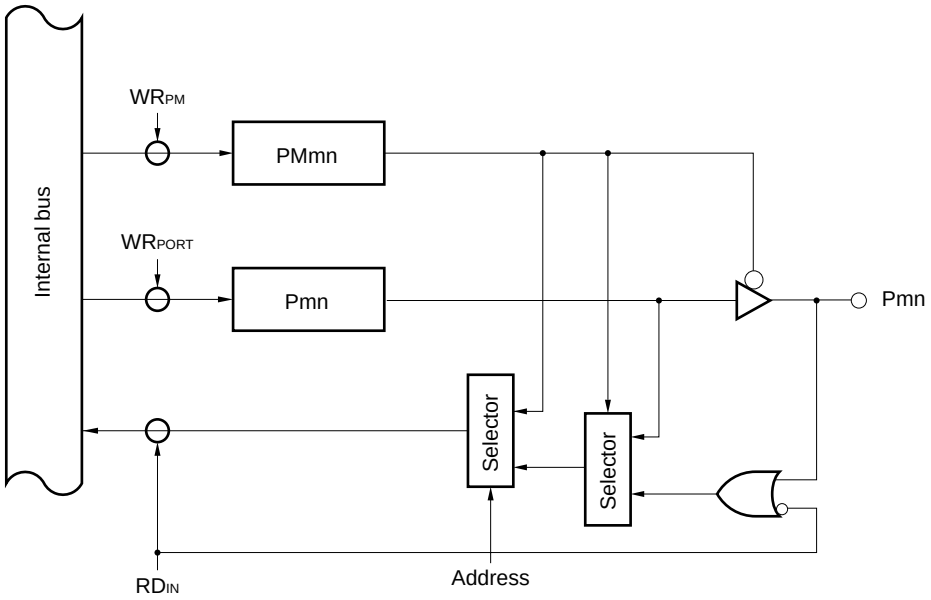
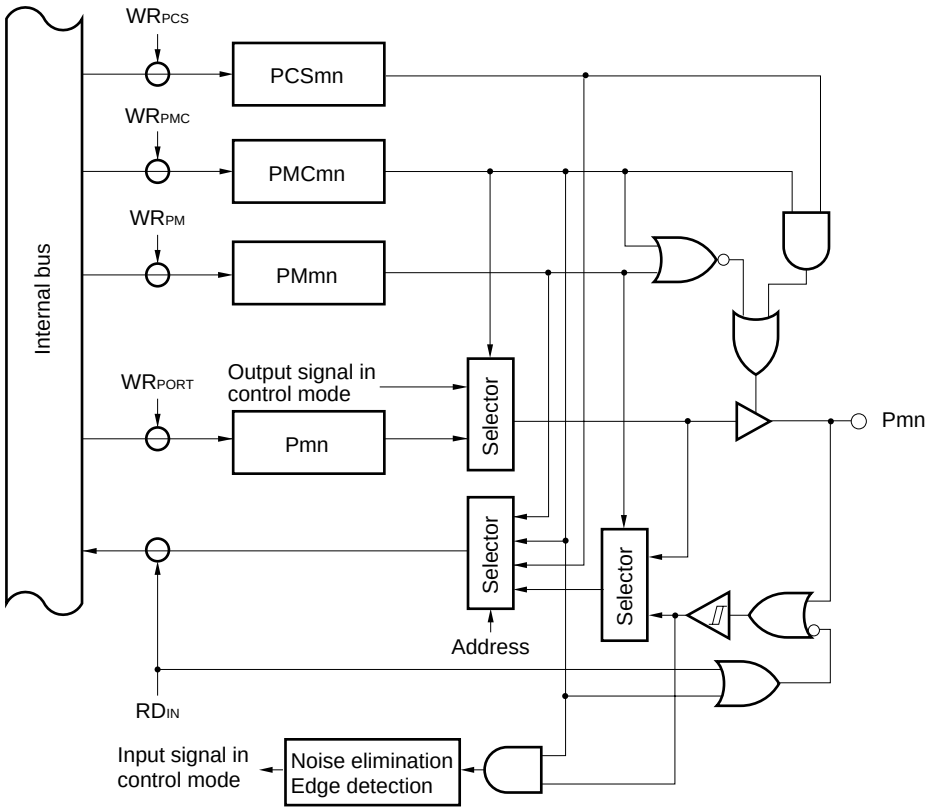


Figure 13-10. Block Diagram of Type J



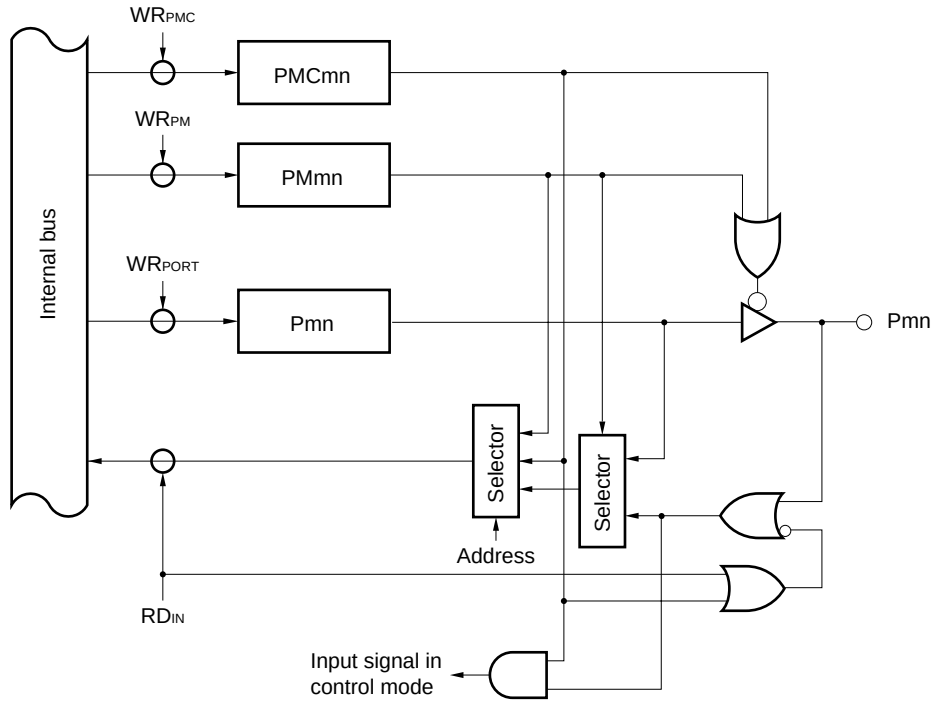
Remark m: port number
n: bit number

Figure 13-11. Block Diagram of Type K



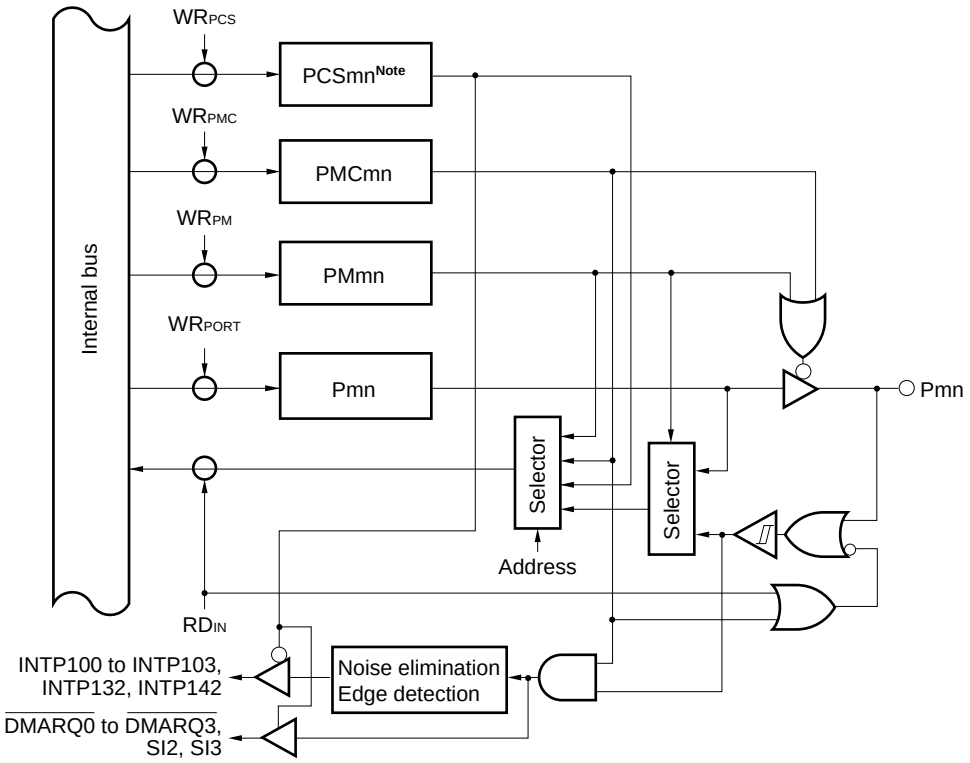
Remark m: port number
n: bit number

Figure 13-12. Block Diagram of Type L



Remark m: port number
n: bit number

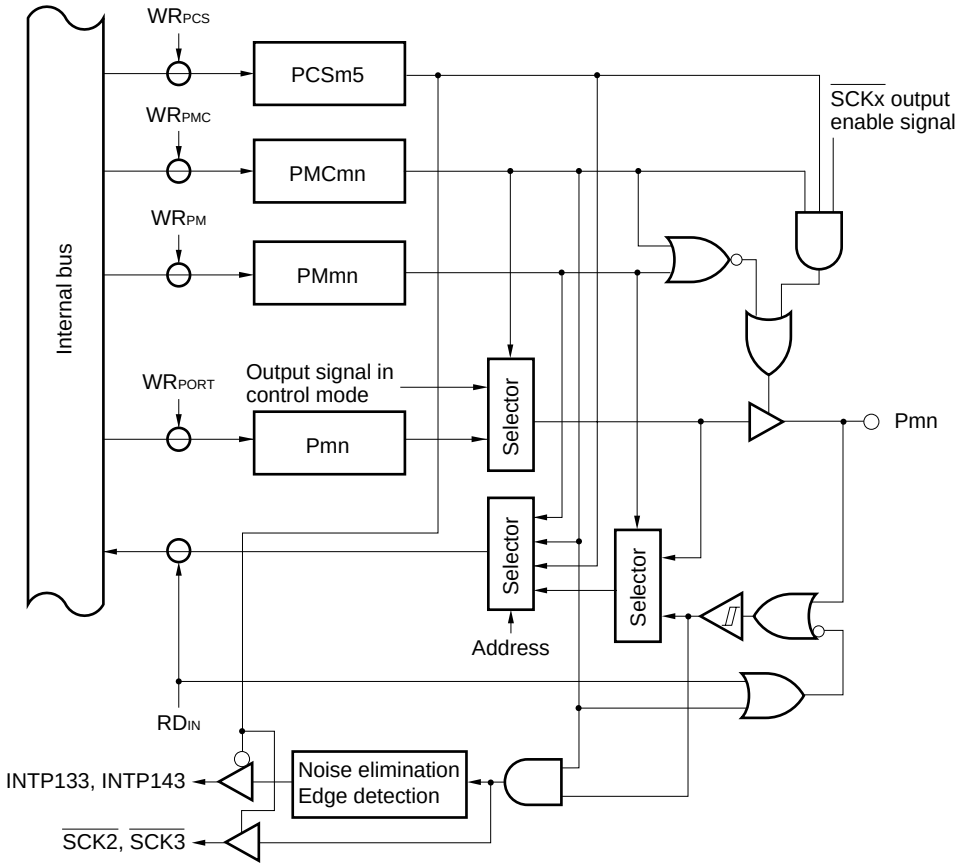
Figure 13-13. Block Diagram of Type M



Note When mn = 36: PCS35
When mn = 116: PCS115

Remark mn: 04 to 07, 36, 116

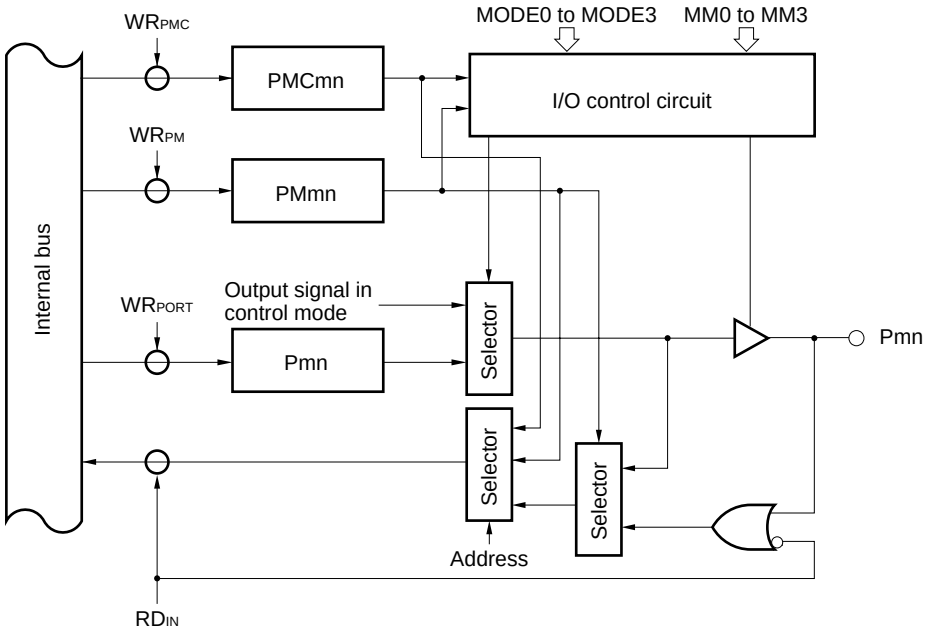
Figure 13-14. Block Diagram of Type N



Remark mn: 37, 117

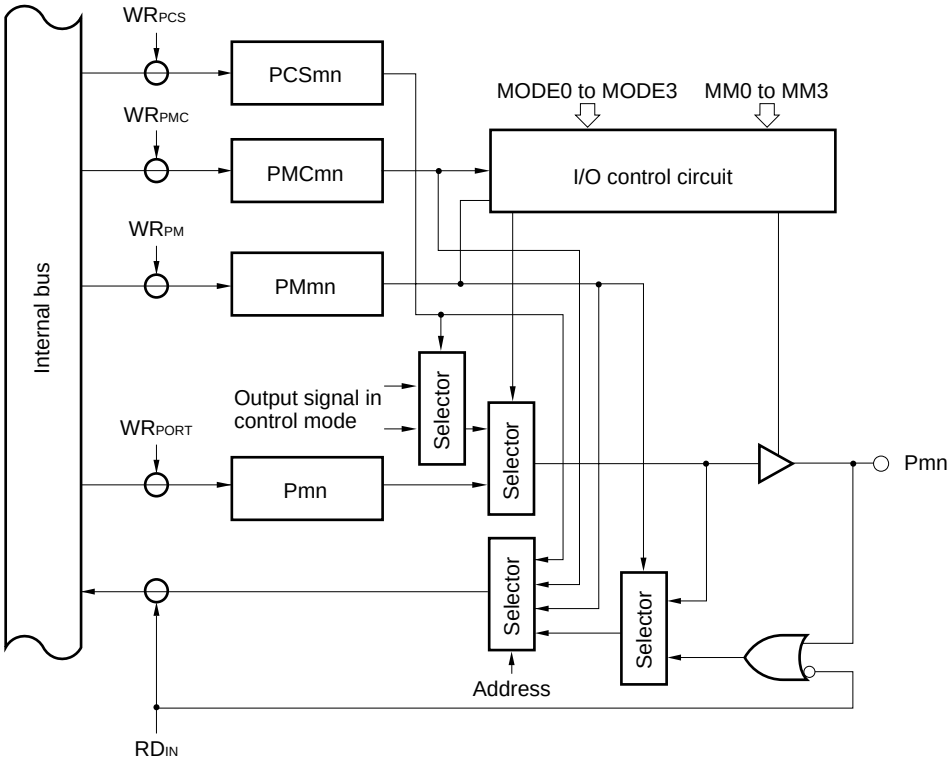
x: 2 (when mn = 37), 3 (when mn = 117)

Figure 13-15. Block Diagram of Type O



Remark m: port number
n: bit number

Figure 13-16. Block Diagram of Type P



Remark m: port number
n: bit number

14. RESET FUNCTION

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, a system reset is performed and the various on-chip hardware devices are initialized.

When the $\overline{\text{RESET}}$ input changes from low to high, the reset state is canceled and the CPU begins program execution (the contents of the various registers should be initialized within the program as necessary).

An on-chip noise elimination circuit, which uses analog delay (≒ 60 ns) to eliminate noise, is provided for the $\overline{\text{RESET}}$ pin.

15. INSTRUCTION SET

Table 15-1. Symbols Used to Describe Operands

Symbol	Description
reg1	General registers (r0 to r31): used as source registers
reg2	General registers (r0 to r31): used mainly as destination registers
reg3	General registers (r0 to r31): used mainly to store the remainders of division results and the higher 3 bits of multiplication results
imm×	×-bit immediate
disp×	×-bit displacement
regID	System register number
bit#3	3-bit data for specifying the bit number
ep	Element pointer (r30)
cccc	4-bit data indicating the condition code
vector	5-bit data used for specifying the trap vector (00H to 1FH)
list×	List of × registers

Table 15-2. Symbols Used to Describe Opcodes

Symbol	Description
R	1-bit data of code specifying reg1 or regID
r	1-bit data of code specifying reg2
w	1-bit data of code specifying reg3
d	1-bit displacement data
i	1-bit immediate data
cccc	4-bit data indicating condition code
bbb	3-bit data for specifying bit number
L	1-bit data specifying register list

Table 15-3. Symbols Used in Operation

Symbol	Description
←	Input for
GR [ ]	General register
SR [ ]	System register
zero-extend (n)	Extend n with zeros until word length
sign-extend (n)	Extend n with signs until word length
load-memory (a, b)	Read data of size b from address a
store-memory (a, b, c)	Write data b of address a by size c
load-memory-bit (a, b)	Read bit b of address a
store-memory-bit (a, b, c)	Write c to bit b of address a
saturated (n)	Execute saturation processing of n (n is a two's complement) If, as a result of the calculation, n ≥ 7FFFFFFFH, let it be 7FFFFFFFH. n ≤ 80000000H, let it be 80000000H
result	Reflect the result in a flag
Byte	Byte (8 bits)
Half-word	Half word (16 bits)
Word	Word (32 bits)
+	Add
–	Subtract
||	Bit concatenation
×	Multiply
÷	Divide
%	Remainder of division result
AND	Logical AND
OR	Logical OR
XOR	Exclusive OR
NOT	Logical NOT
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

Table 15-4. Symbols Used for Execution Clock

Symbol	Description
i : issue	When executing another instruction immediately after executing an instruction
r : repeat	When repeating the same instruction immediately after executing the instruction
l : latency	When referring to instruction execution results in the next instruction

Table 15-5. Symbols Used in Flag Operations

Identifier	Description
(Blank)	No change
0	Clear to 0
×	Set or cleared according to the results
R	Previously saved values are restored

Table 15-6. Condition Codes

Condition Name (cond)	Condition Code (cccc)	Condition Formula	Description
V	0000	OV = 1	Overflow
NV	1000	OV = 0	No overflow
C/L	0001	CY = 1	Carry Lower (Less than)
NC/NL	1001	CY = 0	No carry Not lower (Greater than or equal)
Z/E	0010	Z = 1	Zero Equal
NZ/NE	1010	Z = 0	Not zero Not equal
NH	0011	(CY or Z) = 1	Not higher (Less than or equal)
H	1011	(CY or Z) = 0	Higher (Greater than)
N	0100	S = 1	Negative
P	1100	S = 0	Positive
T	0101	–	Always (unconditional)
SA	1101	SAT = 1	Saturated
LT	0110	(S xor OV) = 1	Less than signed
GE	1110	(S xor OV) = 0	Greater than or equal signed
LE	0111	((S xor OV) or Z) = 1	Less than or equal signed
GT	1111	((S xor OV) or Z) = 0	Greater than signed

Instruction Set

(1/7)

Mnemonic	Operand	Opcode	Operation		Execution Clock i	Execution Clock r	Execution Clock l	Flags CY	Flags OV	Flags S	Flags Z	Flags SAT
ADD	reg1,reg2	rrrrr001110RRRRR	GR[reg2]←GR[reg2]+GR[reg1]		1	1	1	×	×	×	×	
	imm5,reg2	rrrrr010010iiiii	GR[reg2]←GR[reg2]+sign-extend(imm5)		1	1	1	×	×	×	×	
ADDI	imm16,reg1,reg2	rrrrr110000rrrrr iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)		1	1	1	×	×	×	×	
AND	reg1,reg2	rrrrr001010RRRRR	GR[reg2]←GR[reg2]AND GR[reg1]		1	1	1		0	×	×	
ANDI	imm16,reg1,reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]AND zero-extend(imm16)		1	1	1		0	0	×	
Bcond	disp9	ddddd1011dddccc **Note 1**	if conditions are satisfied then PC ← PC+sign-extend(disp9)	When conditions are satisfied	2 Note 2	2 Note 2	2 Note 2					
				When conditions are not satisfied	1	1	1					
BSH	reg2,reg3	rrrrr111111100000 wwwww0110100010	GR[reg3]←GR[reg2] (23 : 16) II GR[reg2] (31 : 24) II GR[reg2] (7 : 0) II GR[reg2] (15 : 8)		1	1	1	×	0	×	×	
BSW	reg2,reg3	rrrrr111111100000 wwwww0110100000	GR[reg3]←GR[reg2] (7 : 0) II GR[reg2] (15 : 8) II GR[reg2] (23 : 16) II GR[reg2] (31 : 24)		1	1	1	×	0	×	×	
CALLT	imm6	0000001000iiiiii	CTPC←PC+2(return PC) CTPSW←PSW adr←CTBP+zero-extend(imm6 logically shift left by 1) PC←CTBP+zero-extend(Load-memory(adr, Half-word))		4	4	4					
CLR1	bit#3, disp 16[reg1]	10bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flags←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit (adr,bit#3,0)		3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100100	adr←GR[reg1] Z flags←Not(Load-memory-bit(adr,reg2)) Store-memory-bit (adr,reg2,0)		3 Note 3	3 Note 3	3 Note 3				×	
CMOV	cccc,imm5,reg2, reg3	rrrrr111111iiiii wwwww011000cccc0	if condition are satisfied then GR[reg3]←sign-extended(imm5) else GR[reg3]←GR[reg2]		1	1	1					
	cccc,reg1,reg2, reg3	rrrrr111111RRRRR wwwww011001cccc0	if conditions are satisfied then GR[reg3]←GR[reg1] else GR[reg3]←GR[reg2]		1	1	1					
CMP	reg1,reg2	rrrrr001111RRRRR	result←GR[reg2]–GR[reg1]		1	1	1	×	×	×	×	
	imm5,reg2	rrrrr010011iiiii	result←GR[reg2]–sign-extend(imm5)		1	1	1	×	×	×	×	
CTRET		0000011111100000 0000000101000100	PC←CTPC PSW←CTPSW		3	3	3	R	R	R	R	R
DI		0000011111100000 0000000101100000	PSW.ID←1		1	1	1					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
DISPOSE	imm5,list12	0 0 0 0 0 1 1 0 0 1 i i i i i L L L L L L L L L L L L 0 0 0 0 0	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded	N+1 Note 4	N+1 Note 4	N+1 Note 4					
	imm5,list12,[reg1]	0 0 0 0 0 1 1 0 0 1 i i i i i L L L L L L L L L L L L R R R R R **Note 5**	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list 12 is loaded PC←GR[reg1]	N+3 Note 4	N+3 Note 4	N+3 Note 4					
DIV	reg1,reg2,reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 1 0 0 0 0 0 0	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	35	35	35					
DIVH	reg1,reg2	r r r r r 0 0 0 0 1 0 R R R R R	GR[reg2]←GR[reg2]÷GR[reg1] Note 6	35	35	35	×	×	×		
	reg1,reg2,reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 0 0 0 0 0 0 0	GR[reg2]←GR[reg2]÷GR[reg1] Note 6 GR[reg3]←GR[reg2]%GR[reg1]	35	35	35	×	×	×		
DIVHU	reg1,reg2,reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 0 0 0 0 1 0	GR[reg2]←GR[reg2]÷GR[reg1] Note 6 GR[reg3]←GR[reg2]%GR[reg1]	34	34	34	×	×	×		
DIVU	reg1,reg2,reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 1 0 0 0 1 0	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	34	34	34	×	×	×		
EI		1 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID←0	1	1	1					
HALT		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0	Stop	1	1	1					
HSW	reg2,reg3	r r r r r 1 1 1 1 1 1 0 0 0 0 0 w w w w w 0 1 1 0 1 0 0 0 1 0 0	GR[reg3]←GR[reg2] (15 : 0) II GR[reg2] (31: 16)	1	1	1	×	0	×	×	
JARL	disp22,reg2	r r r r r 1 1 1 1 0 d d d d d d d d d d d d d d d d d d d d d 0 **Note 7**	GR[reg2]←PC+4 PC←PC+sign–extend(disp22)	2	2	2					
JMP	[reg1]	0 0 0 0 0 0 0 0 0 0 1 1 R R R R R	PC←GR[reg1]	3	3	3					
JR	disp22	0 0 0 0 0 1 1 1 1 0 d d d d d d d d d d d d d d d d d d d d d 0 **Note 7**	PC←PC+sign-extend(disp22)	2	2	2					
LD.B	disp16[reg1],reg2	r r r r r 1 1 1 0 0 0 R R R R R d d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory (adr,Byte))	1	1	n Note 9					

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Mnemonic	Operand	Opcode	Operation		Execution Clock			Flags				
					i	r	l	CY	OV	S	Z	SAT
LD.BU	disp16[reg1],reg2	rrrrr11111bRRRRR ddddddddddddddd1 **Notes 8, 10**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory (adr,Byte))		1	1	n Note 11					
LD.H	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory (adr,Half-word))		1	1	n Note 9					
LD.HU	disp16[reg1],reg2	rrrrr111111RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory (adr,Half-word))		1	1	n Note 11					
LD.W	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←Load-memory(adr,Word)		1	1	n Note 9					
LDSR	reg2,regID	rrrrr111111RRRRR 0000000000100000 **Note 12**	SR[regID]←GR[reg2]	Other than regID=PSW	1	1	1					
				regID=PSW				×	×	×	×	×
MOV	reg1,reg2	rrrrr000000RRRRR	GR[reg2]←GR[reg1]		1	1	1					
	imm5,reg2	rrrrr010000iiiii	GR[reg2]←sign-extend(imm5)		1	1	1					
	imm32,reg1	00000110001RRRRR iiiiiiiiiiiiiiii iiiiiiiiiiiiiiii	GR[reg1]←imm32		2	2	2					
MOVEA	imm16,reg1,reg2	rrrrr110001RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+ sign-extend(imm16)		1	1	1					
MOVHI	imm16,reg1,reg2	rrrrr110010RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+(imm16 II 0^{16})		1	1	1					
MUL	reg1,reg2,reg3	rrrrr111111RRRRR wwwww0100010000	GR[reg3] II GR[reg2]←GR[reg2] × GR[reg1]		1	2 Note 14	2					
	imm9,reg2,reg3	rrrrr111111iiiii wwwww0100111110 0	GR[reg3] II GR[reg2]←GR[reg2] × sign-extend(imm9) **Note 13**		1	2 Note 14	2					
MULH	reg1,reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2]Note 6 × GR[reg1]Note 6		1	1	2					
	imm5,reg2	rrrrr010111iiiii	GR[reg2]←GR[reg2]Note 6 × sign-extend (imm5)		1	1	2					
MULHI	imm16,reg1,reg2	rrrrr11011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]Note 6 × imm16		1	1	2					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
MULU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww0100010010	GR[reg3] II GR[reg2]←GR[reg2] × GR[reg1]	1	2 Note 14	2					
	imm9,reg2,reg3	rrrrr111111iiiii wwwww0100111110	GR[reg3] II GR[reg2]←GR[reg2] × zero-extend(imm9) **Note 13**	1	2 Note 14	2					
NOP		0000000000000000	Pass at least one clock cycle doing nothing	1	1	1					
NOT	reg1,reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])	1	1	1		0	×	×	
NOT1	bit#3,disp16[reg1]	01bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,Z flag)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100010	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,Z flag)	3 Note 3	3 Note 3	3 Note 3				×	
OR	reg1,reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2] OR GR[reg1]	1	1	1		0	×	×	
ORI	imm16,reg1,reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1] OR zero-extend(imm16)	1	1	1		0	×	×	
PREPARE	list12,imm5	0000011110iiiiiL LLLLLLLLLLL00001	Store-memory(sp-4,GR[reg in list12],Word) sp←sp-4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5)	N+1 Note 4	N+1 Note 4	N+1 Note 4					
	list12,imm5, sp/imm[Note 15]	0000011110iiiiiL LLLLLLLLLLLff011 imm16/imm32 **Note 16**	Store-memory(sp-4,GR[reg in list12],Word) sp←sp-4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5) ep←sp/imm	N+2 Note 4 Note 17	N+2 Note 4 Note 17	N+2 Note 4 Note 17					
RETI		0000011111100000 0000000101000000	if PSW.EP=1 then PC ←EIPC PSW ←EIPSW else if PSW.NP = 1 then PC ←FEPC PSW ←FEPSW else PC ←EIPC PSW ←EIPSW	3	3	3	R	R	R	R	R
SAR	reg1,reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010101iiiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SASF	cccc,reg2	rrrrr111110ccccc 0000001000000000	if conditions are satisfied then GR[reg2]←(GR[reg2] Logically shift left by 1) OR 00000001H else GR[reg2]←(GR[reg2] Logically shift left by 1) OR 00000000H	1	1	1					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SATADD	reg1,reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	1	1	1	×	×	×	×	×
	imm5,reg2	rrrrr010001iiiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5)	1	1	1	×	×	×	×	×
SATSUB	reg1,reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]–GR[reg1])	1	1	1	×	×	×	×	×
SATSUBI	imm16,reg1,reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]–sign-extend(imm16)	1	1	1	×	×	×	×	×
SATSUBR	reg1,reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]–GR[reg2])	1	1	1	×	×	×	×	×
SETF	cccc,reg2	rrrrr111111ccccc 0000000000000000	If conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H	1	1	1					
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	n Note 9					
SLD.BU	disp4[ep],reg2 **Note 18**	rrrrr00001110dddd	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	n Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 19**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Half-word))	1	1	n Note 9					
SLD.HU	disp5[ep],reg2 **Notes 18, 20**	rrrrr00001111dddd	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Half-word))	1	1	n Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010ddddddd0 **Note 21**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word))	1	1	n Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 19**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Half-word)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 21**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR ddddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Half-word)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					
SUB	reg1,reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	1	1	1	×	×	×	×	
SUBR	reg1,reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	1	1	1	×	×	×	×	
SWITCH	reg1	0000000001 0RRRRR	adr←(PC+2)+(GR[reg1] logically shift left by 1) PC←(PC+2)+(sign-extend(Load-memory(adr,Half-word))) logically shift left by 1	5	5	5					
SXB	reg1	0000000101RRRRR	GR[reg1]←sign-extend (GR[reg1] (7 : 0)	1	1	1					
SXH	reg1	0000000111RRRRR	GR[reg1]←sign-extend (GR[reg1] (15 : 0))	1	1	1					
TRAP	vector	00001111111iiiii 0000000100000000	EIPC ←PC+4 (restore PC) EIPSW ←PSW ECR.EICC ←Interrupt code PSW.EP ←1 PSW.ID ←1 PC ←00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1,reg2	rrrrr001011RRRRR	result←GR[reg2] AND GR[reg1]	1	1	1		0	×	×	
TST1	bit#3,disp16[reg1]	11bbb111110RRRRR ddddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3))	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100110	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2))	3 Note 3	3 Note 3	3 Note 3				×	

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
XOR	reg1,reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1		0	×	×	
XORI	imm16,reg1,reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1] XOR zero-extend (imm16)	1	1	1		0	×	×	
ZXB	reg1	0000000100RRRRR	GR[reg1]←zero-extend(GR[reg1] (7 : 0))	1	1	1					
ZXH	reg1	0000000110RRRRR	GR[reg1]←zero-extend(GR[reg1] (15 : 0))	1	1	1					

Notes 1. ddddddddd: Higher 8 bits of disp9.

2. 3 clocks if the final instruction includes PSW write access.

3. If there is no wait state (3 + the number of read access wait states).

4. N is the total number of list 12 read registers (according to the number of wait states. Also, if there are no wait states, N is the number of list 12 registers.).

5. RRRRR other than 00000.

6. Only the lower half word data are valid.

7. ddddddddddddddddddddd: Higher 21 bits of disp22.

8. ddddddddddddddd: Higher 15 bits of disp16.

9. According to the number of wait states (1 if there are no wait states).

10. b: bit 0 of disp16.

11. According to the number of wait states (2 if there are no wait states).

12. In this instruction, for convenience of mnemonic description, the source register is made reg2, but the reg1 field is used in the op code. Therefore, the meaning of the register specification in the mnemonic description and in the opcode differs from other instructions.
rrrrr: regID specification
RRRRR: reg2 specification

13. 11111: Lower 5 bits of imm9.
1111: Lower 4 bits of imm9.

14. 1 when r = w (the lower 32 bits of the results are not written in the register) or w = r0 (the higher 32 bits of the results are not written in the register).

15. sp/imm: specified by bits 19 and 20 of the sub opcode.

16. ff = 00: load sp in ep.
01: load sign expanded 16-bit immediate data (bits 47 to 32) in ep.
10: load 16-bit logically left shifted 16-bit immediate data (bits 47 to 32) in ep.
11: load 32-bit immediate data (bits 63 to 32) in ep.

17. If imm=imm32, N + 3 clocks.

18. rrrrr other than 00000.

19. ddddddd: Higher 7 bits of disp8.

20. dddd: Higher 4 bits of disp5.

21. dddddd: Higher 6 bits of disp8.

16. ELECTRICAL SPECIFICATIONS (PRELIMINARY VALUES)

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage	V_{DD}	V_{DD} pin		–0.5 to +4.6	V
	HV_{DD}	HV_{DD} pin, $HV_{DD} \geq V_{DD}$		–0.5 to +4.6	V
	CV_{DD}	CV_{DD} pin		–0.5 to +4.6	V
	CV_{SS}	CV_{SS} pin		–0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin		–0.5 to HV_{DD} + 0.5	V
	AV_{SS}	AV_{SS} pin		–0.5 to +0.5	V
Input voltage	V_I	X1 pin, except MODE3 pin		–0.5 to HV_{DD} + 0.5	V
		MODE3 pin		–0.5 to V_{DD} + 0.5	V
Clock input voltage	V_K	X1, V_{DD} = 3.0 to 3.6 V		–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin		4.0	mA
		Total of all pins		100	mA
Output current, high	I_{OH}	1 pin		–4.0	mA
		Total of all pins		–100	mA
Output voltage	V_O	HV_{DD} = 3.0 V to 3.6 V		–0.5 to HV_{DD} + 0.5	V
Analog input voltage	V_{IAN}	P70/ANI0 to P77/ANI7 pins	$AV_{DD} > HV_{DD}$	–0.5 to HV_{DD} + 0.5	V
			$HV_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	V
A/D converter reference input voltage	AV_{REF}	$AV_{DD} > HV_{DD}$		–0.5 to HV_{DD} + 0.5	V
		$HV_{DD} \geq AV_{DD}$		–0.5 to AV_{DD} + 0.5	V
Operating ambient temperature	T_A	μPD703100A-40		–40 to +70	°C
		μPD703100A-33, 703101A-33, 703102A-33		–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution 1. Do not make direct connections of the output (or input/output) pins of the IC product with each other, and also avoid direct connections to V_{DD}, V_{CC}, or GND. However, the open drain pins or the open collector pins can be directly connected with each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to high-impedance state.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD} = HV_{DD} = CV_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)		Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD}, HV_{DD})
Direct mode	μPD703100A-40	2 to 40 MHz	−40 to +70°C	3.0 to 3.6 V
	μPD703100A-33	2 to 33 MHz	−40 to +85°C	
	μPD703101A-33, 703102A-33	10 to 33 MHz	−40 to +85°C	
PLL mode	μPD703100A-40	2 to 40 MHz[Note 1]	−40 to +70°C	
	μPD703100A-33	2 to 33 MHz[Note 2]	−40 to +85°C	
★	μPD703101A-33, 703102A-33	20 to 33 MHz[Note 2]	−40 to +85°C	

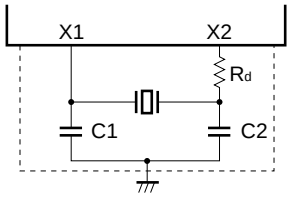
Notes 1. The input clock frequency used in PLL mode should be 4.0 to 8.0 MHz.

2. The input clock frequency used in PLL mode should be used by 4.0 to 6.6 MHz.

Recommended Oscillation Circuits

(a) Ceramic resonator (T_A = –40 to +70°C ... μPD703100A-40,
T_A = –40 to +85°C ... μPD703100A-33, 703101A-33, 703102A-33)

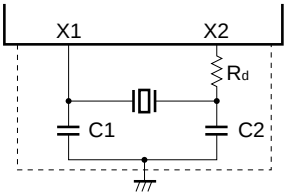
(i) Murata Mfg. Co., Ltd.



Type	Product Name	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
Surface mount	CSAC2.00MGC040	2.0	100	100	0	3.0	3.6	0.4
	CSTC2.00MG	2.0	On-chip	On-chip	1.0	3.0	3.6	0.2
	CSAC3.20MGC040	3.2	100	100	0	3.0	3.6	0.4
	CSTC3.20MG	3.2	On-chip	On-chip	1.0	3.0	3.6	0.2
	CSAC4.00MGC040	4.0	100	100	0	3.0	3.6	0.5
	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.3
	CSAC5.00MGC040	5.0	100	100	0	3.0	3.6	0.4
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.2
	CSAC6.60MT	6.6	30	30	0	3.0	3.6	0.2
	CSTCC6.60MG0H6	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSAC8.00MT	8.0	30	30	0	3.0	3.6	0.2
	CSTCC8.00MG0H6	8.0	On-chip	On-chip	0	3.0	3.6	0.3
Lead	CSA2.00MG040	2.0	100	100	0	3.0	3.6	0.4
	CST2.00MG040	2.0	On-chip	On-chip	0	3.0	3.6	0.4
	CSA3.20MG040	3.2	100	100	0	3.0	3.6	0.4
	CST3.20MGW040	3.2	On-chip	On-chip	0	3.0	3.6	0.4
	CSA4.00MG040	4.0	100	100	0	3.0	3.6	0.5
	CST4.00MGW040	4.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA5.00MG040	5.0	100	100	0	3.0	3.6	0.5
	CST5.00MGW040	5.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA6.60MTZ	6.6	30	30	0	3.0	3.6	0.1
	CST6.60MTW	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSA8.00MTZ	8.0	30	30	0	3.0	3.6	0.1
	CST8.00MTW	8.0	On-chip	On-chip	0	3.0	3.6	0.1

Cautions 1. Connect the oscillation circuits as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area indicated by the broken line.
3. Thoroughly evaluate the matching between the μPD703100A-33, 703100A-40, 703101-A33, 703102A-33 and the resonators.

(ii) TDK Corporation (T_A = –40 to +85°C)



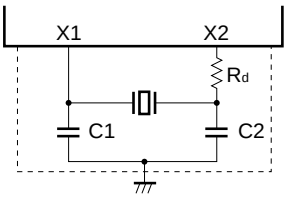
Type	Product Name	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
TDK	CCR4.0MC3	4.0	On-chip	On-chip	0	3.0	3.6	0.17
	CCR5.0MC3	5.0	On-chip	On-chip	0	3.0	3.6	0.15
	CCR8.0MC5	8.0	On-chip	On-chip	0	3.0	3.6	0.11

Cautions 1. Connect the oscillation circuits as closely to the X1 and X2 pins as possible.

2. Do not wire any other signal lines in the area indicated by the broken line.

3. Thoroughly evaluate the matching between the μPD703100A-33, 703100A-40, 703101A-33, 703102A-33 and the resonators.

(iii) Kyocera Corporation (T_A = –20 to +80°C)



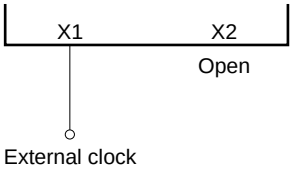
Type	Product Name	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
Kyocera	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.00BR-A	6.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.60BR-A	6.6	On-chip	On-chip	0	3.0	3.6	0.06

Cautions 1. Connect the oscillation circuits as closely to the X1 and X2 pins as possible.

2. Do not wire any other signal lines in the area indicated by the broken line.

3. Thoroughly evaluate the matching between the μPD703100A-33, 703100A-40, 703101A-33, 703102A-33 and the resonators.

(b) External clock input (TA = –40 to +70°C ... μPD703100A-40,
TA = –40 to +85°C ... μPD703100A-33, 703101A-33, 703102A-33)



Caution Input CMOS-level voltage to the X1 pin.

Cautions when turning on/off the power

The μPD703100A-33, 703100A-40, 703101A-33, and 703102A-33 are configured with power supply pins for internal unit (V_{DD}) and for external pin (HV_{DD}).

Operation guaranteed range is $V_{DD} = HV_{DD}$ = 3.0 to 3.6 V. The input and output state of ports may be undefined when the voltage exceeds this range.

DC Characteristics (T_A = –40 to +70°C ... μPD703100A-40,
T_A = –40 to +85°C ... μPD703100A-33, μPD703101A-33, μPD703102A-33,
V_{DD} = HV_{DD} = CV_{DD} = 3.0 to 3.6 V, = V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	Except **Note 1**		0.65HV_{DD}		HV_{DD} + 0.3	V
		Note 1		0.8HV_{DD}		HV_{DD} + 0.3	V
Input voltage, low	V_{IL}	Except **Note 1** and **Note 2**		–0.5		0.2HV_{DD}	V
		Note 1		–0.5		0.15HV_{DD}	V
Clock input voltage, high	V_{XH}	X1 pin	Direct mode	0.8V_{DD}		V_{DD} + 0.3	V
			PLL mode	0.8V_{DD}		V_{DD} + 0.3	V
Clock input voltage, low	V_{XL}	X1 pin	Direct mode	–0.3		0.15V_{DD}	V
			PLL mode	–0.3		0.15V_{DD}	V
Schmitt-triggered input threshold voltage	HV_T^+	**Note 1**, rising edge			2.0		V
	HV_T^-	**Note 1**, falling edge			1.0		V
Schmitt-triggered input hysteresis width	$HV_T^+ - HV_T^-$	**Note 1**		0.3			V
Output voltage, high	V_{OH}	I_{OH} = –1.0 mA		0.8HV_{DD}			V
Output voltage, low	V_{OL}	I_{OL} = 2.5 mA				0.15HV_{DD}	V
Input leakage current, high	I_{LIH}	Except V_I = HV_{DD} or **Note 2**				10	μA
Input leakage current, low	I_{LIL}	Except V_I = 0 V or **Note 2**				–10	μA
Output leakage current, high	I_{LOH}	V_O = HV_{DD}				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA

Notes 1. P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$

2. When the P70/ANI0 to P77/ANI7 pins are used as analog input.

Remarks 1. TYP. values are reference values for when T_A = 25°C, V_{DD} = CV_{DD} = HV_{DD} = 3.3 V.

2. Direct mode:

f_X = 2 to 40 MHz (μPD703100A-40)

f_X = 2 to 33 MHz (μPD703100A-33)

f_X = 10 to 33 MHz (μPD703101A-33, 703102A-33)

PLL mode:

f_X = 2 to 40 MHz (μPD703100A-40)

f_X = 2 to 33 MHz (μPD703100A-33)

f_X = 20 to 33 MHz (μPD703101A-33, 703102A-33)

DC Characteristics (T_A = –40 to +70°C ... μPD703100A-40,
T_A = –40 to +85°C ... μPD703100A-33, μPD703101A-33, μPD703102A-33,
V_{DD} = CV_{DD} = HV_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply current	During normal operation	I_{DD1}	Direct mode		2.7 × fx	4.0 × fx +5.0	mA
			PLL mode		2.5 × fx	4.0 × fx+5.0	mA
	HALT mode	I_{DD2}	Direct mode		1.5 × fx	2.7 × fx	mA
			PLL mode		1.2 × fx	2.7 × fx	mA
	IDLE mode	I_{DD3}	Direct mode		2.0	5.0	mA
			PLL mode		2.0	5.0	mA
	STOP mode	I_{DD4}			5.0	150	μA

Remarks 1. TYP. values are reference values for when T_A = 25°C, V_{DD} = CV_{DD} = HV_{DD} = 3.3 V.

2. Direct mode:

f_X = 2 to 40 MHz (μPD703100A-40)

f_X = 2 to 33 MHz (μPD703100A-33)

f_X = 10 to 33 MHz (μPD703101A-33, 703102A-33)

PLL mode:

f_X = 2 to 40 MHz (μPD703100A-40)

f_X = 2 to 33 MHz (μPD703100A-33)

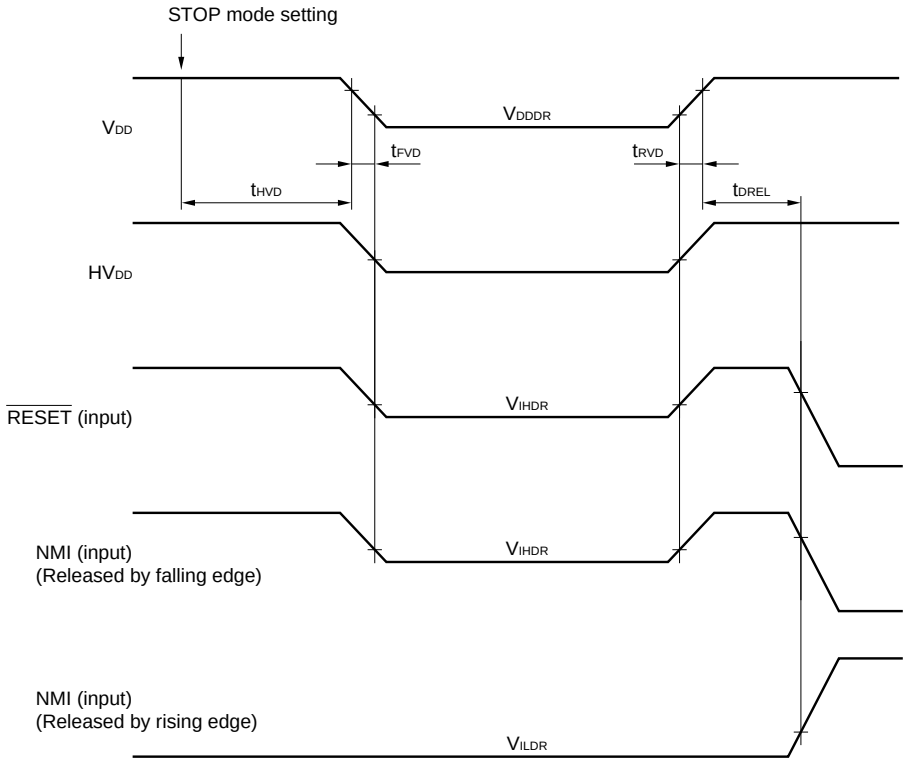
f_X = 20 to 33 MHz (μPD703101A-33, 703102A-33)

Data Hold Characteristics (T_A = –40 to +70°C ... μPD703100A-40,
T_A = –40 to +85°C ... μPD703100A-33, μPD703101A-33, μPD703102A-33)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode, $V_{DD} = V_{DDDR}$	1.5		3.6	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$			150	μA
Power supply voltage rise time	t_{RVD}		200			μs
Power supply voltage fall time	t_{FVD}		200			μs
Power supply voltage hold time (to STOP mode setting)	t_{HVD}		0			ms
STOP mode release signal input time	t_{DREL}		0			ns
Data hold high-level input voltage	V_{IHDR}	**Note**	0.8 HV_{DDDR}		V_{DDDR}	V
Data hold low-level input voltage	V_{ILDR}	**Note**	0		0.2 V_{DDDR}	V

Note P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$

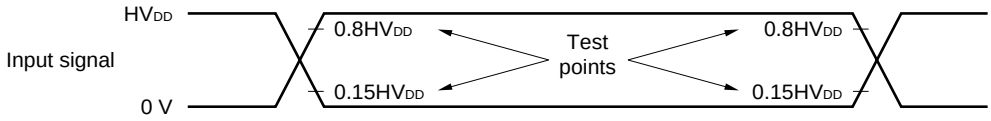
Remark TYP. values are reference values for when T_A = 25°C.



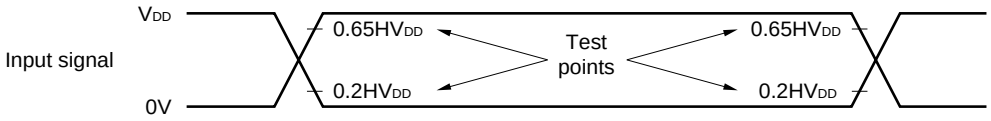
AC Characteristics (T_A = –40 to +70°C ... μPD703100A-40,
T_A = –40 to +85°C ... μPD703100A-33, μPD703101A-33, μPD703102A-33,
V_{DD} = HV_{DD} = CV_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, output pin load capacitance: C_L = 50 pF)

AC Test Input Waveform

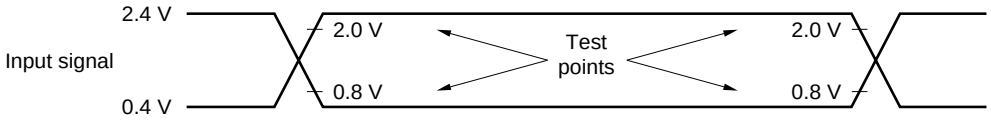
(a) P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$



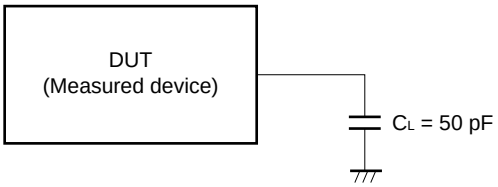
(b) Pins other than those listed in (a) above



AC Test Output Test Points



Load Condition

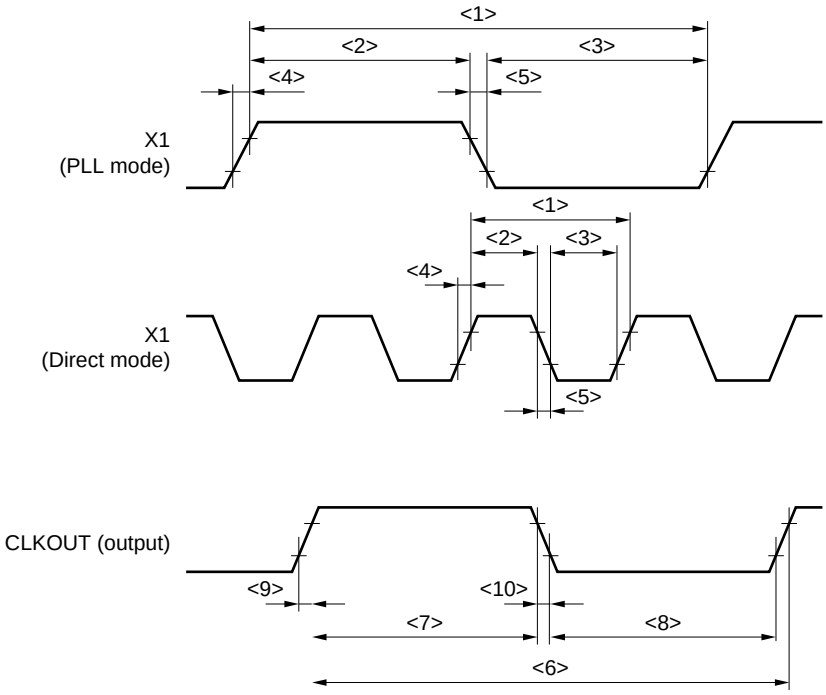


Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance to 50 pF or lower.

(1) Clock timing

Parameter	Symbol		Condition		MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	μPD703100A-40	12.5	250	ns
				μPD703100A-33	15	250	ns
				μPD703101A-33, μPD 703102A-33,	15	50	ns
			PLL mode	μPD703100A-40	125	250	ns
				μPD703100A-33, 703101A-33, 703102-A33	150	250	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode		5		ns
			PLL mode		50		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode		5		ns
			PLL mode		50		ns
X1 input rise time	<4>	t_{XR}	Direct mode			4	ns
			PLL mode			10	ns
X1 input fall time	<5>	t_{XF}	Direct mode			4	ns
			PLL mode			10	ns
CPU operating frequency	–	ϕ	μPD703100A-40		2	40	MHz
			μPD703100A-33		2	33	MHz
			μPD703101A-33, 703102A-33		10	33	MHz
CLKOUT output cycle	<6>	t_{CYK}	μPD703100A-40		25	500	ns
			μPD703100A-33		30	500	ns
			μPD703101A-33, 703102A-33		30	100	ns
CLKOUT input high-level width	<7>	t_{WKH}			0.5T – 7		ns
CLKOUT input low-level width	<8>	t_{WKL}			0.5T – 4		ns
CLKOUT input rise time	<9>	t_{KR}				5	ns
CLKOUT input fall time	<10>	t_{KF}				5	ns

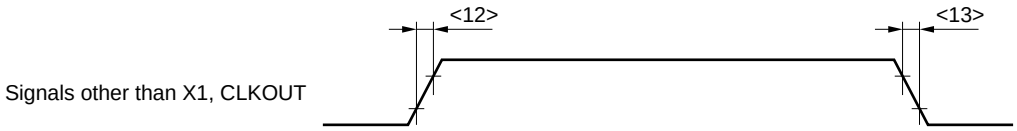
Remark T = t_{CYK}


<1>
<2>
<3>
<4>
<5>
X1
(PLL mode)
<1>
<2>
<3>
<4>
X1
(Direct mode)
<5>

CLKOUT (output)
<9>
<10>
<7>
<8>
<6>

(2) Output waveform (other than X1, CLKOUT)

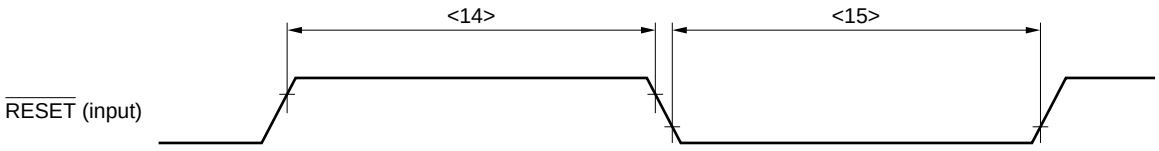
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	t_{OR}			5	ns
Output fall time	<13>	t_{OF}			5	ns



(3) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<14>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	<15>	t_{WRSL}	When power supply is on, and STOP mode has been released	500 + T_{OS}		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

Remark T_{OS}: Oscillation stabilization time



(4) SRAM, external ROM, external I/O access timing

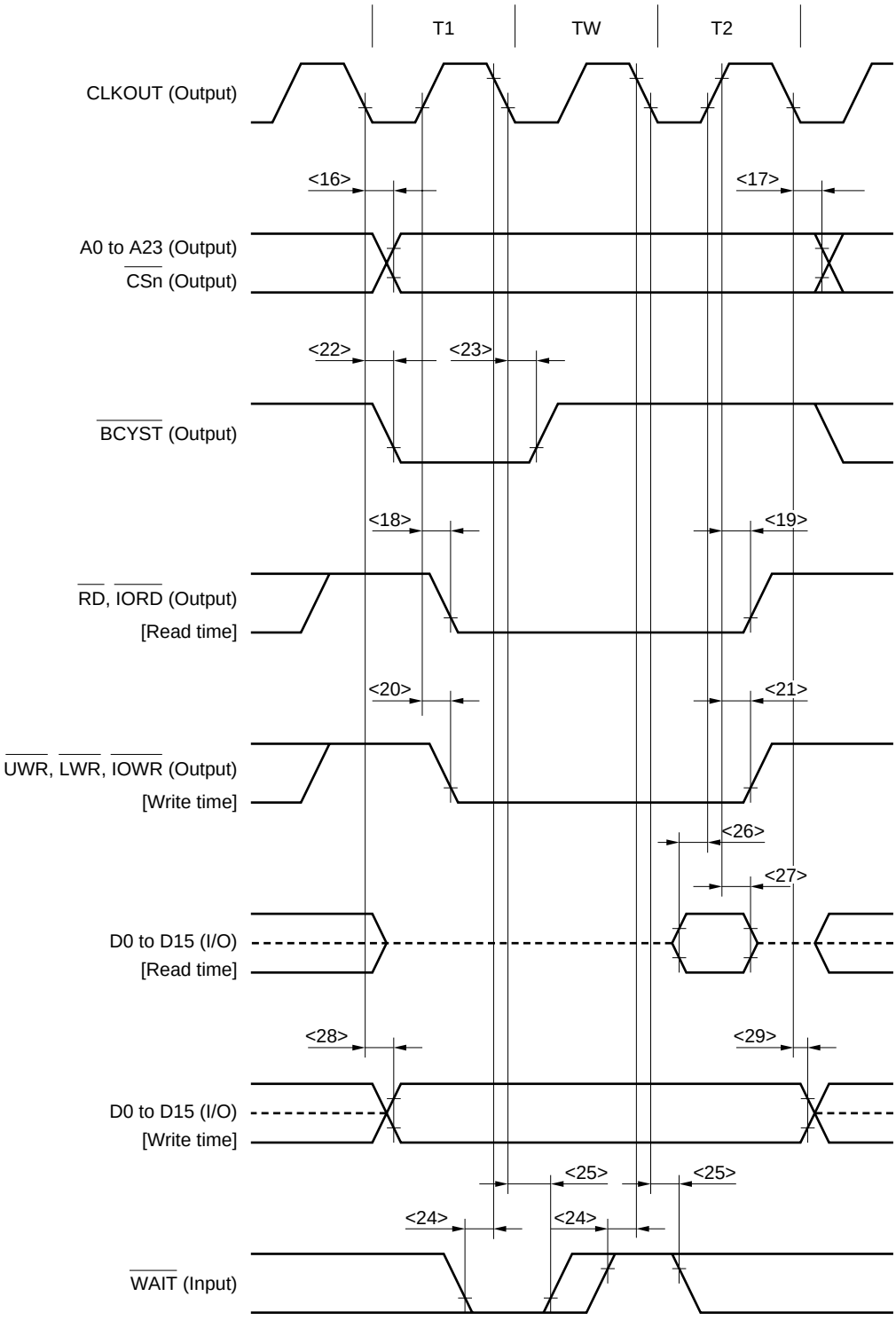
(a) Access timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Address, $\overline{CSn}$ output delay time (from CLKOUT ↓)	<16>	t_{DKA}		2	10	ns
Address, $\overline{CSn}$ output hold time (from CLKOUT ↓)	<17>	t_{HKA}		2	10	ns
$\overline{RD}$, $\overline{IORD}$ ↓ delay time (from CLKOUT ↑)	<18>	t_{DKRDL}		2	14	ns
$\overline{RD}$, $\overline{IORD}$ ↑ delay time (from CLKOUT ↑)	<19>	t_{HKRDH}		2	14	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↓ delay time (from CLKOUT ↑)	<20>	t_{DKWRL}		2	10	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑ delay time (from CLKOUT ↑)	<21>	t_{HKWRH}		2	10	ns
$\overline{BCYST}$ ↓ delay time (from CLKOUT ↓)	<22>	t_{DKBSL}		2	10	ns
$\overline{BCYST}$ ↑ delay time (from CLKOUT ↓)	<23>	t_{HKBSH}		2	10	ns
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		10		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Data output delay time (from CLKOUT ↓)	<28>	t_{DKOD}		2	10	ns
Data output hold time (from CLKOUT ↓)	<29>	t_{HKOD}		2	10	ns

Remarks 1. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

2. n = 0 to 7

(a) Access timing (SRAM, external ROM, external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(b) Read timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to address)	<30>	t_{SAID}			$(1.5 + w_D + w) T - 20$	ns
Data input setup time (to $\overline{RD}$)	<31>	t_{SRDID}			$(1 + w_D + w) T - 24$	ns
$\overline{RD}$, $\overline{IORD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w) T - 10$		ns
$\overline{RD}$, $\overline{IORD}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
$\overline{RD}$, $\overline{IORD}$ ↓ delay time from address, $\overline{CSn}$	<34>	t_{DARD}		$0.5T - 10$		ns
Address delay time from $\overline{RD}$, $\overline{IORD}$ ↑	<35>	t_{DRDA}		$(0.5 + i) T - 5$		ns
Data input hold time (from $\overline{RD}$, $\overline{IORD}$ ↑)	<36>	t_{HRDID}		0		ns
Data output delay time from $\overline{RD}$, $\overline{IORD}$ ↑	<37>	t_{DRDOD}		$(0.5 + i) T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		$T - 20$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		$T - 20$	ns
$\overline{WAIT}$ hold time (to $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

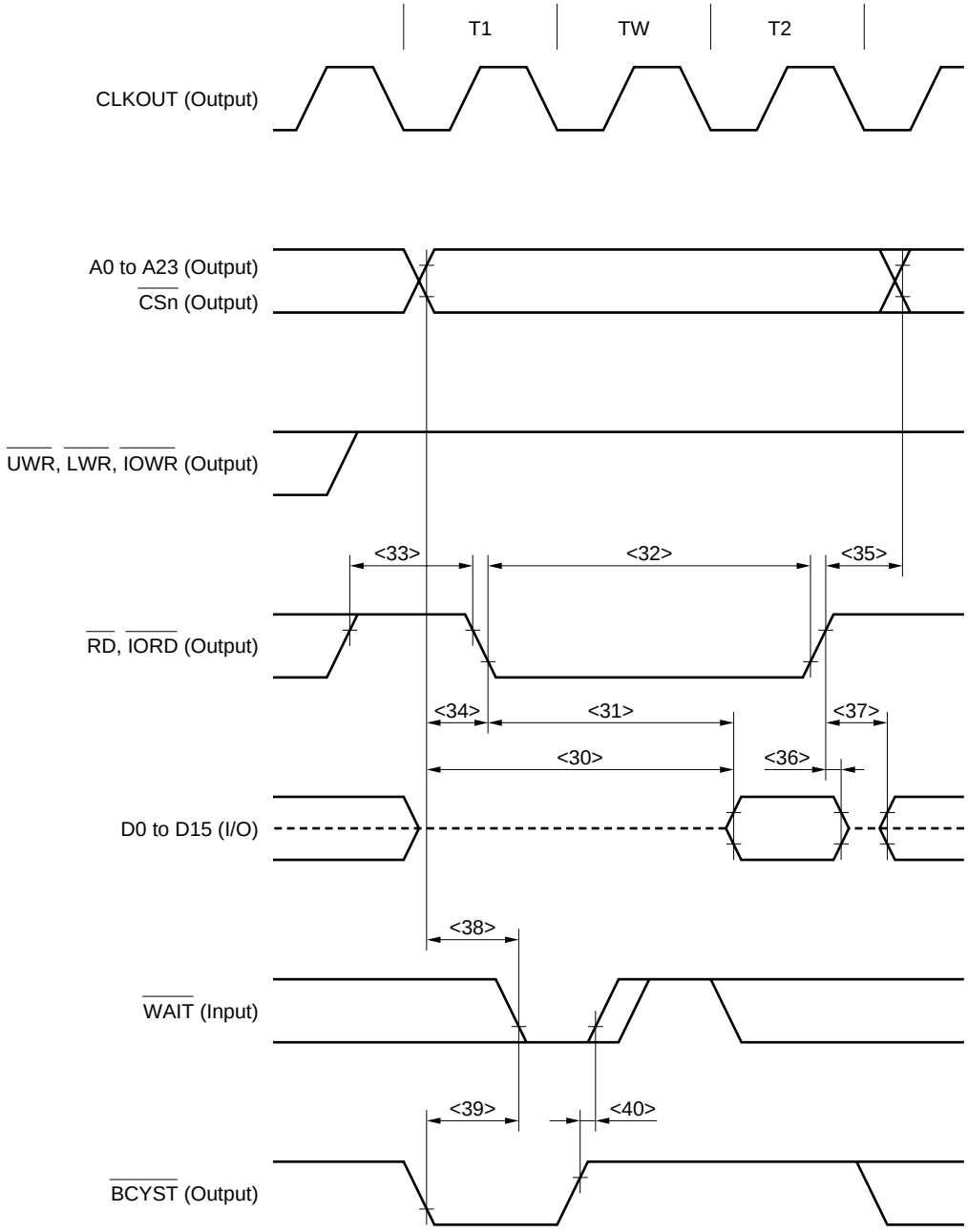
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. i: the number of idle states that are inserted when a write cycle follows a read cycle.

5. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

6. n = 0 to 7

(b) Read timing (SRAM, external ROM, external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(c) Write timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 20	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		T – 20	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↓ delay time from address, $\overline{CSn}$	<41>	t_{DAWR}		0.5T – 5		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		(1.5 + w_D + w) T – 10		ns
Address delay time from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑	<43>	t_{DWRA}		0.5T – 5		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ low-level width	<45>	t_{WWRL}		(1 + w_D + w) T – 10		ns
Data output setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑)	<46>	t_{SODWR}		(1.5 + w_D + w) T – 10		ns
Data output hold time (from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑)	<47>	t_{HWROD}		0.5T – 5		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

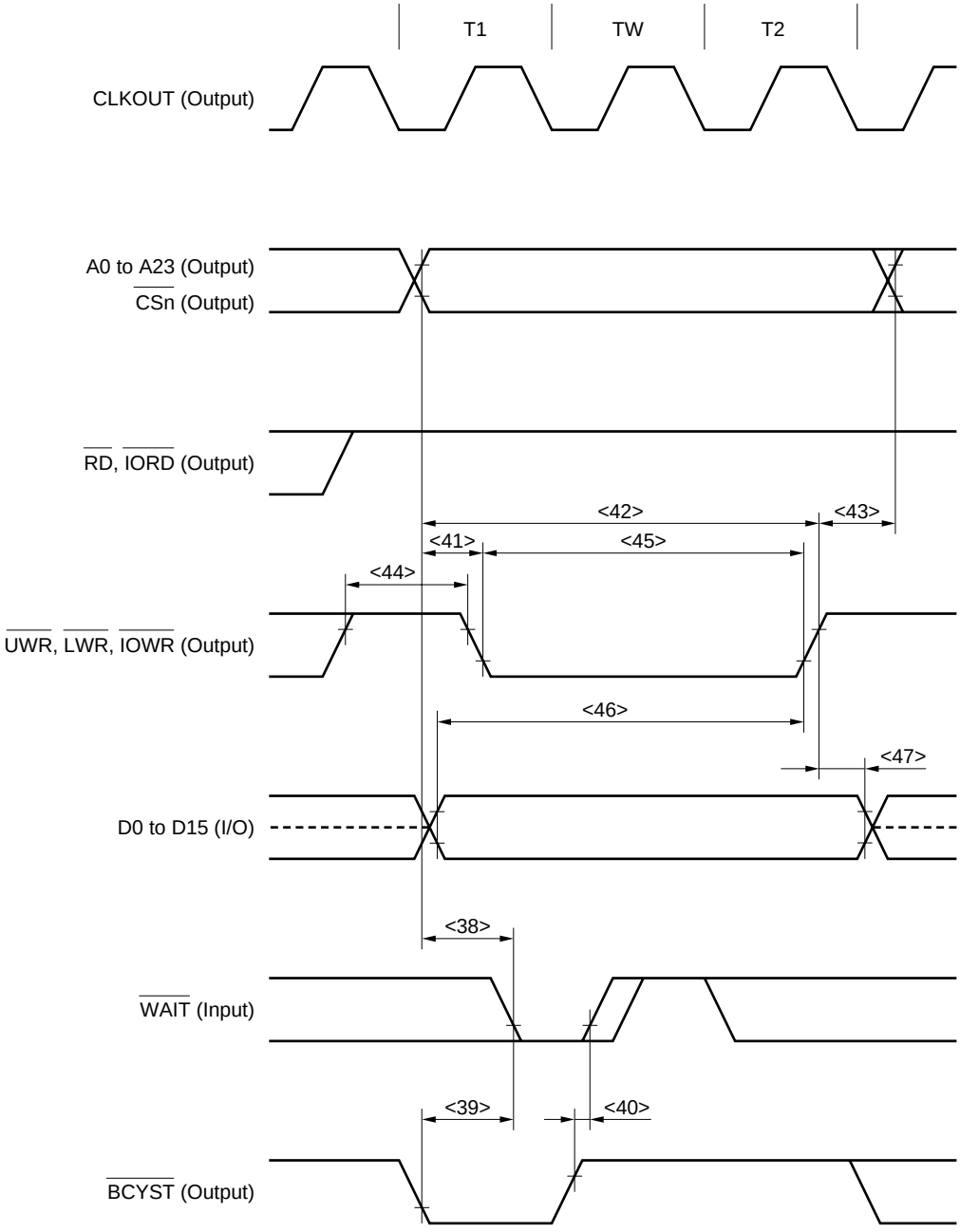
Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. n = 0 to 7

(c) Write timing (SRAM, external ROM, external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{RD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w_F + w)$ T – 10		ns
$\overline{RD}$ high-level width	<33>	t_{WRDH}		T – 10		ns
$\overline{RD}$ ↓ delay time from address, $\overline{CS}$n	<34>	t_{DARD}		0.5T – 5		ns
Address delay time from $\overline{RD}$ ↑	<35>	t_{DRDA}		(0.5 + i) T – 5		ns
Data output delay time from $\overline{RD}$ ↑	<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 20	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		T – 20	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
$\overline{IOWR}$ ↓ delay time from address	<41>	t_{DAWR}		0.5T – 5		ns
Address setup time (to $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		(1.5 + w_D + w) T – 10		ns
Address delay time from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑	<43>	t_{DWRA}		0.5T – 5		ns
$\overline{IOWR}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{IOWR}$ low-level width	<45>	t_{WWRL}		(1 + w_D + w) T – 10		ns
$\overline{RD}$ ↑ delay time from $\overline{IOWR}$ ↑	<48>	t_{DWRRD}	w_F = 0	0		ns
			w_F = 1	T – 10		ns
$\overline{IOWR}$ ↓ delay time from $\overline{DMAAKm}$ ↓	<49>	t_{DDAWR}		0.5T – 10		ns
$\overline{DMAAKm}$ ↑ delay time from $\overline{IOWR}$ ↑	<50>	t_{DWRDA}		($0.5 + w_F$) T – 10		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

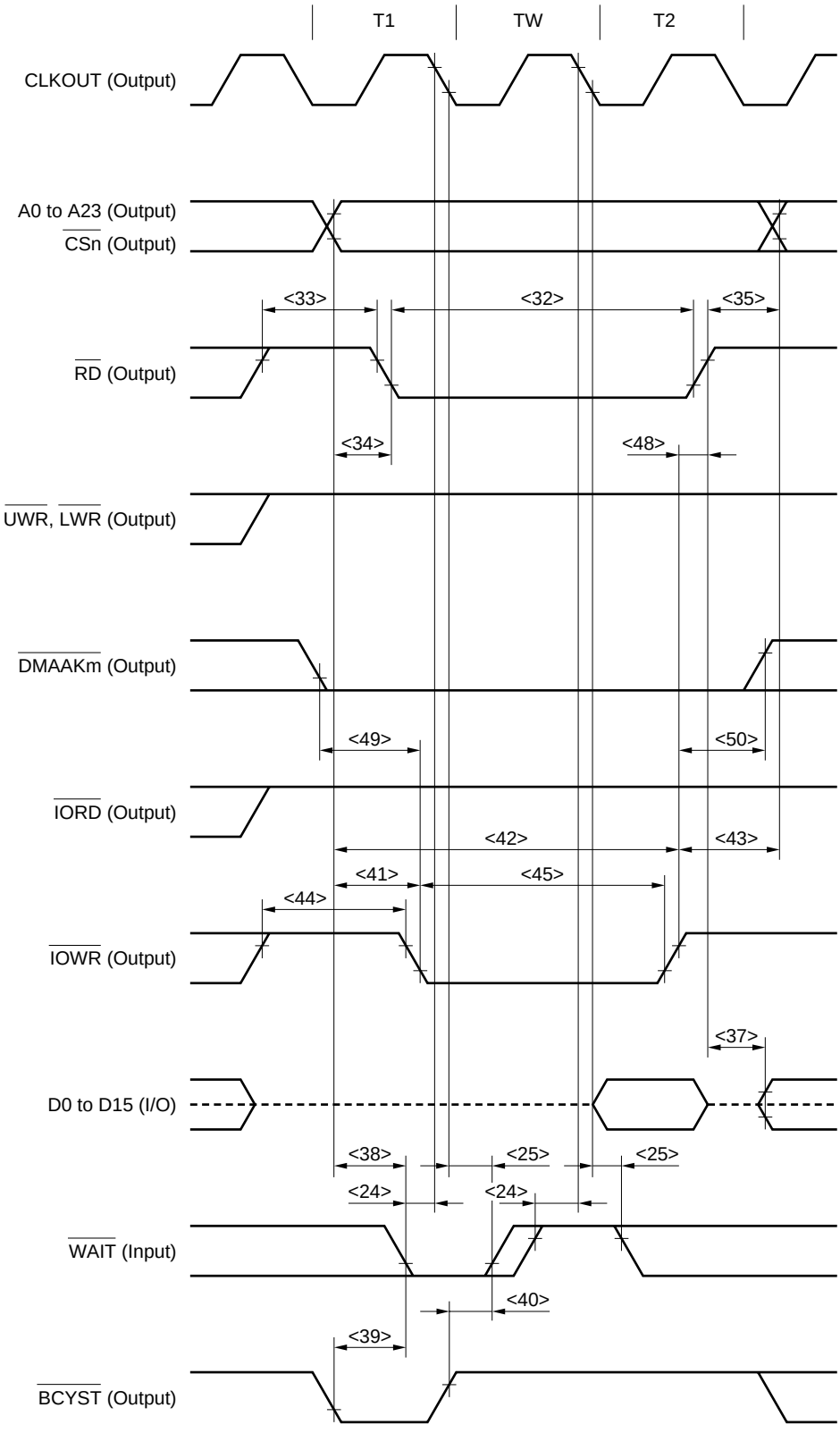
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i: the number of idle states that are inserted when a write cycle follows a read cycle.

6. n = 0 to 7, m = 0 to 3

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{IORD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w_F + w)$ T – 10		ns
$\overline{IORD}$ high-level width	<33>	t_{WRDH}		T – 10		ns
$\overline{IORD}$ ↓ delay time from address, $\overline{CSn}$	<34>	t_{DARD}		0.5T – 5		ns
Address delay time from $\overline{IORD}$ ↑	<35>	t_{DRDA}		(0.5 + i) T – 5		ns
Data output delay time from $\overline{IORD}$ ↑	<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 20	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		T – 20	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
$\overline{UWR}$, $\overline{LWR}$ ↓ delay time from address	<41>	t_{DAWR}		0.5T – 5		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$ ↑)	<42>	t_{SAWR}		(1.5 + w_D + w) T – 10		ns
Address delay time from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑	<43>	t_{DWRA}		0.5T – 5		ns
$\overline{UWR}$, $\overline{LWR}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{UWR}$, $\overline{LWR}$ low-level width	<45>	t_{WWRL}		(1 + w_D + w) T – 10		ns
$\overline{IORD}$ ↑ delay time from $\overline{UWR}$, $\overline{LWR}$↑	<48>	t_{DWRRD}	w_F = 0	0		ns
			w_F = 1	T – 10		ns
$\overline{IORD}$ ↓ delay time from $\overline{DMAAKm}$ ↓	<51>	t_{DDARD}		0.5T – 10		ns
$\overline{DMAAKm}$ ↑ delay time from $\overline{IORD}$ ↑	<52>	t_{DRDDA}		0.5T – 10		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

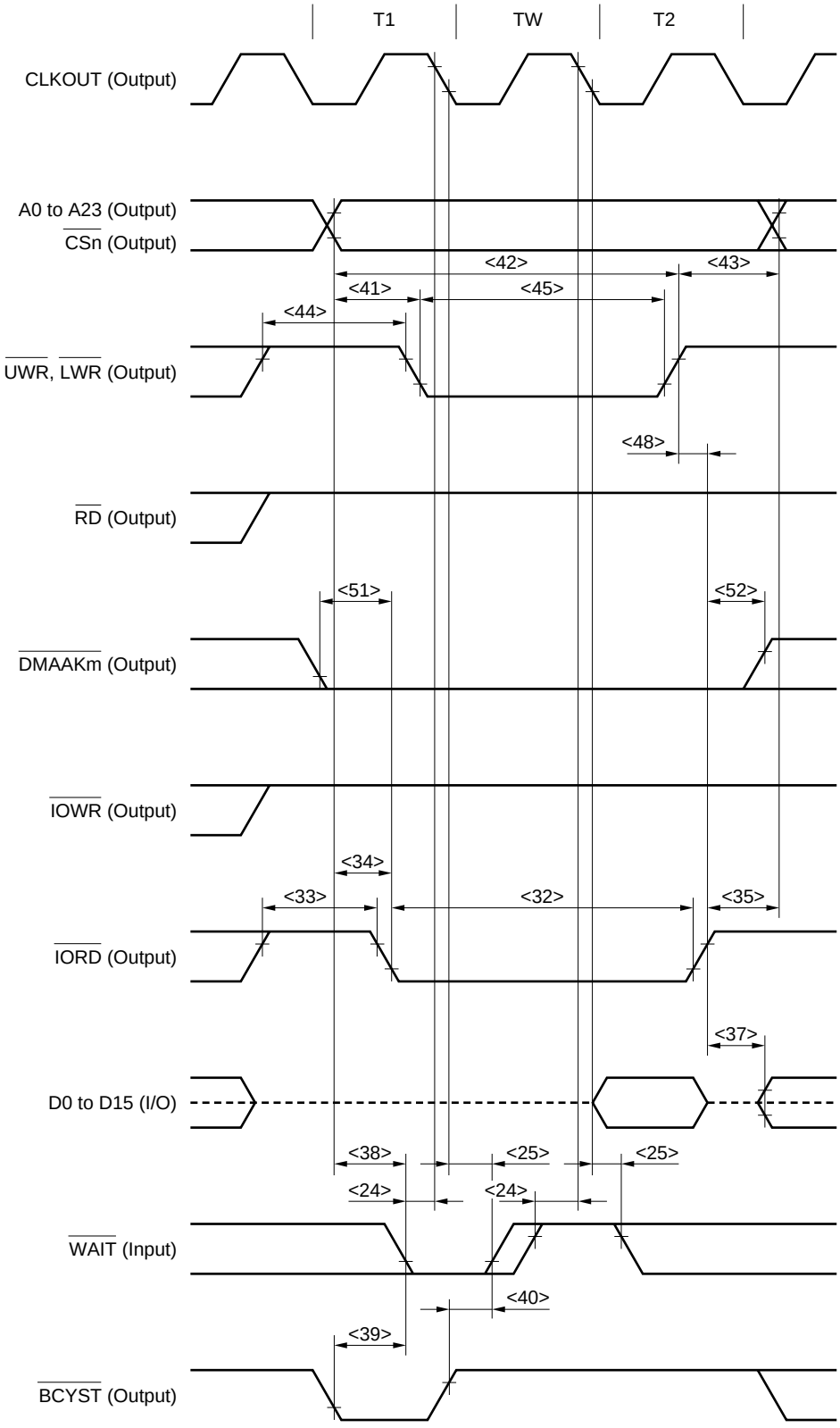
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i: the number of idle states that are inserted when a write cycle follows a read cycle.

6. n = 0 to 7, m = 0 to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(5) Page ROM access timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		10		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Off-page data input setup time (to address)	<30>	t_{SAID}			$(1.5 + w_D + w)$ T – 20	ns
Off-page data input setup time (to $\overline{RD}$)	<31>	t_{SRDID}			$(1 + w_D + w)$ T – 24	ns
Off-page $\overline{RD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w)$ T – 10		ns
$\overline{RD}$ high-level width	<33>	t_{WRDH}		0.5T – 10		ns
Data input hold time (from $\overline{RD}$)	<36>	t_{HRDID}		0		ns
Data output delay time from $\overline{RD}$ ↑	<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
On-page $\overline{RD}$ low-level width	<53>	t_{WORDL}		$(1.5 + w_{PR} + w)$ T – 10		ns
On-page data input setup time (to address)	<54>	t_{SOAID}			$(1.5 + w_{PR} + w)$ T – 20	ns
On-page data input setup time (to $\overline{RD}$)	<55>	t_{SORDID}			$(1.5 + w_{PR} + w)$ T – 24	ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

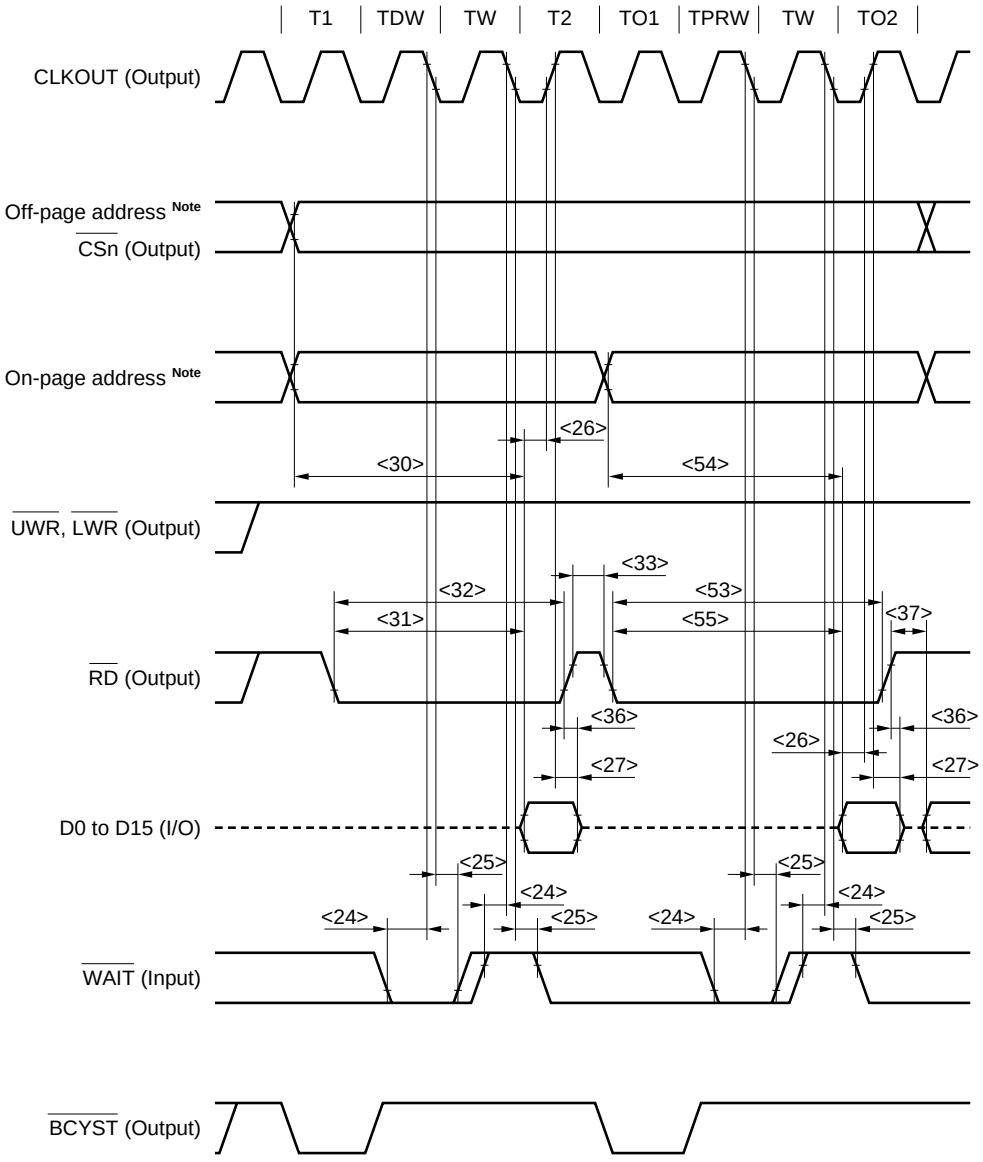
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. w_{PR}: the number of waits due to the PRC register.

5. i: the number of idle states that are inserted when a write cycle follows a read cycle.

6. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

(5) Page ROM access timing (2/2)



Note On-page and off-page addresses are as follows.

PRC Register			On-page Addresses	Off-page Addresses
MA5	MA4	MA3		
0	0	0	A0, A1	A2 to A23
0	0	1	A0 to A2	A3 to A23
0	1	1	A0 to A3	A4 to A23
1	1	1	A0 to A4	A5 to A23

Remarks 1. This is the timing for the following case.
Number of waits due to the DWC1 and DWC2 registers (TDW): 1
Number of waits due to the PRC register (TPRW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		10		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Data output delay time from $\overline{OE}$ ↑	<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
Row address setup time	<56>	t_{ASR}		(0.5 + w_{RP}) T – 10		ns
Row address hold time	<57>	t_{RAH}		(0.5 + w_{RH}) T – 10		ns
Column address setup time	<58>	t_{ASC}		0.5T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA} + w) T – 10		ns
Read/write cycle time	<60>	t_{RC}		(3 + w_{RP} + w_{RH} + w_{DA} + w) T – 10		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		(0.5 + w_{RP}) T – 5		ns
$\overline{RAS}$ pulse time	<62>	t_{RAS}		(2.5 + w_{RH} + w_{DA} + w) T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA} + w) T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		(2 + w_{DA} + w) T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA} + w) T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		(1 + w_{RP}) T – 10		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		(2 + w_{RH} + w_{DA} + w) T – 10		ns
$\overline{WE}$ setup time	<68>	t_{RCS}		(2 + w_{RP} + w_{RH}) T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t_{RCH}		T – 10		ns
$\overline{CAS}$ precharge time	<71>	t_{CPN}		(2 + w_{RP} + w_{RH}) T – 5		ns
Output enable access time	<72>	t_{OEA}			(2 + w_{RP} + w_{RH} + w_{DA} + w) T – 20	ns
$\overline{RAS}$ access time	<73>	t_{RAC}			(2 + w_{RH} + w_{DA} + w) T – 20	ns
Access time from column address	<74>	t_{AA}			(1.5 + w_{DA} + w) T – 20	ns
$\overline{CAS}$ access time	<75>	t_{CAC}			(1 + w_{DA} + w) T – 20	ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. i: the number of idle states that are inserted when a write cycle follows a read cycle.

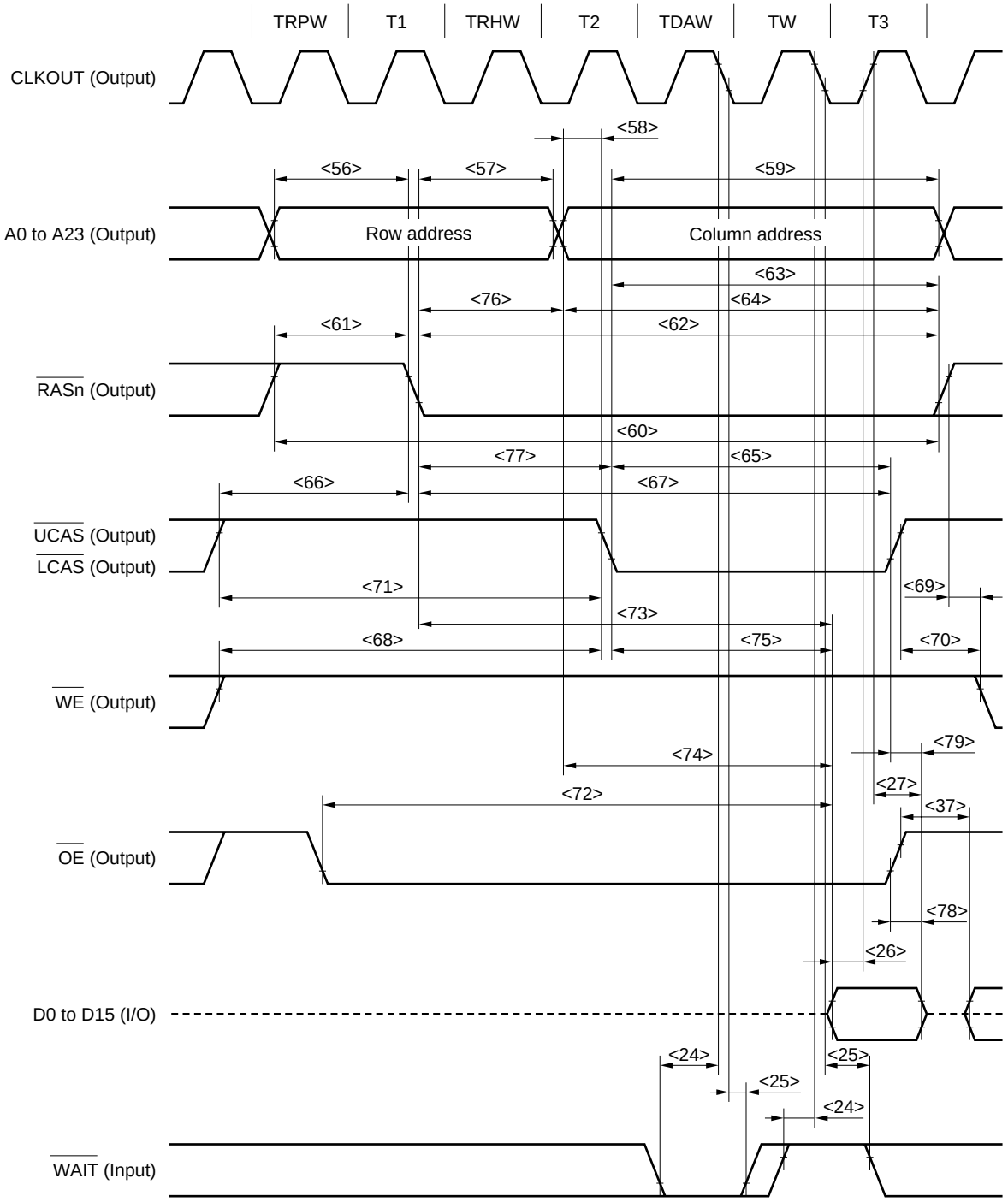
(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{RAS}$ column address delay time	<76>	t_{RAD}		(0.5 + w_{RH}) T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time	<77>	t_{RCD}		(1 + w_{RH}) T – 10		ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)	<79>	t_{OFF}		0		

Remarks 1. T = t_{CYK}

2. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

[MEMO]

(b) Read timing (high-speed page DRAM access: on-page) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		10		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Data output delay time from $\overline{OE}$ ↑	<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
Column address setup time	<58>	t_{ASC}		(0.5 + w_{CP}) T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA}) T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA}) T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		(2 + w_{CP} + w_{DA}) T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA}) T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<68>	t_{RCS}		(1 + w_{CP}) T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t_{RCH}		T – 10		ns
Output enable access time	<72>	t_{OEA}			(1 + w_{CP} + w_{DA}) T – 20	ns
Access time from column address	<74>	t_{AA}			(1.5 + w_{CP} + w_{DA}) T – 20	ns
$\overline{CAS}$ access time	<75>	t_{CAC}			(1 + w_{DA}) T – 20	ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)	<79>	t_{OFF}		0		ns
Access time from $\overline{CAS}$ precharge	<80>	t_{ACP}			(2 + w_{CP} + w_{DA}) T – 20	ns
$\overline{CAS}$ precharge time	<81>	t_{CP}		(1 + w_{CP}) T – 5		ns
High-speed page mode cycle time	<82>	t_{PC}		(2 + w_{CP} + w_{DA}) T – 10		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t_{RHCP}		(2.5 + w_{CP} + w_{DA}) T – 10		ns

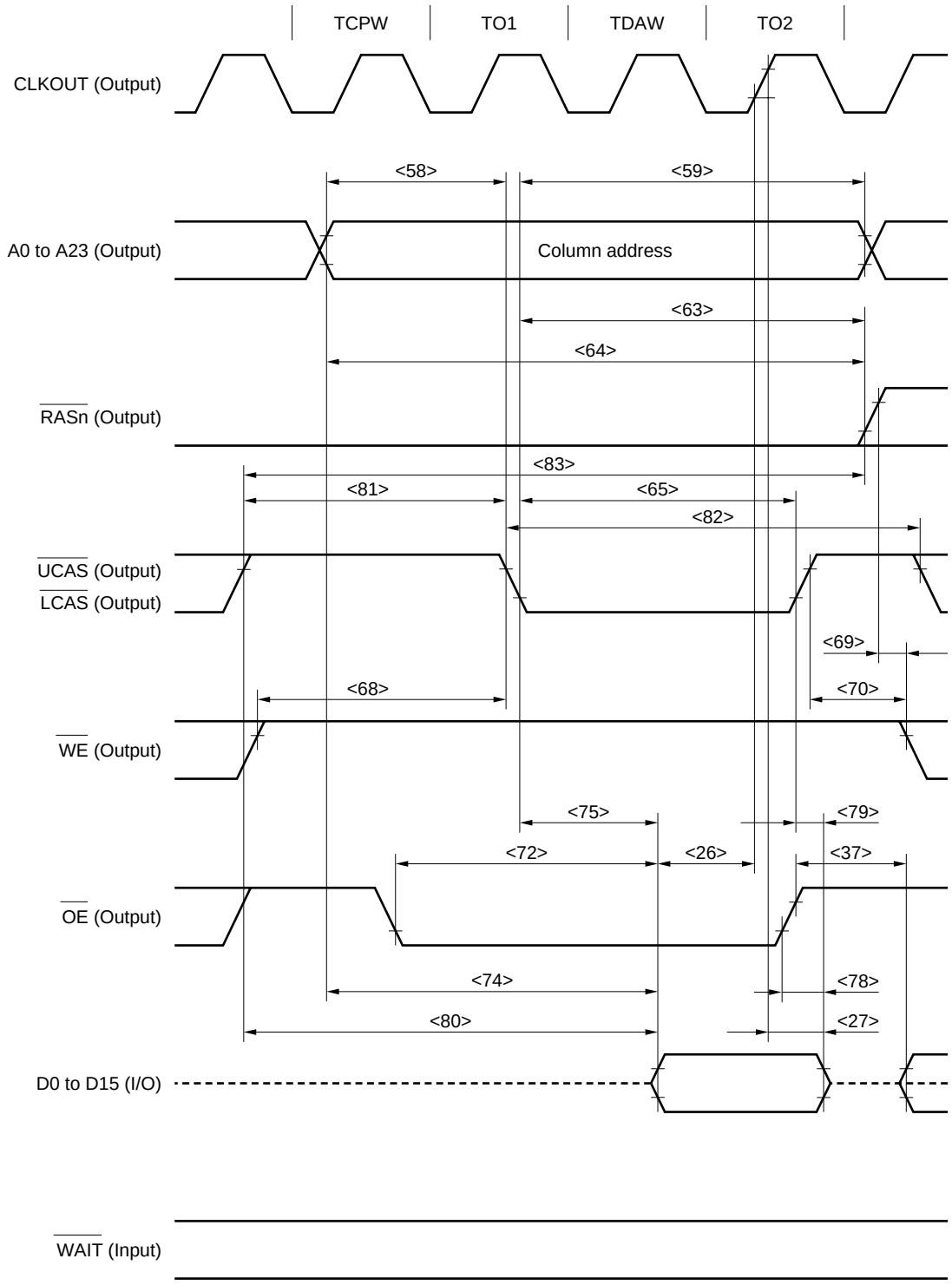
Remarks 1. T = t_{CYK}

2. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. i: the number of idle states that are inserted when a write cycle follows a read cycle.

(b) Read timing (high-speed page DRAM access: on-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Row address setup time	<56>	t_{ASR}		$(0.5 + w_{RP})$ T – 10		ns
Row address hold time	<57>	t_{RAH}		$(0.5 + w_{RH})$ T – 10		ns
Column address setup time	<58>	t_{ASC}		0.5T – 10		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA} + w)$ T – 10		ns
Read/write cycle time	<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w)$ T – 10		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		$(0.5 + w_{RP})$ T – 5		ns
$\overline{RAS}$ pulse time	<62>	t_{RAS}		$(2.5 + w_{RH} + w_{DA} + w)$ T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA} + w)$ T – 10		ns
Column address read time (from $\overline{RAS}$ ↑)	<64>	t_{RAL}		$(2 + w_{DA} + w)$ T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA} + w)$ T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		$(1 + w_{RH})$ T – 10		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w)$ T – 10		ns
$\overline{CAS}$ precharge time	<71>	t_{CPN}		$(2 + w_{RP} + w_{RH})$ T – 5		ns
$\overline{RAS}$ column address delay time	<76>	t_{RAD}		$(0.5 + w_{RH})$ T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time	<77>	t_{RCD}		$(1 + w_{RH})$ T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<84>	t_{WCS}		$(1 + w_{RP} + w_{RH})$ T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA} + w)$ T – 10		ns
Data setup time (to $\overline{CAS}$ ↓)	<86>	t_{DS}		$(1.5 + w_{RP} + w_{RH})$ T – 10		ns
Data hold time (from $\overline{CAS}$ ↓)	<87>	t_{DH}		$(1.5 + w_{DA} + w)$ T – 10		ns

Remarks 1. T = t_{CYK}

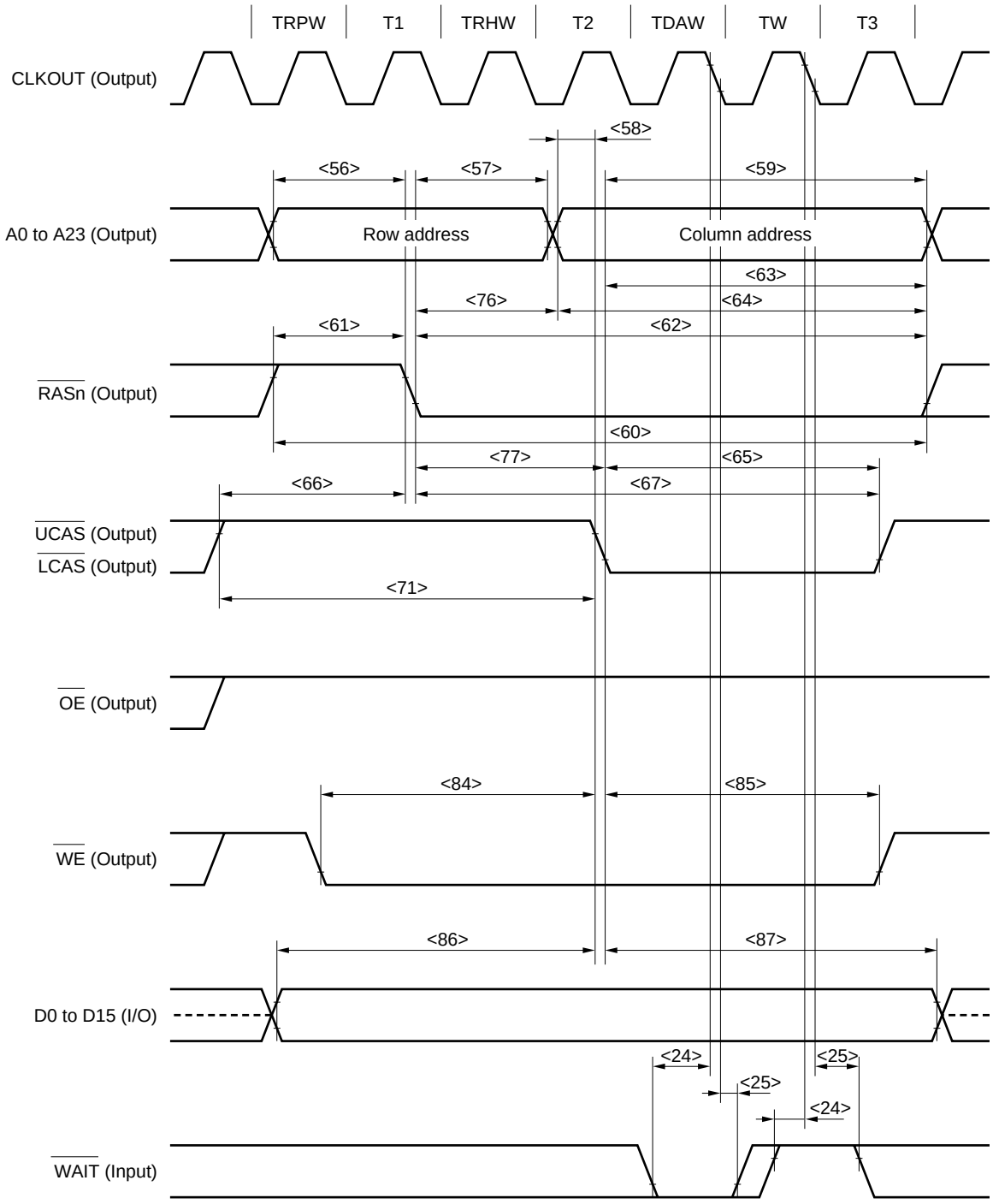
2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(d) Write timing (high-speed page DRAM access: on-page) (1/2)

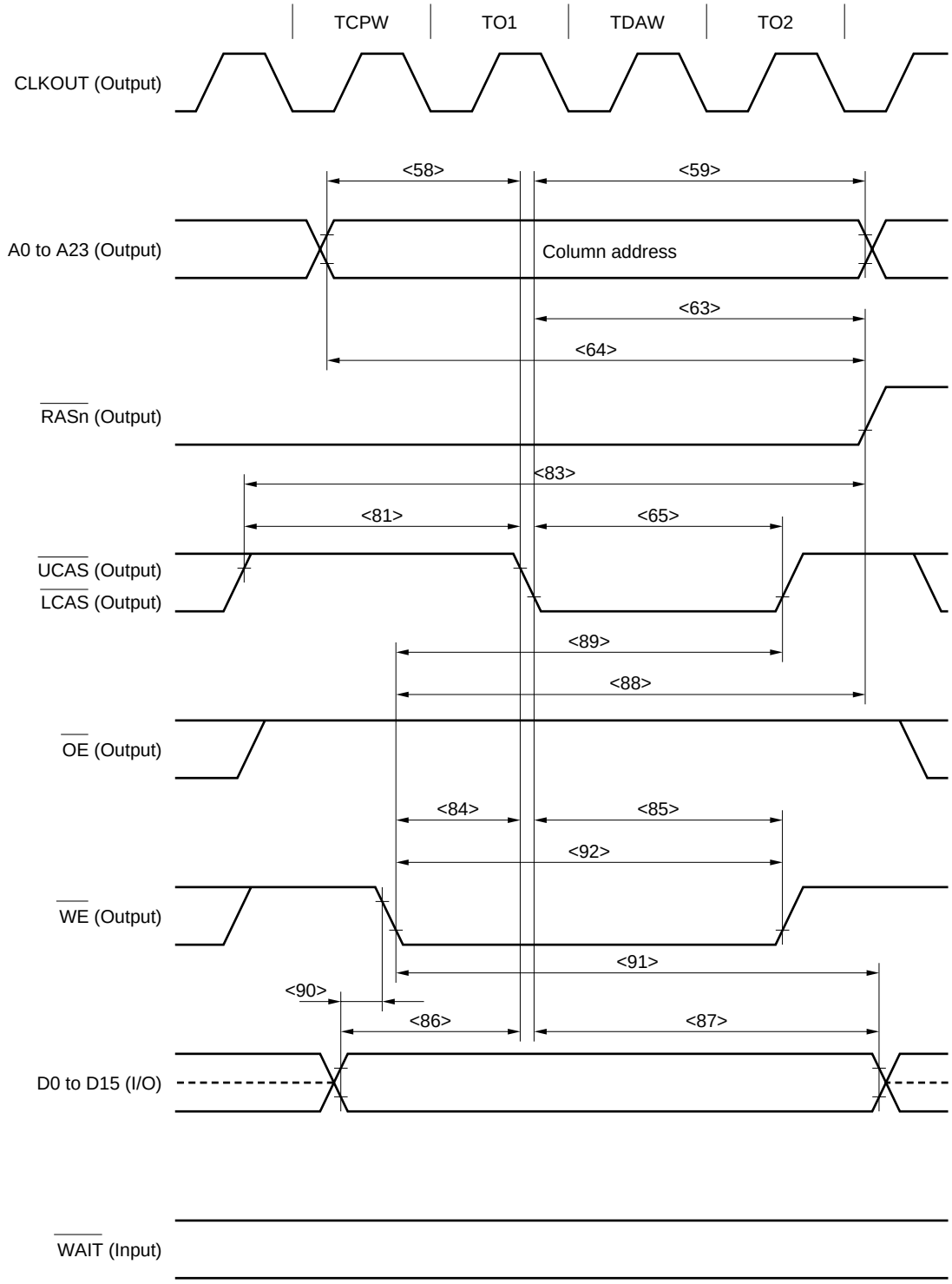
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Column address setup time	<58>	t_{ASC}		(0.5 + w_{CP}) T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA}) T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA}) T – 10		ns
Column address read time (from $\overline{RAS}$ ↑)	<64>	t_{RAL}		(2 + w_{CP} + w_{DA}) T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA}) T – 10		ns
$\overline{CAS}$ precharge time	<81>	t_{CP}		(1 + w_{CP}) T – 5		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t_{RHCP}		(2.5 + w_{CP} + w_{DA}) T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<84>	t_{WCS}	$w_{CP} \geq 1$	w_{CP}T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<85>	t_{WCH}		(1 + w_{DA}) T – 10		ns
Data setup time (to $\overline{CAS}$ ↓)	<86>	t_{DS}		(0.5 + w_{CP}) T – 10		ns
Data hold time (from $\overline{CAS}$ ↓)	<87>	t_{DH}		(1.5 + w_{DA}) T – 10		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)	<88>	t_{RWL}	w_{CP} = 0	(1.5 + w_{DA}) T – 10		ns
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)	<89>	t_{CWL}	w_{CP} = 0	(1 + w_{DA}) T – 10		ns
Data setup time (to $\overline{WE}$ ↓)	<90>	t_{DSWE}	w_{CP} = 0	0.5T – 10		ns
Data hold time (from $\overline{WE}$ ↓)	<91>	t_{DHWE}	w_{CP} = 0	(1.5 + w_{DA}) T – 10		ns
$\overline{WE}$ pulse width	<92>	t_{WP}	w_{CP} = 0	(1 + w_{DA}) T – 10		ns

Remarks 1. T = t_{CYK}

2. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(d) Write timing (high-speed page DRAM access: on-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(e) Read timing (EDO DRAM) (1/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)		<26>	t_{SKID}		10		ns
Data input hold time (from CLKOUT ↑)		<27>	t_{HKID}		2		ns
Data output delay time from $\overline{OE}$ ↑		<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
Row address setup time		<56>	t_{ASR}		(0.5 + w_{RP}) T – 10		ns
Row address hold time		<57>	t_{RAH}		(0.5 + w_{RH}) T – 10		ns
Column address setup time		<58>	t_{ASC}		0.5T – 10		ns
Column address hold time		<59>	t_{CAH}		(0.5 + w_{DA}) T – 10		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}		(0.5 + w_{RP}) T – 5		ns
Column address read time (from $\overline{RAS}$ ↑)		<64>	t_{RAL}		(2 + w_{CP} + w_{DA}) T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time		<66>	t_{CRP}		(1 + w_{RP}) T – 10		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}		(1.5 + w_{RH} + w_{DA}) T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)		<68>	t_{RCS}		(2 + w_{RP} + w_{RH}) T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)		<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)		<70>	t_{RCH}		1.5T – 10		ns
$\overline{RAS}$ access time		<73>	t_{RAC}			(2 + w_{RH} + w_{DA}) T – 20	ns
Access time from column address		<74>	t_{AA}			(1.5 + w_{DA}) T – 20	ns
$\overline{CAS}$ access time		<75>	t_{CAC}			(1 + w_{DA}) T – 20	ns
Column address delay time from $\overline{RAS}$		<76>	t_{RAD}		(0.5 + w_{RH}) T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		(1 + w_{RH}) T – 10		ns
Output buffer turn-off delay time (from $\overline{OE}$)		<78>	t_{OEZ}		0		ns
Access time from $\overline{CAS}$ precharge		<80>	t_{ACP}			(1.5 + w_{CP} + w_{DA}) T – 20	ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		(0.5 + w_{CP}) T – 5		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		(2 + w_{CP} + w_{DA}) T – 10		ns
Read cycle time		<93>	t_{HPC}		(1 + w_{DA} + w_{CP}) T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		(2.5 + w_{RH} + w_{DA}) T – 10		ns
$\overline{CAS}$ pulse width		<95>	t_{HCAS}		(0.5 + w_{DA}) T – 10		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<96>	t_{OCH1}		(2 + w_{RH} + w_{DA}) T – 10		ns
	On-page	<97>	t_{OCH2}		(0.5 + w_{DA}) T – 10		ns
Data input hold time (from $\overline{CAS}$ ↓)		<98>	t_{DHC}		0		ns

Remarks 1. T = t_{CYK}

2. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. i: the number of idle states that are inserted when a write cycle follows a read cycle.

(e) Read timing (EDO DRAM) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	t_{OEA1}			$(2 + w_{PR} + w_{RH} + w_{DA})$ T – 20	ns
	On-page	<100>	t_{OEA2}			$(1 + w_{CP} + w_{DA})$ T – 20	ns

Remarks 1. T = t_{CYK}

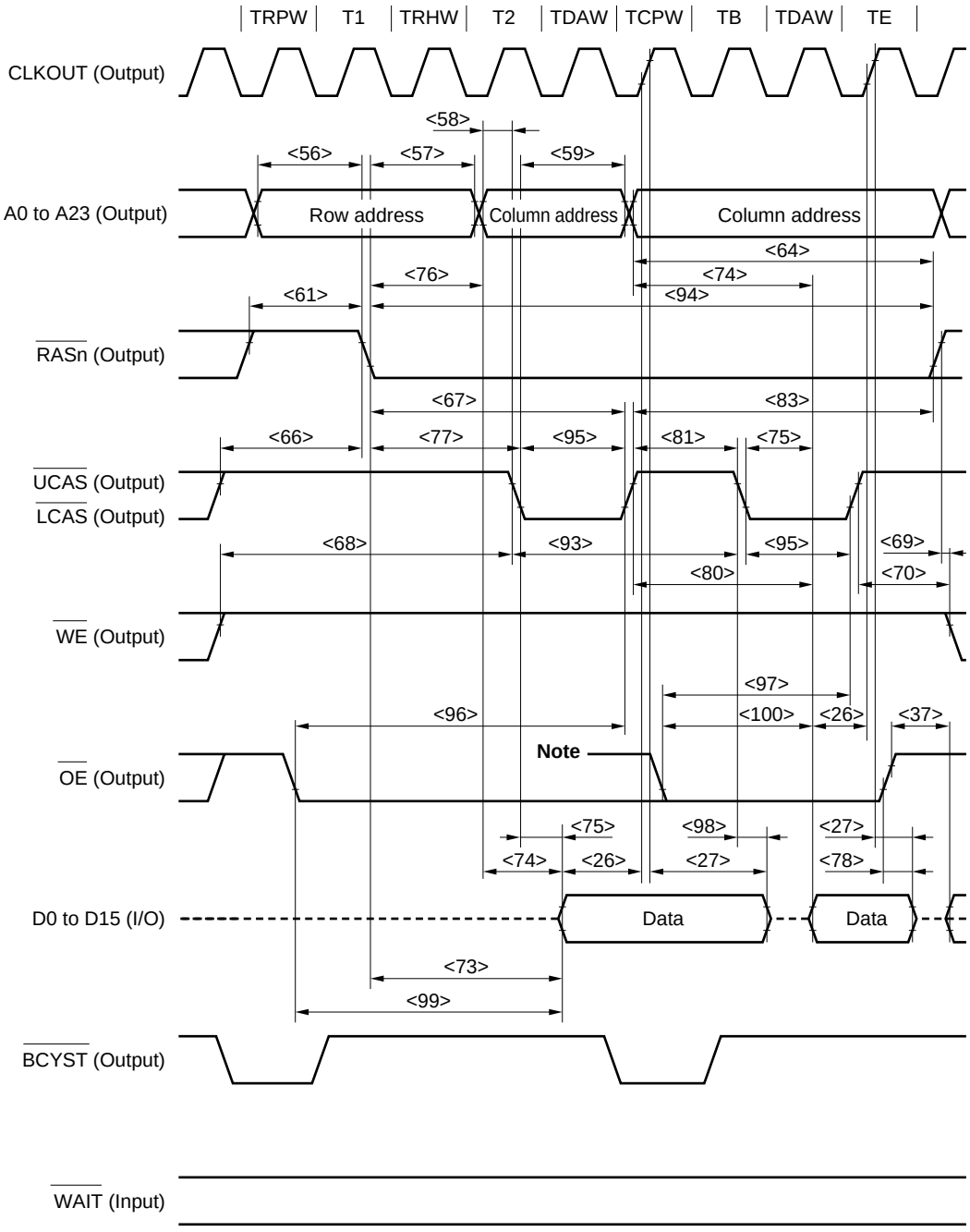
2. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(e) Read timing (EDO DRAM) (3/3)



Note For on-page access from another cycle during the $\overline{\text{RASn}}$ low level signal.

Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

[MEMO]

(f) Write timing (EDO DRAM) (1/2)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Row address setup time		<56>	t_{ASR}		$(0.5 + w_{RP})$ T – 10		ns
Row address hold time		<57>	t_{RAH}		$(0.5 + w_{RH})$ T – 10		ns
Column address setup time		<58>	t_{ASC}		0.5T – 10		ns
Column address hold time		<59>	t_{CAH}		$(0.5 + w_{DA})$ T – 10		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}		$(0.5 + w_{RP})$ T – 5		ns
$\overline{RAS}$ hold time		<63>	t_{RSH}		$(1.5 + w_{DA})$ T – 10		ns
Column address read time (from $\overline{RAS}$ ↑)		<64>	t_{RAL}		$(2 + w_{CP} + w_{DA})$ T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time		<66>	t_{CRP}		$(1 + w_{RP})$ T – 10		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}		$(1.5 + w_{RH} + w_{DA})$ T – 10		ns
Column address delay time from $\overline{RAS}$		<76>	t_{RAD}		$(0.5 + w_{RH})$ T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		$(1 + w_{RH})$ T – 10		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP})$ T – 5		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		$(2 + w_{CP} + w_{DA})$ T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)		<85>	t_{WCH}		$(1 + w_{DA})$ T – 10		ns
Data hold time (from $\overline{CAS}$ ↓)		<87>	t_{DH}		$(0.5 + w_{DA})$ T – 10		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)	On-page	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA})$ T – 10		ns
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)	On-page	<89>	t_{CWL}	$w_{CP} = 0$	$(0.5 + w_{DA})$ T – 10		ns
$\overline{WE}$ pulse width	On-page	<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA})$ T – 10		ns
Write cycle time		<93>	t_{HPC}		$(1 + w_{DA} + w_{CP})$ T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA})$ T – 10		ns
$\overline{CAS}$ pulse width		<95>	t_{HCAS}		$(0.5 + w_{DA})$ T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	Off-page	<101>	t_{WCS1}		$(1 + w_{RP} + w_{RH})$ T – 10		ns
	On-page	<102>	t_{WCS2}	$w_{CP} \geq 1$	w_{CP}T – 10		ns
Data setup time (to $\overline{CAS}$ ↓)	Off-page	<103>	t_{DS1}		$(1.5 + w_{RP} + w_{RH})$ T – 10		ns
	On-page	<104>	t_{DS2}		$(0.5 + w_{CP})$ T – 10		ns

Remarks 1. T = t_{CYK}

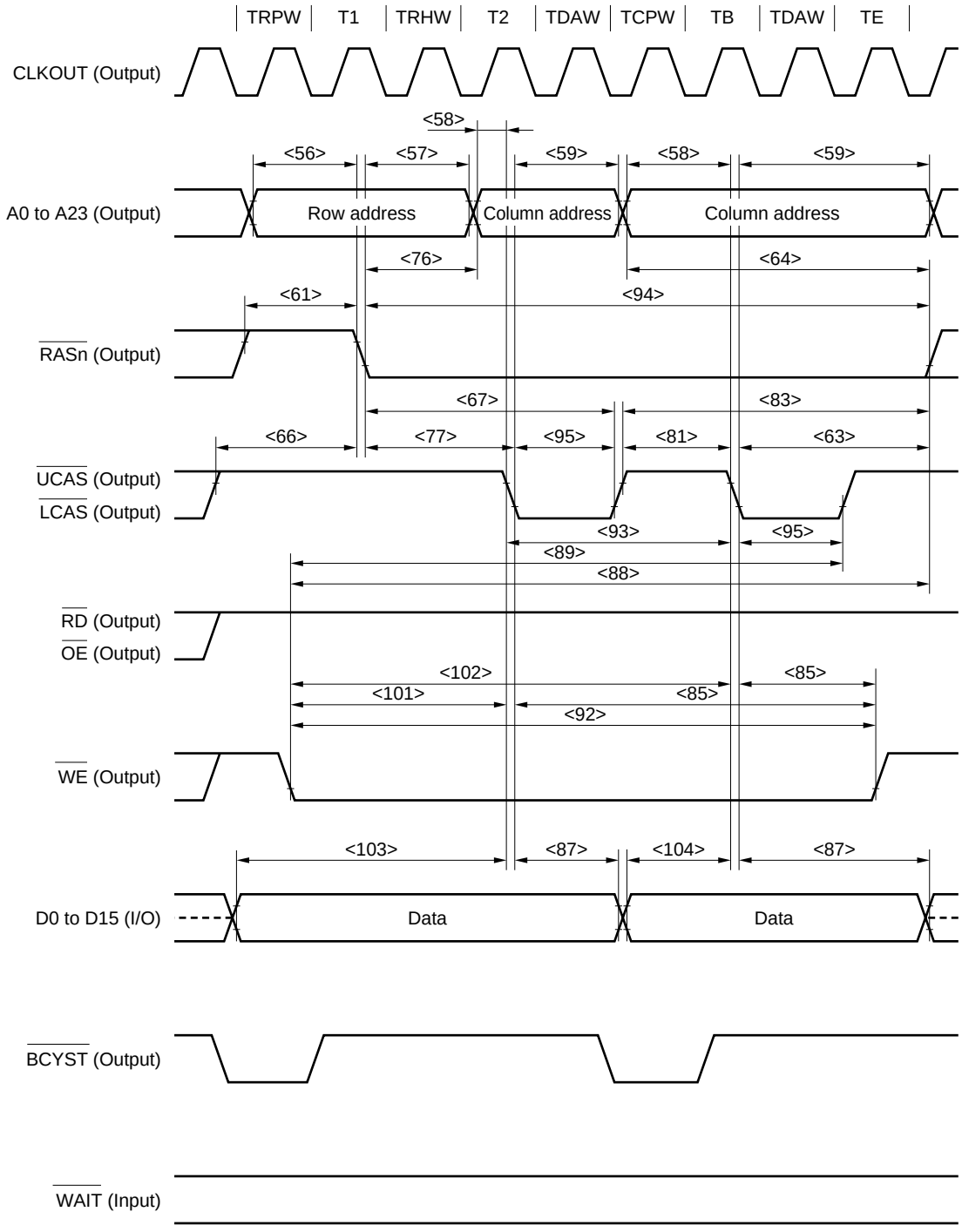
2. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(f) Write timing (EDO DRAM) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data output delay time from $\overline{OE}$ ↑	<37>	t_{DRDOD}		(0.5 + i) T – 10		ns
$\overline{IOWR}$ ↓ delay time from address	<41>	t_{DAWR}		($0.5 + w_{RP}$) T – 5		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$ $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		($2 + w_{RP} + w_{RH} + w_{DA}$) T – 10		ns
Address delay time from $\overline{IOWR}$ ↑	<43>	t_{DWRA}		0.5T – 5		ns
$\overline{RD}$ ↑ delay time from $\overline{IOWR}$ ↑	<48>	t_{DWRRD}	w_F = 0	0		ns
			w_F = 1	T – 10		ns
$\overline{IOWR}$ low-level width	<50>	t_{WWRL}		($2 + w_{RH} + w_{DA} + w$) T – 10		ns
Row address setup time	<56>	t_{ASR}		($0.5 + w_{RP}$) T – 10		ns
Row address hold time	<57>	t_{RAH}		($0.5 + w_{RH}$) T – 10		ns
Column address setup time	<58>	t_{ASC}		0.5T – 10		ns
Column address hold time	<59>	t_{CAH}		($1.5 + w_{DA} + w_F + w$) T – 10		ns
Read/write cycle time	<60>	t_{RC}		($3 + w_{RP} + w_{RH} + w_{DA} + w_F + w$) T – 10		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		($0.5 + w_{RP}$) T – 5		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		($1.5 + w_{DA} + w_F + w$) T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		($2 + w_{CP} + w_{DA} + w_F + w$) T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		($1 + w_{DA} + w_F + w$) T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		($1 + w_{RP}$) T – 10		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		($2 + w_{RH} + w_{DA} + w_F + w$) T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<68>	t_{RCS}		($2 + w_{RP} + w_{RH}$) T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t_{RCH}		1.5T – 10		ns
$\overline{CAS}$ precharge time	<71>	t_{CPN}		($2 + w_{RP} + w_{RH}$) T – 5		ns
$\overline{RAS}$ column address delay time	<76>	t_{RAD}		($0.5 + w_{RH}$) T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time	<77>	t_{RCD}		($1 + w_{RH}$) T – 10		ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. i: the number of idle states that are inserted when a write cycle follows a read cycle.

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output buffer turn-off delay time (from $\overline{OE}$ ↑)		<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)		<79>	t_{OFF}		0		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP})$ T – 5		ns
High-speed page mode cycle time		<82>	t_{PC}		$(2 + w_{CP} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{RAS}$ hold time for CAS precharge		<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{OE}$ → $\overline{CAS}$ hold time (from $\overline{CAS}$ ↑)	Off-page	<96>	t_{OCH1}		$(2.5 + w_{RP} + w_{RH} + w_{DA} + w_F + w)$ T – 10		ns
	On-page	<97>	t_{OCH2}		$(1.5 + w_{CP} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{CAS}$ ↓ delay time from $\overline{DMAAKm}$ ↓		<105>	t_{DDACS}		$(1.5 + w_{RH})$ T – 10		ns
$\overline{CAS}$ ↓ delay time from $\overline{IOWR}$ ↓		<106>	t_{DRDCS}		$(1 + w_{RH})$ T – 10		ns

Remarks 1. T=t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

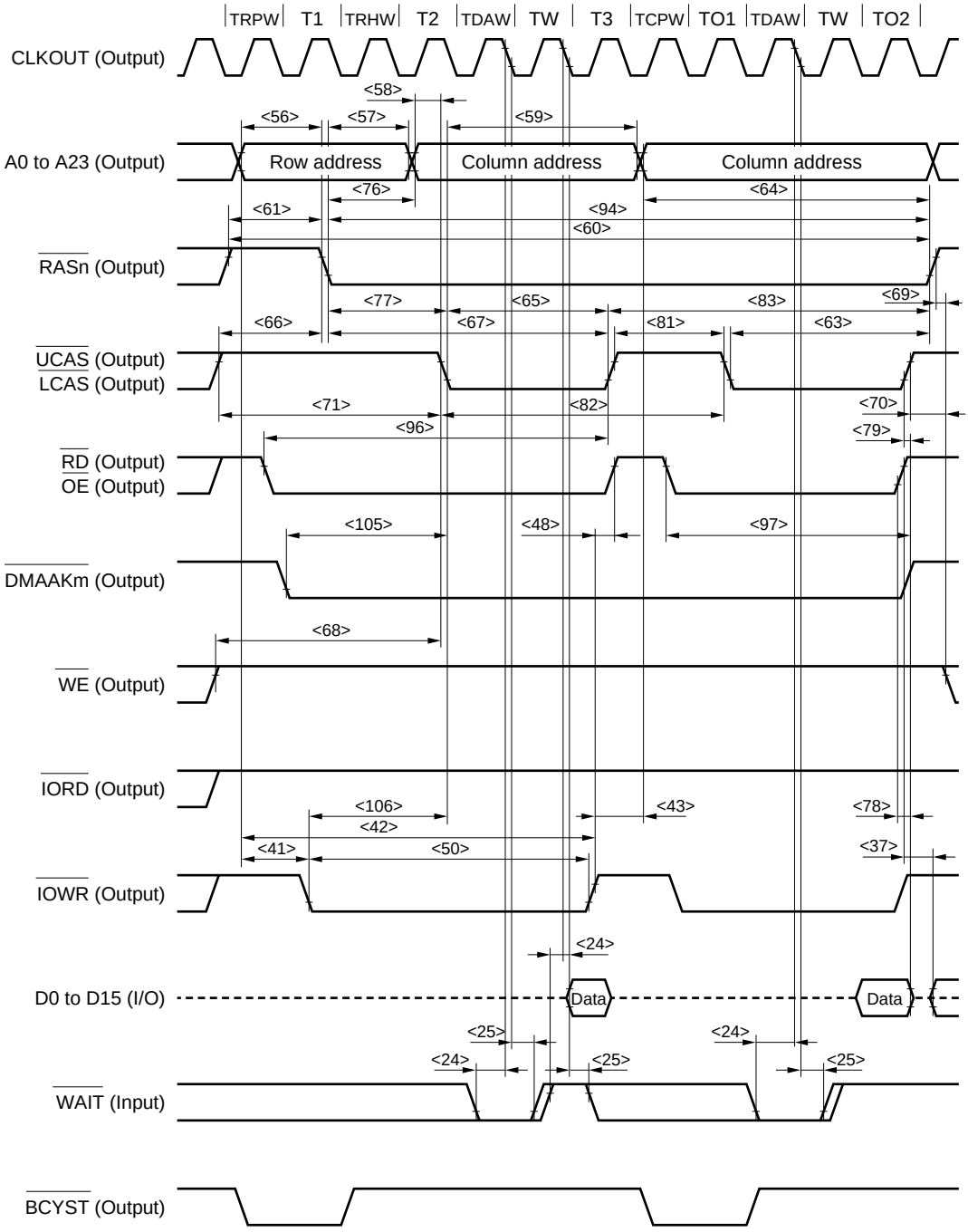
5. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. m = 0 to 3

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)		<24>	t_{SWK}		10		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)		<25>	t_{HKW}		2		ns
$\overline{IORD}$ low-level width		<32>	t_{WRDL}		$(2 + w_{RH} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{IORD}$ high-level width		<33>	t_{WRDH}		T – 5		ns
$\overline{IORD}$ ↑ delay time from address, $\overline{CSn}$		<34>	t_{DARD}		0.5T – 5		ns
Address delay time from $\overline{IORD}$ ↑		<35>	t_{DRDA}		(0.5 + i) T – 5		ns
Row address setup time		<56>	t_{ASR}		$(0.5 + w_{RP})$ T – 10		ns
Row address hold time		<57>	t_{RAH}		$(0.5 + w_{RH})$ T – 10		ns
Column address setup time		<58>	t_{ASC}		0.5T – 10		ns
Column address hold time		<59>	t_{CAH}		$(1.5 + w_{DA} + w_F)$ T – 10		ns
Read/write cycle time		<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}		$(0.5 + w_{RP})$ T – 5		ns
$\overline{RAS}$ hold time		<63>	t_{RSH}		$(1.5 + w_{DA} + w_F)$ T – 10		ns
Column address read time for $\overline{RAS}$		<64>	t_{RAL}		$(2 + w_{CP} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{CAS}$ pulse width		<65>	t_{CAS}		$(1 + w_{DA} + w_F)$ T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time		<66>	t_{CRP}		$(1 + w_{RP})$ T – 10		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{CAS}$ precharge time		<71>	t_{CPN}		$(2 + w_{RP} + w_{RH} + w)$ T – 5		ns
$\overline{RAS}$ column address delay time		<76>	t_{RAD}		$(0.5 + w_{RH})$ T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		$(1 + w_{RH} + w)$ T – 10		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP} + w)$ T – 5		ns
High-speed page mode cycle time		<82>	t_{PC}		$(2 + w_{CP} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA} + w)$ T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)		<85>	t_{WCH}		$(1 + w_{DA})$ T – 10		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)		<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA} + w)$ T – 10		ns
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)		<89>	t_{CWL}	$w_{CP} = 0$	$(1 + w_{DA} + w)$ T – 10		ns
$\overline{WE}$ pulse width		<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA} + w)$ T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA} + w_F + w)$ T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	Off-page	<101>	t_{WCS1}	$w_{CP} = 0$	$(1 + w_{RH} + w_{RP} + w)$ T – 10		ns
	On-page	<102>	t_{WCS2}	$w_{CP} \geq 1$	w_{CP}T – 10		ns

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. i: the number of idle states that are inserted when a write cycle follows a read cycle.

9. n = 0 to 7

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{CAS}$ ↓ delay time from $\overline{DMAAKm}$ ↓	<105>	t_{DDACS}		(1.5 + w_{RH} + w) T – 10		ns
$\overline{CAS}$ ↓ delay time from $\overline{IORD}$ ↓	<106>	t_{DRDCS}		(1 + w_{RH} + w) T – 10		ns
$\overline{IORD}$ ↑ delay time from $\overline{WE}$ ↑	<107>	t_{DWERD}	w_F = 0	0		ns
			w_F = 1	T – 10		ns

Remarks 1. T = t_{CYK}

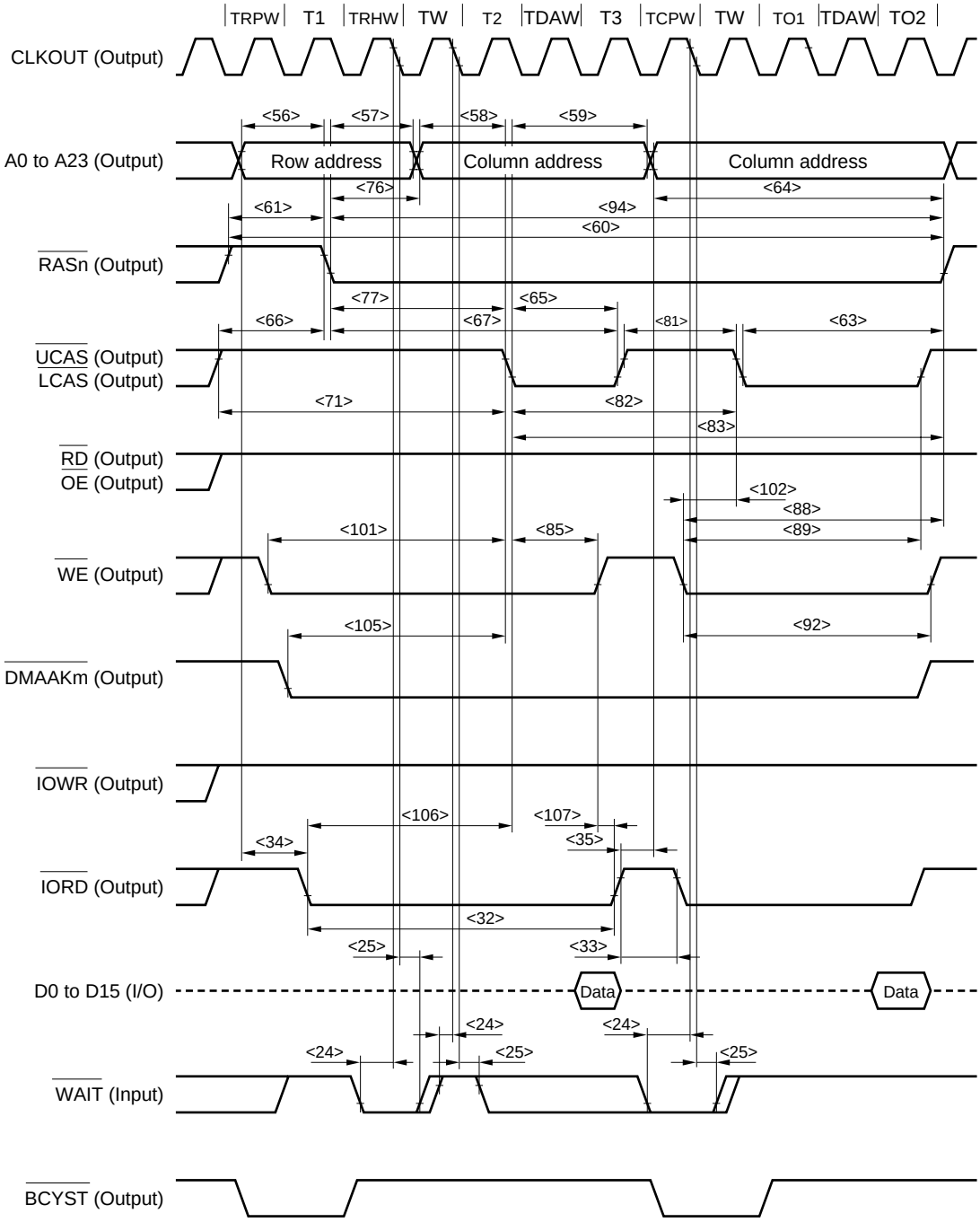
2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(i) CBR refresh timing

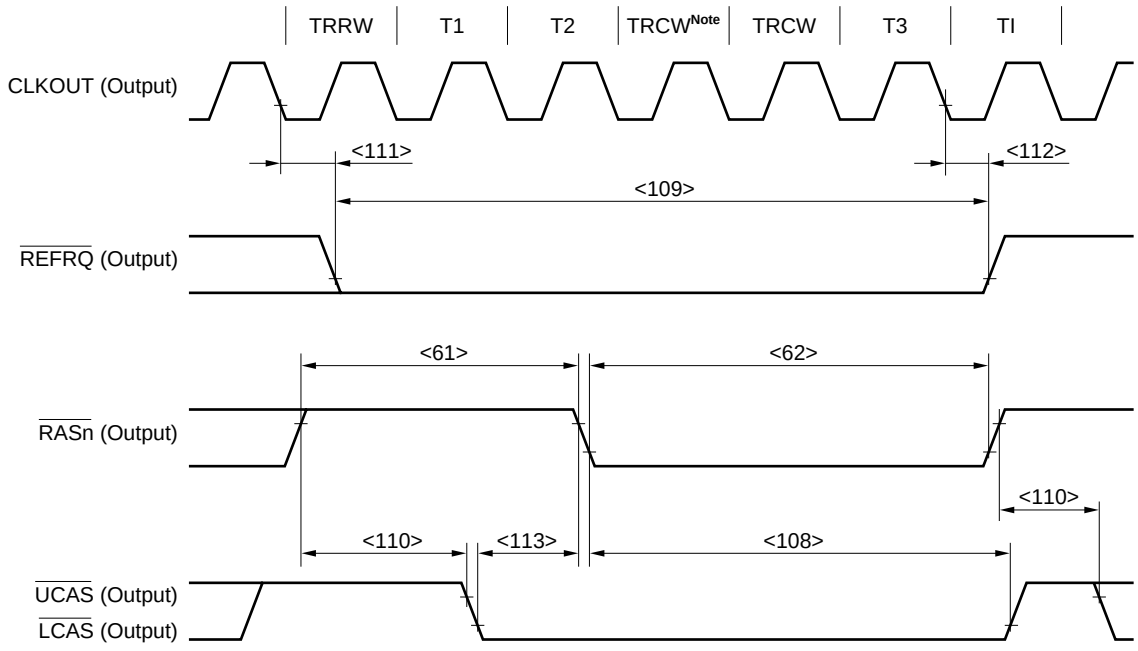
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{RAS}$ precharge time	<61>	t_{RP}		(1.5 + w_{RRW}) T – 5		ns
$\overline{RAS}$ pulse width	<62>	t_{RAS}		(1.5 + w_{RCW}[Note]) T – 10		ns
$\overline{CAS}$ hold time	<108>	t_{CHR}		(1.5 + w_{RCW}[Note]) T – 10		ns
$\overline{REFRQ}$ pulse width	<109>	t_{WRFL}		(3 + w_{RRW} + w_{RCW}[Note]) T – 10		ns
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	<110>	t_{RPC}		(0.5 + w_{RRW}) T – 10		ns
$\overline{REFRQ}$ active delay time (from CLKOUT ↑)	<111>	t_{DKRF}		2	10	ns
$\overline{REFRQ}$ inactive delay time (from CLKOUT ↑)	<112>	t_{HKRF}		2	10	ns
$\overline{CAS}$ setup time	<113>	t_{CSR}		T – 10		ns

Note At least one clock cycle is inserted by default for w_{RCW} regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. T = t_{CYK}

2. w_{RRW}: the number of waits due to the RRW0 and RRW1 bits of the RWC register.

3. w_{RCW}: the number of waits due to the RCW0 to RCW2 bits of the RWC register.



Note This TRCW is always inserted regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. This is the timing for the following case.
Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1
Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 2

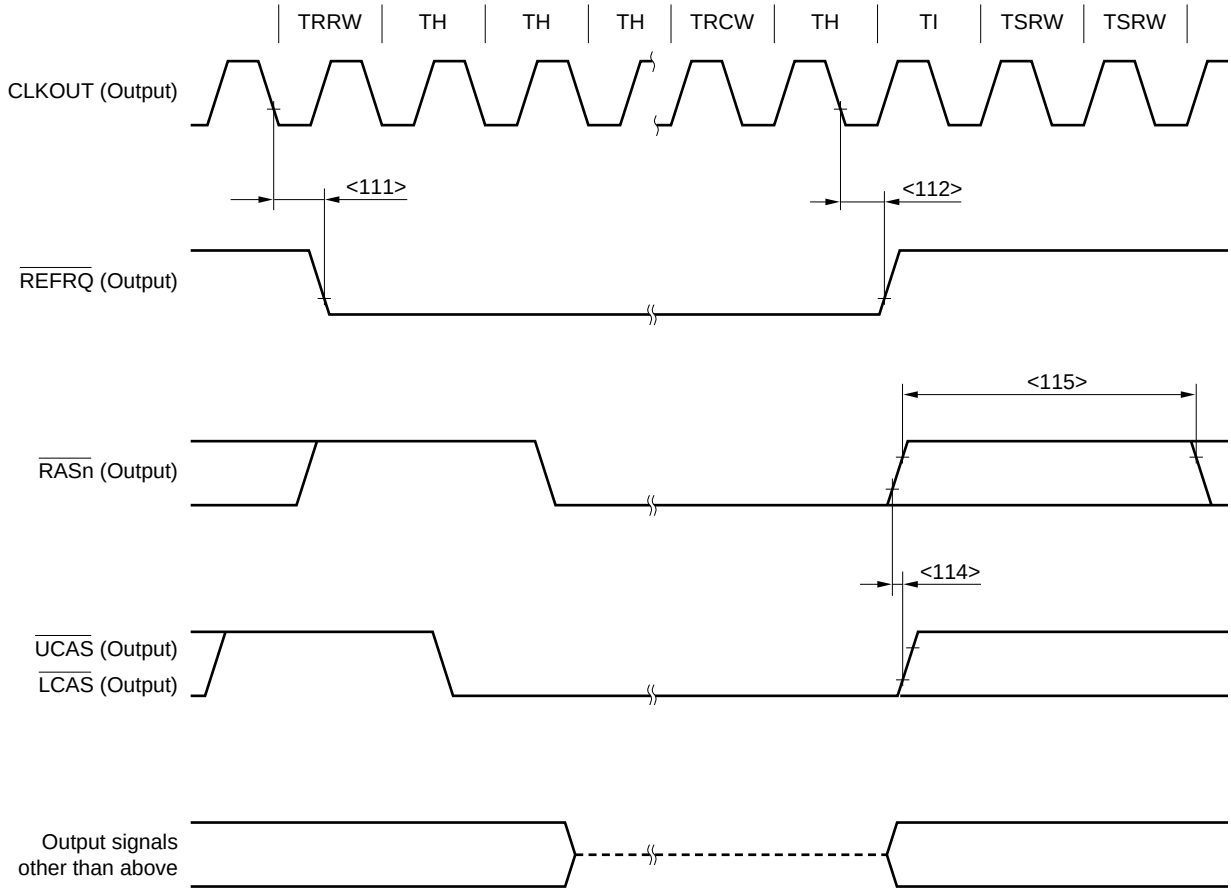
2. n = 0 to 7

(j) CBR self-refresh timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT ↑)	<111>	t_{DKRF}		2	10	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT ↑)	<112>	t_{HKRF}		2	10	ns
$\overline{\text{CAS}}$ hold time	<114>	t_{CHS}		–5		ns
$\overline{\text{RAS}}$ precharge time	<115>	t_{RPS}		(1 + 2w_{SRW}) T – 10		ns

Remarks 1. T = t_{CYK}

2. w_{SRW}: the number of waits due to the SRW0 to SRW2 bits of the RWC register.



Remarks 1. This is the timing for the following case.

Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1

Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 1

Number of waits due to the SRW0 to SRW2 bits of the RWC register (TSRW): 2

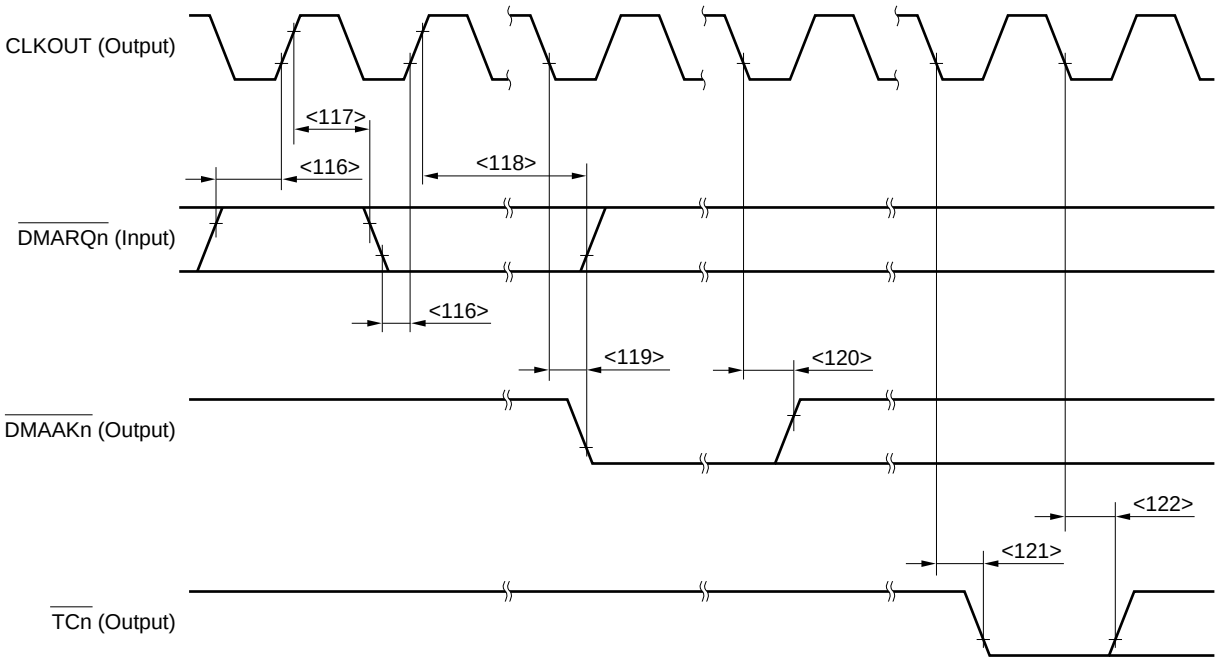
2. The broken lines indicate high impedance.

3. n = 0 to 7

(7) DMAC timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{DMARQn}}$ setup time (to CLKOUT ↑)	<116>	t_{SDRK}		10		ns
$\overline{\text{DMARQn}}$ hold time (from CLKOUT ↑)	<117>	t_{HKDR1}		2		ns
	<118>	t_{HKDR2}		Until $\overline{\text{DMAAKn}}$ ↓		ns
$\overline{\text{DMAAKn}}$ output delay time (from CLKOUT ↓)	<119>	t_{DKDA}		2	10	ns
$\overline{\text{DMAAKn}}$ output hold time (from CLKOUT ↓)	<120>	t_{HKDA}		2	10	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT ↓)	<121>	t_{DKTC}		2	10	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT ↓)	<122>	t_{HKTC}		2	10	ns

Remark n = 0 to 3



Remark n = 0 to 3

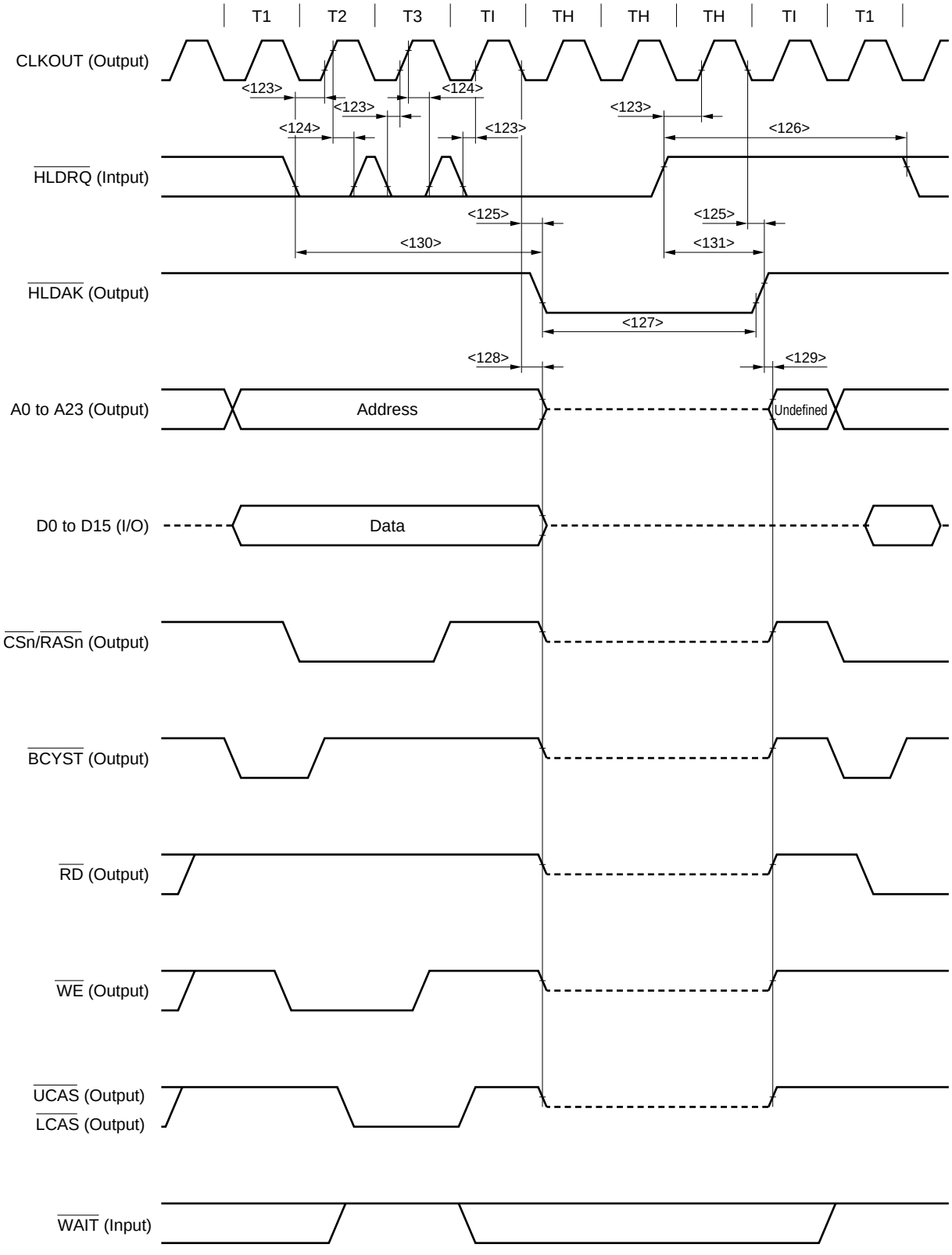
[MEMO]

(8) Bus hold timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↑)	<123>	t_{SHRK}		10		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↑)	<124>	t_{HKHR}		5		ns
$\overline{\text{HLDAK}}$ delay time from CLKOUT ↓	<125>	t_{DKHA}		2	10	ns
$\overline{\text{HLDRQ}}$ high-level width	<126>	t_{WHQH}		T + 17		ns
$\overline{\text{HLDAK}}$ low-level width	<127>	t_{WHAL}		T – 8		ns
Bus float delay time from CLKOUT ↓	<128>	t_{DKCF}			10	ns
Bus output delay time from $\overline{\text{HLDAK}}$ ↑	<129>	t_{DHAC}		0		ns
$\overline{\text{HLDAK}}$ ↓ delay time from $\overline{\text{HLDRQ}}$ ↓	<130>	t_{DHQHA1}		2.5T		ns
$\overline{\text{HLDAK}}$ ↑ delay time from $\overline{\text{HLDRQ}}$ ↑	<131>	t_{DHQHA2}		0.5T	1.5T	ns

Remark T = t_{CYK}

(8) Bus hold timing (2/2)



Remarks 1. The broken lines indicate high impedance.

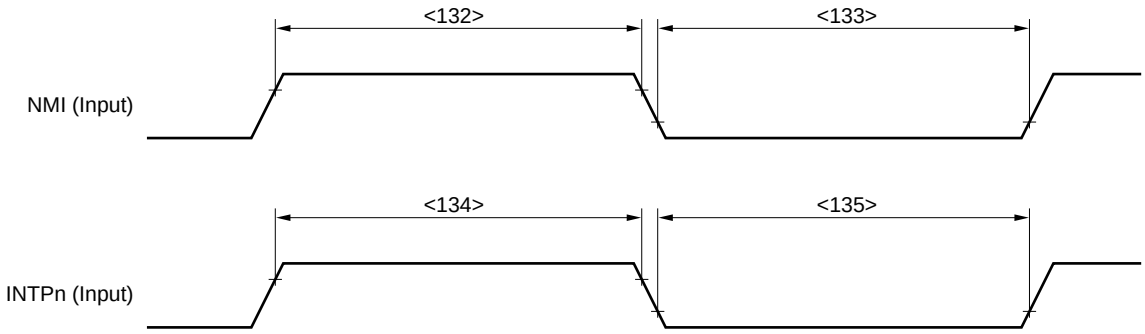
2. n = 0 to 7

(9) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<132>	t_{WNIH}		500		ns
NMI low-level width	<133>	t_{WNIL}		500		ns
INTPn high-level width	<134>	t_{WITH}		4T + 10		ns
INTPn low-level width	<135>	t_{WITL}		4T + 10		ns

Remarks 1. n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153

2. T = t_{CYK}



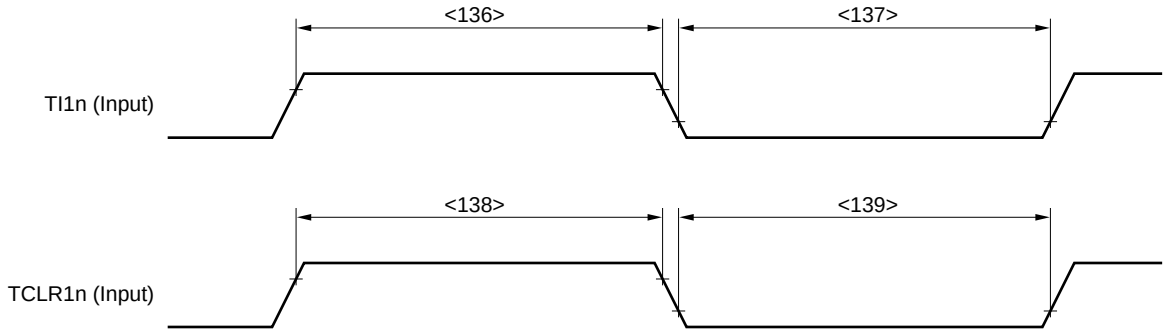
Remark n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1n high-level width	<136>	t_{WTIH}		3T + 18		ns
TI1n low-level width	<137>	t_{WTIL}		3T + 18		ns
TCLR1n high-level width	<138>	t_{WTCH}		3T + 18		ns
TCLR1n low-level width	<139>	t_{WTCL}		3T + 18		ns

Remarks 1. n = 0 to 5

2. T = t_{CYK}

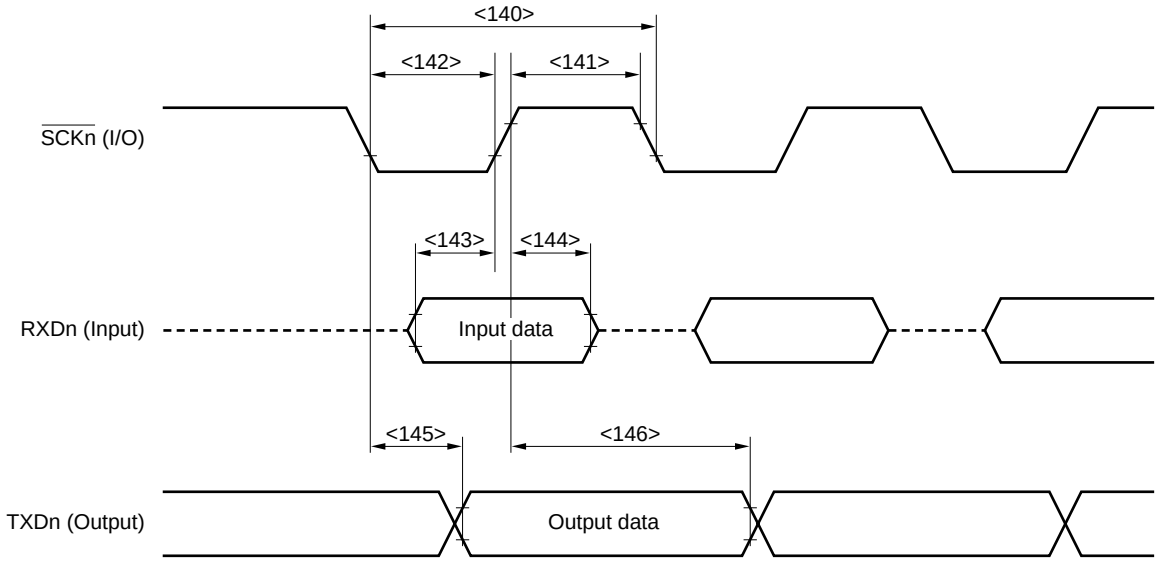


Remark n = 0 to 5

(11) UART0, UART1 timing (clock-synchronized or master mode only)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<140>	t_{CYSK0}	Output	250		ns
$\overline{\text{SCKn}}$ high-level width	<141>	t_{WSK0H}	Output	$0.5t_{CYSK0} - 20$		ns
$\overline{\text{SCKn}}$ low-level width	<142>	t_{WSK0L}	Output	$0.5t_{CYSK0} - 20$		ns
RXDn setup time (to $\overline{\text{SCKn}}$ ↑)	<143>	t_{SRXSK}		30		ns
RXDn hold time (from $\overline{\text{SCKn}}$ ↑)	<144>	t_{HSKRX}		0		ns
TXDn output delay time (from $\overline{\text{SCKn}}$ ↓)	<145>	t_{DSKTX}			20	ns
TXDn output hold time (from $\overline{\text{SCKn}}$ ↑)	<146>	t_{HSKTX}		$0.5t_{CYSK0} - 5$		ns

Remark n = 0, 1



Remarks 1. The broken lines indicate high impedance.

2. n = 0, 1

(12) CSI0 to CSI3 timing

(a) Master mode

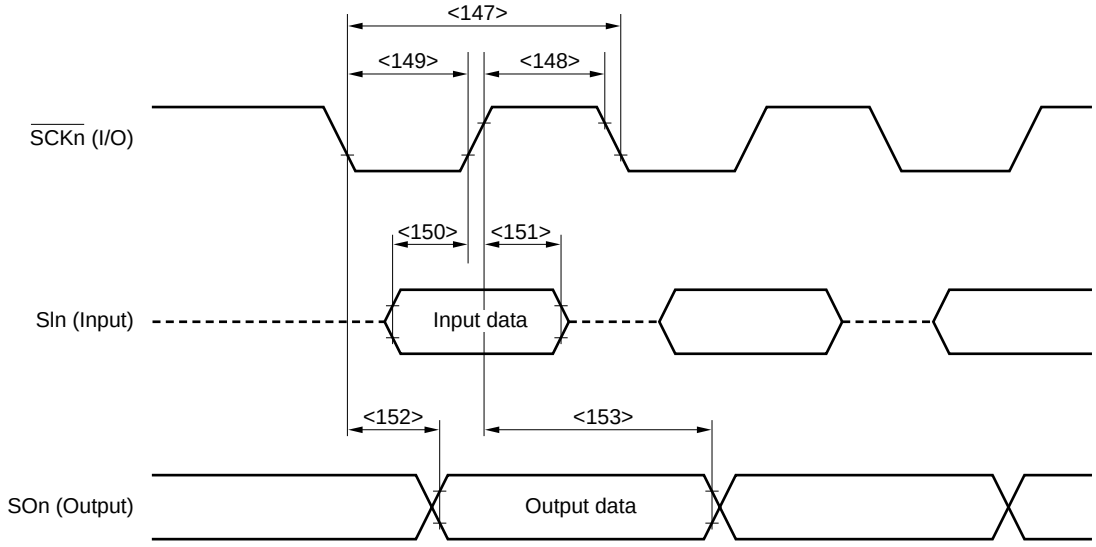
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<147>	t_{CYSK1}	Output	100		ns
$\overline{\text{SCKn}}$ high-level width	<148>	t_{WSK1H}	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{\text{SCKn}}$ low-level width	<149>	t_{WSK1L}	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{\text{SCKn}}$ ↑)	<150>	t_{SSISK}		30		ns
SIn hold time (from $\overline{\text{SCKn}}$ ↑)	<151>	t_{HSKSI}		0		ns
SOn output delay time (from $\overline{\text{SCKn}}$ ↓)	<152>	t_{DSKSO}			20	ns
SOn output hold time (from $\overline{\text{SCKn}}$ ↑)	<153>	t_{HSKSO}		$0.5t_{CYSK1} - 5$		ns

Remark n = 0 to 3

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<147>	t_{CYSK1}	Input	100		ns
$\overline{\text{SCKn}}$ high-level width	<148>	t_{WSK1H}	Input	30		ns
$\overline{\text{SCKn}}$ low-level width	<149>	t_{WSK1L}	Input	30		ns
SIn setup time (to $\overline{\text{SCKn}}$ ↑)	<150>	t_{SSISK}		10		ns
SIn hold time (from $\overline{\text{SCKn}}$ ↑)	<151>	t_{HSKSI}		10		ns
SOn output delay time (from $\overline{\text{SCKn}}$ ↓)	<152>	t_{DSKSO}			30	ns
SOn output hold time (from $\overline{\text{SCKn}}$ ↑)	<153>	t_{HSKSO}		t_{WSK1H}		ns

Remark n = 0 to 3



Remarks 1. The broken lines indicate high impedance.

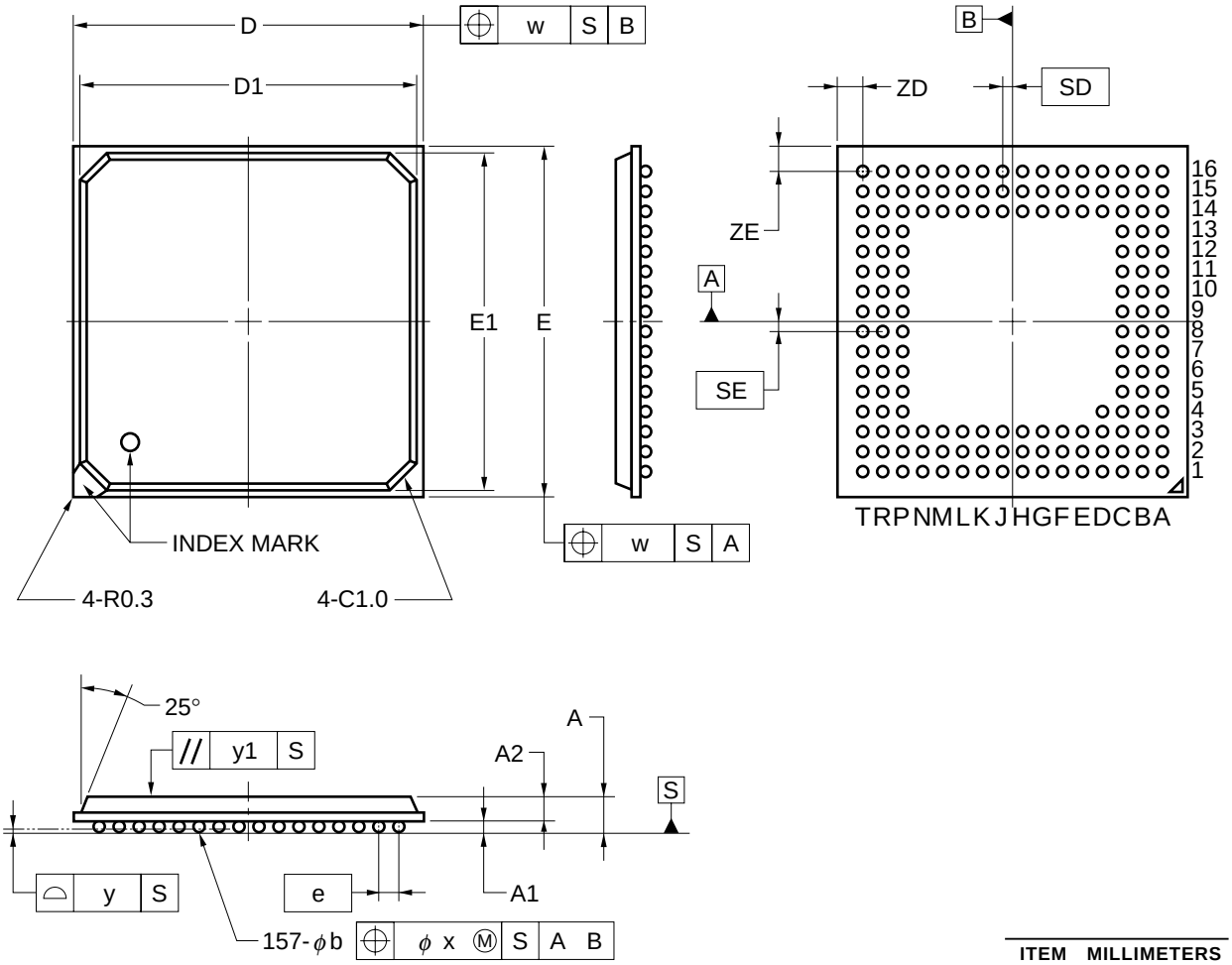
2. n = 0 to 3

A/D Converter Characteristics (T_A = –40 to +70°C ... μPD703100A-40,
T_A = –40 to +85°C ... μPD703100A-33, μPD703101A-33, μPD703102A-33,
$V_{DD} = HV_{DD} = CV_{DD}$ = 3.0 to 3.6 V, V_{SS} = 0 V,
V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD}, output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Total error	–				±5	LSB
Quantization error	–				± 1/2	LSB
Conversion time	t_{CONV}		5		10	μs
Sampling time	t_{SAMP}		833			ns
Zero scale error	–				±5	LSB
Full scale error	–				±5	LSB
Nonlinearity error	–				±3	LSB
Analog input voltage	V_{IAN}		–0.3		AV_{REF} + 0.3	V
Analog input resistance	R_{AN}			1.0		MΩ
AV_{REF} input voltage	AV_{REF}	$AV_{REF} = AV_{DD}$	3.0		AV_{DD}	V
AV_{REF} input current	AI_{REF}				2.0	mA
AV_{DD} current	AI_{DD}				5.0	mA

17. PACKAGE DRAWING

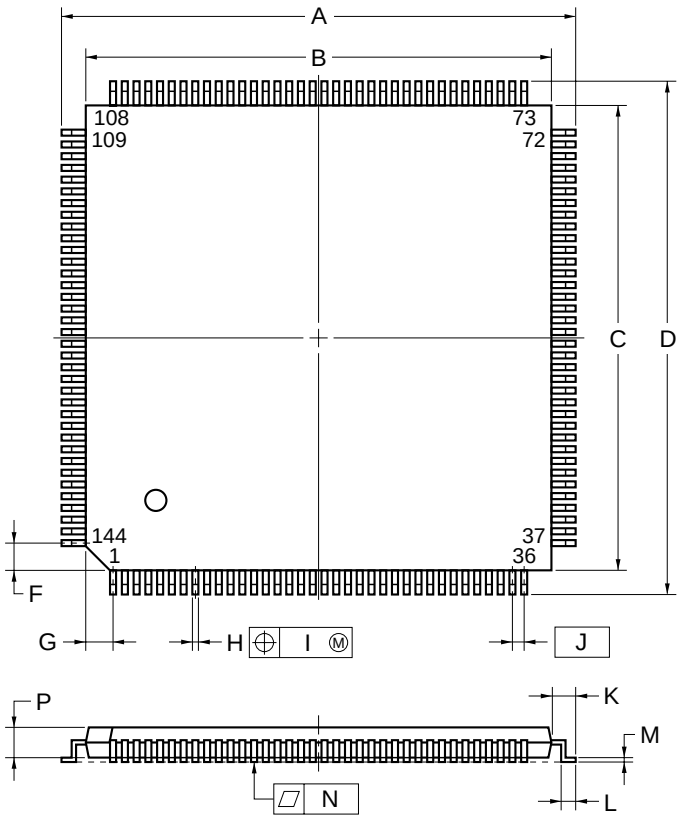
157-PIN PLASTIC FBGA (14x14)

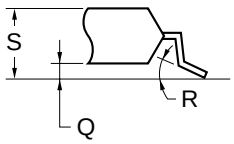


ITEM	MILLIMETERS
D	14.0±0.1
D1	13.4
E	14.0±0.1
E1	13.4
w	0.20
e	0.8
A	1.31±0.15
A1	0.35±0.10
A2	0.96
b	$0.5^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.2
SD	0.4
SE	0.4
ZD	1.0
ZE	1.0

S157F1-80-FA1

144 PIN PLASTIC LQFP (FINE PITCH) (20×20)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	22.0±0.2	0.866±0.008
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	3^{+7}_{-3}	3^{+7}_{-3}
S	1.7 MAX.	0.067 MAX.

S144GJ-50-8EU-2

18. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 18-1. Surface Mounting Type Soldering Conditions

(1) μPD703100AF1-33-FA1: 157-pin plastic FBGA (14 × 14 mm)
μPD703100AF1-40-FA1: 157- pin plastic FBGA (14 × 14 mm)
μPD703101AF1-33-×××-FA1: 157- pin plastic FBGA (14 × 14 mm)
μPD703102AF1-33-×××-FA1: 157- pin plastic FBGA (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 sec. Max. (At 210°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (Per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

(2) μPD703100AGJ-33-8EU: 144-pin plastic LQFP (fine pitch) (20 × 20 mm)
μPD703100AGJ-40-8EU: 144-pin plastic LQFP (fine pitch) (20 × 20 mm)
μPD703101AGJ-33-×××-8EU: 144-pin plastic LQFP (fine pitch) (20 × 20 mm)
μPD703102AGJ-33-×××-8EU: 144-pin plastic LQFP (fine pitch) (20 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related Documents μPD70F3102-33 Data Sheet (U13844E)
μPD703100-33, μPD703100-40, μPD703101-33, μPD703102-33 Data Sheet (U13995E)
μPD70F3102A-33 Data Sheet (U13845E)

Reference Materials: Electrical Characteristics for Microcomputer (IEI-601[Note])

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Lisence not needed : μPD703100A-33, 703100A-40
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