NCT6686D

Nuvoton eSIO

HARDWARE DATASHEET
(External Architecture)

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1. GENERAL DESCRIPTION

NCT6686D is a high performance 8 bit microcontroller to execute MCS51 instruction set. A rich set of features and peripherals enable to match many specific applications, for example, PC mother board Super IO, Notebook/Netbook EC controller or consumer health monitor embedded controller.

The microcontroller includes memory pointer, interrupts, interfaces for serial communication, I2C and SPI interfaces, a timer system, I/O ports, power management unit, multiplication-division unit, watchdog timer and DMA controller. Integrated on-chip debugger is also available.

NCT6686D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO port may serve as simple I/O ports or may be individually configured to provide alternative functions. The GPIO can be programmed to generate interrupt microcontroller. Also the GPIO can be programmed to generate flexible power-on sequence for different CPU and chipset.

NCT6686D monitors several critical parameters in hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, NCT6686D adopts the Current Mode (dual current source) and thermistor sensor approach, as well as PECI (Platform Environment Control Interface) and AMD SB-TSI interface. NCT6686D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ III and SMART Tracking, which makes the system more stable and user-friendly.

NCT6686D supports SMBus host/slave function. As a master, it could access multiple slave devices; as a slave, it could be accessed for reporting useful information.

NCT6686D provides an USB host interface to connect to USB device. Different kinds of USB application could be implemented by firmware.

NCT6686D provides two high-speed serial communication ports (UART), each of them includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K or 921K bps to support higher speed moderms.

NCT6686D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

2. FEATURES

- 1 T XC8051
- 16K bytes of data RAM
- MCU runs on EXTERNAL serial program storage (NOR Flash with SPI interface) on the fly directly. Address space up to 16M bytes was supported.(23-bit addressing).
- MCU interrupt on various system events, to enable glue logic enhancements and customization
- Access to any of NCT6686D registers to provide:
  --- Control over the SIO pin selection.
  --- Control over the configuration of any NCT6686D function or devices.
  --- Control and monitoring of any GPIO pin
- Peripherals
  --- 2 serial ports
  --- 3 timer counters
  --- Internal watchdog timer
  --- SMBus Interfaces used for:
    - Master : Temperature reading
    - Slave : Providing infrastructure for MCTP/PLDM and ASF-based manageability
    - Slave : Remote access to the device registers
  --- SPI interfaces
    - code fetch of NCT6686D execution
  --- USB interface
- 14.318 MHz operation clock with crystal input (Xin / Xout)
- Adjustable internal clock for various utilizations
- Flexible ISP (In-System-Program) Interfaces
  --- LPC Bus
  --- eSPI Bus
  --- SPI (from KBMS pin)

System Hardware Management Support

- Digital Thermal interfaces
  --- PECI 3.0 for Intel CPU thermal monitoring and support up to address 8 CPUs and 2 domains
  --- SB-TSI 1.0/APML for AMD CPU thermal monitoring
  --- SMBus devices.
- Local and remote Thermal measurement sensors
  --- external Thermal Diode or Thermistor monitor interfaces
  --- internal Thermal measurement diode
- Incorporates 8-bit analog-to-digital converter
  --- Analog inputs filtering
  --- Firmware-based digital filtering
  --- Remote thermal sensing designed for typical precision of 1 ^{o}C.
  --- 0.125 ^{o}C resolution.
- Fan Monitor and Control
  --- Adaptive fan control algorithm
  --- 8 PWM-based output fan controls
  --- Up to 8 fan speed monitoring inputs with 12-bit resolution tachometers
  --- Automatic temperature feedback control.
- Generates SMI on critical temperature events

- Voltage Monitoring
  --- Up to 10 VIN
  --- VSB, AVSB, VCC3
  --- VBAT

General Purpose I/O Ports

- GPIO pins can be used either by the MCU or by the host
- All GPIO pins individually configured as input or output
- Programmable features for each output pin:
  --- Drive type (open-drain, push-pull or TRI-STATE
  --- TRI-STATE condition on detection of falling VDD3 for VSB3-powered pins driving VDD-supplied devices
- Programmable option for internal pull-up resistor on some input pin (some with internal pull-down resistor option)
- Lock option for the configuration and data of each GPIO port
- 16 pins can generate MCU interrupt events for the internal microcontroller
- GPIO pins generate IRQ/SIOPME/SMI for wake-up events. Each GPIO has separate:
  --- Enable control of event status routing to IRQ (For Each GPIO Input)
  --- Enable control of event status routing to SIOPME (Only for GPIO Enhance port)
  --- Polarity and edge/level selection
  --- Optional de-bouncing

Diagnostics

- High current driver power indicator LED blinking
  --- Dual Color Control
  --- Fading Mode
- Support two ports for Port80-like message output. Each port supports two digits.
  --- Directly drive 7-Segment LEDs
  --- The decode port is configurable.
  --- To save pin counts, it would be better to support 4 digits with same 7 data pins(LEDA~LEDG).
  --- Through UART port

Fail-safe ACPI and Optional Firmware-Enhanced Features (Control through EC Space)

- ACPI power sequence controls and glue logics, such as RSMRST#, PSON#, PWROK0, RSTOUT0#, PSIN, PSOUT#, ATXPGD, SLP_S3#, SLP_S5#,
  --- Main Power good / power OK signals ATXPGD and internal power sensing.
  --- Power distribution control (for switching between Main and Standby regulators)
  --- Main power supply turn on (PSON#)
  --- Resume reset (Master Reset) according to the stand-by 3V
  --- Reset button de-bouncer
  --- Power Good out mechanism using ATXPGD and internal power sensing
  --- Buffers PCI_RESET to generate 3 reset output signals
- Power restoring policy when AC was recovered
- Advanced watch dog timers
- Hardware Monitoring (including voltage sources, analog / digital / virtual temperature sources, and tachometers)
- Customizable handling about SKTOCC#, CASEOPEN0#, CASEOPEN1# signals
  --- Battery-backed CaseOpen Alert
- Facilities for modern digital sensor interface, such as PECI 3.0, DIMM temperature pushing back, DIMM Ambient Temperature writing back, Sandy Bridge PCH, SMBus sensors, and automatic polling engines …
- Smart fan control algorithms such as Thermal Cruise, Speed Cruise, Smart Fan 3, Smart Fan 4, DTS1.0 and DTS2.0 Control, and Smart Tracking for both Duty/RPM control
- Front Panel Power LED with different blinking patterns and fading effect
- Port 80 Message Buffering with / without 7-segment LED driving
- Up to 5 CIR keys to wake up system from sleep state
- OEM SMBus Slave Interface to allow hardware control from SMBus master such as BMC
- Intel cTDP and LPM support

Power Management

- Supports ACPI Specification Revision 3.0, September 2004
- System Wake-Up Control (SWC)
  --- VSB3-powered event detection and event-logic configuration
  --- Optional routing of events to generate SIOPME
- SIOPME on detection of:
  --- Keyboard key strokes
  --- Mouse movement and/or button click
  --- Ring Indication RI on each of the two serial ports
  --- General-Purpose Input Events from 16 GPIO pins
  --- IRQs of the Keyboard and Mouse Controller
  --- IRQs of the other internal modules
  --- Optional routing of the SCI (SIOPME) to generate IRQ (SERIRQ)
  --- Implements GPE1_BLK of the ACPI General Purpose
- Power status indications
  — VBAT-powered indication of the Main power supply state before an AC power failure
- Extended Power and Wake-Up Control
  — Complements chipset's ACPI controller
  — Low Battery indication
- Advanced Power Saving Control

General

- SMBus access into any of the device registers for data read and configuration
- LPC Bus Interface
  --- Based on Intel's LPC Interface Specification Revision 1.1, August 2002
  --- I/O, Memory and 8-bit Firmware Memory read and write cycles
  --- Up to four 8-bit DMA channels and support LPC DMA
  --- 15 IRQ routing options to serial IRQ
- eSPI Bus Interface
  --- Based on Intel's eSPI Interface Specification
- Configuration Control
  --- PnP Configuration Register structure
  --- Compliant with PC2001 Specification Revision 1.0, 1999-2000
  --- Pre-configurable Base Address of Super I/O Index-Data register pair (defaults to 0x2Eh/ 0x2Fh)
  --- VSB3-powered pin multiplexing
- 5 V tolerance pins supported

LEGACY I/O Functions

- UARTx2
- Parallel port
- KBC
- Infrared
  SIR
  CIR – RLC (Running Length Code, could be used to parse RC5/RC6/QP protocols)
  CIR Receiving - long distance mode (demodulated) and wide band (modulated)
  CIR Emitting – 2 modulated emitting channel

Package

- 128-pin LQFP

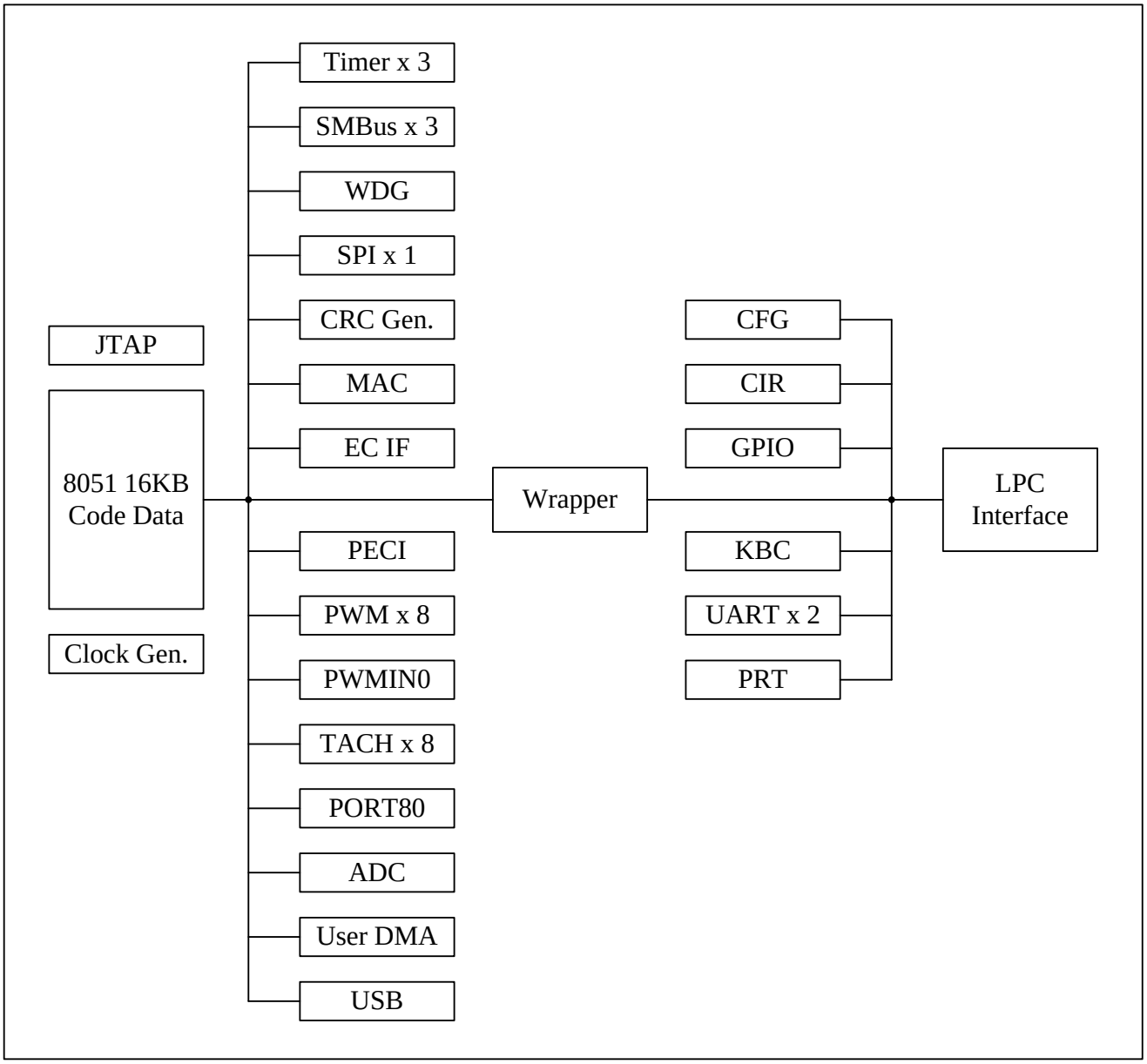


Figure 2-1 NCT6686D Variants Block Diagram

3. PIN LAYOUT

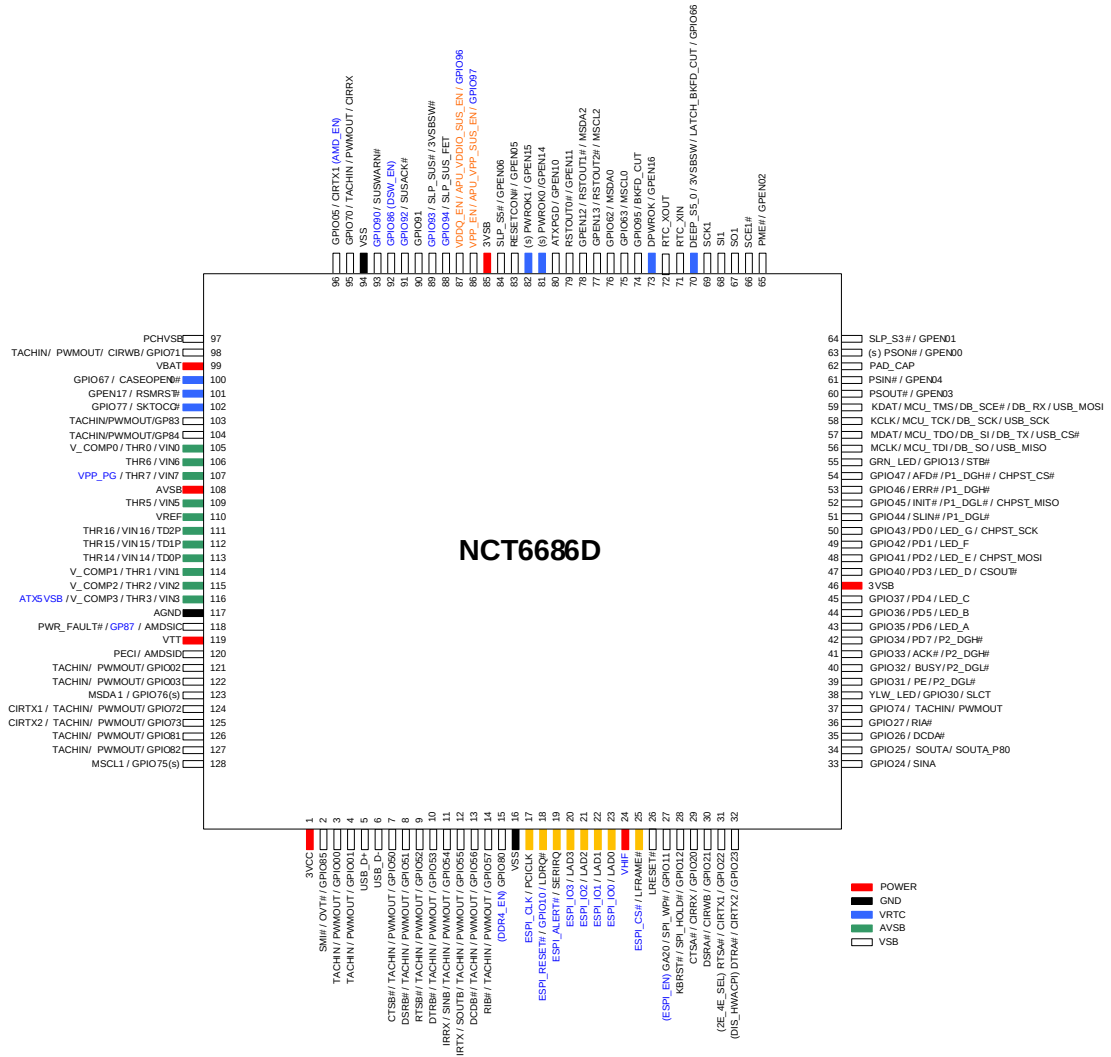


Figure 3-1 Pin Layout for NCT6686D Variants

3.1 PIN MULTIPLEXING

PIN Num	Function_1 (Default)	Function_2	Function_3	Function_4	Function_5
1	3VCC				
2	GPIO85	OVT#	SMI#		
3	GPIO00	PWMOUT	TACHIN		
4	GPIO01	PWMOUT	TACHIN		
5	USB_D+				
6	USB_D-				
7	GPIO50	CTSB#	PWMOUT	TACHIN	
8	GPIO51	DSRB#	PWMOUT	TACHIN	
9	GPIO52	RTSB#	PWMOUT	TACHIN	
10	GPIO53	DTRB#	PWMOUT	TACHIN	
11	GPIO54	SINB	PWMOUT	TACHIN	IRRX
12	GPIO55	SOUTB	PWMOUT	TACHIN	IRTX
13	GPIO56	DCDB#	PWMOUT	TACHIN	
14	GPIO57	RIB#	PWMOUT	TACHIN	
15	GPIO80				
16	VSS				
17	PCICLK		ESPI_CLK		
18	LDRQ#	GPIO10	ESPI_RESET#		
19	SERIRQ		ESPI_ALERT#		
20	LAD3		ESPI_IO3		
21	LAD2		ESPI_IO2		
22	LAD1		ESPI_IO1		
23	LAD0		ESPI_IO0		
24	VHIF				
25	LFRAME#		ESPI_CS#		
26	LRESET#				
27	GPIO11	GA20	SPI_WP#		
28	GPIO12	KBRST#	SPI_HOLD#		
29	GPIO20	CTSA#	CIRRX		
30	GPIO21	DSRA#	CIRWB		
31	GPIO22	RTSA#	CIRTX1		
32	GPIO23	DTRA#	CIRTX2		
33	GPIO24	SINA			
34	GPIO25	SOUTA	SOUTA_P80		
35	GPIO26	DCDA#			
36	GPIO27	RIA#			
37	GPIO74	TACHIN	PWMOUT		
38	YLW_LED	GPIO30	SLCT		
39	GPIO31	PE	P2_DGL#		
40	GPIO32	BUSY	P2_DGL#		
41	GPIO33	ACK#	P2_DGH#		
42	GPIO34	PD7	P2_DGH#		
43	GPIO35	PD6	LED_A		
44	GPIO36	PD5	LED_B		

45	GPIO37	PD4	LED_C		
46	3VSB				
47	GPIO40	PD3	LED_D	CSOUT#	
48	GPIO41	PD2	LED_E	CHPST_MOSI	
49	GPIO42	PD1	LED_F		
50	GPIO43	PD0	LED_G	CHPST_SCK	
51	GPIO44	SLIN#	P1_DGL#		
52	GPIO45	INIT#	P1_DGL#	CHPST_MISO	
53	GPIO46	ERR#	P1_DGH#		
54	GPIO47	AFD#	P1_DGH#	CHPST_CS#	
55	GRN_LED	GPIO13	STB#		
56	MCLK	MCU_TDI	DB_SO	USB_MISO	
57	MDAT	MCU_TDO	DB_SI	DB_TX	USB_CS#
58	KCLK	MCU_TCK	DB_SCK	USB_SCK	
59	KDAT	MCU_TMS	DB_SCE#	DB_RX	USB_MOSI
60	PSOUT#	GPEN03			
61	PSIN#	GPEN04			
62	PAD_CAP				
63	PSON#	GPEN00			
64	SLP_S3#	GPEN01			
65	PME#	GPEN02			
66	SCE1#				
67	SO1				
68	SI1				
69	SCK1				
70	DEEP_S5_0	3VSBSW	LATCH_BKFD_CUT	GPIO66	
71	RTC_XIN				
72	RTC_XOUT				
73	DPWROK	GPEN16			
74	GPIO95	BKFD_CUT			
75	GPIO63	MSCL0			
76	GPIO62	MSDA0			
77	GPEN13	RSTOUT2#	MSCL2		
78	GPEN12	RSTOUT1#	MSDA2		
79	RSTOUT0#	GPEN11			
80	ATXPGD	GPEN10			
81	PWROK0	GPEN14			
82	PWROK1	GPEN15			
83	RESETCON#	GPEN05			
84	SLP_S5#	GPEN06			
85	3VSB				
86	VPP_EN	APU_VPP_SUS_EN	GPIO97		
87	VDDQ_EN	APU_VDDIO_SUS_EN	GPIO96		
88	GPIO94	SLP_SUS_FET			
89	GPIO93	SLP_SUS#	3VSBSW#		
90	GPIO91				
91	GPIO92	SUSACK#			

92	GP86				
93	GPIO90	SUSWARN#			
94	VSS				
95	GPIO70	TACHIN	PWMOUT	CIRRX	
96	GPIO05	CIRTX1			
97	PCHVSB				
98	GPIO71	TACHIN	PWMOUT	CIRWB	
99	VBAT				
100	CASEOPEN0#	GPIO67			
101	RSMRST#	GPEN17			
102	SKTOCC#	GPIO77			
103	GPIO83	TACHIN	PWMOUT		
104	GPIO84	TACHIN	PWMOUT		
105	VIN0	THR0	V_COMP0		
106	VIN6	THR6	VLDT		
107	VIN7	THR7	VPP_PG		
108	AVSB				
109	VIN5	THR5			
110	VREF				
111	TD2P	VIN16	THR16		
112	TD1P	VIN15	THR15		
113	TD0P	VIN14	THR14		
114	VIN1	THR1	V_COMP1		
115	VIN2	THR2	V_COMP2		
116	VIN3	THR3	V_COMP3	ATX5VSB	
117	AGND				
118	AMDSIC	PWR_FAULT#	GP87		
119	VTT				
120	AMDSID	PECI			
121	GPIO02	PWMOUT	TACHIN		
122	GPIO03	PWMOUT	TACHIN		
123	GPIO76	MSDA1			
124	GPIO72	PWMOUT	TACHIN	CIRTX1	
125	GPIO73	PWMOUT	TACHIN	CIRTX2	
126	GPIO61	PWMOUT	TACHIN		
127	GPIO62	PWMOUT	TACHIN		
128	GPIO75	MSCL1			

4. PIN DESCRIPTION

.

Note: Please refer to DC CHARACTERISTICS for details.

AOUT	- Analog output pin
AIN	- Analog input pin
IN_{tp3}	- 3.3V TTL-level input pin
IN_{tsp3}	- 3.3V TTL-level Schmitt-trigger input pin
IN_{tp5}	- 5V TTL-level input pin
IN_{gp5}	- 5V GTL-level input pin
IN_{tdp5}	- 5V TTL level input pin with internal pull-down resistor
IN_{tsp5}	- 5V TTL level Schmitt-trigger input pin
O_{8p3}	- 3.3V output pin with 8-mA source-sink capability
OD_{8p5}	- 5V open-drain output pin with 8-mA source-sink capability
O_{12p3}	- 3.3V output pin with 12-mA source-sink capability
OD_{12p3}	- 3.3V open-drain output pin with 12-mA source-sink capability
OD_{12p5}	- 5V open-drain output pin with 12-mA source-sink capability
O_{24p3}	- 3.3V output pin with 24-mA source-sink capability
OD_{24p5}	- 5V open-drain output pin with 24-mA source-sink capability
I/O_{v3}	- Bi-direction pin with source capability of 6 mA and sink capability of 1 mA

4.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
PME#	65	OD_{12p5}	Generated PME event.
PCICLK	17	IN_{tp5}	PCI-clock 33-MHz input.
LDRQ#	18	O_{12p3}	Encoded DMA Request signal.
SERIRQ	19	IN_{tp3} O_{12p3} OD_{12p3}	Serialized IRQ input / output.
LAD[3:0]	20-23	IN_{tp3} OD_{12p3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	25	IN_{tp3}	Indicates the start of a new cycle or the termination of a broken cycle.
LRESET#	26	IN_{tp3}	Reset signal. It can be connected to the PCIRST# signal on the host.

4.2 ESPI Interface

SYMBOL	PIN	I/O	DESCRIPTION
ESPI_CLK	17	I	The eSPI_CLK provides the reference timing for all the serial input and output operations.
ESPI_RESET#	18	I	Reset the eSPI interface for both master and slaves.
ESPI_ALERT#	19	I	eSPI alert signal
ESPI_IO[3:0]	20-23	I/O	These are bi-directional input/output pins used to transfer data between master and slaves.
ESPI_CS#	25	I	Drving Chip Select# low selects a particular eSPI slave for the transaction.
PLTRST#	26	I	Platform reset can be used to communicate through the PLATFORM reset# vw command.

4.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	DESCRIPTION
SLCT	38	IN_{tsp5}	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PE	39	IN_{tsp5}	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

SYMBOL	PIN	I/O	DESCRIPTION
BUSY	40	IN_{tsp5}	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
ACK#	41	IN_{tsp5}	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
ERR#	53	IN_{tsp5}	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
SLIN#	51	O_{24p3}	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
INIT#	52	O_{24p3}	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
AFD#	54	O_{24p3}	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
STB#	55	O_{12p3}	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD0	50	IN_{tp5} O_{24p3}	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD1	49	IN_{tp5} O_{24p3}	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD2	48	IN_{tp5} O_{24p3}	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD3	47	IN_{tp5} O_{24p3}	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD4	45	IN_{tp5} O_{24p3}	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD5	44	IN_{tp5} O_{24p3}	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

SYMBOL	PIN	I/O	DESCRIPTION
PD6	43	IN_{tp5} O_{24p3}	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD7	42	IN_{tp5} O_{24p3}	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

4.4 Serial Port Interface

SYMBOL	PIN	I/O	DESCRIPTION
RIA#	36	IN_{tp5}	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
DCDA#	35	IN_{tp5}	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
SOUTA	34	O_{12p3}	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
SINA	33	IN_{tp5}	Serial Input. This pin is used to receive serial data through the communication link.
DTRA#	32	O_{12p3}	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
RTSA#	31	O_{12p3}	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
DSRA#	30	IN_{tp5}	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
CTSA#	29	IN_{tp5}	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
RIB#	14	IN_{tsp5}	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
DCDB#	13	IN_{tsp5}	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
SOUTB	12	O_{12p3}	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
SINB	11	IN_{tsp5}	Serial Input. This pin is used to receive serial data through the communication link.
DTRB#	10	O_{12p3}	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
RTSB#	9	O_{12p3}	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
DSRB#	8	IN_{tsp5}	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.

SYMBOL	PIN	I/O	DESCRIPTION
CTSB#	7	IN_{tsp5}	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

4.5 KBC Interface

SYMBOL	PIN	I/O	DESCRIPTION
GA20	27	O_{12p3}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST#	28	O_{12p3}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	58	IN_{tsp5} OD_{12p5}	Keyboard Clock.
KDAT	59	IN_{tsp5} OD_{12p5}	Keyboard Data.
MCLK	56	IN_{tsp5} OD_{12p5}	PS2 Mouse Clock.
MDAT	57	IN_{tsp5} OD_{12p5}	PS2 Mouse Data.

4.6 CIR Interface

SYMBOL	PIN	I/O	DESCRIPTION
CIRRX	29	IN_{tp5}	CIR input for long length
CIRRX	95	IN_{tsp5}	CIR input for long length
CIRTX1	31	O_{12p3}	CIR transmission output
CIRTX1	96	O_{12p3}	CIR transmission output
CIRTX1	124	O_{12p3}	CIR transmission output
CIRTX2	32	O_{12p3}	CIR transmission output
CIRTX2	125	O_{12p3}	CIR transmission output
CIRWB	30	IN_{tp5}	CIR input for wide band.
CIRWB	98	IN_{tsp5}	CIR input for wide band.

4.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	DESCRIPTION
CASEOPEN0#	100	IN_{tp5}	CASE OPEN detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
SKTOCC#	102	IN_{tp5}	CPU socket occupied detection

SYMBOL	PIN	I/O	DESCRIPTION
VREF	110	AOUT	Reference Voltage
V_COMP3	116	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
V_COMP2	115	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
V_COMP1	114	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
V_COMP0	105	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
ATX5VSB	116	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN16	111	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN15	112	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN14	113	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN7	107	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN6	106	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN5	109	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN3	116	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN2	115	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN1	114	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
VIN0	105	AIN	Analog input for voltage measurement (Range: 0 to 2.048 V)
THR16	111	AIN	Thermistor Input
THR15	112	AIN	Thermistor Input
THR14	113	AIN	Thermistor Input
THR7	107	AIN	Thermistor Input
THR6	106	AIN	Thermistor Input
THR5	109	AIN	Thermistor Input
THR3	116	AIN	Thermistor Input
THR2	115	AIN	Thermistor Input
THR1	114	AIN	Thermistor Input
THR0	105	AIN	Thermistor Input
TP2P	111	AIN	The input of temperature sensor 2.
TD1P	112	AIN	The input of temperature sensor 1.
TD0P	113	AIN	The input of temperature sensor 0.
OVT#	2	OD_{12p5}	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit.
SMI#	2	OD_{12p5}	System Management Interrupt channel output.
TACHPWM	3	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	4	IN_{tsp5}	0 to +3 V amplitude fan tachometer input

SYMBOL	PIN	I/O	DESCRIPTION
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	7	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	8	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	9	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	10	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	11	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	12	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	13	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	14	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	37	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	95	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	98	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	103	IN_{tsp5}	0 to +3 V amplitude fan tachometer input

SYMBOL	PIN	I/O	DESCRIPTION
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	104	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	121	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	122	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	124	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	125	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	126	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.
TACHPWM	127	IN_{tsp5}	0 to +3 V amplitude fan tachometer input
		O_{12p3} OD_{12p5}	PWM duty-cycle signal for fan speed control.

4.8 SPI Interface

SCE1#	66	O_{12p3}	Chip enable of MCU SPI interface 1. MCU fetches code from this port.
SCK1	69	O_{12p3}	Clock out of MCU SPI interface 1. MCU fetches code from this port.
SI1	68	IN_{tp5} O_{12p3}	Serial data in of MCU SPI interface 1. MCU fetches code from this port.
SO1	67	IN_{tp5} O_{12p3}	Serial data out of MCU SPI interface 1. MCU fetches code from this port.
SPI_HOLD#	28	IN_{tp5} O_{12p3}	SPI flash hold pin. MCU can fetch code in quad mode operation from this port.
SPI_WP#	27	IN_{tp5} O_{12p3}	SPI flash write protect pin. MCU can fetch code in quad mode operation from this port.

4.9 PECI Interface

SYMBOL	PIN	I/O	DESCRIPTION
PECI	120	I/O_{V3}	INTEL® CPU PECI interface. Connect to CPU.

4.10 SB-TSI Interface

SYMBOL	PIN	I/O	DESCRIPTION
AMDSIC	118	OD_{12p3}	AMD® SB-TSI clock input
AMDSID	120	IN_{tsp3} OD_{12p3}	AMD® SB-TSI data input / output

4.11 Advanced Configuration & Power Interface

SYMBOL	PIN	I/O	DESCRIPTION
PSIN#	61	IN_{tp5}	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
PSOUT#	60	OD_{12p5}	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
RSMRST#	101	OD_{8p5}	Resume reset signal output.
SLP_S3#	64	IN_{tp5}	SLP_S3# input.
SLP_S5#	84	IN_{tp5}	SLP_S5# input.
ATXPGD	80	IN_{tsp5}	ATX power good signal.
PSON#	63	OD_{12p5}	Power supply on-off output.
PWROK0	81	OD_{8p5}	3VCC PWROK0 signal.
PWROK1	82	OD_{8p5}	3VCC PWROK1 signal.
DPWROK	73	OD_{8p5}	V3A signal output
RESETCON#	83	IN_{tsp5}	Connect to the reset button.
RSTOUT0#	79	OD_{24p5}	PCI Reset Buffer 0.
RSTOUT1#	78	OD_{24p5}	PCI Reset Buffer 1.
RSTOUT2#	77	OD_{24p5}	PCI Reset Buffer 2.
3VSBSW#	89	OD_{12p3}	3V Switch Auxiliary Enable. Controls switching 3V standby supply.
3VSBSW	70	OD_{24p3}	3V Switch Auxiliary Enable. Controls switching 3V standby supply.
BKFD_CUT	74	OD_{12p5}	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S3 sleep state.
LATCH_BKFD_CUT	70	O_{24p3}	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

4.12 Port 80 Message Display & LED Control

SYMBOL	PIN	I/O	DESCRIPTION
P1_DGH#	53	O_{24p3}	Common cathode output of high nibble display on decoded Port 1 (ex.: 0x80h) message. Switching frequency is about 10 KHz.
P1_DGH#	54	O_{24p3}	Common cathode output of high nibble display on decoded Port 1 (ex.: 0x80h) message. Switching frequency is about 10 KHz.
P1_DGL#	51	O_{24p3}	Common cathode output of low nibble display on decoded Port 1 (ex.: 0x80h) message. Switching frequency is about 10 KHz.
P1_DGL#	52	O_{24p3}	Common cathode output of low nibble display on decoded Port 1 (ex.: 0x80h) message. Switching frequency is about 10 KHz.
P2_DGH#	41	O_{24p3}	Common cathode output of high nibble display on decoded Port 2 message. Switching frequency is about 10 KHz.
P2_DGH#	42	O_{24p3}	Common cathode output of high nibble display on decoded Port 2 message. Switching frequency is about 10 KHz.
P2_DGL#	39	O_{24p3}	Common cathode output of low nibble display on decoded Port 2 message. Switching frequency is about 10 KHz.
P2_DGL#	40	O_{24p3}	Common cathode output of low nibble display on decoded Port 2 message. Switching frequency is about 10 KHz.
LED_A LED_B LED_C LED_D LED_E LED_F LED_G	43 44 45 47 48 49 50	O_{24p3}	Anode outputs for 7-Segment LED.
YLW_LED	38	OD_{12p5}	Yellow LED output control. This pin could indicate the power status.
GRN_LED	55	OD_{12p5}	Green LED output control. This pin could indicate the power status.

4.13 SMBus Interface

SYMBOL	PIN	I/O	DESCRIPTION
MSCL0	75	IN_{tsp5} OD_{12p5}	SMBus clock.
MSDA0	76	IN_{tsp5} OD_{12p5}	SMBus bi-directional Data.
MSCL1	128	IN_{tsp5} OD_{12p5}	SMBus clock.
MSDA1	123	IN_{tsp5} OD_{12p5}	SMBus bi-directional Data.

SYMBOL	PIN	I/O	DESCRIPTION
MSCL2	77	IN_{tp5} OD_{24p5}	SMBus clock.
MSDA2	78	IN_{tp5} OD_{24p5}	SMBus bi-directional Data.

4.14 USB

SYMBOL	PIN	I/O	DESCRIPTION
USB_D+	5	AOUT	USB PORT
USB_D-	6	AOUT	USB PORT

4.15 PORT80 to UART

SYMBOL	PIN	I/O	DESCRIPTION
SOUTA_P80	34	O_{12p3}	PORT80 serial output

4.16 IR

SYMBOL	PIN	I/O	DESCRIPTION
IRRX	11	IN_{tsp5}	IR Receiver input
IRTX	12	O_{12p3}	IR Transmitter output

4.17 SPI Switch Controller

SYMBOL	PIN	I/O	DESCRIPTION
CHPST_MOSI	48	IN_{tp5}	Chipset Data output
CHPST_SCK	50	IN_{tp5}	Chipset clock input
CHPST_MISO	52	O_{24p3}	Chipset Data input
CHPST_CS#	54	IN_{tp5}	Chipset select signal
USB_MISO	56	O_{12p3}	USB Data output
USB_CS#	57	O_{12p3}	USB select signal
USB_SCK	58	O_{12p3}	USB clock input
USB_MOSI	59	IN_{tsp5}	USB Data input
CSOUT#	47	O_{24p3}	Chipset select signal output

4.18 Advanced Sleep State Control

SYMBOL	PIN	I/O	DESCRIPTION

SYMBOL	PIN	I/O	DESCRIPTION
DEEP_S5_0	70	OD_{24p5}	This pin is to control system power for entering “more power saving mode”.

4.19 RTC Crystal Oscillator

SYMBOL	PIN	DESCRIPTION
RTC_XIN	71	RTC clocks Crystal Oscillator input
RTC_XOUT	72	RTC clocks Crystal Oscillator output

4.20 DDR4 Power Sequence

SYMBOL	PIN	I/O	DESCRIPTION
VPP_PG	107	I	DDR4 VPP power on sequence ok signal
VPP_EN	86	O	VPP Power Enable
VDDQ_EN	87	O	VDDQ Power Enable

4.21 AMD DDR4 Power Sequence

SYMBOL	PIN	I/O	DESCRIPTION
APU_VDDIO_SUS_EN	87	O	APU_VDDIO_SUS enable
APU_VPP_SUS_EN	86	O	APU_VPP_SUS enable

4.22 Strapping Pins

SYMBOL	PIN	DESCRIPTION
DDR4_EN	15	DDR4 Function (Strapped by VSB power) 0: Disable 1: Enable

<table>
<tr><th>SYMBOL</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>ESPI_EN</td><td>27</td><td>ESPI Function
(Strapped by VSB power)
0: Disable
1: Enable
<table>
<tr><td>ESPI_EN</td><td>LDRQ_L_SEL
CR24[7]</td><td>PIN18</td></tr>
<tr><td>1</td><td>x</td><td>ESPI_RESET#</td></tr>
<tr><td>0</td><td>0</td><td>GP10</td></tr>
<tr><td>0</td><td>1</td><td>LDRQ#</td></tr>
</table>
<table>
<tr><td>ESPI_EN</td><td>PIN19</td></tr>
<tr><td>1</td><td>ESPI_ALERT#</td></tr>
<tr><td>0</td><td>SERIRQ</td></tr>
</table>
<table>
<tr><td>ESPI_EN</td><td>PIN20~23</td></tr>
<tr><td>1</td><td>ESPI_IO[3:0]</td></tr>
<tr><td>0</td><td>LAD[3:0]</td></tr>
</table>
<table>
<tr><td>ESPI_EN</td><td>PIN25</td></tr>
<tr><td>1</td><td>ESPI_CS#</td></tr>
<tr><td>0</td><td>LFRAME#</td></tr>
</table>
<table>
<tr><td>ESPI_EN</td><td>PIN26</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>LRESET#</td></tr>
</table></td></tr>
<tr><td>2E_4E_SEL</td><td>31</td><td>SIO I/O address selection
(Strapped by LRESET#)
0: SIO I/O address is 2Eh/2Fh
1: SIO I/O address is 4Eh/4Fh</td></tr>
<tr><td>DIS_HWACPI</td><td>32</td><td>ACPI default value setting
(Strapped by VSB power)
0: Hardware ACPI could take over related signals
1: Hardware ACPI never take over related signals
Output “0” : Pin73, 79, 101
Output “z” : Pin60, 63, 65, 71, 77, 78, 81, 82</td></tr>
</table>

SYMBOL	PIN	DESCRIPTION
DSW_EN	92	DSW Function (Strapped by VSB power) 0: Disable 1: Enable
AMD_EN	96	AMD DDR4 (Strapped by VSB power) 0: Disable 1: Enable

4.23 Power Pins

SYMBOL	PIN	DESCRIPTION
VHIF	24	+1.8V / 3.3 V stand-by power supply for the digital circuits.
3VSB	46, 85	+3.3 V stand-by power supply for the digital circuits.
AVSB	108	+3.3 V stand-by power supply for the analog circuits.
VBAT	99	+3 V on-board battery for the digital circuits.
3VCC	1	+3.3 V power supply for driving 3 V on host interface.
AGND	117	Analog ground.
PAD_CAP	62	External Filter Capacitor 4.7u (for internal VSB 1.8V).
VTT	119	INTEL® CPU VTT power.
VSS	16, 94	Ground.

4.24 General Purpose I/O Port

4.24.1 GPIO-0 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO00	3	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 0 bit 0.
GPIO01	4	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 0 bit 1.
GPIO02	121	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 0 bit 2.
GPIO03	122	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 0 bit 3.

SYMBOL	PIN	I/O	DESCRIPTION
GPIO05	96	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 0 bit 5.

4.24.2 GPIO-1 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO10	18	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 1 bit 0.
GPIO11	27	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 1 bit 1.
GPIO12	28	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 1 bit 2.
GPIO13	55	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 1 bit 3.

4.24.3 GPIO-2 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO20	29	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 0.
GPIO21	30	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 1.
GPIO22	31	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 2.
GPIO23	32	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 3.
GPIO24	33	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 4.
GPIO25	34	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 5.

SYMBOL	PIN	I/O	DESCRIPTION
GPIO26	35	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 6.
GPIO27	36	IN_{tdp5} O_{12p3} OD_{12p5}	General-purpose I/O port 2 bit 7.

4.24.4 GPIO-3 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO30	38	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 3 bit 0.
GPIO31	39	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 1.
GPIO32	40	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 2.
GPIO33	41	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 3.
GPIO34	42	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 4.
GPIO35	43	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 5.
GPIO36	44	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 6.
GPIO37	45	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 3 bit 7.

4.24.5 GPIO-4 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO40	47	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 0.

SYMBOL	PIN	I/O	DESCRIPTION
GPIO41	48	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 1.
GPIO42	49	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 2.
GPIO43	50	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 3.
GPIO44	51	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 4.
GPIO45	52	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 5.
GPIO46	53	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 6.
GPIO47	54	IN_{tsp5} O_{24p3} OD_{24p5}	General-purpose I/O port 4 bit 7.

4.24.6 GPIO-5 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO50	7	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 0.
GPIO51	8	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 1.
GPIO52	9	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 2.
GPIO53	10	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 3.
GPIO54	11	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 4.

SYMBOL	PIN	I/O	DESCRIPTION
GPIO55	12	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 5.
GPIO56	13	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 6.
GPIO57	14	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 5 bit 7.

4.24.7 GPIO-6 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO62	76	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 6 bit 2.
GPIO63	75	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 6 bit 3.
GPIO66	70	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port 6 bit 6.
GPIO67	100	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port 6 bit 7.

4.24.8 GPIO-7 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO70	95	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 0.
GPIO71	98	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 1.
GPIO72	124	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 2.
GPIO73	125	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 3.

SYMBOL	PIN	I/O	DESCRIPTION
GPIO74	37	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 4.
GPIO75	128	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 5.
GPIO76	123	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 7 bit 6.
GPIO77	102	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port 7 bit 7.

4.24.9 GPIO-8 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO80	15	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 0.
GPIO81	126	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 1.
GPIO82	127	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 2.
GPIO83	103	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 3.
GPIO84	104	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 4.
GPIO85	2	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 5.
GPIO86	92	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 6.
GPIO87	118	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 8 bit 7.

4.24.1 GPIO-9 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPIO90	93	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 0.
GPIO91	90	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 1.
GPIO92	91	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 2.
GPIO93	89	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 3.
GPIO94	88	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 4.
GPIO95	74	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 5.
GPIO96	87	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 6.
GPIO97	86	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port 9 bit 7.

4.24.2 GPIO EN0 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPEN00	63	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 0.
GPEN01	64	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 1.
GPEN02	65	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 2.

SYMBOL	PIN	I/O	DESCRIPTION
GPEN03	60	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 3.
GPEN04	61	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port EN0 bit 4.
GPEN05	83	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 5.
GPEN06	84	IN_{tp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 6.

4.24.3 GPIO EN1 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GPEN10	80	IN_{tsp5} O_{12p3} OD_{12p5}	General-purpose I/O port EN0 bit 0.
GPEN11	79	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port EN0 bit 1.
GPEN12	78	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port EN0 bit 2.
GPEN13	77	IN_{tp5} O_{24p3} OD_{24p5}	General-purpose I/O port EN0 bit 3.
GPEN14	81	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port EN0 bit 4.
GPEN15	82	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port EN0 bit 5.
GPEN16	73	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port EN0 bit 6.
GPEN17	101	IN_{tp5} O_{8p3} OD_{8p5}	General-purpose I/O port EN0 bit 7.

4.25 Debug PORT Test

SYMBOL	PIN	I/O	DESCRIPTION
DB_RX	59	IN_{tsp5}	Serial data into MCU UART RX
DB_TX	57	O_{12p3}	Serial data from MCU UART TX
DB_SCK	58	IN_{tsp5}	Patch signal SCK
DB_SI	57	IN_{tsp5}	Patch signal SI
DB_SO	56	O_{12p3}	Patch signal SO
DB_SCE#	59	IN_{tsp5}	Patch signal SCE#
MCU_TCK	58	IN_{tsp5}	Debug Port MCU JTAG clock
MCU_TMS	59	IN_{tsp5}	Debug Port MCU JTAG mode select
MCU_TDO	57	O_{12p3}	Debug Port MCU JTAG data out
MCU_TDI	56	IN_{tsp5}	Debug Port MCU JTAG data in

4.26 DSW

SYMBOL	PIN	I/O	DESCRIPTION
PCHVSB	97	AIN	PCHVSB function
SUSWARN#	93	IN_{tp5}	This pin connects to SUSWARN# in CPT PCH
SUSACK#	91	OD_{12p5}	This pin connects to SUSACK# in CPT PCH
SLP_SUS#	89	IN_{tp5}	This pin connects to SLP_SUS# in CPT PCH
SLP_SUS_FET	88	OD_{12p5}	This pin connects to VSB power switch

4.27 Power Fault

SYMBOL	PIN	I/O	DESCRIPTION
PWR_FAULT#	118	OD_{12p5}	Power Fault output

4.28 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
GPIO					
GPIO20~GPIO27	29~36	3VSB	Pull-down	47.03KΩ	1

Note1. Programmable

5. GLUE LOGIC

5.1 ACPI Glue Logic

Table 5-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	84	SLP_S5# input.
RESETCON#	83	RESETCON# input signal. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
PWROK0	81	This pin generates the PWROK signals while 3VCC is present.
PWROK1	82	This pin generates the PWROK signals while 3VCC is present.
DPWROK	73	This pin generates the DPWROK# signals while 3VSB is present.
ATXPGD	80	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.
RSMRST#	101	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT6686D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

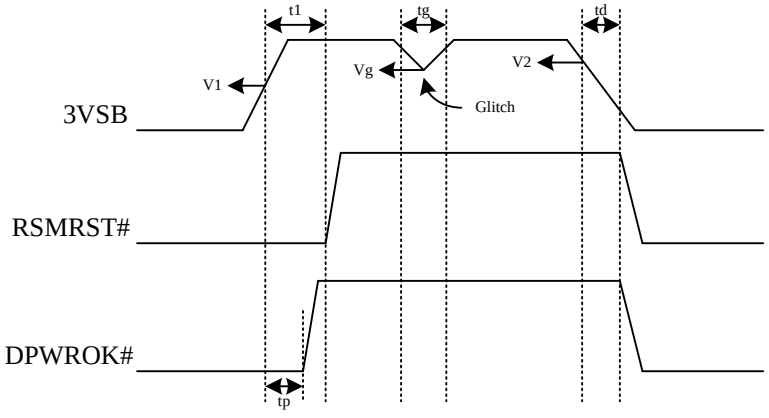


Figure 5-1 RSMRST# and DPWROK#

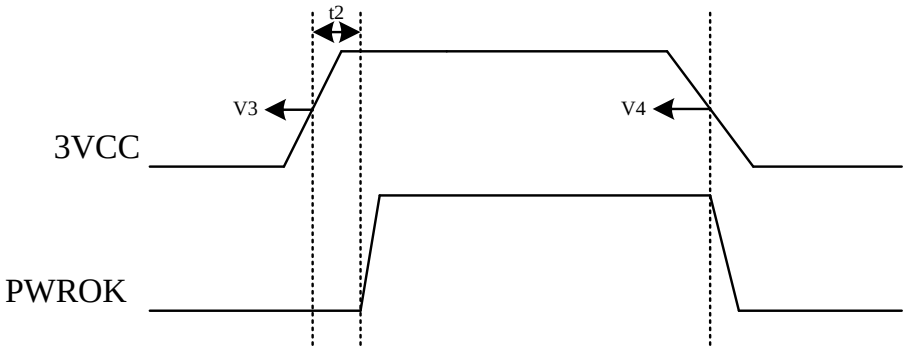


Figure 5-2 PWROK

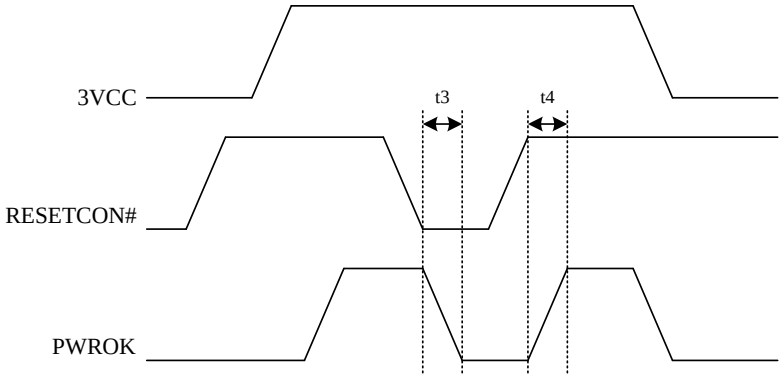


Figure 5-3 RESETCON# and PWROK (Default Disable)

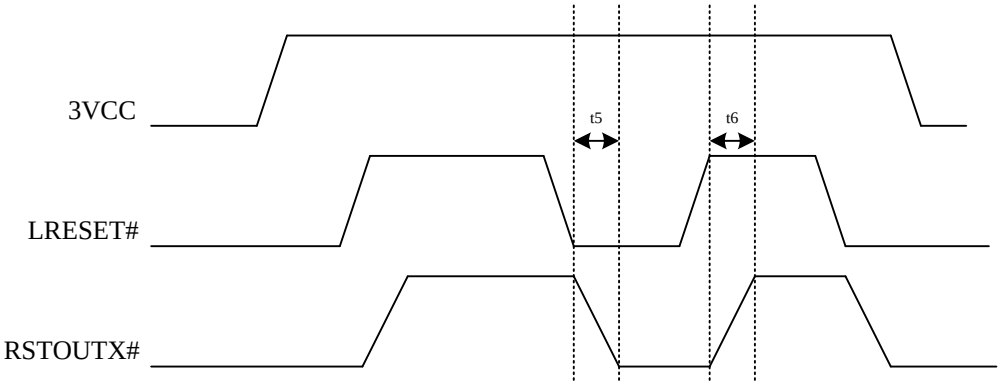


Figure 5-4 RSTOUTX# and LRESET#

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tp	Valid 3VSB to DPWROK# inactive	10	30	mS
tg	3VSB Glitch allowance		1	uS
td	Falling 3VSB supply Delay		1	uS

TIMING	PARAMETER	MIN	MAX	UNIT
t2	Valid 3VCC to PWROK active	300	500	mS
t3	RESETCON# active to PWROK inactive	0	80	nS
t4	RESETCON# inactive to PWROK active	0	80	nS
t5	LRESET# active to RSTOUTx# active	0	80	nS
t6	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	-	3.033	Volt
V2	3VSB Ineffective Voltage	2.882	-	Volt
V3	3VCC Valid Voltage	-	2.83	Volt
V4	3VCC Ineffective Voltage	2.68	-	Volt
Vg	3VSB drops by Power noise	2	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

5.2 BKFD_CUT and LATCHED_BF_CUT

NCT6686D supports BKFD_CUT and LATCHED_BF_CUT functions please refer the timing diagram below:

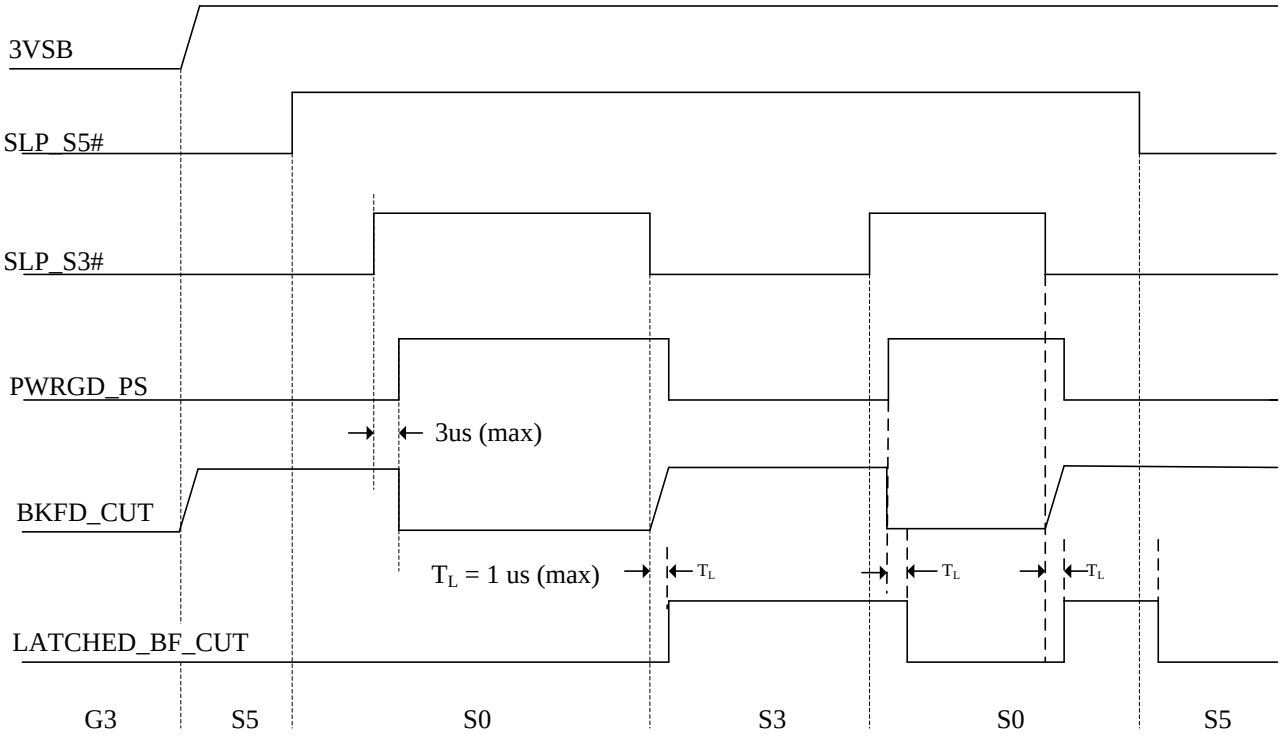


Figure 5-5 BKFD_CUT and LATCH_BKFD_CUT

BKFD_CUT (Backfeed_Cut) – When high, switches dual rails to standby power.

LATCH_BKFD_CUT (Latched_Backfeed_Cut) – When high, switches dual rails to standby power.

5.3 3VSBSW#

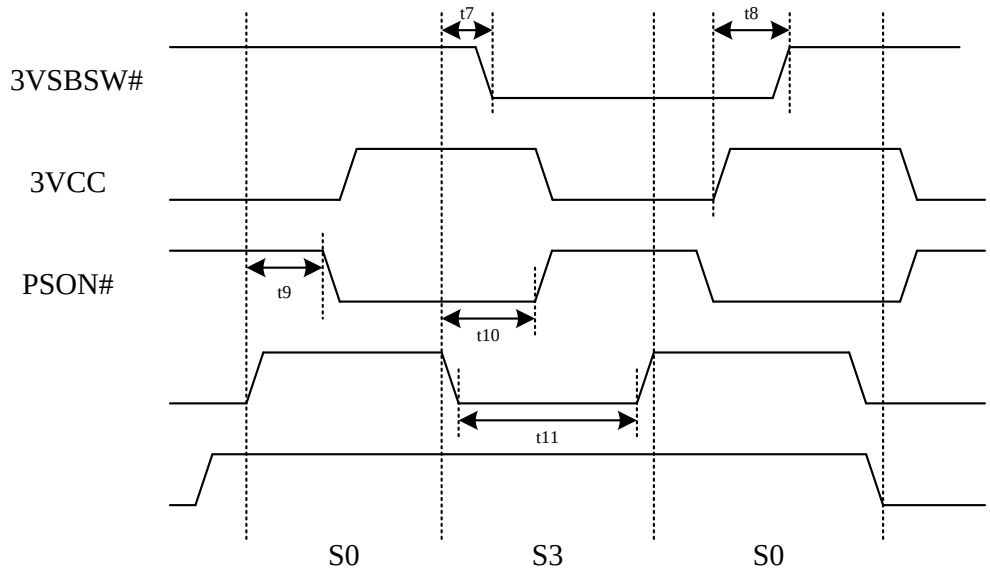


Figure 5-6 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t7	SLP_S3# active to 3VSBSW# active	0	10	mS
t8	3VCC active to 3VSBSW# inactive	120	190	mS
t9	SLP_S3# inactive to PSON# active	0	80	nS
t10	SLP_S3# active to PSON# inactive	15	45	mS
t11	SLP_S3# minimal Low Time	40	-	mS

5.4 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

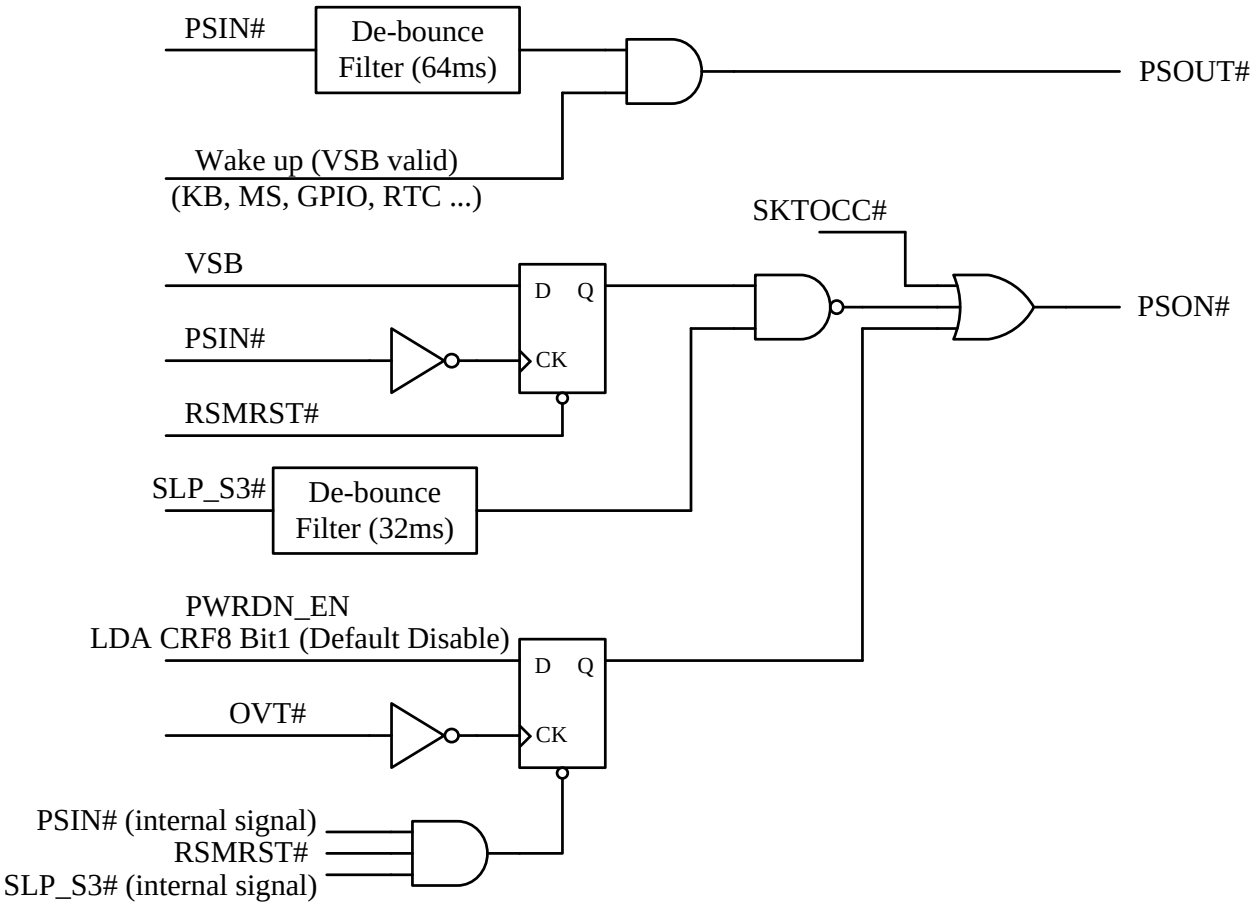


Figure 5-7 PSON# Block Diagram

5.5 DDR4PWR

DDR4PWR is the power sequence control of DDR4 SDRAM. It is a high speed and low power platform. There are two timer register can be select in the sequence (DDR4_VPP: LDF CREB bit[1:0], DDR4_VDDQ: LDF CREB bit[3:2]).Support Intel and AMD mode of DDR4 power sequence.

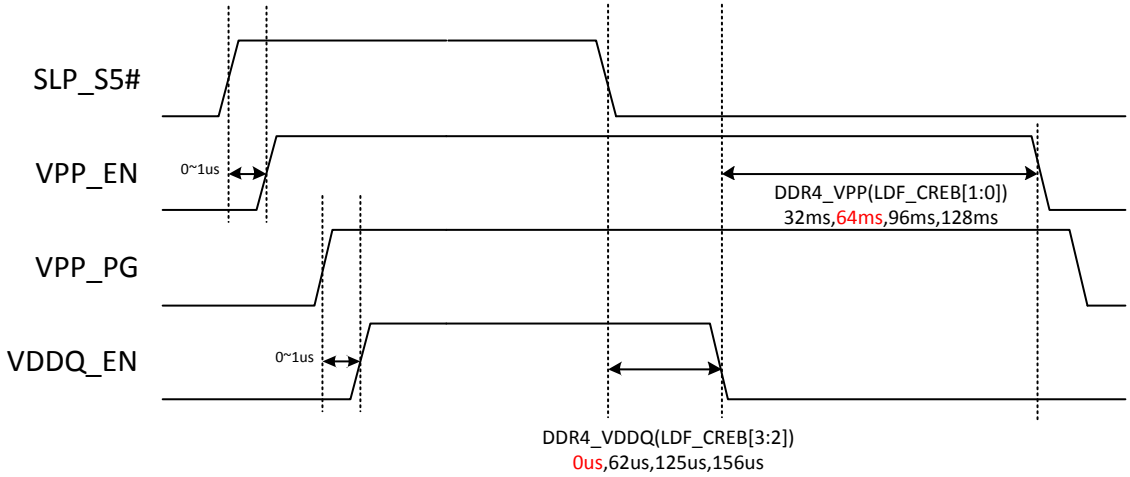


Figure 5-8 DDR4 PWR Intel mode

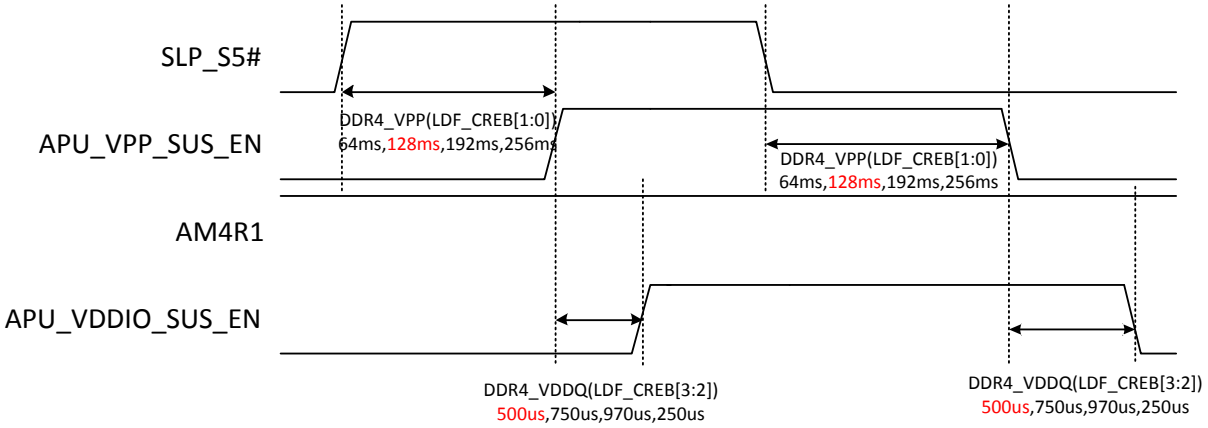


Figure 5-9 DDR4 PWR AMD mode

5.6 PWROK Block Diagram

The PWROK signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

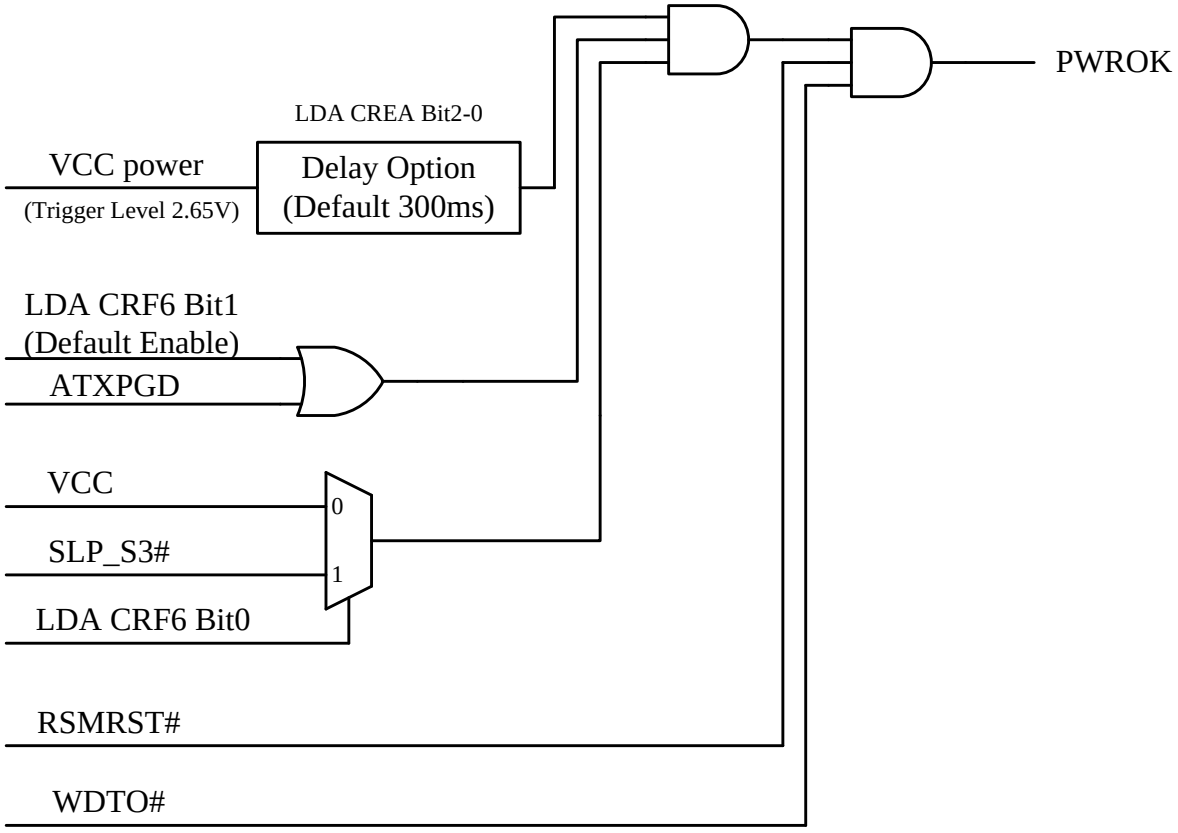


Figure 5-10 PWROK Block Diagram

5.7 Power Fault

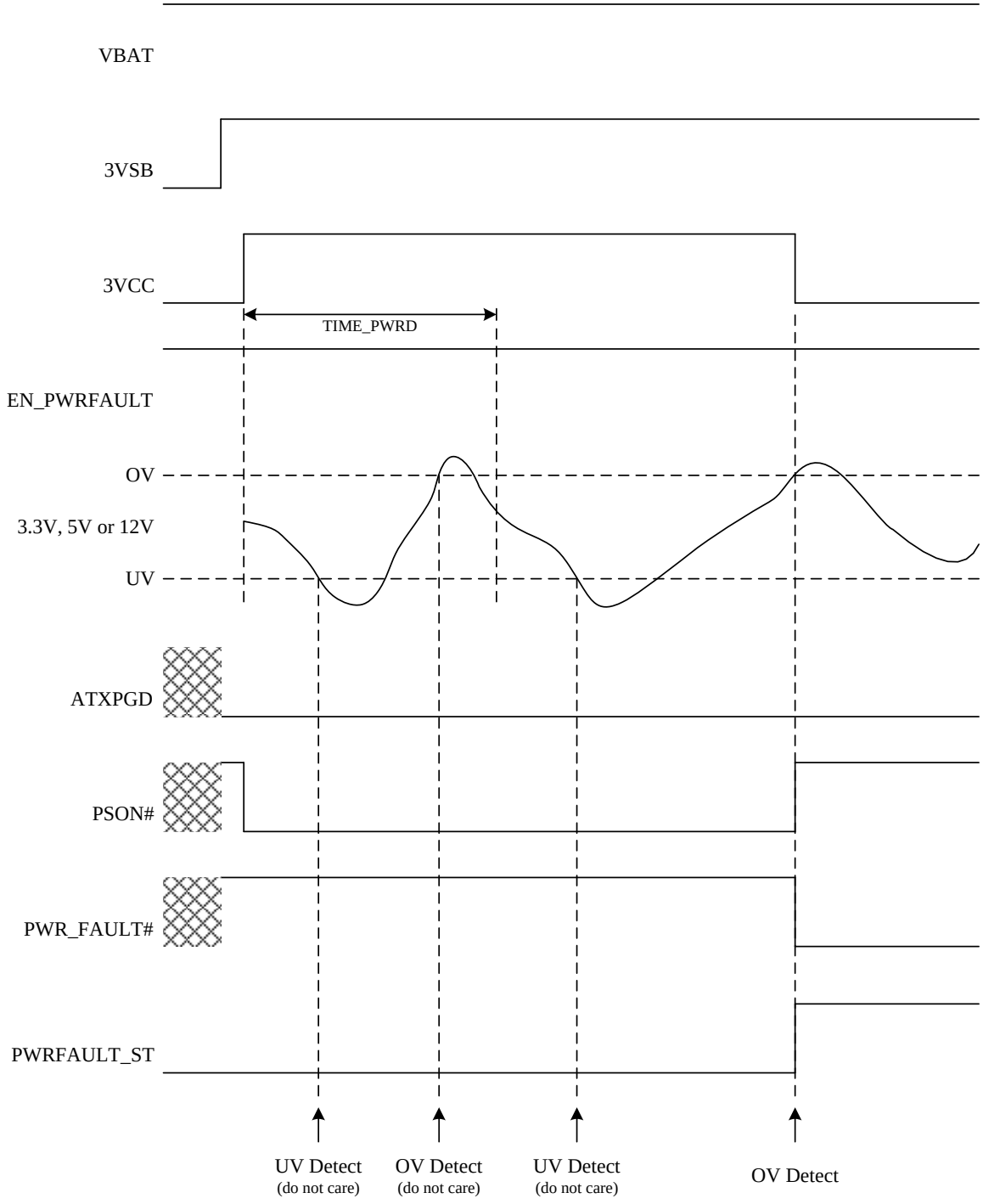


Figure 5-11 Power Fault (EN_PWRFAULT=0)

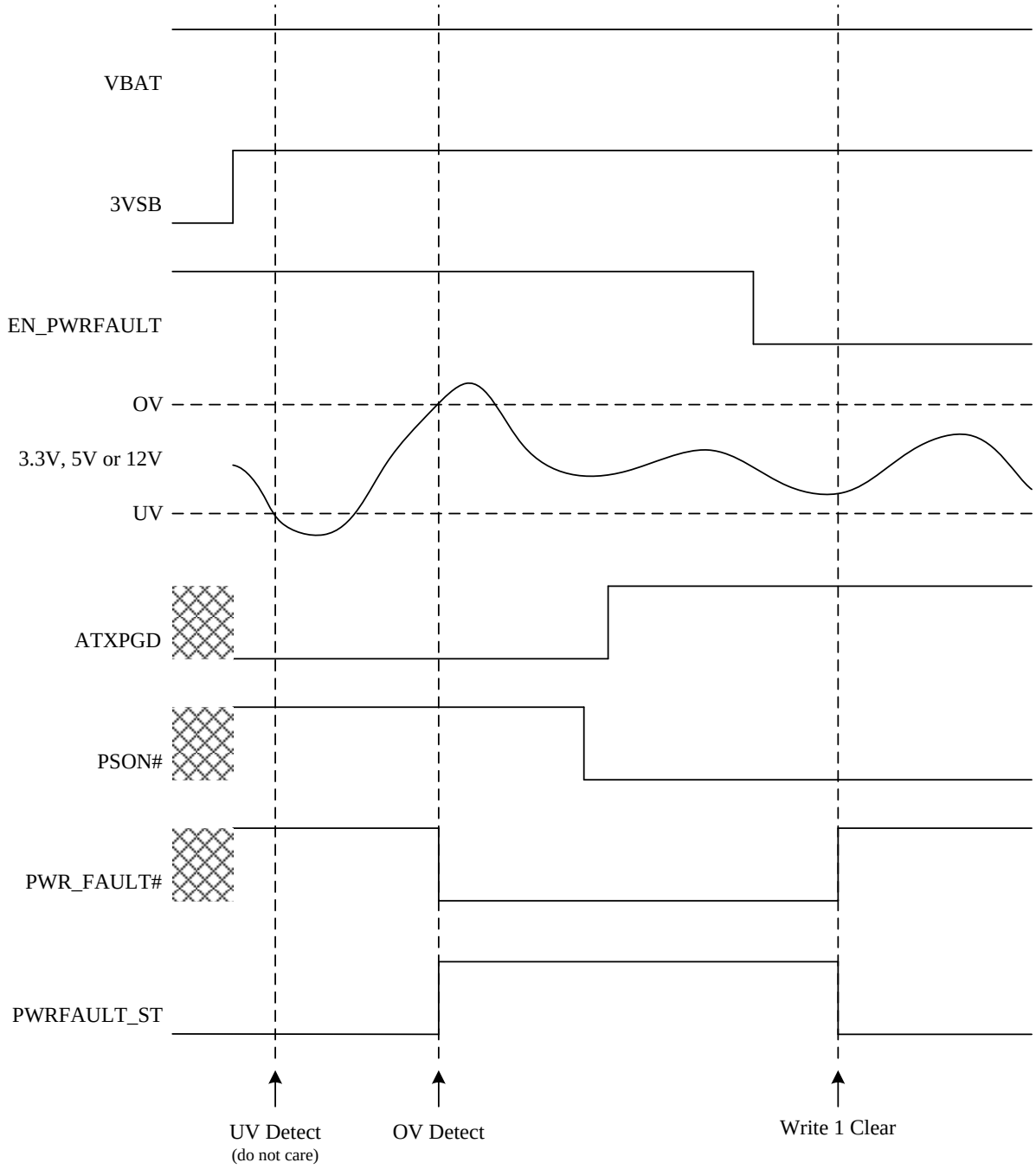


Figure 5-12 Power Fault (EN_PWRFAULT=1, ATXPGD=0, OV Detect)

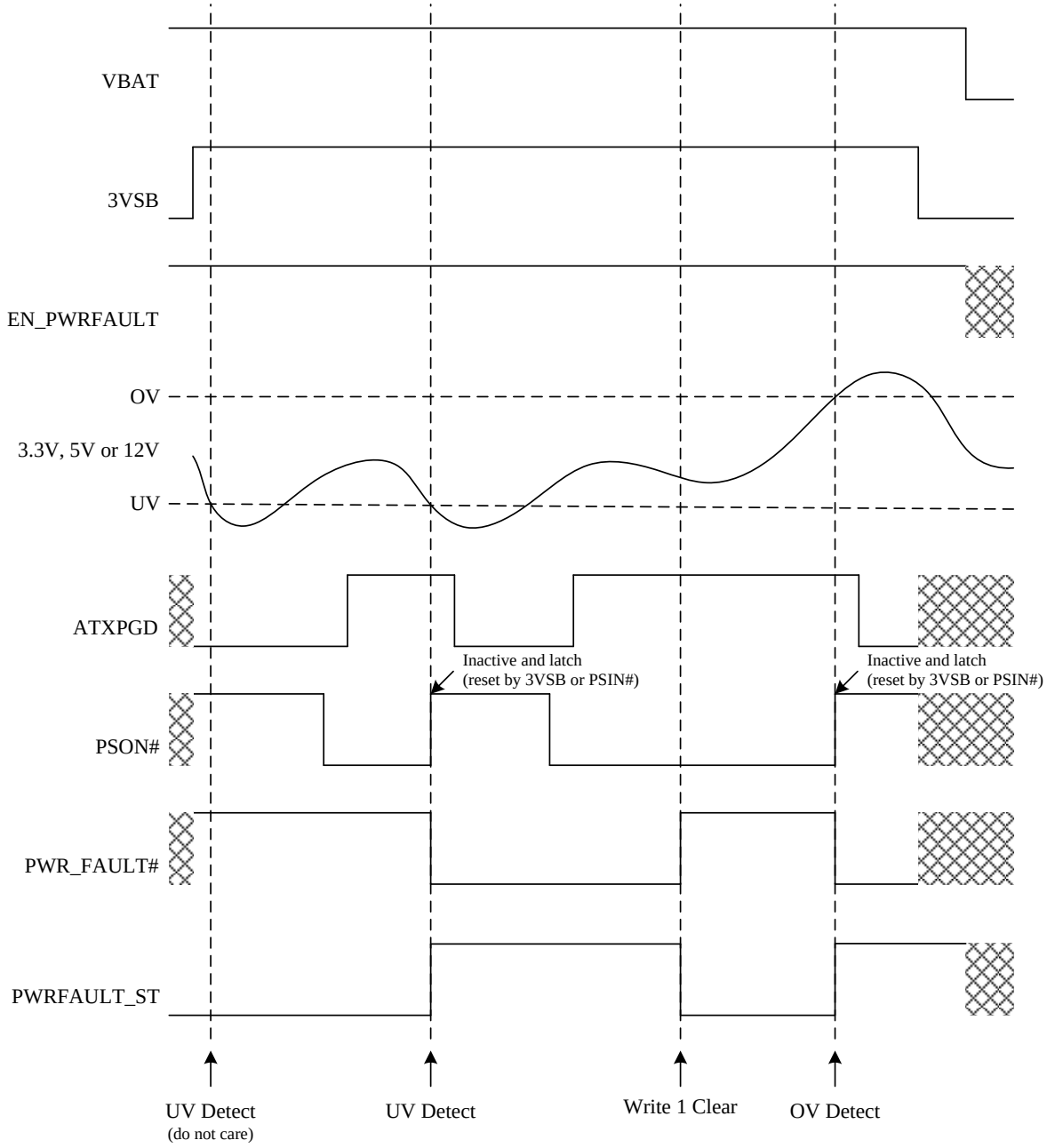


Figure 5-13 Power Fault (EN_PWRFAULT=1, ATXPGD=1, OV/UV Detect)

5.8 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device D CRE0h ~ CRE3h.

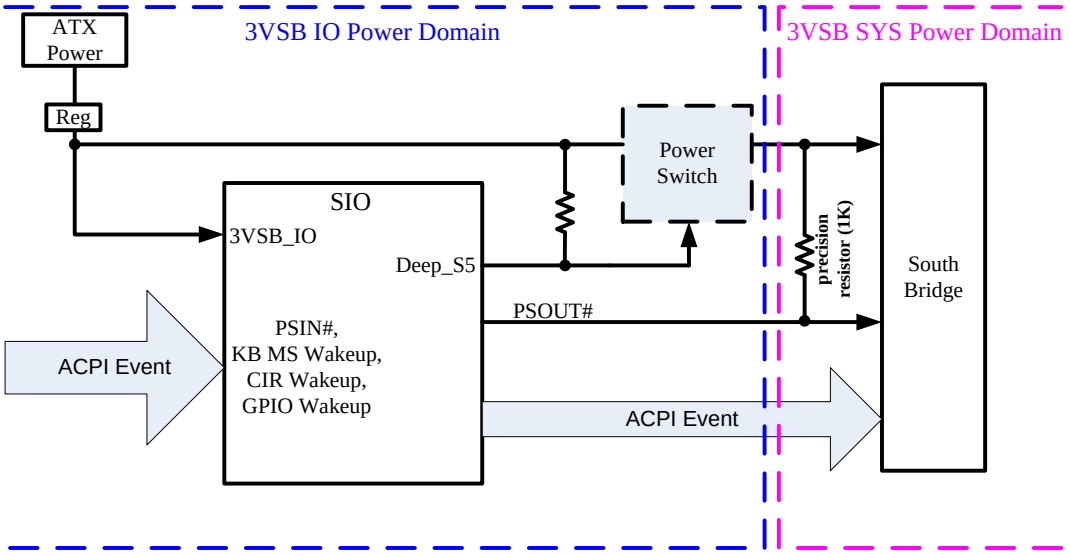
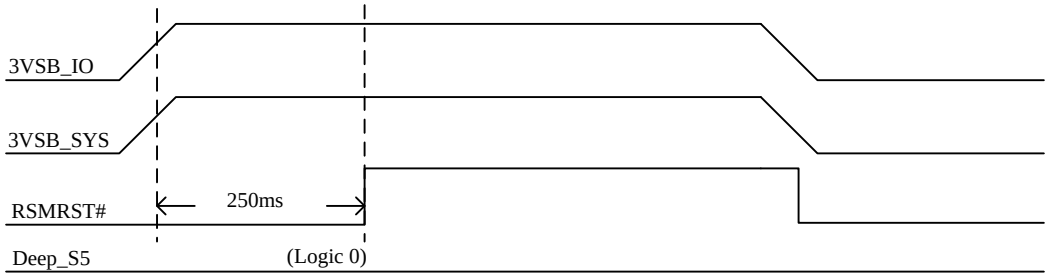


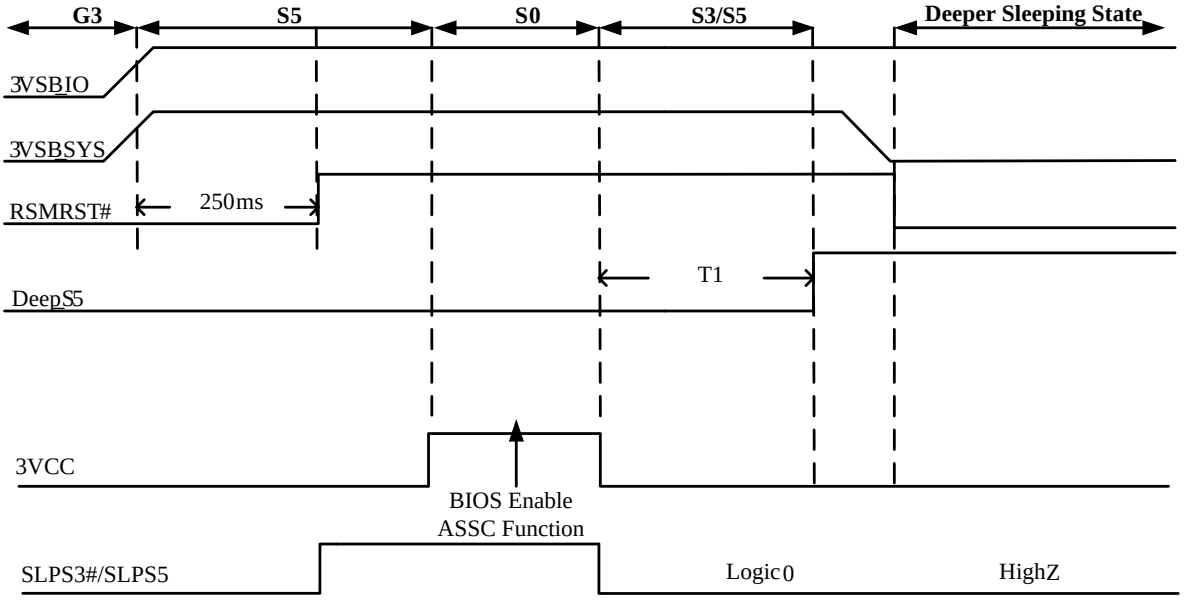
Figure 5-14 ASSC Application Diagram

5.8.1 When ASSC is disabled



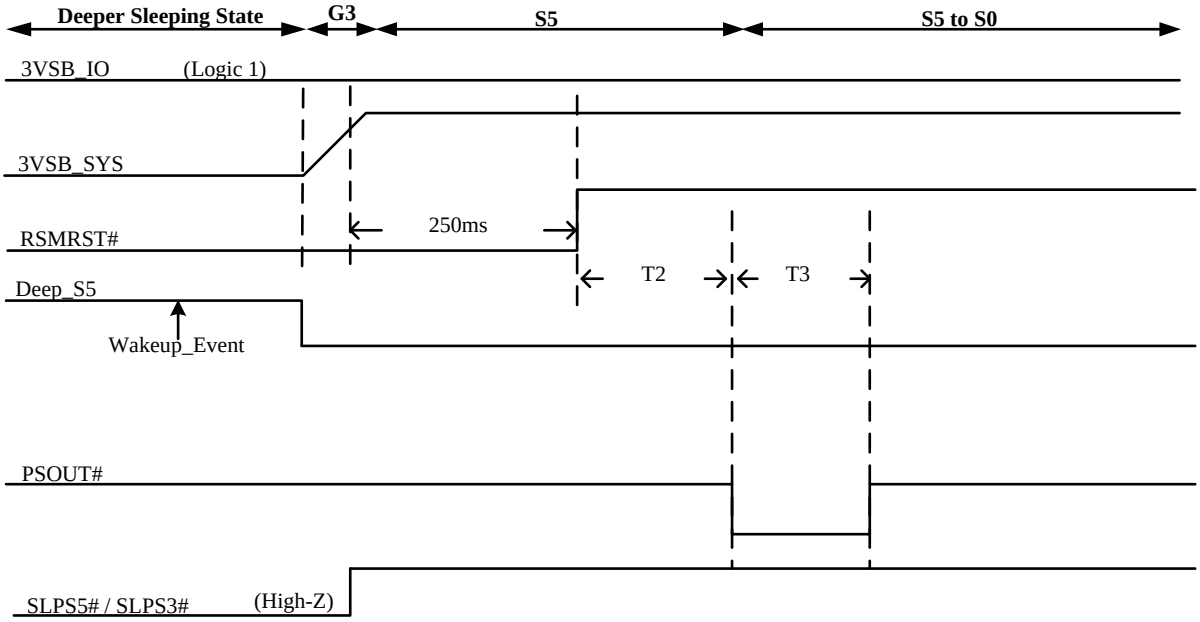
When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

5.8.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS3 or DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the "Deeper Sleeping State (DSS)" where system's VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

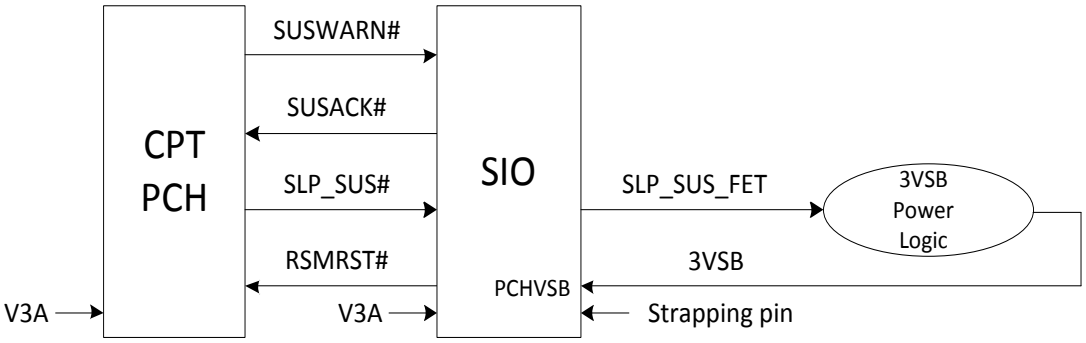
5.8.3 When ASSC is enabled (Exit Deeper Sleeping State)



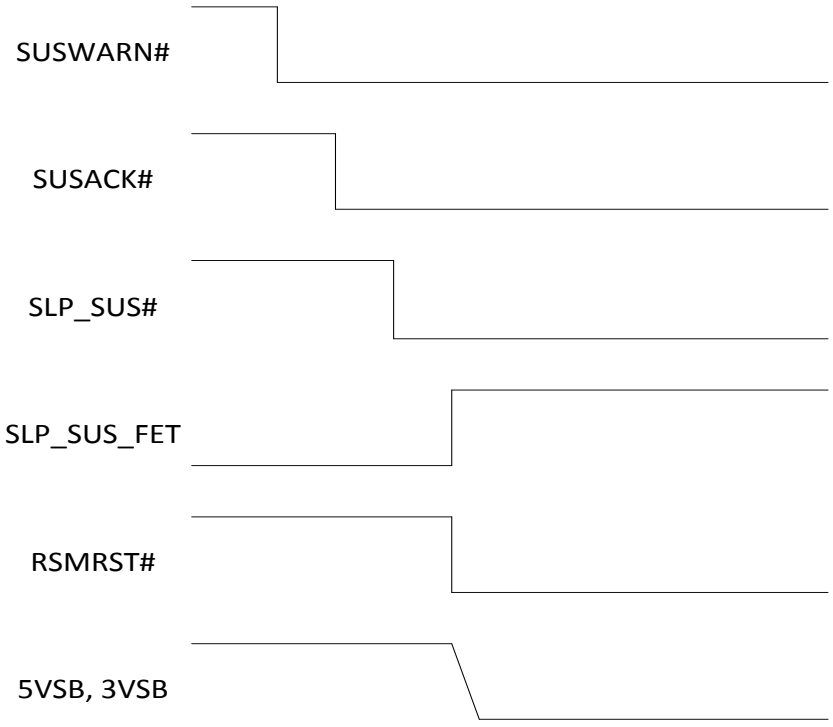
When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time (wakeup delay time, LD16 CRE0). The PSOUT# low pulse is

also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

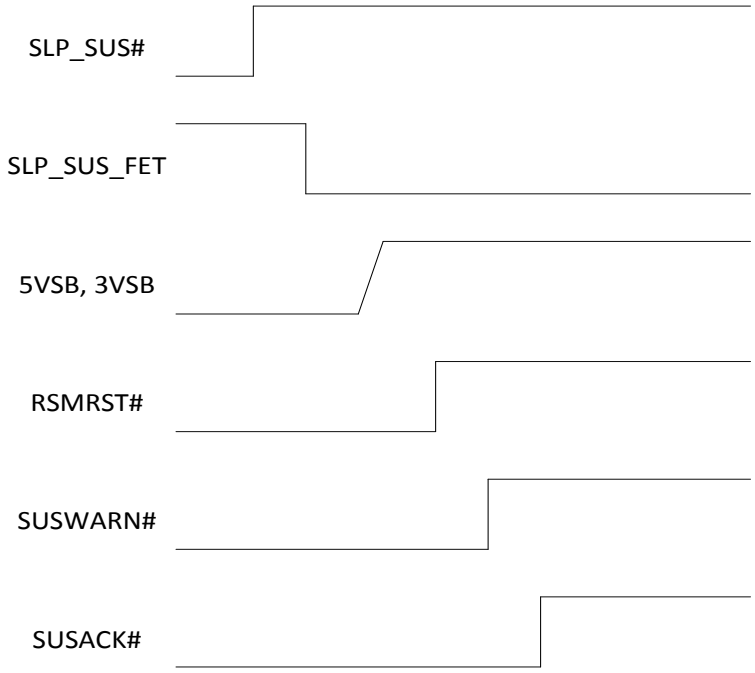
5.9 Intel DSW Function



5.9.1 Enter DSW State timing diagram

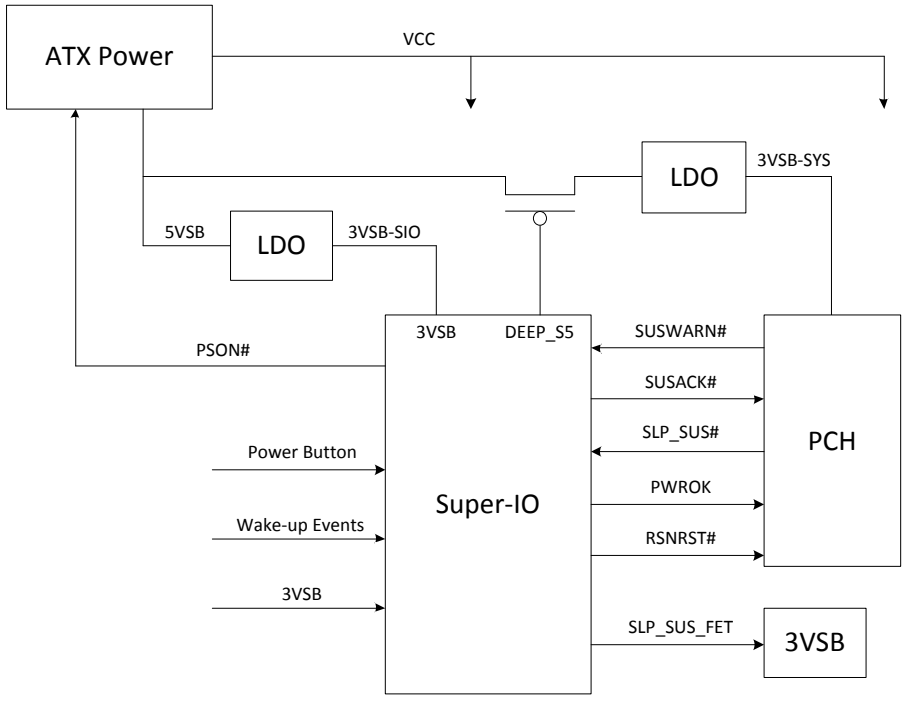


5.9.2 Exit DSW State timing diagram



5.9.3 Application Circuit

The NCT6686D can not only provide SIO Deep S5/S3 function, but Intel DSW function. The application circuit should follow the guide below:



5.10 SPI Switch Controller

The SPI Switch is enabled by embedded controller firmware.

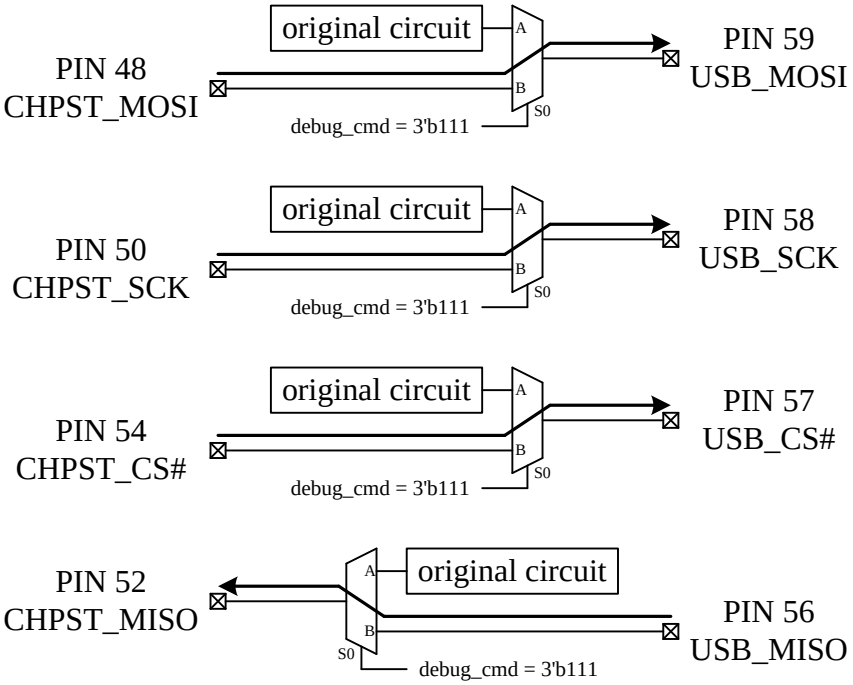


Figure 5-15 SPI Switch Controller (Mode I)

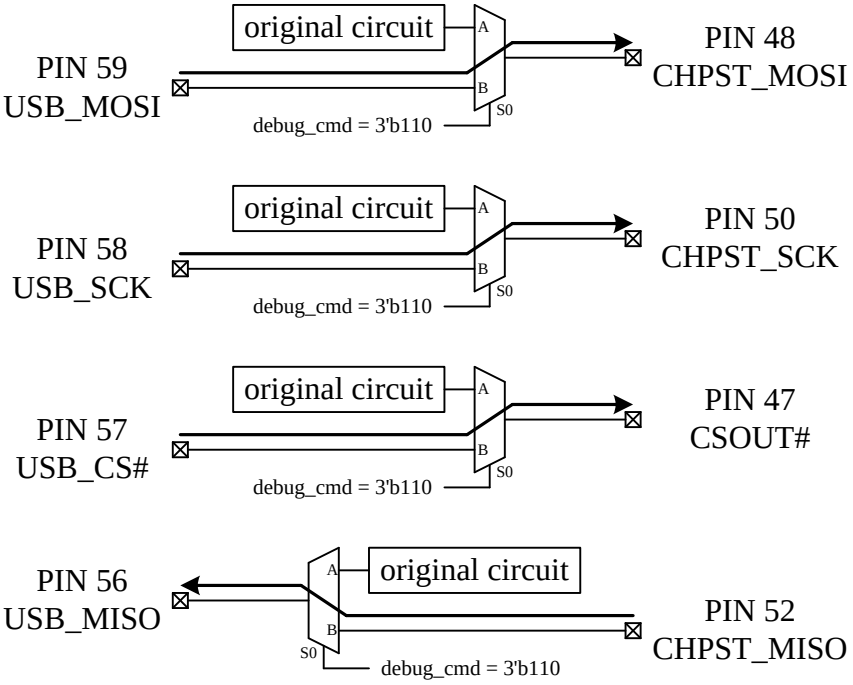


Figure 5-18 SPI Switch Controller (Mode II)

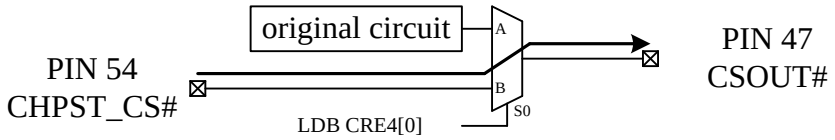


Figure 5-16 SPI Switch Controller (Mode III)

6. CONFIGURATION REGISTER ACCESS PROTOCOL

NCT6686D uses a special protocol to access configuration registers to set up different types of configurations. NCT6686D has a total of sixteen Logical Devices (from Logical Device 0 to Logical Device F with the exception of Logical Device 0, 4 and F for backward compatibility) corresponding to ten individual functions: Parallel Port (Logical Device 1), UART A (Logical Device 2), UARTB (Logical Device 3), Keyboard Controller (Logical Device 5), Consumer Infrared Remote (Logical Device 6), GPIO0~GPIO7 (Logical Device 7), PORT80 UART (Logical Device 8), GPIO8~9, GPIO0 Enhance, GPIO1 Enhance (Logical Device 9), ACPI (Logical Device A), EC Space (Logical Device B), RTC Timer (Logical Device C), Deep Sleep (Logical Device D), Fan Assign (Logical Device E).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. NCT6686D, then, maps the entire configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set by configuration register. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

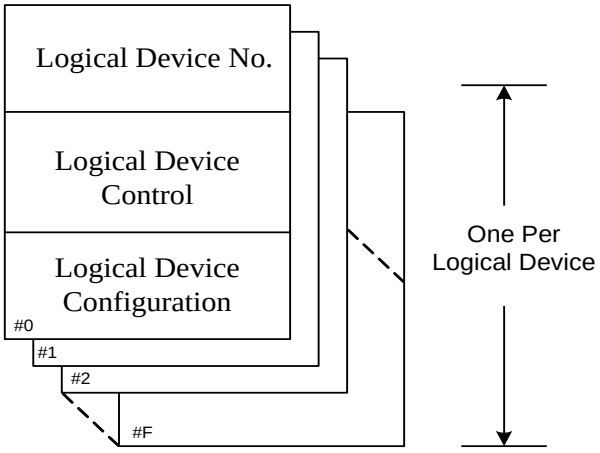


Figure 6-1 Structure of the Configuration Register

Table 6-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	Reserved	
1	Parallel Port	100h ~ FF8h
2	UARTA	100h ~ FF8h
3	UARTB	100h ~ FF8h
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	CIR	100h ~ FF8h
7	GPIO0~GPIO7	Reserved
8	PORT80 UART	Reserved
9	GPIO8~9, GPIO0 Enhance, GPIO1 Enhance	Reserved
A	ACPI	Reserved
B	EC Space (includes functions such as Hardware Monitor, CIR WAKE-UP, WDT, LED, ASF, PECI, TSI, SMBus Master, …)	100h ~ FF8h
C	RTC Timer	Reserved
D	Deep Sleep, Power Fault	Reserved
E	Fan Assign	Reserved
F	Reserved	

6.1 Configuration Sequence

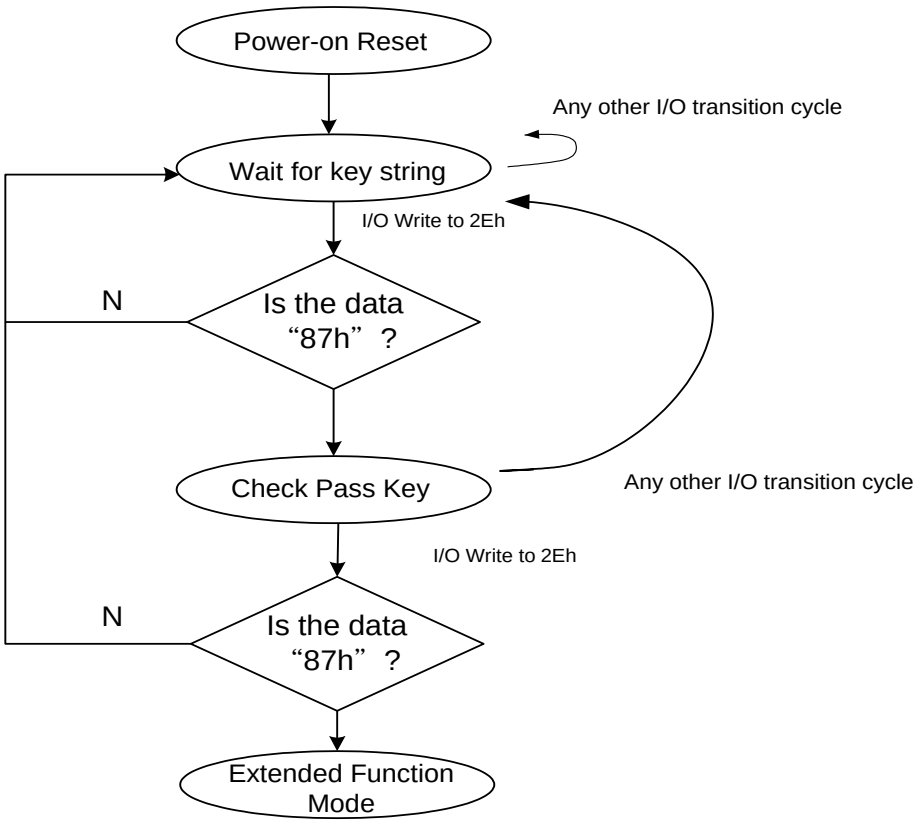


Figure 6-2 Configuration Register

To program NCT6686D configuration registers, the following configuration procedures must be in the followed sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

6.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh). Please see Global Register CR26 [Bit6].

6.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

6.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

6.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV     DX, 2EH
MOV     AL, 87H
OUT     DX, AL
OUT     DX, AL
;-------------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-------------------------------------------------------------------------------
MOV     DX, 2EH
MOV     AL, 07H
OUT     DX, AL          ; point to Logical Device Number Reg.
MOV     DX, 2FH
MOV     AL, 01H
OUT     DX, AL          ; select Logical Device 1
;
MOV     DX, 2EH
MOV     AL, F0H
OUT     DX, AL          ; select CRF0
MOV     DX, 2FH
MOV     AL, 3CH
OUT     DX, AL          ; update CRF0 with value 3CH
;-----------------------------------------------
; Exit the Extended Function Mode
;-----------------------------------------------
MOV     DX, 2EH
MOV     AL, AAH
OUT     DX, AL
```

Table 6-2 Chip (Global) Control Registers

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
07h	R/W	00h	Logical Device
10h	R/W	FFh	Device IRQ Type Selection
11h	R/W	FFh	Device IRQ Type Selection
13h	R/W	00h	Device IRQ Polarity Selection
14h	R/W	00h	Device IRQ Polarity Selection
15h	R/W	00h	Multi-function Pin Selection
1Ah	R/W	00h	Multi-function Pin Selection
1Bh	R/W	10	Multi-function Pin Selection
1Dh	R/W	00h	Test Mode
1E	R/W	00h	Multi-function Pin Selection
1F	R/W	00h	Multi-function Pin Selection
20h	Read Only	C7h	Chip ID, MSB
21h	Read Only	31h(3xh)	Chip ID, LSB
22h	R/W	00h	Device Power Down Option
23h	R/W	80h	Device Power Down Option
24h	R/W	E7h	Multi-function Pin Selection
25h	R/W	01h	Device Power Down Option
26h	R/W	00h	Global Option
27h	R/W	3Eh	Multi-function Pin Selection
28h	R/W	00h	Multi-function Pin Selection
29h	R/W	03h	Multi-function Pin Selection
2Ah	R/W	00h	Multi-function Pin Selection
2Bh	R/W	00h	Multi-function Pin Selection
2Ch	R/W	00h	Multi-function Pin Selection

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
2Dh	R/W	00h	Multi-function Pin Selection
2Eh	R/W	00h	Reserved
2Fh	R/W	SSh	Reserved.

S: Strapping; x: chip version.

7. EC SPACE

7.1 Features Implemented by Firmware

- ACPI power sequence controls and glue logics, such as RSMRST#, PSON#, PWROK, RSTOUT, PSIN#, PSOUT#, ATXPGD, SLP_S3#, SLP_S5#, …
  - --- Main Power good / power OK signals ATXPGD and internal power sensing.
  - --- Power distribution control (for switching between Main and Standby regulators)
  - --- Main power supply turn on (PSON#)
  - --- Resume reset (Master Reset) according to the stand-by 3V
  - --- Reset button de-bouncer
  - --- Power Good out mechanism using ATXPGD and internal power sensing
  - --- Buffers PCI_RESET to generate 3 reset output signals
- Power restoring policy when AC was recovered
- Advanced Deep Sleep Control logic to save more power during S3 / S5
  - --- Memory power switching support
  - --- Scheduling time slot to save more power when system sleeps
- Control logic to wake system up from normal / deep sleep state
- Advanced watch dog timers
- Hardware Monitoring (including voltage sources, analog / digital / virtual temperature sources, and tachometers)
- Customizable handling about SKTOCC#, CASEOPEN0#, CASEOPEN1# signals
- Facilities for modern digital sensor interface, such as PECI 3.0, DIMM temperature pushing back, DIMM Ambient Temperature writing back, Sandy Bridge PCH, SMBus sensors, and automatic polling engines …
- Smart fan control algorithms such as Thermal Cruise, Speed Cruise, Smart Fan 3, Smart Fan 4, DTS1.0 and DTS2.0 Control, and Smart Tracking for both Duty/RPM control
- Front Panel Power LED with different blinking patterns and fading effect
- Port 80 Message Buffering with / without 7-segment LED driving
- Up to 5 CIR keys to wake up system from sleep state
- OEM SMBus Slave Interface to allow hardware control from SMBus master such as BMC
- …

7.2 EC Space Register Set

The EC Space accommodates several functions featured by firmware, such as health management related functions, watchdog timers, PECI / SMBus masters, ACPI controls…This space is accessible via LPC I/O transactions. The I/O space allocated for this module is system dependent. 8 IO ports should be allocated.

- There are two ports begin from this base address. The first port is for BIOS/ACPI accessing and the second port is for application software accessing. Each port has INDEX and PAGE register for DATA register indirect access. A protection lock was provided to make sure synchronous access on registers. If it is enabled by mcu, the two port's PAGE register can be written if its value or writing data is 0xFF ; INDEX register can be written if PAGE register is not 0xFF and its value or writing data is 0xFF.

7.2.1 Page Port0 – Base Address0 + 0

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	PAGE0

7.2.2 Index Port0 – Base Address0 + 1

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	INDEX PORT0

7.2.3 Data Port0 – Base Address0 + 2

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	DATA0

7.2.4 Host Interface Event Register0 – Base Address0 + 3

Attribute: Read/Write
Power Well: VSB
Reset by: -
Default : -
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Host Interface Event Register0

** : it was mapped to EC Space register at Page 0, Index 28h, HIF_EVENT0

7.2.5 Page Port1 – Base Address0 + 4

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	PAGE1

7.2.6 Index Port1 – Base Address0 + 5

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	INDEX1

7.2.7 Data Port1 – Base Address0 + 6

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	DATA1

7.2.8 Host Interface Event Register1 – Base Address0 + 7

Attribute: Read/Write
Power Well: VSB
Reset by: -
Default : -
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Host Interface Event Register1

** : it was mapped to EC Space register at Page 0, Index 29h, HIF_EVENT1

7.3 Operations on EC Space

Please refer to NCT6686D EC Space Specification for details

8. ANALOG INPUTS

NOTICE: Interface for voltage, temperature, and fan speed monitoring were implemented and extended by firmware. About detailed implementation and interface registers for various hardware status monitoring such as PECI, PCH …, please refer to NCT6686D Family EC Space Datasheet. Here only the base hardware and application circuit for analog voltage / temperature monitoring were introduced.

The analog inputs of the hardware monitor block connect to an 7-bit Analog to Digital Converter (ADC) and 4 internal signals connected to the power supplies (AVSB, VBAT, 3VSB and 3VCC, with gain stage to double voltage range detected. Reading values of them are manipulated to have same base unit, 16mV, by firmware). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 16mV LSB (128 steps x 16mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

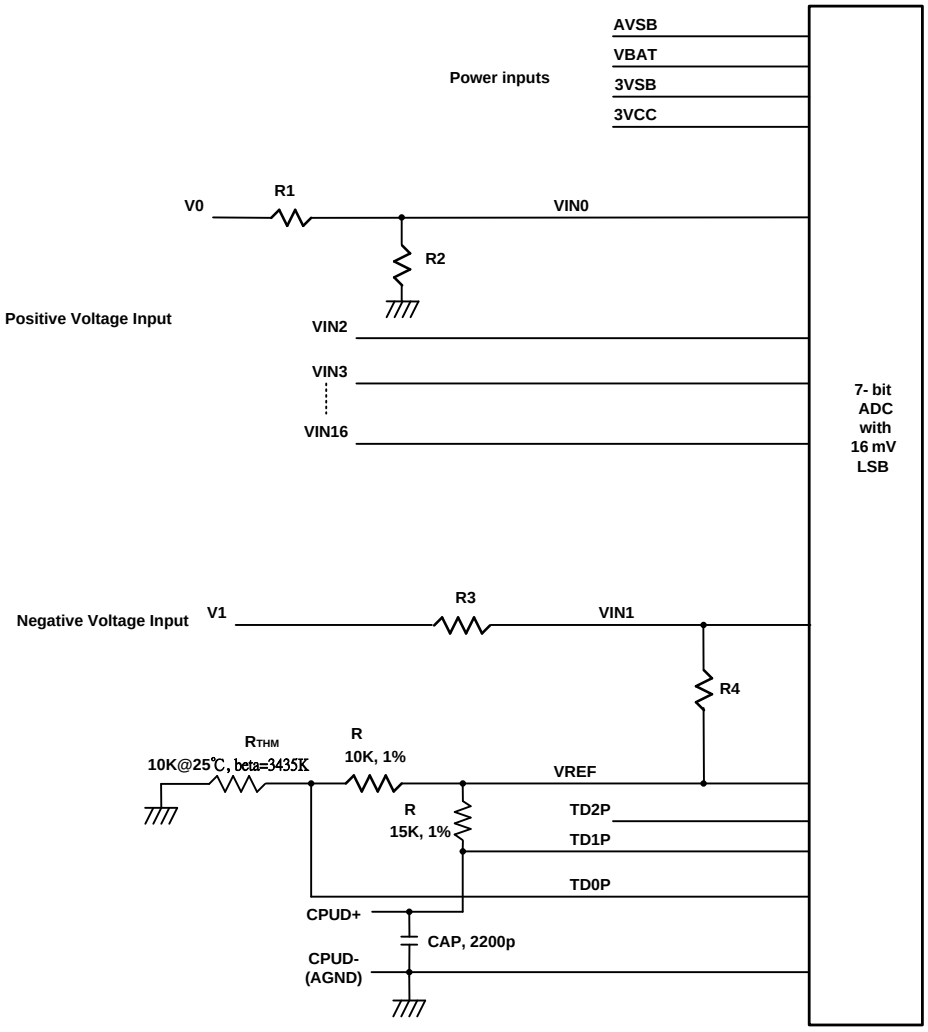


Figure 8-1 Analog Inputs and Application Circuit of the NCT6686D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 7-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVSB, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.2 Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF.

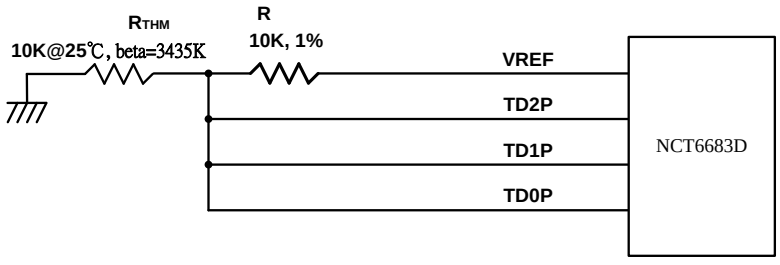


Figure 8-2 Monitoring Temperature from Thermistor

8.3 Monitor Temperature from Thermal Diode (Voltage Mode)

To monitor temperature of thermal diodes, the D- pins of thermal diodes are connected to AGND, and the D+ pins are connected to the temperature sensor pins (TD0P, TD1P, TD2P) of NCT6686D. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and a 2200-pF bypass capacitor is added to filter high-frequency noise.

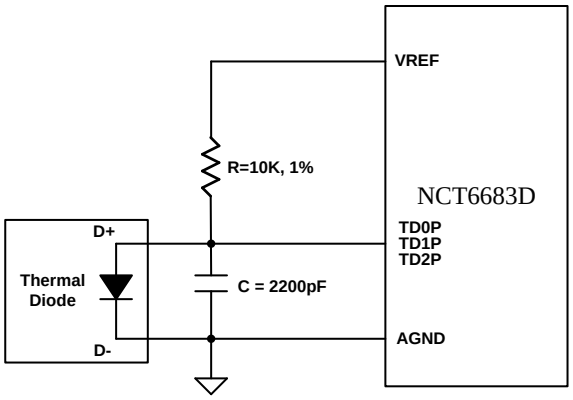


Figure 8-3 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.4 Monitor Temperature from Thermal Diode (Current Mode)

NCT6686D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

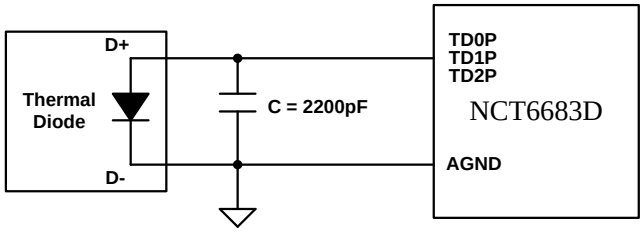


Figure 8-4 Monitoring Temperature from Thermal Diode (Current Mode)

To monitor temperature of thermal diodes through current mode operation, the D- pins of thermal diodes are connected to AGND and the D+ pins are connected to temperature sensor pins (TD0P, TD1P, TD2P) of NCT6686D. A bypass capacitor with C=2200pF should be added to filter the high frequency noise.

9. UART PORT

9.1.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits

DLS1	DLS0	DATA LENGTH
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 9-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

9.1.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

9.1.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**

4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

9.1.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

9.1.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

9.1.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION	
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.	
5-4	**RESERVED.**	
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of

1	**INTERRUPT STATUS BIT 0.**	the pending interrupt, as shown in the table below.
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

9.1.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**RESERVED.**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

9.1.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of

the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

9.1.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

10. PARALLEL PORT

10.1 Printer Interface Logic

The NCT6686D parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The NCT6686D supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 10-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN ATTRIBUTE	SPP	EPP	ECP
1	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	I	nACK	Intr	nACK, PeriphClk[2]
11	I	BUSY	nWait	BUSY, PeriphAck[2]
12	I	PE	PE	PEerror, nAckReverse[2]
13	I	SLCT	Select	SLCT, Xflag[2]
14	O	Nafd	nDStrb	nAFD, HostAck[2]
15	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN ATTRIBUTE	SPP
1	O	nSTB
2	I/O	PD0
3	I/O	PD1
4	I/O	PD2
5	I/O	PD3
6	I/O	PD4
7	I/O	PD5
8	I/O	PD6
9	I/O	PD7
10	I	nACK
11	I	BUSY
12	I	PE
13	I	SLCT
14	O	nAFD
15	I	nERR

HOST CONNECTOR	PIN ATTRIBUTE	SPP
16	O	nINIT
17	O	nSLIN

10.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 10-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 10-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

10.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

10.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	**RESERVED.**
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means hat no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

10.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED.** These two bits are always read as logical 1 and can be written.
5	**DIR (Direction Control Bit).** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

10.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

10.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

10.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
NWrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
NWait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

10.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

10.2.7.1. EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

10.2.7.2. EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

10.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the NCT6686D parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The NCT6686D ECP supports the following modes.

Table 10-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

10.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 10-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 10-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

10.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

10.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	PError	Select	nFault	1	1	1

BIT	DESCRIPTION
7	**nBusy.** This bit reflects the complement of the Busy input.
6	**nAck.** This bit reflects the nAck input.
5	**PError.** This bit reflects the PError input.
4	**Select.** This bit reflects the Select input.
3	**nFault.** This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

10.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**Reserved.** These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**nInit.** This bit is output to the INIT# output.
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

10.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

10.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

10.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

10.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

10.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION
7	**Compress.** This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.
6	**intrValue.** Returns the value on the ISA IRQ line to determine possible conflicts.
5	**IRQx2.** Reflects the IRQ resource assigned for ECP port.
4	**IRQx1.**
3	**IRQx0.**
2-0	**Reserved.** These three bits are logical 1 during a read and can be written.

cnfgB[5:3]	IRQ resource
000	Reflects other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

10.3.10 ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-5	**Mode.** Read/Write. These bits select the mode.

000	Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
010	Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.

BIT	DESCRIPTION	
	011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
	100	EPP Mode. EPP mode is activated if the EPP mode is selected.
	101	Reserved.
	110	Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.
	111	Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.
4	**nErrIntrEn.** Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.	
3	**dmaEn.** Read/Write. 0: Disable DMA unconditionally. 1: Enable DMA.	
2	**serviceIntr.** Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be rest to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.	
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.	
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.	

10.3.11ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
NStrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.

NAME	TYPE	DESCRIPTION
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

10.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

10.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

10.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

10.3.12.3. Data Compression

The NCT6686D hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

10.3.13 FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

10.3.14 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

10.3.15 Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

11. KEYBOARD CONTROLLER

The NCT6686D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

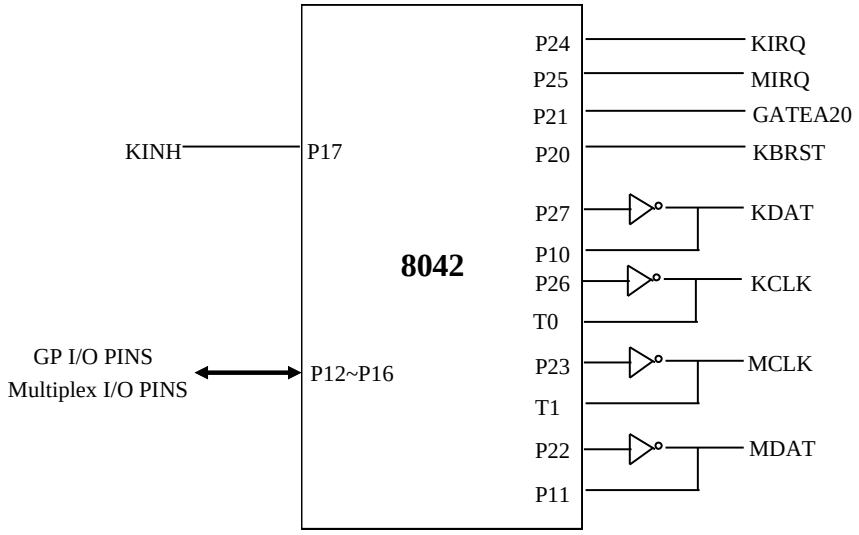


Figure 11-1 Keyboard and Mouse Interface

11.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

11.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

11.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 11-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

11.4 Commands

Table 11-2 KBC Command Sets

COMMAND	FUNCTION
20h	Read Command Byte of Keyboard Controller
60h	Write Command Byte of Keyboard Controller BIT / BIT DEFINITION 7 Reserved 6 IBM Keyboard Translate Mode 5 Disable Auxiliary Device 4 Disable Keyboard 3 Reserve 2 System Flag 1 Enable Auxiliary Interrupt 0 Enable Keyboard Interrupt
A4h	Test Password Returns 0Fah if Password is loaded Returns 0F1h if Password is not loaded

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>ABh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port (P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into the STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into the STATUS register</td></tr>
<tr><td>D0h</td><td>Send Port 2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set / reset GateA20 line based on system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from the Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Auxiliary Device</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Auxiliary Device</td></tr>
<tr><td>E0h</td><td>Reports the status of the test inputs</td></tr>
<tr><td>FXh</td><td>Pulse only RC (the reset line) low for 6µs if the Command byte is even</td></tr>
</table>

11.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

11.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved. 0 1: Reserved. 1 0: KBC clock input is 12 MHz. 1 1: Reserved.
6	**KCLKS0.**	
5-3	**RESERVED.**	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

11.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RES. (0)**
5	**RES. (1)**
4-3	**RES. (0)**
2	**RES. (1)**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high.

	0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

12. POWER MANAGEMENT EVENT

The PME# signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

Four registers in the NCT6686D are associated with the PME function. The four registers are divided into PME status registers and PME interrupt registers of wake-up events [Note.1].

1) The PME status registers of wake-up event:
   - At ACPI interface base address +0, +1, +2, and +3h register
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At ACPI interface base address +4, +5, +6, and +7h register
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the NCT6686D supports include:

- Mouse IRQ event*
- Keyboard IRQ event*
- Printer IRQ event
- Floppy IRQ event
- UART A/B IRQ event
- CIR IRQ event*
- Hardware Monitor / EC Space IRQ event
- RIB (UARTB Ring Indicator) event

Note.2 All the events above support waking system from S1 state. Events with the "*" mark could also support S3 and S5 states if MCU firmware is customized for this.

12.1 System Wakeup Control (SWC)

12.1.1 OVERVIEW

The SWC function block receives external events from system and internal events from internal functional modules. Based on these events, the SWC generates power management event (PME)/system control interrupt (SCI) and system management interrupt (SMI). These signals can also be directed to serial IRQ or MCU interrupt event.

The SWC receives the following external events:

- 16 genera purpose I/O enhance port (GPEN00 – GPEN07, GPEN10 – GPEN17).

The SWC receives the following internal events:

- PRT, UARTA, UARTB, KBC, CIR, GPIO, HM and EC port0/1/2 functional block interrupt events.
- HM SCI event.
- MCU general purpose events.

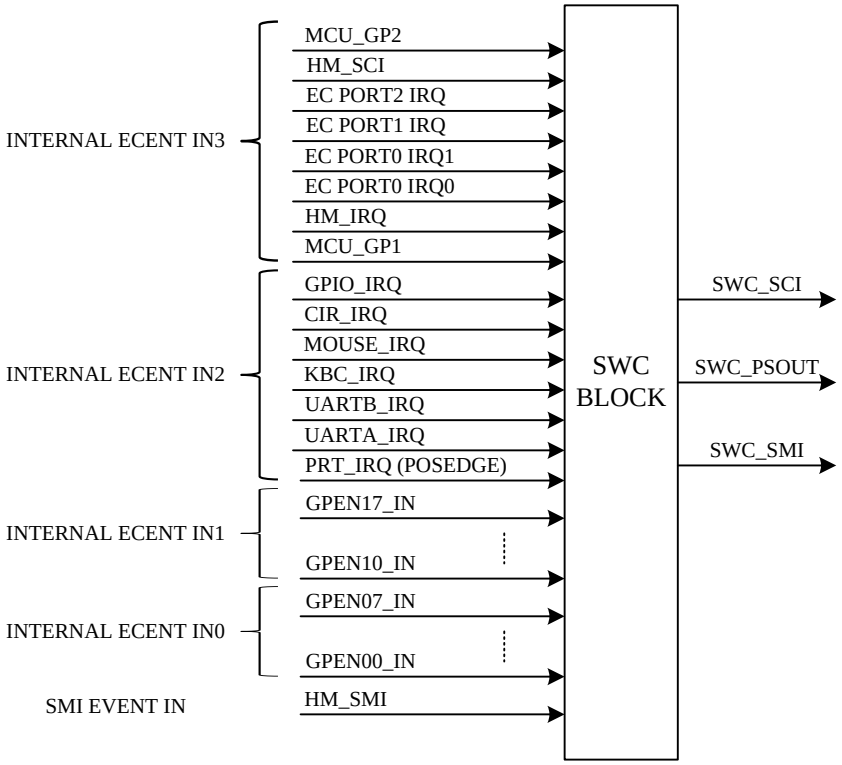


Figure 12-1SWC Block Connection

The SWC outputs SWC_SCI, SWC_SMI and SWC_PSOUT signal.

- SWC_SCI is connected to PME# function pin and it can generate SCI/PME event to system. It can be route to serial IRQ and MCU module to generate interrupt event if its related register enabled.
- SWC_PSOUT is connected to MCU module and it can generate interrupt event to MCU. It informs MCU to generate PSOUT event.
- SWC_SMI is connected to SMI#/OVT# function pin and it can generate SMI#/OVT# event to system. It can be route to serial IRQ channel 2 and MCU module to generate interrupt event if its related register enabled.

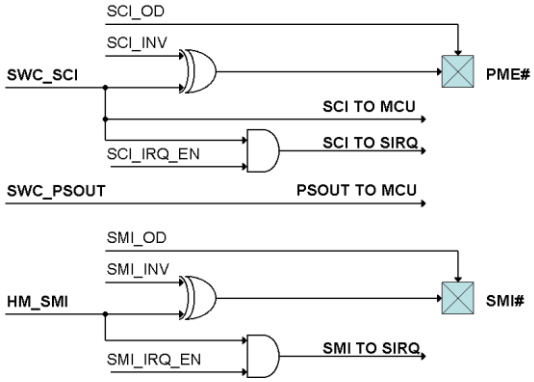


Figure 12-2 SWC signal routing path

12.1.2 Function Description

The SWC function is based on *ACPI Specification Revision3.0 September2, 2004* general-purpose event register blocks. The SWC has an EVENT register group, EVENT_EN/EVENT_STS, to support 16 external events and 16 internal events.

NCT6686D supports two system wakeup signals, PSOUT# and PME#. Each wakeup event input can only be routed to one of them by SCI_PSOUT_ROUTE. System can access two different register groups GPE_EN/GPE_STS and PSOUT_EN/PSOUT_STS in order to separate PSOUT and GPE events.

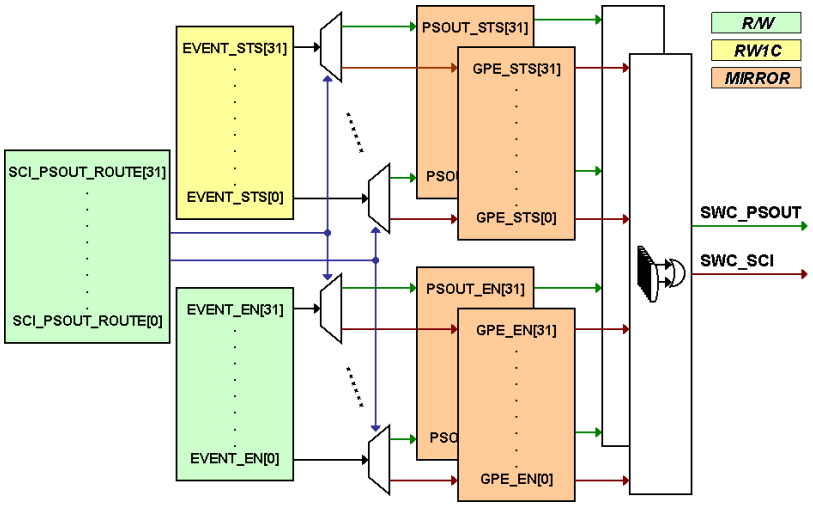


Figure 12-3 SWC registers block diagram

12.1.2.1. External Events

The SWC function receives 16 external GPEN (GPEN17-10, GPEN07-00) inputs as level high active event. Each GPEN function pin has its programmable parity and de-bounces time. After setting GPEN function pin multiplex, parity and de-bounces time, write 1 to its status bit to clear its status event.

12.1.2.2. Internal Events

The SWC function receives 3 kinds of internal event, internal device's IRQ, HM SCI and MCU general purpose event.

- Internal device's IRQ: SWC function receives 13 internal device's IRQ as event input. UARTA, UARTB, KBC, MOUSE, CIR, GPIO, HM and EC PORT0/12 IRQ are level high active event. PRT IRQ signal is edge high-active event.
- HM SCI and MCU general purpose event: They are generated by firmware operation. It includes KBC/Mouse wakeup, CIR wakeup, PSIN, UARTA/B RI#, GPIO input event or others firmware wakeup event.

12.1.2.3. Waken up by Keyboard events

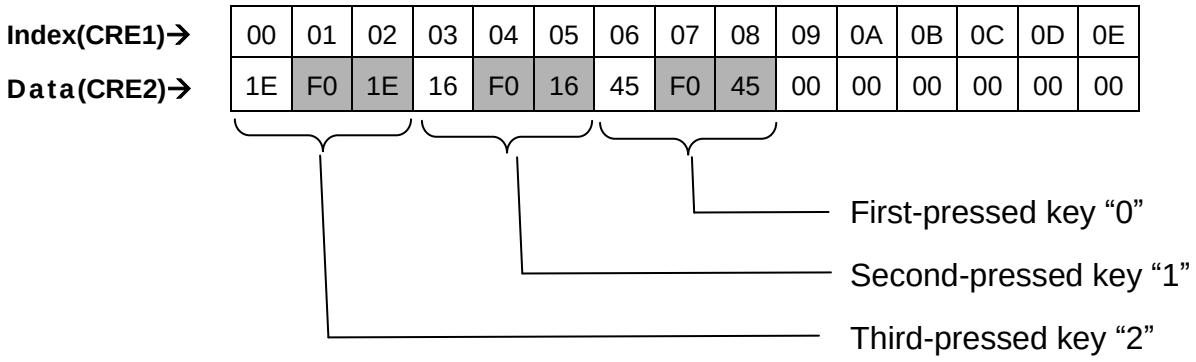
To enable the keyboard Wake-Up function, corresponding function in EC Space register should be initialized by BIOS first, and then BIOS should set "KBC IRQ GPE enable" (and "KBC IRQ PSOUT enable", if the wakeup signal was to be routed to PSOUT), and clear the corresponding status flags (write 1 to corresponding bit locations).

There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to "1" (Default).
2) Specific keys (Password) - Set bit 0 at Logical Device A, CR[E0h] to "0".

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of “0” is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.



12.1.2.4. Waken up by Mouse events

To enable the keyboard Wake-Up function, corresponding function in EC Space register should be initialized by BIOS first, and then BIOS should set “MOUSE IRQ GPE enable” (and “MOUSE IRQ PSOUT enable”, if the wakeup signal was to be routed to PSOUT), and clear the corresponding status flags (write 1 to corresponding bit locations).

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 12-1 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

12.1.3 Registers

NOTICE :

1. GPEN, EC Ports, and MCU general purpose events are internal resources of MCU. Almost all of these registers are controlled by MCU. Please follow programming guide when implementing functions covered in this chapter (e.g. wake up system from sleep state by keyboard) .
2. All XXX Status registers were active only when corresponding XXX Enable registers were enabled.

12.1.3.1. General Purpose Event Status 0 – Base Address + 0

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	GPEN07 GPE status
6	RW1C	GPEN06 GPE status
5	RW1C	GPEN05 GPE status
4	RW1C	GPEN04 GPE status
3	RW1C	GPEN03 GPE status
2	RW1C	GPEN02 GPE status
1	RW1C	GPEN01 GPE status
0	RW1C	GPEN00 GPE status

12.1.3.2. General Purpose Event Status 1 – Base Address + 1

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	GPEN17 GPE status

BIT	READ / WRITE	DESCRIPTION
6	RW1C	GPEN16 GPE status
5	RW1C	GPEN15 GPE status
4	RW1C	GPEN14 GPE status
3	RW1C	GPEN13 GPE status
2	RW1C	GPEN12 GPE status
1	RW1C	GPEN11 GPE status
0	RW1C	GPEN10 GPE status

12.1.3.3. General Purpose Event Status 2 – Base Address + 2

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	GPIO IRQ GPE status. Controlled by EC
6	RW1C	CIR IRQ GPE status
5	RW1C	MOUSE IRQ GPE status
4	RW1C	KBC IRQ GPE status
3	RW1C	UARTB IRQ GPE status
2	RW1C	UARTA IRQ GPE status
1	RW1C	PRT IRQ positive-edge GPE status
0	Reserved	

12.1.3.4. General Purpose Event Status 3 – Base Address + 3

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	MCU general purpose event 0 GPE status
6	RW1C	HM SCI GPE status
5	RW1C	EC PORT2 IRQ GPE status
4	RW1C	EC PORT1 IRQ GPE status
3	RW1C	EC PORT0 IRQ1 GPE status
2	RW1C	EC PORT0 IRQ0 GPE status
1	RW1C	HM IRQ GPE status

BIT	READ / WRITE	DESCRIPTION
0	RW1C	MCU general purpose event 1 GPE status

12.1.3.5. General Purpose Event Enable 0 – Base Address + 4

Attribute: RW
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPEN07 GPE enable
6	R / W	GPEN06 GPE enable
5	R / W	GPEN05 GPE enable
4	R / W	GPEN04 GPE enable
3	R / W	GPEN03 GPE enable
2	R / W	GPEN02 GPE enable
1	R / W	GPEN01 GPE enable
0	R / W	GPEN00 GPE enable

12.1.3.6. General Purpose Event Enable 1 – Base Address + 5

Attribute: RW
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPEN17 GPE enable
6	R / W	GPEN16 GPE enable
5	R / W	GPEN15 GPE enable
4	R / W	GPEN14 GPE enable
3	R / W	GPEN13 GPE enable
2	R / W	GPEN12 GPE enable
1	R / W	GPEN11 GPE enable
0	R / W	GPEN10 GPE enable

12.1.3.7. General Purpose Event Enable 2 – Base Address + 6

Attribute: RW
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO IRQ GPE enable. Controlled by EC
6	R / W	CIR IRQ GPE enable
5	R / W	MOUSE IRQ GPE enable
4	R / W	KBC IRQ GPE enable
3	R / W	UARTB IRQ GPE enable
2	R / W	UARTA IRQ GPE enable
1	R / W	PRT IRQ positive-edge GPE enable
0	Reserved	

12.1.3.8. General Purpose Event Enable 3 – Base Address + 7

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	MCU general purpose event 0 GPE enable
6	RW1C	HM SCI GPE enable
5	RW1C	EC PORT2 IRQ GPE enable
4	RW1C	EC PORT1 IRQ GPE enable
3	RW1C	EC PORT0 IRQ1 GPE enable
2	RW1C	EC PORT0 IRQ0 GPE enable
1	RW1C	HM IRQ GPE enable
0	RW1C	MCU general purpose event 1 GPE enable

12.1.3.9. PSOUT Status 0 – Base Address + 8

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	GPEN07 PSOUT status
6	RW1C	GPEN06 PSOUT status
5	RW1C	GPEN05 PSOUT status
4	RW1C	GPEN04 PSOUT status
3	RW1C	GPEN03 PSOUT status
2	RW1C	GPEN02 PSOUT status

BIT	READ / WRITE	DESCRIPTION
1	RW1C	GPEN01 PSOUT status
0	RW1C	GPEN00 PSOUT status

12.1.3.10. PSOUT Status 1 – Base Address + 9

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	GPEN17 PSOUT status
6	RW1C	GPEN16 PSOUT status
5	RW1C	GPEN15 PSOUT status
4	RW1C	GPEN14 PSOUT status
3	RW1C	GPEN13 PSOUT status
2	RW1C	GPEN12 PSOUT status
1	RW1C	GPEN11 PSOUT status
0	RW1C	GPEN10 PSOUT status

12.1.3.11. PSOUT Status 2 – Base Address + 10

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	GPIO IRQ PSOUT status. Controlled by EC
6	RW1C	CIR IRQ PSOUT status
5	RW1C	MOUSE IRQ PSOUT status
4	RW1C	KBC IRQ PSOUT status
3	RW1C	UARTB IRQ PSOUT status
2	RW1C	UARTA IRQ PSOUT status
1	RW1C	PRT IRQ positive-edge PSOUT status
0	Reserved	

12.1.3.12. PSOUT Status 3 – Base Address + 11

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #

Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	MCU general purpose event 0 PSOUT status
6	RW1C	HM SCI PSOUT status
5	RW1C	EC PORT2 IRQ PSOUT status
4	RW1C	EC PORT1 IRQ PSOUT status
3	RW1C	EC PORT0 IRQ1 PSOUT status
2	RW1C	EC PORT0 IRQ0 PSOUT status
1	RW1C	HM IRQ PSOUT status
0	RW1C	MCU general purpose event 1 PSOUT status

12.1.3.13. PSOUT Enable 0 – Base Address + 12

Attribute: RW
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPEN07 PSOUT enable
6	R / W	GPEN06 PSOUT enable
5	R / W	GPEN05 PSOUT enable
4	R / W	GPEN04 PSOUT enable
3	R / W	GPEN03 PSOUT enable
2	R / W	GPEN02 PSOUT enable
1	R / W	GPEN01 PSOUT enable
0	R / W	GPEN00 PSOUT enable

12.1.3.14. PSOUT Enable 1 – Base Address + 13

Attribute: RW
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPEN17 PSOUT enable
6	R / W	GPEN16 PSOUT enable
5	R / W	GPEN15 PSOUT enable
4	R / W	GPEN14 PSOUT enable

BIT	READ / WRITE	DESCRIPTION
3	R / W	GPEN13 PSOUT enable
2	R / W	GPEN12 PSOUT enable
1	R / W	GPEN11 PSOUT enable
0	R / W	GPEN10 PSOUT enable

12.1.3.15. PSOUT Enable 2 – Base Address + 14

Attribute: RW
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO IRQ PSOUT enable. Controlled by EC
6	R / W	CIR IRQ PSOUT enable
5	R / W	MOUSE IRQ PSOUT enable
4	R / W	KBC IRQ PSOUT enable
3	R / W	UARTB IRQ PSOUT enable
2	R / W	UARTA IRQ PSOUT enable
1	R / W	PRT IRQ positive-edge PSOUT enable
0	Reserved	

12.1.3.16. PSOUT Enable 3 – Base Address + 15

Attribute: RW1C
Power Well: VSB
Reset by: RSMRST #
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	RW1C	MCU general purpose event 0 PSOUT enable
6	RW1C	HM SCI PSOUT enable
5	RW1C	EC PORT2 IRQ PSOUT enable
4	RW1C	EC PORT1 IRQ PSOUT enable
3	RW1C	EC PORT0 IRQ1 PSOUT enable
2	RW1C	EC PORT0 IRQ0 PSOUT enable
1	RW1C	HM IRQ PSOUT enable
0	RW1C	MCU general purpose event 1 PSOUT enable

13. SERIALIZED IRQ

The NCT6686D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

13.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT6686D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT6686D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

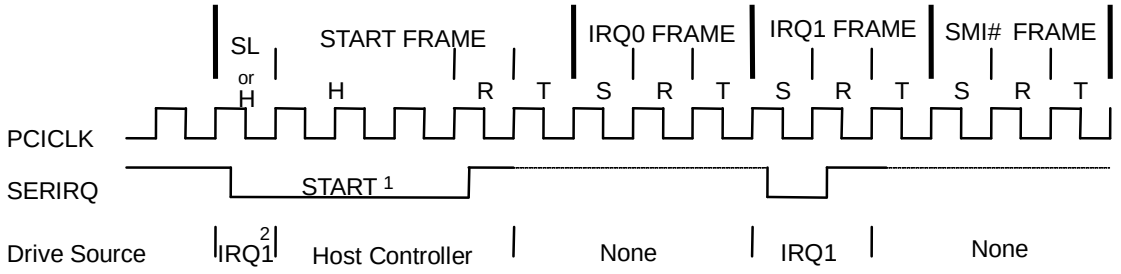


Figure 13-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. 1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT6686D because IRQ1 of the NCT6686D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

13.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT6686D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT6686D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT6686D device drives the SERIRQ high. During the Turn-around phase, the NCT6686D device leaves the SERIRQ tri-stated. The NCT6686D starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 13.1.

Table 13-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	UART B
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	-
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

13.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

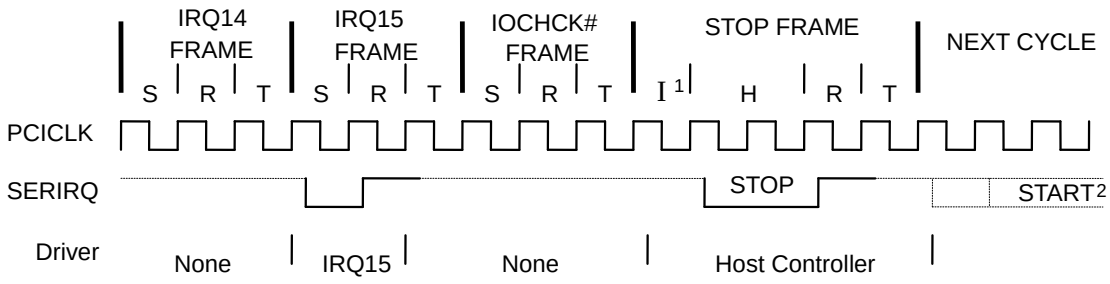


Figure 13-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

14. CONSUMER INFRARED REMOTE (CIR)

NOTICE : Wakeup-related functions by CIR were implemented in EC Space. Please refer to NCT6686D Family EC Space Datasheet about this topic.

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of H Level and L Level. The results are saved/stored in 32*8 RX FIFO. The max widths of H Level and L Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

As for the transmission, the user has to set up the Carrier frequency and the transmission mode first and then writes the widths of H Level and L Level via TX FIFO. The hardware will add Carrier to H Level according to the transmission mode.

14.1 CIR Register Table

Table 14-1 CIR Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	loopback_en	WIREN	TXEN	RXEN	WRXINV	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+2	IREN	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+3	RXFCONT	RXFIFO Count							
base+4	CP	MODE	Reserved						Carrier Prescalar
base+5	CC	Carrier Period							
base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	TXFIFOCLR	R	Tx Trigger Level		RXFIFOCLR	R	Rx Trigger Level	
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
base+A	SRXFIFO	Sample RX FIFO							
base+B	TXFCONT	TX FIFO Count							
base+C	STXFIFO	Sample TX FIFO							
base+D	FCCH	Frame Carrier Count High Byte							
base+E	FCCL	Frame Carrier Count Low Byte							
base+F	IRFSM	R	Decoder FSM			R	Encoder FSM		

14.1.1.1. IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	WIREN	TXEN	RXEN	WRXINV	RXINV	Sample Period Select	
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**Wide-band IR Enable**
5	**TX Enable** 1: Transmission Enable. After confirming that FIFO is not empty, the transmission starts (the hardware will wait until TX FIFO data are written). If TX Enable is set to 0 during the transmission, the transmission stops when the transmission of FIFO data is completed. 0: Transmission Disable.
4	**RX Enable**
3	**Wide-band IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

14.1.1.2. IR Status Register – Base Address + 1

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
Name	**RDR**	**RTR**	**PE**	**RFO**	**TE**	**TTR**	**TFU**	**GH**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**TX FIFO Empty** (Writing 1 will clear the bit).
2	**TX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
1	**TX FIFO Underrun** (Writing 1 will clear the bit).
0	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

14.1.1.3. IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**TX FIFO Empty**
2	**TX FIFO Trigger Level Reach**
1	**TX FIFO Underrun**
0	**Min Length Detected**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

14.1.1.4. RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	**RX FIFO Count**

14.1.1.5. IR TX Carrier Prescalar Configuration Register (CP) – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Mode	Reserved						CP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Mode**

	0 : DC Mode 1 : Pulse Mode
6-1	**Reserved**.
0	**Carrier Prescalar** (CP). This bit is set for the Prescalar value of the IR TX carrier frequency.

14.1.1.6. IR TX Carrier Period Configuration Register (CC) – Base Address + 5

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Period (CC)							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is set for IR TX carrier period. The actual carrier period will be: Period = 2 * (2 ^ (CP*2)) * (CC+1) / (System Clock), where the frequency = 1 / period, and System Clock = 24MHz. Setting CP and CC to 0 will cause stop the device to from use using anyno carrier at all (that is, no light modulation, just constant on and off periods). The period count value CC can be any number from 0 to 255.

14.1.1.7. IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

14.1.1.8. IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

14.1.1.9. IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TXFIFOCLR	Reserved	TX Trigger Level		RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TX FIFO Cleared**.
6	**Reserved**.
5-4	**TX Trigger Level** **Bits** **5 4** 0 0: 31 0 1: 24 1 0: 16 1 1: 8
3	**RX FIFO Cleared**.
2	**Reserved**.
1-0	**RX Trigger Level** **Bits** **1 0** 0 0: 1 0 1: 8 1 0: 16 1 1: 24

14.1.1.10. IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**IR Pending** 1: No Interrupt 0: Interrupt issue
6	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
5	**RX FIFO Trigger Level Active**.

BIT	DESCRIPTION
4	**RX FIFO Empty Flag**.
3	**RX FIFO Full Flag**.
2	**TX FIFO Trigger Level Active**.
1	**TX FIFO Empty Flag**.
0	**TX FIFO Full Flag**.

14.1.1.11. IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6-0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

14.1.1.12. TX FIFO Count– Base Address + B

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TX FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	**TX FIFO Count**

14.1.1.13. IR Sample TX FIFO Register – Base Address + C

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample TX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6-0	**TX data length** (Unit : Sample Period)

14.1.1.14. IR Carrier Count High Byte Register – Base Address + D

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count High Byte							

BIT	DESCRIPTION
7-0	**Carrier Count High Byte**. This byte records the total amount of the total rising edges until time-out event appears.

14.1.1.15. IR Carrier Count Low Byte Register – Base Address + E

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count Low Byte							

BIT	DESCRIPTION
7-0	**Carrier Count Low Byte**. This byte records the total amount of the the rising edges until time-out event appears.

After a time-out of reception on the learning receiver, this response is sent to tell the host the carrier frequency of the previous sample. The Carrier Count High Byte (ch) and Carrier Count Low Byte (cl) specify the cycle counts of cycles of the carrier. Carrier counts can also be thought ofregarded as the number of leading edges in the previous sample.

This is used toe calculation of the calculate carrier frequency is as followsfollowed:

$lastCarrierCount_{(decimal)}$ = ch*256+cl;

Thus,

Carrier frequency = (lastCarrierCount) / (irPacketOnDuration);

The **irPacketOnDuration** value is the total amount of time that the envelope of the signal was is high. The IR receiver should keep track of the time that of the high envelope is high and return it using this response.

This response is unsolicited. It is returned by the receiver when IR arrives but is never explicitly requested.

14.1.1.16. IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved	Encoder FSM		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Decoder over status**
5	**Decoder continuing status**
4	**Decoder wait H status** 1: idle, 0: RX busy
3	**Reserved**.
2	**Encoder Idle Status**. 1: idle, 0: TX busy
1	**Encoder Read Status**
0	**Encoder Level Output Status**

14.1.1.17. IR Minimum Length Register – Base Address + F

Attribute: Write Only

Size: 8 bits

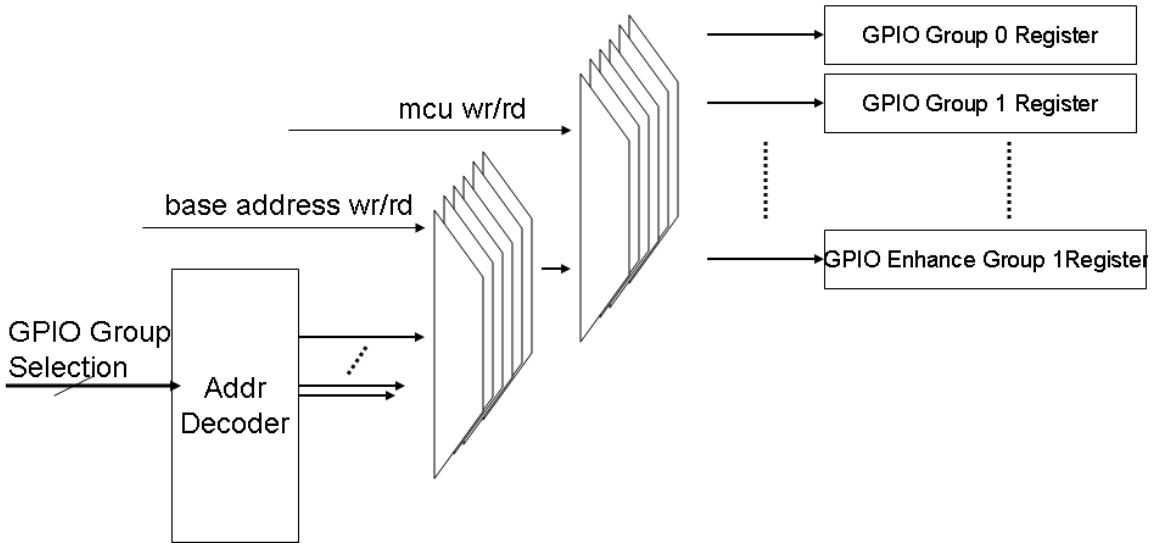
BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Min Length Register**. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

15. GENERAL PURPOSE I/O

NOTICE : Some GPIO pin functions were configured when related SW functions of EC Space were enabled. For such situations BIOS or application programs should not alter these setting to avoid abnormal function of underlying firmware. Please refer to EC Space Specification before going to change any configuration setting of GPIO pins.

GPIO Register can be programmed by LPC or 8051. LPC write to the register has two ways: through Logic Device 7, CRE0 ~ CRF0. Another way is through base address write.



For mcu write to GPIO register, the address bit 7 ~ bit4 represent GPIO Group Selection, and bit3 ~ bit0 represent different GPIO control register or run time register.

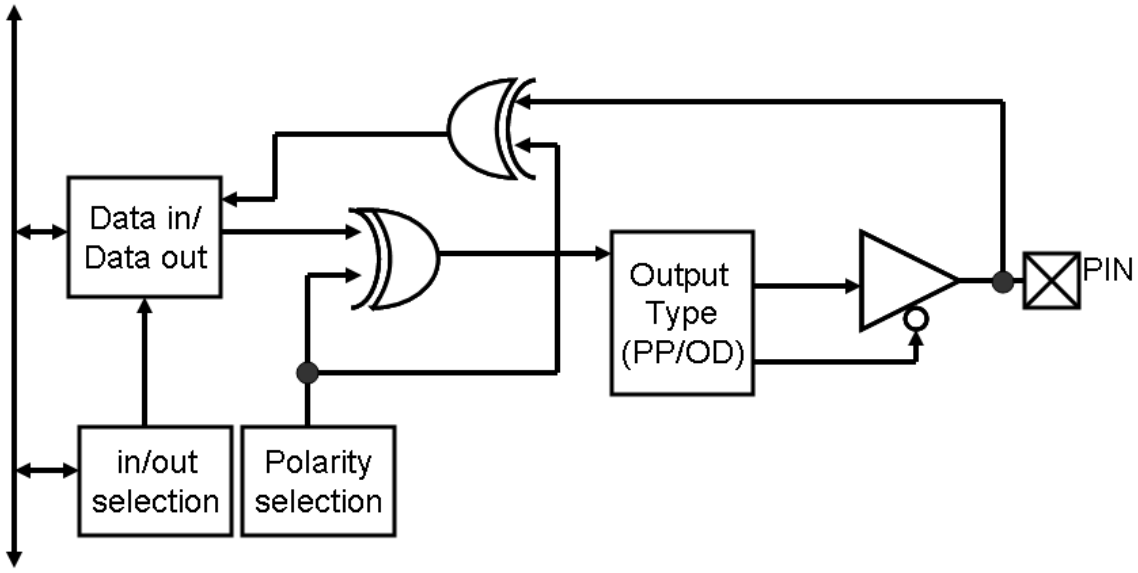


acpi_gpio_mcu_cs & (acpi_gpio_mcu_addr[7:0] = 8'h0x) : Select GPIO_GROUP0

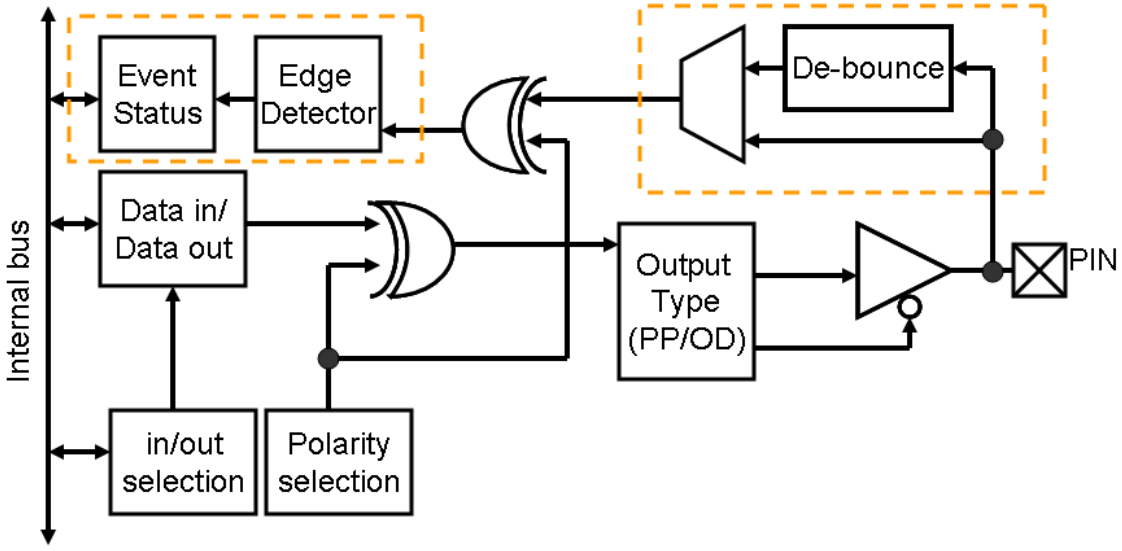
acpi_gpio_mcu_cs & (acpi_gpio_mcu_addr[7:0] = 8'h1x) : Select GPIO_GROUP1

15.1 GPIO Block Diagram

GPIO0 ~ GPIO9 Groups block diagram:

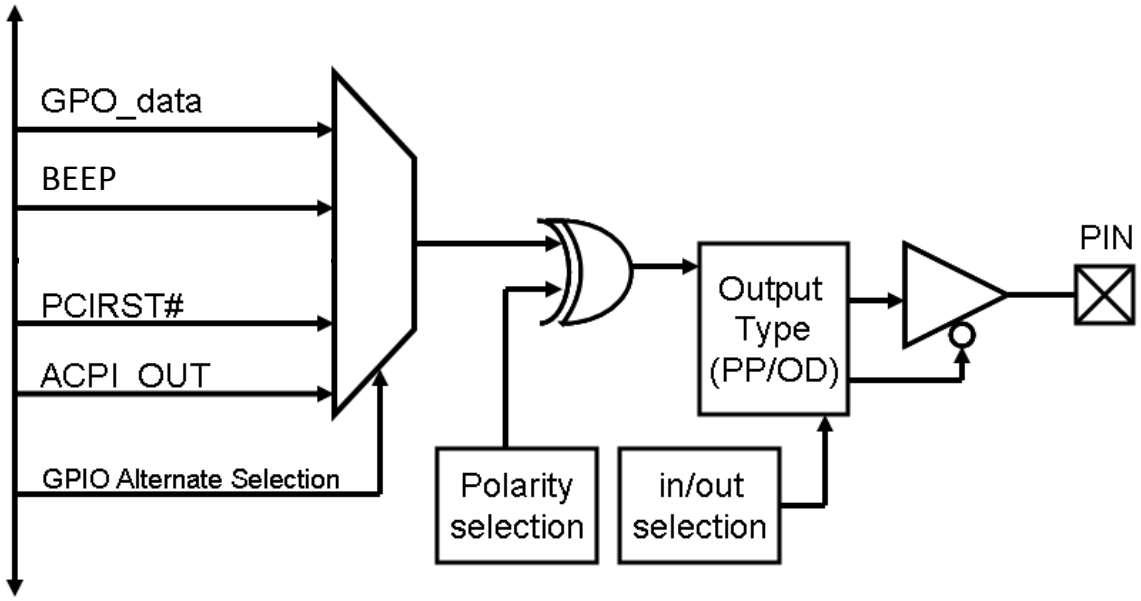


GPIOEN0 & GPIOEN1 Group block diagram:



GPIO Alternate Function block diagram:

The GPIO output can switch to BEEP function, PCIRST_OUT buffer function, and ACPI OUT function when GPO functions active. The Polarity and output type selections will also affect the output behavior.



NOTICE: When GPIO was configured to output data, please notice when GPIO data registers were read, it is the realistic pin DC status instead of wanted output state reflected by these registers. That means if external loading is heavy, the data read might not be the same as state wanted.

15.2 GPIO Runtime Register

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device 7, the GPIO device. CR[60h] is the high byte, and CR[61h] is the low byte.

GPIO Block									
BaseAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Base+0	GPIO0	GPIO Group 0 Run timer register and control register							
Base+1	GPIO1	GPIO Group 1 Run timer register and control register							
Base+2	GPIO2	GPIO Group 2 Run timer register and control register							
Base+3	GPIO3	GPIO Group 3 Run timer register and control register							
Base+4	GPIO4	GPIO Group 4 Run timer register and control register							
Base+5	GPIO5	GPIO Group 5 Run timer register and control register							
Base+6	GPIO6	GPIO Group 6 Run timer register and control register							
Base+7	GPIO7	GPIO Group 7 Run timer register and control register							
Base+8	GPIO8	GPIO Group 8 Run timer register and control register							
Base+9	GPIO9	GPIO Group 9 Run timer register and control register							
Base+A		Reserved							
Base+B	GPIOEN0	GPIO Enhance Group 0 Run timer register and control register							
Base+C	GPIOEN1	GPIO Enhance Group 1 Run timer register and control register							

Base+D	GPSEL		GPIO Control Register Selection
Base+E		Reserved.	
Base+F		Reserved.	

15.2.1 GPIO Group 0 Run timer register and control register (base+0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 0 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Group 0 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.2 GPIO Group 1 Run timer register and control register (base+1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 1 Run timer register and control register							
DEFAULT	Reserved							

BIT	DESCRIPTION
7-0	**GPIO Group 1 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.3 GPIO Group 2 Run timer register and control register (base+2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 2 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Group 2 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.4 GPIO Group 3 Run timer register and control register (base+3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 3 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Group 3 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.5 GPIO Group 4 Run timer register and control register (base+4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 4 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Group 4 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.6 GPIO Group 5 Run timer register and control register (base+5)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 5 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Group 5 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.7 GPIO Group 6 Run timer register and control register (base+6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 6 Run timer register and control register							

DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Group 6 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.8 GPIO Group 7 Run timer register and control register (base+7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 7 Run timer register and control register							
DEFAULT	Reserved							

BIT	DESCRIPTION
7-0	**GPIO Group 7 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.9 GPIO Group 8 Run timer register and control register (base+8)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 8 Run timer register and control register							
DEFAULT	Reserved			Reserved				

BIT	DESCRIPTION
7-0	**GPIO Group 8 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.10 GPIO Group 9 Run timer register and control register (base+9)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Group 9 Run timer register and control register							
DEFAULT	Reserved							

BIT	DESCRIPTION
7-0	**GPIO Group 9 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.11 GPIO Enhance Group 0 Run timer register and control register (base+B)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Enhance Group 0 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Enhance Group 0 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.12 GPIO Enhance Group 1 Run timer register and control register (base+C)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Enhance Group 1 Run timer register and control register							
DEFAULT								

BIT	DESCRIPTION
7-0	**GPIO Enhance Group 1 Run timer register and control register.** This register reflects, for both read and write, the register current selected by the GPSEL register (base+D).

15.2.13 GPIO SLECTION register (base+D)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GPIO Selection register							
DEFAULT	Reserved.				0	0	0	0

BIT	DESCRIPTION
7-0	Selects the control register or run-time register to be configured.

GPSEL	Reflect Register
4'h0	**GPIO Group x Data Register:** For output ports, the respective bits can be read/written and produced to pins. For input ports, the respective bits can be read only from pins. Write accesses will be ignored.
4'h1	**GPIO Group Interrupt Enable**
4'h2	**GPIO Status Register**

4'h3	**GPIO I/O Control Register** 1 – Input 0 – Output
4'h4	**GPIO Inversion Control Register** 1 – Inversion 0 – No Inversion
4'h5	**GPIO PP/OD Control Register** 1 – Push-Pull 0 – Open-Drain
4'h6	**GPIO Interrupt Type0 Register** 00h: Status field is trigger by falling edge. 10h: Status field is trigger by rising edge. x1h: Status field is trigger by both edge.
4'h7	**GPIO Output Data Reflection Register**
4'h8	**GPIO Internal pull down Control Register**
4'h9	**GPIO Reset Source Control Register** 00 : PCI RST# 01 : PWROK 10 : MCU Reset (Software Reset) 11 : RSMRST#
4'hA	**Reserved.**
4'hB	**GPIO De-bounce Clock Option (Only GPEN0 and GPEN1 valid)** 0: De-bounce clock base on 1KHz. 1: De-bounce clock base on 1MHz.
4'hC	**GPIO De-bounce Type 0 (Only GPEN0 and GPEN1 valid)**
4'hD	**GPIO De-bounce Type 1 (Only GPEN0 and GPEN1 valid)** { GP_De_bounce_typ0, GP_De_bounce_typ1} 00: No De-bounce. 01: De-bounce high. 10: De-bounce low. 11: De-bounce high and low.
4'hE	**GPIO De-bounce Time Option 0 (Only GPEN0 and GPEN1 valid)**
4'hF	**GPIO De-bounce Time Option 1 (Only GPEN0 and GPEN1 valid)** { GP_De_bounce_time_opt0, GP_De_bounce_time_opt1} 00: De-Bounce 4 ms / 4us 01: De-Bounce 16 ms / 16us 10: De-Bounce 32 ms / 32us 11: De-Bounce 64 ms / 64us

16. ESPI SLAVE INTERFACE MODULE (ESPI_SIF)

This specification provides a path for migrating LPC devices to a lower pin count, higher bandwidth bus. In addition to Host communication via the peripheral channel, t provides virtual wires support, out-of-band communication and device master- ing option over the chipset SPI flash device (via the PCH). The eSPI interface reuses the timing and electrical specification of the Serial Peripheral Interface (SPI) but with a different protocol to meet a different set of requirements.

16.1 Features

- Supports channels:
  —Peripheral: separate Posted and Non-Posted queues, no bus mastering
  — OOB (Out of Band tunneled SMBus): both master and slave
  — Virtual Wire
  — Master-Attached Flash Access
- Alert by a dedicated pin or by I/O[1] pin
- Supports 64-byte buffer for all channels
- Supports I/O and 32-bit memory addressing
- Up to 66 MHz eSPI clock frequency support
- Module capabilities: default values are set by hardware but can be overwritten by the firmware during initialization
- WAIT_STATE support
- CRC generation and checking by hardware
- Generates Wake-Up and/or Interrupt to the Core
- Virtual wires
  — Hardware or software wire types
  — Flexible programming interface for mapping wires to indices, selecting direction, reset source and hardware/software type
  — 22 system- and platform-specific event indices
  — Total 16 interrupts to Host, with selectable interrupt numbers (0-15, 16-31, 32-47 or 48-63)
- OOB Channel (SMBus tunneling)
  — Core access via register interface
  — 64-byte maximum payload size
- Run-time Flash Access Channel
  — Master-Attached channel: Indirect mapping for read, program and erase
  — 64 byte maximum payload size
  — Two outstanding requests with double buffer for response.
  — Automatic mode for Core reading up to 16 KB data chunks from Master-Attached flash.
  — On-the-fly flash image CRC calculation by hardware - not used.
- Port 80 support
  — Supports addresses 80h to 8Fh

16.2 Module Interface

- eSPI Interface:
  — eSPI_CLK: eSPI clock input
  — eSPI_IO3-0: bidirectional data
  — $\overline{\text{eSPI_CS}}$: eSPI chip-select input
  — $\overline{\text{eSPI_ALERT}}$: eSPI alert dedicated output
  — $\overline{\text{eSPI_RST}}$: eSPI reset input

- HMIB (SIB) master
- Core bus (APB3) slave for accessing Core-based registers
  — DMA request
- Hardware in-band event wires
- 16 Host interrupt inputs, each with interrupt number, polarity and edge/level select signals.
- Core wake-up and interrupt outputs
- Freeze enable for debug, to freeze the FIFO read pointers.
- Module enable input (puts the module in low-power state)

16.3 Block Diagram

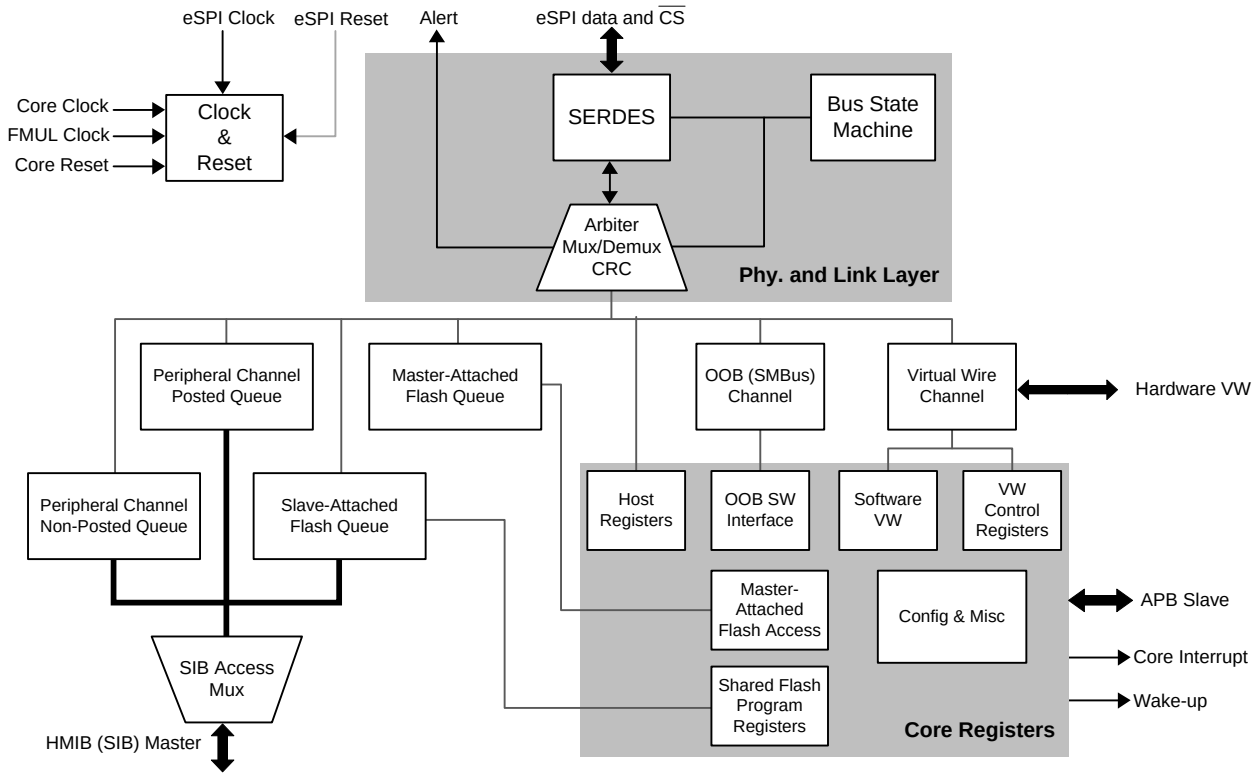


Figure 16-1 eSPI_SIF Module Block Diagram

16.4 Protocol Layer

16.4.1 WAIT_STATE Cycles

The eSPI Slave Interface Module implements a “best effort” policy for transaction completion. Where possible, transactionswill be completed within the same protocol cycle. If the transaction cannot be completed immediately, WAIT_STATE cycleswill be inserted up to maximum number configured by the Maximum WAIT_STATE Allowedfield in the General Capabilitiesand Configurations register. After that, if the module is not ready, the transaction is deferred.

16.4.2 Turn-Around Cycles

The module supports two TAR cycles.

16.4.3 Alert Indication

An Alert indication can be either output via a dedicated eSPI_ALERT pin or shared with the eSPI_IO1 pin as configured by Alert Mode bit in the General Capabilities and Configurations register. The output buffer type of the eS-PI_ALERT pin can be either push-pull or open-drain, as configured by the Open-Drain ALERT Support bit in the General

Capabilities and Configurations register.

The eSPI_ALERT output is activated (low) when eSPI_CS input is high and at least one bit in the STATUS register has changed since the previous Response phase.

16.4.4 Address Decoding

Since every eSPI slave has a dedicated chip-select input, the eSPI Slave Interface module will respond to any transaction directed to it. For Peripheral Channel access, if there is no matching address within the chip (i.e., the address is either not implemented or is currently read or write protected), the eSPI Slave Interface module will still respond **normally** (i.e., with an ACCEPT). However, the data written will be ignored and unpredictable data will be returned on read.

16.4.5 Completion Appended

The module does not support appending completion to the GET_STATUS command.

16.4.6 Error Conditions

The eSPI Slave Interface module detects various error conditions on the bus and reports them to the Host and Core, as shown in Table:

Error	Report to Host	Report to Core	Comment
Invalid Command Opcode	NO_RESPONSE	ESPIERR.INVCMD	(Note[1])
Invalid Cycle Type	NO_RESPONSE	ESPIERR.INVCYC	(Note[1])
Command Phase CRC Error	NO_RESPONSE	ESPIERR.CRCERR	(Note[1])
Unexpected Deassertion of Chip-Select	N/A	ESPIERR.ABCOMP	(Note[2])
Protocol Error: - GET without _AVAIL - PUT without _FREE	FATAL_ERROR_RESPONSE	ESPIERR.PROTERR	(Note[1])(GET without _AVAIL might occur for a Virtual Wire access after a Core Reset)
Malformed Packet, Bad Size: Payload size or Read request size is too big to fit into internal buffer.	FATAL_ERROR_RESPONSE	ESPIERR.BADSIZE	For Peripheral, OOB and Flash Access channels. (Note[3]),(Note[4])
Malformed Packet, Peripheral Channel Alignment Error: Non-Posted transaction address crosses 4 KB boundary	FATAL_ERROR_RESPONSE	ESPIERR.NPBADALN	(Note[1])
Malformed Packet, Peripheral Channel Alignment Error: Posted transaction address crosses 4 KB boundary	FATAL_ERROR_RESPONSE	ESPIERR.PCBADALN	(Note[1])
Malformed Packet, Virtual Wire Channel: Wire count for PUT_VWIRE command bigger than Maximum Virtual Wire Count configured by Host.	FATAL_ERROR_RESPONSE	ESPIERR.VWERR	(Note[5])
Unsupported Command Opcode or Cycle Type	NON_FATAL_ERROR _RESPONSE	ESPIERR.UNCMD	(Note[1])(Includes access to a disabled eSPI Channel)
Virtual Wire Channel, PUT_VWIRE	ACCEPT	ESPIERR.VWERR	(Note[1])(Unsupported

command accessing unsupported Virtual Wire index.			Virtual Wire index access includes indexes with INDEX_EN bit set to 0.)
Short Command terminated as connected (non-DEFER) that fails to be complected successfully.	ACCEPT	SMC_STS.HWERR, SMC_STS.HRERR	For Peripheral Channel access to protected area. (Note[1])
Unexpected completion received (i.e., completion with invalid tag).	ACCEPT	ESPISTS.AMERR	For Master Attached Flash Access in Automatic mode (Note[1])

1. The transaction is discarded (write is ignored and read data is unpredictable).
2. The transaction may be partially or fully executed internally before the error occurs. The eSPI Slave Interface module floats (TRI-STATE) the data outputs after the Chip-Select is deasserted.
3. The transaction might be partially or fully executed internally before the error is detected. (This is a deviation from the eSPI specification.)
4. Split completions are not supported; therefore, the request size is checked vs. buffer size and not vs. the 'Max Read Request Size' field (as required by the standard).
5. The erroneous indexes are discarded (write is ignored).

In addition to the hardware's automatic error reporting, the Core firmware can use the ERROR_FATAL and ERROR_NON_-FATAL virtual wires to report errors asynchronously to the Host.

16.5 Transaction Layer

16.5.1 Peripheral Channel

The eSPI Slave Interface Module implements slave functionality and supports the following commands:

- GET_PC, only for completions
- PUT_PC and PUT_NP, for read or write requests with 32-bit memory addressing
- PUT_IORD_SHORT, PUT_IOWR_SHORT

The following commands are not supported:

- All command / cycle types specific to bus master mode (because eSPI bus master is not supported)
- Message and Message with Data cycle types (the data packet is ignored and NON_FATAL_ERROR is returned)

When an unsupported command / cycle type is received, the Peripheral Channel returns NON_FATAL_ERROR. When an invalid (i.e., not defined in eSPI) command / cycle type is received, the module returns NO_RESPONSE. The Peripheral Channel supports separate 64-byte buffers for read (Non-Posted) and write (Posted) directions. (After receiving the request and verifying CRC, the Peripheral Channel translates the eSPI data burst into the required number of read or write trans-actions on the HMIB (SIB) with the transaction being 1, 2 or 4 byte wide. HMIB transaction width is indicated by the HMIB addressed coder at the beginning of the transfer, immediately after the eSPI Slave Interface module places the address on the bus.)

The Peripheral Channel is enabled when HPCHANEN and PCHANEN bits in ESPICFG register are both 1. (When the Periph- eral Channel is disabled or if it is not supported (PCCHN_SUPP bit in ESPICFG register is 0), all internal bits are reset, the queues are invalidated, PC_AVAIL and NP_AVAIL bits are set to 0, and if CHAN_FREE_EN bit in TEST11 register is set to 1then PC_FREE and NP_FREE bits are forced to 0; in addition, Alert is not generated.)

Queues and Ordering

The Peripheral Channel implements separate queues for Posted and Non-Posted transactions. The depth of both queues is 1,which means that only one transaction per queue can be pending at a time. The Posted Queue is given priority (on the HMIB bus), i.e., ongoing Non-Posted transfers (on HMIB) will be put on hold if there is a

pending request from the Posted Queue.(The Posted Queue will complete the whole transfer before releasing ownership on HMIB.)

16.5.2 Virtual Wire Channel

At initialization time, the Core firmware should poll for HVWCHANEN bit in ESPICFG register being set to 1, to start using this channel.

Virtual wires supported by the eSPI_SIF module are divided into the following categories:

- Interrupts
- System and Platform Specific Events
- “Floating” Events

The Virtual Wire Channel is enabled when HVWCHANEN and VWCHANEN bits in ESPICFG register are both 1. (When the Virtual Wire Channel is disabled or if it is not supported (VWCHN_SUPP bit in ESPICFG register is 0), the Virtual Wires are not affected, the queues are not affected, VWIRE_AVAIL bit is set to 1 if a Slave-to-Master Virtual Wire changes, and Alert is not generated)

Interrupts

The module receives up to 16 interrupt inputs from the NPCX667K. Each interrupt input is accompanied by three additional configuration inputs: interrupt number, polarity and edge/level selection. If the interrupt number is 0, the interrupt input is disabled. The 16 interrupts can be mapped to eSPI IRQs according to INTWIN field in VWCTL register. The module supported edge-triggered interrupts by allowing sending an IRQ number twice during a single eSPI transaction.

System- and Platform-Specific Events

The eSPI Slave Interface module provides a flexible mechanism for managing event virtual wires. The module provides a pool of up to 22 Virtual Wire indices. The indices are divided into two (three, including the “Floating Events”) groups, based on their direction (Master-to-Slave or Slave-to-Master). Every index manages four virtual wires. Registers VWEV(MS/SM)n provide a programming interface for index configuration and run-time functionality.

At initialization time, the Core firmware must enable the required indices for every group, set the “Valid” bits for output type indices and map each group to an eSPI Virtual Wire Index value. Mapping is performed via the INDEX field. The Core firmware may update the configuration of the virtual wires only when the eSPI bus is idle or when the Virtual Wire Channel is disabled. Some of the indices wake up already enabled and configured to match the current usage by the system; it is recommended to leave these indices at their default configuration values. Core firmware may change all defaults at initialization time.

Each virtual wire that is managed by the index registers can be used as a software wire (read or written by the Core firmware)or hardware wire (connected to other modules in the NPCX667K). When Master-to-Slave Virtual Wires are updated by the Host, only a wire with a corresponding Valid bit set is updated. The value of the other wires is ignored (i.e., they remain unchanged). The value of the Valid bits can be read by the Core.

The state of the Master-to-Slave virtual wires is updated only after deassertion of the eSPI_CS input. In the opposite direc- tion, the updating of the Slave-to-Master virtual wires by the NPCX667K is disabled (the bits are latched) during eSPI trans- actions (i.e., when eSPI_CS is asserted). Therefore, writes to the virtual wire bits or changes of hardware signals take effect only after the transaction is completed. Because of this, the time between two consecutive state changes of a Slave-to-Mas- ter virtual wire must be longer than the longest eSPI Virtual Wire Channel transaction used (depending on the setting of the Operating Maximum Virtual Wire Count field in the Channel 1 Capabilities and Configuration register). In addition, if the NP-CX667K is in Sleep or Deep Sleep power state and CLK clock is stopped, the minimum time between consecutive Virtual Wire transactions must be longer than the clock wake-up time. Note that faster Virtual Wire state changes might be “missed”.

An exception is PLTRST Virtual Wire (in Index 3 - VWEVMS1 register), which can be asserted and then deasserted in two consecutive transactions without requiring the minimum time between the transactions, as described above.

(Note that eSPI-based systems do not require the Valid bits of the Slave-to-Master virtual wires to be changed, except at eSPI_SIF module initialization.)

Some of the virtual wires (e.g., PLTRST) have special functionality that affects NPCX667K behavior. (To keep the architecture flexible, they are still handled via the index registers. At the chip integration level, the relevant Virtual

Wire outputs must be looped back to the relevant module inputs. The firmware must set the configuration registers accordingly.)

The Core firmware is responsible for performing the handshake with the Host and for sending the required acknowledge virtual wire events (e.g., HOST_RST_WARN, OOB_RST_WARN).

"Floating" Events

The Core firmware can send a Slave-to-Master group of events of any index to the Host, using VWPING register. These are called "floating" events, because the value of INDEX field can be changed, dynamically, at run-time instead of being fixed at initialization. DIRTY bit of the "floating" events group is set to 1 on any Core write to VWPING register, as opposed to the other Slave-to-Master virtual wire events, where the DIRTY bit is set to 1 only on a change of one of the valid Wire 3-0 bits.

VWIRE_AVAIL Generation

VWIRE_AVAIL bit in STATUS register is set to 1 when one or more Slave-to-Master virtual wire events are pending, i.e., when the DIRTY bit of one or more Slave-to-Master Virtual Wire groups becomes 1. Note that DIRTY and VWIRE_AVAIL bits are also set to 1 if a virtual wire changed as a result of a Core Reset (if it is enabled by ENCDRST bit in the respective VWEVSMn register). Also note that DIRTY and VWIRE_AVAIL bits are not affected by a PLTRST reset even if this reset is enabled by ENPLTRST bit in the respective VWEVSMn register; however, they are cleared to 0 after eSPI_RST reset (also after V_{CC} Power-Up reset or VCC_RST reset).

Arbitration between Slave-to-Master Virtual Wires

To avoid "starvation", when more than one Slave-to-Master virtual wire group is pending, the eSPI Slave Interface module decides which groups to send in the current transaction, based on arbitration rules with the following priority scheme (from highest to lowest):

- "Floating" events (via VWPING register)
- Interrupts
- Round robin between events and GPIOs - not used (no GPIO Virtual Wires).

Virtual Wire Connection in NPCX667K

The table below shows the System and Platform-Specific Virtual Wire Events connected by the hardware to other NPCX-667K modules. The Virtual Wires in the table are compatible with the eSPI Specification and Intel chipset.

Table eSPI System- and Platform-Specific Virtual Wires

Index #	Direction	Bit #	Bit Name	eSPI_SIF Reg.	Connection
02h	In (Master-to-Slave)	3	Reserved	VWEVMS0	N.C.
		2	$\overline{\text{SLP_S5}}$		VW_SLPST.VW_SLP_S5
		1	$\overline{\text{SLP_S4}}$		VW_SLPST.VW_SLP_S4
		0	$\overline{\text{SLP_S3}}$		VW_SLPST.VW_SLP_S3
03h	In (Master-to-Slave)	3	Reserved	VWEVMS1	N.C.
		2	OOB_RST_WARN		N.C.
		1	$\overline{\text{PLTRST}}$		Host Hardware Reset
		0	$\overline{\text{SUS_STAT}}$		N.C.

Table eSPI System- and Platform-Specific Virtual Wires (Continued)

Index #	Direction	Bit #	Bit Name	eSPI_SIF Reg.	Connection
04h	Out(Slave-to-Master)	3	$\overline{\text{PME}}$	VWEVSM0	N.C.
		2	$\overline{\text{WAKE}}$		N.C.
		1	Reserved		N.C.
		0	OOB_RST_ACK		N.C.
05h	Out(Slave-to-Master)	3	SLAVE_BOOT_LOAD_STATUS	VWEVSM1	N.C.
		2	ERROR_NON_FATAL		N.C.
		1	ERROR_FATAL		N.C.

		0	SLAVE_BOOT_LOAD_DONE		N.C.
06h	Out(Slave-to-Master)	3	HOST_RST_ACK	VWEVSM2	N.C.
		2	$\overline{\text{RCIN}}$		$\overline{\text{KBRST}}$ internal output signal
		1	$\overline{\text{SMI}}$		$\overline{\text{SMI}}$ internal output signal
		0	$\overline{\text{SCI}}$		$\overline{\text{EC_SCI}}$ internal output signal
07h	In (Master-to-Slave)	3	Reserved	VWEVMS2	N.C.
		2	Reserved		N.C.
		1	Reserved		N.C.
			HOST_RST_WARN		N.C.
40h	Out(Slave-to-Master)	3	Reserved	VWEVSM3	N.C.
		2	Reserved		N.C.
		1	Reserved		N.C.
		0	SUS_ACK		N.C.
41h	In (Master-to-Slave)	3	$\overline{\text{SLP_A}}$ ($\overline{\text{SLP_M}}$)	VWEVMS3	VW_SLPST.VW_SLP_A
		2	Reserved		N.C.
		1	$\overline{\text{SUS_PWRDN_ACK}}$		N.C.
		0	$\overline{\text{SUS_WARN}}$		N.C.
42h	In (Master-to-Slave)	3	Reserved	VWEVMS4	N.C.
		2	Reserved		N.C.
		1	SLP_WLAN		VW_SLPST.VW_SLP_WLAN
		0	SLP_LAN		VW_SLPST.VW_SLP_LAN
43h	In (Master-to-Slave)	3	PCH_TO_EC_GENERIC_3	VWEVMS5	N.C.
		2	PCH_TO_EC_GENERIC_2		N.C.
		1	PCH_TO_EC_GENERIC_1		N.C.
		0	PCH_TO_EC_GENERIC_0		N.C.
44h	In (Master-to-Slave)	3	PCH_TO_EC_GENERIC_7	VWEVMS6	N.C.
		2	PCH_TO_EC_GENERIC_6		N.C.
		1	PCH_TO_EC_GENERIC_5		N.C.
		0	PCH_TO_EC_GENERIC_4		N.C.
45h	Out(Slave-to-Master)	3	PCH_TO_EC_GENERIC_3	VWEVSM4	N.C.
		2	PCH_TO_EC_GENERIC_2		N.C.
		1	PCH_TO_EC_GENERIC_1		N.C.
		0	PCH_TO_EC_GENERIC_0		N.C.

Table eSPI System- and Platform-Specific Virtual Wires (Continued)

Index #	Direction	Bit #	Bit Name	eSPI_SIF Reg.	Connection
46h	Out(Slave-to-Master)	3	EC_TO_PCH_GENERIC_7	VWEVSM5	N.C.
		2	EC_TO_PCH_GENERIC_6		N.C.
		1	EC_TO_PCH_GENERIC_5		N.C.
		0	EC_TO_PCH_GENERIC_4		N.C.
47h	In (Master-to-Slave)	3	Reserved	VWEVMS7	N.C.
		2	Reserved		N.C.
		1	Reserved		N.C.

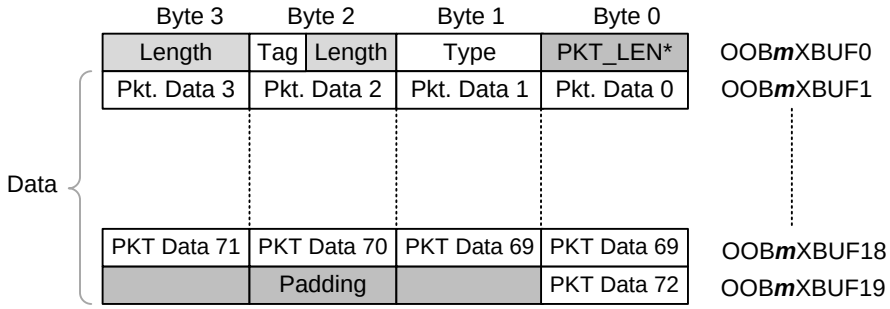
		0	HOST_C10		N.C.

16.5.3 OOB (Tunneled SMBus) Channel

The OOB Channel is operational (enabled) when HOOBCHANEN and OOBCHANEN bits in ESPICFG register are both 1. At initialization time, the Core firmware should poll for HOOBCHANEN bit in ESPICFG register set to 1, to start using this channel.(When the OOB Channel is disabled or if it is not supported (OOBCHN_SUPP bit in ESPICFG register is 0), the data buffers are flushed, queues are invalidated, OOB_AVAIL bit in both STATUS and OOBCTL registers is set to 1 (if a Slave-to-Master message is ready in the Tx buffer), and if CHAN_FREE_EN bit in TEST11 register is set to 1, then OOB_FREE bit (in STATUS register only) is forced to 0; in addition, Alert is not generated.)

The eSPI_SIF module provides a simple register interface for the OOB Channel. The received packets are placed in the OOB Receive Buffer (OOBRXBUFn) register group. The buffer holds the header and the payload but not the eSPI command field of the packet. The Core firmware should write the packets for transmission in the OOB Transmit Buffer (OOBTXBUFn) registers. The Core firmware is responsible for SMBus protocol handling, such as SMB us Slave address decoding, error detection, etc.

The maximum payload size is 73 bytes; however, it is reported as 64 bytes in the Maximum Payload Size Supported field of the Channel 2 Capabilities and Configurations register. The Rx and Tx buffer registers have 80 bytes each, as shown in Figure 16-2 : (73 bytes for data payload + 3 bytes for Header + 1 byte (byte 0) for alignment + 3 padding bytes (the last) to make the total size a multiple of 4. Byte 0 is used for alignment; it is reserved and should be ignored by the Core firmware when reading from OOBRXBUF0 register of the Rx buffer. In the Tx buffer, the Core firmware must write the packet length to byte 0 of OOB-TXBUF0 register.)



* - PKT_LEN holds the total packet length (including Header - i.e., starting from Byte 1 of OOBmXBUF0) for the Tx buffer;
it is ignored for the Rx buffer.

m - Replace with “T” for Tx buffer or with “R” for Rx buffer.

Figure 16-2 OOB Rx and Tx Buffers

To send a message via the OOB Channel, the Core firmware should perform the following sequence:

1. Check if OOB_AVAIL bit in OOBCTL register is 0, to verify that the Tx buffer is empty.
2. Write the whole packet (including header and data payload but excluding the transaction opcode) as follows:
   2.1 Write the data to OOBTXBUF1-OOBTXBUF19 DWord registers.
   2.2 Write the Length, Tag, Type and PKT_LEN (total packet length, including header and data payload but excluding the transaction opcode) field data to OOBTXBUF0 DWord register.
3. Set OOB_AVAIL bit in OOBCTL register to 1 to enqueue the packet for transmission.

When a tunneled SMBus message is received via the OOB Channel, OOBRX bit in ESPISTS register is set. If enabled, an interrupt to the Core is also generated. In response, the Core firmware should perform the following sequence:

1. Clear OOBRX bit in ESPISTS register to 0.
2. Read the message from the OOBRXBUFn DWord registers. The length of the message is indicated by LENGTH field in the packet header.
3. Set OOB_FREE bit in OOBCTL register to 1.

16.5.4 Master-Attached Flash Access Channel

The Master-Attached Flash Access Channel is operational (enabled) when HFLASHCHANEN and FLASHCHANEN bits in ESPICFG register are both 1. On initialization, the Core firmware should poll for HFLASHCHANEN bit in ESPICFG register set to 1, to start using this channel. (When the Master-Attached Flash Access Channel is disabled or if it is not supported(FLASHCHN_SUPP bit in ESPICFG register is 0), the data buffers are flushed, queues are invalidated, FLASH_NP_AVAIL and FLASH_C_AVAIL bits are set to 1 (if Slave-to-Master data is ready in one of the Tx buffers) and Alert is not generated.)

The Master-Attached Flash Access Channel provides two modes of operation: Manual and Automatic. Mode selection is via AMTEN bit in FLASHCTL register.

Manual Mode. Manual mode operation is similar to the OOB channel. The Master-Attached Flash Access Channel provides a simple register interface for indirect access of the Master-Attached flash. The register groups Flash Transmit Buffer(FLASHTXBUFn) and Flash Receive Buffer (FLASHRXBUFn) serve the Core firmware for placing request packets and reading completion packets, respectively. The buffers hold full transaction layer packets, including cycle type, tag and length. The Core firmware is responsible for encoding and decoding the packet contents, including handling of unsuccessful completions.

The maximum payload size supported for completion (Rx) is 64 bytes. Therefore:

- For STRPHDR bit in FLASHCTL register set to 0, the Rx buffer registers hold 68 bytes (64 bytes for data payload, 3 bytes for Header and 1 byte (byte 0) for alignment to make the total size a multiple of 4; byte 0 is reserved and should be ignored by the Core firmware when reading from FLSHRXBUF0 register of the Rx buffer); see Figure 16-3.
- For STRPHDR bit set to 1 (i.e., “removed” header), the Rx buffer registers hold 64 bytes (for data payload); see Figure 16-3.

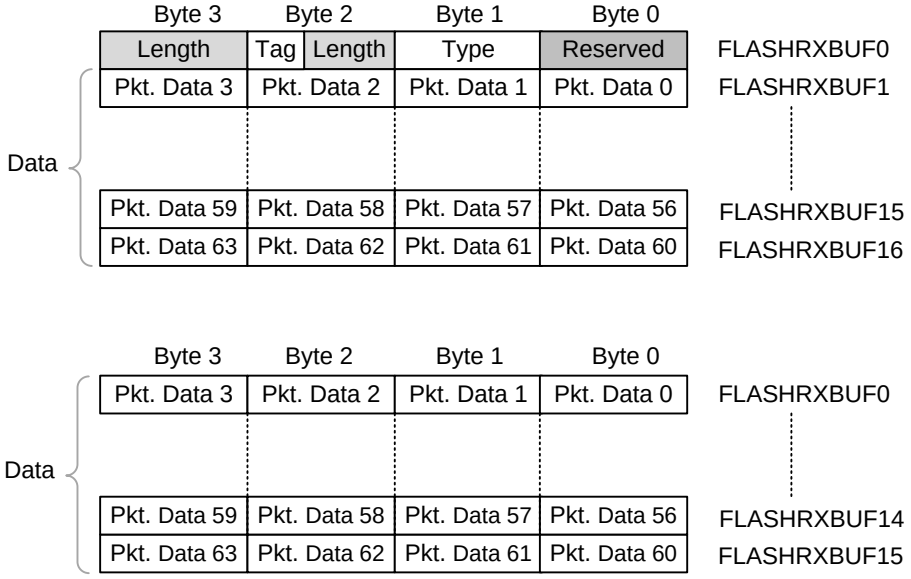
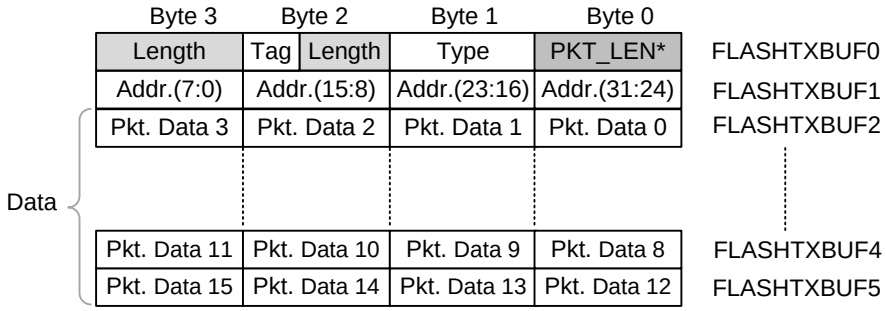


Figure 16-3 Flash Access Channel Rx Buffer for STRPHDR = 1

The maximum payload size supported for requests (Tx) is 16 bytes. Therefore, the Tx buffer registers hold 24 bytes, as shown in Figure 16-4 (24 bytes = 16 bytes for data payload + 4 bytes address + 3 bytes for Header + 1 byte (Byte 0) for alignment to make the total size a multiple of 4. The Core firmware must write the packet length to byte 0 ofFLASHTXBUF0 register.).



* - PKT_LEN holds the total packet length (including Header - i.e., starting from Byte 1 of FLASHTXBUF0).

Figure 16-2 Flash Access Channel Tx Buffer

To send a request via Master-Attached Flash Access Channel in Manual mode, the Core firmware should perform the fol- lowing sequence:

1. Optionally, set STRPHDR bit in FLASHCTL register to 1.
2. Set AMTEN bit in FLASHCTL register to 0, to select Manual mode.
3. Check if FLASH_TX_AVAIL bit in FLASHCTL register is 0, to verify that the Tx buffer is empty.
4. Write the whole packet (including header and data payload but excluding the transaction opcode) as follows:
   4.1 Write the data to FLASHTXBUF1-FLASHTXBUF5 DWord registers.
   4.2 Write the Length, Tag, Type and PKT_LEN (total packet length, including header and data payload but excluding the transaction opcode) field data to FLASHTXBUF0 DWord register.
5. Set FLASH_TX_AVAIL bit in FLASHCTL register to 1, to enqueue the packet for transmission.
6. Wait for completion (interrupt or polling) indicated by FLASHRX bit in ESPISTS register.
7. Read the completion data from the FLASHRXBUFn DWord registers (either directly or via FLASHRXRDHEAD register)and verify if the completion is successful. The length of the message is indicated by LENGTH field in the packet header.

Automatic Mode. In Automatic mode (i.e., when AMTEN bit in FLASHCTL register is set to 1), the Master-Attached Flash Access Channel supports sequential reading up to 256 64-byte blocks, from consecutive addresses in the flash. The hard-ware will automatically place the required number of requests with addresses incremented by 64 and with an alternating 0/1TAG field. For best performance, the channel allows pipe-lined reading from the flash by placing up to two outstanding re-quests to the eSPI master and maintaining a double buffer (two, 64-byte receive buffers) for completions.

In Automatic mode, the module hardware checks for tag consistency in the completion packets. In addition, it verifies if the com -pletion is successful. In case of an unsuccessful completion, a bad tag or bad length, Automatic mode operation halts, AMTENbit in FLASHCTL register is set to 0 and an error is indicated to the firmware via AMERR bit in ESPISTS register. In case of normal completion, AMDONE bit in ESPISTS register is set to 1; in case of unsuccessful completion, AMDONE and AMERR bits are both set to 1.

Note that split completions are not supported by the module. If a split completion is received in Automatic mode, the hard-ware treats it as an ‘Unsupported Cycle type’ error. (In Manual mode, the Core firmware must provide the error response.)

If $\overline{\text{eSPI_RST}}$ is asserted during Automatic mode (i.e., after FLASH_TX_AVAIL bit in FLASHCTL register is set to 1), the fol- lowing occurs:

- AMTEN bit in FLASHCTL register is set to 0 (i.e., Automatic mode is terminated).
- FLASH_TX_AVAIL bit in FLASHCTL register is set to 0 (i.e., the transmit queue is empty).
- AMDONE bit in ESPISTS register is set to 1 (i.e., Automatic mode was completed).
- AMERR bit in ESPISTS register is set to 1 (i.e., Automatic transfer failed).

In Automatic mode, the Core firmware should perform the following **request** sequence:

It **not** working with **DMA**:

1. **Optionally** set STRPHDR bit in FLASHCTL register to 1.
2. Set AMTEN bit in FLASHCTL register to 1, to select Automatic mode.
3. Write the required burst size (i.e., the number of 64-byte transfers) to AMTSIZE field in FLASHCTL register.
4. Check if FLASH_TX_AVAIL bit in FLASHCTL register is 0, to verify that the Tx buffer is empty.
5. Write the first request packet to the FLASHTXBUFn DWord registers (either directly or via FLASHTXWRHEAD register).LENGTH field must be set to 64, the TAG field must be set to 0 and the

Address must be aligned to the size of the entire Automatic mode burst.

6. Set FLASH_TX_AVAIL bit in FLASHCTL register to 1, to enqueue the packet for transmission.
7. Wait for completion (interrupt or polling) indicated by FLASHRX bit in ESPISTS register.
8. Clear the FLASHRX bit by writing 1 to it.
9. Read 64 bytes of the completion data from FLASHRXBUFn DWord registers via FLASHRXRDHEAD register.
10. Read the AMT_BFULL bit in FLASHCTL register and repeat item 9, as long as the bit is set to 1.
11. If AMDONE bit in ESPISTS register is 0 (i.e., not “done” yet), repeat from item 7; otherwise, continue.
12. Check if AMERR bit in ESPISTS register is set to 0 (i.e., if no error occurred).
13. Set AMTEN bit in FLASHCTL register to 0 to terminate the Automatic mode and select Manual mode.

Important note: It must not enter Sleep or Deep Sleep power states (i.e., the APB clock must be active)during the entire Automatic mode transfer operation.

Transmit/Receive Buffers Pointer Reset. Every buffer has two pointers, as follows:

- **Transmit** buffer:
  - — Write pointer: this pointer is used to fill the buffer by writing new data to it
  - — Transmit pointer: this internal pointer is used to transmit the data via eSPI
- **Receive** buffer:
  - — Receive pointer: this internal pointer is used to receive the data from the eSPI
  - — Read pointer: this pointer is used to empty the buffer by reading the data from it

The pointers of the **Transmit buffer** are reset in the following cases:

- The Transmit pointer is reset when:
  - — After the number of bytes in PKT_LEN field was transmitted
- The Write pointer (FLASHTXWRHEAD) is reset when:
  - — FLASH_TX_AVAIL bit in FLASHCTL register is set to 1 (to enqueue a new packet for transmission)
  - — 1 is written to RSTBUFHEADS bit in FLASHCTL register (to reset the buffer pointers)

The pointers of the **Receive buffer** are reset in the following cases:

- The Receive pointer is reset when:
  - — A PUT_FLASH_C transaction is detected
- The Read pointer (FLASHRXRDHEAD) is reset when:
  - — In Manual mode, any PUT_FLASH transaction is received (PUT_FLASH_C in Master-Attached Flash Access mode)
  - — In Automatic mode, after all the transaction bytes were read from the buffer
  - — When 1 is written to RSTBUFHEADS bit in FLASHCTL register (to reset the buffer pointers)

A Buffer Pointer reset, via RSTBUFHEADS bit in FLASHCTL register, should be used only when a Manual or Automatic flashtransaction was aborted. After the pointers are reset, writing to the Transmit buffer overwrites the old data in the buffer andreading from the Receive buffer returns the old data from the buffer.

On-The-Fly CRC/Checksum Calculation - Not Used

The Master-Attached Flash Access Channel supports on-the-fly, 32-bit CRC or Checksum calculation for data read by the Core from the FLASHRXBUFn registers. The Core firmware must set STRPHDR bit in FLASHCTL register to 1 so that only data bytes will be taken into account (and not the command and the header). The current result is held in FLASHCRC register. The current result is updated continuously on every Core bus (APB) read from the FLASHRXBUFn registers as long as CRCEN bit in FLASHCTL register is set. To reset the CRC/Checksum result, the Core firmware must write a new seed value to FLASHCRC register. CHKSUMSEL bit in FLASHCTL register selects either Checksum or CRC calculation.

The CRC calculation uses CRC32 algorithm with this polynomial:
$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X^{1}+X^{0}$

Note: This CRC is unrelated to the eSPI packet CRC.

16.6 Core Interrupt

- The eSPI_SIF module generates an interrupt to the Core when it detects an enabled interrupt event, as follows:
- An in-band RESET Command is received, indicated by IBRST bit in ESPISTS register.

- The eSPI configuration is updated, indicated by CFGUPD bit in ESPISTS register.
- An eSPI bus error is detected, indicated by BERR bit in ESPISTS register.
- A Peripheral Channel transaction is received, indicated by PERACC bit in ESPISTS register.
- Peripheral Channel transaction is deferred, indicated by DFRD bit in ESPISTS register.
- Any Master-to-Slave Virtual Wire is updated by the Host, indicated by VWUPD bit in ESPISTS register.
- PLTRST Virtual Wire is asserted, indicated by PLTRST bit in ESPISTS register.
- Any of four general-purpose Slave-to-Master Virtual Wire “floating” events occurs (for future use), indicated by VW1-4bits in ESPISTS register.
- OOB Channel message data is received, indicated by OOBRX bit in ESPISTS register.

The Master-Attached Flash Access Channel data is received, indicated by FLASHRX bit in ESPISTS register.
The module keeps the interrupt request active until the Core firmware clears or disables all the active and enabled interrupt events.

16.7 Core Wake-Up

The eSPI_SIF module asserts the wake-up output signal when it detects an enabled wake-up event, as follows:

- eSPI_RST input pin is asserted, indicated by ESPIRST bit in ESPISTS register.
- An in-band RESET Command is received, indicated by IBRST bit in ESPISTS register.
- The eSPI configuration is updated, indicated by CFGUPD bit in ESPISTS register.
- An eSPI bus error is detected, indicated by BERR bit in ESPISTS register.
- A Peripheral Channel transaction is received, indicated by PERACC bit in ESPISTS register.
- Peripheral Channel transaction is deferred, indicated by DFRD bit in ESPISTS register.
- Any Master-to-Slave Virtual Wire is updated by the Host, indicated by VWUPD bit in ESPISTS register.
- OOB Channel message data is received, indicated by OOBRX bit in ESPISTS register.
- The Master-Attached Flash Access Channel data is received, indicated by FLASHRX bit in ESPISTS register.

The module keeps the wake-up request active until the Core firmware clears or disables all the active and enabled wake-up events.
To use wake-up event, must to set ESPIIE register for wake-up event sources, and set IEN4[0] (SFR register) to 1 for enable eSPI wake-up.

16.8 Clock

The eSPI_SIF module uses three clock sources:

- eSPI Clock (eSPI_CLK)
- High-frequency Clock (FMCLK)
- Core Clock (CLK) (actually, the APB3 clock)

The eSPI Slave Interface module requires the following frequency rations between the clock sources:
$^{f}FMCLK \geqq (^{f}eSPI_{CLK} / 1.9)$ (for example, at 66 MHz eSPI operation, the FMCLK frequency should **not** be less than 35 MHz) $^{f}CLK \geqq (^{f}eSPI_{CLK} / 6)$
The eSPI_SIF module has three clock domains:

- **eSPI Clock (eSPI_CLK).** This clock serves the Phy. and Link Layer block, Host registers, Host side of the buffers for OOB, Flash Access and Virtual Wire channels. The clock is idle except during eSPI bus activity, when it is active.
- **APB3 (Core) Clock (CLK)**. This clock serves the Core register block, Core side of the buffers for OOB, Flash Access and Virtual Wire channels. The clock is idle while the Core is in Sleep and Deep Sleep power states.
- **Combined Clock (COMB_CLK)**. This clock is internally generated by multiplexing the eSPI_CLK and the internal FMCLK clock sources , as follows:
  - If eSPI_CS is active, the eSPI_CLK clock is selected.
  - Otherwise, the internal FMCLK is selected. Note that this clock is idle while the Core is in Sleep or Deep Sleep power state.

  To prevent data loss, before the Core enters Sleep or Deep Sleep power states, the COMB_CLK clock source switches to eSPI_CLK. The internal FMCLK clock serves all the sub-modules with HMIB (SIB) interface, i.e., Peripheral channel and Slave-Attached Flash Access channel read logic.

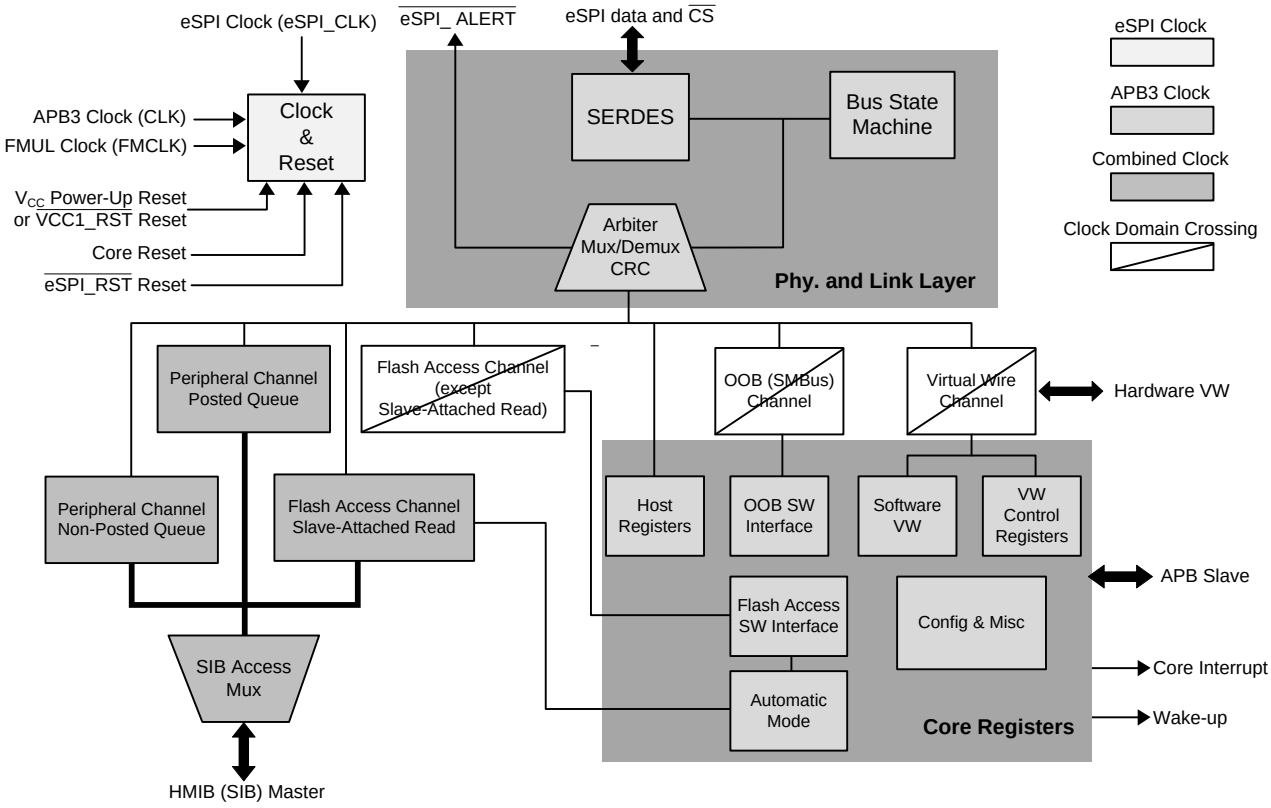


Figure 16-3 eSPI_SIF Module Clock Domains

16.9 Reset

The eSPI_SIF module uses the following reset sources:

- V_{CC} Power-Up reset or VCC_RST reset - resets the whole module
- Core Reset - resets the Core bus related part of the module and part of the Core registers. This reset is generated by Core Domain reset (only, or by either V_{CC} Power-Up reset or VCC_RST reset). Since this reset might cause a loss of state “synchronization” between the eSPI Master in the Chipset and the eSPI Slave, it is recommended to perform a full Chipset/platform reset following a Core Reset. (For Intel-based systems, it should control both RSMRST and DSW_PWROK signals, each having an external pull-down resistor. When a Core Domain reset occurs, the GPIOs become floating; therefore, the external pull-down resistors drive both RSMRST and DSW_PWROK signals to low, thus generating a Deep-Sx reset without turning off the V_{CC} and the Prim_xxx power supplies.)
- eSPI reset (eSPI_RST) - resets the eSPI bus related part of the module, eSPI registers and part of the Core registers
- eSPI in-band RESET Command - resets only the General Capabilities and Configuration register
- eSPI_CS chip-select input - resets only the Phy. and Link Layer logic
- PLTRST Virtual Wire - resets the Peripheral Channel (including the SIB Transaction layer) and some of the Virtual Wires

The entire module is reset by V_{CC} Power-Up reset or VCC_RST reset. In addition, the reset domains mainly follow the clock domains, i.e., the logic clocked by eSPI_CLK or by COMB_CLK is reset by eSPI_RST, and the logic clocked by APB3clock (CLK) is reset by Core Reset. The following are exceptions:

- PHY and Link layers are also reset when eSPI_CS is inactive (high). This guarantees recovery from abnormally terminated transactions.
- The Flash Access and OOB channels transmit and receive buffers contents are reset only by V_{CC} Power-Up reset or VCC_RST reset.

- The General Capabilities and Configuration Register is also reset by the eSPI in-band RESET Command.
- The Configuration Core registers are reset only by V_{CC} Power-Up reset or VCC_RST reset.
- The reset sources of the Virtual Wires vary. See Section 16.12 for details.
- When the PLTRST Virtual Wire reset is asserted (i.e., set to 0), if a Peripheral Channel transaction is in progress, itis aborted, PC_AVAIL bit is set to 0 (i.e., no “available”), and PC_FREE and NP_FREE bits are set to 1 (i.e., free).

The Core firmware must complete the configuration of the eSPI_SIF module before releasing the system from reset.

16.10 Low-Power Support

If the eSPI_SIF module is not in use, it can be powered down (i.e., both its FMCLK and CLK clocks can be turned off) to minimize power consumption in all the power states. eSPI_SIF module power-down is controlled by eSPI_PD bit in PWDWN_CTL6 register. After Core Reset, the eSPI_SIF module is powered up.

(Note that in “eSPI Mode” (i.e., when V_{HIF} is 1.8V), setting this bit to 1 disables the COMB_CLK clock to both the SHM mod-ule and the Debug Port 80 function.)

16.11 eSPI_SIF Host Registers

The eSPI Host registers are defined in the eSPI specification. This section shows the implementation-specific data.

16.11.1 eSPI_SIF Host Register Map

Base address: 0000h, I/O mapped

Offset	Mnemonic	Register Name	Size	Type
N/A	STATUS	Status	Word	RO
04h		Device Identification	Dword	RO
08h		General Capabilities and Configuration	Dword	Varies per bit
10h		Channel 0 Capabilities and Configuration	Dword	Varies per bit
20h		Channel 1 Capabilities and Configuration	Dword	Varies per bit
30h		Channel 2 Capabilities and Configuration	Dword	Varies per bit
40h		Channel 3 Capabilities and Configuration	Dword	Varies per bit

16.11.2 Status Register (STATUS)

Offset: N/A (accessed via GET_STATUS Command)
Reset: Varies per bit
Type: RO

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**		**FALSH_N-P_AVAIL**	**Reserved**				**FLASH_C_FREE**
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**OOB_AVAIL**	**VWIRE_AVAIL**	**NP_AVAIL**	**PC_AVAIL**	**OOB_FREE**	**VWIRE_FREE**	**NP_FREE**	**PC_FREE**
Reset	0	0	0	0	1	1	1	1

Bit	Type	Description
15-14		**Reserved.**

13	RO	**FLASH_NP_AVAIL (Flash Channel Non-Posted Tx Available)**. This bit reflects the value of FLASH_TX_AVAIL bit in FLASHCTL register. It is reset by eSPI_RST or Core Reset. 0: Empty (default). 1: Available.
12-9		**Reserved.**
8	RO	**FLASH_C_FREE (Flash Channel Completion Rx Available)**. This bit is always 1 (i.e., "free").
7	RO	**OOB_AVAIL (OOB Channel Posted Tx. Available)**. Reflects the value of OOB_AVAIL bit in OOBCTL register. This bit is reset by eSPI_RST or Core Reset. 0: Empty (default). 1: Available.
6	RO	VWIRE_AVAIL (Virtual Wire Channel Tx Available). This bit is set to 1 (by hardware) when one or more virtual wire events are pending. Otherwise, this bit is 0. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: No event is pending (default). 1: At least one virtual wire event is pending
5	RO	**NP_AVAIL (Peripheral Channel Non-Posted Tx Available).**This bit is always 0 because the module does not support bus mastering.
4	RO	**PC_AVAIL (Peripheral Channel Posted/Completion Tx. Available).** This bit is set to 1 (by hardware)when a Peripheral Channel Completion with optional data is available. This bit is reset to 0 when the Completion is transmitted or the Peripheral Channel is disabled. It is also reset by eSPI_RST or PLTRST or Core Reset. 0: Empty (default). 1: Available.
3	RO	**OOB_FREE (OOB Channel Posted Rx Free).** Reflects the value of OOB_FREE bit in OOBCTL register. (If CHAN_FREE_EN bit in TEST11 register is set to 1, while the OOB Channel is disabled (or not supported), this bit (but not OOB_FREE bit in OOBCTL register) is forced to 0.) This bit is reset by eSPI_RST or Core Reset. 0: Busy. 1: Free (default).
2	RO	**VWIRE_FREE (Virtual Wire Channel Rx Free)**. This bit is always 1 (i.e., "free").
1	RO	**NP_FREE (Peripheral Channel Non-Posted Rx. Free)**. (If CHAN_FREE_EN bit in TEST11 register is set to 1, while the Peripheral Channel is disabled (or not supported), this bit is forced to 0.) This bit is set to its default value by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST. 0: Peripheral channel Non-Posted queue is full. Module cannot accept Non-Posted requests. 1: Peripheral channel Non-Posted queue has a place for one Non-Posted request (default).
0	RO	**PC_FREE (Peripheral Channel Posted Rx Free)**. (If CHAN_FREE_EN bit in TEST11 register is set to 1, while the Peripheral Channel is disabled (or not supported), this bit is forced to 0.) This bit is set to its default value by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST. 0: Peripheral channel Posted queue is full. Module cannot accept more Posted requests. 1: Peripheral channel Posted queue has a place for one Posted request (default).

16.11.3 Device Identification Register

Offset: 04h

Reset: Core Reset

Type: RO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**Reserved**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**Reserved**								**Version ID**							
Reset	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Bit	Type	Description
31-8		**Reserved.**
7-0	RO	**Version ID (Version ID)**. Reflects the value of ID field in ESPIID register

16.11.4General Capabilities and Configuration Register

Offset: 08h

Reset: Varies per bit

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**CRE Checking Enable**	**Response Modifier Enable**	**Reserved**	**$\overline{\text{ALERT}}$ Mode**	**I/O Mode Select**		**I/O Mode Support**	
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
Name(all)	**Open-Drain $\overline{\text{ALERT}}$ Select**	**Operating Frequency**			**Open-Drain $\overline{\text{ALERT}}$ Support**	**Maximum Frequency Supported**		
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Maximum WAIT_STATE Allowed**				**Reserved**			
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**Reserved**				**Flash Chan. Supported**	**OOB Chan. Supported**	**VW Chan. Supported**	**Periph. Chan. Supported**
Reset	0	0	0	0	0	0	1	1

Bit	Type	Description
31	R/W	**CRC Checking Enable (CRC Checking Enable)**. This bit is reflected in CRC_CHK_EN bit in ESPICFG register. (The setting of this bit does not affect the behavior of CRCERR bit in ESPIERR register.) This bit is reset by V_{CC} Power-Up reset, $\overline{\text{VCC_RST}}$ reset, e$\overline{\text{SPI_RST}}$ or in-band RESET command. 0: CRC checking is disabled (default).

		1: CRC checking is enabled.
30	R/W	**Response Modifier Enable (Response Modifier Enable).**This bit is ignored by the module, because completion appending is not supported. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command.
29	R/W	**Reserved.**
28	R/W	ALERT Mode (Alert Mode). Reflects ALERTMODE bit in ESPICFG register. This bit is reset by eSPI_RST or in-band RESET command. 0: ALERT is multiplexed with eSPI_IO1 (default). 1: ALERT is generated via eSPI_ALERT pin.
27-26	R/W	I/O Mode Select (I/O Mode Select). Reflects IOMODESEL field in ESPICFG register. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command. **Bits** **27 26 I/O Mode** 0 0: Single I/O (default). 0 1: Dual I/O. 1 0: Quad I/O. 1 1: Reserved.
25-24	RO	**I/O Mode Support (/O Mode Support)**. Reflects IOMODE field in ESPICFG register. This field is reset by V_{CC} Power-Up reset or VCC_RST reset. **Bits** **25 24 I/O Mode** 0 0: Single I/O (default). 0 1: Single and Dual I/O. 1 0: Single and Quad I/O. 1 1: Single, Dual and Quad I/O.
23	R/W	**Open-Drain ALERT Select (Open-Drain ALERT Select).** This bit is reset by $_{VCC}$ Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command. (This bit does not affect the output buffer of the eSPI_IO1 signal, which is only open-drain when the eSPI_IO1 signal is used as ALERT indication.) 0: Push-pull eSPI_ALERT pin buffer (default). 1: Open-drain eSPI_ALERT pin buffer.
22-20	R/W	**Operating Frequency (Operating Frequency).** This field is reflected in OPERFREQ field of ESPICFG register. This field is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command. **Bits** **22 21 20 Frequency** 0 0 0: 20 MHz (default). 0 0 1: 25 MHz. 0 1 0: 33 MHz. 0 1 1: 50 MHz. 1 0 0: 66 MHz. Others: Reserved.
19	RO	Open-Drain ALERT Support (Open-Drain ALERT Support). This bit is always 1 (i.e., open-drain ALERT is supported).
18-16	RO	**Maximum Frequency Supported (Maximum Frequency Supported).** Reflects MAXFREQ field in ESPICFG register. This field is reset by V_{CC} Power-Up reset or VCC_RST reset. **Bits** **18 17 16 Frequency** 0 0 0: 20 MHz (default). 0 0 1: 25 MHz. 0 1 0: 33 MHz.

		0 1 1: 50 MHz. 1 0 0: 66 MHz. Others: Reserved.
15-12	R/W	**Maximum WAIT_STATE Allowed (Maximum WAIT_STATE Allowed).** This field is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command. **Bits** **15 14 13 12 Number of WAIT_STATE Cycles** 0 0 0 1: 1. 0 0 1 0: 2. … 1 1 1 1: 15. 0 0 0 0: 16 (default).
11-4		**Reserved.**
3	RO	**Flash Access Channel Supported (Flash Access Channel Supported).** Indicates module support of the Flash Access Channel. It reflects FLASHCHN_SUPP bit in ESPICFG register. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Channel is not supported (default). 1: Channel is supported.
2	RO	**OOB Channel Supported (OOB Channel Supported).** Indicates module support of the OOB Channel. It reflects the OOBCHN_SUPP bit in ESPICFG register. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Channel is not supported (default). 1: Channel is supported.
1	RO	**Virtual Wire Channel Supported (Virtual Wire Channel Supported).** Indicates module support of the Virtual Wire Channel. It reflects VWCHN_SUPP bit in ESPICFG register. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Channel is not supported. 1: Channel is supported (default).
0	RO	**Peripheral Channel Supported (Peripheral Channel Supported).** Indicates module support of Peripheral Channel. It reflects the PCCHN_SUPP bit in ESPICFG register. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Channel is not supported. 1: Channel is supported (default).

16.11.5Channel 0 Capabilities and Configuration Register

Offset: 10h

Reset: Varies per bit

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8

Name(all)	**Reserved**	**Peripheral Channel Maximum Read Request Size**			**Reserved**	**Peripheral Channel Maximum Payload Size Selected**		
Reset	0	0	0	1	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Name(all)	**Reserved**	**Peripheral Channel Maximum Payload Size Supported**			**Reserved**	**Bus Master Enable**	**Peripheral Channel Ready**	**Peripheral Channel Enable**
Reset	0	0	0	1	0	0	0	1

Bit	Type	Description
31-15		**Reserved.**
14-12	R/W	**Peripheral Channel Maximum Read Request Size (Peripheral Channel Maximum Read Request Size).** This field has no effect on the module because the module does not support bus mastering. This field is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST.
11		**Reserved.**
10-8	R/W	**Peripheral Channel Maximum Payload Size Selected (Peripheral Channel Maximum Payload Size Selected).** This field is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST. **Bits** **10 9 8 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
7		**Reserved.**
6-4	RO	**Peripheral Channel Maximum Payload Size Supported (Peripheral Channel Maximum Payload Size Supported).** The module advertises 64 bytes (i.e., '001'). This field is reset by V_{CC} Power-Up reset orVCC_RST reset. **Bits** **6 5 4 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
3		**Reserved.**
2	R/W	**Bus Master Enable (Bus Master Enable).** This bit has no effect on the module because the module does not support bus mastering. The bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST.
1	RO	**Peripheral Channel Ready (Peripheral Channel Ready).** Reflects PCHANEN bit in ESPICFG register. This bit is reset by eSPI_RST or PLTRST or Core Reset. 0: Channel not ready (default). 1: Channel ready.
0	R/W	**Peripheral Channel Enable (Peripheral Channel Enable).** When this bit is cleared to 0, the Peripheral Channel is set to an idle state, (and all the queues and pending events are cleared). This bit is reflected in HPCHANEN bit of ESPICFG register. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST. 0: Channel disable.

		1: Channel enable (default).

16.11.6 Channel 1 Capabilities and Configuration Register

Offset: 20h
Reset: Varies per bit
Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**		**Operating Maximum Virtual Wire Count**					
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**		**Maximum Virtual Wire Count Supported**					
Reset	0	0	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
Name(all)	**Reserved**						**Virtual Wire Channel Ready**	**Virtual Wire Channel Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
31-22		**Reserved.**
21-16	R/W	**Operating Maximum Virtual Wire Count (Operating Maximum Virtual Wire Count).** This field is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. Count = [field_value] + 1
15-14		**Reserved.**
13-8	RO	**Maximum Virtual Wire Count Supported (Maximum Virtual Wire Count Supported).** Although the total number of wires actually implemented might be different from the value in this field, the module supports packets with any count. This field is reset by V_{CC} Power-Up reset or VCC_RST reset. Count = [field_value] + 1
7-2		**Reserved.**
1	RO	**Virtual Wire Channel Ready (Virtual Wire Channel Ready).** Reflects VWCHANEN bit in ESPICFG register. This bit is reset by eSPI_RST or Core Reset. 0: Channel not ready (default). 1: Channel ready.
0	R/W	**Virtual Wire Channel Enable (Virtual Wire Channel Enable).** When this bit is cleared to 0, the Virtual Wire Channel is set to an idle state, (and all the queues and pending events are cleared). This bit is reflected in HVWCHANEN bit of the ESPICFG register; however, it does not affect the state of the Virtual Wires. The bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: Channel disable (default). 1: Channel enable.

16.11.7 Channel 2 Capabilities and Configuration Register

Offset: 30h
Reset: Varies per bit
Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**					**OOB Message Channel Maximum Payload Size Selected**		
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Name(all)	**Reserved**	**OOB Message Channel Maximum Payload Size Supported**			**Reserved**		**OOB Message Channel Ready**	**OOB Message Channel Enable**
Reset	0	0	0	1	0	0	0	0

Bit	Type	Description
31-11		**Reserved.**
10-8	R/W	**OOB Message Channel Maximum Payload Size Selected (OOB Message Channel Maximum Payload Size Selected).** This field is reflected in OOBPLSIZE field of OOBCTL register; however, it has no effect on the eSPI_SIF module behavior since the maximum supported payload size is 64 bytes the minimal possible configuration). The field is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST. **Bits** **10 9 8 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
7		**Reserved.**
6-4	RO	**OOB Message Channel Maximum Payload Size Supported (OOB Message Channel Maximum Payload Size Supported).** The module advertises 64 bytes (i.e., '001'). This field is reset by V_{CC} Power-Up reset or VCC_RST reset. **Bits** **6 5 4 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
3-2		**Reserved**

1	RO	**OOB Message Channel Ready (OOB Message Channel Ready).** Reflects OOBCHANEN bit in ESPICFG register. This bit is reset by eSPI_RST or Core Reset. 0: Channel not ready (default). 1: Channel ready.
0	R/W	**OOB Message Channel Enable (OOB Message Channel Enable).** When this bit is cleared to 0, the OOB Channel is set to an idle state, (and all the queues and pending events are cleared). This bit is reflected in HOOBCHANEN bit of ESPICFG register. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: Channel disable (default). 1: Channel enable.

16.11.8 Channel 3 Capabilities and Configuration Register

Offset: 40h

Reset: Varies per bit

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**	**Flash Access Channel Maximum Read Request Size**			**Flash Sharing Mode**	**Flash Access Channel Maximum Payload Size Selected**		
Reset	0	0	0	1	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Name(all)	**Flash Access Channel Maximum Payload Size Supported**			**Flash Block Erase Size**			**Flash Access Channel Ready**	**Flash Access Channel Enable**
Reset	0	0	1	0	0	1	0	0

Bit	Type	Description
31-15		**Reserved.**
14-12	R/W	**Flash Access Channel Maximum Read Request Size (Flash Access Channel Maximum Read Request Size).** This field is reflected in FLASHREQSIZE field of FLASHCFG register. The field is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. **Bits** **14 13 12 Read Request Size** 0 0 0: Reserved. 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes.

		1 0 0: 512 bytes. 1 0 1: 1024 bytes. 1 1 0: 2048 bytes. 1 1 1: 4096 bytes.
11	RO	**Flash Sharing Mode (Flash Sharing Mode).** 0: Master-Attached Flash sharing (default). 1: Slave-Attached Flash sharing - not used in NPCX667K.
10-8	R/W	**Flash Access Channel Maximum Payload Size Selected (Flash Access Channel Maximum Payload Size Selected).** This field is reflected in FLASHPLSIZE field of FLASHCFG register. The field is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. **Bits** **10 9 8 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
7-5	RO	**Flash Access Channel Maximum Payload Size Supported (Flash Access Channel Maximum Payload Size Supported)**. The module advertises 64 bytes (i.e., '001'). This field is reset by V_{CC} Power-Up reset or VCC_RST reset. **Bits** **7 6 5 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
4-2	R/W	**Flash Block Erase Size (Flash Block Erase Size).** This field is reflected in FLASHBLERSSIZE field of FLASHCFG register. This field is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. **Bits** **4 3 2 Block Erase Size** 0 0 0: Reserved. 0 0 1: 4 Kbytes (default). 0 1 0: 64 Kbytes. 0 1 1: Both 4 Kbytes and 64 Kbytes. 1 0 0: 128 Kbytes. 1 0 1: 256 Kbytes. Others: Reserved.
1	RO	**Flash Access Channel Ready (Flash Access Channel Ready).** Reflects FLASHCHANEN bit in ESPICFG register. This bit is reset by eSPI_RST or Core Reset. 0: Channel not ready (default). 1: Channel ready.
0	R/W	**Flash Access Channel Enable (Flash Access Channel Enable).** When this bit is cleared to 0, the Flash Access Channel is set to an idle state, (and all the queues and pending events are leared). This bit is reflected in HFLASHCHANEN bit of the ESPICFG register. The bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: Channel disable (default). 1: Channel enable.

16.12 eSPI_SIF Core Registers

All Core registers are 32 bits wide and must be accessed as DWord. The registers are assembled in groups: one

group for common registers and one group for each channel, except for the Peripheral Channel, which does not require registers. Un- less otherwise stated, all reserved locations return 0 when read.

For a summary of the abbreviations used for Register Type. (The allocated address range is B000h - BFFFh.)

16.12.1 eSPI_SIF Core Register Map

Base address: B000h

Offset	Mnemonic	Register Name	Size	Type
Common Registers				
00h	ESPIID	eSPI Identification	Dword	Varies per bit
04h	ESPICFG	eSPI Configuration	Dword	Varies per bit
08h	ESPISTS	eSPI Status	Dword	R/W1C
0Ch	ESPIIE	eSPI Interrupt Enable	Dword	R/W
14h	VWREGIDX	Virtual Wire Register Index	Dword	R/W
18h	VWREGDATA	Virtual Wire Register Data	Dword	R/W
24h	OOBCTL	OOB Channel Control	Dword	Varies per bit
30h	FLASHCRC	Flash CRC/Checksum	Dword	R/W
34h	FLASHCFG	Flash Channel Configuration	Dword	RO
38h	FLASHCTL	Flash Channel Control	Dword	Varies per bit
3Ch	ESPIERR	eSPI Error Status	Dword	R/W1C
Virtual Wire Channel Rigisters				
100h-127h	VWEVSM0-9	Virtual Wire Event Slave-to-Master 0-9	Dword	Varies per bit
140h-16Fh	VWEVMS0-11	Virtual Wire Event Master-to-Slave 0-11	Dword	Varies per bit
208h	VWEVSMTYPE	Virtual Wire Event Slave-to-Master Type	Dword	Varies per bit
2F8h	VWPING	Virtual Wire Programmable Index Group	Dword	Varies per bit
2FCh	VWCTL	Virtual Wire Channel Control	Dword	R/W
OOB Channel Regitsters				
300h-34Fh	OOBRXBUF0-19	OOB Receive Buffer 0-19	Dword	RO
380h-3CFh	OOBTXBUF0-19	OOB Transmit Buffer 0-19	Dword	WO
3FCh	OOBCTL	OOB Channel Control	Dword	Varies per bit
Flash Access Channel Register				
400h-443h	FLASHRXBUF0-16	Flash Receive Buffer 0-16	Dword	RO
480h-497h	FLASHTXBUF0-5	Flash Transmit Buffer 0-5	Dword	WO
4F4h	FLASHCRC	Flash CRC/Checksum	Dword	R/W
4F8h	FLASHCFG	Flash Channel Configuration	Dword	RO
4FCH	FLASHCTL	Flash Channel Control	Dword	Varies per bit

16.12.2 eSPI Identification Register (ESPIID)

Offset: 00h

Reset: Core Reset

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**Reserved**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	Reserved (VERSION)								ID							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit	Type	Description
31-8		**Reserved.**
15-8	RO	**VERSION (Module Hardware Version).** Change this field for every new version of hardware, including configuration changes. In NPCX667K this field is 02h.
7-0	R/W	**ID (Host Version ID).** This field is reflected in Version ID field of the (Host) Device Identification register.

16.12.3 eSPI Configuration Register (ESPICFG)

Offset: 04h

Reset: Varies per bit

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	Reserved				FLASHCHIN_SUPP	OOBCHN_SUPP	VWCHN_SUPP	PCCHN_SUPP
Reset	0	0	0	0	1	1	1	1

Bit	23	22	21	20	19	18	17	16
Name(all)	CRC_CHK_EN	ALERTMODE	IOMODESEL		OPFREQ			Reserved
Reset	0	0	0	0	0	0	1	1

Bit	15	14	13	12	11	10	9	8
Name(all)	Reserved			MAXFREQ			IOMODE	
Reset	0	0	0	0	1	0	1	1

Bit	7	6	5	4	3	2	1	0
Name(all)	HFLASH-CHANEN	HOOB-CHANEN	HVW CHANEN	HP CHANEN	FLASH-CHANEN	OOB-CHANEN	VWCHANEN	PCHANEN
Reset	0	0	0	1	0	0	0	0

Bit	Type	Description
31-28		**Reserved.**
27	R/W	**FLASHCHN_SUPP (Flash Access Channel Supported).** This bit is reflected in Flash Access Channel Supported bit of General Capabilities and Configuration register. The bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Flash Access Channel is not supported (default). 1: Flash Access Channel is supported.
26	R/W	**OOBCHN_SUPP (OOB Channel Supported).** This bit is reflected in OOB Channel Supported bit of General Capabilities and Configuration register. The bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: OOB Channel is not supported (default). 1: OOB Channel is supported.
25	R/W	**VWCHN_SUPP (Virtual Wire Channel Supported).** This bit is reflected in Virtual Wire

		Channel Supported bit of General Capabilities and Configuration register. The bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Virtual Wire Channel is not supported. 1: Virtual Wire Channel is supported (default).
24	R/W	**PCCHN_SUPP (Peripheral Channel Supported).** This bit is reflected in Peripheral Channel Supported bit of General Capabilities and Configuration register. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Peripheral Channel is not supported. 1: Peripheral Channel is supported (default).
23	RO	**CRC_CHK_EN (CRC Checking Enable).** Reflects the CRC Checking Enable bit in the General Capabilities and Configuration register. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command. 0: CRC checking is disabled (default). 1: CRC checking is enabled.
22	RO	**ALERTMODE (ALERT Mode).** Reflects the ALERT Mode bit in the General Capabilities and Configuration register. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in- band RESET command. 0: ALERT is multiplexed with eSPI_IO1 (default). 1: ALERT is generated via eSPI_ALERT pin.
21-20	RO	**IOMODESEL (I/O Mode Select).** Reflects the I/O Mode Select field in the General Capabilities and Configuration register. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in- band RESET Command. **Bits** **21 20 I/O Mode** 0 0: Single I/O (default). 0 1: Dual I/O. 1 0: Quad I/O. 1 1: Reserved.
19-17	RO	**OPFREQ (Operating Frequency).** Reflects the Operating Frequency field in the General Capabilities and Configuration register. This field is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or in-band RESET command. **Bits** **19 18 17 Frequency** 0 0 0: 20 MHz (default). 0 0 1: 25 MHz. 0 1 0: 33 MHz. 0 1 1: 50 MHz. 1 0 0: 66 MHz. Others: Reserved.
16-13		**Reserved**
12-10	R/W	**MAXFREQ (Maximum Frequency Supported).** This field is reflected in the Maximum Frequency Supported field of the General Capabilities and Configuration register. The field is reset by V_{CC} Power-Up reset or VCC_RST reset. **Bits** **12 11 10 Frequency** 0 0 0: 20 MHz (default). 0 0 1: 25 MHz. 0 1 0: 33 MHz. 0 1 1: 50 MHz. 1 0 0: 66 MHz. Others: Reserved.
9-8	R/W	**IOMODE (I/O mode support).** This field is reflected in the I/O Mode Support field of the General Capabilities and Configuration register. This field is reset by V_{CC} Power-Up reset or

		VCC_RST reset. **Bits** **9 8 I/O Mode** 0 0: Single I/O (default). 0 1: Single and Dual I/O. 1 0: Single and Quad I/O. 1 1: Single, Dual and Quad I/O.
7	RO	**HFLASHCHANEN (Host Flash Access Channel Enable).** Reflects the Flash Access Channel Enable bit of Channel 3 Capabilities and Configuration register. The Flash Access Channel is enabled if this bit and FLASHCHANEN bit are both set to 1. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: Flash Access channel is disabled (default). 1: Flash Access channel is enabled from the Host side.
6	RO	**HOOBCHANEN (Host OOB Channel Enable).** Reflects the OOB Message Channel Enable bit of Channel 2 Capabilities and Configuration register. The OOB Channel is enabled if this bit and OOBCHANEN bit are both set to 1. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: OOB channel is disabled (default). 1: OOB channel is enabled from the Host side.
5	RO	**HVWCHANEN (Host Virtual Wire Channel Enable).** Reflects the Virtual Wire Channel Enable bit of Channel 1 Capabilities and Configuration register. The Virtual Wire Channel is enabled if this bit and VWCHANEN bit are both set to 1. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. 0: Virtual Wire channel is disabled (default). 1: Virtual Wire channel is enabled from the Host side.
4	RO	**HPCHANEN (Host Peripheral Channel Enable).** Reflects the Peripheral Channel Enable bit of Channel 0 Capabilities and Configuration register. The Peripheral Channel is enabled if this bit and PCHANEN bit are both set to 1. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST. 0: Peripheral channel is disabled. 1: Peripheral channel is enabled from the Host side (default).
3	R/W	**FLASHCHANEN (Core Flash Access Channel Enable).** This bit is reflected in Flash Access Channel Ready bit of Channel 3 Capabilities and Configuration register. The Flash Access Channel is enabled if this bit and HFLASHCHANEN bit are both set to 1. This bit is reset by eSPI_RST or Core Reset. 0: Flash Access channel is disabled (default). 1: Flash Access channel is enabled from the Core side.
2	R/W	**OOBCHANEN (Core OOB Channel Enable).** This bit is reflected in OOB Message Channel Ready bit of Channel 2 Capabilities and Configuration register. The OOB Channel is enabled if this bit and HOOBCHANEN bit are both set to 1. This bit is reset by eSPI_RST or Core Reset. 0: OOB channel is disabled (default). 1: OOB channel is enabled from the Core side.
1	R/W	**VWCHANEN (Core Virtual Wire Channel Enable).** This bit is reflected in Virtual Wire Channel Ready bit of Channel 1 Capabilities and Configuration register. The Virtual Wire Channel is enabled if this bit and HVWCHANEN bit are both set to 1. This bit is reset by eSPI_RST or Core Reset. 0: Virtual Wire channel is disabled (default). 1: Virtual Wire channel is enabled from the Core side.
0	R/W	**PCHANEN (Core Peripheral Channel Enable).** This bit is reflected in Peripheral Channel Ready bit of Channel 0 Capabilities and Configuration register. The Peripheral Channel is

		enabled if this bit and HPCHANEN bit are both set to 1. This bit is reset by eSPI_RST or PLTRST or Core Reset. 0: Peripheral channel is disabled (default). 1: Peripheral channel is enabled from the Core side.

16.12.4 eSPI Status Register (ESPISTS)

Offset: 08h

Reset: Core Reset

Type: R/W1C

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)		**Reserved**						**AMDONE**
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**AMERR**	**Reserved**				**PLTRST**	**ESPIRST**	**VWUPD**
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	10
Name(all)	**DFRD**	**PERACC**	**Reserved**	**FLASHRX**	**OOBRX**	**BERR**	**CFGUPD**	**IBRST**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
31-17		**Reserved.**
16	R/W1C	**AMDONE (Automatic Mode Transfer Done).** When set to 1, this bit indicates that the Automatic mode transfer was completed and all the data was transferred from the two receive buffers. If enabled, an interrupt is generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. (Note that this bit is operational regardless of whether DMA is used or not.) 0: Automatic mode in progress or idle (default). 1: Automatic mode complete.
15	R/W1C	**AMERR (Automatic Mode Transfer Error).** When set to 1, this bit indicates that the Automatic mode transfer was aborted with error. If enabled, an interrupt is generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: Successful transfer or Automatic mode idle (default). 1: Automatic mode transfer failed.
14-11		**Reserved**
10	R/W1C	**PLTRST ($\overline{\text{PLTRST}}$ Activated).** When set to 1, this bit indicates that the $\overline{\text{PLTRST}}$ Virtual Wire was activated. If enabled, an interrupt is generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: $\overline{\text{PLTRST}}$ Virtual Wire is 1 (deasserted) or the bit was cleared (default). 1: $\overline{\text{PLTRST}}$ Virtual Wire was set to 0 (asserted).
9	R/W1C	**ESPIRST ($\overline{\text{eSPI_RST}}$ Activated).** When set to 1, this bit indicates that the $\overline{\text{eSPI_RST}}$ signal

		was activated. If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: eSPI_RST signal is high or the bit was cleared (default). 1: eSPI_RST signal was asserted (low).
8	R/W1C	**VWUPD (Virtual Wire Updated).** When set to 1, this bit indicates that the state of one of configured Master-to-Slave virtual wires was changed. If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No change to Master-to-Slave Virtual Wires (default). 1: Master-to-Slave Virtual Wires were updated.
7	R/W1C	**DFRD (Peripheral Channel Transaction Deferred).** When set to 1, this bit indicates that a Peripheral Channel transaction was deferred. If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: Peripheral Channel transactions end without DEFER response (default). 1: A Peripheral Channel transaction was ended with DEFER response.
6	R/W1C	**PERACC (Peripheral Channel Access Detected).** When set to 1, this bit indicates that a Peripheral Channel transaction occurred. If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No Peripheral Channel transactions (default). 1: A Peripheral Channel transaction occurred.
5		**Reserved**
4	R/W1C	**FLASHRX (Flash Data Received).** When set to 1, this bit indicates that a Flash Access Completion packet was received (both in Manual mode and in Automatic mode). If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. (Note that this bit is also set to 1 when an Unsuccessful Completion Without Data is received in response to a GET_FLASH_NP command. This indicates that the previous flash request was completed, though with an error.) 0: No Flash Access transaction received (default). 1: The Flash Access transaction (with or without data payload) was received.
3	R/W1C	**OOBRX (OOB Data Received).** When set to 1, this bit indicates that an OOB Channel packet was received. If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No OOB Channel packet received (default). 1: An OOB Channel packet was received.
2	R/W1C	**BERR (eSPI Bus Error).** When set to 1, this bit indicates that an error was detected on eSPI interface one of the bits in ESPIERR register is set). If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No eSPI bus error detected (default). 1: An eSPI bus error was detected.
1	R/W1C	**CFGUPD (eSPI Configuration Updated).** When set to 1, this bit indicates that the Host wrote data to one or more configuration registers (not necessarily changing the register contents). If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No change to Host configuration registers (default). 1: One or more Host configuration register were written.
0	R/W1C	**IBRST (In-Band Reset Command Received).** When set to 1, this bit indicates that an in-band RESET Command was received. If enabled, an interrupt and/or wake-up are generated when this bit is set to 1. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No in-band RESET Command was received (default).

		1: An in-band RESET Command was received.

16.12.5 eSPI Interrupt Enable Register (ESPIIE)

Offset: 0Ch

Reset: Core Reset

Type: R/W

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)		**Reserved**						**AMODONEIE**
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**AMERRIE**	**Reserved**				**PLTRSTIE**	**ESPIRSTIE**	**VWUPDIE**
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**DFRDIE**	**PERACCIE**	**Reserved**	**FLASHRXIE**	**OOBRXIE**	**BERRIE**	**CFGUPDIE**	**IBRSTIE**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
31-17		**Reserved.**
16	R/W	**AMDONEIE (AMDONE Interrupt Enable).** When set to 1, this bit enables an interrupt when AMDONE bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if AMDONE bit is set to 1.
15	R/W	**AMERRIE (AMERR Interrupt Enable).** When set to 1, this bit enables an interrupt when AMERR bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if AMERR bit is set to 1.
14-11		**Reserved**
10	R/W	**PLTRSTIE (PLTRST Interrupt Enable).** When set to 1, this bit enables an interrupt when PLTRST bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if PLTRST bit is set to 1.
9	R/W	**ESPIRSTIE (eSPI_RST Interrupt Enable).** When set to 1, this bit enables an interrupt when ESPIRST bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if ESPIRST bit is set to 1.
8	R/W	**VWUPDIE (VWUPD Interrupt Enable).** When set to 1, this bit enables an interrupt when VWUPD bit in ESPISTS register is set to 1.

		0: Interrupt is disabled (default). 1: A Core interrupt is generated if VWUPD bit is set to 1.
7	R/W	**DFRDIE (DFRD Interrupt Enable).** When set to 1, this bit enables an interrupt when DFRD bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if DFRD bit is set to 1.
6	R/W	**PERACCIE (PERACC Interrupt Enable).** When set to 1, this bit enables an interrupt when PERACC bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if PERACC bit is set to 1.
5		**Reserved**
4	R/W	**FLASHRXIE (FLASHRX Interrupt Enable).** When set to 1, this bit enables an interrupt when FLASHRX bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if FLASHRX bit is set to 1.
3	R/W	**OOBRXIE (OOBRX Interrupt Enable).** When set to 1, this bit enables an interrupt when OOBRX bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if OOBRX bit is set to 1.
2	R/W	**BERRIE (BERR Interrupt Enable).** When set to 1, this bit enables an interrupt when BERR bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if BERR bit is set to 1.
1	R/W	**CFGUPDIE (CFGUPD Interrupt Enable).**When set to 1, this bit enables an interrupt when CFGUPD bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if CFGUPD bit is set to 1.
0	R/W	**IBRSTIE (IBRST Interrupt Enable).** When set to 1, this bit enables an interrupt when IBRST bit in ESPISTS register is set to 1. 0: Interrupt is disabled (default). 1: A Core interrupt is generated if IBRST bit is set to 1.

16.12.6 Virtual Wire Register Index Register (VWREGIDX)

Offset: 14h
Reset: Core Reset
Type: R/W

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**Reserved**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**Reserved**				**VWREGIDX**										**Reserved ('00')**	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Type	Description
31-10		**Reserved.**
11-2	R/W	**VWREGIDX (Virtual Wire Register Index).** Provides indexed access to Virtual Wire Channel

		registers. For indexed access to the Virtual Wire Channel registers, write the required register offset (as specified in section “eSPI_SIF Core Register Map”) to this field, and then access the Virtual Wire Channel register through VWREGDATA register. Writing an offset value outside Virtual Wire Channel registers space is illegal and gives unpredictable results.
1-0		**Reserved.** (These bits must be ‘00’.)

16.12.7 Virtual Wire Register Data Register (VWREGDATA)

Offset: 18h
Reset: N/A
Type: R/W

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**VWREGDATA**															
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**VWREGDATA**															
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	Type	Description
31-0	R/W	**VWREGDATA (Virtual Wire Register Data).** Data of the register pointed to by VWREGIDX register.

16.12.8 OOB Channel Control Register (OOBCTL)

Offset: 24h (Option 1), 3FCh (Option 2)
Reset: Varies per bit
Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**			**OOBPLSIZE**			**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**Reserved**					**RSTBUF HEADS**	**OOB_AVAIL**	**OOB_FREE**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
31-13		**Reserved.**
12-10	RO	**OOBPLSIZE (OOB Channel Maximum Payload Size).** Reflects the value of the OOB Channel Maximum Payload Size field in the (Host) Channel 2 Capabilities and Configurations register. This field

		is reset by eSPI_RST. **Bits** **12 11 10 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
9-3		**Reserved.**
2	WO	**RSTBUFHEADS (Reset Buffer Heads).** When this bit is set to 1, the Read Pointer for OOBRXRDHEAD register is set to OOBRXBUF0 and the Write Pointer for OOBTXWRHEAD register is set to OOBTXBUF0.Writing 0 is ignored. Read always returns 0. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Ignored (default). 1: Reset pointers.
1	R/W1S	**OOB_AVAIL (OOB Transmit Queue Available).** The Core firmware must set this bit after writing data to the OOB transmit buffer registers, to signal the availability of a new OOB packet to the Host. The bit is cleared by the hardware following the successful completion of the GET_OOB command. (Actually, OOB_AVAIL bit is already cleared to 0 after the CRC byte of the GET_OOB transaction command phase, regardless of the "successful completion" of the command.) Writing 1 sets the bit to 1; writing 0 is ignored. This bit is reflected in OOB_AVAIL bit of the (Host) STATUS register. This bit is reset by eSPI_RST or Core Reset. 0: Transmit queue empty (default). 1: Transmit queue full.
0	R/W1S	**OOB_FREE (OOB Receive Queue Free).** This bit is cleared to 0 by hardware when a PUT_OOB command is received. The Core firmware must set this bit to 1 after reading data from the OOB receive buffer registers. Writing 1 sets the bit to 1; writing 0 is ignored. This bit is reflected in OOB_FREE bit of the (Host) STATUS register, however this bit is not forced to 0 when the OOB Channel is disabled or not supported, regardless of the register value of CHAN_FREE_EN bit in TEST11. This bit is reset by eSPI_RST or Core Reset. 0: Receive queue full. 1: Receive queue empty (default).

16.12.9 Flash CRC/Checksum Register (FLASHCRC) - Not Used

Offset: 30h (Option 1), 4F4h (Option 2)
Reset: Core Reset
Type: R/W

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**CRC_CKSM**															
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**CRC_CKSM**															
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	Type	Description
31-0	RW	**CRC_CKSM (CRC/Checksum Result).** The Core firmware must write the CRC/Checksum to this register, before it starts to read the Master-Attached Access Flash Channel data from the receive buffer.When all the received data is read, this field holds the CRC or Checksum of the data

16.12.10 Flash Channel Configuration Register (FLASHCFG)

Offset: 34h (Option 1), 4F8h (Option 2)

Reset: Varies per bit
Type: RO

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**FLASHREQSIZE**			**FLASHPLSIZE**			**FLASHBLERSSIZE**	
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**FLASHBLERSSIZE**	**Reserved**						
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
31-16		**Reserved.**
15-13	RO	**FLASHREQSIZE (Flash Access Channel Maximum Read Request Size).** Reflects the value of the Flash Access Channel Maximum Read Request Size field in the (Host) Channel 3 Capabilities and Configurations register. This field is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. **Bits** **15 14 13 Read Request Size** 0 0 0: Reserved. 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. 1 0 0: 512 bytes. 1 0 1: 1024 bytes. 1 1 0: 2048 bytes. 1 1 1: 4096 bytes.
12-10	RO	**FLASHPLSIZE (Flash Access Channel Maximum Payload Size).** Reflects the value of the Flash Access Channel Maximum Payload Size field in the (Host) Channel 3 Capabilities and Configurations register. This field is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST. **Bits** **12 11 10 Payload Size** 0 0 1: 64 bytes (default). 0 1 0: 128 bytes. 0 1 1: 256 bytes. Others: Reserved.
9-7	RO	**FLASHBLERSSIZE (Flash Access Channel Block Erase Size).**Reflects the value of the Flash Block Erase Size field in the (Host) Channel 3 Capabilities and Configurations register. This field is reset by eSPI_RST. **Bits** **9 8 7 Block Erase Size** 0 0 0: Reserved. 0 0 1: 4 Kbytes (default). 0 1 0: 64 Kbytes. 0 1 1: Both 4 Kbytes and 64 Kbytes. 1 0 0: 128 Kbytes.

		1 0 1: 256 Kbytes. Others: Reserved.
6-0		**Reserved.**

16.12.11 Flash Channel Control Register (FLASHCTL)

Offset: 38h (Option 1), 4FCh (Option 2)

Reset: Varies per bit

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**						**AMT_BFULL**	**AMTEN**
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**		**RSTBUF HEADS**	**AMTSIZE**				
Name(Eng)	**CHKSUMSEL**	**CRCEN**	**RSTBUF HEADS**	**AMTSIZE**				
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**AMTSIZE**			**DMATHRESH**		**STRPHDR**	**FLASH TX_AVAIL**	**Reserved**
Reset	0	0	0	0	0	0	0	1

Bit	Type	Description
31-18		**Reserved.**
17	RO	**AMT_BFULL (Automatic Mode Receive Buffer Full).** When set to 1, this bit indicates that at least one of the two Flash Access Rx buffers (of the receive Queue) is full, i.e. contains 64 bytes of received data. This bit is set to 0 when the total received data in the two buffers is less than 64 bytes. It is also set to 0 when AMTEN bit is 0 (i.e., in Manual mode) and when a Core Reset occurs. AMT_BFULL bit should be used only in Automatic mode, when not working with DMA. For correct operation, the firmware must read a full buffer (i.e., 64 bytes) from the FLASHRXBUFn DWord registers.(An internal indication is set to 1 when a Flash Access Rx buffer becomes full (i.e., when the 64th payload data byte is received). It is cleared to 0 by a Core read from the respective buffer. There are two internal indications, one for each Flash Access Rx buffer. AMT_BFULL bit is controlled by the OR between these internal indications; therefore, the bit becomes 0 only when **both** indications become 0.) 0: The total received data in the two buffers is less than 64 bytes (default). 1: The total received data in the two buffers is 64 bytes or more.
16	R/W	**AMTEN (Automatic Mode Enable).** Controls Automatic/Manual mode selection . This bit is set to 0 when the AMERR bit in ESPISTS register is set to 1 (i.e., when an Automatic mode error occurs). It is **not** allowed to set this bit to 0 (i.e., to terminate the Automatic mode) while Automatic mode operation is in progress (i.e., while AMDONE bit in ESPISTS register is 0). This bit is reset by Core Reset. (When Manual mode is selected, the Automatic mode Tag generation, block counter and request generation are disabled. Note, however, that setting AMTEN bit to 0 does not affect the pointers of the Transmit and

		Receive buffers.) 0: Manual mode (default). 1: Automatic mode.
15-14		**Reserved.**
15	R/W	**CHKSUMSEL (Checksum Select).** When CRCEN bit is set to 1, this bit selects either Checksum or CRC on-the fly calculation. The bit is reset by Core Reset. 0: On-the-fly CRC calculation (default). 1: On-the-fly Checksum calculation.
14	R/W	**CRCEN (CRC/Checksum Enable).** When this bit is set to 1, it enables on-the-fly CRC/Checksum calculation for data read from Flash Channel Receive Buffer. The bit is reset by Core Reset. 0: CRC/Checksum calculation for flash channel data is disabled. 1: CRC/Checksum calculation for flash channel data is enabled.
13	WO	**RSTBUFHEADS (Reset Buffer Heads).** When this bit is set to 1, the Read Pointer for FLASHRXRDHEAD register is set to FLASHRXBUF0 and the Write Pointer for FLASHTXWRHEAD register is set to FLASHTXBUF0. Writing 0 is ignored. Read always returns 0. This bit is reset by VCC_RST reset or Core Reset. This bit must not be used to reset the Read and Write pointers during Automatic mode (i.e., while AMTEN bit is set to 1). 0: Ignored (default). 1: Reset pointers.
12-5	R/W	**AMTSIZE (Automatic Mode Transfer Size).** Defines the transfer size in Automatic mode, in multiples of 64 bytes. This is a 0-based count: a value of 0 indicates a size of 1; a value of FFh indicates a size of 256. This field is reset by Core Reset. This field must **not** be changed during Automatic mode (i.e., while AMTEN bit is set to 1).
4-3	R/W	**DMATHRESH (DMA Request Threshold).** Defines a threshold value of the Flash Receive buffer, above which a DMA request is asserted. If the DMA transfer in Automatic mode is used (i.e., it the GDMA controller is configured and enabled), DMATHRESH field must be set to either '01' or '11'. This field is reset by eSPI_RST or Core Reset. **Bits** **4 3 DMA Threshold Size** 0 0: DMA request is disabled (default). 0 1: Reserved. 1 0: 4 bytes - for 4-byte or 16-byte aligned destination address. 1 1: 16 bytes - **only** for 16-byte aligned destination address.
2	R/W	**STRPHDR (Strip Header).** When this bit is set to 1, the packet header is not stored in the Flash Access Channel Receive buffer. This bit may be changed only when there is no flash transaction in progress or pending in either Manual or Automatic mode (i.e., when the Master-Attached Flash Access Channel is idle). This bit is reset by Core Reset. 0: The buffer contains the packet header and the payload (default). 1: The buffer contains only the payload.
1	R/W1S	**FLASH_TX_AVAIL (Flash Access Transmit Queue Available).** The Core firmware must set this bit after writing data to the Flash Access Channel transmit buffer registers, to signal the availability of a new Master-Attached flash request to the Host. The bit is cleared by the hardware following the successful completion of the GET_FLASH_NP or the GET_FLASH_C command. Writing 1 sets the bit to 1; writing 0 is ignored. This bit is reflected in FLASH_NP_AVAIL bit of the (Host) STATUS register. This bit is reset by eSPI_RST reset or Core Reset. 0: Transmit queue empty (default). 1: Transmit queue full
0		**Reserved.**

16.12.12 eSPI Error Status Register (ESPIERR)

Offset: 3Ch

Reset: Core Reset

Type: R/W1C

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**				**VWERR**	**EXTRACYC**	**UNCMD**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**PCBADALN**	**NPBADALN**	**BADSIZE**	**PROTERR**	**AMCOMP**	**CRCERR**	**INVCYC**	**INVCMD**
Reset	0	0	0	0	0	0	0	1

Bit	Type	Description
31-12		**Reserved.**
10	R/W1C	**VWERR (Virtual Channel Access Error).** When this bit is set to 1, it indicates that the current PUT_VWIRE transaction either has a Virtual Wire Count higher than the Operating Maximum Virtual Wire Count or it accesses an unsupported Virtual Wire Index (this includes indexes with INDEX_EN bit set to 0). This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
10	R/W1C	**EXTRACYC (Extra eSPI Clock Cycles).** When this bit is set to 1, it indicates that additional clock cycles were received after the end of response phase while eSPI_CS was asserted. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
9	R/W1C	**UNCMD (Unsupported Command or Cycle Type).** When this bit is set to 1, it indicates that an unsupported command or an invalid cycle type was received during the current transaction. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
8		**Reserved.**
7	R/W1C	**PCBADALN (Posted Peripheral Channel Bad Address Alignment).** When this bit is set to 1, it indicates an error of the address alignment (i.e., the address crosses the 4 Kbyte boundary) during a Posted Peripheral Channel transaction. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
6	R/W1C	**NPBADALN (Non-Posted Peripheral Channel Bad Address Alignment).** When this bit is set to 1, it indicates an error of the address alignment (i.e., the address crosses the 4 Kbyte boundary) during a Non-Posted Peripheral Channel transaction. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected
5	R/W1C	**BADSIZE (Bad Size).** When this bit is set to 1, it indicates that the current transaction has a Payload

		size or a Read request size too big to fit into internal buffer. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
4	R/W1C	**PROTERR (Protocol Error).** When this bit is set to 1, it indicates that a GET command was received without the corresponding _FREE status bit set or a PUT command was received without the corresponding _AVAIL status bit set. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
3	R/W1C	**ABCOMP (Abnormal Completion).** When this bit is set to 1, it indicates that the eSPI transaction was ended abnormally (i.e., by an unexpected $\overline{\text{ESPI_CS}}$ deassertion). This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
2	R/W1C	**CRCERR (Transaction CRC Error).** When this bit is set to 1, it indicates that a CRC Error was detected in the current transaction. This bit is updated regardless of the setting of the CRC Checking Enable bit in General Capabilities and Configuration register. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
1	R/W1C	**INVCYC (Invalid Cycle Type).** When this bit is set to 1, it indicates that a invalid Cycle Type was received in the current transaction. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.
0	R/W1C	**INVCMD (Invalid Cycle Type).**When this bit is set to 1, it indicates that a invalid Command was received in the current transaction. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No error (default). 1: Error detected.

16.12.13 Virtual Wire Event Register Reset Values

The following table summarizes reset values for VWEVMSn and VWEVSMn registers. All the registers that do not have spe- cial reset value default to 0.

Table 50. Virtual Wire Event Register Reset Values

Register	Offset	ENESP	IE	ENPL	D/M	EN	Index							Valid				Wire				Hex Value
Bit		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VWEVMS0	140h	0	0	0	0	**1**	**0**	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0000 8200
VWEVMS1	144h	**1**[1]	0	N.A.[2]	0	**1**	0	0	0	0	0	**1**	**1**	0	0	0	0	0	0	0	0	0008 8300
VWEVMS2	148h	**1**	0	**1**	0	**1**	0	0	0	0	**1**	**1**	**1**	0	0	0	0	0	**1**	**1**	**0**	000A 8706
VWEVSM0	100h	N.A.	N.A	0	0	**1**	0	0	0	0	**1**	0	0	**1**	**1**	0	**1**	**1**	**1**	0	0	0000 84DC
VWEVSM1	104h	N.A.	N.A	0	0	**1**	0	0	0	0	**1**	0	**1**	**1**	**1**	**1**	**1**	0	0	0	0	0000 85F0
VWEVSM2	108h	N.A.	N.A	**1**	0	**1**	0	0	0	0	**1**	**1**	0	**1**	**1**	**1**	**1**	0	**1**	**1**	**1**	0002 86F7
VWEVMS3	14Ch	**1**	0	0	0	**1**	**1**	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0008 C100
VWEVMS4	150h	0	0	0	0	**1**	**1**	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0000 C200
VWEVMS5	154h	**1**	0	0	0	**1**	**1**	0	0	0	0	**1**	**1**	0	0	0	0	0	0	0	0	0008 C300
VWEVMS6	158h	**1**	0	0	0	**1**	**1**	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0008 C400
VWEVMS7	15Ch	**1**	0	**1**	0	**1**	**1**	0	0	0	**1**	**1**	**1**	0	0	0	0	0	0	0	0	000A C700
VWEVSM3	10Ch	N.A.	N.A	0	0	**1**	**1**	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0000 C010
VWEVSM4	110h	N.A.	N.A	0	0	**1**	**1**	0	0	0	**1**	0	**1**	**1**	**1**	**1**	**1**	0	0	0	0	0000 C5F0
VWEVSM5	114h	N.A.	N.A	0	0	**1**	**1**	0	0	0	**1**	**1**	0	**1**	**1**	**1**	**1**	0	0	0	0	0000 C6F0

Other		**1**	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0000 0000

1. ENESPIRST bit is reserved in VWEVMS1 register and must be set to 1 (its default value) (because VWEVMS1 is mapped to Index = 3, which includes the PLTRST, required to be set to its default value by eSPI_RST reset).
2. ENPLTRST bit is not available in VWEVMS1 register (because VWEVMS1 is mapped to Index = 3, which includes the PLTRST virtual wire).

16.12.14 Virtual Wire Event Slave-to-Master Register n (VWEVSMn), n = 0 – 9

Offset: 100h + n*4 with n =0 - 9
Reset: Varies per bit
Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**				**ENCDRST**	**Reserved**	**ENPLTRST**	**DIRTY**
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**INDEX_EN**	**INDEX**						
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**Wire 3-0 Valid**				**Wire 3-0**			
Reset	See table							

Bit	Type	Description
31-12		**Reserved.**
19	R/W	**ENCDRST (Enable Core Reset).** When set to 1, this bit enables the Wire 3-0 bits to be reset when Core Reset is asserted. This bit is reset by VCC Power-Up reset or VCC_RST reset. 0: Wire 3-0 bits are reset by eSPI_RST or PLTRST (according to ENPLTRST bit). 1: Wire 3-0 bits are reset by eSPI_RST, PLTRST (according to ENPLTRST bit) or Core Reset.
18		**Reserved.**
17	R/O	**ENPLTRST (Enable PLTRST).** When set to 1, this bit enables the Wire 3-0 bits to be reset when PLTRST is asserted. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Wire 3-0 bits are reset by eSPI_RST reset or Core Reset (according to ENCDRST bit). 1: Wire 3-0 bits are reset by eSPI_RST reset or Core Reset (according to ENCDRST bit) or **PLTRST**.
16		**DIRTY (Dirty).** This bit is set to 1 when at least one of the Wire 3-0 bits has changed (regardless of the cause of the change: the hardware signal changed, the Core wrote a different value to the bit or the bit was reset) and its respective Wire 3-0 Valid bit is 1. Note that DIRTY bit is not set if the Wire 3-0 bit change was caused by an enabled PLTRST reset. This bit is reset by V_{CC} Power-Up reset, VCC_RST reset or eSPI_RST reset. 0: The group was read by the Host after Wire 3-0 bits changed (default). 1: Wire 3-0 bits changed (regardless of the change cause)
15	R/W	**INDEX_EN (Index Enable).** Defines the index of the Virtual Wire group. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: The index is disabled. The hardware ignores the register contents. 1: The index is enabled (default).

14-8	R/W	**INDEX (Index Value).** Defines the lower 7 bits of the index of the Virtual Wire group. The upper bit (bit 8) is constant 0. Index values of 0 and 1 are illegal (they are used for interrupts). This field is reset by V_{CC} Power-Up reset or VCC_RST reset.
7-4	R/W	**Wire 3-0 Valid (Wire 3-0 Valid).** Each bit controls the "valid" state of the corresponding Wire 3-0 bit. When set to 1, this bit indicates that the corresponding Wire 3-0 bit is valid and its value should be accounted for. The Core firmware should initialize and maintain this field. These bits are reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Wire n is invalid. 1: Wire n is valid.
3-0	R/W	**Wire 3-0 (Wire 3-0).** Each bit indicates the state of a Virtual Wire of the group. These bits are reset by eSPI_RST or PLTRST (according to ENPLTRST bit) or Core Reset (according to ENCDRST bit).

16.12.15 Virtual Wire Event Master-to-Slave Register n (VWEVMSn), n = 0 – 11

Offset: 140h + n*4 with n =0 - 11

Reset: Varies per bit

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**				**ENESPIRST**	**IE**	**ENPLTRST**	**MODIFIED**
Reset	0	0	0	0	See table	0	See table	Reset

Bit	15	14	13	12	11	10	9	8
Name(all)	**INDEX_EN**	**INDEX**						
Reset	See table							

Bit	7	6	5	4	3	2	1	0
Name(all)	**Wire 3-0 Valid**				**Wire 3-0**			
Reset	See table				See table			

Bit	Type	Description
31-18		**Reserved.**
19	R/W	**ENESPIRST (Enable eSPI_RST).** When set to 1, this bit enables the Wire 3-0 Valid and Wire 3-0 bits to be reset when eSPI_RST is asserted. When this bit is set to 0, ENPLTRST bit must also be set to 0 (i.e., PLTRST must be disabled). This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: Wire 3-0 Valid and Wire 3-0 bits are reset only by V_{CC} Power-Up reset or VCC_RST reset. (PLTRST is disabled by ENPLTRST bit set to 0.) 1: Wire 3-0 Valid and Wire 3-0 bits are reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST or PLTRST (according to ENPLTRST bit).
18	R/W	**IE (Interrupt/Wake-up Enable).** If this bit is set1, VWUPD bit in ESPISTS register is set to 1 when MODIFIED bit becomes 1. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: VWUPD bit is not affected by MODIFIED bit (default). 1: VWUPD bit is set to 1 when MODIFIED bit becomes 1. If enabled, VWUPD bit can generate a Core interrupt and/or wake-up.
17	R/W	**ENPLTRST (Enable PLTRST).** When set to 1, this bit enables the Wire 3-0 Valid and Wire 3-0 bits to be reset when PLTRST is asserted. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset.

		0: Wire 3-0 Valid and Wire 3-0 bits are reset only by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST (according to ENESPIRST bit). 1: Wire 3-0 Valid and Wire 3-0 bits are reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST (according to ENESPIRST bit) or **PLTRST**.
16	R/W1C	**MODIFIED (Modified).** This bit is set to 1 when at least one of the Wire 3-0 bits has changed (regardless of the cause of the change: the Host wrote a different value to the bit or the bit was reset). If enabled, an interrupt/wake-up is generated when this bit becomes 1. This bit is cleared by writing 1 to it; writing 0 is ignored. This bit is reset by Core Reset. 0: No change to Wire 3-0 bits (default). 1: Wire 3-0 bits of the group changed (regardless of the change cause).
15	R/W	**INDEX_EN (Index Enable).** Defines the index of the Virtual Wire group. This bit is reset by V_{CC} Power-Up reset or VCC_RST reset. 0: The index is disabled. The hardware ignores the register contents. 1: The index is enabled (default).
14-8	R/W	**INDEX (Index Value).** Defines the lower 7 bits of the index of the Virtual Wire group. The upper bit (bit 8) is constant 0. Index values of 0 and 1 are illegal (they are used for interrupts). This field is reset by V_{CC} Power-Up reset or VCC_RST reset
7-4	RO	**Wire 3-0 Valid (Wire 3-0 Valid).** Each bit indicates the “valid” state of the corresponding Wire 3-0 bit. When set to 1, this bit indicates that the corresponding Wire 3-0 bit is valid and its value should be accounted for. These bits are reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST (according to ENESPIRST bit) or PLTRST (according to ENPLTRST bit). 0: Wire n is invalid. 1: Wire n is valid.
3-0	RO	**Wire 3-0 (Wire 3-0).** Each bit indicates the state of a Virtual Wire of the group. These bits are reset by V_{CC} Power-Up reset, VCC_RST reset, eSPI_RST (according to ENESPIRST bit) or PLTRST (according to ENPLTRST bit).

16.12.16 Virtual Wire Event Slave-to-Master Type Register n (VWEVSMTYPE)

Offset: 208h
Reset: eSPI Reset
Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**Reserved**					**RCINTYPE**	**SMITYPE**	**SCITYPE**
Reset	0	0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
Name(all)	**Reserved**				**PMETYPE**	**WAKETYPE**	**Reserved**	
Reset	0	0	0	0	1	1	0	0

Bit	Type	Description

31-11		**Reserved.**
10	R/W	**RCINTYPE (RCIN# Event Type).** 0: RCIN# event use software path. 1: RCIN# event use hardware path. (default)
9	R/W	**SMITYPE (SMI# Event Type).** 0: SMI# event use software path. 1: SMI# event use hardware path. (default)
8	R/W	**SCITYPE (SCI# Event Type).** 0: SCI# event use software path. 1: SCI# event use hardware path. (default)
7-4		**Reserved.**
3	R/W	**PMETYPE (PME# Event Type).** 0: PME# event use software path. 1: PME# event use hardware path. (default)
2	R/W	**WAKETYPE (WAKE# Event Type).** 0: WAKE# event use software path. 1: WAKE# event use hardware path. (default)
1-0		**Reserved.**

16.12.17 Virtual Wire Programmable Index Group Register (VWPING)

Offset: 2F8h

Reset: Core Reset

Type: Varies per bit

Bit	31	30	29	28	27	26	25	24
Name(all)	**Reserved**							
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name(all)	**Reserved**							**DIRTY**
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name(all)	**INDEX**							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name(all)	**Valid**				**DATA**			
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
31-17		**Reserved.**
16	R/O	**DIRTY (Dirty).** This bit is set to 1 when VWPING register is written by the Core. 0: The group was read by the Host after VWPING register is written by the Core (default). 1: The group was not yet read by the Host.
15-8	R/W	**INDEX (Index Value).** Defines the index of the Virtual Wire group. Index values of 0 and 1 are illegal(they are used for interrupts).

7-4	R/W	**VALID (DATA is Valid).** Each bit controls the "valid" state of the corresponding bit of the DATA field. When set to 1, this bit indicates that the corresponding DATA field bit is valid and its value should be accounted for. The Core firmware should initialize and maintain this field. 0: DATA bit n is invalid (default). 1: DATA bit n is valid.
3-0	R/W	**DATA (Data).** Each bit indicates the state of a Virtual Wire of the group.

16.12.18 Virtual Wire Channel Control Register (VWCTL)

Offset: 2FCh
Reset: V_{CC} Power-Up reset or VCC_RST reset
Type: R/W

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**Reserved**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**Reserved**														**INTWIN**	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Type	Description
31-2		**Reserved.**
1-0	R/W	**INTWIN (Interrupt Window Select).** Controls the mapping of interrupts 15-0 (in this order) originating from the device modules to the reported IRQ lines of the Host. **Bits** **1 0 IRQ Line** 0 0: 15-0 (default). 0 1: 31-16. 1 0: 47-32. 1 1: 63-48.

16.12.19 OOB Receive Buffer Register n (OOBRXBUFn), n = 0-19

Offset: 300h + n*4 with n= 0-19 (Option 2 only)
Reset: V_{CC} Power-Up reset or VCC_RST reset
Type: RO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**RXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**RXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Type	Description
31-0	RO	**RXBDATA (Receive Buffer Data).** Returns bytes n*4 through n *4 + 3 of the message data received from the Host. In OOBRXBUF19 register, bits 31-24 of RXBDATA field are reserved and should be ignored.

16.12.20 OOB Transmit Buffer Register n (OOBTXBUFn), n = 0-19

Offset: 380h + n*4 with n = 0-19 (Option 2 only)
Reset: V_{CC} Power-Up reset or VCC_RST reset
Type: WO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**TXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**TXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Type	Description
31-0	WO	**TXBDATA (Transmit Buffer Data).** Holds bytes n*4 through n*4 + 3 of the message data written by the Core. In OOBTXBUF19 register, bits 31-24 of TXBDATA field are reserved and should be written 00h.

16.12.21 Flash Receive Buffer Register n, (FLASHRXBUFn), n = 0-16

Offset: 400h + n*4 with n = 0-16 (Option 2 only)

Note: This register should not be accessed if the Flash Access Channel is set to Automatic mode.

Reset: V_{CC} Power-Up reset or $\overline{VCC_RST}$ reset

Type: RO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**RXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**RXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Type	Description
31-0	RO	**RXBDATA (Receive Buffer Data).** Returns bytes n*4 through n*4 + 3 of the Master-Attached Flash Access Channel Completion message data received from the Host.

16.12.22 Flash Transmit Buffer Register n, (FLASHTXBUFn), n = 0-5

Offset: 480h + n*4 with n = 0-5 (Option 2 only)

Reset: V_{CC} Power-Up reset or $\overline{VCC_RST}$ reset

Type: WO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name(all)	**TXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name(all)	**TXBDATA**															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Type	Description
31-0	WO	**TXBDATA (Transmit Buffer Data).** Holds bytes n*4 through n*4 + 3 of the Master-Attached Flash Access Channel request message data written by the Core.

16.13 eSPI_SIF Integration Implementation Notes

HMIB (SIB) Data Width Control

SIB data width control signals (sib_width_sup_in) are generated by the SIB Interface Circuit according to the maximum SIB data width of the accessed module/function, as follows:

- For read transactions from the SHM Shared RAM Access windows, the value of sib_width_sup_in is '10' (4-bytes).
- For any other read or write transactions, the value of sib_width_sup_in is '00' (1-byte).

When the value of the sib_width_sup_in is '00', the eSPI_SIF controls the SIB transaction as follows:

- If the payload data size of the eSPI transaction is 1 byte, a 1-byte SIB transaction is performed. The data is always transferred via byte 0 (bits 7-0) of SIB, regardless of the value of SIB address bits 1-0
- If the payload data size of the eSPI transaction is more than 1 byte, the transaction is broken down into 1-byte SIB transactions, performed as above.

When the value of the sib_width_sup_in is '10', the eSPI Interface controls the SIB transaction as follows:

- If the payload data size of the eSPI transaction is 1 byte, a 4-byte SIB transaction is performed. The data is transferred via the SIB byte according to the value of SIB address bits 1-0.
- If the payload data size of the eSPI transaction is more than 1 byte, the transaction is broken down into 4-byte SIB transactions. The number or transactions depends on the data address being 4-byte aligned or not. The 4-byte SIB transactions are as follows:
  - The "middle" transactions (if relevant) are 4-byte SIB transactions accessing a 4-byte aligned address; therefore, all 4 data bytes are transferred.
  - The "first" and/or the "last" transactions (if relevant) are 4-byte SIB transactions accessing a non-aligned address; therefore, only 1-3 of the data bytes are transferred. The data byte(s) are transferred via the SIB byte(s) according to the value of SIB address bits 1-0.

HMIB (SIB) Arbitration

The eSPI_SIF and the Core Access to Host Modules (APB2SIB) arbitrate access to the SIB. Arbitration priority is controlled by CSAE bit in SIBCTRL register as follows:

- CSAE = 0 Core access to the Host modules is disabled, or the NPCX667K is in Sleep or Deep Sleep power state. In this case, the eSPI_SIF has immediate access to the SIB and does not have to wait for the arbitration handshake signal to be returned by the APB2SIB. This is implemented by the SIB interface circuit driving the arbitration handshake signal to "SIB free" state. In this case, only one WAIT cycle is required for any Peripheral Channel access except for access to the Shared RAM Access windows or to Indirect Memory Access registers. **Note**: CSAE must be set to 0 before the NPCX667K enters a Sleep or Deep Sleep power state.
- CSAE = 1 Core access to the Host modules is enabled; therefore, APB2SIB **might** access the SIB: In this case, before accessing the SIB, the eSPI_SIF sends an SIB request to the APB2SIB and then waits for the arbitration handshake signal to be returned by the APB2SIB. If the APB2SIB is currently using the SIB, the eSPI_SIF waits until the SIB is free; even if the APB2SIB is not currently using the SIB, the eSPI SIB transaction is delayed by a few APB clock cycles until the arbitration handshake signal is updated. **Note**: It is recommended to ensure fair APB2SIB access to SIB during a burst SIB access by the eSPI_SIF.
- After CSAE bit is set to 1, APB2SIB access to SIB is disabled for a few APB cycles to ensure that the arbitration and shake signal is sampled by the eSPI_SIF.

17. ON-CHIP DEBUG SUPPORT INTERFACE (ODCS)

17.1 Overview

The OCDS function allows user to read/write memory and stop/run/step MCU core unit. Most of the registers are accessible according to the way described in the NEXUS 5001 standard. All registers are accessible through the IEEE1149.1 port independently of the state of the MCU.

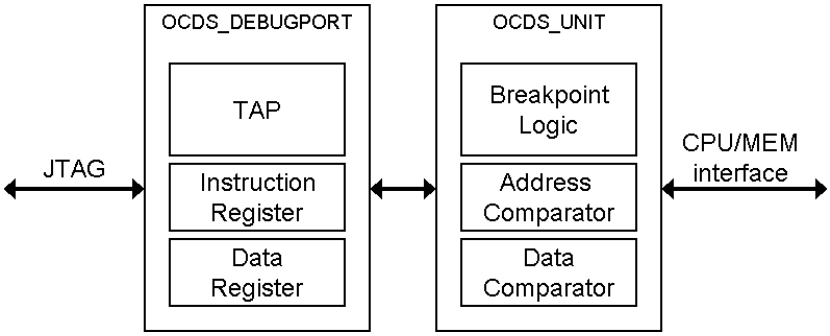


Figure 17-1 JTAG I/O Shifter Register

17.2 Function Description

17.2.1 JTAG Interface

NCT6686D has 4 IEEE1149.1 required pin.

- Test Clock Input (MCU_TCK) provides clock for JTAG port.
- Test Data Input (MCU_TDI) provides for serial movement of data into JTAG port. It is sampled by NCT6686D on the rising edge of MCU_TCK.
- Test Data Output (MCU_TDO) provides for serial movement of data out of JTAG port. It is driven by NCT6686D on the falling edge of MCU_TCK.
- Test Mode Select Input (MCU_TMS) provides access to the JTAG TAP state machine. It is sampled by NCT6686D on the rising edge of MCU_TCK.

The IEEE149.1 TRST function pin is connected to internal VSB power-on reset. After power-on reset, it has to insert 2 dummy clocks to MCU_TCK pin to release reset condition. It is recommend that forces MCU_TMS high and inserts 7 clocks to MCU_TCK to insure TAP state keeping in TEST_LOGIC_RESET state.

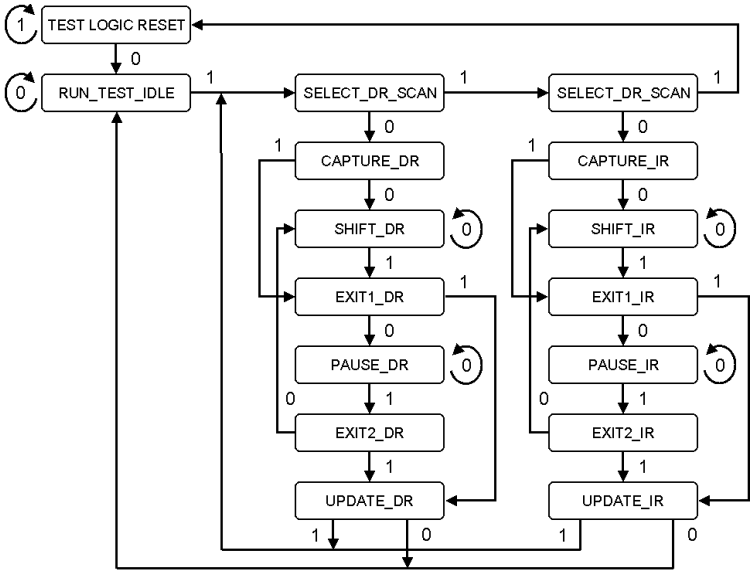


Figure 17-2 JTAG TAP State Machine

JTAG port can read/write register when TAP is in SHIFT_DR/SHIFT_IR state. MCU_TDI and MCU_TDO shifts in/out LSB bit first when data read/write.

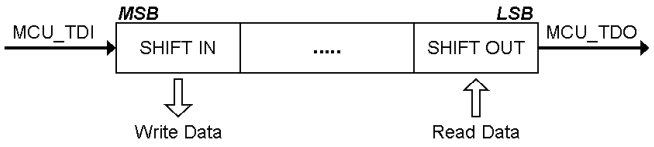


Figure 17-3 JTAG Port Shift Register

Instruction Code	Function Name	Data Register	Type
0001	IDCODE	32-bit ID value = 1050_5538h	RO
1010	OCDSMEMACC	Memory data read/write access	R/W
1011	NEXUS-ENABLE	NRR registers	per register
others	BYPASS	BYPASS register	R/W

NCT6686D JTAG function supports 4 instructions as followed.

17.2.2 NRR access

When the “NEXUS-ENABLE” instruction is being decoded by the JTAG controller, the JTAG allows communications to NRRs. Each NRR is referenced by a unique register address index. All communication with the Nexus controller is performed via the SELECT_DR_SCAN path. The Nexus controller will default to a register select state when enabled. Accessing an NRR requires two passes through the SELECT-DR_SCAN path, one pass to select the NRR and the second pass to read or write the NRR data. The first pass through the SELECT-DR_SCAN path is used to enter an 8-bit Nexus command consisting of a read/write control bit in the LSB followed by a 7-bit NRR address, as illustrated in Figure15-4. When a NRR is read, the register value is loaded into JTAG shifter register during CAPTURE_DR state. When a NRR is written, the value is loaded from JTAG shifter register during UPDATE_DR state.

BIT 7-1	BIT 0
7-bit NRR address	0 = Write 1 = Read

Figure 17-4 Nexus Command Field

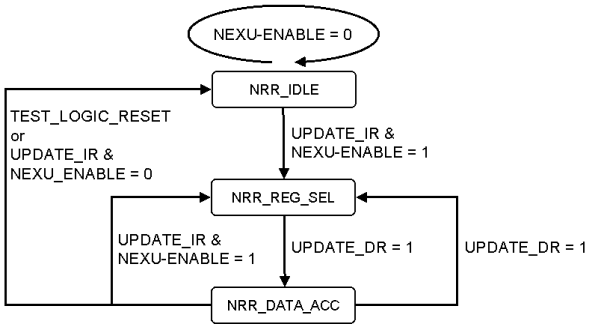


Figure 17-5 NEXU Controller State Machine

17.2.3 NRR Description

There are 45 NRRs in NCT6686D. It supports five major functions to monitor/debug program.

- Monitor accumulator/program counter value.
- Execute single instruction from user/debug program.
- Read/Write external program/data memory.
- Software breakpoint. Code : 0xA5
- Hardware breakpoint

NCT6686D supports 8 hardware breakpoints. Each hardware breakpoint function has 5 NRRs to monitor internal memory, external data memory and program memory operation.

17.2.3.1. OCDSCTL Register – NRR Address = 40h

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 11 bits

BIT	READ / WRITE	DESCRIPTION
10	RO	Software breakpoint status = 0 software breakpoint didn't occur. = 1 software breakpoint occurred.
9	RO	Reserved.
8	R / W	Debugger program selector 1
7	RO	Reserved.
6	R / W	Peripheral clock enable = 1 Disable all module clock but MCU (it will cause system crash) = 0 normal operation

BIT	READ / WRITE	DESCRIPTION
5	R / W	MCU reset.
4	R / W	OCDS enable. = 1 OCDS enable. = 0 OCDS disable. The MCU will not stop at breakpoint. 0xA5 instruction is executed like NOP. MCU reset is ignored.
3	RO	Debug acknowledge = 1 The MCU is stopped at the breakpoint or debug request. = 0 The MCU is executing instruction.
2	R / W	Debug request It causes MCU enter debug mode when debug acknowledge active.
1	R / W	Debug step It causes MCU to execute single instruction when it set to 1. This bit is automatically cleared by hardware after instruction executed. This bit has to be set after debug request. Debug step and debug request can't be set simultaneously.
0	R / W	Debugger program selector 0 select1 select0 = 00 User program. PC is normally incremented. = x1 OCDSINSTR program. PC is not incremented. = 10 OCDSINSTR program. PC is normally incremented. Branch instruction will update PC normally.

17.2.3.2. OCDSACC Register – NRR Address = 41h

Attribute: Read Only
Power Well: VSB
Reset by: RSMRST#
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	RO	MCU accumulator register

17.2.3.3. OCDSPC Register – NRR Address = 42h

Attribute: Read Only
Power Well: VSB
Reset by: RSMRST#
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
15-0	RO	MCU program counter register

17.2.3.4. OCDSINSTR Register – NRR Address = 43h

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 000000h
Size: 24 bits

BIT	READ / WRITE	DESCRIPTION
23-0	R/W	BIT23-BIT16 debug instruction byte0 BIT15-BIT8 debug instruction byte1 BIT7-BIT0 debug instruction byte2

17.2.3.5. OCDSMAC Register – NRR Address = 44h

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
2	R / W	Memory read = 1 memory read operation when OCDSMEMACC = 1 = 0 no operation
1	R / W	Memory write = 1 memory write operation when OCDSMEMACC = 1 = 0 no operation
0	R / W	Memory selection = 1 data memory = 0 program memory

17.2.3.6. OCDSBPDn Register – NRR Address = 46h + n*4

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Data value

17.2.3.7. OCDSBPDMn Register – NRR Address = 47h + n*4

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Data mask value

17.2.3.8. OCDSBPAn Register – NRR Address = 48h + n*4

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 000000h
Size: 23 bits

BIT	READ / WRITE	DESCRIPTION
22-0	R / W	Address start value

17.2.3.9. OCDSBPAMn Register – NRR Address = 49h + n*4

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 000000h
Size: 23 bits

BIT	READ / WRITE	DESCRIPTION
22-0	R / W	Address end value

17.2.3.10. OCDSBPCn Register – NRR Address = 50h + n*4

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	Trace mode = 000 breakpoint function = others NA.
4	R / W	Data memory select = 1 internal memory = 0 external memory
3	R / W	Program stopped at breakpoint = 1 active = 0 inactive
2	R / W	Memory select = 1 program memory = 0 data memory
1	R / W	Read select = 1 read accesses are monitored for breakpoint = 0 read accesses are not monitored for breakpoint.

BIT	READ / WRITE	DESCRIPTION
0	R / W	Write select = 1 write accesses are monitored for breakpoint = 0 write accesses are not monitored for breakpoint.

18. CONFIGURATION REGISTER

18.1 Chip (Global) Control Register

CR 07h. Logical Device Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	Sharing SPI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	PRT IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

BIT	READ / WRITE	DESCRIPTION
0	R / W	GPIO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR1D [Bit3] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6-2	Reserved	
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	SCI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR1D [Bit3] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR1D [Bit3] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR1D [Bit3] must be set to logic 1.

CR 15h. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Pin122 function selection CR15 [Bit7-6] / Pin122 00 / GPIO03 01 / tri-state 1x / TACHPWM
5-4	R / W	Pin121 function selection CR15 [Bit5-4] / Pin121 00 / GPIO02 01 / tri-state 1x / TACHPWM
3-2	R / W	Pin4 function selection CR15 [Bit3-2] / Pin4 00 / GPIO01 1x / TACHPWM
1-0	R / W	Pin3 function selection CR15 [Bit1-0] / Pin3 00 / GPIO00 1x / TACHPWM

CR 1Ah. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin15 function selection
<table>
<tr><td>CR1A [Bit7]</td><td>Pin15</td></tr>
<tr><td>0</td><td>GPIO80</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin103 function selection
<table>
<tr><td>CR1A [Bit6-5]</td><td>Pin103</td></tr>
<tr><td>00</td><td>GPIO83</td></tr>
<tr><td>01</td><td>reserved</td></tr>
<tr><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>4-3</td><td>R / W</td><td>Pin37 function selection
<table>
<tr><td>CR1A [Bit4-3]</td><td>Pin37</td></tr>
<tr><td>00</td><td>GPIO74</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>2-0</td><td>R / W</td><td>Pin125 function selection
<table>
<tr><td>CR1A [Bit2-0]</td><td>Pin125</td></tr>
<tr><td>000</td><td>GPIO73</td></tr>
<tr><td>001</td><td>CIRTX2</td></tr>
<tr><td>010</td><td>Reserved</td></tr>
<tr><td>011</td><td>tri-state</td></tr>
<tr><td>1xx</td><td>TACHPWM</td></tr>
</table></td></tr>
</table>

CR 1Bh. Multi-function Pin Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 10h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin91 function selection
<table>
<tr><td>DIS_HWACPI</td><td>CR1B [Bit7]</td><td>DSW_EN</td><td>Pin91</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>SUSACK#</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>tri-state</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GPIO92</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GPIO92</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>Pin90 function selection
<table>
<tr><td>CR1B [Bit6]</td><td>DIS_HWACPI</td><td>Pin90</td></tr>
<tr><td>0</td><td>0</td><td>GPIO91</td></tr>
<tr><td>0</td><td>1</td><td>tri-state</td></tr>
<tr><td>1</td><td>x</td><td>GPIO91</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin93 function selection
<table>
<tr><td>CR1B [Bit5]</td><td>DSW_EN</td><td>Pin93</td></tr>
<tr><td>0</td><td>1</td><td>SUSWARN#</td></tr>
<tr><td>x</td><td>0</td><td>GPIO90</td></tr>
<tr><td>1</td><td>1</td><td>GPIO90</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin96 function selection
<table>
<tr><td>CR1B [Bit4]</td><td>Pin96</td></tr>
<tr><td>0</td><td>CIRTX1</td></tr>
<tr><td>1</td><td>GPIO05</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin34 function selection
<table>
<tr><td>CR1B [Bit3]</td><td>CR24 [Bit2-1]</td><td>Pin34</td></tr>
<tr><td>1</td><td>xx</td><td>SOUTA_P80</td></tr>
<tr><td>0</td><td>00</td><td>SOUTA</td></tr>
<tr><td>0</td><td>01</td><td>GPIO25</td></tr>
<tr><td>0</td><td>10</td><td>reserved</td></tr>
<tr><td>0</td><td>11</td><td>GPIO25</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Hardware PME Enable Bit
0: Disable PME
1: Enable PME</td></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin65 function selection
<table>
<tr><td>CR1B [Bit1-0]</td><td>DIS_HWACPI</td><td>Pin65</td></tr>
<tr><td>00</td><td>0</td><td>PME# (HW)</td></tr>
<tr><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>01</td><td>x</td><td>PME# (SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN02</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
</table>

CR 1Dh. TEST Mode Register (TEST MODE.)

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	IRQ TYPE Control Bit (TEST MODE) 0 : Disable 1 : Enable
2-0	Reserved	

CR 1Eh. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Pin95 function selection CR1E [Bit7-6] / Pin95 00 / GPIO70 01 / CIRRX 1x / TACHPWM
5-4	R / W	Pin98 function selection CR1E [Bit5-4] / Pin98 00 / GPIO71 01 / CIRWB 1x / TACHPWM
3-2	R / W	Pin124 function selection CR1E [Bit3-2] / Pin124 00 / GPIO72 01 / CIRTX1 1x / TACHPWM
1-0	R / W	Pin104 function selection CR1E [Bit1-0] / Pin104 00 / GPIO84 01 / Reserved 1x / TACHPWM

CR 1Fh. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin127 function selection
<table>
<tr><td>CR1F [Bit7-6]</td><td>Pin127</td></tr>
<tr><td>00</td><td>GPIO82</td></tr>
<tr><td>01</td><td>Tri-state</td></tr>
<tr><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin126 function selection
<table>
<tr><td>CR1F [Bit5-4]</td><td>Pin126</td></tr>
<tr><td>00</td><td>GPIO81</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin128 function selection
<table>
<tr><td>CR29 [Bit4]</td><td>CR1F [Bit3-2]</td><td>AMDPWR_EN</td><td>Pin128</td></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>MSCL1</td></tr>
<tr><td>0</td><td>00</td><td>0</td><td>GPIO75</td></tr>
<tr><td>0</td><td>00</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>GPIO75</td></tr>
<tr><td>0</td><td>1x</td><td>x</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin123 function selection
<table>
<tr><td>CR29 [Bit4]</td><td>CR1F [Bit1-0]</td><td>Pin123</td></tr>
<tr><td>1</td><td>xx</td><td>MSDA1</td></tr>
<tr><td>0</td><td>00</td><td>GPIO76</td></tr>
<tr><td>0</td><td>01</td><td>GPIO76</td></tr>
<tr><td>0</td><td>1x</td><td>Reserved</td></tr>
</table></td></tr>
</table>

CR 20h. Chip ID (High Byte)

Attribute: Read Only
Power Well: VSB
Reset by: None
Default : C7h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = C7h

CR 21h. Chip ID (Low Byte)

Attribute: Read Only
Power Well: VSB
Reset by: None
Default : 3Ah

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 3Ah

CR 22h. Device Power down Option

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	KBC Power Down. 0: Powered down. 1: Not powered down.
6	Reserved	
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2	R / W	CIR Power Down. 0: Powered down. 1: Not powered down.
1-0	Reserved	

CR 23h. Device Power down Option

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	PORT80 to UART Power Down. 0: Powered down. 1: Not powered down.
6	R / W	ACPI Power Down. 0: Powered down. 1: Not powered down.
5	Reserved	
4	R / W	GPIO0 Power Down. 0: Powered down. 1: Not powered down.
3	R / W	GPIO1 Power Down. 0: Powered down. 1: Not powered down.
2	R / W	GPIO2 Power Down. 0: Powered down. 1: Not powered down.
1	R / W	GPIO3 Power Down. 0: Powered down. 1: Not powered down.
0	R / W	GPIO4 Power Down. 0: Powered down. 1: Not powered down.

CR 24h. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 67h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin18 function selection
<table>
<tr><td>ESPI_EN</td><td>CR24 [Bit7]</td><td>Pin18</td></tr>
<tr><td>1</td><td>X</td><td>ESPI_RESET#</td></tr>
<tr><td>0</td><td>0</td><td>GPIO10</td></tr>
<tr><td>0</td><td>1</td><td>LDRQ#</td></tr>
</table></td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin27 function selection
<table>
<tr><td>CR24 [Bit6-5]</td><td>Pin27</td></tr>
<tr><td>00</td><td>GA20</td></tr>
<tr><td>01</td><td>SPI_WP#</td></tr>
<tr><td>1x</td><td>GPIO11</td></tr>
</table>
Pin28 function selection
<table>
<tr><td>CR24 [Bit6-5]</td><td>Pin28</td></tr>
<tr><td>00</td><td>KBRST#</td></tr>
<tr><td>01</td><td>SPI_HOLD#</td></tr>
<tr><td>1x</td><td>GPIO12</td></tr>
</table></td></tr>
<tr><td>4-3</td><td colspan="2">Reserved</td></tr>
<tr><td>2-1</td><td>R / W</td><td>Pin29 function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin29</td></tr>
<tr><td>00</td><td>CTSA#</td></tr>
<tr><td>01</td><td>CIRRX</td></tr>
<tr><td>10</td><td>CIRRX</td></tr>
<tr><td>11</td><td>GPIO20</td></tr>
</table>
Pin30 function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin30</td></tr>
<tr><td>00</td><td>DSRA#</td></tr>
<tr><td>01</td><td>CIRWB</td></tr>
<tr><td>10</td><td>CIRWB</td></tr>
<tr><td>11</td><td>GPIO21</td></tr>
</table>
Pin31 function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin31</td></tr>
<tr><td>00</td><td>RTSA#</td></tr>
<tr><td>01</td><td>CIRTX1</td></tr>
<tr><td>10</td><td>CIRTX1</td></tr>
<tr><td>11</td><td>GPIO22</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>2-1</td><td>R / W</td><td>
Pin32 function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin32</td></tr>
<tr><td>00</td><td>DTRA#</td></tr>
<tr><td>01</td><td>CIRTX2</td></tr>
<tr><td>10</td><td>CIRTX2</td></tr>
<tr><td>11</td><td>GPIO23</td></tr>
</table>
Pin33function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin33</td></tr>
<tr><td>00</td><td>SINA</td></tr>
<tr><td>01</td><td>GP24</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>GP24</td></tr>
</table>
Pin34 function selection
<table>
<tr><td>CR1B [Bit3]</td><td>CR24 [Bit2-1]</td><td>Pin34</td></tr>
<tr><td>1</td><td>xx</td><td>SOUTA_P80</td></tr>
<tr><td>0</td><td>00</td><td>SOUTA</td></tr>
<tr><td>0</td><td>01</td><td>GPIO25</td></tr>
<tr><td>0</td><td>10</td><td>Reserved</td></tr>
<tr><td>0</td><td>11</td><td>GPIO25</td></tr>
</table>
Pin35 function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin35</td></tr>
<tr><td>00</td><td>DCDA#</td></tr>
<tr><td>01</td><td>GPIO26</td></tr>
<tr><td>10</td><td>GPIO26</td></tr>
<tr><td>11</td><td>GPIO26</td></tr>
</table>
Pin36 function selection
<table>
<tr><td>CR24 [Bit2-1]</td><td>Pin36</td></tr>
<tr><td>00</td><td>RIA#</td></tr>
<tr><td>01</td><td>GPIO27</td></tr>
<tr><td>10</td><td>GPIO27</td></tr>
<tr><td>11</td><td>GPIO27</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>R / W</td><td>PNPCVS =>
= 0 The compatible PNP address-select registers have default values.
= 1 The compatible PNP address-select registers have no default values.</td></tr>
</table>

CR 25h. Multi-function Pin Selection

Attribute: Read/Write

Power Well: VSB
Reset by: RSMRST#
Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>GPIO5 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>6</td><td>R / W</td><td>GPIO6 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>5</td><td>R / W</td><td>GPIO7 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>4</td><td>R / W</td><td>GPIO8 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>3</td><td>R / W</td><td>GPIO9 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>2</td><td>R / W</td><td>GPIOEN0 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>1</td><td>R / W</td><td>GPIOEN1 Power Down. 0: Powered down. 1: Not powered down.</td></tr>
<tr><td>0</td><td>R / W</td><td>Pin38 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>CR25 [Bit0]</th><th>Pin38</th></tr>
<tr><td>1</td><td>x</td><td>SLCT</td></tr>
<tr><td>0</td><td>0</td><td>GPIO30</td></tr>
<tr><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
Pin55 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>CR25 [Bit0]</th><th>Pin55</th></tr>
<tr><td>1</td><td>x</td><td>STB#</td></tr>
<tr><td>0</td><td>0</td><td>GPIO13</td></tr>
<tr><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table></td></tr>
</table>

CR 26h. Global Option
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin102 function selection
<table>
<tr><th>CR29 [Bit0]</th><th>Pin102</th></tr>
<tr><td>0</td><td>GPIO77</td></tr>
<tr><td>1</td><td>SKTOCC#</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>HEFRAS =>
= 0 Write 87h to location 2E twice.
= 1 Write 87h to location 4E twice.</td></tr>
<tr><td>5-3</td><td colspan="2">Reserved</td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. Multi-function Pin Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 3Eh

BIT	READ / WRITE	DESCRIPTION

<table>
<tr>
<td>7-6</td>
<td>R / W</td>
<td>
Pin38 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>CR25 [Bit0]</th><th>Pin38</th></tr>
<tr><td>1</td><td>x</td><td>SLCT</td></tr>
<tr><td>0</td><td>0</td><td>GPIO30</td></tr>
<tr><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
Pin39 function selection
<table>
<tr><th>CR27 [Bit7-6]</th><th>Pin39</th></tr>
<tr><td>1x</td><td>PE</td></tr>
<tr><td>01</td><td>P2_DGL#</td></tr>
<tr><td>00</td><td>GPIO31</td></tr>
</table>
Pin40 function selection
<table>
<tr><th>CR27 [Bit7-6]</th><th>Pin40</th></tr>
<tr><td>1x</td><td>BUSY</td></tr>
<tr><td>01</td><td>P2_DGL#</td></tr>
<tr><td>00</td><td>GPIO32</td></tr>
</table>
Pin41 function selection
<table>
<tr><th>CR27 [Bit7-6]</th><th>Pin41</th></tr>
<tr><td>1x</td><td>ACK#</td></tr>
<tr><td>01</td><td>P2_DGH#</td></tr>
<tr><td>00</td><td>GPIO33</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr>
<td>7-6</td>
<td>R / W</td>
<td>
Pin42 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin42</td></tr>
<tr><td>1x</td><td>PD7</td></tr>
<tr><td>01</td><td>P2_DGH#</td></tr>
<tr><td>00</td><td>GPIO34</td></tr>
</table>
Pin43 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin43</td></tr>
<tr><td>1x</td><td>PD6</td></tr>
<tr><td>01</td><td>LED_A</td></tr>
<tr><td>00</td><td>GPIO35</td></tr>
</table>
Pin44 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin44</td></tr>
<tr><td>1x</td><td>PD5</td></tr>
<tr><td>01</td><td>LED_B</td></tr>
<tr><td>00</td><td>GPIO36</td></tr>
</table>
Pin45 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin45</td></tr>
<tr><td>1x</td><td>PD4</td></tr>
<tr><td>01</td><td>LED_C</td></tr>
<tr><td>00</td><td>GPIO37</td></tr>
</table>
Pin47 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin47</td></tr>
<tr><td>1x</td><td>PD3</td></tr>
<tr><td>01</td><td>LED_D</td></tr>
<tr><td>00</td><td>GPIO40</td></tr>
</table>
Pin48 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin48</td></tr>
<tr><td>1x</td><td>PD2</td></tr>
<tr><td>01</td><td>LED_E</td></tr>
<tr><td>00</td><td>GPIO41</td></tr>
</table>
Pin49 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin49</td></tr>
<tr><td>1x</td><td>PD1</td></tr>
<tr><td>01</td><td>LED_F</td></tr>
<tr><td>00</td><td>GPIO42</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr>
<td>7-6</td>
<td>R / W</td>
<td>
Pin50 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin50</td></tr>
<tr><td>1x</td><td>PD0</td></tr>
<tr><td>01</td><td>LED_G</td></tr>
<tr><td>00</td><td>GPIO43</td></tr>
</table>
Pin51 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin51</td></tr>
<tr><td>1x</td><td>SLIN#</td></tr>
<tr><td>01</td><td>P1_DGL#</td></tr>
<tr><td>00</td><td>GPIO44</td></tr>
</table>
Pin52 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin52</td></tr>
<tr><td>1x</td><td>INIT#</td></tr>
<tr><td>01</td><td>P1_DGL#</td></tr>
<tr><td>00</td><td>GPIO45</td></tr>
</table>
Pin53 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin53</td></tr>
<tr><td>1x</td><td>ERR#</td></tr>
<tr><td>01</td><td>P1_DGH#</td></tr>
<tr><td>00</td><td>GPIO46</td></tr>
</table>
Pin54 function selection
<table>
<tr><td>CR27 [Bit7-6]</td><td>Pin54</td></tr>
<tr><td>1x</td><td>AFD#</td></tr>
<tr><td>01</td><td>P1_DGH#</td></tr>
<tr><td>00</td><td>GPIO47</td></tr>
</table>
Pin55 function selection
<table>
<tr><td>CR27 [Bit7]</td><td>CR25 [Bit0]</td><td>Pin55</td></tr>
<tr><td>1</td><td>x</td><td>STB#</td></tr>
<tr><td>0</td><td>0</td><td>GPIO13</td></tr>
<tr><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table>
</td>
</tr>
<tr>
<td>5</td>
<td>R / W</td>
<td>
Pin64 function selection
<table>
<tr><td>CR27 [Bit5]</td><td>ESPI_OUT_SEL CR22[0]</td><td>ESPI_EN (Strap)</td><td>Pin64</td></tr>
<tr><td>0</td><td>x</td><td>x</td><td>GPEN01</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>SLP_S3#</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Tri-state (VW)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>SLP_S3_OUT# (VW)</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td>4</td><td>R / W</td><td>Pin61 function selection
<table>
<tr><th>CR27 [Bit4]</th><th>Pin61</th></tr>
<tr><td>0</td><td>GPEN04</td></tr>
<tr><td>1</td><td>PSIN#</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin83 function selection
<table>
<tr><th>CR27 [Bit3]</th><th>Pin83</th></tr>
<tr><td>0</td><td>GPEN05</td></tr>
<tr><td>1</td><td>RESETCON#</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin84 function selection
<table>
<tr><th>CR27 [Bit2]</th><th>ESPI_OUT_SEL CR22[0]</th><th>ESPI_EN</th><th>Pin84</th></tr>
<tr><td>0</td><td>x</td><td>x</td><td>GPEN06</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>SLP_S5#</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Tri-state</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>SLP_S5_OUT# (VW)</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin80 function selection
<table>
<tr><th>CR27 [Bit1]</th><th>Pin80</th></tr>
<tr><td>0</td><td>GPEN10</td></tr>
<tr><td>1</td><td>ATXPGD</td></tr>
</table></td></tr>
<tr><td>0</td><td colspan="2">Reserved</td></tr>
</table>

CR 28h. Multi-function Pin Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMSRT#

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin63 function selection
<table>
<tr><th>CR28 [Bit7-6]</th><th>DIS_HWACPI</th><th>Pin63</th></tr>
<tr><td>00</td><td>0</td><td>PSON#(HW)</td></tr>
<tr><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>01</td><td>x</td><td>PSON#(SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN00</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin60 function selection
<table>
<tr><th>CR28 [Bit5-4]</th><th>DIS_HWACPI</th><th>Pin60</th></tr>
<tr><td>00</td><td>0</td><td>PSOUT#(HW)</td></tr>
<tr><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>01</td><td>x</td><td>PSOUT#(SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN03</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>3</td><td colspan="2">Reserved</td></tr>
<tr><td>2-0</td><td>R / W</td><td>PRTMODS2 ~ 0 =>
Bits
2 1 0
= 0 x x Parallel Port Mode.
= 1 x x Reserved.</td></tr>
</table>

CR 29h. Multi-function Pin Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMSRT#

Default : 03h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin89 function selection
<table>
<tr><th>LDB CRE4 [Bit3-2]</th><th>CR29 [Bit7]</th><th>DSW_EN</th><th>Pin89</th></tr>
<tr><td>00</td><td>0</td><td>1</td><td>SLP_SUS#</td></tr>
<tr><td>00</td><td>1</td><td>x</td><td>GPIO93</td></tr>
<tr><td>00</td><td>0</td><td>0</td><td>GPIO93</td></tr>
<tr><td>01</td><td>x</td><td>x</td><td>3VSBSW#(HW)</td></tr>
<tr><td>10</td><td>x</td><td>x</td><td>3VSBSW#(SW)</td></tr>
<tr><td>11</td><td>x</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>6-5</td><td>R / W</td><td>Reserved</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>Pin123 function selection
<table>
<tr><th>CR29 [Bit4]</th><th>CR1F [Bit1-0]</th><th>Pin123</th></tr>
<tr><td>1</td><td>xx</td><td>MSDA1</td></tr>
<tr><td>0</td><td>00</td><td>GPIO76</td></tr>
<tr><td>0</td><td>01</td><td>GPIO76</td></tr>
<tr><td>0</td><td>1x</td><td>Reserved</td></tr>
</table>
Pin128 function selection
<table>
<tr><th>CR29 [Bit4]</th><th>CR1F [Bit3-2]</th><th>Pin128</th></tr>
<tr><td>1</td><td>xx</td><td>MSCL1</td></tr>
<tr><td>0</td><td>00</td><td>GPIO75</td></tr>
<tr><td>0</td><td>01</td><td>GPIO75</td></tr>
<tr><td>0</td><td>1x</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin76 function selection
<table>
<tr><th>CR29 [Bit3]</th><th>Pin76</th></tr>
<tr><td>0</td><td>GPIO62</td></tr>
<tr><td>1</td><td>MSDA0</td></tr>
</table>
Pin75 function selection
<table>
<tr><th>CR29 [Bit3]</th><th>Pin75</th></tr>
<tr><td>0</td><td>GPIO63</td></tr>
<tr><td>1</td><td>MSCL0</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin77function selection
<table>
<tr><th>CR29 [Bit2]</th><th>CR2A [Bit1-0]</th><th>DIS_HWACPI</th><th>Pin77</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>MSCL2</td></tr>
<tr><td>0</td><td>00</td><td>0</td><td>RSTOUT2#(HW)</td></tr>
<tr><td>0</td><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>RSTOUT2#(SW)</td></tr>
<tr><td>0</td><td>10</td><td>x</td><td>tri-state</td></tr>
<tr><td>0</td><td>11</td><td>x</td><td>GPEN13</td></tr>
</table>
Pin78 function selection
<table>
<tr><th>CR29 [Bit2]</th><th>CR2A [Bit3-2]</th><th>DIS_HWACPI</th><th>Pin78</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>MSCL2</td></tr>
<tr><td>0</td><td>00</td><td>0</td><td>RSTOUT1#(HW)</td></tr>
<tr><td>0</td><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>RSTOUT1#(SW)</td></tr>
<tr><td>0</td><td>10</td><td>x</td><td>tri-state</td></tr>
<tr><td>0</td><td>11</td><td>x</td><td>GPEN12</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>R / W</td><td>Pin2 function selection
<table>
<tr><td>CR29 [Bit1]</td><td>Pin2</td></tr>
<tr><td>0</td><td>OVT# / SMI#</td></tr>
<tr><td>1</td><td>GPIO85</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin100 function selection
<table>
<tr><td>CR29 [Bit0]</td><td>Pin100</td></tr>
<tr><td>0</td><td>GPIO66</td></tr>
<tr><td>1</td><td>CASEOPEN0#</td></tr>
</table></td></tr>
</table>

CR 2Ah. Multi-function Pin Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 0Fh

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin88 function selection
<table>
<tr><td>DIS_HWACPI</td><td>CR2A [Bit7]</td><td>DSW_EN</td><td>Pin88</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>SLP_SUS_FET</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>tri-state</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>GPIO94</td></tr>
<tr><td>0</td><td>x</td><td>0</td><td>GPIO94</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>
Pin7 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2C [Bit1-0]</td><td>Pin7</td></tr>
<tr><td>1</td><td>xx</td><td>CTSB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO50</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
Pin8 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2C [Bit3-2]</td><td>Pin8</td></tr>
<tr><td>1</td><td>xx</td><td>DSRB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO51</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
Pin9 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2C [Bit5-4]</td><td>Pin9</td></tr>
<tr><td>1</td><td>xx</td><td>RTSB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO52</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
Pin10 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2C [Bit7-6]</td><td>Pin10</td></tr>
<tr><td>1</td><td>xx</td><td>DTRB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO53</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
Pin11 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2D [Bit1-0]</td><td>Pin11</td></tr>
<tr><td>1</td><td>xx</td><td>SINB</td></tr>
<tr><td>0</td><td>00</td><td>GPIO54</td></tr>
<tr><td>0</td><td>01</td><td>IRRX</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
Pin12 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2D [Bit3-2]</td><td>Pin12</td></tr>
<tr><td>1</td><td>xx</td><td>SOUTB</td></tr>
<tr><td>0</td><td>00</td><td>GPIO55</td></tr>
<tr><td>0</td><td>01</td><td>IRTX</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>Pin13 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2D [Bit5-4]</th><th>Pin13</th></tr>
<tr><td>1</td><td>xx</td><td>DCDB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO56</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table>
Pin14 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2D [Bit7-6]</th><th>Pin14</th></tr>
<tr><td>1</td><td>xx</td><td>RIB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO57</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin79 function selection
<table>
<tr><th>CR2A [Bit5-4]</th><th>DIS_HWACPI</th><th>Pin79</th></tr>
<tr><td>00</td><td>0</td><td>RSTOUT0#(HW)</td></tr>
<tr><td>00</td><td>1</td><td>output low</td></tr>
<tr><td>01</td><td>x</td><td>RSTOUT0#(SW)</td></tr>
<tr><td>10</td><td>x</td><td>tri-state</td></tr>
<tr><td>11</td><td>x</td><td>GPEN11</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin78 function selection
<table>
<tr><th>CR29 [Bit2]</th><th>CR2A [Bit3-2]</th><th>DIS_HWACPI</th><th>Pin78</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>MSCL2</td></tr>
<tr><td>0</td><td>00</td><td>0</td><td>RSTOUT1#(HW)</td></tr>
<tr><td>0</td><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>RSTOUT1#(SW)</td></tr>
<tr><td>0</td><td>10</td><td>x</td><td>tri-state</td></tr>
<tr><td>0</td><td>11</td><td>x</td><td>GPEN12</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R/W</td><td>Pin77function selection
<table>
<tr><th>CR29 [Bit2]</th><th>CR2A [Bit1-0]</th><th>DIS_HWACPI</th><th>Pin77</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>MSCL2</td></tr>
<tr><td>0</td><td>00</td><td>0</td><td>RSTOUT2#(HW)</td></tr>
<tr><td>0</td><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>RSTOUT2#(SW)</td></tr>
<tr><td>0</td><td>10</td><td>x</td><td>tri-state</td></tr>
<tr><td>0</td><td>11</td><td>x</td><td>GPEN13</td></tr>
</table></td></tr>
</table>

CR 2Bh. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin81 function selection
<table>
<tr><th>CR2B [Bit7-6]</th><th>DIS_HWACPI</th><th>Pin81</th></tr>
<tr><td>00</td><td>0</td><td>PWROK0(HW)</td></tr>
<tr><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>01</td><td>x</td><td>PWROK0(SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN14</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin82 function selection
<table>
<tr><th>CR2B [Bit5-4]</th><th>DIS_HWACPI</th><th>Pin82</th></tr>
<tr><td>00</td><td>0</td><td>PWROK1(HW)</td></tr>
<tr><td>00</td><td>1</td><td>tri-state</td></tr>
<tr><td>01</td><td>x</td><td>PWROK1(SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN15</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin73 function selection
<table>
<tr><th>CR2B [Bit3-2]</th><th>DIS_HWACPI</th><th>Pin73</th></tr>
<tr><td>00</td><td>0</td><td>DPWROK(HW)</td></tr>
<tr><td>00</td><td>1</td><td>output low</td></tr>
<tr><td>01</td><td>x</td><td>DPWROK(SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN16</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R/W</td><td>Pin101 function selection
<table>
<tr><th>CR2B [Bit1-0]</th><th>DIS_HWACPI</th><th>Pin101</th></tr>
<tr><td>00</td><td>0</td><td>RSMRST#(HW)</td></tr>
<tr><td>00</td><td>1</td><td>output low</td></tr>
<tr><td>01</td><td>x</td><td>RSMRST#(SW)</td></tr>
<tr><td>10</td><td>x</td><td>GPEN17</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
</table>

CR 2Ch. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin10 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2C [Bit7-6]</th><th>Pin10</th></tr>
<tr><td>1</td><td>xx</td><td>DTRB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO53</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin9 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2C [Bit5-4]</th><th>Pin9</th></tr>
<tr><td>1</td><td>xx</td><td>RTSB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO52</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin8 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2C [Bit3-2]</th><th>Pin8</th></tr>
<tr><td>1</td><td>xx</td><td>DSRB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO51</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin7 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2C [Bit1-0]</th><th>Pin7</th></tr>
<tr><td>1</td><td>xx</td><td>CTSB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO50</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
</table>

CR 2Dh. Multi-function Pin Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin14 function selection
<table>
<tr><th>CR2A [Bit6]</th><th>CR2D [Bit7-6]</th><th>Pin14</th></tr>
<tr><td>1</td><td>xx</td><td>RIB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO57</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin13 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2D [Bit5-4]</td><td>Pin13</td></tr>
<tr><td>1</td><td>xx</td><td>DCDB#</td></tr>
<tr><td>0</td><td>00</td><td>GPIO56</td></tr>
<tr><td>0</td><td>01</td><td>tri-state</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin12 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2D [Bit3-2]</td><td>Pin12</td></tr>
<tr><td>1</td><td>xx</td><td>SOUTB</td></tr>
<tr><td>0</td><td>00</td><td>GPIO55</td></tr>
<tr><td>0</td><td>01</td><td>IRTX</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin11 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>CR2D [Bit1-0]</td><td>Pin11</td></tr>
<tr><td>1</td><td>xx</td><td>SINB</td></tr>
<tr><td>0</td><td>00</td><td>GPIO54</td></tr>
<tr><td>0</td><td>01</td><td>IRRX</td></tr>
<tr><td>0</td><td>1x</td><td>TACHPWM</td></tr>
</table></td></tr>
</table>

CR 2Fh. Strapping Function Result

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : by 0ss1_ssss

BIT	READ / WRITE	DESCRIPTION
7	R / W	ESPI_EN Strapping result reading
6	R / W	DSW_EN Strapping result reading
5	R / W	DDR4 Strapping result reading
4-3	Reserved	
2	R / W	DIS_HWACPI Strapping result reading
1	R / W	AMDPWR_EN Strapping result reading
0	Reserved	

18.2 Logical Device 1 (Parallel Port)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for PRT.

CR 74h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 3Fh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-3	R / W	ECP FIFO Threshold.
2-0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). **Bits** **2 1 0** 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved. 1 1 1: ECP and EPP – 1.7 mode.

18.3 Logical Device 2 (UARTA)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.

BIT	READ / WRITE	DESCRIPTION
4-2	Reserved	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: UART A clock source is 14.769MHz (24Mhz / 1.625)

18.4 Logical Device 3 (UARTB, IR)

Logical Device 3 (UARTB, IR)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 2 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for Serial Port 2

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.

BIT	READ / WRITE	DESCRIPTION
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved	
1-0	R / W	**Bits** **1 0** 0 0: UART B clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART B clock source is 2 MHz (24 MHz / 12). 1 0: UART B clock source is 24 MHz (24 MHz / 1). 1 1: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: reserved. 1: Through IRRX / IRTX.
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX

IR MODE	IR FUNCTION	IRTX	IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

18.5 Logical Device 5 (Keyboard Controller)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 83h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: 12MHz 1 1: Reserved
5-3	Reserved	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

18.6 Logical Device 6 (CIR)

NOTICE : CR30h of Logic Device 6 does not affect CIR receiving function of MCU.

CR 30h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for CIR.

CR F0h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 08h

BIT	READ / WRITE	DESCRIPTION
7	R/W	CIR TX1 Enbale 0: Disable CIR TX1 1: Enable CIR TX1

BIT	READ / WRITE	DESCRIPTION
6	R/W	CIR TX2 Enable 0: Disable CIR TX2 1: Enable CIR TX2
5-4	Reserved	
3	R/W	CIR wide band filter select 0: Low-pass filter 1: Band-pass filter
2-1	R/W	Timeout margin selection of CIR wide band band-pass filter 00: 200% recording carrier period 01: 100% recording carrier period 10: 50% recording carrier period 11: 25% recording carrier period
0	R/W	Carrier recording mode CIR wide band band-pass filter 0: Second carrier 1: Every carrier

CR F1h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 09h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Highest input period of CIR wide band band-pass filter (unit : us)

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 32h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Lowest input period of CIR wide band band-pass filter (unit : us)

CR F3h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	

BIT	READ / WRITE	DESCRIPTION
5-0	R / W	Recording carrier period of CIR wide band band-pass filter (unit : us)

18.7 Logical Device 7 (GPIO0~GPIO7)

NOTICE :

1. All GPIO pin functions should always be customized by firmware. BIOS / Driver should not touch all configuration registers here and related IO ports unless firmware opens them.

2. Under any situations, CR30h should always be controlled by EC and never be opened for BIOS / Drivers !!

3. Some GPIO group may not have full set of 8 pins (please refer to Chapter 3 & 4), but the corresponding register bits still exist in the chip. Please program those that are needed.

CR 30h. GPIO Device Enable Register

Location: Address 30h

Attribute: Read/Write

Power Well: VSB

Reset by: Varies per bit

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO Group 7 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 7 1: Only LPC can access GPIO Group 7
6	R / W	GPIO Group 6 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 6 1: Only LPC can access GPIO Group 6
5	R / W	GPIO Group 5 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 5 1: Only LPC can access GPIO Group 5
4	R / W	GPIO Group 4 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 4 1: Only LPC can access GPIO Group 4
3	R / W	GPIO Group 3 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 3 1: Only LPC can access GPIO Group 3
2	R / W	GPIO Group 2 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 2 1: Only LPC can access GPIO Group 2
1	R / W	GPIO Group 1 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 1 1: Only LPC can access GPIO Group 1
0	R / W	GPIO Group 0 Access Option. (Controlled by EC) 0: Only mcu can access GPIO Group 0 1: Only LPC can access GPIO Group 0

CR 60h, 61h.
Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select GPIO runtime Interface I/O base address <100h: FF0h> on 16 byte boundary.

CR 70h.
Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for GPIO. (Controlled by EC)

CR E0h. GPIO Data Register
Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Data Register. This register reflects, for both read and write, the register current selected by the GPSEL register. For output ports, the respective bits can be read/ written and produced to pins. The reading data is reflecting to pin status. (Only GPIOA Group is reflecting to data registers.) For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E1h. Interrupt Enable Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Data Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 0: Disable 1: Enable

CR E2h. GPIO Status Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W1C	GPIO Status Register. This register reflects, for both read and write, the register current selected by the GPSEL register.

CR E3h. GPIO I/O Control Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : FFh (Only GPIO Enhance Group1 default vaule is F0h)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Output Enable Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 0: Output mode 1: Input mode

CR E4h. GPIO Inversion Control Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Inversion Control Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 0: No inversion. 1: Inversion input/output.

CR E5h. GPIO PP/OD Control Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Output Type Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 0: Open-Drain 1: Push-Pull

CR E6h. GPIO Interrupt Type Control Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2		Reserved.
1-0	R / W	GPIO Interrupt Type0 Control Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 00h: Status field is trigger by falling edge. 01h: Status field is trigger by rising edge. 10h: Status field is trigger by both edge. 11h: Any trigger

CR E7h. GPIO Output Data Reflection Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R	GPIO Output Data Reflection Register. This register reflects the register current selected by the (GPSEL+8'h0) register.

CR E8h. GPIO Internal Pull Down Control Register (Only GPIO2 group is valid)

Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Internal Pull Down Control Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 0: Disable internal pull down 1: Enable internal pull down GP2 ➔ internal pull down

CR E9h. GPIO Reset Source Type Control Register

Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	R / W	Reserved.
1-0	R / W	GPIO Reset Source Type Control Register. This register reflects, for both read and write, the register current selected by the GPSEL register. 00 : PCI RST# 01 : PWROK 10 : MCU Reset (Software Reset) 11 : RSMRST#

CR EBh. GPIO De-Bounce Clock Option Register

Location: Address EBh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO De-Bounce Clock Option. This register reflects, for both read and write, the register current selected by the GPSEL register. (Only for GPIO Enhance Group) 0: De-bounce clock is 1MHz. 0: De-bounce clock is 1KHz. PS. The CREB[7:0] correspond to GPIOENX port [0:7].

CR ECh. GPIO De-Bounce Type 0 Register

Location: Address ECh
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO De-Bounce Type 0 Register. This register reflects, for both read and write, the register current selected by the GPSEL register. (Only for GPIO Enhance Group)

CR EDh. GPIO De-Bounce Type 1 Register

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO De-Bounce Type 1 Register. This register reflects, for both read and write, the register current selected by the GPSEL register. { De-Bounce Type 0, De-Bounce Type 1} 00: No De-bounce. 01: De-bounce high. (form low to high) 10: De-bounce low. (form high to low) 11: De-bounce high and low. (Only for GPIO Enhance Group)

CR EEh. GPIO De-Bounce Time Control 0 Register

Location: Address EEh
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO De-Bounce Time Control 0 Register. This register reflects, for both read and write, the register current selected by the GPSEL register. (Only for GPIO Enhance Group)

CR EFh. GPIO De-Bounce Time Control 1 Register

Location: Address EFh
Attribute: Read/Write
Power Well: VSB
Reset by: Varies per bit
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO De-Bounce Time Control 1 Register. This register reflects, for both read and write, the register current selected by the GPSEL register. { De-Bounce Time Control 0, De-Bounce Time Control 1} 00: De-Bounce 4 ms 01: De-Bounce 16 ms 10: De-Bounce 32 ms 11: De-Bounce 64 ms (Only for GPIO Enhance Group)

CR F0h. GPIO Group Selection Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	GPIO Group Selection. 4'h0: GPIO Group0 4'h1: GPIO Group1 … 4'hC: GPIO Enhance Group 1

CR F1h. GPIO Software Reset Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W0C	Write 0 to clear GPIO register.

18.8 Logical Device 8 (PORT80 UART)

CR E0h. PORT80 UART Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length selecion) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	R / W	P80_data_mux 0: UART data is from P80 1: UART data is from P81

CR E1h. PORT80 UART Status Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

18.9 Logical Device 9 (GPIO8~9, GPIO 1~8 Alternate Function, GPIO Enhance Group 0~1)

NOTICE :

1. All GPIO pin functions should always be customized by firmware. BIOS / Driver should not touch all configuration registers here.

2. Under any situations, CR30h should always be controlled by EC and never be opened for BIOS / Drivers !!

3. Some GPIO group may not have full set of 8 pins (please refer to Chapter 3 & 4), but the corresponding register bits still exist in the chip. Please program those that are needed.

CR 30h. GPIO Device Enable Register

Location: Address 30h

Attribute: Read/Write

Power Well: VSB

Reset by: Varies per bit

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	GPIO Enhance Group 1 Access Option. 0: Only mcu can access GPIO Enhance Group 1 1: Only LPC can access GPIO Enhance Group 1
3	R / W	GPIO Enhance Group 0 Access Option. 0: Only mcu can access GPIO Enhance Group 0 1: Only LPC can access GPIO Enhance Group 0
2-1	Reserved	
1	R / W	GPIO Group 9 Access Option. 0: Only mcu can access GPIO Group 9 1: Only LPC can access GPIO Group 9
0	R / W	GPIO Group 8 Access Option. 0: Only mcu can access GPIO Group 8 1: Only LPC can access GPIO Group 8

Some GPIO pins have alternate functions and could be selected by two control bits. The definition of the control bits is as the following :

{alternate_sel_bit0, alternate_sel_bit1}

00: GPIO

01: BEEP

10: LRESET#

11: ACPI_OUT

Others: GPIO

The following section describes the control bits for each GPIO group. In the register, bit x stands for pin x in that GPIO group.

CR E0h. GPIO1 Alternate Function Selection Bit 0 Register

Location: Address E0h

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	GPIO Group 1 alternate function selection Bit 0

CR E1h. GPIO1 Alternate Function Selection Bit 1 Register

Location: Address E1h

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	GPIO Group 1 alternate function selection Bit 1

CR E2h. GPIO2 Alternate Function Selection Bit 0 Register

Location: Address E2h

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 2 alternate function selection Bit 0

CR E3h. GPIO2 Alternate Function Selection Bit 1 Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 2 alternate function selection Bit 1

CR E4h. GPIO3 Alternate Function Selection Bit 0 Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 3 alternate function selection Bit 0

CR E5h. GPIO3 Alternate Function Selection Bit 1 Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 3 alternate function selection Bit 1

CR E6h. GPIO4 Alternate Function Selection Bit 0 Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 4 alternate function selection Bit 0

CR E7h. GPIO4 Alternate Function Selection Bit 1 Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 4 alternate function selection Bit 1

CR E8h. GPIO5 Alternate Function Selection Bit 0 Register

Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 5 alternate function selection Bit 0

CR E9h. GPIO5 Alternate Function Selection Bit 1 Register

Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 5 alternate function selection Bit 1

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 5 port 7 to port 0 alternate function {alternate_sel_bit0, alternate_sel_bit1} 00: GPIO 01: BEEP 10: LRESET# 11: ACPI_OUT Others: GPIO

CR EAh. GPIO6 Alternate Function Selection Bit 0 Register

Location: Address EAh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 6 alternate function selection Bit 0 (Note. Only bit 2,3,7 have corresponding pins at GPIO62, GPIO63 and GPIO67.)

CR EBh. GPIO6 Alternate Function Selection Bit 1Register

Location: Address EBh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Group 6 alternate function selection Bit 1 (Note. Only bit 2,3,7 have corresponding pins at GPIO62, GPIO63 and GPIO67.)

CR ECh. GPIO7 Alternate Function Selection Bit 0 Register

Location: Address ECh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO Group 7 alternate function selection Bit0

CR EDh. GPIO7 Alternate Function Selection Bit 1 Register

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO Group 7 alternate function selection Bit 1

CR EEh. GPIO8 Alternate Function Selection Bit 0 Register

Location: Address EEh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	GPIO Group 8 alternate function selection Bit 0

CR EFh. GPIO8 Alternate Function Selection Bit 1 Register

Location: Address EFh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	GPIO Group 8 alternate function selection Bit 1

18.10 Logical Device A (ACPI)

NOTICE : Logic Device A is to control the SWC logic. The ACPI building blocks for MCU is not affected by registers of this logic device.

CR 30h.
Attribute: Read/Write
Power Well: VRTC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: ACPI(SWC) Interface is inactive. 1: ACPI(SWC) Interface is active.

CR 60h, 61h.
Attribute: Read/Write
Power Well: VRTC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select ACPI(SWC) Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.
Attribute: Read/Write
Power Well: VRTC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for ACPI(SWC).

CR E0h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.

<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#
1: PSIN is blocked and cannot affect PSOUT#</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
<tr><td>0</td><td>R / W</td><td>KBXKEY =>
0: Only the pre-determined key combination in sequence can wake up the system.
1: Any character received from the keyboard can wake up the system.</td></tr>
</table>

CR E1h. KBC Wake-Up Index Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Attribute: Read/Write

Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h.
Attribute: Read/Write
Power Well: VRTC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.

CR E4h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable Mouse wake-up 0: Disable mouse wake-up function via PSOUT# 1: Enable mouse wake-up function via PSOUT#
6	R / W	Enable KBC wake-up 0: Disable Keyboard wake-up function via PSOUT# 1: Enable Keyboard wake-up function via PSOUT#
5	R / W	Enable GPIO wake-up 0: Disable GPIO wake-up function via PSOUT# 1: Enable GPIO wake-up function via PSOUT#
4	R / W	Enable CIR wake-up 0: Disable CIR wake-up function via PSOUT# 1: Enable CIR wake-up function via PSOUT#
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2-0	Reserved	

CR E6h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6-0	Reserved	

CR E7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : EFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3-0	Reserved	

CR E8h. CASEOPEN# Event Status

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 80h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W1C	CASEOPEN0# Status 1: caseopen event happeded. 0: caseopen event doesn't happen.
6	R / W1C	SKTOCC# Status 1: sktocc event happeded. 0: sktocc event doesn't happen.
5-0	Reserved	

CR EAh.

Attribute: Read/Write

Power Well: VRTC

Reset by: PWROK(Bit3), RSMRST#(Bit2-0)

Default : 2Eh

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	PWROK_TRIG_L => 0: PWROK keep low or from high to low immediately 1: PWROK work normally.
2-0	R / W	PWROK_DEL => Set the delay time when rising from 3VCC to PWROK 000: 300 ~ 600mS 001: 330 ~ 670mS 010: 390 ~ 730mS 011: 520 ~ 860mS 100: 200 ~ 300mS 101: 230 ~ 370mS 110: 290 ~ 430mS 111: 420 ~ 560mS

CR EBh.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset, PWROK(Bit4), LRESET#(Bit2)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	

BIT	READ / WRITE	DESCRIPTION
6-5	R / W	Power-loss control [Note] (These two bits will determine the system turn on or off after AC resume, from G3 to S5 state.) 0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before the power loss. 1 1: User defined mode for power loss last-state. (The last-state flag is located on "CREC, bit0.")
4	R / W	3VSBSW# enable bit 0: Disable 1: Enable
3	Reserved	
2	R / W	Enable the hunting mode for wake-up events set in CRE4. This bit is cleared when any wake-up event is captured. (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1-0	Reserved	

CR ECh.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	Power-loss Last State Flag 0: ON 1: OFF

CR EEh.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Enable RIB# pin wake-up 0: Disable RIB# pin wake-up function via PME# 1: Enable RIB# pin wake-up function via PME#
4	R / W	Enable RIA# pin wake-up 0: Disable RIA# pin wake-up function via PME# 1: Enable RIA# pin wake-up function via PME#

BIT	READ / WRITE	DESCRIPTION
3	R / W	Enable GP70 pin wake-up 0: Disable GP70 pin wake-up function via PME# 1: Enable GP70 pin wake-up function via PME#
2	R / W	Enable GP70 pin wake-up 0: Disable GP70 pin wake-up function via PSOUT# 1: Enable GP70 pin wake-up function via PSOUT#
1	R / W	Enable RIB# pin wake-up 0: Disable RIB# pin wake-up function via PSOUT# 1: Enable RIB# pin wake-up function via PSOUT#
0	R / W	Enable RIA# pin wake-up 0: Disable RIA# pin wake-up function via PSOUT# 1: Enable RIA# pin wake-up function via PSOUT#

CR F0h. SCI# / PSOUT# route selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO ENHANCE 0 GROUP 0: gpioen0 group can generate SCI# 1: gpioen0 group can generate PSOUT#

CR F1h. SCI# / PSOUT# route selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO ENHANCE 1 GROUP 0: gpioen1 group can generate SCI# 1: gpioen1 group can generate PSOUT#

CR F2h. SCI# / PSOUT# route selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO_IRQ. (Controlled by EC): 0: gpio_irq can generate SCI# 1: gpio_irq can generate PSOUT#

BIT	READ / WRITE	DESCRIPTION
6	R / W	CIR_IRQ: 0: cir_irq can generate SCI# 1: cir_irq can generate PSOUT#
5	R / W	MOUSE_IRQ: 0: mouse_irq can generate SCI# 1: mouse_irq can generate PSOUT#
4	R / W	KEYBOARD_IRQ: 0: keyboard_irq can generate SCI# 1: keyboard_irq can generate PSOUT#
3	R / W	UARTB_IRQ: 0: UARTB_irq can generate SCI# 1: UARTB_irq can generate PSOUT#
2	R / W	UARTA_IRQ: 0: UARTA_irq can generate SCI# 1: UARTA_irq can generate PSOUT#
1	R / W	PRT_IRQ: 0: PRT_irq can generate SCI# 1: PRT_irq can generate PSOUT#
0	Reserved	

CR F3h. SCI# / PSOUT# route selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	MCU_GPIO_OUT: (test mode) 0: MCU_GPIO_OUT can generate SCI# 1: MCU_GPIO_OUT can generate PSOUT#
6	R / W	HM_SCI: 0: HM_SCI can generate SCI# 1: HM_SCI can generate PSOUT#
5	R / W	ECIF2 0: ecif2 can generate SCI# 1: ecif2 can generate PSOUT#
4	R / W	ECIF 1: 0: ecif1 can generate SCI# 1: ecif1 can generate PSOUT#
3	R / W	ECIF 01: 0: ecif01 can generate SCI# 1: ecif01 can generate PSOUT#

BIT	READ / WRITE	DESCRIPTION
2	R / W	ECIF00: 0: ecif00 can generate SCI# 1: ecif00 can generate PSOUT#
1	R / W	HM_IRQ: 0: hm_irq can generate SCI# 1: hm_irq can generate PSOUT#
0	Reserved	

CR F4h. SCI# configuration

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 0Dh

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	SCI Output Mode (SCI_PSMD): 0: Level mode 1: Pulse mode
2	R / W	SCI_OD: 0: SCI is push-pull signal 1: SCI is open-drain signal.
1	Reserved	
0	R / W	SCI_INV : 0: Normal operation 1: Inverse SCI signal

CR F5h. SMI# configuration

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 0Dh

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	SMI Output Mode (SMI_PSMD) 0: SMI level mode 1: SMI pulse mose enable
2	R / W	SMI_OD: 0: SMI is push-pull signal 1: SMI is open-drain signal
1	R / W	SMI_IRQ_EN : 0: Disable SMI to SIRQ path. 1: SMI routes to SIRQ channel 2

BIT	READ / WRITE	DESCRIPTION
0	R / W	SMI_INV : 0: Normal operation 1: Inverse SMI signal

CR F6h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable
2	R / W	RESETCON# signal to control PWROK 0: Disable 1: Enable
1	R / W	ATXPGD signal to control PWROK 0: Enable 1: Disable
0	R / W	Route to PWROK source selection 0: PSON# 1: SLP_S3#

CR F7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	Mask WDTO to affect PWROK 0: Mask enable 1: Mask disable
0	R / W	LV_DETECT_L 0: AMD power sequence detect level and time delay 1: AMD power sequence non detect level but time delay

CR F8h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	SLPS3 to VSB3VSW debounce select 0: Enable 1:Disable
2	R / W	SLPS3 to PWROK debounce select 0: Enable 1:Disable
1-0	Reserved	

CR F9h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W1C	PME status of the RIB# pin event Write 1 to clear this status
6	R / W1C	PME status of the RIA# pin event Write 1 to clear this status
5	R / W1C	PME status of the GP70 event Write 1 to clear this status
4	R / W1C	PME status of the Mouse event Write 1 to clear this status
3	R / W1C	PME status of the KBC event Write 1 to clear this status
2	R / W1C	PME status of the PRT IRQ event Write 1 to clear this status
1	R / W1C	PME status of the URA IRQ event Write 1 to clear this status
0	R / W1C	PME status of the URB IRQ event Write 1 to clear this status

CR FAh.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	

BIT	READ / WRITE	DESCRIPTION
3	R / W1C	PME status of the HM IRQ event Write 1 to clear this status
2	R / W1C	PME status of the WDTO IRQ event Write 1 to clear this status
1	R / W1C	PME status of the RIA IRQ event Write 1 to clear this status
0	R / W1C	PME status of the RIB IRQ event Write 1 to clear this status

CR FBh.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable PME interrupt of the HDM IRQ event 1: Enable PME interrupt of the HDM IRQ event
6	R / W	0: Disable PME interrupt of the RIB IRQ event 1: Enable PME interrupt of the RIB IRQ event
5	R / W	0: Disable PME interrupt of the RIA IRQ event 1: Enable PME interrupt of the RIA IRQ event
4	R / W	0: Disable PME interrupt of the URB IRQ event 1: Enable PME interrupt of the URB IRQ event
3	R / W	0: Disable PME interrupt of the URA IRQ event 1: Enable PME interrupt of the URA IRQ event
2	R / W	0: Disable PME interrupt of the PRT IRQ event 1: Enable PME interrupt of the PRT IRQ event
1	R / W	0: Disable PME interrupt of the KBC event 1: Enable PME interrupt of the KBC event
0	R / W	0: Disable PME interrupt of the Mouse event 1: Enable PME interrupt of the Mouse event

CR FCh.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	0: Enable PME interrupt of the CIRWAKEUP event. 1: Disable PME interrupt of the CIRWAKEUP event.

BIT	READ / WRITE	DESCRIPTION
1	R / W	0: Disable PME interrupt of the GPIO IRQ event 1: Enable PME interrupt of the GPIO IRQ event
0	R / W	0: Disable PME interrupt of the WDTO IRQ event 1: Enable PME interrupt of the WDTO IRQ event

18.11 Logical Device B (EC Space)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: EC Space interface is inactive. 1: EC Space interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the EC Space interface base address <100h : FF8h> aligned to an eight-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select the IRQ resource for EC Space.(MCU to Host Interrupt)

CR E0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	Beep Function Enable 0: Disable 1: Enable
5-4	Reserved	

BIT	READ / WRITE	DESCRIPTION
3	R / W	Disconnect 8042 KBC from 4 PS2 pins (DISCON_KBCPINS) 0: The 4 PS2 pins were connected to KBC when VCC arrived 1: The 4 PS2 pins kept NOT tied to KBC when VCC arrived Notes : 1. With this bit cleared (as 0), when function of the 4 PS2 pins was switched to functions other than PS2 by external debug daughter board, they won't be tied to KBC any more when VCC arrives. 2. With this bit cleared (as 0), once KBC took over the 4 PS2 pins after VCC arrives, the only way to break this connection before exiting S0 state is to set this bit as 1, by LPC or MCU FW. External debug daughter board cannot help under this situation.
2-0	Reserved	

CR E3h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Switch Reg Enable 1 When SBI_CFG_EN = 0 0: the connection of switch 1 is controlled by ATXPGD (ATXPGD is low, switch 1 is dis-connected. ATXPGD is high, switch 1 is connected) 1: the connection of switch 1 is controlled by Switch Control 1 When SBI_CFG_EN = 1 0: the connection of switch 1 is controlled by Switch Control 1 1: the connection of switch 1 is controlled by ATXPGD (ATXPGD is low, switch 1 is dis-connected. ATXPGD is high, switch 1 is connected)
6	R / W	Switch Control 1 0: switch 1 is always dis-connected. 1: switch 1 is alywas connected.

BIT	READ / WRITE	DESCRIPTION
5	R / W	Switch Reg Enable 2 When SBI_CFG_EN = 0 0: the connection of switch 2 is controlled by ATXPGD (ATXPGD is low, switch 2 is dis-connected. ATXPGD is high, switch 2 is connected) 1: the connection of switch 2 is controlled by Switch Control 2 When SBI_CFG_EN = 1 0: the connection of switch 2 is controlled by Switch Control 2 1: the connection of switch 2 is controlled by ATXPGD (ATXPGD is low, switch 2 is dis-connected. ATXPGD is high, switch 2 is connected)
4	R / W	Switch Control 2 0: switch 2 is always dis-connected. 1: switch 2 is alywas connected.
3	R / W	Switch Reg Enable 3 When SBI_CFG_EN = 0 0: the connection of switch 3 is controlled by ATXPGD (ATXPGD is low, switch 3 is dis-connected. ATXPGD is high, switch 3 is connected) 1: the connection of switch 3 is controlled by Switch Control 3 When SBI_CFG_EN = 1 0: the connection of switch 3 is controlled by Switch Control 3 1: the connection of switch 3 is controlled by ATXPGD (ATXPGD is low, switch 3 is dis-connected. ATXPGD is high, switch 3 is connected)
2	R / W	Switch Control 3 0: switch 3 is always dis-connected. 1: switch 3 is alywas connected.
1-0	Reserved	

CR E4h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin71 function selection
<table>
<tr><th>CR29 [Bit6-5]</th><th>DIS_HWACPI</th><th>LDB CRE4[Bit7]</th><th>Pin71</th></tr>
<tr><td>00</td><td>0</td><td>0</td><td>3VSBSW#(HW)</td></tr>
<tr><td>00</td><td>0</td><td>1</td><td>LATCH_BKFD_CUT#(HW)</td></tr>
<tr><td>00</td><td>1</td><td>x</td><td>tri-state</td></tr>
<tr><td>01</td><td>x</td><td>x</td><td>3VSBSW#(SW)</td></tr>
<tr><td>10</td><td>x</td><td>x</td><td>LATCH_BKFD_CUT#(SW)</td></tr>
<tr><td>11</td><td>x</td><td>x</td><td>GPEN07</td></tr>
</table></td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin74 function selection
<table>
<tr><th>LDB CRE4[Bit6-5]</th><th>Pin74</th></tr>
<tr><td>00</td><td>GPIO95</td></tr>
<tr><td>01</td><td>BKFD_CUT(HW)</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin89 function selection
<table>
<tr><th>LDB CRE4 [Bit3-2]</th><th>CR29 [Bit7]</th><th>Pin89</th></tr>
<tr><td>00</td><td>0</td><td>SLP_SUS#</td></tr>
<tr><td>00</td><td>1</td><td>GPIO93</td></tr>
<tr><td>01</td><td>x</td><td>VSB3VSW#(HW)</td></tr>
<tr><td>10</td><td>x</td><td>VSB3VSW#(SW)</td></tr>
<tr><td>11</td><td>x</td><td>tri-state</td></tr>
</table></td></tr>
<tr><td>1</td><td colspan="2">Reserved</td></tr>
<tr><td>0</td><td>R / W</td><td>SPI Switch Controller (Mode III)
0: Disable
1: Enable</td></tr>
</table>

18.12 Logical Device C (RTC Timer)

CR 30h. RTC Timer configuration register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Issue wakeup event to PME 0: Disable 1: Enable
4	R / W	Issue wakeup event to PSOUT 0: Disable 1: Enable
3	R / W	RTC power down configuration register when AC LOSS 0: Not powered down. 1: Powered down.
2	R / W	Daylight saving time configuration register 0: Disable 1: Enable
1	R / W	24-hour or 12-hour selection 0: In 24-hour mode (HOUR[5:0] = 00 ~ 23) 1: In 12-hour mode (HOUR[4:0] = 01 ~ 12). PM toggles every 12hours.
0	R / W	RTC Function configuration register 0: Disable 1: Enable

CR E0h. Second of RTC

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	Second of RTC (SECOND = 00 ~ 59)

CR E1h. Minute of RTC

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	Minute of RTC (MINUTE = 00 ~ 59)

CR E2h. Hour of RTC

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Hour of RTC 24-hour mode HOUR[5:0] = 00 ~ 23 12-hour mode HOUR[4:0] = 01 ~12 HOUR[5] = 0 => AM HOUR[5] = 1 => PM

CR E3h. Enumeration of day in the month

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Enumeration of day in the month (DAY = 01 ~ 31)

CR E4h. Days of the week

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	Days of the week (WEEKDAY = 0 ~ 6) 0 => Sunday; 1 => Monday; … 6 => Saturday;

CR E5h. Month of RTC

Attribute: Read/Write
Power Well: VRTC

Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4-0	R / W	Month of RTC (MONTH = 01 ~ 12) 01 => January; 02 => February; … 12 => December;

CR E6h. Year of RTC
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Year of RTC (YEAR = 00 ~ 99)

CR E7h. Alarm of weekday
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable Alarm of weekday 1: Disabe Alarm of weekday
6-3	Reserved	
2-0	R / W	Alarm of weekday (0 ~ 6)

CR E8h. Alarm of hour
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable Alarm of hour 1: Disabe Alarm of hour
6	Reserved	
5-0	R / W	Alarm of hour (00 ~ 23 or 01 ~ 12)

CR E9h. Alarm of minute
Attribute: Read/Write

Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable Alarm of minute 1: Disabe Alarm of minute
6-0	R / W	Alarm of minute (00 ~ 59)

CR EAh. Interrupt Enable Bits
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	Interrupt enable of time alarm. 0: Disable 1: Enable

CR EBh. Interrupt flags
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	The flag of time alarm. This bit can be cleared to 0 by writing 1 to it.

CR ECh. Alarm of year、month and day
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 07h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	0: Enable Alarm of year 1: Disabe Alarm of year
1	R / W	0: Enable Alarm of month 1: Disabe Alarm of month
0	R / W	0: Enable Alarm of day 1: Disabe Alarm of day

CR EDh. Alarm of year

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Alarm of year (00 ~ 99)

CR EEh. Alarm of month

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4-0	R / W	Alarm of month (01 ~ 12)

CR EFh. Alarm of day

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Alarm of day (01 ~ 31)

CR F0h. Alarm of second

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable Alarm of second 1: Disabe Alarm of second
6-0	R / W	Alarm of second (00 ~ 59)

18.13 Logical Device D (Deep Sleep, Power Fault)

CR 30h. Deep Sleep configuration register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : A0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_SLPSUS_PULLUP (test mode) 0: Enable SLP_SUS# internal pull-up. 1: Disable SLP_SUS# internal pull-up.
6-5	Reserved	
4	R / W	dsw_wake_opt (test mode) 0: The PSOUT# will assert until SLPS3# high when deep s5 wakeup event happened. 1: The PSOUT# will assert until RSMRST_L high and SLP_SUS_L high when deep s5 wakeup event happened. **PS. This bit only active when DSW_EN & (Deep S5 Enable | Deep S3 Enable)**
3-2	Reserved	
1	R / W	Deep S3 Enable 0: If SLP_S3# state will not enter Deep S3 state. 1: If SLP_S3# state will enter Deep S3 state.
0	R / W	Deep S5 Enable 0: Disable Deep S5 function when into S5 state (SLP_S5#). 1: Enable Deep S5 function when into S5 state (SLP_S5#).

CR E0h. Deep Sleep wake up PSOUT# delay time

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **20h** (Default: 512ms)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : **04h** (Default: 128 ms)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Deep Sleep Delay Time Control

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 05h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6-0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

CR E3h. SUSACK Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 6Eh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SUSACK Counter Register. When system enter or exit DSW State, SUSACK will wait a delay time to pull down or up. Default is 220ms. Example:Reg = 0 -> Delay = 0~1ms Reg = 1 -> Delay = 1~3ms Reg = 2 -> Delay = 3~5ms

CR E4h. Deep S5 Front Panel Green & Yellow LED control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-4	R / W	**Deep S5**_YLW_BLK_FREQ bits (This function affects by LDB CRE6 Bit 5) 000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 001: YLW_LED outputs 0.0625Hz. 010: YLW_LED outputs 0.125Hz. 011: YLW_LED outputs 0.25Hz. 100: YLW_LED outputs 0.5Hz 101: YLW_LED outputs 1Hz. 110: YLW_LED outputs 2Hz. 111: YLW_LED outputs low.
3	Reserved	
2-0	R / W	**Deep S5**_GRN_BLK_FREQ bits (This function affects by LDB CRE6 Bit 4) 000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 001: GRN_LED outputs 0.0625Hz. 010: GRN_LED outputs 0.125Hz. 011: GRN_LED outputs 0.25Hz. 100: GRN_LED outputs 0.5Hz 101: GRN_LED outputs 1Hz. 110: GRN_LED outputs 2Hz. 111: GRN_LED outputs low.

CR E5h. Deep S3 Front Panel Green & Yellow LED control register
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-4	R / W	**Deep S3**_YLW_BLK_FREQ bits (This function affects by LDB CRE6 Bit 7) 000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 001: YLW_LED outputs 0.0625Hz. 010: YLW_LED outputs 0.125Hz. 011: YLW_LED outputs 0.25Hz. 100: YLW_LED outputs 0.5Hz 101: YLW_LED outputs 1Hz. 110: YLW_LED outputs 2Hz. 111: YLW_LED outputs low.
3	Reserved	

BIT	READ / WRITE	DESCRIPTION
2-0	R / W	**Deep S3**_GRN_BLK_FREQ bits (This function affects by LDB CRE6 Bit 6) 000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 001: GRN_LED outputs 0.0625Hz. 010: GRN_LED outputs 0.125Hz. 011: GRN_LED outputs 0.25Hz. 100: GRN_LED outputs 0.5Hz 101: GRN_LED outputs 1Hz. 110: GRN_LED outputs 2Hz. 111: GRN_LED outputs low.

CR E6h. Deep Sleep LED Enable register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Deep S3_YLW_BLK_FREQ : 0: Depend on setting of CRF2h, bit7-4. 1: Always output high.
6	R / W	Deep S3_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3-0. 1: Always output high.
5	R / W	Deep S5_YLW_BLK_FREQ : 0: Depend on setting of CRF6h, bit7-4. 1: Always output high.
4	R / W	Deep S5_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3-0. 1: Always output high.
3-0	Reserved	

CR E7h. Front Panel Yellow & Green LED control register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 88h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**YLW_LED_RST#** (Default =1) 0: YLW_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: YLW_BLK_FREQ will be kept when into S3~S5 state.
6	R / W	YLW_LED_POL 0: YLW_LED output is active low. (Default) 1: YLW_LED output is active high.
5	R / W	**GRN_LED_RST#** (Default= 0) 0: GRN_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: GRN_BLK_FREQ will be kept when into S3~S5 state.

BIT	READ / WRITE	DESCRIPTION
4	R / W	GRN_LED_POL 0: GRN_LED output is active low. (Default) 1: GRN_LED output is active high.
3	R / W	**AUTO_EN** (Powered by VSB, RSMRST# reset , default = 1) 0: GRN_LED and YLW_LED are controlled by GRN_ LED_ RST, GRN_BLK_FREQ and YLW_LED_RST, YLW_BLK_FREQ bits. 1: GRN_LED and YLW_LED are controlled by “SLP_S5#” and “SLP_S3#”.
2-0	Reserved	

CR E8h. Front Panel Yellow & Green LED control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 77h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-4	R / W	**YLW_BLK_FREQ** bits (The reset depends on bit6,YLW_LED_RST#) 000: High-Z. (The output type of YLW_LED is open-drain.) 001: YLW_LED outputs 0.0625Hz. 010: YLW_LED outputs 0.125Hz. 011: YLW_LED outputs 0.25Hz. 100: YLW_LED outputs 0.5Hz 101: YLW_LED outputs 1Hz. 110: YLW_LED outputs 2Hz. 111: YLW_LED outputs low. (Default)
3	Reserved	
2-0	R / W	**GRN_BLK_FREQ** bits (The reset depends on bit6, GRN_LED_RST#) 000: High-Z. (The output type of YLW_LED is open-drain.) 001: GRN_LED outputs 0.0625Hz. 010: GRN_LED outputs 0.125Hz. 011: GRN_LED outputs 0.25Hz. 100: GRN_LED outputs 0.5Hz 101: GRN_LED outputs 1Hz. 110: GRN_LED outputs 2Hz. 111: GRN_LED outputs low. (Default)

CR F0h. Power Fault Control Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 70h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	V_COMP3 Detect Enable 0: Disable 1: Enable
6	R / W	V_COMP2 Detect Enable 0: Disable 1: Enable
5	R / W	V_COMP1 Detect Enable 0: Disable 1: Enable
4	R / W	V_COMP0 Detect Enable 0: Disable 1: Enable
3-2	Reserved	
1	R / W	Power Fault Status. Write 1 Clear.
0	R / W	Power Fault Enable 0: Disable 1: Enable

CR F1h. Power Fault Voltage Setting Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : AAh

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	V_COMP3 high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%
5-4	R / W	V_COMP2 high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%
3-2	R / W	V_COMP1 high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%

BIT	READ / WRITE	DESCRIPTION
1-0	R / W	V_COMP0 high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%

CR F3h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset(Bit1:0), RSMRST#(Bit6:2)

Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">Reserved</td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin72 function selection
<table>
<tr><th>LDD CRF3 [Bit5-4]</th><th>DIS_HWACPI</th><th>Pin72</th></tr>
<tr><td>00</td><td>0</td><td>DEEP_S5_1</td></tr>
<tr><td>00</td><td>1</td><td>output low</td></tr>
<tr><td>01</td><td>x</td><td>CASEOPEN1#</td></tr>
<tr><td>10</td><td>x</td><td>DEEP_S5_1(SW)</td></tr>
<tr><td>11</td><td>x</td><td>GPIO65</td></tr>
</table></td></tr>
<tr><td>4-2</td><td>R / W</td><td>Pin70 function selection
<table>
<tr><th>LDD CRF3 [Bit3-1]</th><th>DIS_HWACPI</th><th>Pin70</th></tr>
<tr><td>000</td><td>0</td><td>DEEP_S5_0</td></tr>
<tr><td>000</td><td>1</td><td>output low</td></tr>
<tr><td>001</td><td>x</td><td>VSB3VSW(HW)</td></tr>
<tr><td>010</td><td>x</td><td>LATCH_BKFD_CUT(HW)</td></tr>
<tr><td>011</td><td>x</td><td>DEEP_S5_0(SW)</td></tr>
<tr><td>100</td><td>x</td><td>VSB3VSW(SW)</td></tr>
<tr><td>101</td><td>x</td><td>Reserved</td></tr>
<tr><td>110</td><td>x</td><td>GPIO66</td></tr>
<tr><td>111</td><td>x</td><td>Reserved</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>R / W</td><td>Pin120 function selection
<table>
<tr><td>LDD CRF3 [Bit1-0]</td><td>Pin120</td></tr>
<tr><td>00, 10, 11</td><td>PECI</td></tr>
<tr><td>01</td><td>AMDSID</td></tr>
</table>
Pin118 function selection
<table>
<tr><td>LDD CRF3 [Bit1:0]</td><td>Pin118</td></tr>
<tr><td>00</td><td>PWR_FAULT#</td></tr>
<tr><td>x1</td><td>AMDSIC</td></tr>
<tr><td>10</td><td>GP87</td></tr>
</table></td></tr>
</table>

18.14 Logical Device E (TACHIN/PWMOUT Assignment)

CR E0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin4 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin3 TACHPWM assign 0000: PWMOUT0 0001: PWMOUT1 0010: PWMOUT2 0011: PWMOUT3 0100: PWMOUT4 0101: PWMOUT5 0110: PWMOUT6 0111: PWMOUT7 1000: TACHIN0 1001: TACHIN1 1010: TACHIN2 1011: TACHIN3 1100: TACHIN4 1101: TACHIN5 1110: TACHIN6 1111: TACHIN7

CR E1h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin122 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin121 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E2h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin98 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin95 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E3h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin125 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin124 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E4h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin126 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin37 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E5h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin103 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin127 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E6h.
Attribute: Read/Write
Power Well: VSB

Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	Pin104 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved	

CR E8h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin8 TACHPWM assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin7 TACHPWM assign (same as LDE CRE0 Bit3-0)

CR E9h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin10 TACHPWM19 assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin9 TACHPWM18 assign (same as LDE CRE0 Bit3-0)

CR EAh.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin12 TACHPWM21 assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin11 TACHPWM20 assign (same as LDE CRE0 Bit3-0)

CR EBh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Pin14 TACHPWM23 assign (same as LDE CRE0 Bit3-0)
3-0	R / W	Pin13 TACHPWM22 assign (same as LDE CRE0 Bit3-0)

18.15 Logical Device F (Function Register)

CR E3h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	LCLK_FRQ[7:0] LCLK / (31.25KHz * 2) = LCLK_FRQ Example: 33MHz / (31.25KHz *2) = 11'h210 = 11'd528 24MHz / (31.25KHz *2) = 11'h180 = 11'd384

CR E4h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	LCLK_FRQ[10:8] LCLK / (31.25KHz * 2) = LCLK_FRQ Example: 33MHz / (31.25KHz *2) = 11'h210 = 11'd528 24MHz / (31.25KHz *2) = 11'h180 = 11'd384

CR E5h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	EN_CALI 0: Disable Oscillator free calibrate 1: Enable Oscillator free calibrate

CR E8h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
3-2	R / W	DDR4 VDDQ_EN Selection:
1-0	R / W	DDR4 VPP_EN Selection:

CR E9h. PWR_FAULT DETECT TIME REGISTER

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1-0	R / W	Power Fault detect time select: 00: 20ms ~35ms 01: 1.5s ~ 2s 10: 93.75ms ~ 125ms (Default) 11: 187.5ms ~ 250ms

CR EAh. PWR_FAULT DETECT TIME REGISTER

Attribute: Read/Write
Power Well: VRTC
Reset by: VPS
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
0	R / W	ATX5VSB Control Register: 0: Enable ATX5VSB Function 1: Disable ATX5VSB Function

19. SPECIFICATIONS

19.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
VBAT	RTC Battery Voltage VBAT	2.2 to 4.0	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

19.2 DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

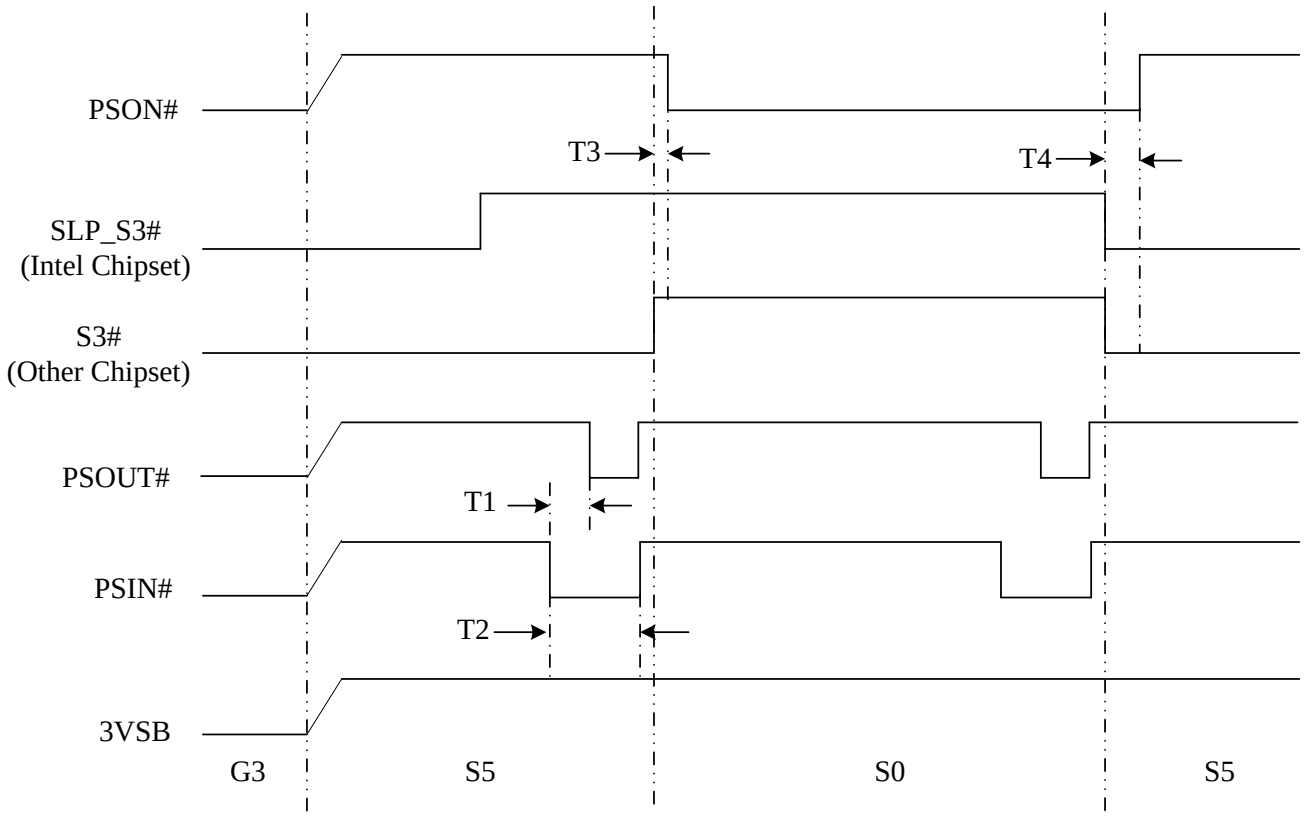
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	IBAT			2.4	µA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			20	mA	VSB ,VCC ,AVSB = 3.3 V LRESET = High IOCLK = 48MHz All GPIO pins are tri-state.
VCC Quiescent Current	IVCC			1	mA	VSB ,VCC ,AVSB = 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
Vtt Quiescent Current	IVTT			1	mA	VSB ,VCC ,AVSB = 3.3 V VTT = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
AIN – Analog input						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
AOUT – Analog output						
IN_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{gp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
$O8_{p3}$ – 3.3V Output pin with 8mA source-sink capability						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = -8 mA
OD8p5 – 5V Open-drain output pin with 8mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
O12p3 – 5V Output pin with 12mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD12p3 – 3.3V Open-drain output pin with 12mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD12p5 – 5V Open-drain output pin with 12mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
O24p3 – 3.3V Output pin with 24mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA
OD24p5 – 5V Open-drain output pin with 24mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
I/O$_{V3}$ – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275*V_{tt}		0.5*V_{tt}	V	
Input High Voltage	V_{IH}	0.55*V_{tt}		0.725*V_{tt}	V	
Output Low Voltage	V_{OL}			0.25*V_{tt}	V	
Output High Voltage	V_{OH}	0.75*V_{tt}			V	
Hysterisis	V_{Hys}	0.1*V_{tt}			V	

20. AC CHARACTERISTICS

20.1 Power On / Off Timing

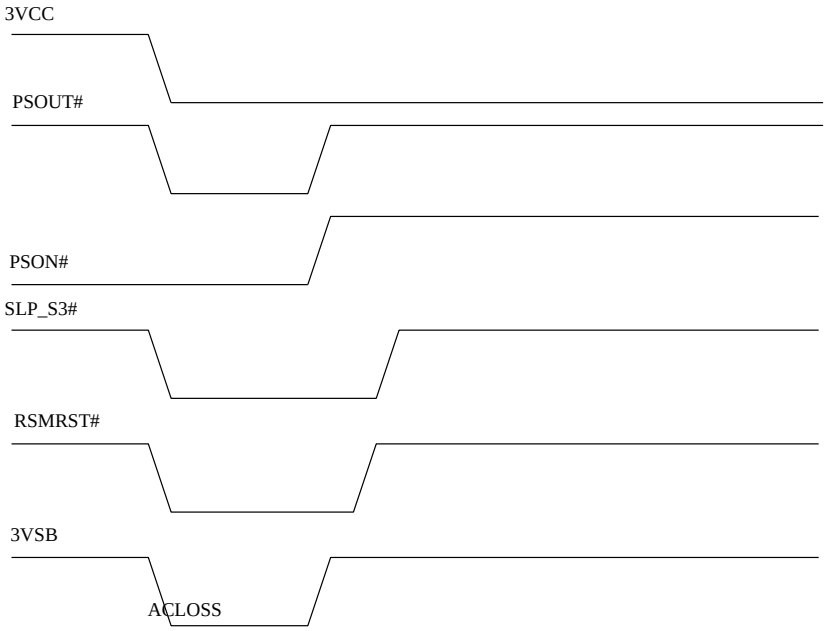


	T1	T2	T3	T4
IDEAL TIMING	48ms~66ms	Over 64ms at least	< 10ns	15ms~32ms

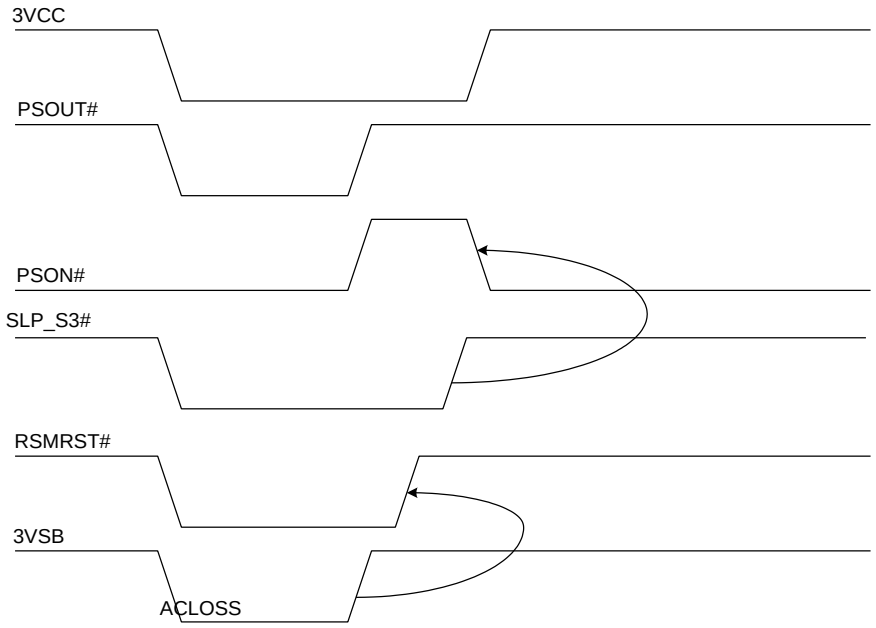
20.2 AC Power Failure Resume Timing

(1) Logical Device A, CR [EBh] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)



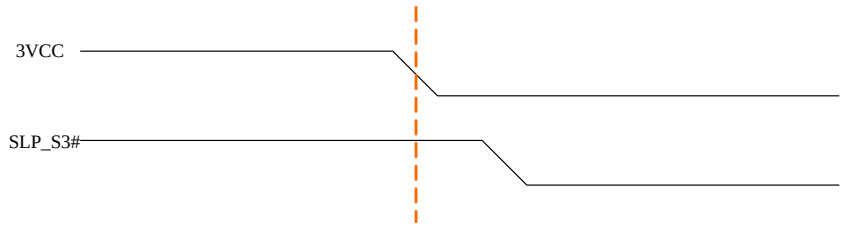
(2) Logical Device A, CR [Ebh] bits [6:5]=01 means “ON” state.
(“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

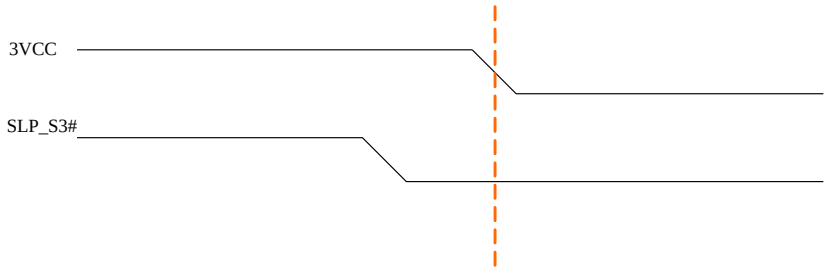
1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6686D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR Ebh and bit 4 of CR Ech in Logical Device A.

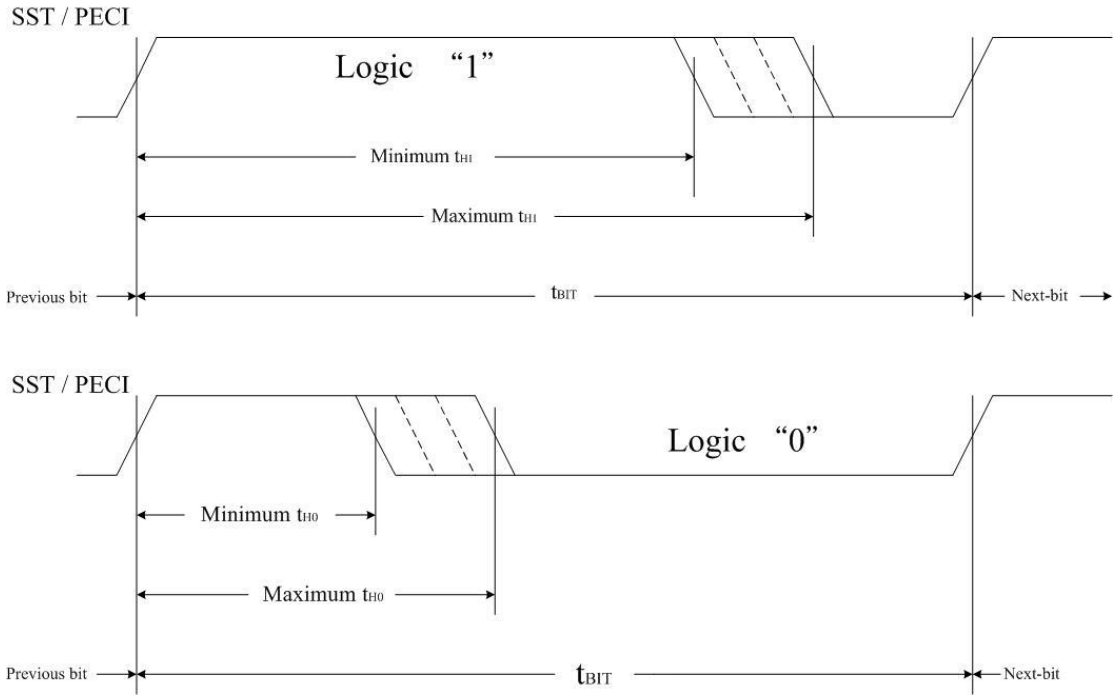
CR Ebh

BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR Ech

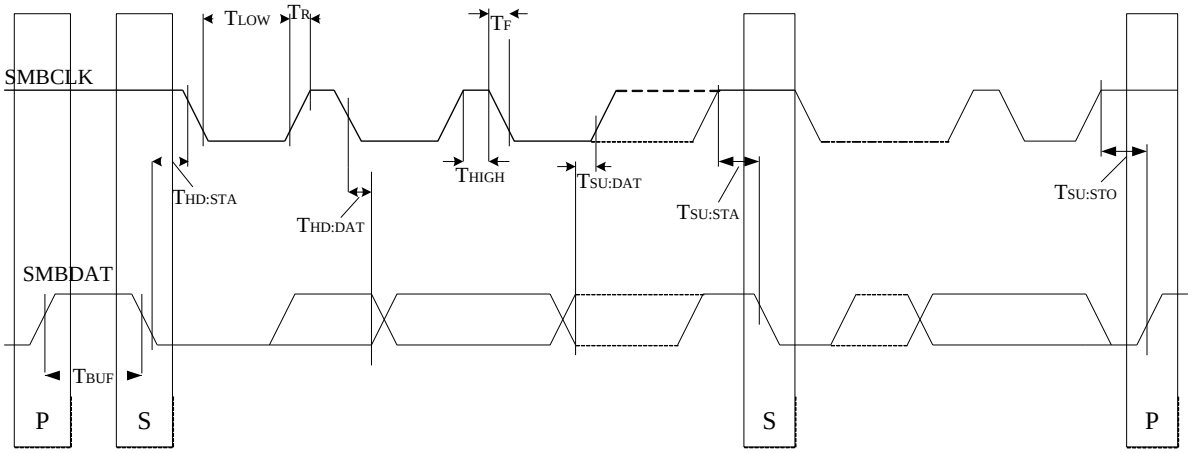
BIT	READ/WRITE	DESCRIPTION
0	R / W	Power-loss Last State Flag. 0: ON 1: OFF

20.3 PECI Timing



SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

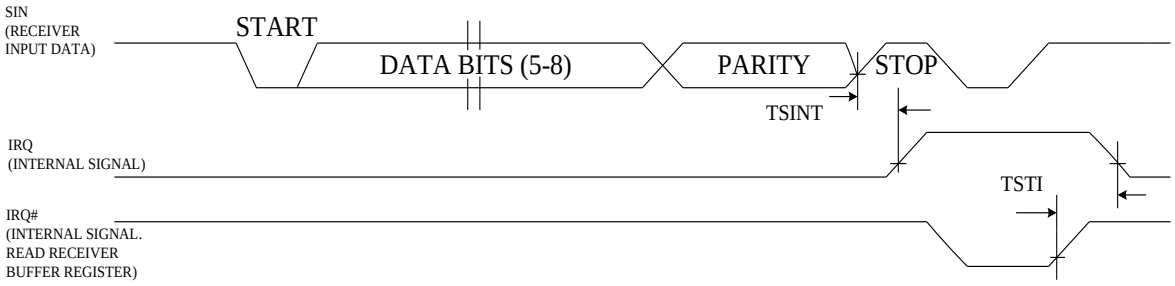
20.4 SMBus Timing



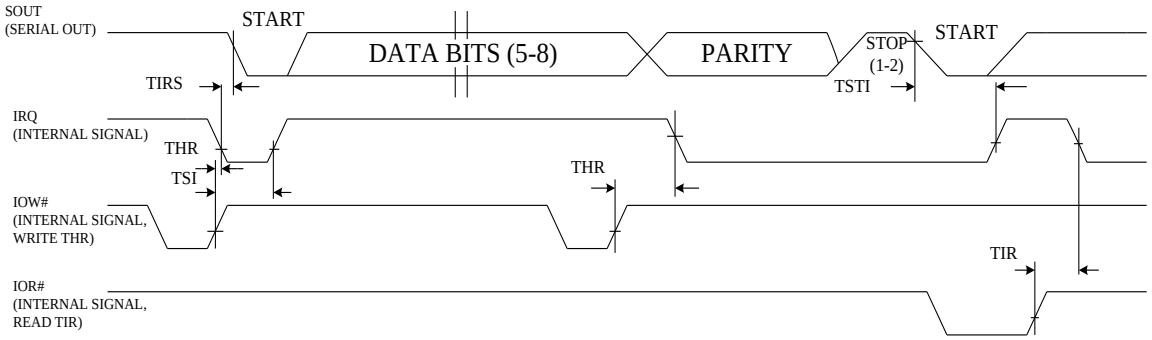
20.5 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

Receiver Timing

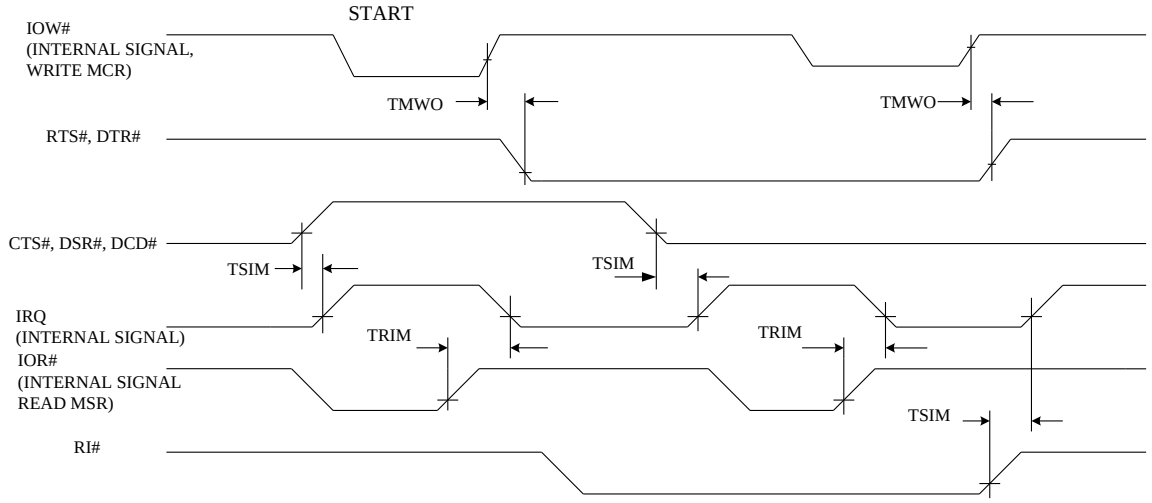


UART Transmitter Timing



20.6 Modem Control Timing

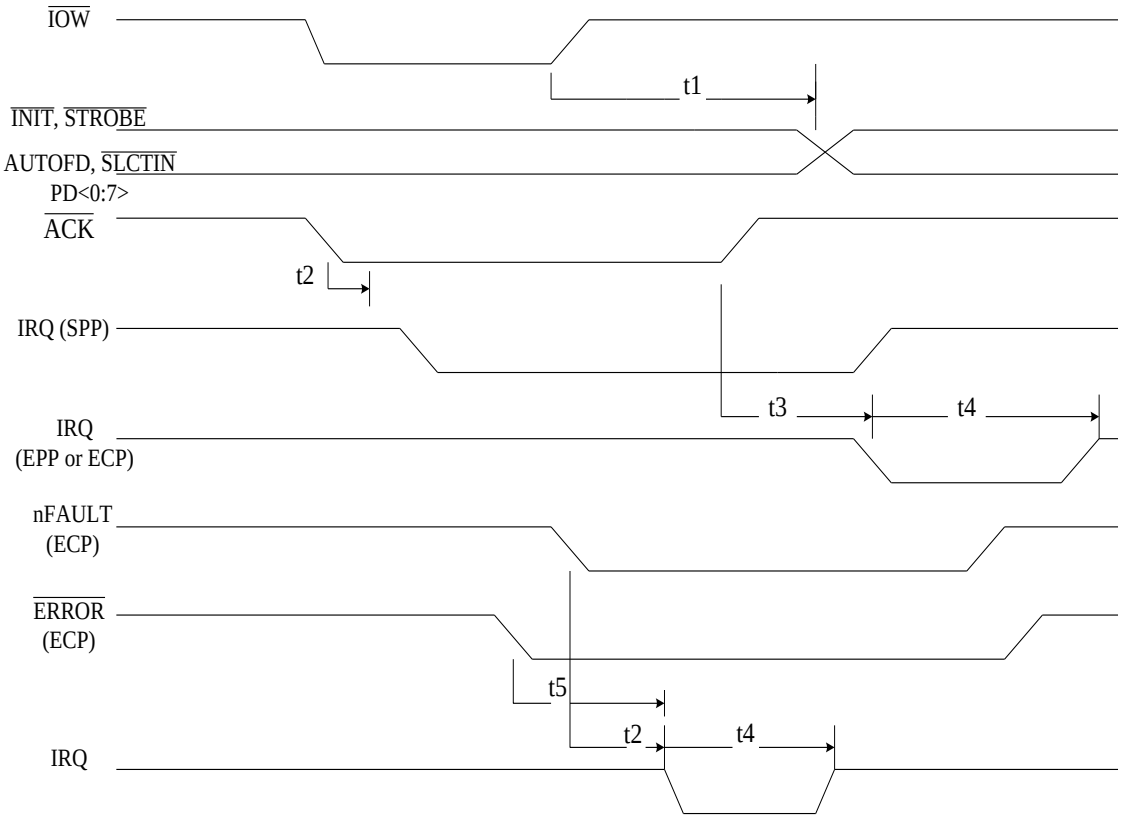
MODEM Control Timing



20.7 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, INDEX, STROBE, AUTOFD Delay from IOW	t1			100	nS
IRQ Delay from ACK, nFAULT	t2			60	nS
IRQ Delay from IOW	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
ERROR Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, INDEX, STROBE, AUTOFD Delay from IOW	t1			100	nS
IRQ Delay from ACK, nFAULT	t2			60	nS
IRQ Delay from IOW	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
ERROR Active to IRQ Active	t5			105	nS

20.7.1 Parallel Port Timing



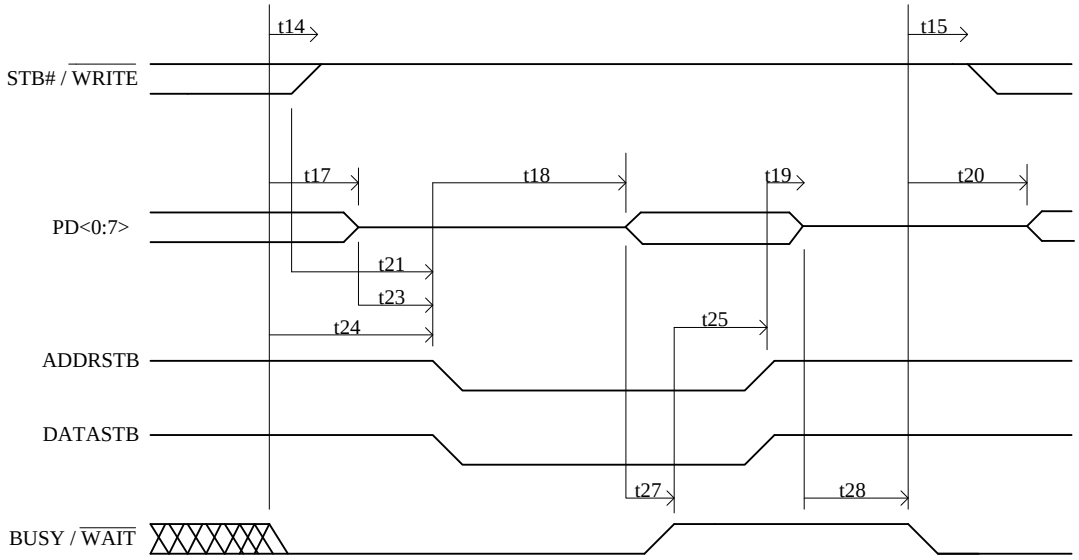
20.7.2 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

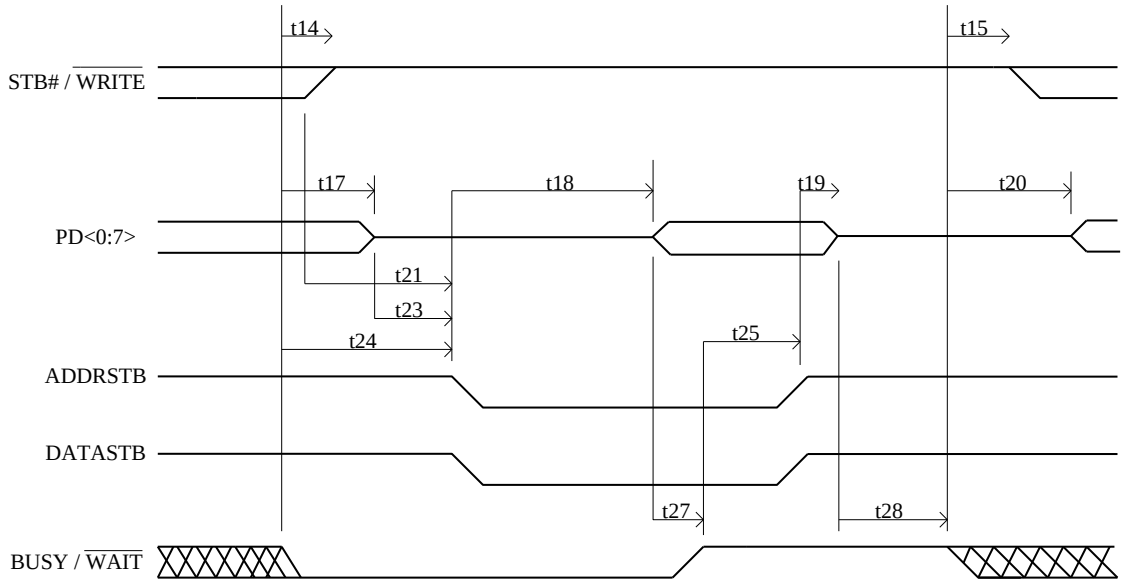
20.7.3 EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)



20.7.4 EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



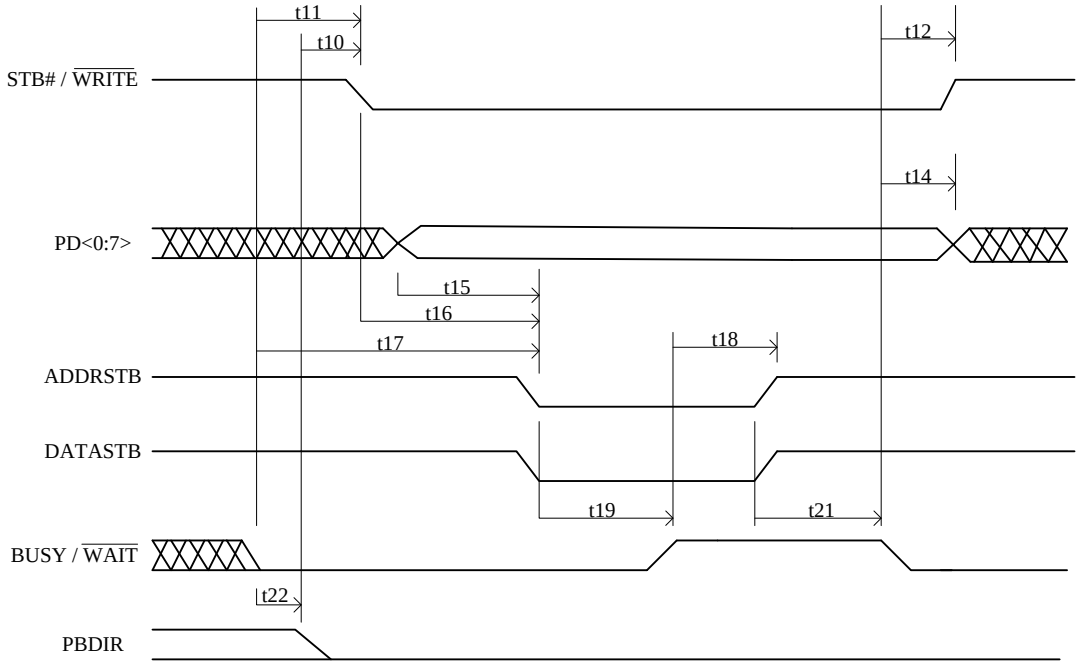
20.7.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to WRITE Asserted	t10	0		nS
WAIT Asserted to WRITE Asserted	t11	60	185	nS
WAIT Asserted to WRITE Change	t12	60	185	nS
WAIT Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
WAIT Asserted to Command Asserted	t17	60	210	nS
WAIT Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to WAIT Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to WAIT Asserted	t21	0		nS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to IOW Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
IOW Deasserted to Ax Invalid	t3	10		nS
WAIT Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to WAIT Deasserted	t5	10		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{IOW}$ Deasserted to $\overline{IOW}$ or $\overline{IOR}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{IOW}$ Deasserted	t7	0	24	nS
$\overline{WAIT}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{IOW}$ Asserted to $\overline{WAIT}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{WRITE}$ Asserted	t10	0		nS
$\overline{WAIT}$ Asserted to $\overline{WRITE}$ Asserted	t11	60	185	nS
$\overline{WAIT}$ Asserted to $\overline{WRITE}$ Change	t12	60	185	nS
$\overline{IOW}$ Asserted to PD Valid	t13	0	50	nS
$\overline{WAIT}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{IOW}$ to Command Asserted	t16	5	35	nS
$\overline{WAIT}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{WAIT}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{WAIT}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{WAIT}$ Asserted	t21	0		nS
$\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid	t22	0		nS
$\overline{WRITE}$ to Command Asserted	t16	5	35	nS

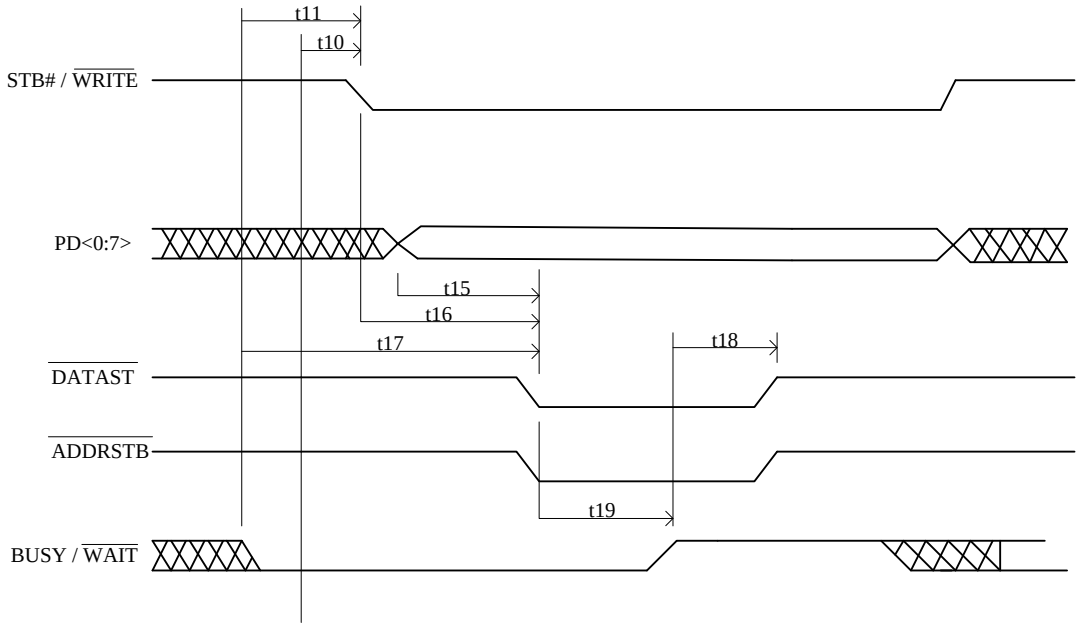
20.7.6 EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



20.7.7 EPP Data or Address Write Cycle (EPP Version 1.7)

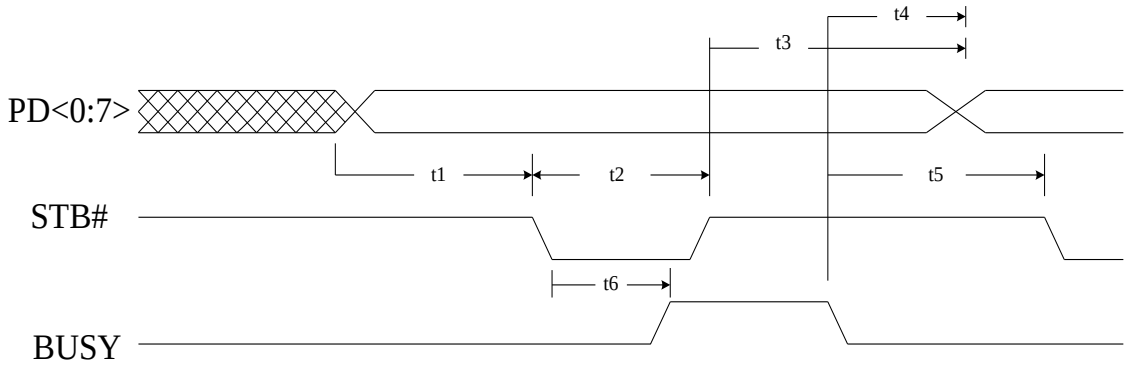
EPP Data or Address Write Cycle (EPP Version 1.7)



20.7.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

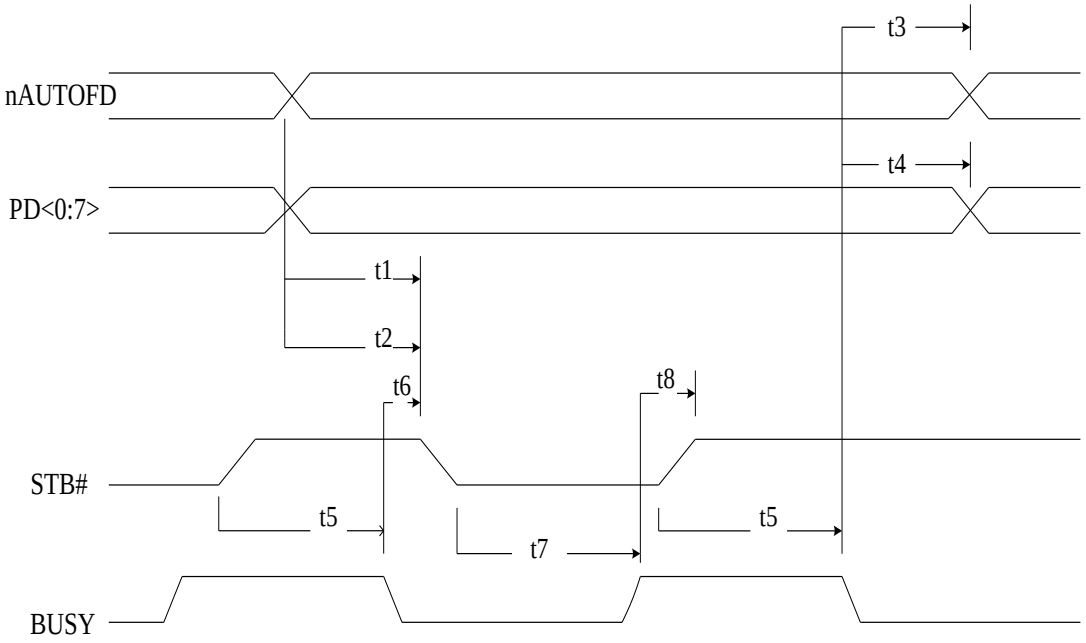
20.7.9 Parallel FIFO Timing



20.7.10 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

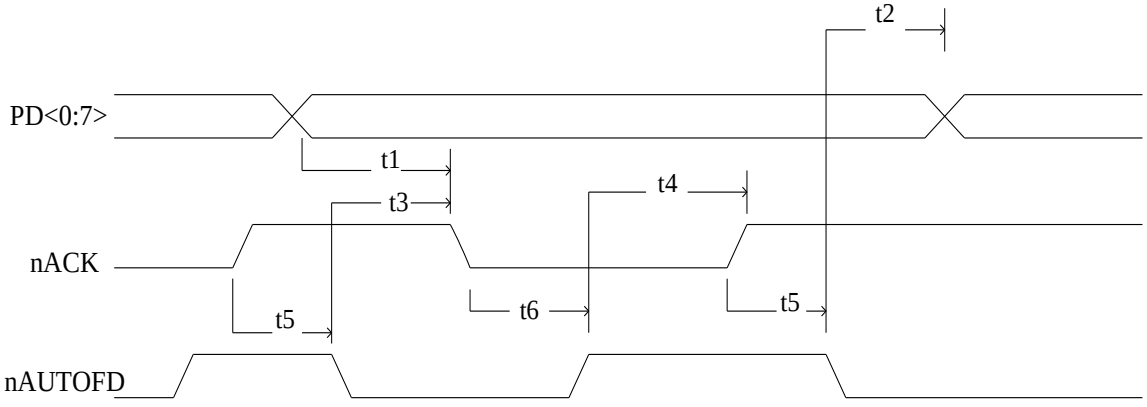
20.7.11 ECP Parallel Port Forward Timing



20.7.12 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

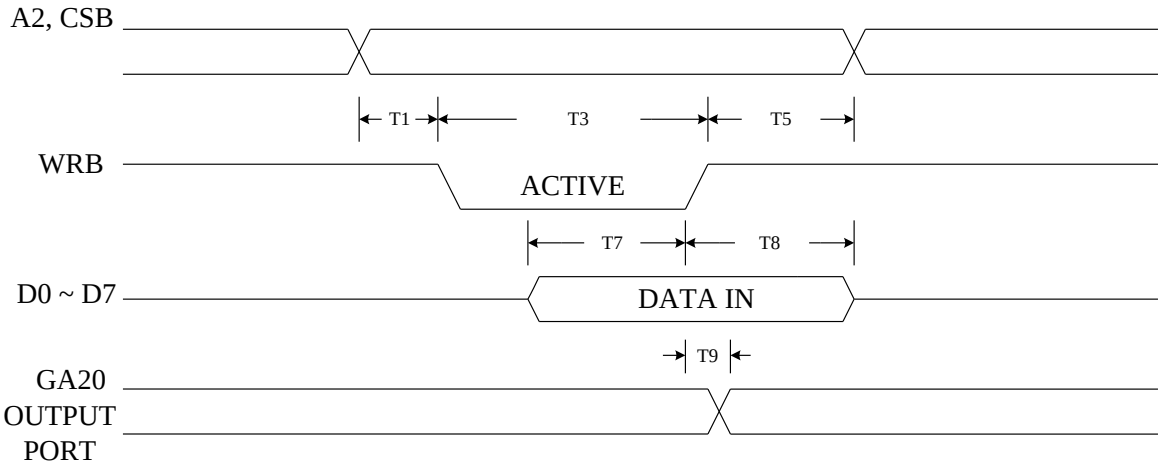
20.7.13 ECP Parallel Port Reverse Timing



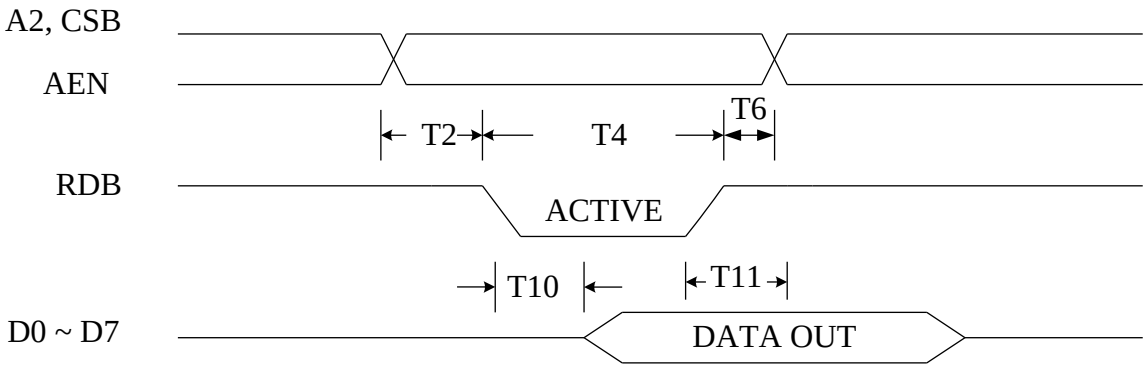
20.8 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

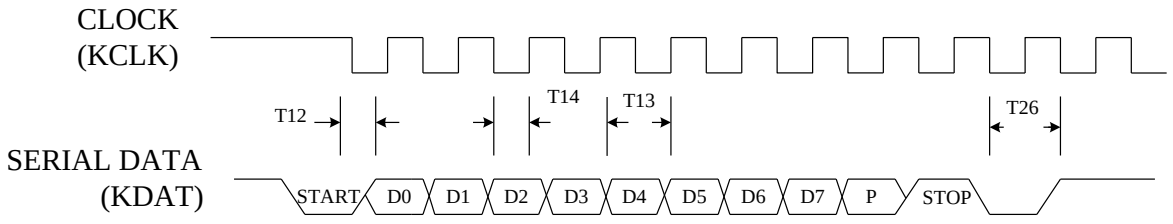
20.8.1 Writing Cycle Timing



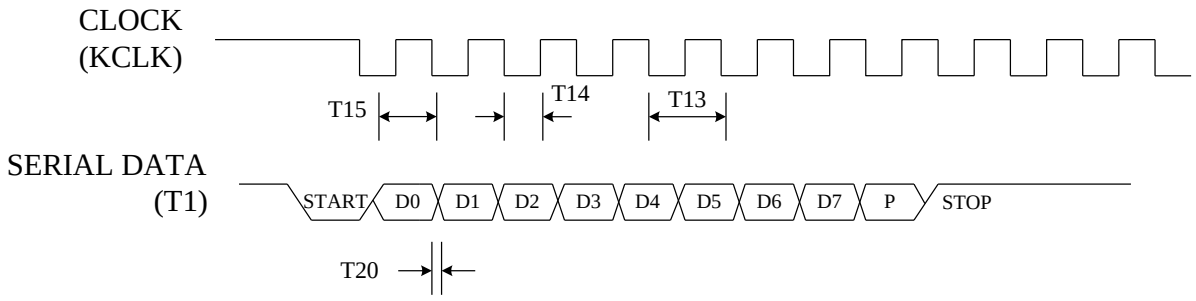
20.8.2 Read Cycle Timing



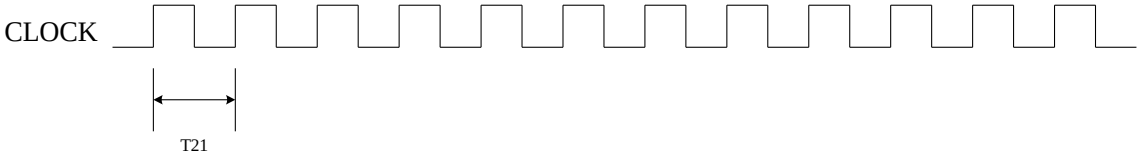
20.8.3 Send Data to K/B



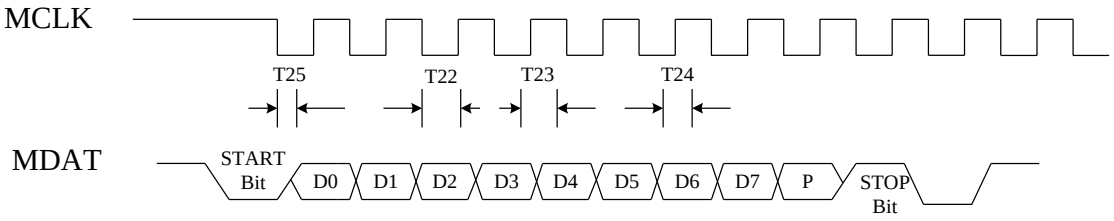
20.8.4 Receive Data from K/B



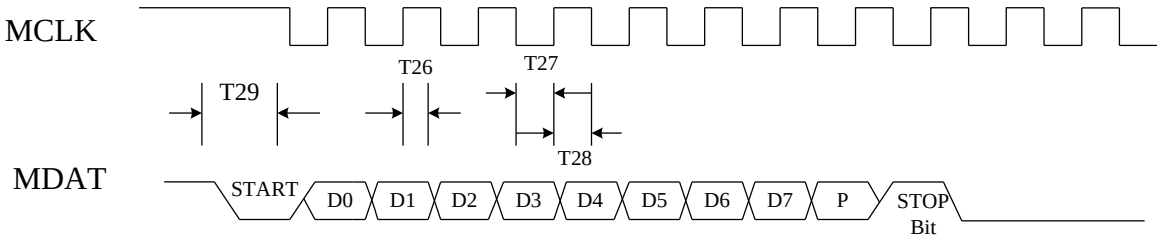
20.8.5 Input Clock



20.8.6 Send Data to Mouse



20.8.7 Receive Data from Mouse

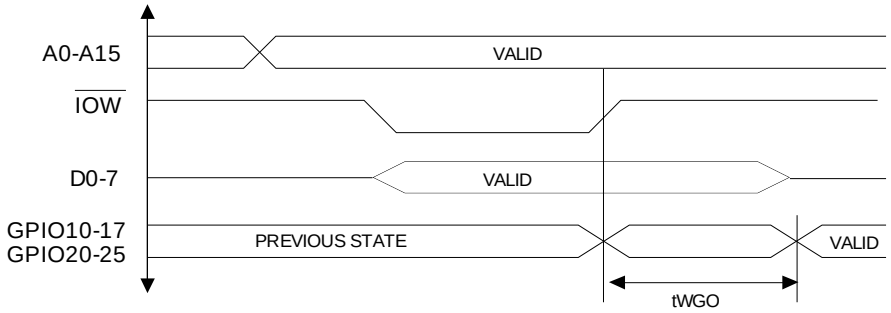


20.9 GPIO Timing Parameters

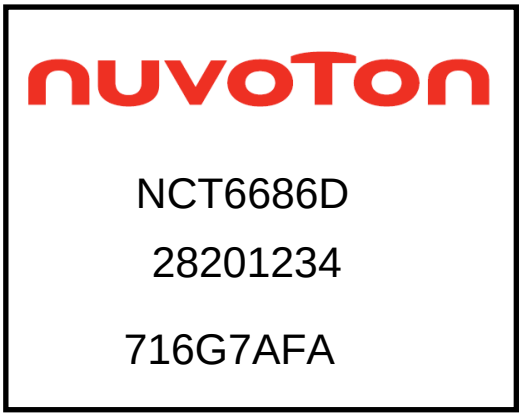
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns

Note: Refer to Microprocessor Interface Timing for Read Timing

20.9.1 GPIO Write Timing



21. TOP MARKING SPECIFICATIONS



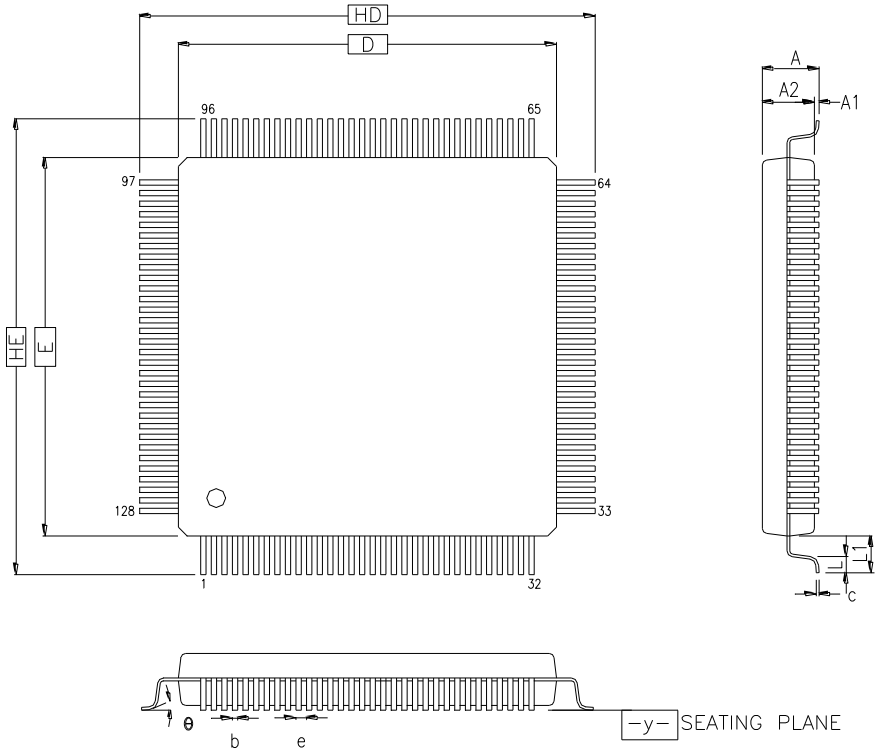
1st line: Nuvoton logo
2nd line: part number: NCT6686D
3rd line: wafer production series lot number: 28201234
4th line: tracking code 716G7AFA

716: packages made in 2017, week 16
G: assembly house ID; G means GR, A means ASE, etc.
7: code version; 7 means code 007
A: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use.

22. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6686D	128Pin LQFP	Commercial, 0°C to +70°C

23. PACKAGE SPECIFICATION



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-pin (LQFP)

24. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.5	04/21/2017	N.A.	First release to public

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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