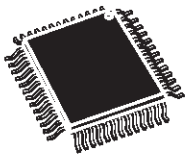
M89 FAMILY

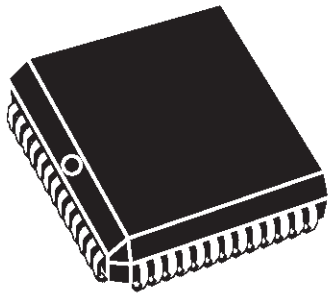
In-System Programmable (ISP) Multiple-Memory and Logic FLASH+PSD Systems for MCUs

DATA BRIEFING

- Single Supply Voltage:
  - 5 V±10% for M89xxFxY
  - 3 V (+20/–10%) for M89xxFxW
- 1 or 2 Mbit of Primary Flash Memory (8 uniform sectors, 16K x 8, or 32K x 8)
- A second non-volatile memory:
  - 256 Kbit (32K x 8) EEPROM (for M8913F1x) or Flash memory (for M89x3F2x)
  - 4 uniform sectors (8K x 8)
- SRAM (16 Kbit, 2K x 8; or 64 Kbit, 8K x 8)
- Over 2,000 Gates of PLD: DPLD and GPLD
- 27 Reconfigurable I/O ports
- Enhanced JTAG Serial Port
- Programmable power management
- Stand-by current:
  - 50 µA for M89xxFxY
  - 25 µA for M89xxFxW
- High Endurance:
  - 100,000 Erase/Write Cycles of Flash Memory
  - 10,000 Erase/Write Cycles of EEPROM
  - 1,000 Erase/Write Cycles of PLD



PQFP52 (T)



PLCC52 (K)

Figure 1. Logic Diagram

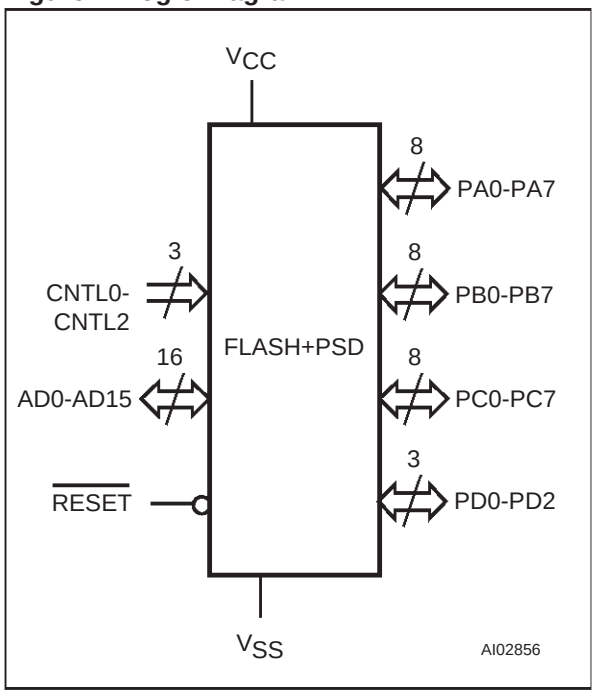


Table 1. Signal Names

PA0-PA7	Port-A
PB0-PB7	Port-B
PC0-PC7	Port-C
	PC2 = Voltage Stand-by
PD0-PD2	Port-D
AD0-AD15	Address/Data
CNTL0-CNTL2	Control
$\overline{\text{RESET}}$	Reset
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. PLCC Connections

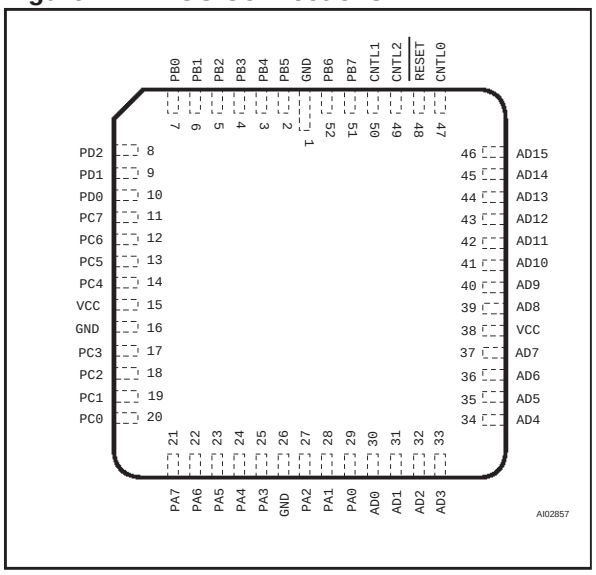
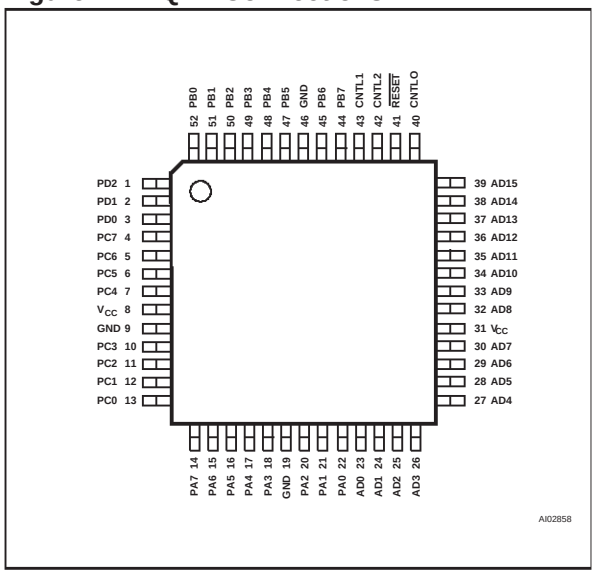


Figure 2B. PQFP Connections



DESCRIPTION

The FLASH+PSD family of memory systems for microcontrollers (MCUs) brings In-System-Programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. FLASH+PSD devices combine many of the peripheral functions found in MCU based applications. FLASH+PSD provides a glueless interface to most commonly-used ROMless MCUs.

Table 2 summarizes all the devices in the M89 Family.

The FLASH+PSD device includes a JTAG Serial Programming interface, to allow In-System Programming (ISP) of the entire device. This feature reduces development time, simplifies the manufacturing flow, and dramatically lowers the cost of field upgrades. Using ST's special Fast-JTAG programming, a design can be rapidly programmed into the FLASH+PSD.

The innovative FLASH+PSD family solves key problems faced by designers when managing discrete Flash memory devices, such as:

– Complex address decoding
– In-System (first-time) Programming (ISP)
– Concurrent EEPROM or Flash memory programming (IAP).

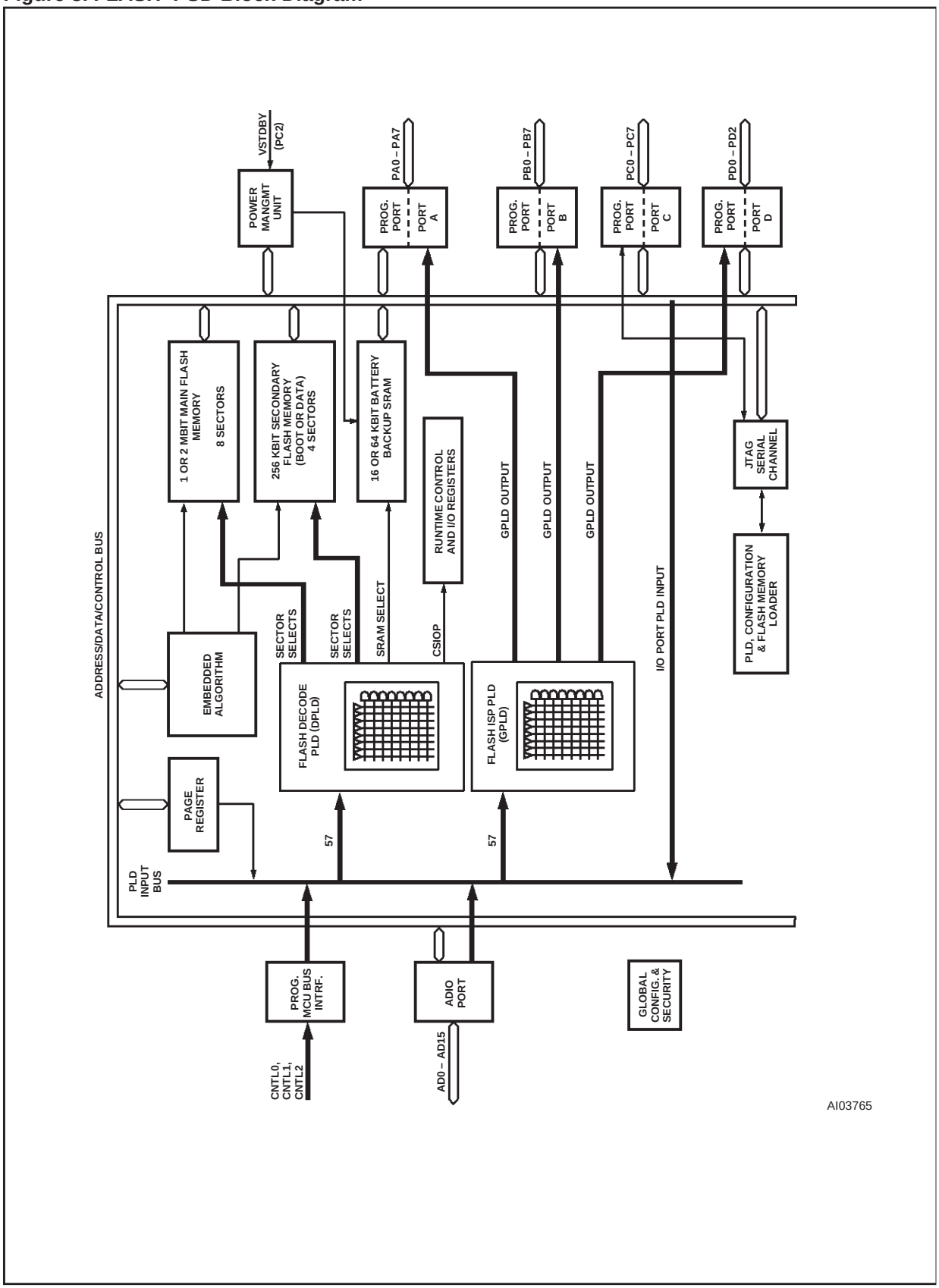
The JTAG Serial Interface block allows In-System Programming (ISP). Embedded dual-bank memories eliminates the need for an external Boot

Table 2. Product Range[1]

Part Number	Primary Flash Memory	Secondary NVM	SRAM[2]	I/O Ports	Voltage Range	Access Time
M8913F1Y	1 Mbit	256 Kbit EEPROM	16 Kbit	27	4.5-5.5 V	90 ns or 150 ns
M8913F2Y	1 Mbit	256 Kbit Flash memory	16 Kbit	27		
M8934F2Y	2 Mbit	256 Kbit Flash memory	64 Kbit	27		
M8913F1W	1 Mbit	256 Kbit EEPROM	16 Kbit	27	2.7-3.6 V	150 ns
M8913F2W	1 Mbit	256 Kbit Flash memory	16 Kbit	27		
M8934F2W	2 Mbit	256 Kbit Flash memory	64 Kbit	27		

Note: 1. All products support: JTAG serial ISP, MCU parallel ISP, ISP Flash memory, ISP GPLD, Security features, Power Management Unit (PMU), Automatic Power-down (APD)
2. SRAM may be backed up using an external battery.

Figure 3. FLASH+PSD Block Diagram



EPROM or Flash memory, or an external programmer. To simplify Flash memory updates, program execution is performed from a secondary Flash memory (for the M89xxF2x) or EEPROM (for the M8913F1x) while the primary Flash memory is being updated. This solution avoids the complicated hardware and software overhead necessary to implement IAP.

ST makes available a software development tool, PSDsoft Express, that generates ANSI-C compliant code for use with your target MCU. This code allows you to manipulate the non-volatile memory (NVM) within the FLASH+PSD. Code examples are also provided for:

– Flash memory IAP via the UART of the host MCU
– Memory paging to execute code across several FLASH+PSD memory pages

FLASH+PSD ARCHITECTURAL OVERVIEW

FLASH+PSD devices contain several major functional blocks. Figure 3 shows the architecture of the M89 FLASH+PSD device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

Memory

The 1 or 2 Mbit (128K x 8, or 256K x 8) Flash memory is the primary memory of the FLASH+PSD. It is divided into eight equally-sized sectors that are individually selectable.

The 256 Kbit (32K x 8) secondary EEPROM or Flash memory is divided into four equally-sized sectors. Each sector is individually selectable.

The SRAM is intended for use as a scratch-pad memory or as an extension to the MCU SRAM. If an external battery is connected to Voltage Stand-by (VSTBY, PC2), data is retained in the event of power failure.

Each sector of memory can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

The M8913F1x has 64 bytes of OTP memory for product identifiers, serial numbers, calibration constants, etc..

Page Register

The 8-bit Page Register expands the address range of the MCU by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals, or internal memory and I/O. The Page Register can also be used to change the address mapping of sectors of the Flash memories into different memory spaces for IAP.

PLDs

The device contains two PLDs, the Decode PLD (DPLD) and the General PLD (GPLD), each optimized for a different function, as shown in Table 3. The functional partitioning of the PLDs reduces power consumption, optimizes cost/ performance, and eases design entry.

The Decode PLD (DPLD) is used to decode addresses and to generate chip selects for the FLASH+PSD internal memory and registers. The DPLD has 14 combinatorial outputs, which are used to select memory sectors and internal registers. The General PLD (GPLD) can be used to implement user-defined external chip select signals and other combinatorial logic functions.

The PLDs consume minimal power. The speed and power consumption of the PLD is controlled by the Turbo bit in the PMMR0 register and other bits in the PMMR2 registers. These registers are set by the MCU at run-time. There is a slight penalty to PLD propagation time when invoking the power management features.

I/O Ports

The FLASH+PSD has 27 individually configurable I/O pins distributed over the four ports (Port A, B, C, and D). Each I/O pin can be individually configured for different functions. Ports can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for MCUs using multiplexed address/data buses. Ports A and B can be configured to be open drain.

The JTAG pins can be enabled on Port C for In-System Programming (ISP).

Port A can also be configured as a data port for a non-multiplexed bus.

MCU Bus Interface

FLASH+PSD interfaces easily with most 8-bit MCUs that have either multiplexed or non-multiplexed address/data buses. The device is configured to respond to the MCU's control signals, which are also used as inputs to the PLDs. For examples, please see the full data sheet.

JTAG Port

In-System Programming (ISP) can be performed through the JTAG signals on Port C. This serial interface allows complete programming of the entire FLASH+PSD device. A blank device can be completely programmed for the first time after it is soldered to the board. The JTAG signals (TMS, TCK, $\overline{\text{TSTAT}}$, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on Port C. Table 4 indicates the JTAG pin assignments. Four-pin JTAG is also fully supported.

In-System Programming (ISP)

Using the JTAG signals on Port C, the entire FLASH+PSD device can be programmed or

Table 3. PLD I/O

Name	Inputs	Outputs	Product Terms
Decode PLD (DPLD)	57	14	39
General PLD (GPLD)	57	19	114

erased without the use of the MCU. The primary Flash memory can also be programmed in-system by the MCU executing the programming algorithms out of the secondary memory, or SRAM. The secondary memory can be programmed the same way by executing out of the primary Flash memory. The PLD or other FLASH+PSD Configuration blocks can be programmed through the JTAG port or a device insertion programmer. Table 5 indicates which programming methods can program different functional blocks of the FLASH+PSD.

Power Management Unit (PMU)

The Power Management Unit (PMU) gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power-down (APD) Unit that turns off device functions during MCU inactivity. The APD Unit has a Power-down mode that helps reduce power consumption.

The FLASH+PSD also has some bits that are configured at run-time by the MCU to reduce power consumption of the GPLD. The Turbo bit in the PMMR0 register can be reset to 0 and the GPLD latches its outputs and goes to sleep until the next transition on its inputs.

Additionally, bits in the PMMR2 register can be set by the MCU to block signals from entering the GPLD to reduce power consumption. Please see the full data sheet for details.

SECURITY AND NVM SECTOR PROTECTION

A security bit in the Protection Register enables the software project, coded in the FLASH+PSD, to be locked up. This bit is only accessible by the system designer from the JTAG serial port, or from a parallel insertion programmer. It cannot be

Table 4. JTAG SIgnals on Port C

Port C Pins	JTAG Signal
PC0	TMS
PC1	TCK
PC3	$\overline{\text{TSTAT}}$
PC4	$\overline{\text{TERR}}$
PC5	TDI
PC6	TDO

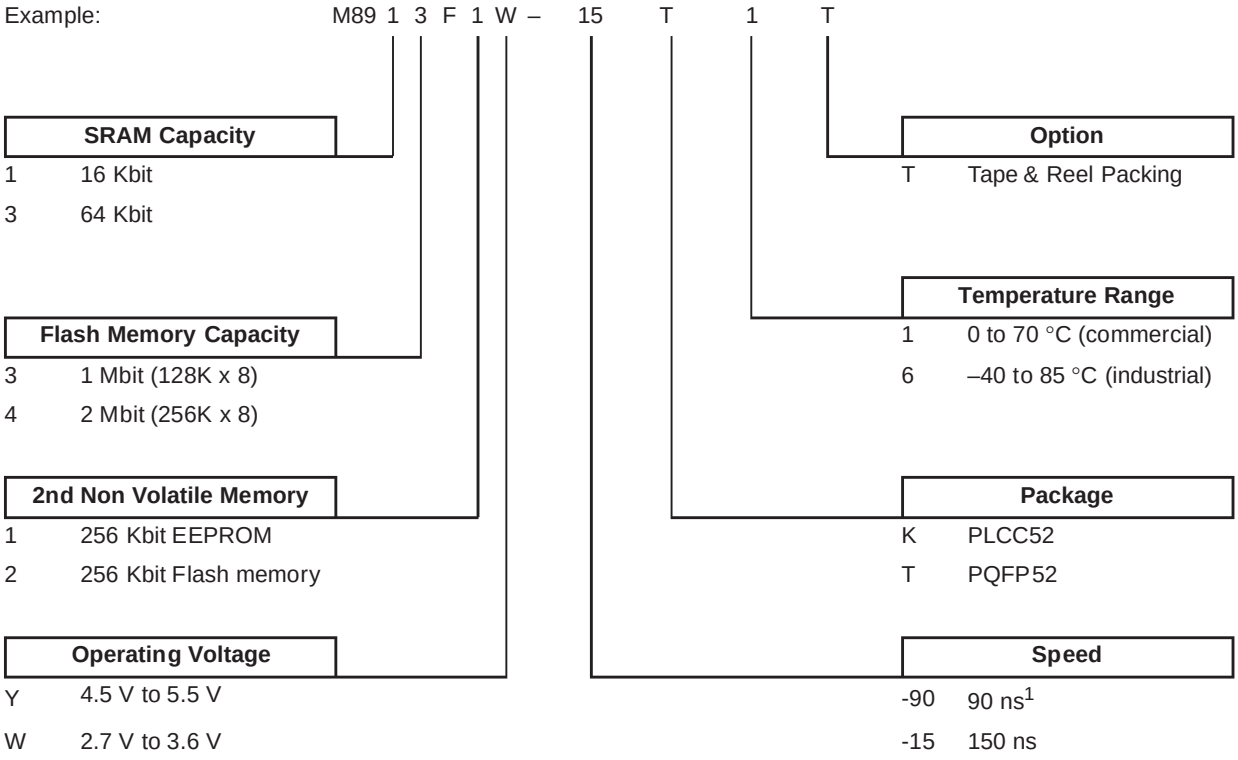
accessed from the MCU. The only way a security bit can be cleared is to erase the entire chip.

The contents of the sectors of the primary and secondary NVM blocks can be protected using bits in the Protection Registers. These bits are accessible from the MCU in the application code, or from a programmer during the set-up procedure.

Table 5. Methods of Programming Different Functional Blocks of the FLASH+PSD

Functional Block	JTAG Programming	Device Programmer	IAP
Primary Flash Memory	Yes	Yes	Yes
Secondary EEPROM or Flash memory	Yes	Yes	Yes
PLD Array (DPLD and GPLD)	Yes	Yes	No
FLASH+PSD Configuration	Yes	Yes	No
OTP Row	No	Yes	Yes

Table 6. Ordering Information Scheme



Note: 1. Available on the 4.5 to 5.5 V range, only.

ORDERING INFORMATION SCHEME

When delivered from ST, the FLASH+PSD device has all bits in the memory and PLDs set to 1. The FLASH+PSD Configuration Register bits are set to 0. The code, configuration, and PLD logic are loaded using the programming procedure. Information for programming the device is available directly from ST. Please contact your local sales representative.

The notation used for the device number is as shown in Table 6. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please see the full data sheet (please consult our pages on the world wide web: *www.st.com/flashpsd*). Alternatively, please contact your nearest ST Sales Office.