Integrated 10-bit Data Acquisition system for Imaging Applications

Description

WM8144-10 integrates the analogue signal conditioning required by CCD sensors with a 10-bit ADC and optional pixel-by-pixel image compensation. WM8144-10 requires minimal external circuitry and provides a cost effective sensor-to-digital domain system solution.

Each analogue conditioning channel provides reset level clamp, CDS, fine offset level shifting and gain amplification. The three channels are multiplexed into the ADC. Output from the ADC can either be direct or passed through a digital post-processing function. The post-processing provides compensation for variations in offset and shading on a pixel-by-pixel basis.

The flexible output architecture allows ten-bit data to be accessed either on a ten-bit bus or via a time-multiplexed eight-bit bus. The WM8144-10 can be configured for pixel-by-pixel or line-by-line multiplexing operation. Reset level clamp and/or CDS features can be optionally bypassed. Device configuration is either by a simple serial or eight-bit parallel interface.

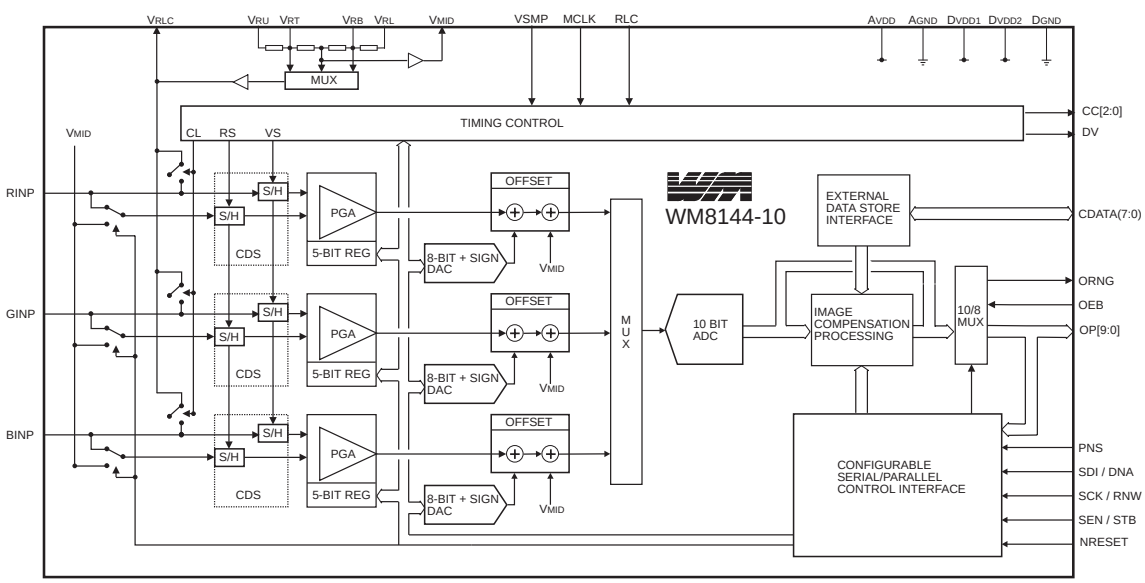
Features

- **Reset level clamp**
- **Correlated Double Sampling (CDS)**
- **Fine offset level shifting**
- **Programmable Gain Amplification**
- **10-Bit ADC with maximum 6 MSPS**
- **Digital post-processing for pixel-by-pixel image compensation**
- **Simple clocking scheme**
- **Control by serial or parallel interface**
- **Time-multiplexed eight-bit data output mode**
- **48 pin TQFP package**
- **Pin compatible with WM8144-12**

Applications

- **Document scanners**
- **CCD sensor interfaces**
- **Contact image sensor (CIS) interfaces**

Block Diagram



Production Data data sheets contain final specifications current on publication date. Supply of products conforms to Wolfson Microelectronics standard terms and conditions

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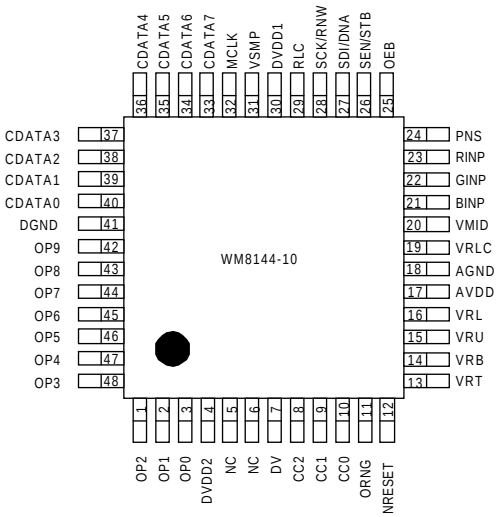
Package Outline



NC - Make no external connection

Ordering Information

DEVICE	TEMP RANGE	PACKAGE
WM8144-10CFT/V	0^0C - 70^0C	48 Pin TQFP

Absolute Maximum Ratings

Analogue Supply Voltage. . . AGND - 0.3 V, AGND +7 V
Digital Supply Voltage. . . . DGND - 0.3 V, DGND +7 V
Digital Inputs . . . . . DGND - 0.3 V, DVDD + 0.3 V
Digital Outputs. . . . . .DGND - 0.3 V, DVDD + 0.3 V
Reference inputs . . . . . AGND - 0.3 V, AVDD + 0.3 V
RINP, GINP, BINP . . . . . .AGND - 0.3 V, AVDD + 0.3 V

Operating temperature range, T_A . . . . . 0^0C to $+70^0$C
Storage Temperature . . . . . -50^0C to $+150^0$C
Lead Temperature (soldering, 10 sec) . . . . . $+260^0$C

Note: Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. The WM8144-10 is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112-A and A113-A this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity level of 2 and as such will be supplied in vacuum sealed moisture barrier bags.

Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage			4.75		5.25	V
Operating Temperature Range	T_A		0		70	^{o}C
Input Common Mode Range	VCMR		0.5		4.5	V

Electrical Characteristics

V_{DD} = 4.75V to 5.25V, GND = 0 V, ...T_A = 0°C to +70°C, MLCK = 12MHz unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current - Active				110.0	150	mA
Supply Current - Standby				10.0	15	mA
Digital Inputs						
High Level Input Voltage	V_{IH}		0.8*DVDD			V
Low Level Input Voltage	V_{IL}				0.2*DVDD	V
High Level Input Current	I_{IH}				1.0	µA
Low Level Input Current	I_{IL}				1.0	µA
Input Capacitance				10.0		pF
Digital Outputs						
High Level Output Voltage	V_{OH}	I_{OH} = 1.0mA	DVDD-0.75			V
Voltage output range	V_{OL}	I_{OL} = 1.0mA			DGND+0.75	V
High Impedance Output Current	I_{OZ}				1.0	µA
Input Multiplexer						
Channel to Channel Gain Matching				0.5		%
Input Video Set-up Time	tVSU		10			ns
Input Video Hold Time	tVH		25			ns
Reset Video Set-up Time	tRSU	CDS Mode only	10			ns
Reset Video Hold Time	tRH	CDS Mode only	25			ns
Reference String						
Reference Voltage - Top	V_{RT}	V_{RU} = 5.00 V, V_{RL} = 0.00V	3.465	3.5	3.535	V
Reference Voltage - Bottom	V_{RB}	V_{RU} = 5.00 V, V_{RL} = 0.00V	1.465	1.5	1.535	V
DAC Reference Voltage	V_{MID}	V_{RU} = 5.00 V, V_{RL} = 0.00V	2.475	2.5	2.525	V
R.L.C. Switch Impedence				200		Ohms
Reset Level Clamp Options	V_{RLC}	V_{RU} = 5.00 V, V_{RL} = 0.00V	1.425	1.5	1.575	V
		Voltage set by user	2.375	2.5	2.625	V
		configuration - Table 7	3.325	3.5	3.675	V
Impedance V_{RT} to V_{RB}			490	700	910	Ohms
Impedance V_{RU} to V_{RL}			1190	1700	2210	Ohms
8-bit DACs						
Resolution			8			Bits
Zero Code Voltage			VDAC -10		VDAC+10	mV
Full Scale Voltage Error			0		10	mV
Differential Non Linearity	DNL			0.1	1	LSB
Integral Non Linearity	INL			0.4	1	LSB

Electrical Characteristics (Contd.)

V_{DD} = 4.75V to 5.25V, GND = 0 V, ...T_A = 0°C to +70°C, MLCK = 12MHz unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10-Bit ADC						
Resolution		V_{DD} = 5V	10			Bits
Maximum Sampling Rate		V_{DD} = 5V	6			MSPS
Full Scale Transition Error Voltage at VINP		DAC Code = 000H, V_{DD}=5V, measured relative to VRT		+/-50	+/-200	mV
Zero Scale Transition Error Voltage at VINP		DAC Code = 000H, V_{DD}=5V, measured relative to VRB		+/-50	+/-200	mV
Differential Non Linearity	DNL	V_{DD} = 5V	-1		+1.25	LSB
Number of missing codes					0	Code
PGA Gain						
Red Channel Max. Gain, Note 1	Gr_{12}	MCLK=12MHz; VDD=5V	4			Times
Green Channel Max. Gain, Note 2	Gg_{12}	Mode=1	7			Times
Blue Channel Max. Gain, Note 2	Gb_{12}		7			Times
Red Channel Max. Gain, Note 2	Gr_8	MCLK=8MHz; VDD=5V	6			Times
Green Channel Max. Gain, Note 2	Gg_8	Mode=1	7			Times
Blue Channel Max. Gain, Note 2	Gb_8		7			Times

Note 1: Guaranteed monotonic up to PGA Gain code 0Fh
Note 2: Guaranteed monotonic up to PGA Gain code 1Fh

Electrical Characteristics (Contd.)

V_{DD} = 4.75V to 5.25V, GND = 0 V, ...T_A = 0°C to +70°C, MLCK = 12MHz unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics						
MCLK Period	tPER		83.3			ns
MCLK High	tCKH		37.5			ns
MCLK Low	tCKL		37.5			ns
Data Set-up time	tDSU		10			ns
VSMP, RLC Data Hold Time	tDH		10			ns
CDATA Data Hold Time	tDH		30			ns
Output Propagation Delay	tPD	I_{OH} = 1.0mA			75	ns
Output Enable TIme	tPZE	I_{OL} = 1.0mA			75	ns
Output Disable Time	tPEZ				25	ns
Serial Interface						
SCK Period	tSPER		83.3			ns
SCK High	tSCKH		37.5			ns
SCK Low	tSCKL		37.5			ns
SDI Set up time	tSSU		10			ns
SDI Hold Time	tSH		10			ns
Set up time - SCK to SEN	tSCE		20			ns
Set up time - SEN to SCK	tSEC		20			ns
SEN Pulse Width	tSEW		50			ns
Parallel Interface						
RNW Low to OP[9:2] Tristate	tOPZ				20	ns
Address Setup Time to STB Low	tASU		0			ns
DNA Low Setup Time to STB Low	tADLS		10			ns
Strobe Low Time	tSTB		50			ns
Address Hold Time from STB High	tAH		10			ns
DNA Low Hold Time from STB High	tADLH		10			ns
Data Set-up Time to STB Low	tDSU		0			ns
DNA High Setup Time to STB Low	tADHS		10			ns
Data Hold Time from STB High	tDH		10			ns
DNA High Hold Time from STB High	tADHH		10			ns
RNW High to OP[9:2] Output	tOPD		0			ns

Pin Descriptions

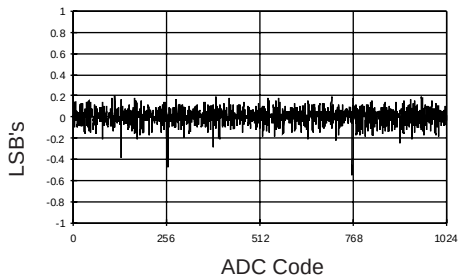
Pin No.	Name	Type	Description
23	RINP	Analogue IP	Red Channel input video
22	GINP	Analogue IP	Green Channel input video
21	BINP	Analogue IP	Blue Channel input video
33	CDATA[7]	Digital IO	Image compensation data read/write at twice ADC conversion rate
34	CDATA[6]	Digital IO	
35	CDATA[5]	Digital IO	
36	CDATA[4]	Digital IO	
37	CDATA[3]	Digital IO	
38	CDATA[2]	Digital IO	
39	CDATA[1]	Digital IO	
40	CDATA[0]	Digital IO	
32	MCLK	Digital IP	Master clock. This clock is applied at either six, four or two times the input pixel rate depending on the operational mode. MCLK is divided internally to define the ADC samples rate and to provide the clock source for digital logic.
31	VSMP	Digital IP	Video sample synchronisation pulse. This signal is applied synchronously with MLCK to specify the point in time that the input is sampled. The timing of internal multiplexing between the R, G and B channels is derived from this signal
29	RLC	Digital IP	Selects whether reset level clamp is applied on a pixel-by-pixel basis. If RLC is required on each pixel then this pin can be tied high
19	VRLC	Analogue OP	Selectable analogue output voltage for RLC
13	VRT	Analogue IP	ADC reference voltages. The ADC reference range is applied between VRT (full scale) and VRB (zero level). VRU and VRL can be used to derive optimum reference voltages from an external 5V reference
14	VRB	Analogue IP	
15	VRU	Analogue IP	
16	VRL	Analogue IP	
20	VMID	Analogue OP	Buffered mid-point of ADC reference string.
42	OP[9]	Digital IO	Tri-state digital 10-bit bi-directional bus. There are four modes: Tri-state: when OEB = 1 Output ten-bit: ten bit data is output from bus Output 8-bit multiplexed: data output on OP[9:2] at 2*ADC conversion rate Input 8-bit: control data is input on bits OP[9:2]
43	OP[8]	Digital IO	
44	OP[7]	Digital IO	
45	OP[6]	Digital IO	
46	OP[5]	Digital IO	
47	OP[4]	Digital IO	
48	OP[3]	Digital IO	
1	OP[2]	Digital IO	
2	OP[1]	Digital IO	
3	OP[0]	Digital IO	

Pin Descriptions (contd.)

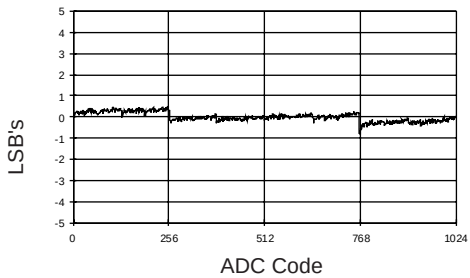
Pin No.	Name	Type	Description
8	CC[2]	Digital OP	Colour code outputs. These outputs indicate from which channel the current output sample was taken (R = 00X, G = 01X, B = 10X). Two codes are provided per channel.
9	CC[1]	Digital OP	
10	CC[0]	Digital OP	
11	ORNG	Digital OP	Out-of-range signal, active high. This signal indicates that the current output pixel has exceeded the maximum or minimum achievable somewhere within the pixel processing.
25	OEB	Digital IP	Output tri-state control, all outputs (OP[9:0], DV, ORNG, CC[2:]) enabled when OEB=0
7	DV	Digital OP	Data valid output, active low.
12	NRESET	Digital IP	Reset input, active low. This signal forces a reset of all internal registers.
24	PNS	Digital IP	Control interface parallel (high) or serial (low, default)
27	SDI/DNA	Digital IP	Serial Interface: serial interface input data signal Parallel interface: high = data, low = address
28	SCK/RNW	Digital IP	Serial Interface: serial interface clock signal Parallel interface: high = OP[9:2] is output, low = OP[9:2] is input bus
26	SEN/STB	Digital IP	Serial Interface: enable, active high Parallel interface: strobe, active low
30	DVDD1	Digital supply	Positive Digital Supply (5V)
4	DVDD2	Digital supply	Positive Digital Supply (5V)
41	DGND	Digital supply	Digital ground (0V)
17	AVDD	Analogue supply	Positive Analogue supply (5V)
18	AGND	Analogue supply	Analogue Ground (0V)
5	NC	Unused	Pin must be left unconnected
6	NC	Unused	Pin must be left unconnected

Typical Performance

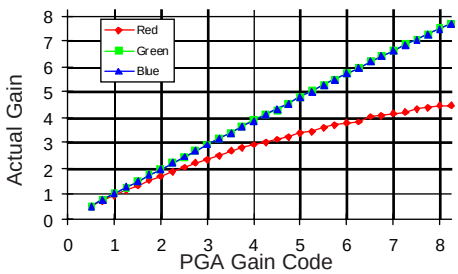
V_{DD} = 5V, GND = 0 V, ...T_A = 25°C.



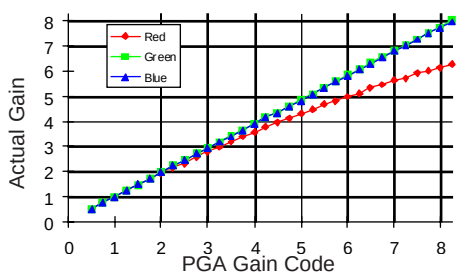
ADC 10 Bit DNL



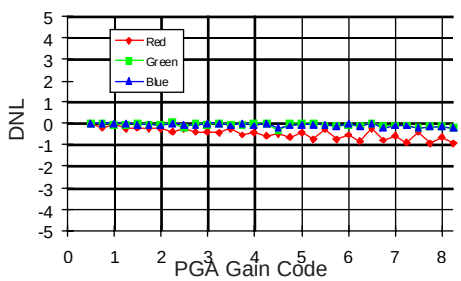
ADC 10 Bit INL



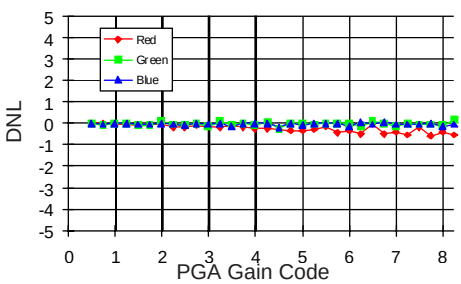
PGA Gain Code vs. Actual Gain @ MCLK = 12.3MHz



PGA Gain Code vs. Actual Gain @ MCLK = 8MHz

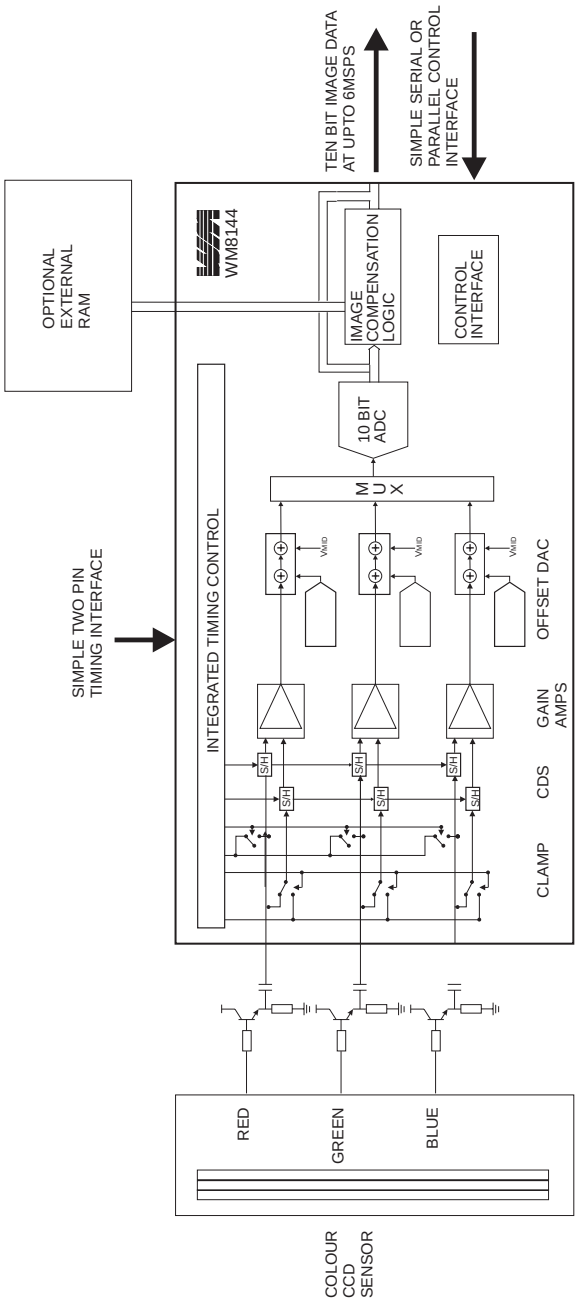


PGA DNL @ MCLK = 12.3MHz



PGA DNL @ MCLK = 8MHz

System Diagram



Theory of Operation

S/H, Offset DAC's and PGA

Each analogue input (RINP, GINP, BINP) of the WM8144-10 consists of a sample and hold, a programmable gain amplifier, and a DC offset correction block. The operation of the red input stage is summarised in Figure 1.

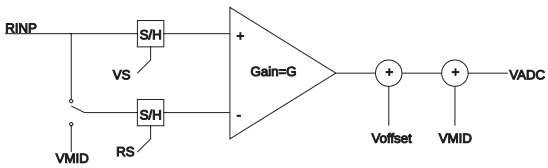


Figure 1

The sample/hold block can operate in two modes of operation, CDS (Correlated Double Sampling) or Single Ended. In CDS operation the video signal processed is the difference between the voltage applied at the RINP input when RS occurs, and the voltage at the RINP input when VS occurs. This is summarised in Figure 2.

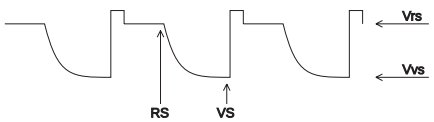


Figure 2

When using CDS the actual DC value of the input signal is not important, as long as the signal extremes are maintained within 0.5 volts of the chip power supplies. This is because the signal processed is the difference between the two sample voltages, with the common DC voltage being rejected.

In single ended operation, the VS and RS control signals occur simultaneously, and the voltage applied to the reset switch is fixed at VMID. This means that the voltage processed is the difference between the voltage applied to RINP when VS/RS occurs, and VMID. When using Single ended operation the DC content of the video signal is not rejected.

The Programmable Gain Amplifier block multiplies the resulting input voltage by a value between 0.5 and 8.25 which can be programmed independently for each of the three input channels via the serial (or parallel) interface. PGA gain is dependent on the 5-bit binary code programmed in the PGA registers. A typical plot of PGA gain versus code is shown on Page 8. The DC value of the gained signal can then be trimmed by the 8 bit plus sign DAC. The voltage output by this DAC is shown as Voffset in Figure 1. The range of the DAC is (VMID/2).

The output from the offset DAC stage is referenced to the VMID voltage. This allows the input to the ADC to maximise the dynamic range, and is shown diagrammatically in Figure 1 by the final VMID addition.

For the input stage the final analogue voltage applied to the ADC can be expressed as:

$$VADC = G(Vvs - Vrs) + \left[(1 - 2 * Sign) * \frac{DAC_CODE}{255} * \frac{VMID}{2} \right] + VMID$$

Where: VADC is the voltage applied to the ADC
G is the programmed gain
Vvs is the voltage of the video sample
Vrs is the voltage of the reset sample
Sign is the Offset DAC sign bit
DAC_CODE is the offset DAC value
VMID is the WM8144-10 generated VMID voltage

The ADC has a lower reference of VRB (typically 1.5 V) and an upper reference of VRT (typically 3.5 V). When an ADC input voltage is applied to the ADC equal to VRB the resulting code is 000(hex). When an ADC input voltage is applied to the ADC equal to VRT the resulting code is 3FF(hex).

Reset Level Clamp

Both CDS and Single ended operation can be used with Reset Level Clamping. A typical input configuration is shown in Figure 3.

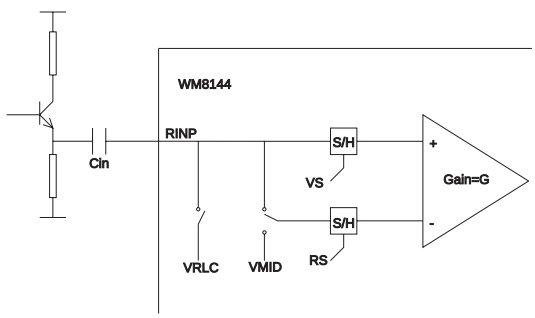


Figure 3

Theory of Operation (contd.)

The position of the clamp relative to the video sample is programmable by CDSREF1-0 (see Table 7). By default, the reset sample occurs on the fourth MCLK rising edge after VSMP. The relative timing between the reset sample (and CL) and video sample can be altered as shown in Figure 4.

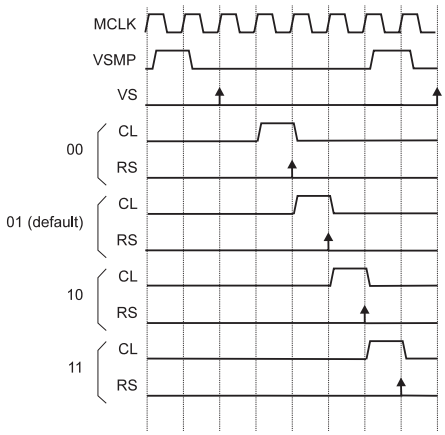


Figure 4: Reset Sample and Clamp Timing

When the clamp pulse is active the voltage on the WM8144-10 side of Cin, i.e. RINP, will be forced to be equal to the VRLC clamp voltage (see Figure 5). The VRLC clamp voltage is programmable to three different levels via the serial interface (1.5V, 2.5V or 3.5V). The voltage to which the clamp voltage should be programmed is dependent on the type of sampling selected and the polarity of the input video signal. For CDS operation it is important to match the clamp voltage to the amplitude and polarity of the video signal. This will allow the best use of the wide input common-mode range offered by the WM8144-10. If the input video is positive going it is advisable to clamp to Vcl (Lower clamp voltage). If the video is negative going it is advisable to clamp to Vcu (Upper clamp voltage). Regardless of where the video is clamped the offset DAC is programmed to move the ADC output corresponding to the reset level to an appropriate value to maximise the ADC dynamic range. For Single Ended operation it is recommended that the clamp voltage is set to Vcm (Middle clamp voltage).

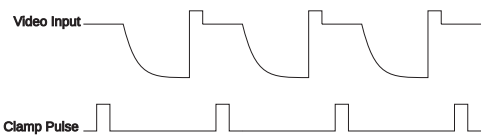


Figure 5

A reset level clamp is activated if the RLC pin is high on an MCLK rising edge (Figure 6). By default this initiates an internal clamp pulse three MCLK pulses later (Figure 4: CL). The relationship between CL and RS is fixed. Therefore altering the RS position also alters the CL position (Figure 4). Table 7 shows the three possible voltages to which the reset level can be clamped.

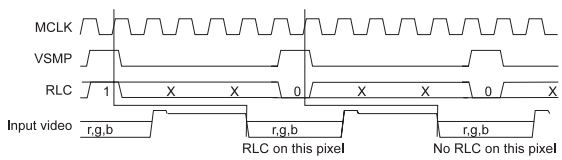


Figure 6: RLC Timing

RINP, GINP and BINP Input Impedence

The input impedence of the WM8144-10 analogue inputs is dependent on the sampling frequency of the input signal and the configuration of the internal gain amplifiers.

The input impedence = 1/(Capacitance * frequency)

where the Capacitance value changes from 0.3pF for minimum gain to 9.6pF for maximum gain. Table 1 illustrates the minimum and maximum input impedence at different frequencies.

Sampling Frequency (MHz)	Impedence with minimum gain (MΩ)	Impedence with maximum gain (KΩ)
0.5	6.6	208
1	3.3	104
2	1.6	52
4	0.8	26
6	0.5	17

Table 1: Effects of Frequency on Input Impedence

Theory of Operation (Contd)

Example of Gain and Offset Operation

Input Video polarity	negative
Input sampling	CDS
Input voltage amplitude (V_{VS} - V_{RS})	1.6V
Programmable gain	x1
Clamping	Yes, V_{CL} = 3.5V

After the input capacitor the input to the WM8144-10 can be represented as:

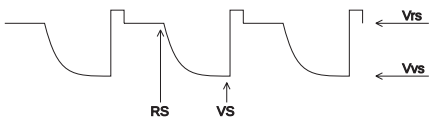


Figure 7

For a black pixel: $V_{RS} = V_{CL}$
$V_{VS} = V_{CL}$

Assuming that the offset DAC is set to 00dec:

$$VADC = 1*(Vcl - Vcl) + \left[(1 - 2*0) * \frac{0}{255} VMID * \frac{VMID}{2}\right] + VMID$$

$$VADC = 0 + 0 + VMID$$

$$VADC = VMID$$

An input voltage of V_{MID} corresponds to a code of 512(dec) from the ADC.

To maximise the dynamic range of the ADC input it is necessary to program the offset DAC code to move the ADC code corresponding to the black level towards code 1024(dec).

Hence set the offset DAC to 164(dec) with the sign bit not set.

$$V_{ADC} = 1*(V_{CL} - V_{CL}) + \left[(1 - 2*0) * \frac{164}{255} * \frac{V_{MID}}{2}\right] + V_{MID}$$

$$V_{ADC} = 0 + \frac{82}{255} * V_{MID} + V_{MID}$$

$$V_{ADC} = \frac{337}{255} * V_{MID}$$

When the VMID is 2.5v, the ADC input voltage becomes 3.3 volts which will result in an ADC code of 921(dec). This is near the ideal full-scale of 1023(dec).

For a white pixel: $V_{RS} = V_{CL}$
$V_{VS} = V_{CL} - 1.6$

For the white pixel, using the same offset DAC value, the ADC input can be expressed as:

$$V_{ADC} = 1*(V_{CL} - 1.6 - V_{CL}) + \left[(1 - 2*0) * \frac{164}{255} * \frac{V_{MID}}{2}\right] + V_{MID}$$

$$V_{ADC} = -1.6 + \frac{82}{255} * V_{MID} + V_{MID}$$

$$V_{ADC} = \frac{337}{255} * V_{MID} - 1.6$$

When the VMID is 2.5V, the ADC input voltage becomes 1.7 volts which will result in a code of 102(dec). This is near the ideal full-scale of 000(dec).

Therefore the output codes from the ADC are between 921(dec) and 102(dec), which implies that the ADC input has been set up to maximise the dynamic range available. If a digital representation of the ADC output with a black level near 000(dec) and a white level near 1023(dec) is required then the INVOP control bit should now be set to ONE.

Theory of Operation (contd.)

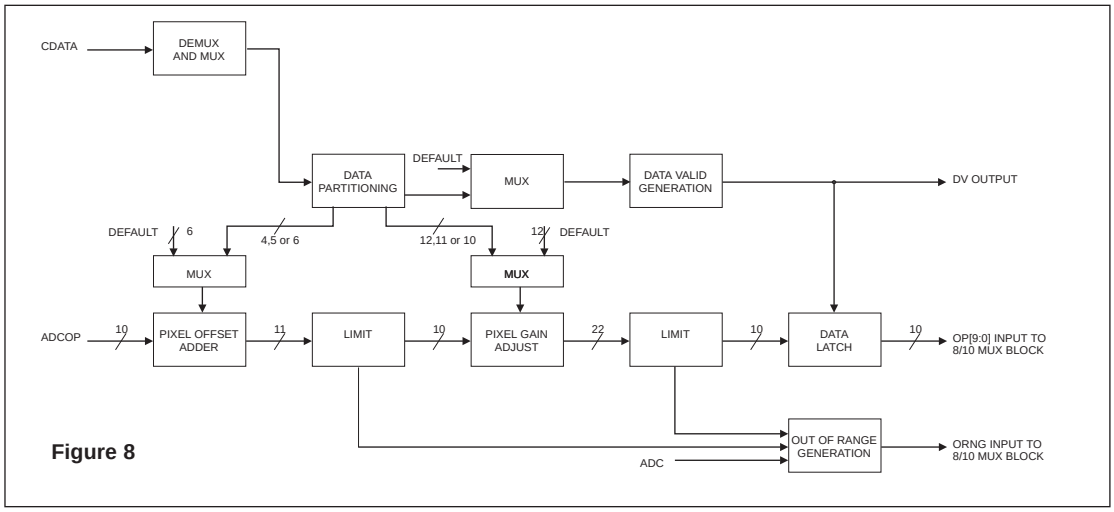


Figure 8

Digital Signal Processing

By default, the output from the ADC passes through the digital compensation block without being altered and is output directly on the OP[9:0] pins. If required, the pixel data from the ADC can be processed further by the digital compensation block (Figure 8). This section describes the sub-blocks of the digital compensation block.

CDATA Demultiplexor

The input to this block is coefficient data presented to the CDATA[7:0] pins at twice the pixel rate. i.e. two eight-bit words are input for each pixel of video data.

Data Partitioning

The sixteen bits of data per pixel from the CDATA Demultiplexor is partitioned into pixel offset, pixel gain and pixel valid bits (Table 3) . Table 4 details the resulting range and resolution options.

Pixel Offset Adder

This uses the offset coefficients that are either supplied externally via the CDATA interface or from the internal default registers. The object of this block is to correct for the small offsets which can occur from the CCD on a pixel-by-pixel basis. The output from the Pixel Offset Adder is limited to be between 0 and 1023(dec).

Pixel Gain Adjust

This block corrects for the pixel-by-pixel shading curve non-uniformity and photo response non-uniformity within the CCD sensor. This block has a gain range of 0 to 2. The output word from the Pixel Gain Adjust is limited to between 0 and 1023(dec).

Effect of digital compensation on ADC output

The combined effect of the digital compensation sections on the ADC output is summarised by the formula:

$$OP[9:0] = (ADCOP + POC) * PSCF$$

where:

All values are decimal

OP[9:0] is the 10 bit result output from the WM8144-10

ADCOP is a 10 bit unsigned number from the ADC

POC is a 2's compliment number divided byNUMBER OF POC BITS ALLOCATED/2

PSCF is an unsigned number divided by NUMBER OF PSC BITS ALLOCATED/2

For this example assume PSC is allocated 12 bits and POC is allocated 4 bits (refer to table 3:DVMODE,PWP0,PWP1 = 0). Table 1 shows some examples of the effect of the digital backend on the ADC output.

	ADCOP	POC	PSC	OP[9:0]	ORNG
Range	0:1023	-8:7	0:4095	0:1023	0:1
Default		0	2048 (x1)		
Ex 1	512	0	2048	512	0
Ex 2	512	-7	2048	505	0
Ex 3	512	6	2048	518	0
Ex 4	1022	6	2048	1023	1
Ex 5	1022	6	512	257	1
Ex 6	512	0	2560	640	0
Ex 7	512	0	512	128	0
Ex 8	512	0	4095	1023	1
Ex 9	511	0	4095	1021	0

Table 2: Examples of digital backend calculation

Theory of Operation (contd.)

			CDATA WORD 1								CDATA WORD 2							
DVMODE	PWP1	PWP0	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	O3	O2	O1	O0
0	0	1	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	O4	O3	O2	O1	O0
0	1	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	O5	O4	O3	O2	O1	O0
1	0	0	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	DV	O3	O2	O1	O0
1	0	1	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	DV	O4	O3	O2	O1	O0

Table 3: Bit Allocation Assignment

DVMODE	PWP1	PWP0	No. of offset bits	offset range	No. of gain bits	gain range	gain resolution (LSB steps)	DV bits
0	0	0	4	-8 : 7	12	0:2	0.25	0
0	0	1	5	-16 - 15	11	0:2	0.5	0
0	1	0	6	-32 - 31	10	0:2	1	0
1	0	0	4	-8 - 7	11	0:2	0.5	1
1	0	1	5	-16 : 15	10	0:2	1	1

Table 4: Bit Range and Resolution Options

Data Valid Generation

The DV pin can be controlled to determine whether a DV pulse will be generated for a particular pixel. For example, if red pixels only are required the following DV pulse can be generated.

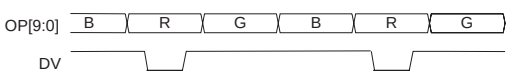


Figure 9

Data Latch

Under control of the LATCHOP bit the output data bus can be prevented from clamping until the next Data Valid pulse. Hence the above output would become:

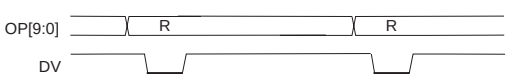
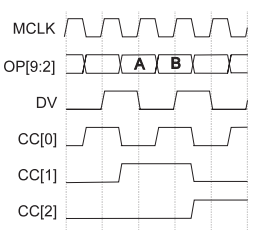


Figure 10

Output data interface

By default, data is output from the device as a ten-bit wide word on OP[9:0]. Optionally, data can be output in an eight-bit word format. Figure 11 shows this function.

Data is presented on pins OP[9:2] at twice pixel rate.



A = d9,d8,d7,d6,d5,d4,d3,d2
B = d1,d0,X,X,X,X,X,ORNG

Figure 11: Eight-bit Multiplexed Bus Output

Operational Modes

Video Sampling Options

WM8144-10 can interface to CCD sensors using four basic modes of operation (summarised in Table 4). Mode configurations are controlled by a combination of control bits and timing applied to MCLK and VMSP pins. The default operational mode is mode 1: colour with CDS enabled.

Colour mode definition (mode 1)

Figure 12 summarises the timing relationships within the Colour mode. MCLK is applied at twice the required ADC conversion rate. Synchronisation of sampling and channel multiplexing to the incoming video signal is performed by the VSMP pulse (active high). The three input channels (R,G,B) are sampled in parallel on the rising edge of MCLK following a VSMP pulse. The sampled data is multiplexed into a single data stream at three times the VSMP rate and passes through the internal pipeline and emerges on the OP[9:0] bus 20.5 MCLK periods later.

If the digital post-processing stage is activated, compensation data will be clocked into the device at twice the ADC conversion rate (e.g. two reads per red pixel). The first of the two bytes will be required on the CDATA bus 15.5 MCLK periods after the corresponding VSMP pulse. CC[2:0] can be used to control the three lower address lines of an external RAM. Both Correlated Double Sampling (CDS) and single sample modes of operation are available.

Monochrome mode definitions

One input channel is continuously sampled on the rising edge of MCLK following a VSMP pulse. The user can specify which input channel (R,G,B) to be sampled by writing to WM8144-10 internal control registers. There are three separate monochrome modes with different maximum sample rates and CDS availability.

Details of Monochrome mode timing (mode 2)

Figure 13 summarises the timing relationships. The timing in this mode is identical to mode 1 except for the CC[2:0] outputs. One input channel is sampled three times (due to the multiplexer being held in one position) and passes through the device as three separate samples. Two of the samples can be ignored at the output. The CC[2:1] output pins reflect the input channel selected (R,G or B).

Details of Fast Monochrome mode timing (mode 3)

Figure 14 summarises the timing relationships. This mode allows the maximum sample rate to be increased to 4 MSPS. This is achieved by altering the MCLK:VSMP ratio to 3:1. In this mode, the timing of RS and CL must be fixed (refer to Table 5).

The sampled video data will pass through the internal pipeline and emerge on the OP[9:0] bus 29.5 MCLK periods later.

If the digital post-processing stage is activated compensation data will be clocked into the device at twice the internal pixel rate (e.g. two reads per red pixel). The first of the two bytes will be required on the CDATA bus 22.5 MCLK periods after the corresponding VSMP pulse.

Details of Max. Speed Monochrome mode (mode 4)

Figure 15 summarises the timing relationships. This mode allows the maximum sample rate to be increased to 6 MSPS. This is achieved by altering the MCLK:VSMP ratio to 2:1. The latency through the device is identical to modes 1 and 2. CDS is not available in this mode.

Operational Modes (Contd.)

Mode	Description	CDS available	Max. Sample Rate	Sensor Interface Description	Timing Requirements	Register Contents with CDS*	Register Contents without CDS*
1	Colour	Yes	2 MSPS	The three input channels (R,G,B) are sampled in parallel at max. 2MSPS. The sampled data is multiplexed into a single data stream before the internal ADC giving an internal serial data rate of max. 6MSPS.	MCLK max. 12MHz. MCLK:VSMP ratio is 6:1.	Setup Reg 1: 1B(H)	Setup Reg 1: 19(H)
2	Monochrome	Yes	2 MSPS	One input channel is continuously sampled. The internal multiplexer is held in one position under control of the user.	Identical to Mode 1	Setup Reg 1: 1F(H) Setup Reg 3: bits b[7-6] define which channel to be sampled	Setup Reg 1: 1D(H) Setup Reg 3: bits b[7-6] define which channel to be sampled
3	Fast Monochrome	Yes	4 MSPS	Identical to Mode 2	MCLK max. 12MHz. MCLK:VSMP ratio is 3:1.	Identical to Mode 2 plus Setup Reg 3: bits b[5-4] must be set to 00(H)	Identical to Mode 2
4	Max Speed Monochrome	No	6 MSPS	Identical to Mode 2	MCLK max. 12MHz. MCLK:VSMP ratio is 2:1.	Not Applicable	Setup Reg 1: 5D(H) Setup Reg 3: bits b[7-6] define which channel to be sampled

* Only indicates relevant register bits

Table 5: WM8144-10 Mode Summary

Operational Modes (Contd.)

Device timing for mode 1

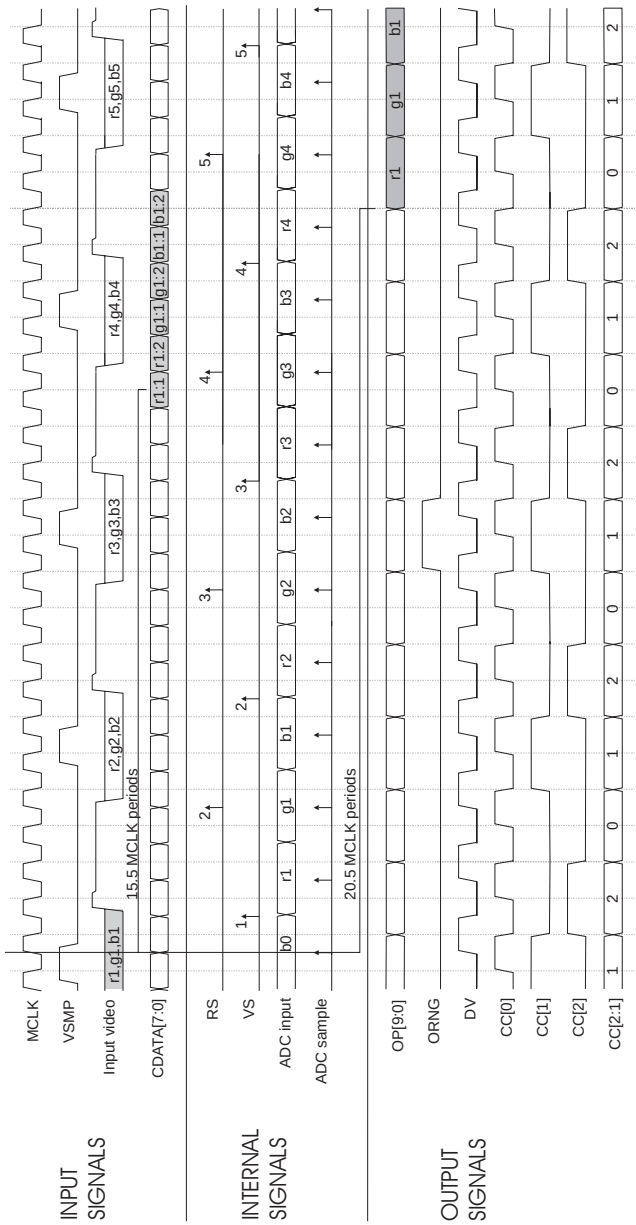


Figure 12: Default Timing in CDS Colour Mode

Operational Modes (Contd.)

Device timing for mode 2

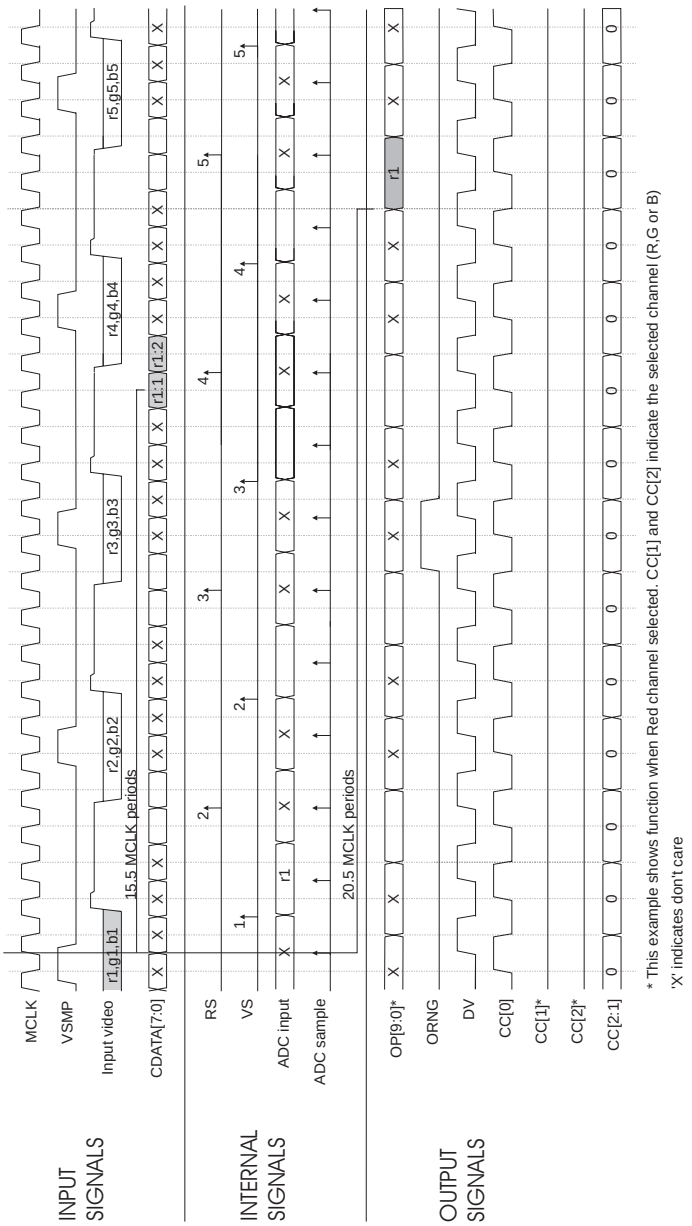


Figure 13: Default Timing in CDS Monochrome Mode

Operational Modes (Contd.)

Device timing for mode 3

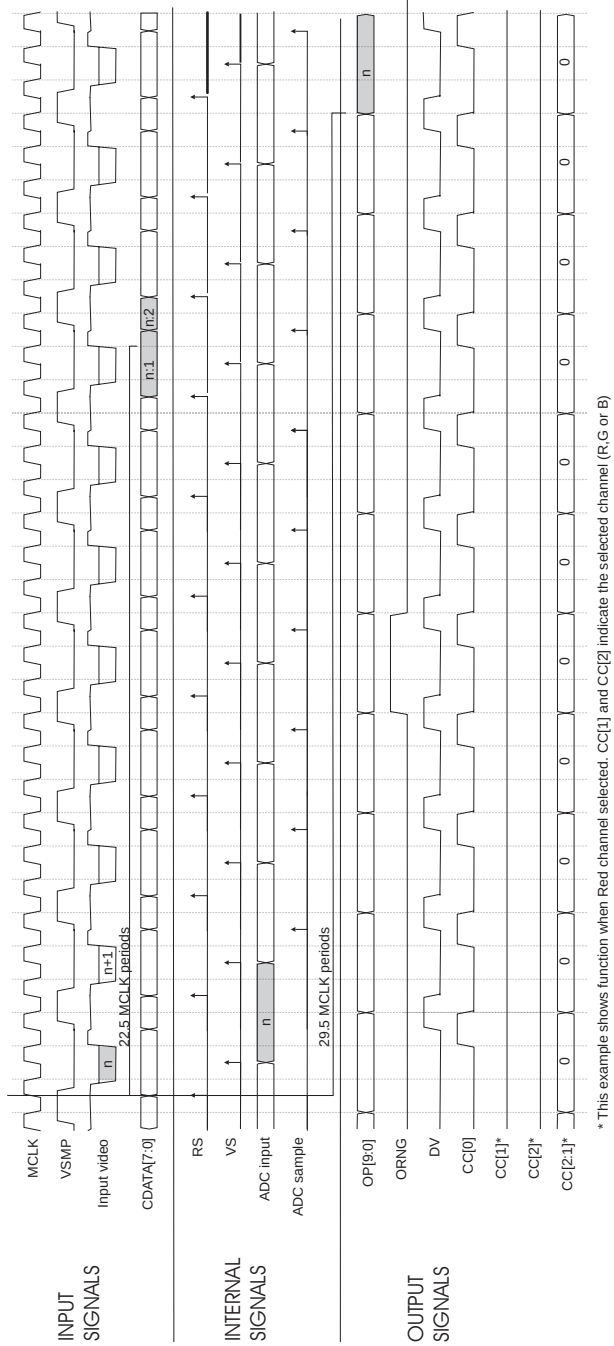


Figure 14: Default Timing in Fast CDS Monochrome Mode

Operational Modes (Contd.)

Device timing for mode 4

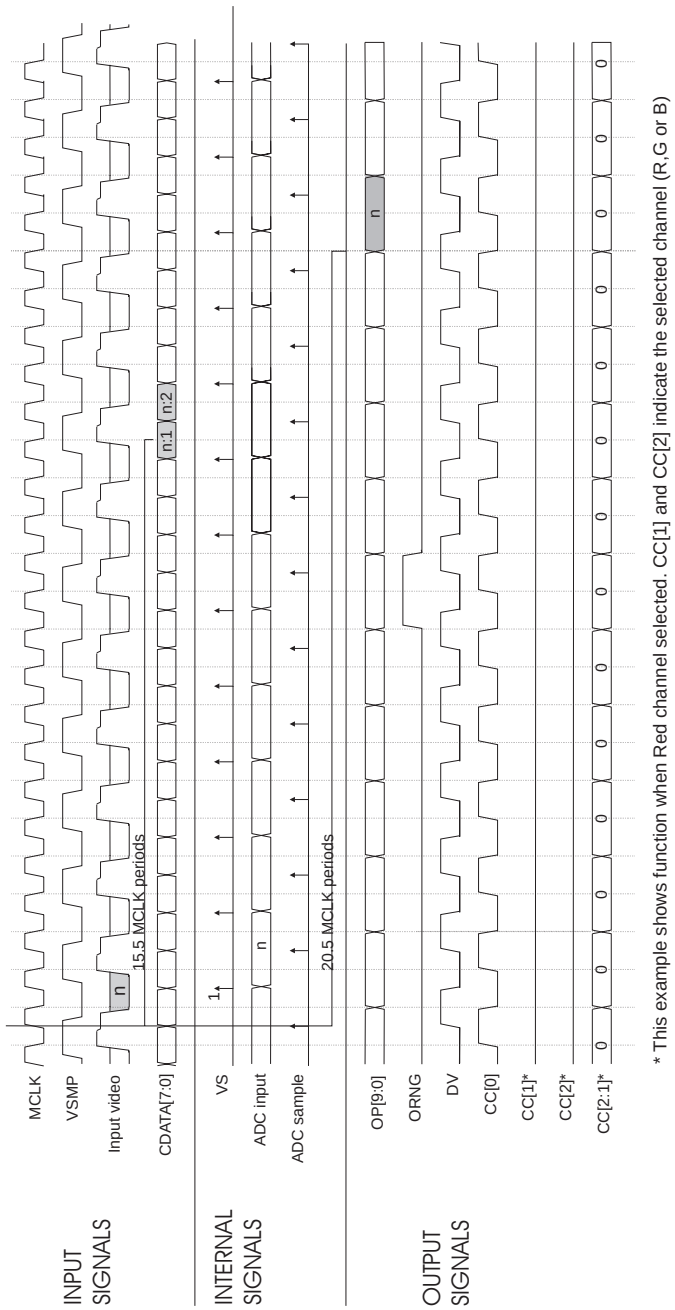


Figure 15: Default Timing in Max. Speed non-CDS Monochrome Mode

Configuration of the WM8144-10

The WM8144-10 can be configured through a serial interface or a parallel interface. Selection of the interface type is by the PNS pin which must be tied high (parallel) or low (serial).

Serial Interface

The serial interface consists of three pins (refer to figure 16). A six-bit address is clocked in MSB first followed by an eight-bit data word, also MSB first. Each bit is latched on the rising edge of SCK, which can operate at upto 12MHz. Once the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register.

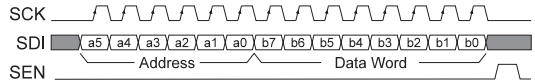


Figure 16: Serial Interface Timing

Parallel Interface

The parallel interface uses bits [9:2] of the OP bus as well as the STB, DNA and RNW pins (refer to figure 17). Pin RNW must be low during a write operation. The DNA pin defines whether the data byte is address (low) or data (high). The data bus OP[9:2] is latched in during the low period of STB. This interface is compatible with the Extended Parallel Port interface.

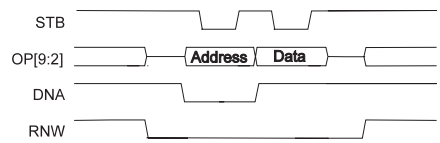


Figure 17: Parallel Interface Timing

Internal Register Definition

Table 5 summarises the internal register content. The first 4 addresses in the table are used to program setup registers and to provide a software reset feature (00H is reserved). The remaining 7 entries in the table define the address location of internal data registers. In each case, a further three sub-addresses are defined for the red, green and blue register. Selection between the red, green and blue registers is performed by address bits a1 and a0, as defined in the table. Setting both a1 and a0 equal to 1 forces all three registers to be updated to the same data value. Blank entries can be taken as 'don't care' values.

Address <a5:a0>	Description	Def'lt (Hex)	Bit b7	b6	b5	b4	b3	b2	b1	b0
000000	Reserved									
000001	Setup Register 1	1B	DVMODE	VSMP6M	DEFDV	DEFPO	DEFPG	MONO	CDS	ENADC
000010	Setup Register 2	00			CDATOUT	BYPASS	LATCHOP	INVOP		MUXOP
000011	Setup Register 3	11	CHAN[1]	CHAN[0]	CDSREF[1]	CDSREF[0]	PWP[1]	PWP[0]	RLC[1]	RLC[0]
000100	Software Reset	00								
000101	Setup Register 4	00							DACRNG	
1000xx	DAC values	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
1001xx	DAC signs	00								DSIGN
1010xx	PGA Gains	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]
1011xx	Pixel Offsets	00			OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]
1100xx	Pixel Gain MSB	80	GAIN[11]	GAIN[10]	GAIN[9]	GAIN[8]	GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]
1101xx	Pixel Gain LSB	00					GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]
1110xx	Data Valid	01								DV

xx	Address LSB decode	a1	a0
	Red Register	0	0
	Green Register	0	1
	Blue Register	1	0
	Red, Green and Blue	1	1

Table 6: Register Map Contents

Configuration of the WM8144-10 (Contd.)

Register	Bit No	Bit(s)	Default	Description
Setup Register 1	0	ENADC	1	ADC standby control: 0 = standby, 1 = active
	1	CDS	1	Select Correlated double sampling mode: 0 = normal sampling, 1 = CDS mode
	2	MONO	0	Mono/Colour select: 0 = colour, 1 = monochrome operation
	3	DEFPG	1	Select Default Pixel Gain: 0 = external pixel gain, 1 = internal
	4	DEFPO	1	Select Default Pixel Offsets: 0 = external pixel offsets, 1 = internal
	5	DEFDV	0	Select default internal Data Valid: 0 = external DV, 1 = internal
	6	VSMP6M	0	Required when VSMP at 6MSPS: 0 = other mode, 1 = VSMP at 6MSPS
	7	DVMODE	0	External Data Valid control (refer to Bit Allocation Assignment table)
Setup Register 2	0	MUXOP	0	Eight bit output mode: 0 = ten-bit, 1 = 8-bit multiplexed
	1			
	2	INVOP	0	Inverts ADC output: 0 = non-inverting, 1 = inverting
	3	LATCHOP	0	OP bus updated on DV pulse; OP bus updated each sample, 1 = update only on DV pulse
	4	BYPASS	0	Bypass digital post-processing; 0 = no bypass, 1 = bypass
	5	CDATOUT	0	Data on OP pins available on CDAT pins; 0 = no, 1 = yes
	6			
	7			
Setup Register 3	1-0	RLC1-0	01	Reset Level Clamp voltage 00 = 1.5V 01 = 2.5V 10 = 3.5V 11 = Reserved
	3-2	PWP1-0	00	Parallel Word Partitioning See Bit Allocation Assignment (Table 3)
	5-4	CDSREF1-0	01	CDS Mode Reset Timing Adjust 00 = Advance 1 MCLK Period 01 = Normal 10 = Retard 1 MCLK Period 11 = Retard 2 MCLK Period
	7-6	CHAN1-0	00	Monochrome mode channel select 00 = Red Channel 01 = Green Channel 10 = Blue Channel 11 = Reserved
Setup Register 4	1	DACRNG	0	Alters range of offset DAC output 0 = DAC output range equal to Vmid/2 (1.25V) 1 = DAC output range equal to 1.5 * Vmid/2 (1.875V)

Table 7: Control Bit Descriptions

Detailed timing diagrams

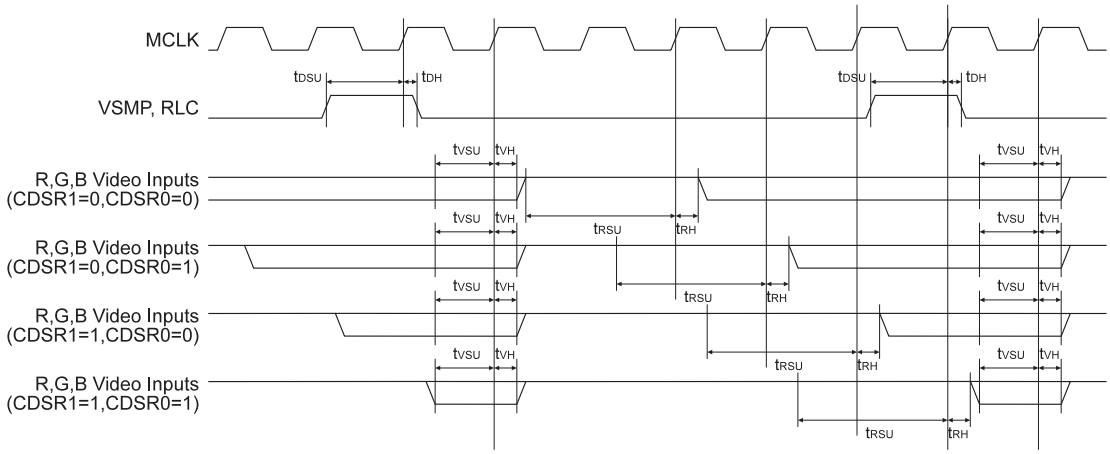


Figure 18: Detailed Video Input Timing - Modes 1 and 2

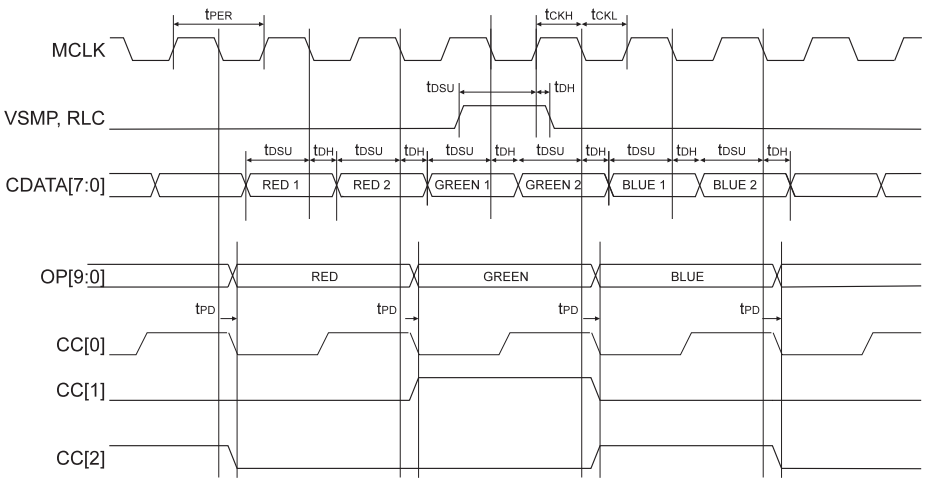


Figure 19: Detailed Digital Timing - Modes 1 and 2

Detailed timing Diagrams (Contd.)

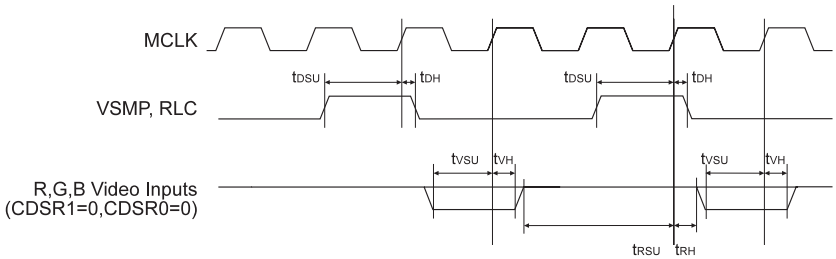


Figure 20: Detailed Video Input Timing - Mode 3

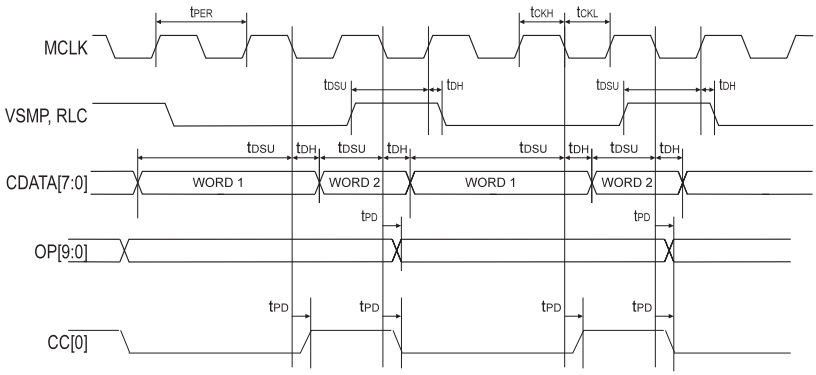


Figure 21: Detailed Digital Timing - Mode 3

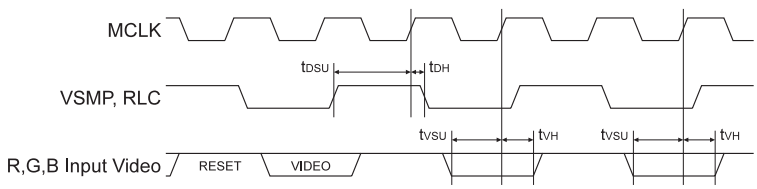


Figure 22: Detailed Video Input Timing - Mode 4

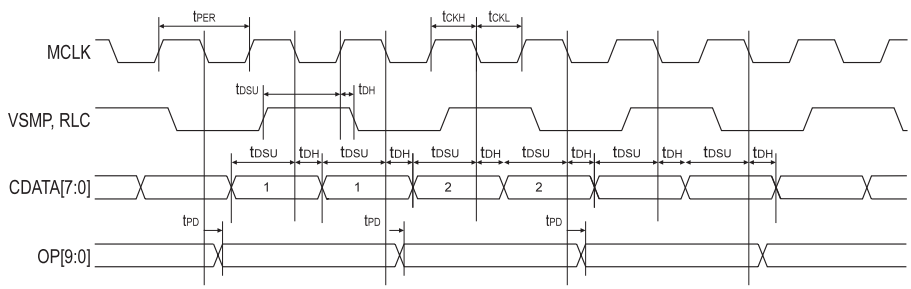


Figure 23: Detailed Digital Timing - Mode 4

Detailed timing Diagrams (Contd.)

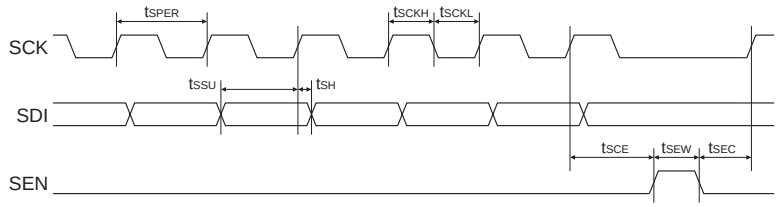


Figure 24: Detailed Timing Diagram for Serial Interface

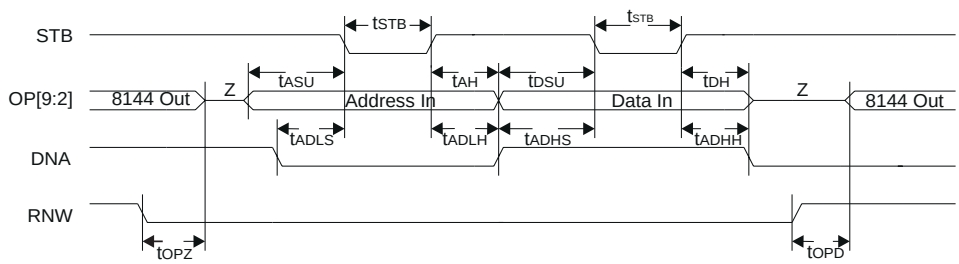
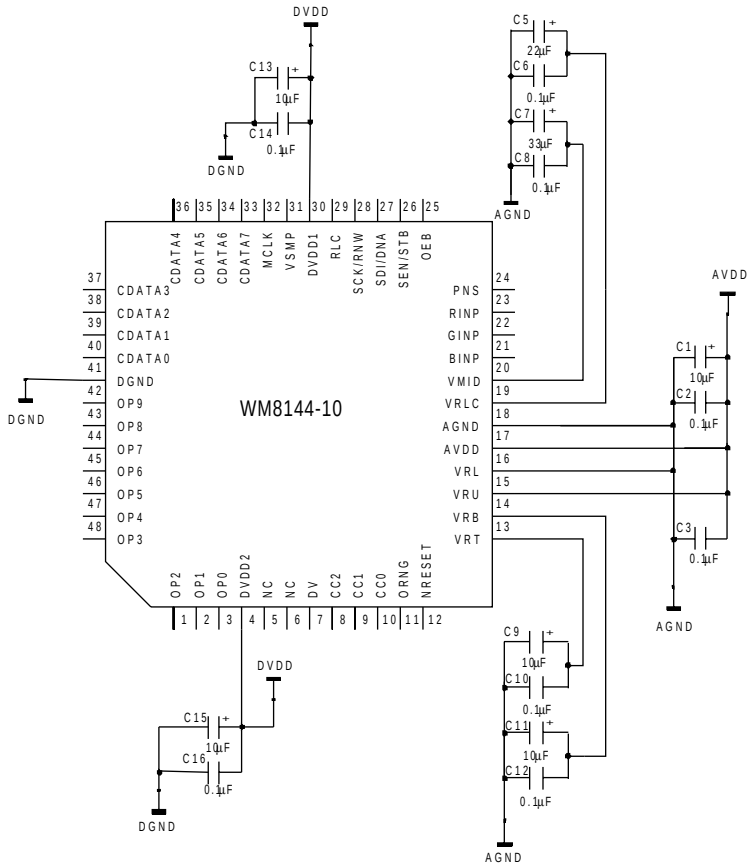
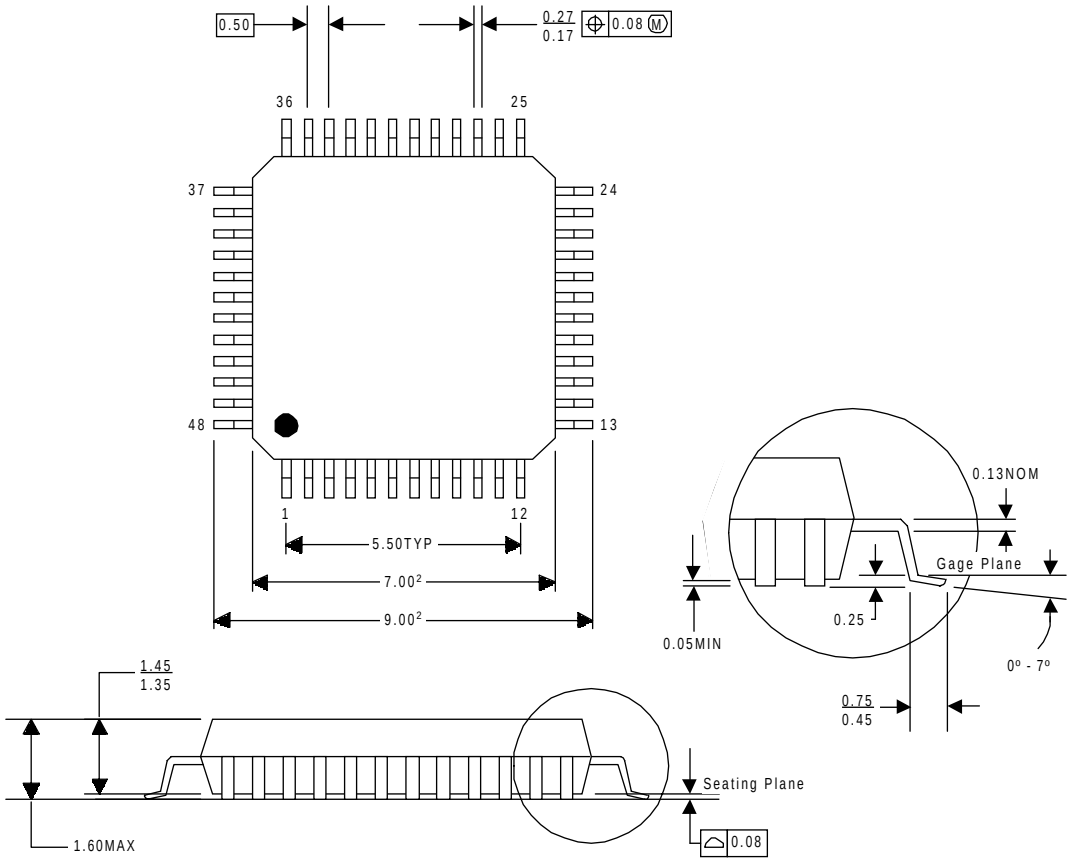


Figure 25: Detailed Timing Diagram for Parallel Interface

External component recommendations



Package Dimensions



48 Pin TQFP

Notes: A. All linear dimensions are in millimeters
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-026