ZL40123

High Speed, Current Feedback Dual Operational Amplifier

Data Sheet

March 2006

Features

- 450 MHz small signal bandwidth
- 1500V/µs slew rate
- 5.2 mA/channel static supply current
- 65 mA output current
- 120 MHz gain flatness to +/- 0.1 dB
- 8 pin SOIC

Ordering Information

ZL40123/DCA	8 Pin SOIC	Tubes
ZL40123/DCB	8 Pin SOIC	Tape & Reel
ZL40123DCE1	8 Pin SOIC*	Tubes, Bake & Drypack
ZL40123DCF1	8 Pin SOIC*	Trays, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

Applications

- Video switchers/routers
- Video line drivers
- Twisted pair driver/receiver
- Active filters

Description

The ZL40123 is a high speed, dual, current feedback operational amplifier offering high performance at a low cost. The device has a very high output current drive capability of 65 mA while requiring only 5.2 mA of static supply current. This feature makes the ZL40123 the ideal choice where a high density of high speed devices is required.

The flat gain response to 120 MHz, 450 MHz small signal bandwidth and 1500V/µs slew rate make the device an excellent solution for video applications such as driving video signals down significant cable lengths.

Other applications which may take advantage of the ZL40123 superior dynamic performance features include low cost high order active filters and twisted pair driver/receivers.

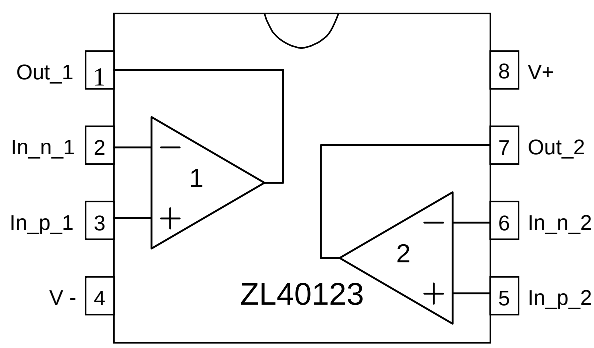


Figure 1 - Functional Block Diagram and Pin Connection

Change Summary

Changes from January 2005 Issue to March 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1		Updated Ordering Information

Application Notes

Current Feedback Op Amps

Current feedback op amps offer several advantages over voltage feedback amplifiers:

- AC bandwidth not dependent on closed loop gain
- High Slew Rate
- Fast settling time

The architecture of the current feedback opamp consists of a high impedance non-inverting input and a low impedance inverting input which is always feedback connected. The error current is amplified by a transimpedance amplifier which can be considered to have gain

$$Z(f) = \frac{Z_o}{1 + j\left(\frac{f}{f_o}\right)}$$

where Z_o is the DC gain.

It can be shown that the closed loop non-inverting gain is given by

$$\frac{Vout}{Vin} = \frac{Av}{1 + j\left(\frac{fR_f}{f_o Z_o}\right)}$$

where Av is the DC closed loop gain, R_f is the feedback resistor. The closed loop bandwidth is therefore given by

$$BW_{CL} = \frac{f_o Z_o}{R_f} = \frac{GB_{OL}}{R_f}$$

and for low values of closed loop gain Av depends only on the feedback resistor R_f and not the closed loop gain.

Increasing the value of R_f

- Increases closed loop stability
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Reduces overshoot

Using a resistor value of R_f=510 Ω for Av=+2 V/V gives good stability and bandwidth. However since requirements for stability and bandwidth vary it may be worth experimentation to find the optimal R_f for a given application.

Layout Considerations

Correct high frequency operation requires a considered PCB layout as stray capacitances have a strong influence over high frequency operation for this device. The Zarlink evaluation board serves as a good example layout that should be copied. The following guidelines should be followed:

- Include 6.8 uF tantalum and 0.1 uF ceramic capacitors on both positive and negative supplies
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitances
- Minimize all trace lengths to reduce series inductance

Application Diagrams

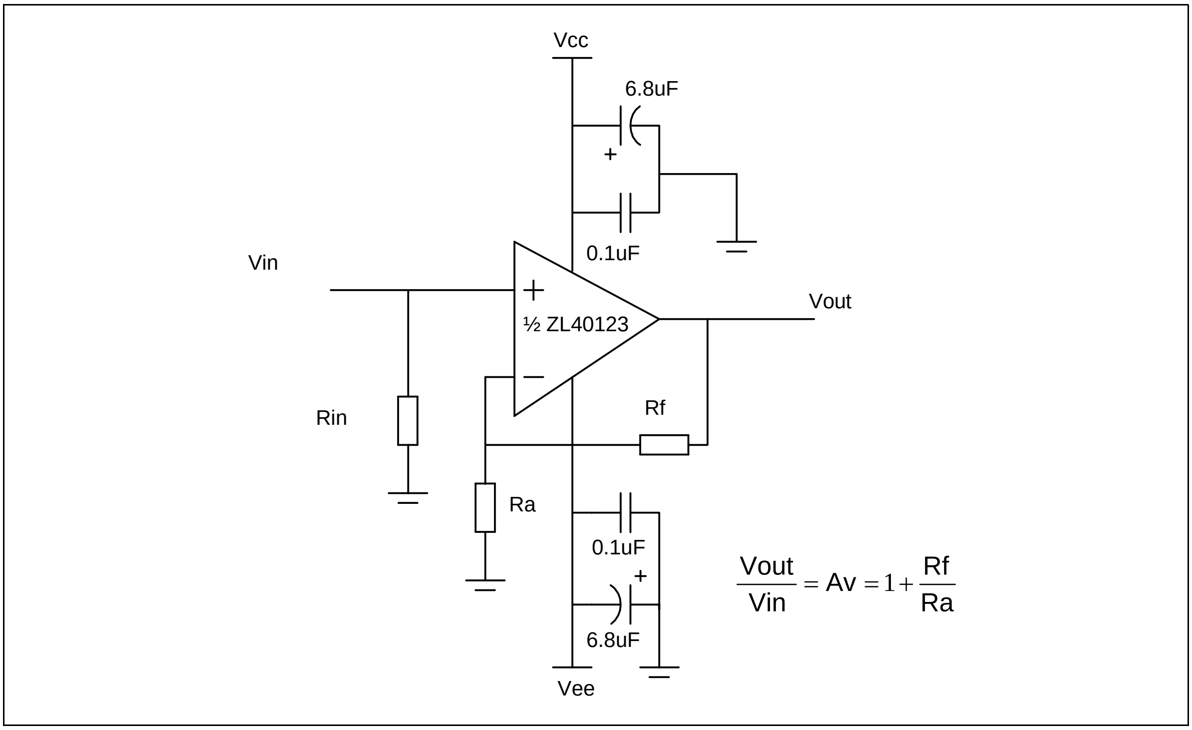


Figure 2 - Non-inverting Gain

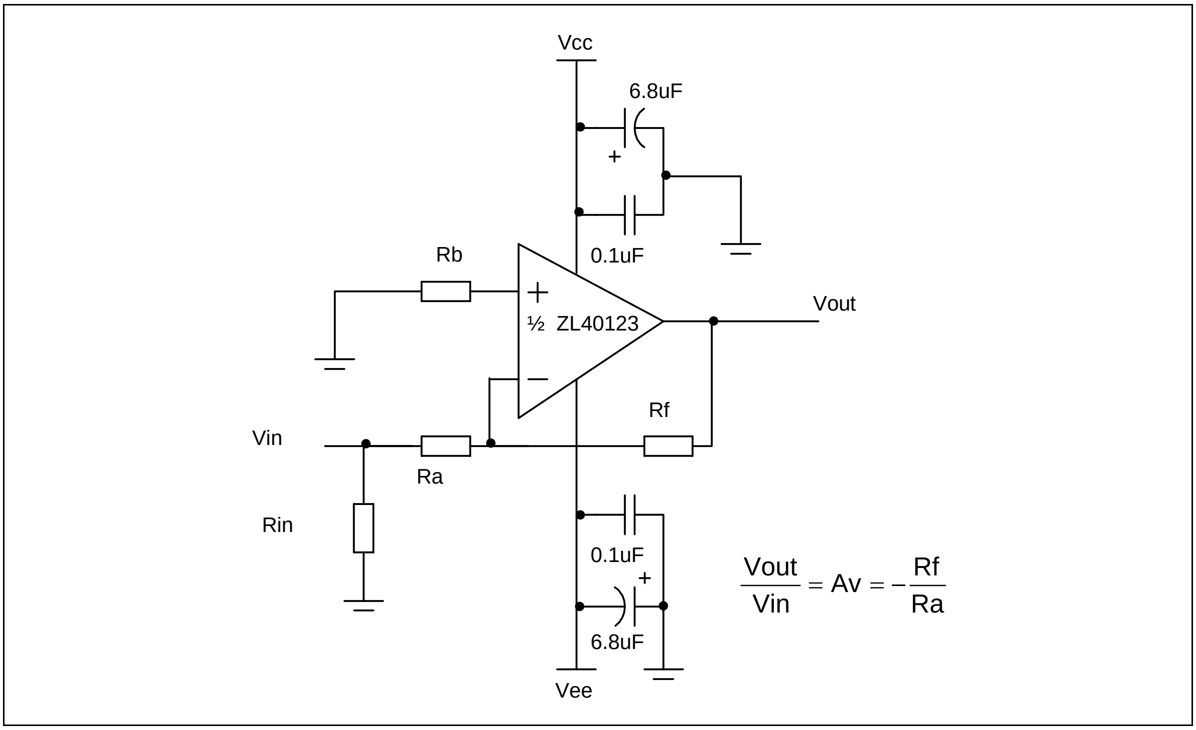


Figure 3 - Inverting Gain

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	Vin Differential	V_{IN}		±1.2	V
2	Output Short Circuit Protection	$V_{OS/C}$		See Apps Note in this data sheet	
3	Supply voltage	V+, V-		±6.5	V
4	Voltage at Input Pins	$V_{(+IN)}$, $V_{(-IN)}$	V-	V+	V
5	Voltage at Output Pins	V_O	V-	V+	V
6	EDS Protection (HBM Human Body Model) (see Note 2)		2	(see Note 3)	kV
7	Storage Temperature		-55	+150	°C
8	Latch-up test		±100 mA for 100 ms	(see Note 4)	
9	Supply transient test		20% pulse for 100ms	(see Note 5)	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model, 20 Ω in series with 100 pF.

Note 3: 0.8 kV between the pairs of +INA, -INA and +INB pins only. 2kV between supply pins, OUTA or OUTB pins and any input pin.

Note 4: ±100 mA applied to input and output pins to force the device to go into "latch-up". The device passes this test to JEDEC spec 17.

Note 5: Positive and Negative supply transient testing increases the supplies by 20% for 100 ms.

Operating Range

Characteristic	Min.	Typ.	Max.	Units	Comments
Supply Voltage (Vcc)	±4.0		±6.0	V	
Operating Temperature (Ambient)	-40		+85	°C	
Junction to Ambient resistance	Rth(j-a)	150		°C 4 layer FR4 board	
Junction to Case resistance	Rth(j-c)	60		°C 4 layer FR4 board	

Electrical Characteristics - Vcc=±5 V, T_{amb}=25°C(typ.),T_{amb}=-40°C to +85°C(min-max), Av=+2V/V, Rf=510 Ω, Rload=100 Ω unless specified.

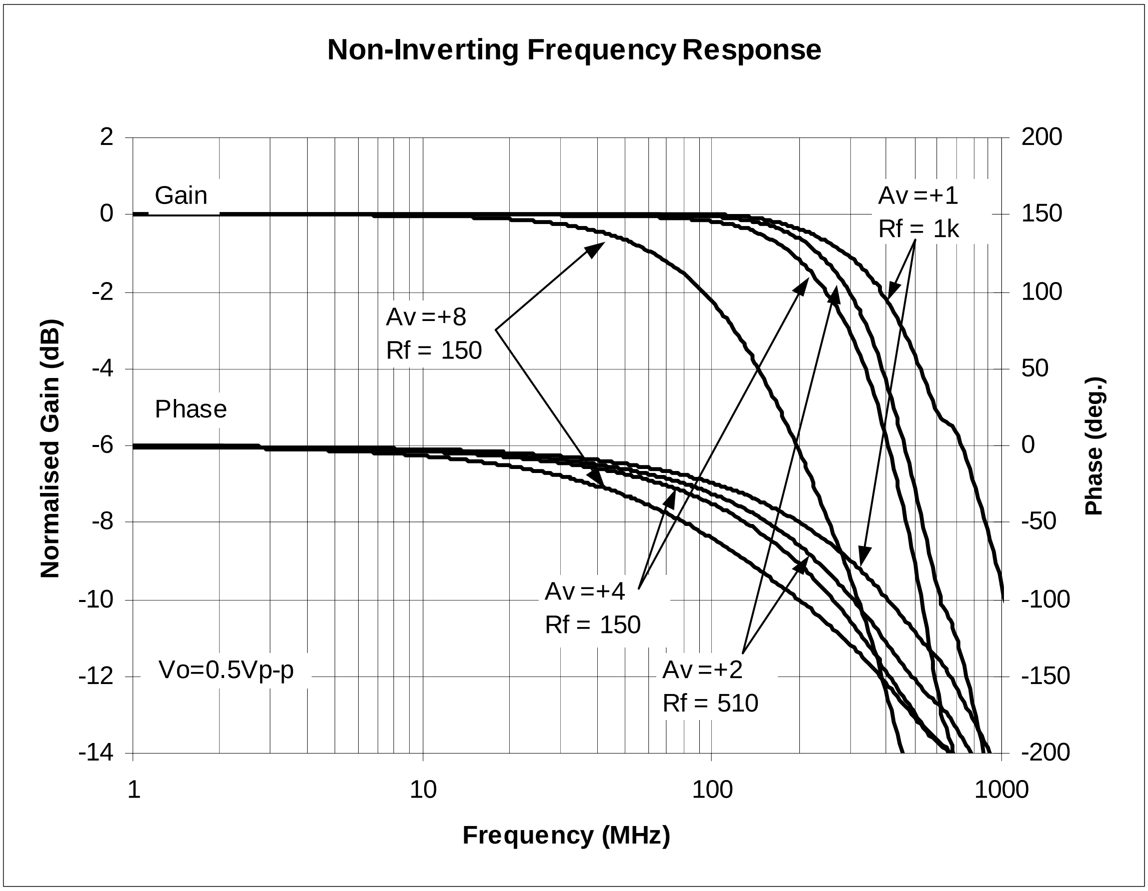
Characteristic	Conditions	Typ. 25°C	Min./ Ma.x 25°C	Min./ Max. –40 to +85°C	Units	Test Type[1]
Frequency Domain Response						
-3 dB Bandwidth	Av=+1; Vo < 0.5Vp-p; Rf=1.5 kΩ	450	-	-	MHz	C
	Av=+2; Vo < 0.5Vp-p; Rf=510 Ω	380	-	-	MHz	C
	Av=+2; Vo < 5V p-p; Rf=510 Ω	170	-	-	MHz	C
+/- 0.1dB Flatness	Av=+2; Vo < 0.5Vp-p; Rf=510 Ω	120	-	-	MHz	C
Differential Gain (NTSC)	Rload=150 Ω	0.01	-	-	%	C
Differential Phase (NTSC)	Rload=150 Ω	0.015	-	-	deg.	C
Time Domain Response						
Rise and Fall Time	Vout=0.5 V Step	1	-	-	ns	C
	Vout=5 V Step	2.8	-	-	ns	C
Settling Time to 0.1%	Vout=2 V Step	6	-	-	ns	C
Overshoot	Vout=0.5 V Step	4	-	-	%	C
Slew Rate	Vout=5 V Step	1500	-	-	V/µs	C
Noise and Distortion						
2nd Harmonic Distortion	Vout=2Vp-p, 1 MHz	-84	-	-	dBc	C
3nd Harmonic Distortion	Vout=2Vp-p, 1 MHz	-85	-	-	dBc	C
Equivalent Input Noise						
Voltage	>1 MHz	5.5	-	-	$nV\sqrt{Hz}$	C
Non-Inverting Current	>1 MHz	1.3	-	-	$pV\sqrt{Hz}$	C
Inverting Current	>1 MHz	11	-	-	$pA\sqrt{Hz}$	C
Static, DC Performance						
Input Offset Voltage		2.7	±6.3	±7.7	mV	A
Average Drift		-	-	15	µV/deg. C	C
Input Bias Current – Non-inverting		2.6	±5.6	±6	µA	A

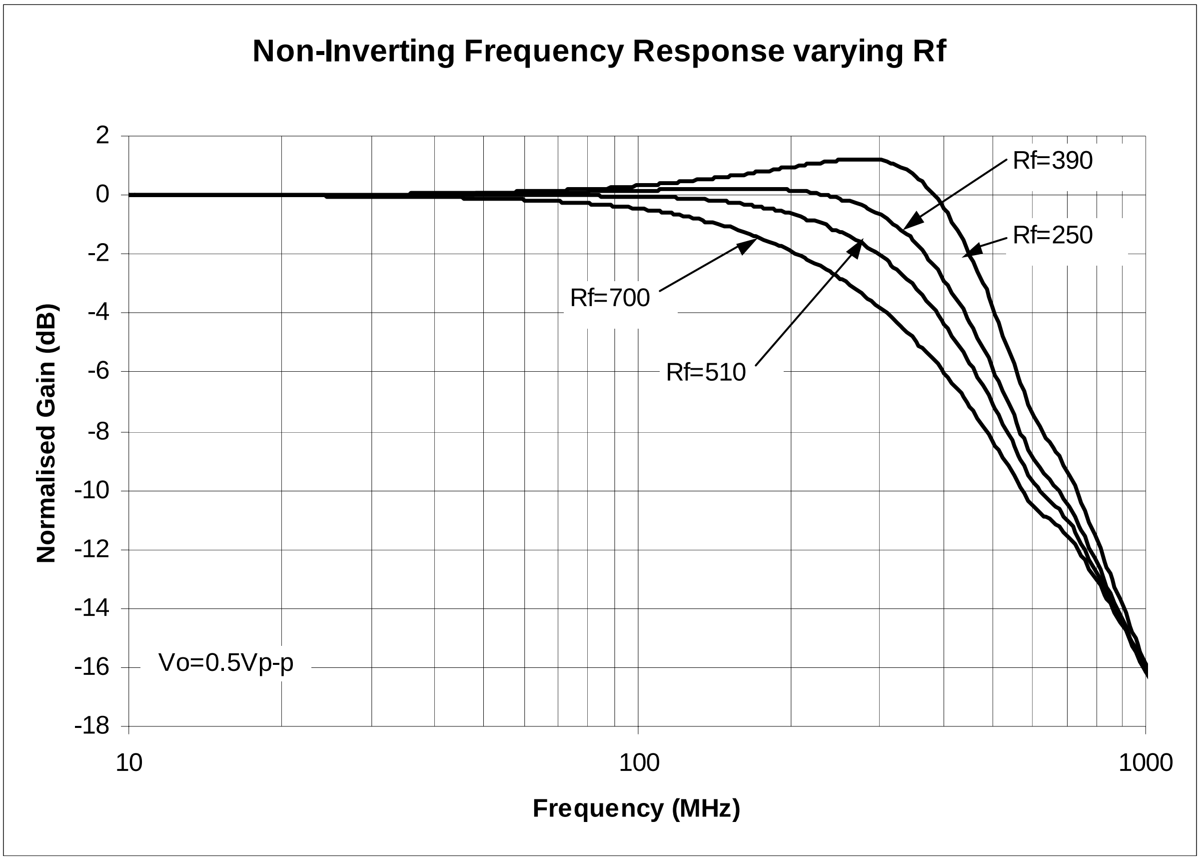
Characteristic	Conditions	Typ. 25°C	Min./ Ma.x 25°C	Min./ Max. −40 to +85°C	Units	Test Type[1]
Average Drift		-	-	6	nA/deg. C	C
Input Bias Current – Inverting		7.4	±25	±28	uA	A
Average Drift		-	-	15	nA/deg. C	C
Power Supply Rejection Ratio (+ve)	DC	61	58	57	dB	A
Power Supply Rejection Ratio (-ve)	DC	58	56	55	dB	A
Common Mode Rejection Ratio	DC	54	50	49	dB	A
Supply Current (per Channel)	Quiescent	5.2	6.5	6.7	mA	A
Miscellaneous Performance						
Input Resistance (Non-inverting)		8	-	-	MΩ	C
Input Capacitance (Non-inverting)		1	-	-	pF	C
Common Mode Input Range		±2.4	±2.2	±2.0	V	A
Output Voltage Range	Rload=100 Ω	±2.8	±2.7	±2.6	V	A
Output Current (max)		65	-	-	mA	C
Output Resistance, Closed Loop	DC	90	-	-	mΩ	C

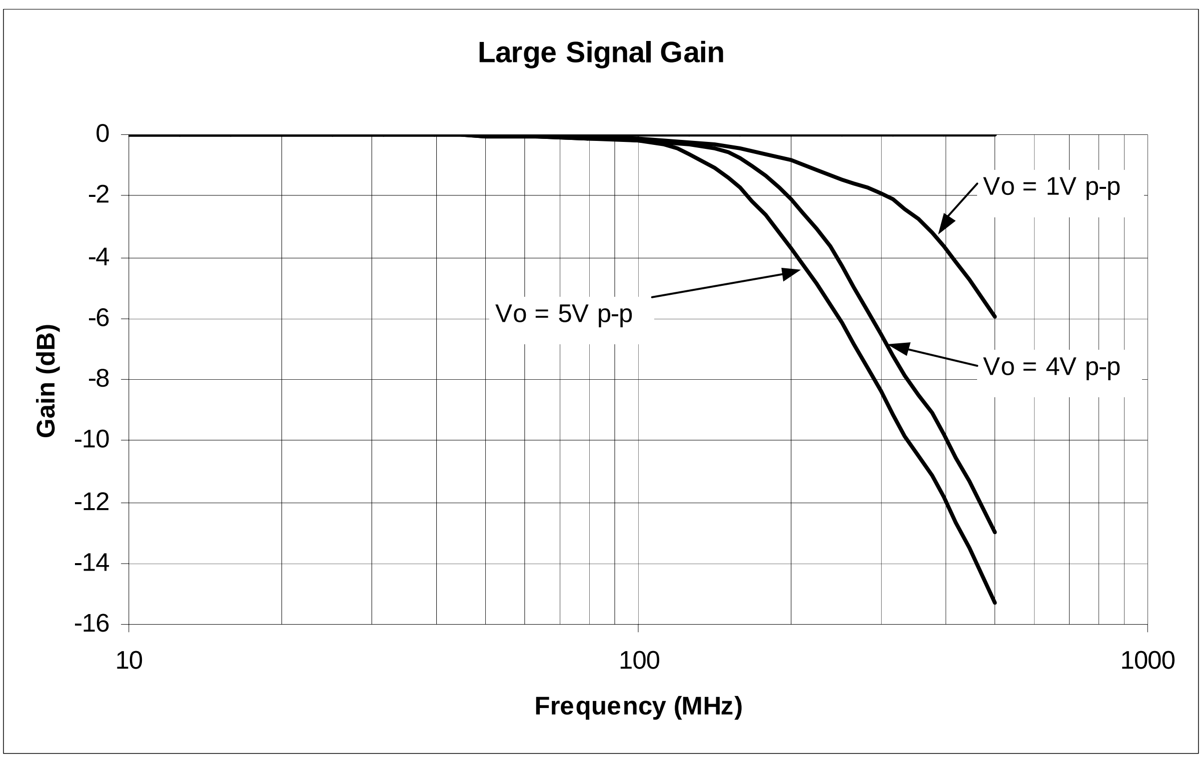
Note: Test Types:

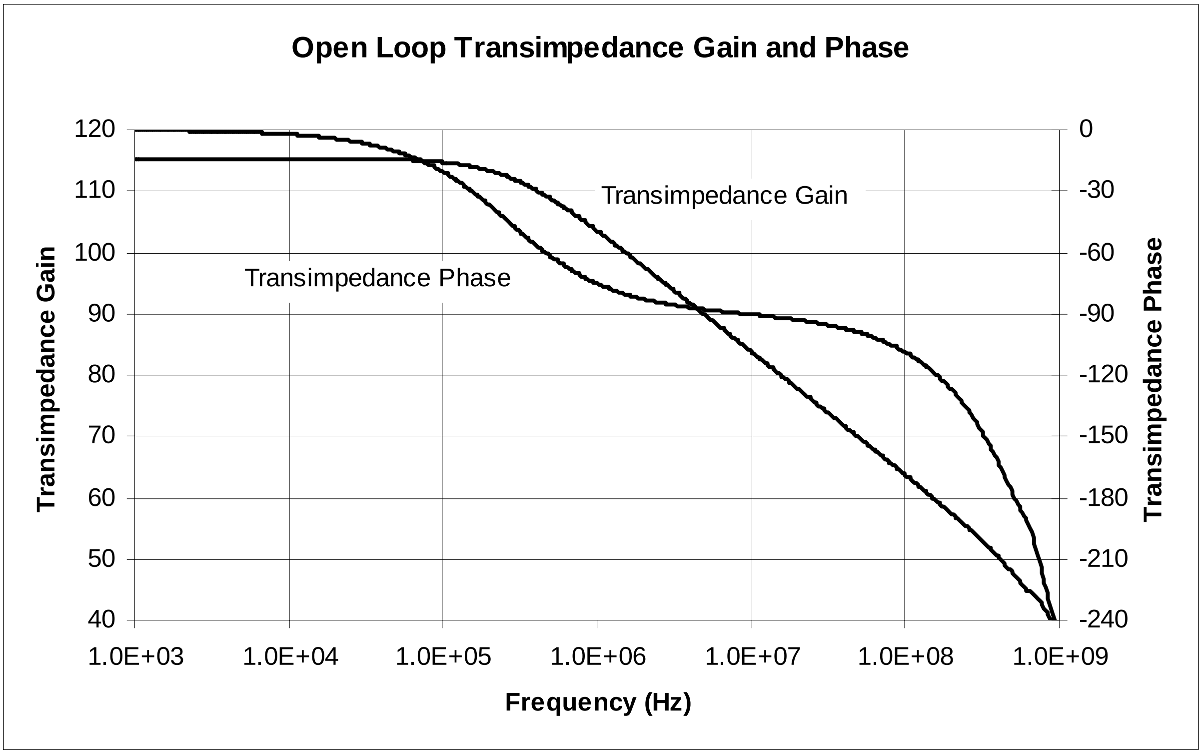
(A) 100% tested at 25°C. Over temperature limits are set by characterization and simulation.
(B) Limits set by characterization or simulation.
(C) Typical value only for information.

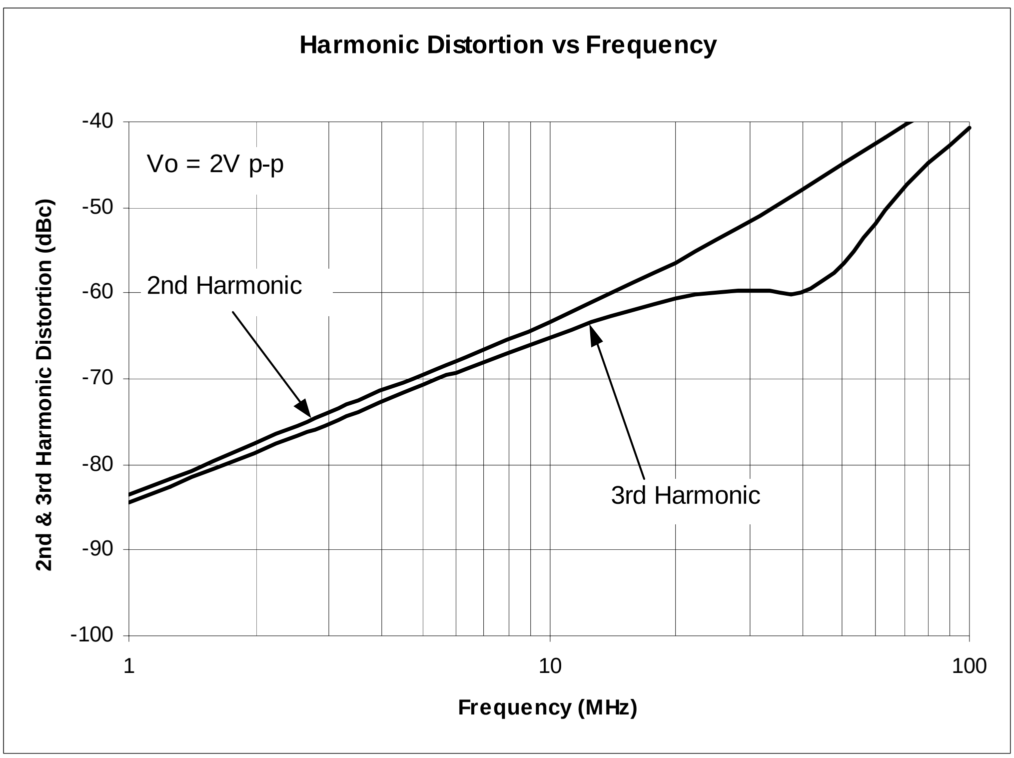
Typical Performance Characteristics - T_{amb}=25°C, V_{supply}=± 5 V, Rload=100 Ω, Av=+2V/V, Rf=510 Ω, unless otherwise specified.

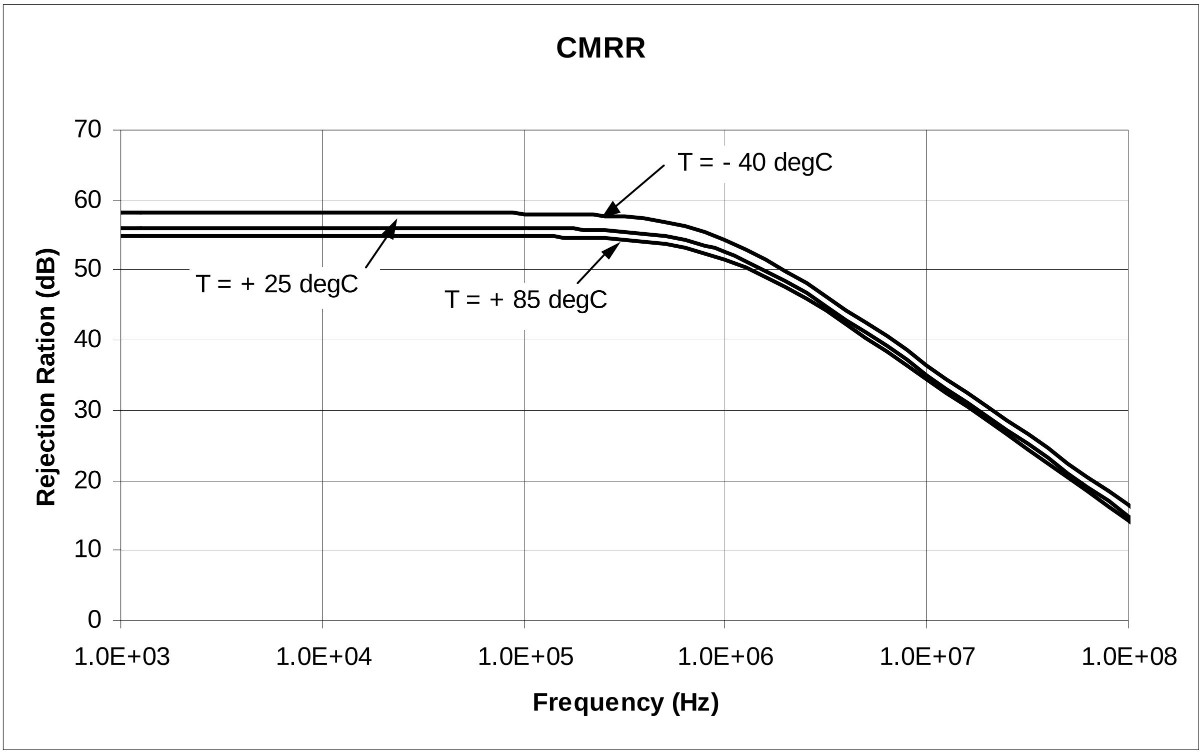


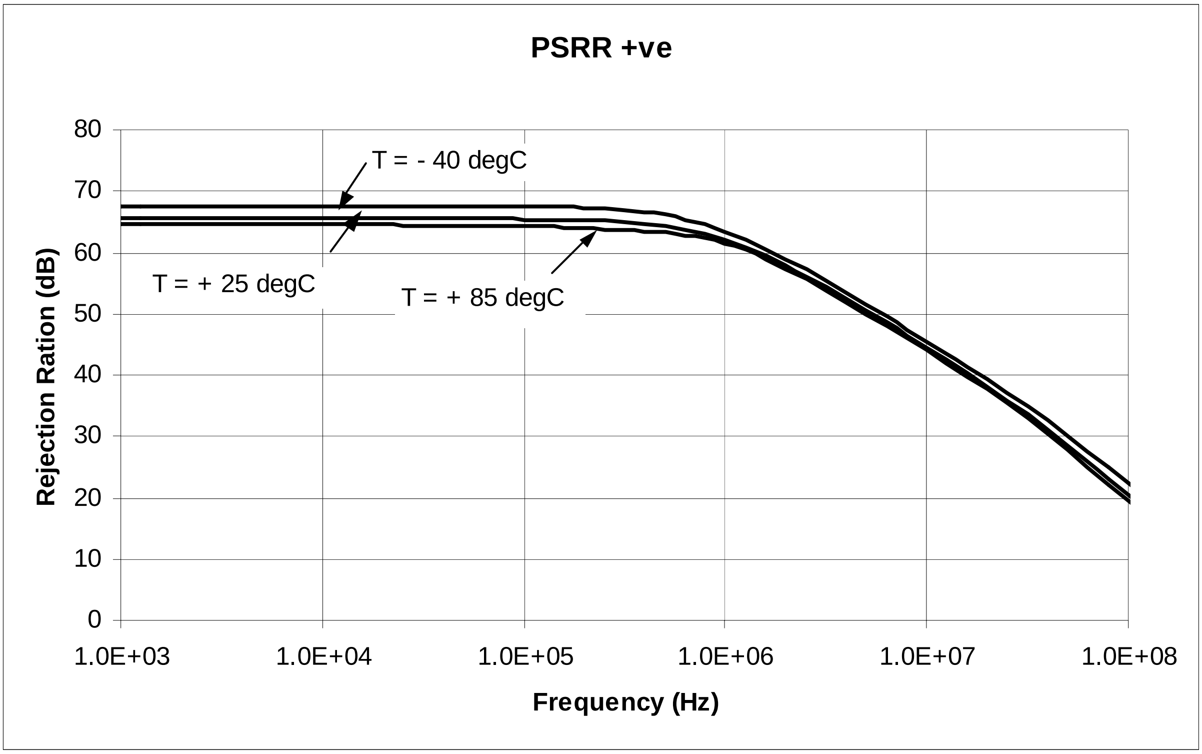

Non-Inverting Frequency Response varying Rf
Normalised Gain (dB)
2
0
-2
-4
-6
-8
-10
-12
-14
-16
-18
10
100
1000
Frequency (MHz)
Rf=390
Rf=250
Rf=700
Rf=510
Vo=0.5Vp-p

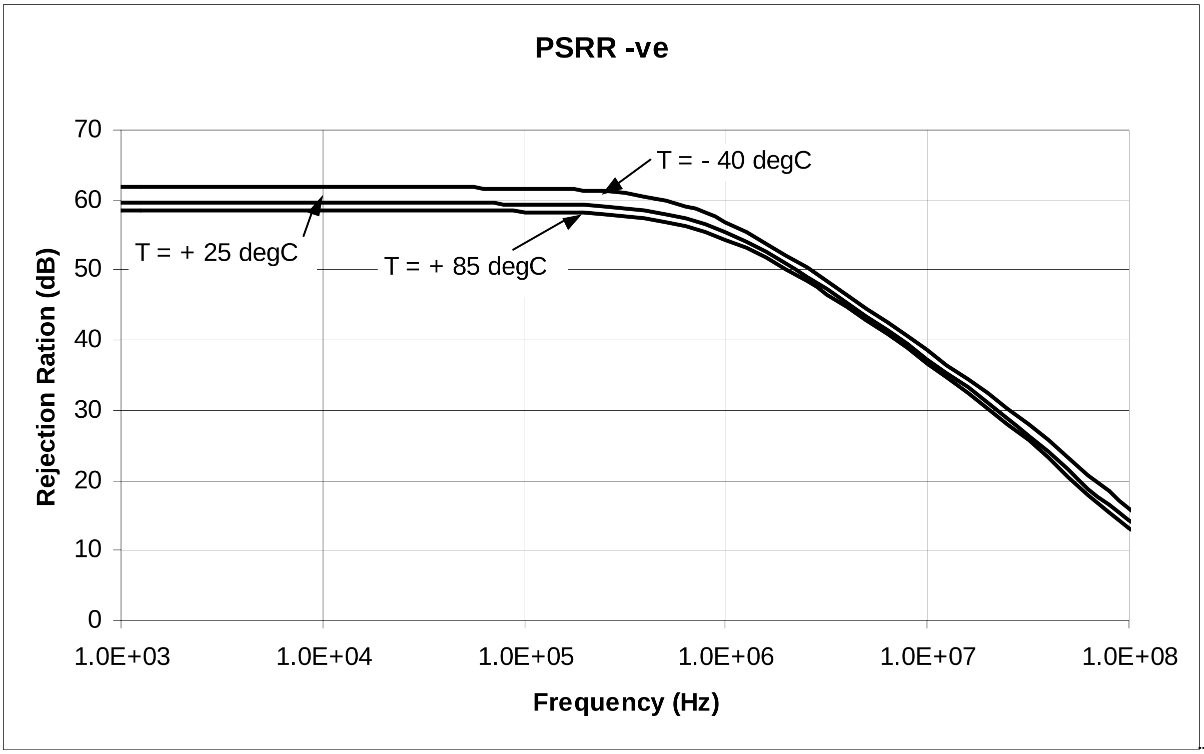

Large Signal Gain
Gain (dB)
0
-2
-4
-6
-8
-10
-12
-14
-16
10
100
1000
Frequency (MHz)
Vo = 1V p-p
Vo = 5V p-p
Vo = 4V p-p

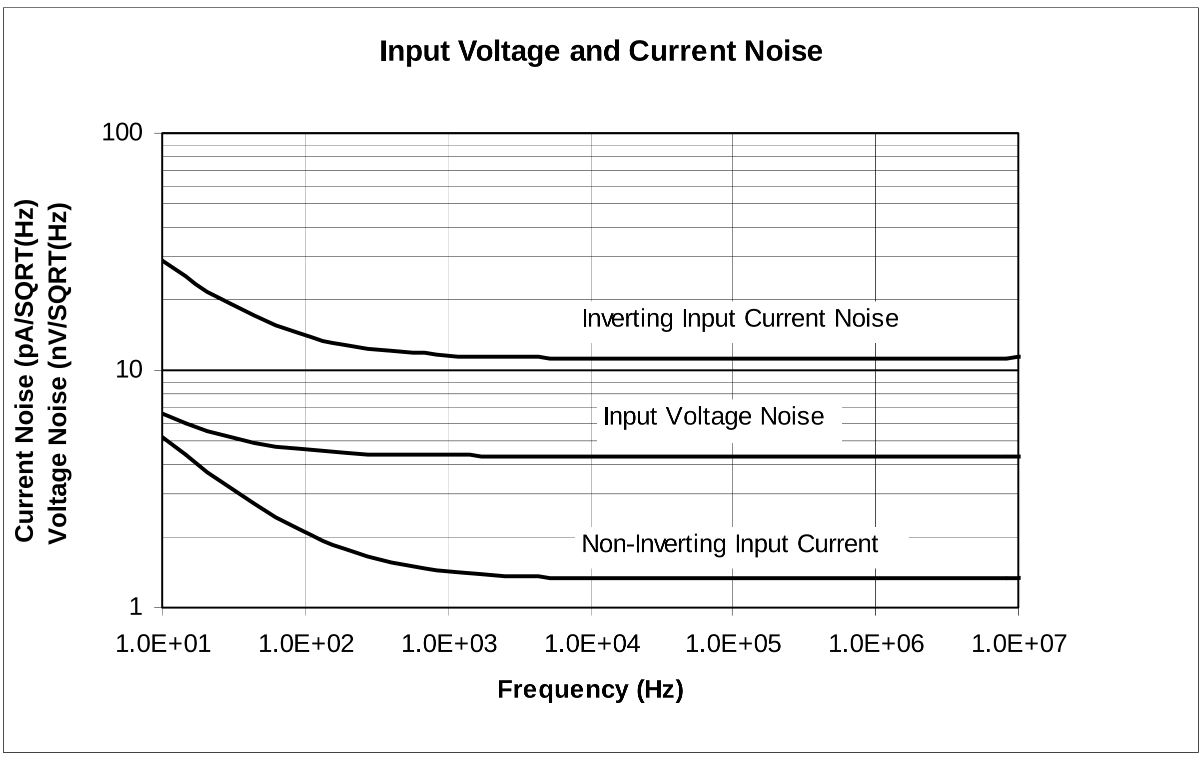

Open Loop Transimpedance Gain and Phase
Transimpedance Gain
Transimpedance Phase
Transimpedance Gain
Transimpedance Phase
Frequency (Hz)
120
110
100
90
80
70
60
50
40
0
-30
-60
-90
-120
-150
-180
-210
-240
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
1.0E+09

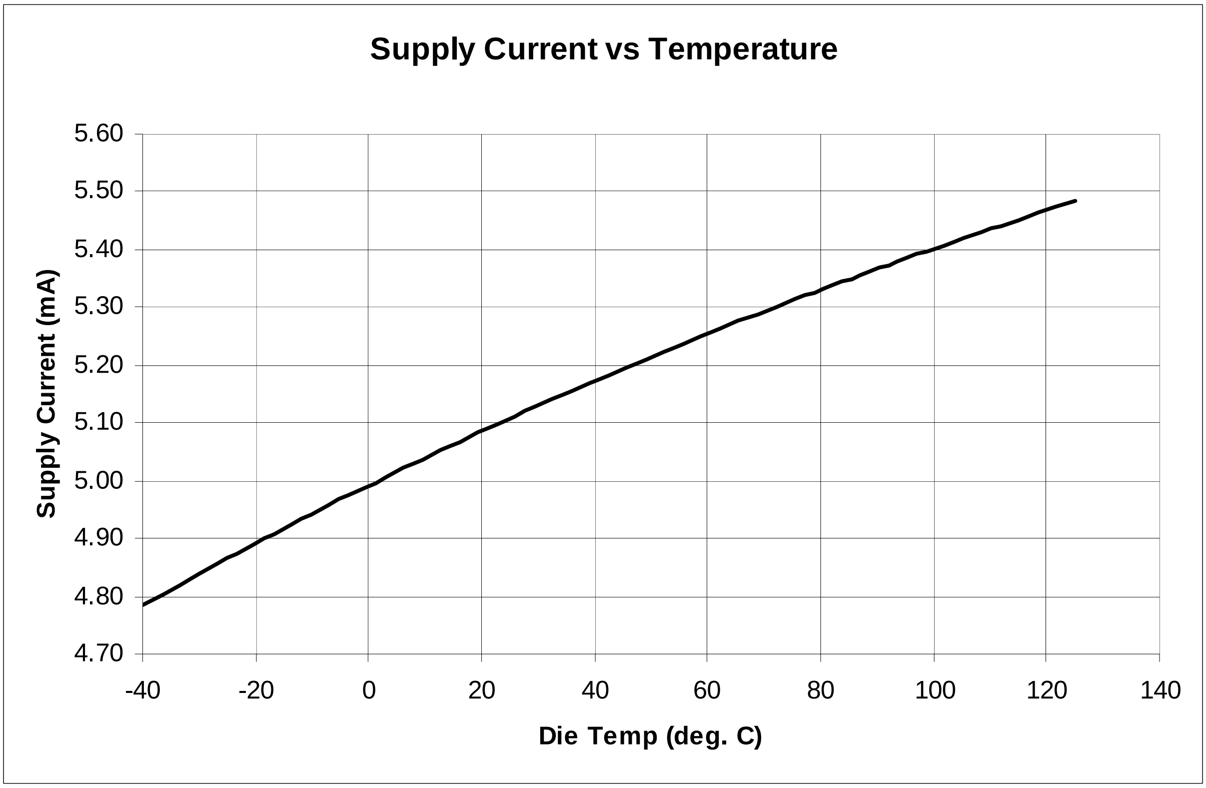

Harmonic Distortion vs Frequency
Vo = 2V p-p
2nd Harmonic
3rd Harmonic
2nd & 3rd Harmonic Distortion (dBc)
Frequency (MHz)
-40
-50
-60
-70
-80
-90
-100
1
10
100

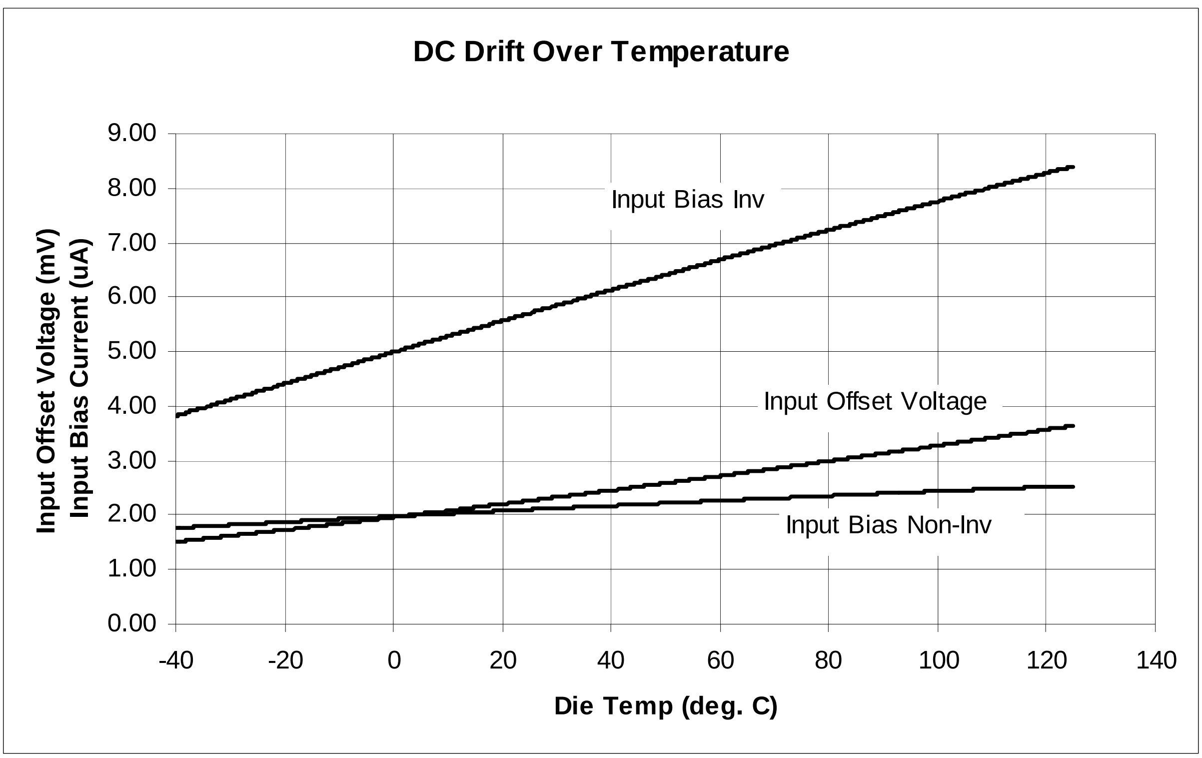

CMRR
T = - 40 degC
T = + 25 degC
T = + 85 degC
Rejection Ration (dB)
70
60
50
40
30
20
10
0
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)

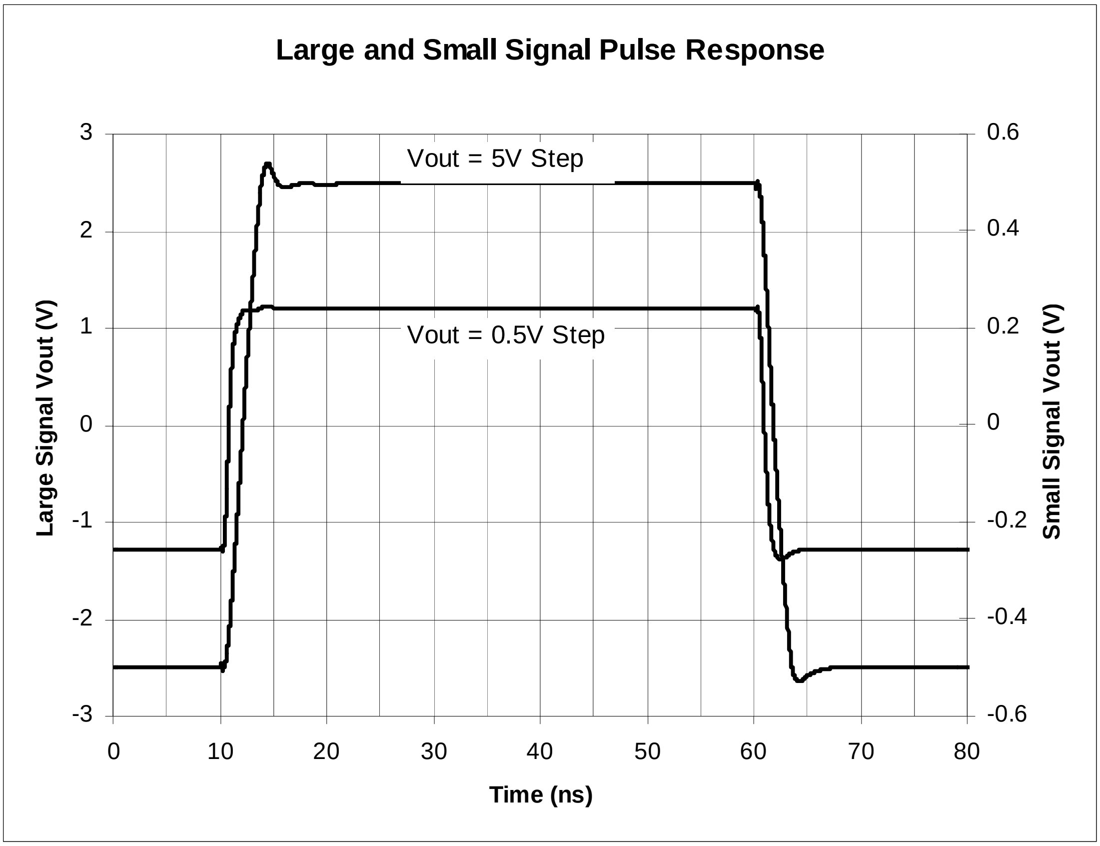

PSRR +ve
T = - 40 degC
T = + 25 degC
T = + 85 degC
Rejection Ration (dB)
80
70
60
50
40
30
20
10
0
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)

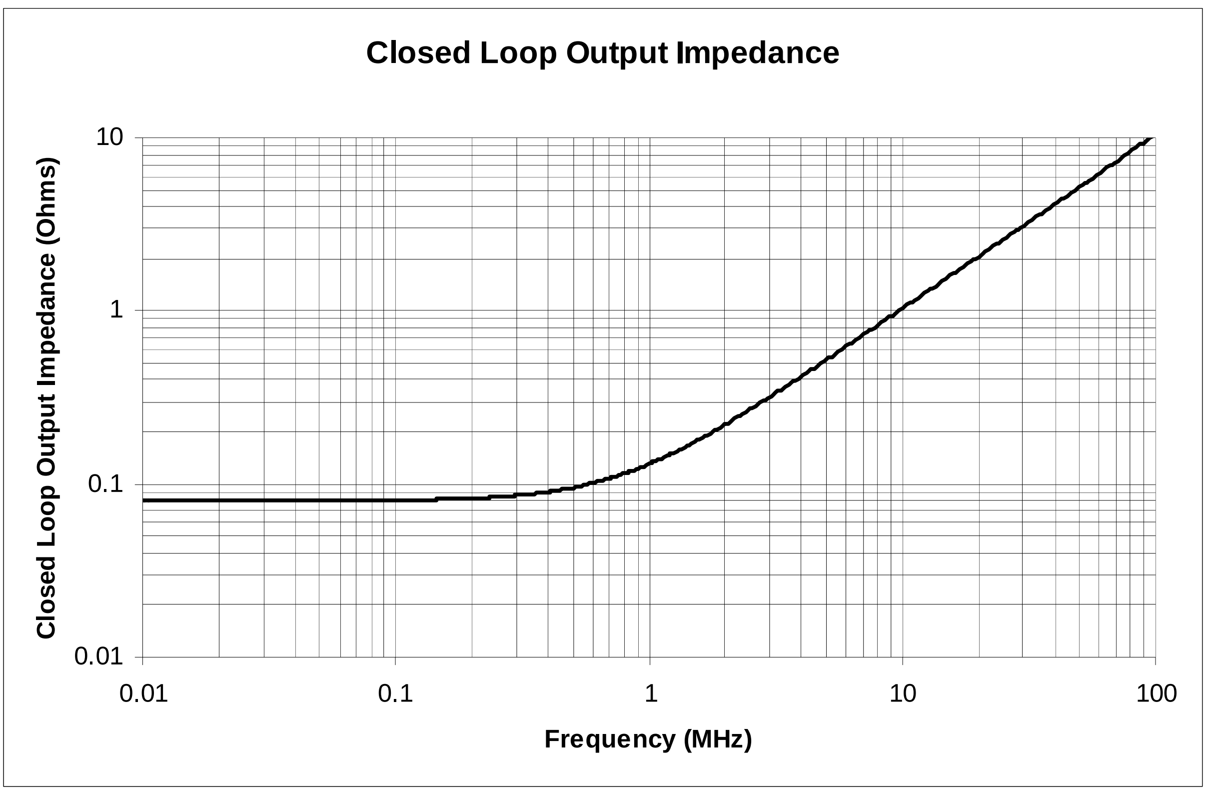

PSRR -ve
T = - 40 degC
T = + 25 degC
T = + 85 degC
70
60
50
40
30
20
10
0
Rejection Ration (dB)
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)

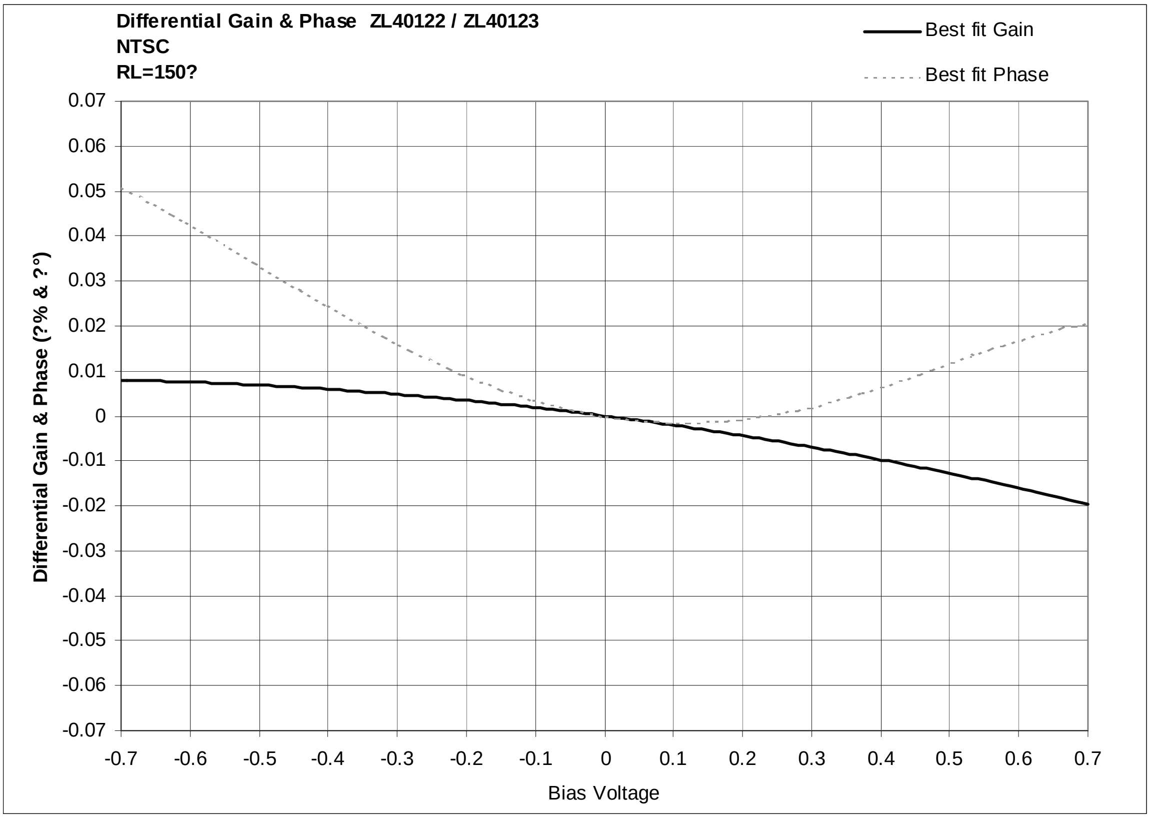

Input Voltage and Current Noise
100
10
1
Current Noise (pA/SQRT(Hz)
Voltage Noise (nV/SQRT(Hz)
Inverting Input Current Noise
Input Voltage Noise
Non-Inverting Input Current
1.0E+01
1.0E+02
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
Frequency (Hz)

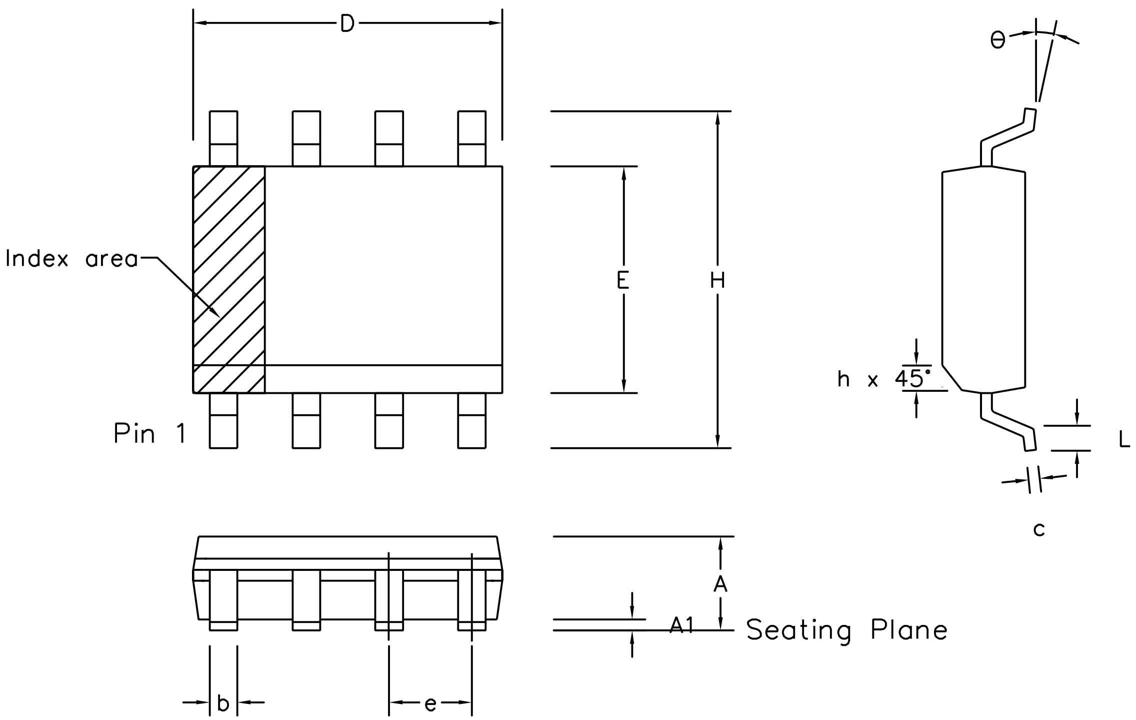

Supply Current vs Temperature
5.60
5.50
5.40
5.30
5.20
5.10
5.00
4.90
4.80
4.70
Supply Current (mA)
-40
-20
0
20
40
60
80
100
120
140
Die Temp (deg. C)


DC Drift Over Temperature
9.00
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
Input Offset Voltage (mV)
Input Bias Current (uA)
Input Bias Inv
Input Offset Voltage
Input Bias Non-Inv
-40
-20
0
20
40
60
80
100
120
140
Die Temp (deg. C)


Large and Small Signal Pulse Response
Vout = 5V Step
Vout = 0.5V Step
Large Signal Vout (V)
Small Signal Vout (V)
Time (ns)
3
2
1
0
-1
-2
-3
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0
10
20
30
40
50
60
70
80


Closed Loop Output Impedance
Closed Loop Output Impedance (Ohms)
Frequency (MHz)
10
1
0.1
0.01
0.01
0.1
1
10
100


Differential Gain & Phase ZL40122 / ZL40123
NTSC
RL=150?
Best fit Gain
Best fit Phase
Differential Gain & Phase (?% & ?°)
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
-0.07
-0.7
-0.6
-0.5
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
Bias Voltage



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
O	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

GPD00010

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com