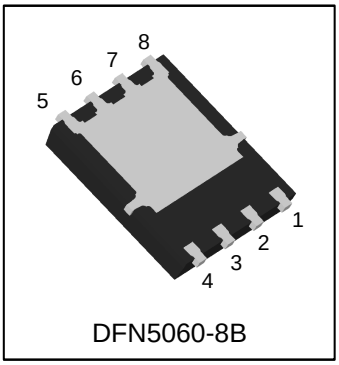
LN7610DT1WG

N-Channel Power Trench MOSFET



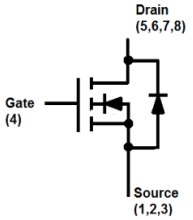
DFN5060-8B

1. FEATURES

- Max RDS(on) = 9 mΩ at VGS = 10 V, ID = 13 A
- Advanced Package and Silicon combination for low RDS(on) and high efficiency.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS

- DC-DC Conversion



3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
LN7610DT1WG	LN7610	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	100	V
Gate-to-Source Voltage		VGS	+20/-12	V
Continuous Drain Current	TC=25℃	ID	60	A
	TA=25℃		12.4	A
Pulsed Drain Current	TC=25℃	ID	200	A
Avalanche Current(L=0.1mH)		IAS	36	A
Avalanche Energy(L=0.1mH)		EAS	64.8	mJ
Power Dissipation	TC=25℃	PD	104	W
	TA=25℃		2.5	
Operating Junction and Storage Temperature Range		Tj/Tstg	-55~+150	℃

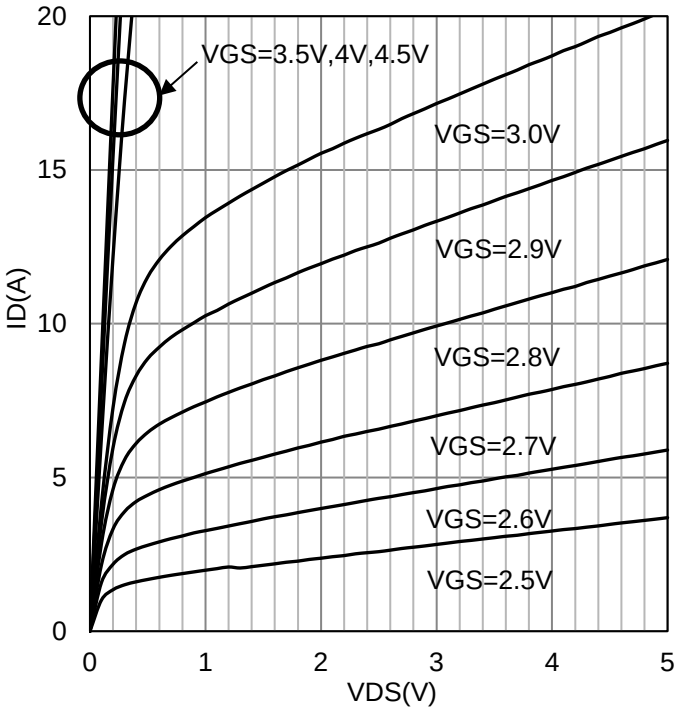
5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction-to-Ambient	Rthja	50	℃/W
Junction-to-Case	Rthjc	1.2	

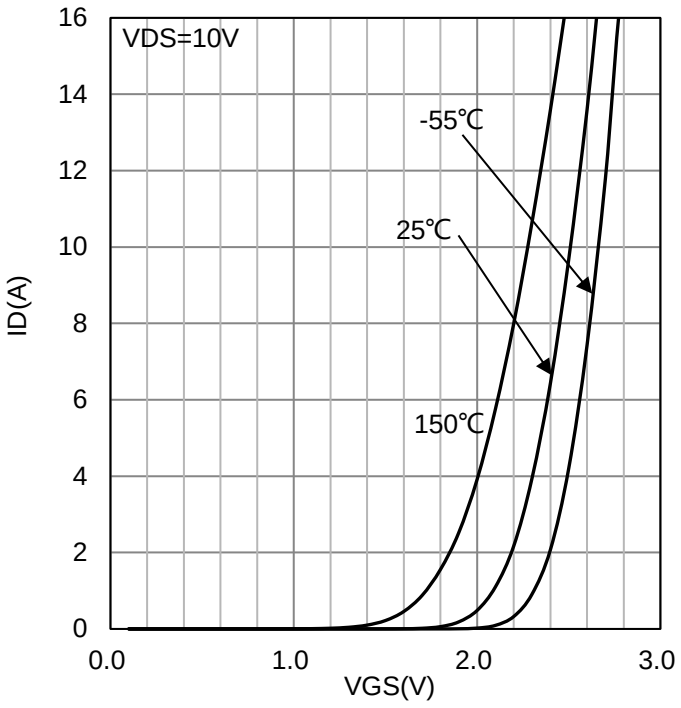
6. ELECTRICAL CHARACTERISTICS (Ta= 25ºC)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Drain to Source Breakdown Voltage (VGS =0V, ID =250μA)		VDSS	100	-	-	V
Drain-to-Source Leakage Current (VDS =80V, VGS =0V)		IDSS	-	-	800	nA
Gate-Body leakage current,Forward (VDS =0V, VGS = 20V)		IGSSF	-	-	100	nA
Gate-Body leakage current,Reverse (VDS =0V, VGS = -12V)		IGSSR	-	-	-100	nA
Gate Threshold Voltage (VDS = VGS , ID = 250μA)		VGS(TH)	1	1.5	3	V
Drain-to-Source On-Resistance (VGS = 10 V, ID = 13 A) (VGS = 4.5 V, ID = 7 A) (VGS = 10 V, ID = 13 A, TJ = 125 °C)		RDS(ON)	- - -	7.2 9 10.9	9 14 14	mΩ
Gate Resistance		Rg	-	1.2	6	Ω
Forward Transconductance (VDS = 10V, ID = 13A)		gfs	-	20	-	S
Total Gate Charge VGS(0 ~10 V)	(ID =13A,VDD =50V)	Qg	-	45	60	nC
Total Gate Charge VGS(0 ~5 V)		Qg	-	27	-	
Gate to Source Charge		Qgs	-	6	-	
Gate to Drain Charge		Qgd	-	16	-	
Turn-on Delay Time	(VDD = 50V, ID = 13A, RG = 6 Ω,VGS = 10V)	td(on)	-	15	-	nS
Rise Time		tr	-	8	-	
Turn-Off Delay Time		td(off)	-	23	-	
Fall Time		tf	-	7	-	
Input Capacitance	(VGS = 0V ,VDS = 50V, f = 1MHz)	Ciss	-	2370	-	pF
Output Capacitance		Coss	-	489	-	
Reverse Transfer Capacitance		Crss	-	33.6	-	
Diode Forward Voltage (VGS = 0 V, IS = 2.1 A) (VGS = 0 V, IS = 13 A)		VSD	- -	0.7 0.8	1.2 1.3	V
Reverse Recovery Time (IF = 13 A, di/dt = 100 A/μs)		trr	-	56	90	nS
Reverse Recovery Charge (IF = 13 A, di/dt = 100 A/μs)		Qrr	-	80	118	nC

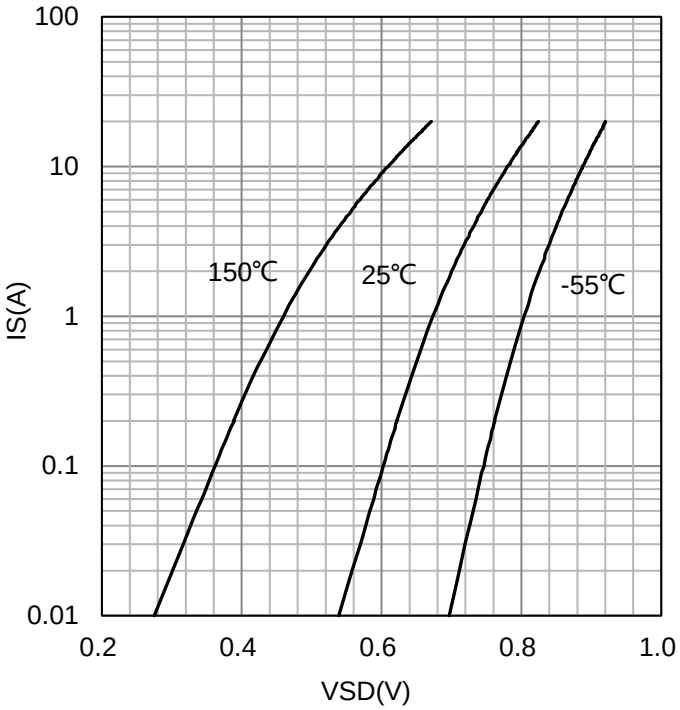
7.ELECTRICAL CHARACTERISTICS CURVES



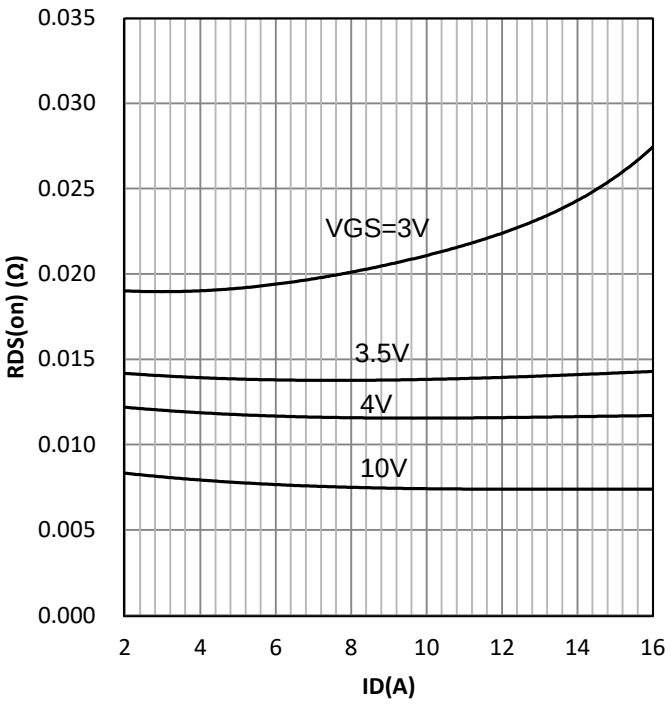
ID vs. VDS



ID vs. VGS

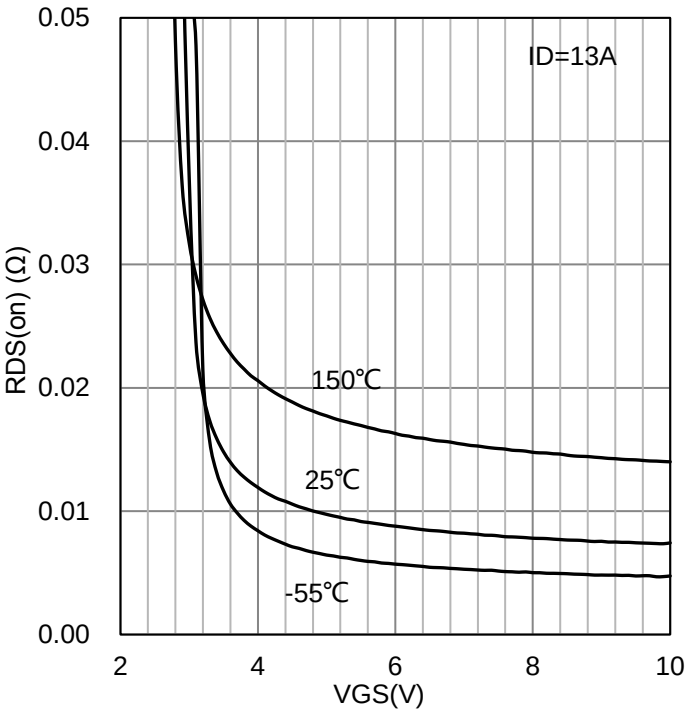


IS vs. VSD

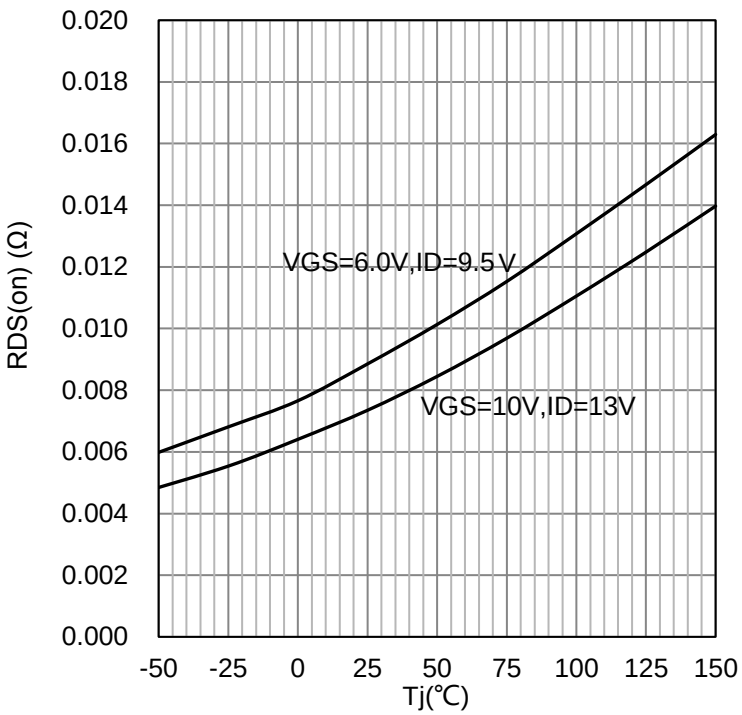


RDS(on) vs. ID

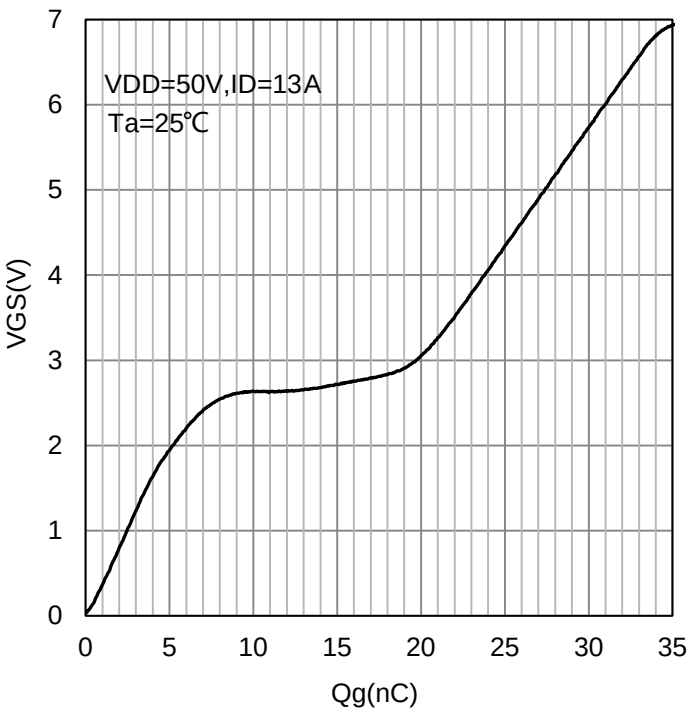
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



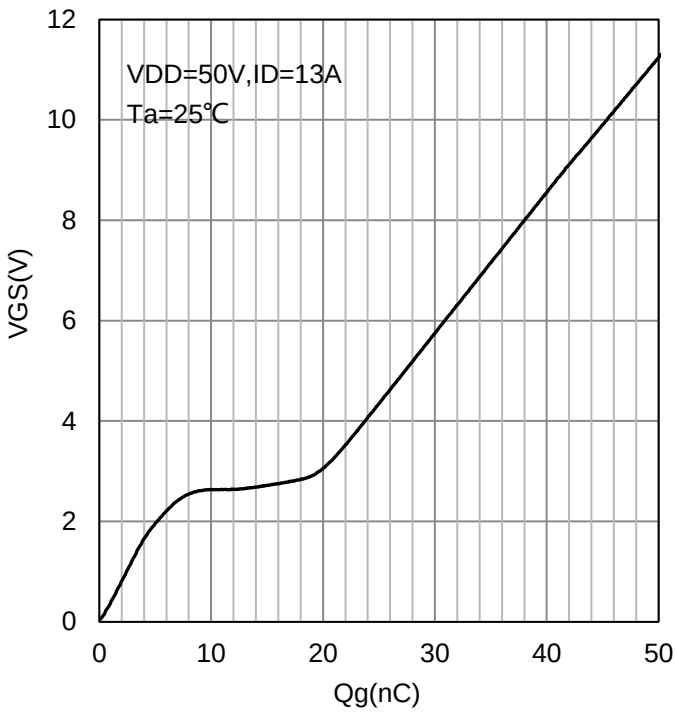
RDS(on) vs. VGS



RDS(on) vs. Tj

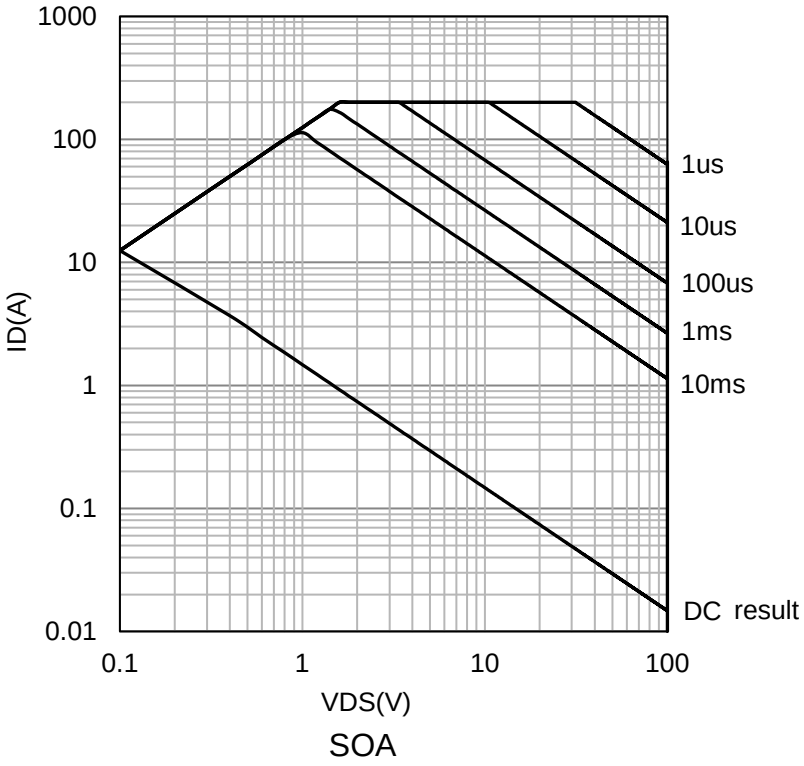


VGS vs. Qg (VGS=5V)

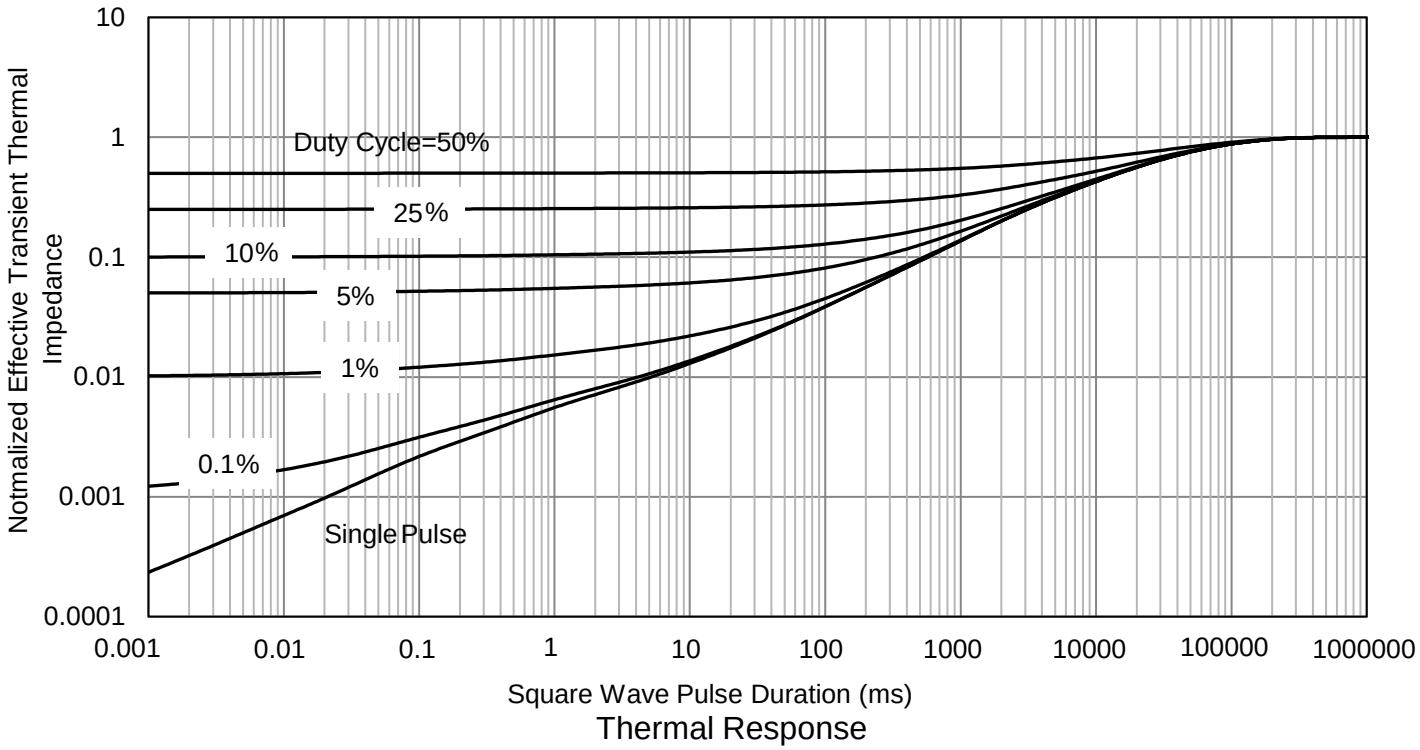


VGS vs. Qg (VGS=10V)

7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



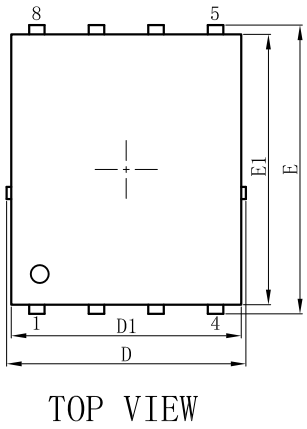
SOA

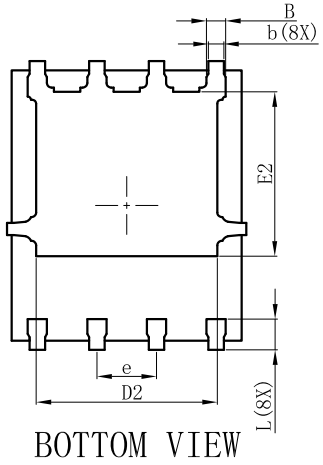


Thermal Response

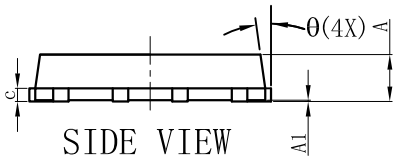
8.OUTLINE AND DIMENSIONS

DFN5060-8B





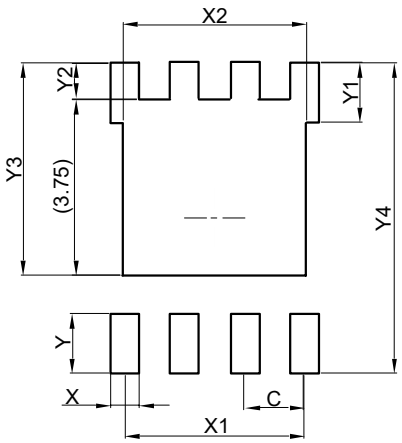
DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			



GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61