



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Delete Icc1 Spec.	Sep.21.2004
Rev. 1.2	Added I Grade Spec. Revised Test Condition of I _{CC} /I _{SB1} /I _{DR} Revised V _{TERM} to V _{T1} and V _{T2} Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS Added packing type in ORDERING INFORMATION	Apr.20.2009
Rev. 1.3	Adding PKG type : 32 TSOP-II	Jan.5.2010
Rev. 1.4	Revised PACKAGE OUTLINE DIMENSION in page 8	May.7.2010
Rev. 1.5	Revised ORDERING INFORMATION in page 10	Aug.25.2010

FEATURES

- Fast access time : 8/10/12/15ns
- Low power consumption:
Operating current : 80/75/70/65mA (TYP.)
Standby current : 0.6mA (TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 32-pin 8mm x 13.4mm STSOP
32-pin 400 mil TSOP-II

GENERAL DESCRIPTION

The LY61L1288 is a 1,048,576-bit high speed CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

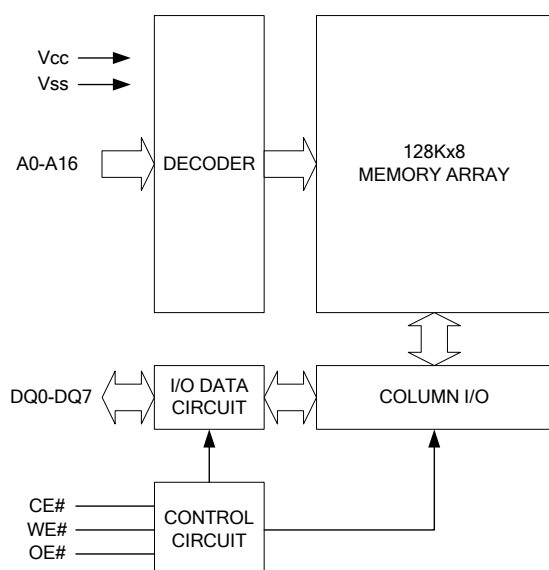
The LY61L1288 is well designed for high speed system application. Easy expansion is provided by using an active LOW Chip Enable(CE#). The active LOW Write Enable(WE#) controls both writing and reading of the memory.

The LY61L1288 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY61L1288	0 ~ 70°C	3.15 ~ 3.6V	8/10ns	0.6mA	80/75mA
LY61L1288	0 ~ 70°C	3.0 ~ 3.6V	12/15ns	0.6mA	70/65mA
LY61L1288(E)	-20 ~ 80°C	3.15 ~ 3.6V	8/10ns	0.6mA	80/75mA
LY61L1288(E)	-20 ~ 80°C	3.0 ~ 3.6V	12/15ns	0.6mA	70/65mA
LY61L1288(I)	-40 ~ 85°C	3.15 ~ 3.6V	8/10ns	0.6mA	80/75mA
LY61L1288(I)	-40 ~ 85°C	3.0 ~ 3.6V	12/15ns	0.6mA	70/65mA

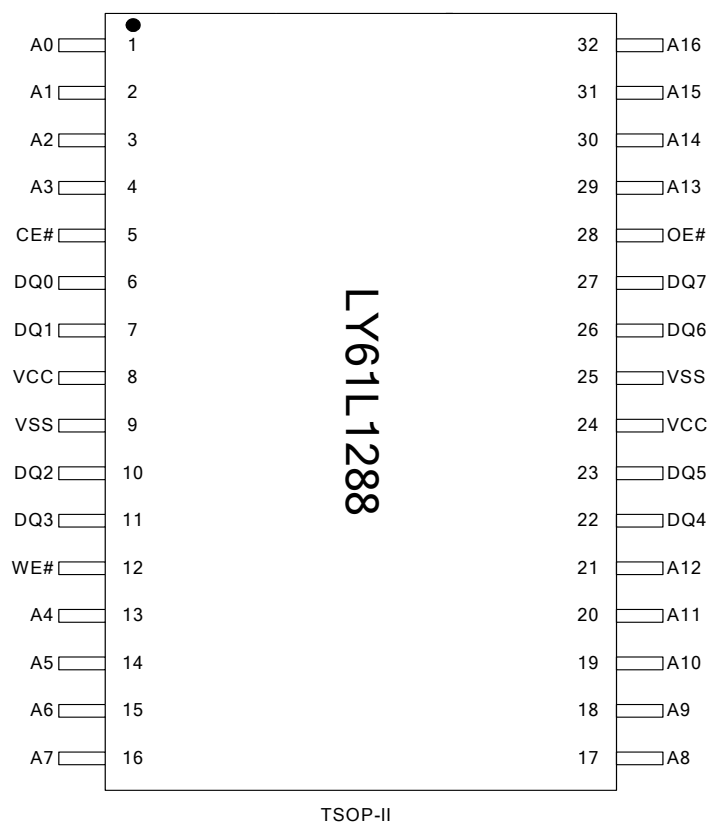
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}		-8/-10	3.15	3.3	V
			-12/-15	3.0	3.3	V
Input High Voltage	V _{IH} ¹		2.0	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ²		-0.3	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Other pins at V _{IH} or V _{IL}	-8	80	150	mA
			-10	75	120	mA
			-12	70	100	mA
			-15	65	90	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} , others at V _{IH} or V _{IL}	-	3	10	mA
	I _{SB1}	CE# ≥ V _{CC} - 0.2V, Other pins at 0.2V or V _{CC} -0.2V	-	0.6	3 ⁵	mA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- 1mA for special request

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

PARAMETER	SYM.	LY61L1288 -8		LY61L1288 -10		LY61L1288 -12		LY61L1288 -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns

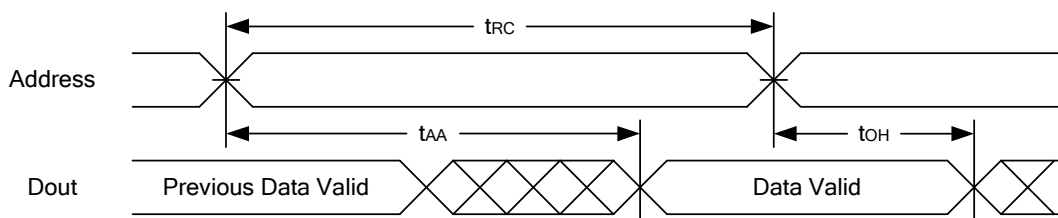
(2) WRITE CYCLE

PARAMETER	SYM.	LY61L1288 -8		LY61L1288 -10		LY61L1288 -12		LY61L1288 -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	6.5	-	8	-	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	6.5	-	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	1.5	-	2	-	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	5	-	6	-	7	-	8	ns

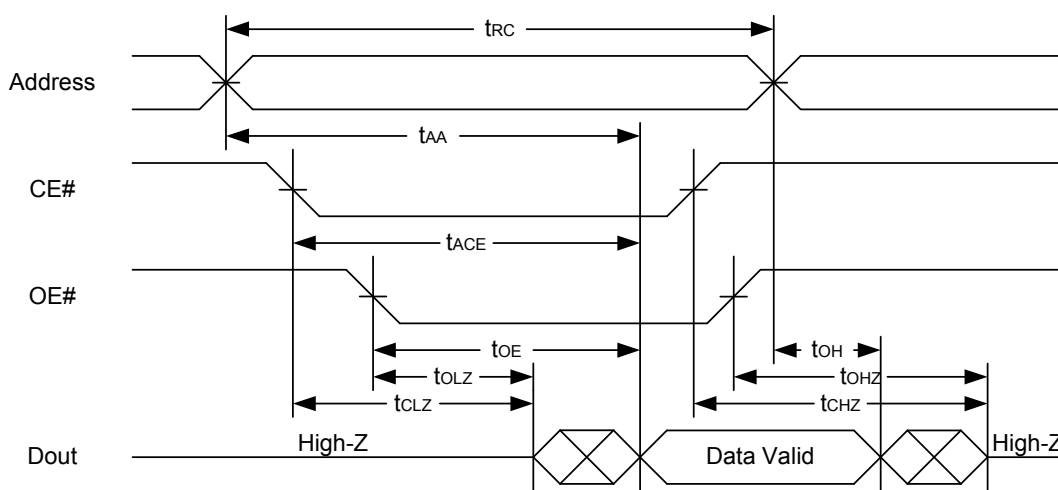
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

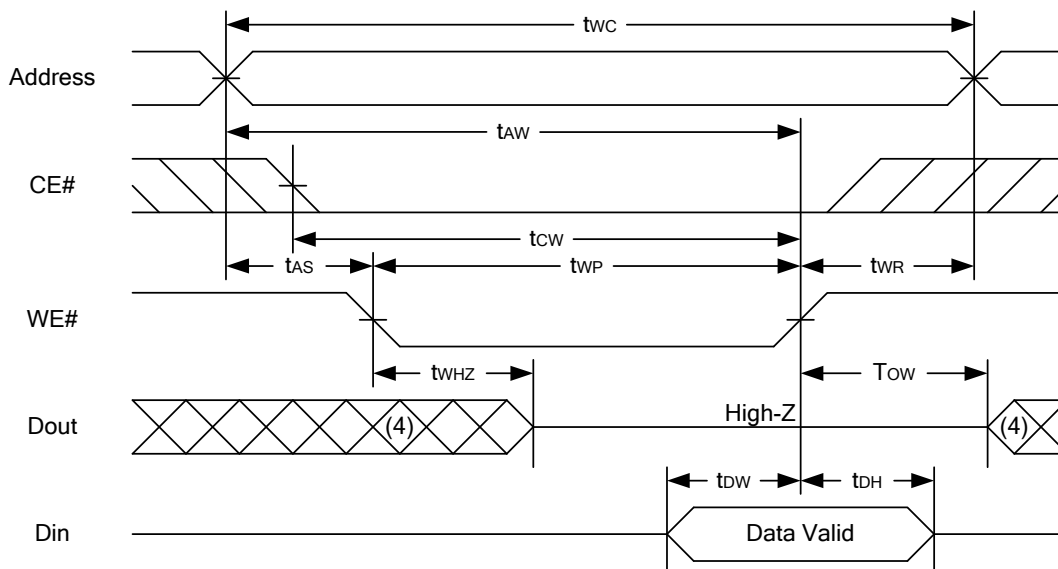


Notes :

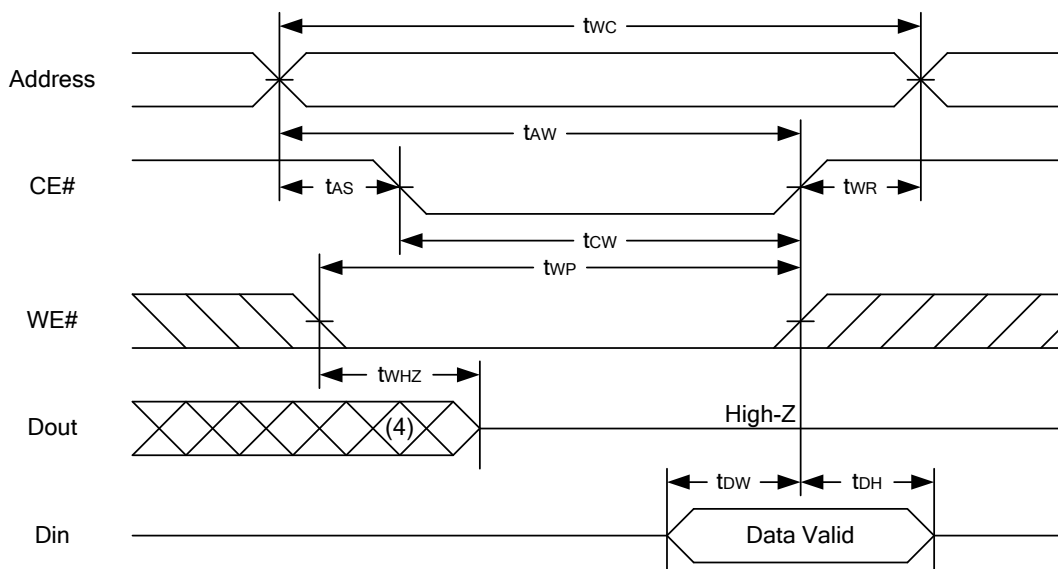
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

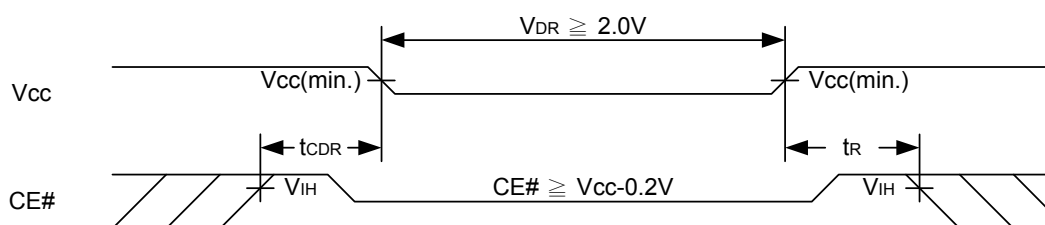
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.

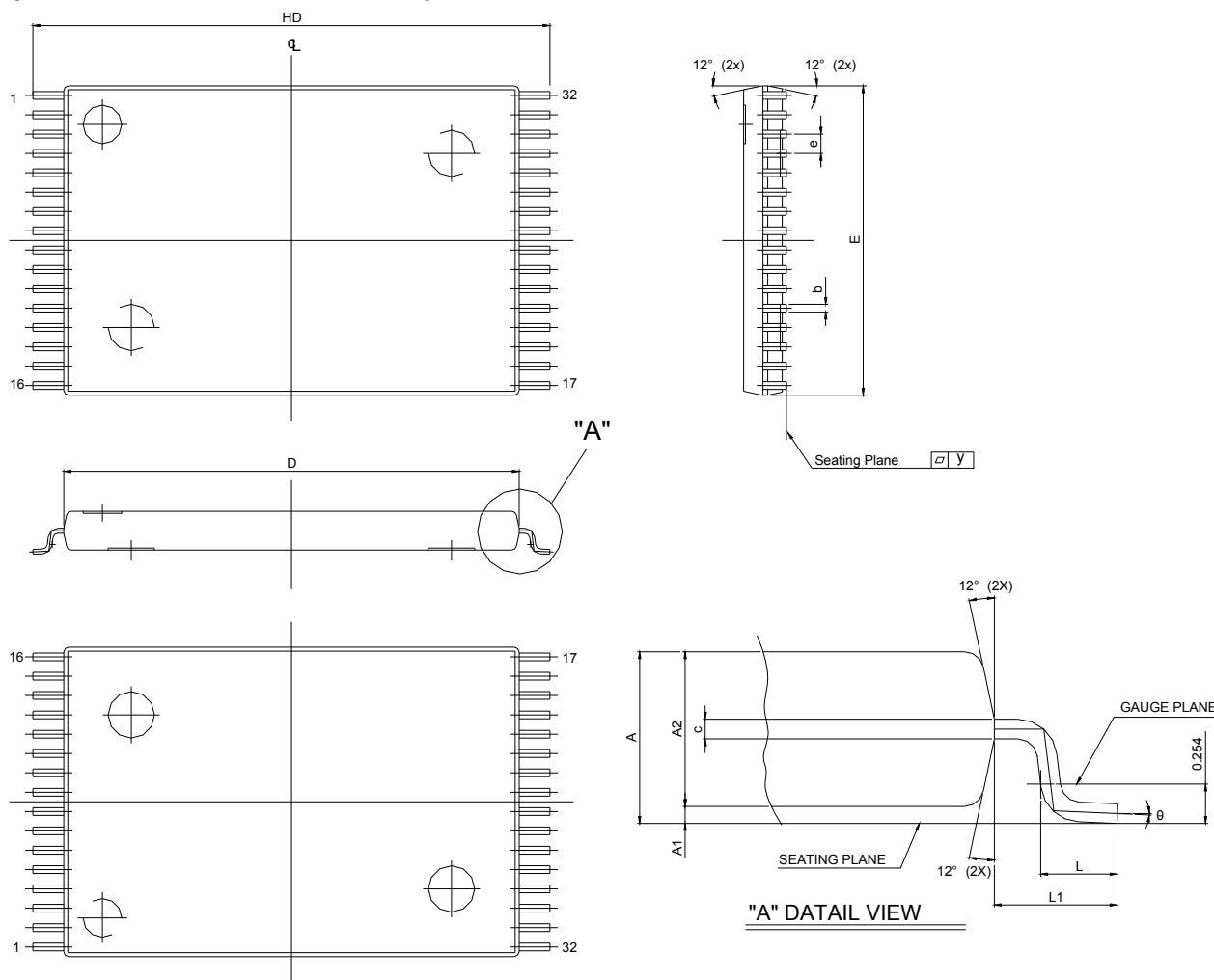
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	2.0	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V others at 0.2V or V _{CC} - 0.2V	-	0.4	2	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

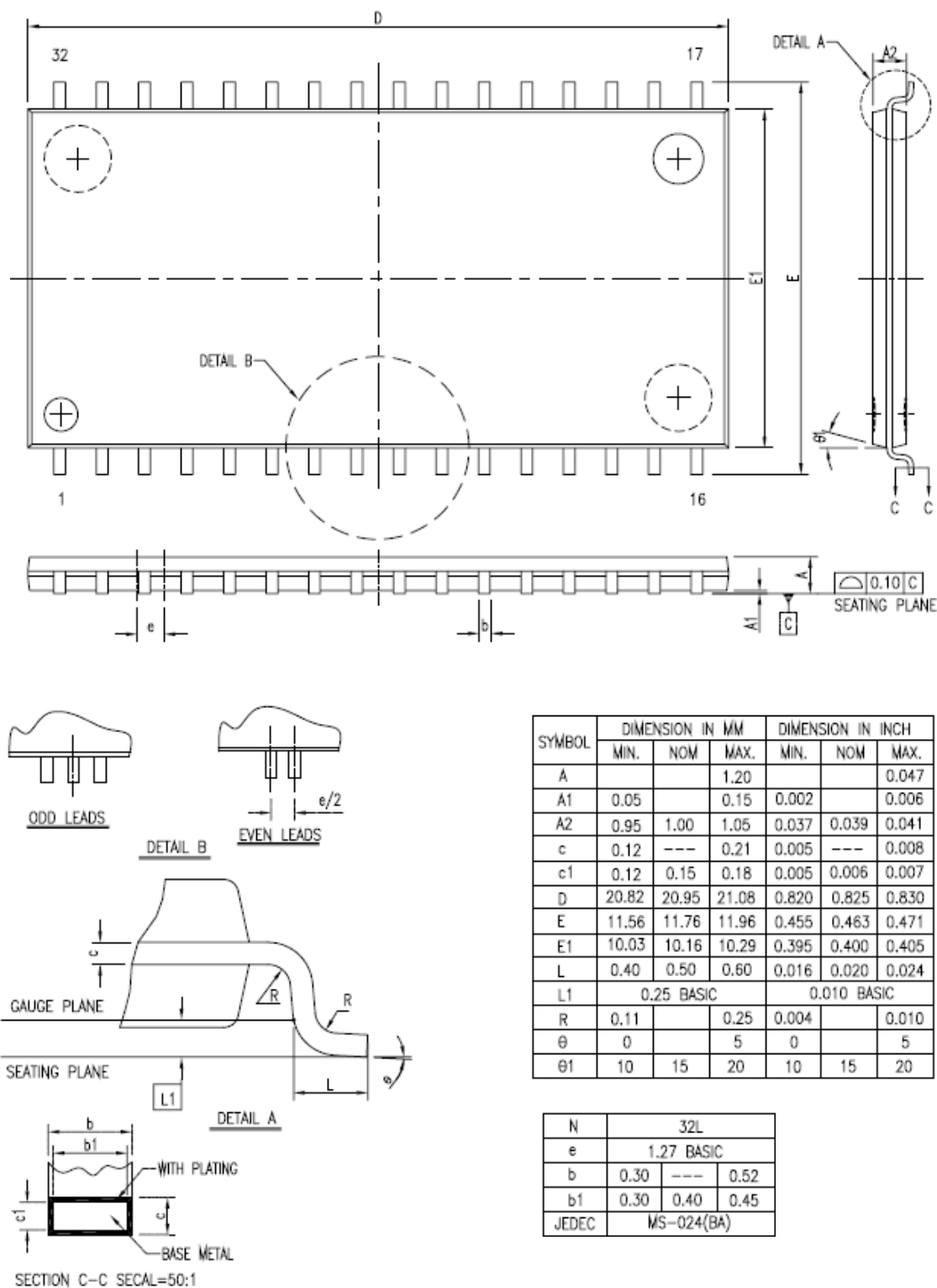
DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION
32 pin 8mm x 13.4mm STSOP Package Outline Dimension


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.465 ±0.008	11.80 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.02 ±0.008	0.50 ±0.20
L1		0.031 ±0.005	0.8 ±0.125
y		0.003 (MAX)	0.076 (MAX)
Θ		0°~5°	0°~5°

32-pin 400mil TSOP- II Package Outline Dimension





ORDERING INFORMATION

LY61L1288 U V - WW Y Z

Z : Packing Type

Blank : Tube or Tray

Tray : 32-pin 8 mm X 13.4 mm STSOP

32-pin 400 mil TSOP-II

T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C

E : (Extended) -20°C ~ +80°C

I : (Industrial) -40°C ~ +85°C

WW : Access Time(Speed)

V : Lead Information

L : Lead Free

U : Package Type

R : 32-pin 8 mm X 13.4 mm STSOP

W : 32-pin 400 mil TSOP-II



Lyontek Inc.

LY61L1288

Rev. 1.5

128K X 8 BIT HIGH SPEED CMOS SRAM

THIS PAGE IS LEFT BLANK INTENTIONALLY.