MH16D72AKLB-10,75

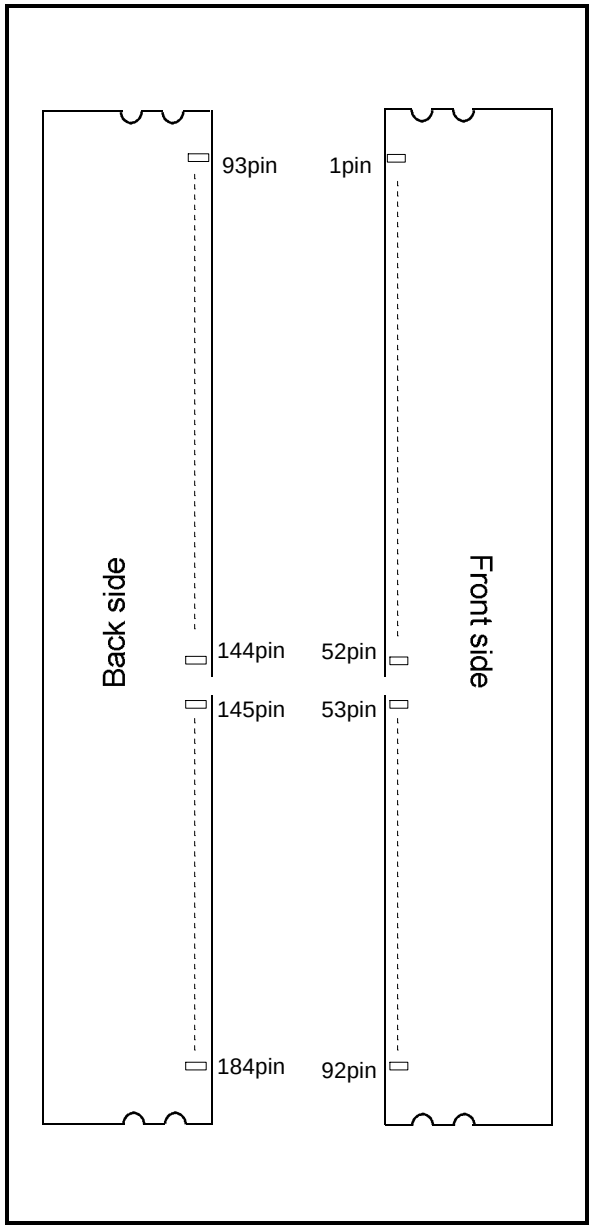
1,207.959,552-BIT (16,777,216-WORD BY 72-BIT) Double Data Rate Synchronous DRAM Module

DESCRIPTION

The MH16D72AKLB is 16777216 - word x 72-bit Double Data Rate(DDR) Synchronous DRAM mounted module.

This consists of 9 industry standard 16M x 8 DDR Synchronous DRAMs in TSOP with SSTL_2 interface which achieves very high speed data rate up to 133MHz.

This socket-type memory module is suitable for main memory in computer systems and easy to interchange or add modules.



FEATURES

Type name	Max. Frequency	CLK Access Time [component level]
MH16D72AKLB-75	133MHz	± 0.75ns
MH16D72AKLB-10	100MHz	± 0.8ns

- Utilizes industry standard 16M X 8 DDR Synchronous DRAMs in TSOP package , industry standard Registered Buffer in TSSOP package , and industry standard PLL in TSSOP package.
- Vdd=Vddq=2.5v ±0.2V
- Double data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data
- Differential clock inputs (CK0 and /CK0)
- data and data mask referenced to both edges of DQS
- /CAS latency - 2.0/2.5 (programmable)
- Burst length- 2/4/8 (programmable)
- Auto precharge / All bank precharge controlled by A10
- 4096 refresh cycles /64ms
- Auto refresh and Self refresh
- Row address A0-11 / Column address A0-9
- SSTL_2 Interface
- Module 1bank Configration
- Burst Type - sequential/interleave(programmable)
- Commands entered on each positive CLK edge

APPLICATION

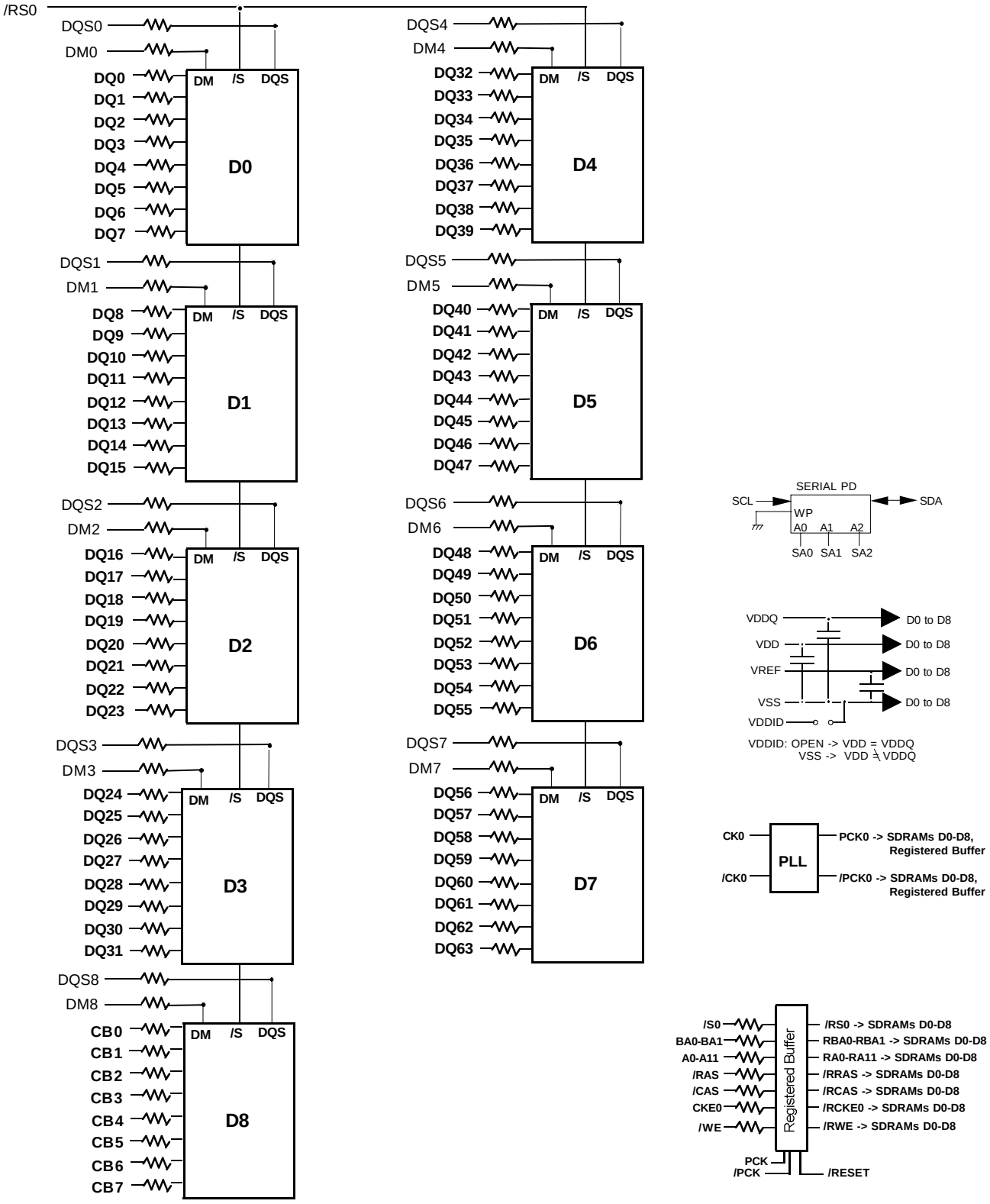
Main memory unit for PC, PCserver

PIN CONFIGURATION

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	VREF	43	A1	84	DQ57	126	DQ28	167	NC
2	DQ0	44	CB0	85	VDD	127	DQ29	168	VDD
3	VSS	45	CB1	86	DQS7	128	VDDQ	169	DM6
4	DQ1	46	VDD	87	DQ58	129	DM3	170	DQ54
5	DQS0	47	DQS8	88	DQ59	130	A3	171	DQ55
6	DQ2	48	A0	89	VSS	131	DQ30	172	VDDQ
7	VDD	49	CB2	90	NC	132	VSS	173	NC
8	DQ3	50	VSS	91	SDA	133	DQ31	174	DQ60
9	NC	51	CB3	92	SCL	134	CB4	175	DQ61
10	$\overline{\text{RESET}}$	52	BA1	93	VSS	135	CB5	176	VSS
11	VSS	KEY		94	DQ4	136	VDDQ	177	DM7
12	DQ8	53	DQ32	95	DQ5	137	CK0	178	DQ62
13	DQ9	54	VDDQ	96	VDDQ	138	/CK0	179	DQ63
14	DQS1	55	DQ33	97	DM0	139	VSS	180	VDDQ
15	VDDQ	56	DQS4	98	DQ6	140	DM8	181	SA0
16	NC	57	DQ34	99	DQ7	141	A10	182	SA1
17	NC	58	VSS	100	VSS	142	CB6	183	SA2
18	VSS	59	BA0	101	NC	143	VDDQ	184	VDDSPD
19	DQ10	60	DQ35	102	NC	144	CB7		
20	DQ11	61	DQ40	103	A13	KEY			
21	CKE0	62	VDDQ	104	VDDQ	145	VSS		
22	VDDQ	63	/WE	105	DQ12	146	DQ36		
23	DQ16	64	DQ41	106	DQ13	147	DQ37		
24	DQ17	65	/CAS	107	DM1	148	VDD		
25	DQS2	66	VSS	108	VDD	149	DM4		
26	VSS	67	DQS5	109	DQ14	150	DQ38		
27	A9	68	DQ42	110	DQ15	151	DQ39		
28	DQ28	69	DQ43	111	CKE1	152	VSS		
29	A7	70	VDD	112	VDDQ	153	DQ44		
30	VDDQ	71	NC	113	NC	154	/RAS		
31	DQ19	72	DQ48	114	DQ20	155	DQ45		
32	A5	73	DQ49	115	A12	156	VDDQ		
33	DQ24	74	VSS	116	VSS	157	/S0		
34	VSS	75	NC	117	DQ21	158	/S1		
35	DQ25	76	NC	118	A11	159	DM5		
36	DQS3	77	VDDQ	119	DM2	160	VSS		
37	A4	78	DQS6	120	VDD	161	DQ46		
38	VDD	79	DQ50	121	DQ22	162	DQ47		
39	DQ26	80	DQ51	122	A8	163	NC		
40	DQ27	81	VSS	123	DQ23	164	VDDQ		
41	A2	82	VDDID	124	VSS	165	DQ52		
42	VSS	83	DQ56	125	A6	166	DQ53		

NC: Not Connected

Block Diagram

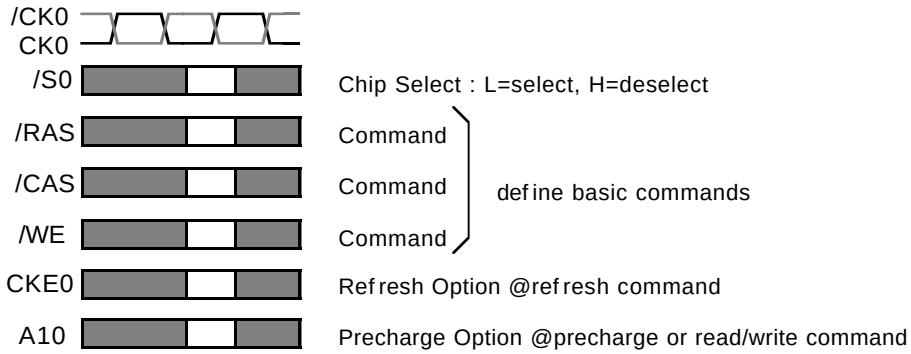


PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CK0,/CK0	Input	Clock: CK0 and /CK0 are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK0 and negative edge of /CK0. Output (read) data is referenced to the crossings of CK0 and /CK0 (both directions of crossing).
CKE0	Input	Clock Enable: CKE0 controls SDRAM internal clock. When CKE0 is low, the internal clock for the following cycle is ceased. CKE0 is also used to select auto / self refresh. After self refresh mode is started, CKE0 becomes asynchronous input. Self refresh is maintained as long as CKE0 is low.
/S0	Input	Physical Bank Select: When /S0 is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-9. A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks in SDRAM to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ 0-64 CB 0-7	Input / Output	Data Input/Output: Data bus
DQS0-8	Input / Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
DM0-8	Input	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.
Vddspd	Power Supply	Power Supply for SPD
Vref	Input	SSTL_2 reference voltage.
$\overline{\text{RESET}}$	Input	This signal is asynchronous and is driven low to the register in order to guarantee the register outputs are low.
SDA	Input / Output	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup.
SA0-2	Input	These signals are tied at the system planar to either VSS or VDD to configure the serial SPD EEPROM address range.
VDDID	——	VDD identification flag

BASIC FUNCTIONS

The MH16D72AKLB provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /S0 ,CKE0 and A10 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge,**READA**)

Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE0 =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE0 n-1	CKE0 n	/S	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11	note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X	
Precharge All Banks	PREA	H	X	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	H	V	
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X	1
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V	2

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A11 provide the op-code to be written to the selected Mode Register.

FUNCTION TRUTH TABLE

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
IDLE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA	
	L	L	H	L	BA, A10	PRE / PREA	NOP	4
	L	L	L	H	X	REFA	Auto-Refresh	5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set	5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	NOP	
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ (Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	Terminate Burst	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
WRITE (Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge	3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	PRECHARGE/ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	PRECHARGE/ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)	
	L	H	H	H	X	NOP	NOP (Idle after tRP)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	NOP (Idle after tRP)	4
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)	
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)	
	L	H	H	H	X	NOP	NOP (Idle after tRC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)	
	L	H	H	H	X	NOP	NOP (Idle after tRSC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries assume that CKE0 was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state o that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

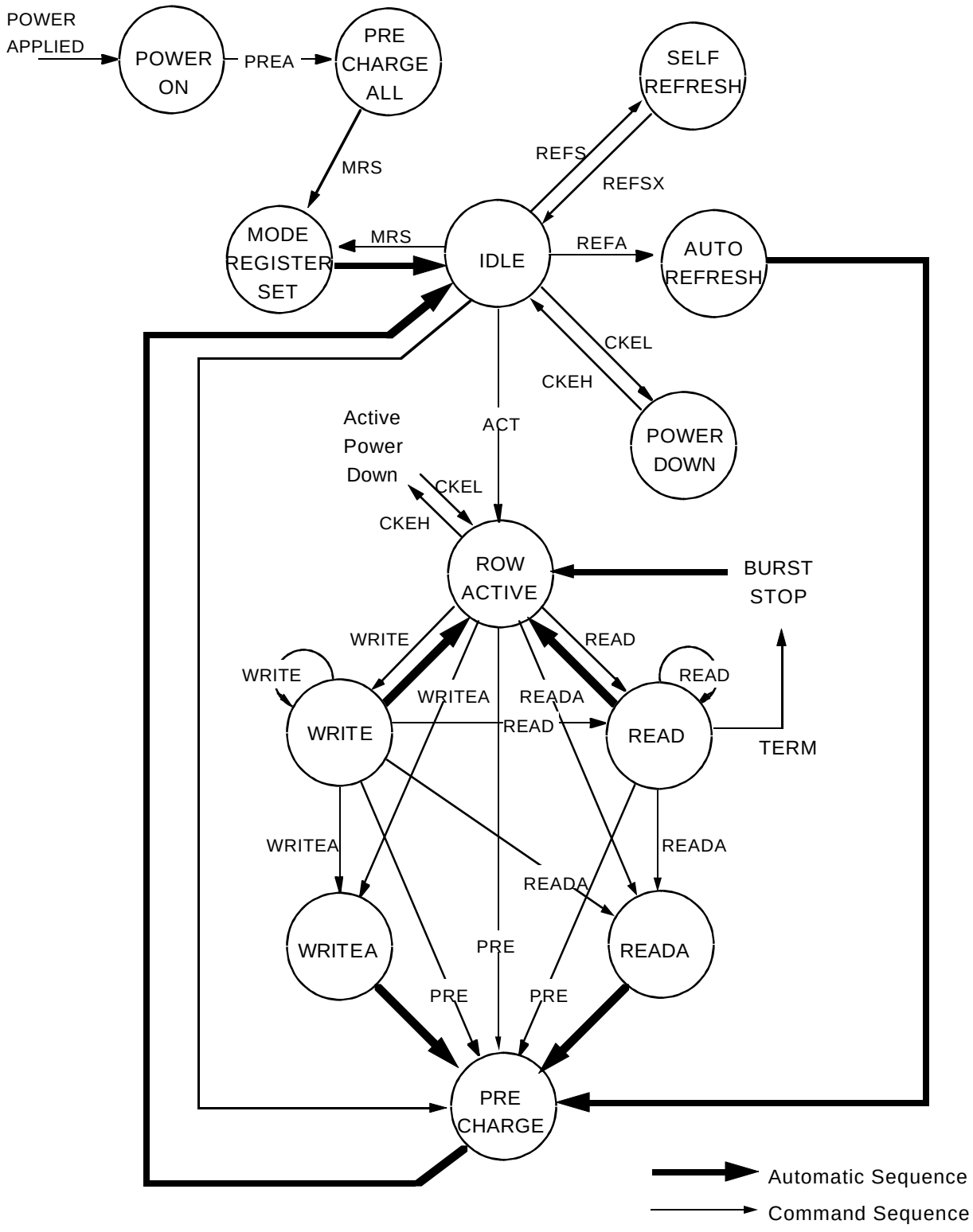
FUNCTION TRUTH TABLE for CKE

Current State	CKE0 n-1	CKE0 n	/S	/RAS	/CAS	/WE	Add	Action	Notes
SELF-REFRESH	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)	1
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	L	X	X	ILLEGAL	1
	L	H	L	L	X	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	1
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down to Idle	
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2
	H	L	L	L	L	H	X	Enter Self-Refresh	2
	H	L	H	X	X	X	X	Enter Power Down	2
	H	L	L	H	H	H	X	Enter Power Down	2
	H	L	L	H	H	L	X	ILLEGAL	2
	H	L	L	H	L	X	X	ILLEGAL	2
	H	L	L	L	X	X	X	ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Current State =Power Down	2
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle	3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle	3
	L	L	X	X	X	X	X	Maintain CLK Suspend	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE0 Low to High transition will re-enable CK0 and other inputs **asynchronously**
. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

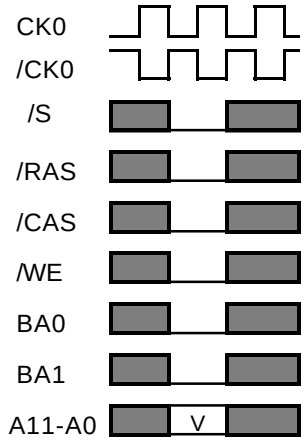
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or multifunctioning.

1. Apply VDD before or the same time as VDDQ
2. Apply VDDQ before or at the same time as VTT & Vref
3. Maintain stable condition for 200us after stable power and CLK, apply NOP or DSEL
4. Issue precharge command for all banks of the device
5. Issue EMRS
6. Issue MRS for Mode Register and to reset the DLL
7. Issue 2 or more Auto Refresh commands
8. Maintain stable condition for 200 cycle

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when all banks in discrete in idle state. After tMRD from a MRS command, the DDR DIMM is ready for new command.



BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	DR	0	LTMODE			BT	BL		

	CL	/CAS Latency
Latency Mode	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	R
	1 0 0	R
	1 0 1	R
	1 1 0	2.5
	1 1 1	R

	BL	BT= 0	BT= 1
Burst Length	0 0 0	R	R
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	R	R

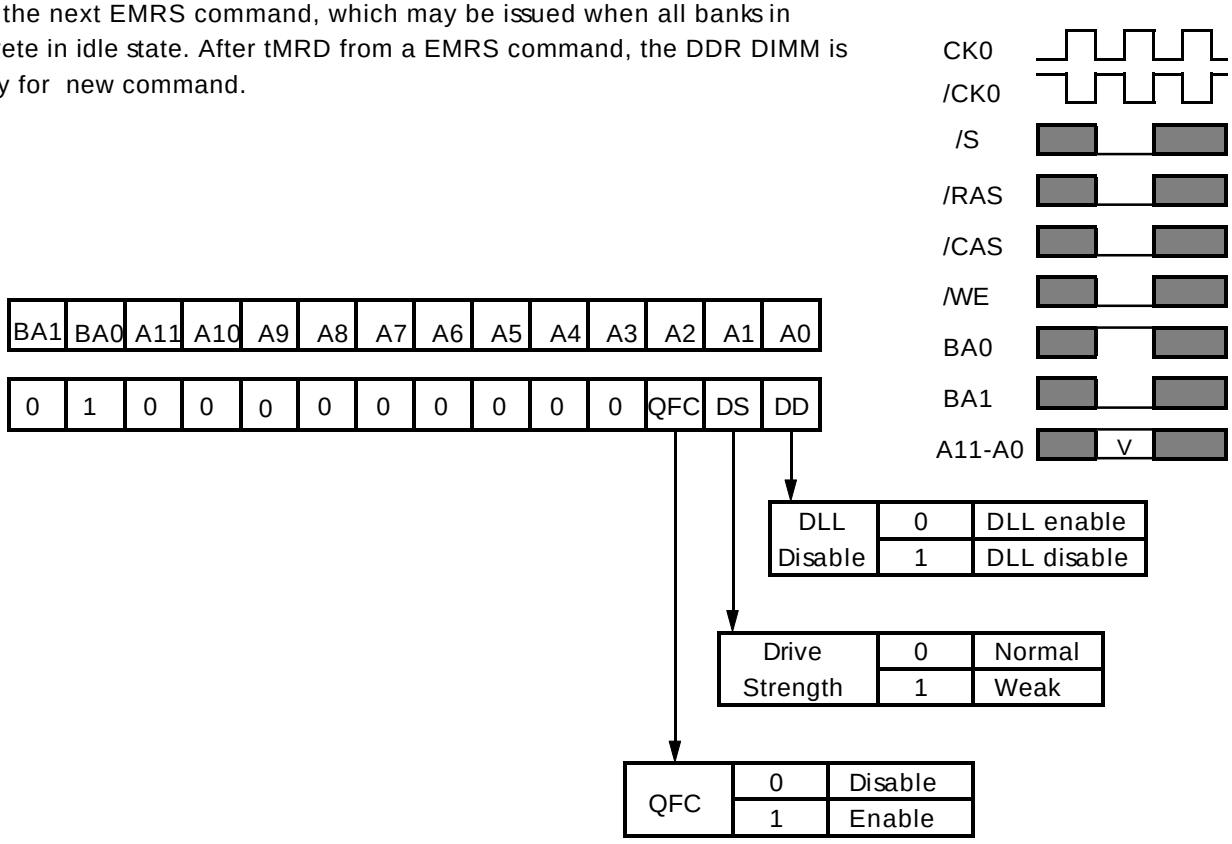
Burst Type	0	Sequential
	1	Interleaved

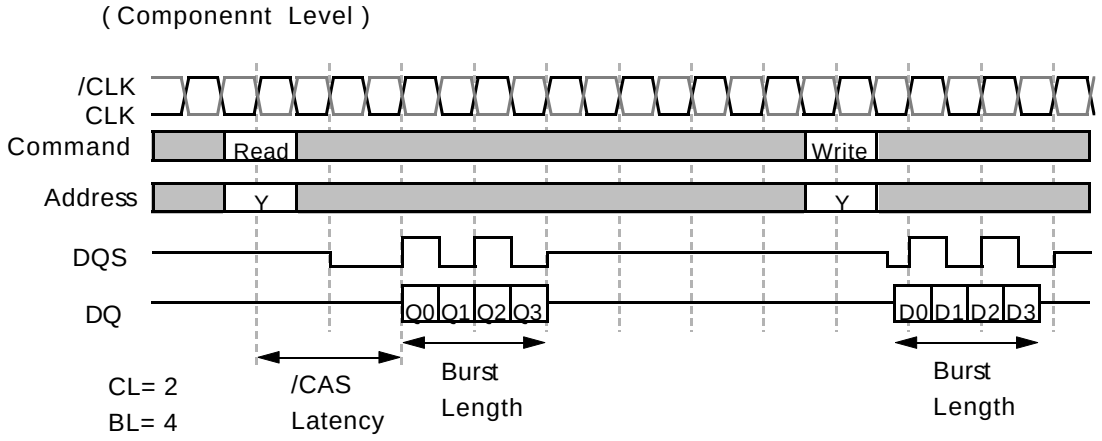
DLL Reset	0	NO
	1	YES

R: Reserved for Future Use

EXTENDED MODE REGISTER

DLL disable / enable mode can be programmed by setting the extended mode register (EMRS). The extended mode register stores these data until the next EMRS command, which may be issued when all banks in discrete in idle state. After tMRD from a EMRS command, the DDR DIMM is ready for new command.





Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 3.7	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 ~ 3.7	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to VssQ	-0.5 ~ VddQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 C	10	W
Topr	Operating Temperature		0 ~ 70	C
Tstg	Storage Temperature		-45 ~ 100	C

DC OPERATING CONDITIONS

(Ta=0 ~ 70℃ , unless otherwise noted)

Symbol	Parameter	Limits			Unit	Notes
		Min.	Typ.	Max.		
Vdd	Supply Voltage	2.3	2.5	2.7	V	
VddQ	Supply Voltage for Output	2.3	2.5	2.7	V	
Vref	Input Reference Voltage	1.15	1.25	1.35	V	5
VIH(DC)	High-Level Input Voltage	Vref + 0.18		VddQ+0.3	V	
VIL(DC)	Low-Level Input Voltage	-0.3		Vref - 0.18	V	
VIN(DC)	Input Voltage Level, CK0 and /CK0	-0.3		VddQ + 0.3	V	
VID(DC)	Input Differential Voltage, CK0 and /CK0	0.36		VddQ + 0.6	V	7
VTT	I/O Termination Voltage	Vref - 0.04		Vref + 0.04	V	6

CAPACITANCE

(Ta=0 ~ 70℃, Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits(max.)	Unit	Notes
CI(A)	Input Capacitance, address pin	VI - 1.25V f=100MHz VI = 25mVrm	8.0	pF	11
CI(C)	Input Capacitance, control pin		8.0	pF	11
CI(K)	Input Capacitance, CK0 pin		15.3	pF	11
CI/O	Input Capacitance, I/O pin		13.3	pF	11

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/Test Conditions	Limits(max)		Unit	Notes
		-75	-10		
IDD0	OPERATING CURRENT: One Bank; Active-Precharge; t RC = t RC MIN; t CK = t CK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1390	1273	mA	
IDD1	OPERATING CURRENT: One Bank; Active-Read-Precharge; Burst = 2; t RC = t RC MIN; CL = 2.5; t CK = t CK MIN; IOUT= 0 mA;Address and control inputs changing once per clock cycle	1435	1318	mA	
IDD2P	PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; CKE≦ VIL (MAX); t CK = t CK MIN	580	508	mA	
IDD2N	IDLE STANDBY CURRENT: /CS > VIH (MIN); All banks idle; CKE > VIH (MIN); t CK = t CK MIN; Address and other control inputs changing once per clock cycle	760	688	mA	
IDD3P	ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; CKE≦ VIL (MAX); t CK = t CK MIN	760	688	mA	
IDD3N	ACTIVE STANDBY CURRENT: /CS > VIH (MIN); CKE > VIH (MIN); One bank; Active-Precharge; t RC = t RAS MAX; t CK = t CK MIN; DQ,DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	985	868	mA	
IDD4R	OPERATING CURRENT: Burst = 2; Reads; Continuous burst;One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; t CK = t CK MIN; IOUT = 0 mA	1930	1768	mA	
IDD4W	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; t CK = t CK MIN; DQ, DM and DQS inputs changing twice per clock cycle	1885	1723	mA	
IDD5	AUTO REFRESH CURRENT: t RC = t RFC (MIN)	2110	1948	mA	
IDD6	SELF REFRESH CURRENT: CKE≦ 0.2V	427	355	mA	9

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 ~ 70°C , Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter/Test Conditions	Limits		Unit	Notes
		Min.	Max.		
VIH(AC)	High-Level Input Voltage (AC)	Vref + 0.35		V	
VIL(AC)	Low-Level Input Voltage (AC)		Vref - 0.35	V	
VID(AC)	Input Differential Voltage, CLK and /CLK	0.7	$V_{DD}Q$ + 0.6	V	7
VIX(AC)	Input Crossing Point Voltage, CLK and /CLK	0.5*$V_{DD}Q$-0.2	0.5*$V_{DD}Q$+0.2	V	8
IOZ	Off-state Output Current /Q floating Vo=0~$V_{DD}Q$	-5	5	µA	
Ii	Input Current / VIN=0 ~ VddQ	-2	2	µA	

AC TIMING REQUIREMENTS (Component Level)

(Ta=0 ~ 70 °C, Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

	AC Characteristics		-75		-10			
Symbol	Parameter		Min.	Max.	Min.	Max.	Unit	Notes
tAC	DQ Output Valid data delay time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	
tDQSCK	DQ Output Valid data delay time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	
tCH	CLK High level width		0.45	0.55	0.45	0.55	tCK	
tCL	CLK Low level width		0.45	0.55	0.45	0.55	tCK	
tHP	CLK half period		min(tCL, tCH		min(tCL, tCH		ns	20
tCK	CLK cycle time	CL=2.5	7.5	15	8	15	ns	
		CL=2	10	15	10	15	ns	
tDH	Input Setup time (DQ,DM)		0.5		0.6		ns	
tDS	Input Hold time(DQ,DM)		0.5		0.6		ns	
tDIPW	DQ and DM input pulse width (for each input)		1.75		2		ns	
tHZ	Data-out-high impedance time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	14
tLZ	Data-out-low impedance time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	14
tDQSQ	DQS-DQ Skew(for DQS and associated DQ signals)			+0.5		+0.6	ns	
tDQSQA	DQS-DQ Skew(for DQS and all DQ signals)			+0.5		+0.6	ns	
tDV	DQ and DQS data Valid window		0.35		0.35		tCK	
tQH	DQ/DQS output hold time from DQS		tHP-0.75		tHP-1.0		ns	
tDQSS	Write command to first DQS latching transition		0.75	1.25	0.75	1.25	tCK	
tDQSH	DQS input High level width		0.35		0.35		tCK	
tDQSL	DQS input Low level width		0.35		0.35		tCK	
tDSS	DQS falling edge to CLK setup time		0.2		0.2		tCK	
tDSH	DQS falling edge hold time from CLK		0.2		0.2		tCK	
tMRD	Mode Register Set command cycle time		15		15		ns	
tWPRES	Write preamble setup time		0		0		ns	16
tWPST	Write postamble		0.4	0.6	0.4	0.6	tCK	15
tWPRE	Write preamble		0.25		0.25		tCK	
tIS	Input Setup time (address and control)		0.9		1.2		ns	19
tIH	Input Hold time (address and control)		0.9		1.2		ns	19
tRPST	Read postamble		0.4	0.6	0.4	0.6	tCK	
tRPRE	Read preamble		0.9	1.1	0.9	1.1	tCK	

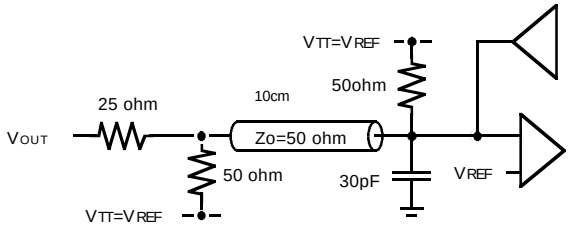
AC TIMING REQUIREMENTS(Continues)

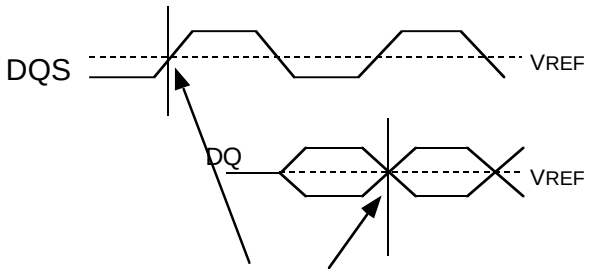
(Ta=0 ~ 70 °C , Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

	AC Characteristics	-75		-10			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	Notes
tRAS	Row Active time	45	120,000	50	120,000	ns	
tRC	Row Cycle time(operation)	65		70		ns	
tRFC	Auto Ref. to Active/Auto Ref. command period	75		80		ns	
tRCD	Row to Column Delay	20		20		ns	
tRP	Row Precharge time	20		20		ns	
tRRD	Act to Act Delay time	15		15		ns	
tWR	Write Recovery time	15		15		ns	
tDAL	Auto Precharge write recovery + precharge time	35		35		ns	
tWTR	Internal Write to Read Command Delay	1		1		tCK	
tXSNR	Exit Self Ref. to non-Read command	75		80		ns	
tXSRD	Exit Self Ref. to -Read command	200		200		tCK	
tXPNR	Exit Power down to command	1		1		tCK	
tXPRD	Exit Power down to -Read command	1		1		tCK	18
tREFI	Average Periodic Refresh interval	15.6		15.6		us	17

Output Load Condition

(for component measurement)





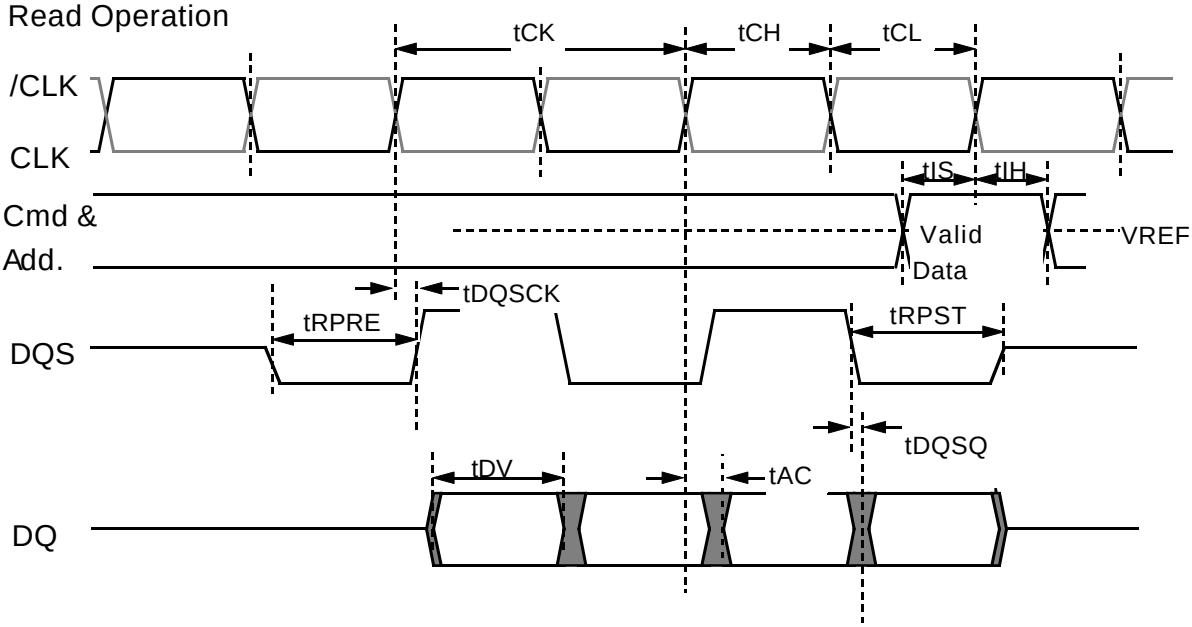
Output Timing Measurement Reference Point

Notes

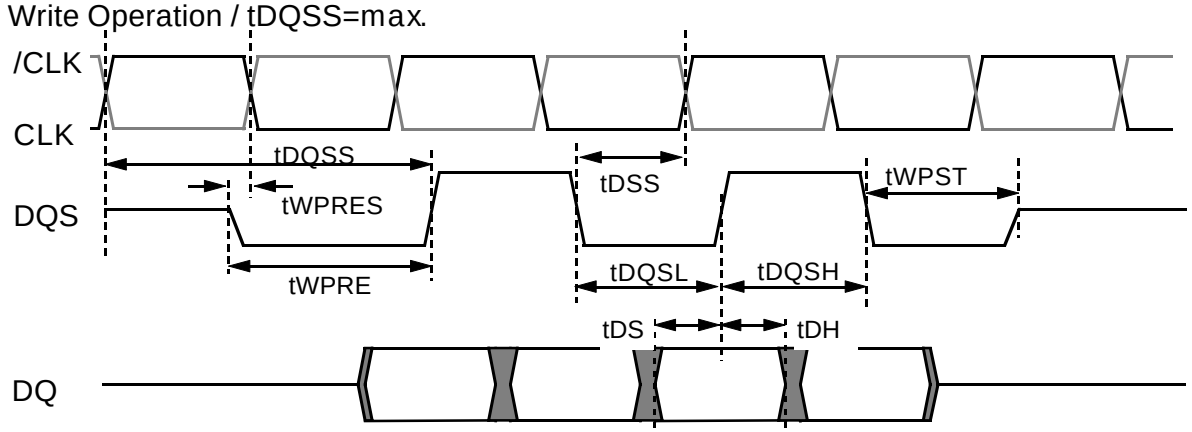
1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specification are tested after the device is properly initialized.
11. This parameter is sampled. VddQ = +2.5V+/-0.2V, Vdd = +2.5V+/-0.2V, f =100MHz, Ta = 25 °C , VOUT(DC)= VddQ/2, VOUT(PEAK TO PEAK) = 25mV, DM inputs are grouped with I/O pins - reflecting the fact that they are matched in laoding (to faciliate trace matching at the board level).
12. The CLK//CLK input reference level (for signals other than CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilized. Exception: during the period before VREF stabilizes, CKE=< 0.3VddQ is recognized as LOW.
14. t HZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.
19. For command/address and CLK & /CLK slew rate ≥1.0V/ns.
20. Min(tCL, tCH)refers to the smaller of the actual clock low time and the actualclock high time as provided to the device.

(Component Level)

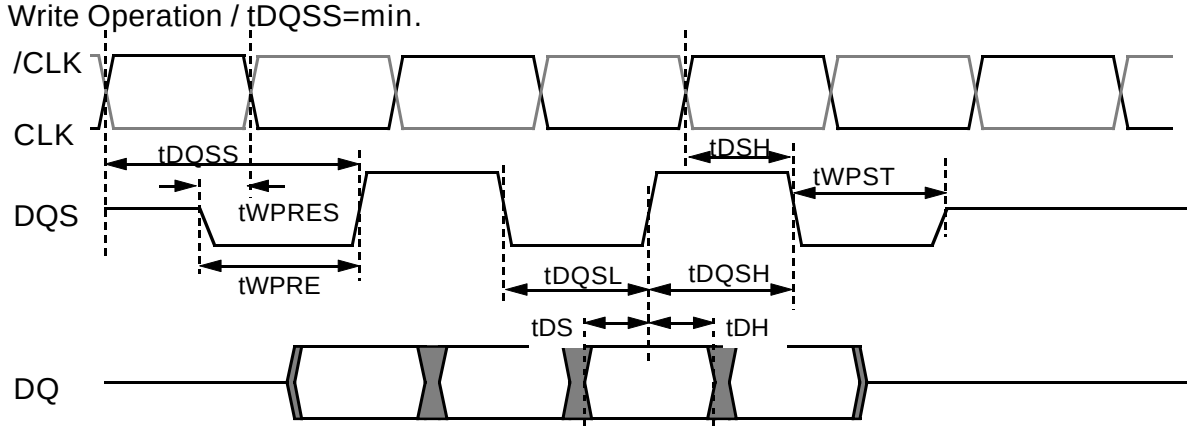
Read Operation



Write Operation / tDQSS=max.



Write Operation / tDQSS=min.



OPERATIONAL DESCRIPTION

BANK ACTIVATE

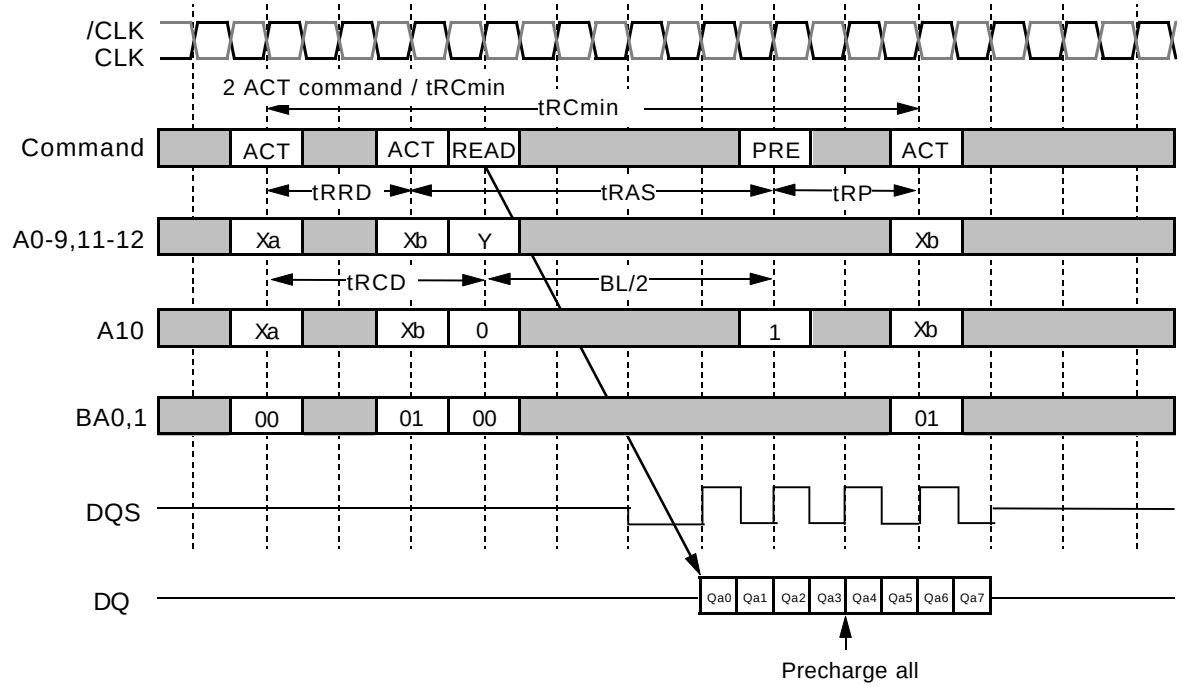
The DDR SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row address A11-0. The minimum activation interval between one bank and the other bank is tRRD. Maximum 2 ACT commands are allowed within tRC,although the number of banks which are active concurrently is not limited.

PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA,PRE+A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

Bank Activation and Precharge All (BL=8, CL=2 (Discrete level))

Module input and output timing.



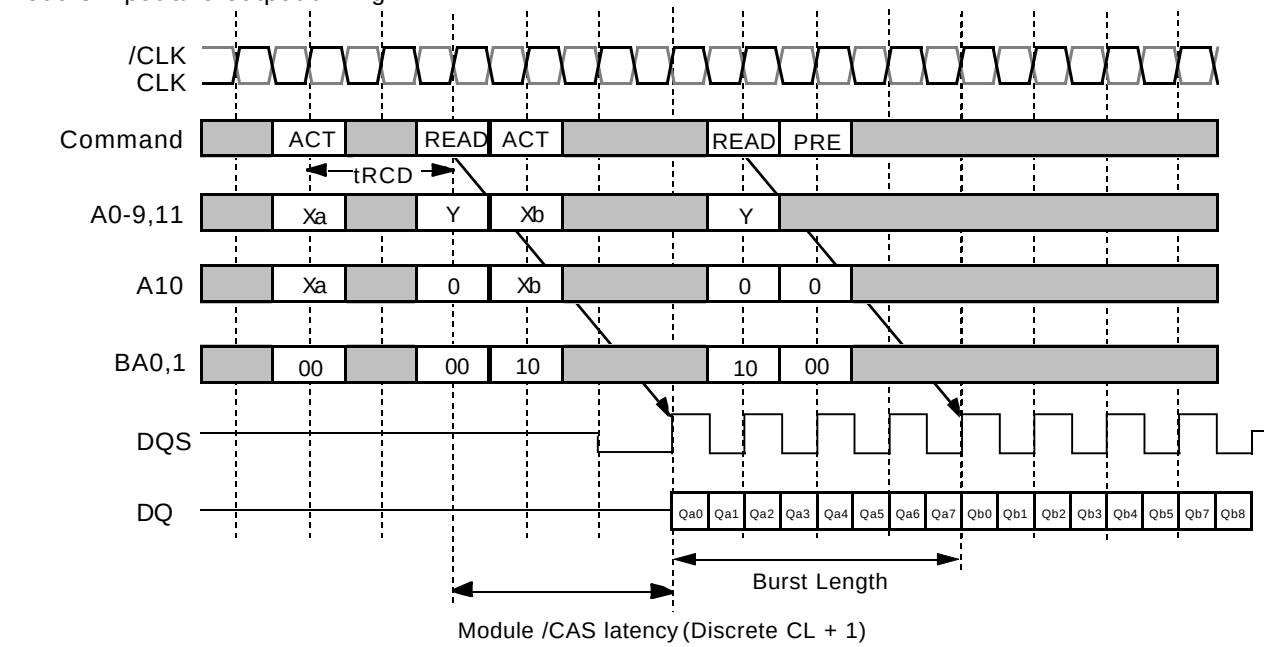
A precharge command can be issued at BL/2(Discrete) from a read command without data loss.

READ

After tRCD from the bank activation, a READ command can be issued. 1st Output data is available after the /CAS Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A11,A9-A0, and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge(READA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL/2 after READA. The next ACT command can be issued after (BL/2+tRP) from the previous READA.

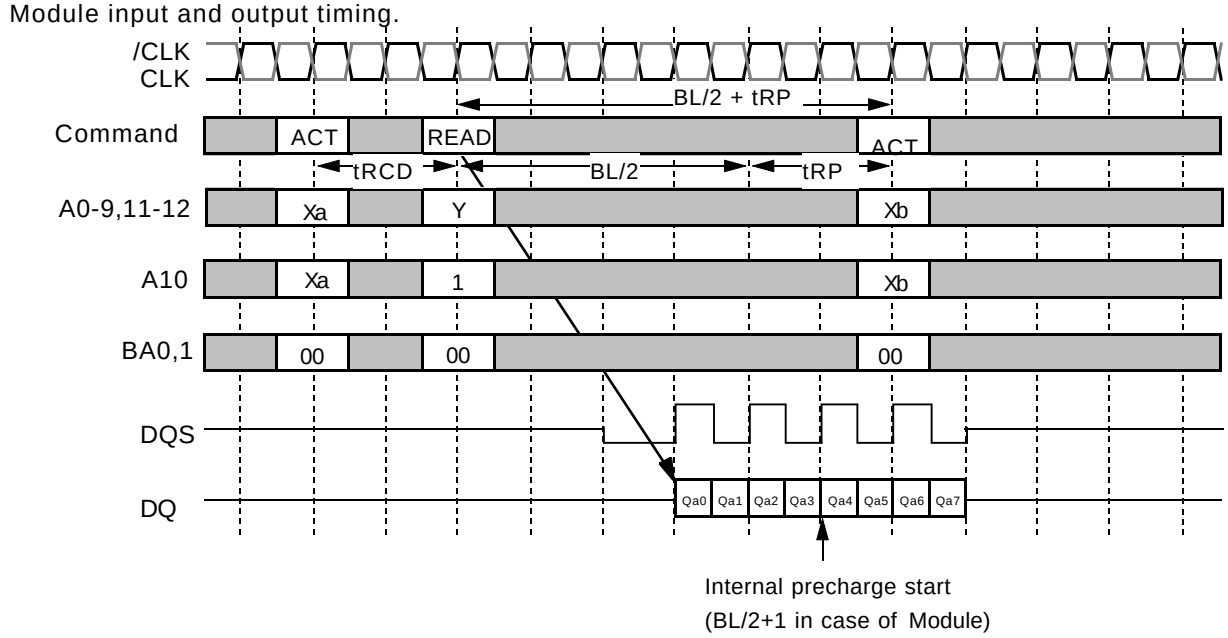
Multi Bank Interleaving READ (BL=8, CL=2(Discrete level))

Module input and output timing.



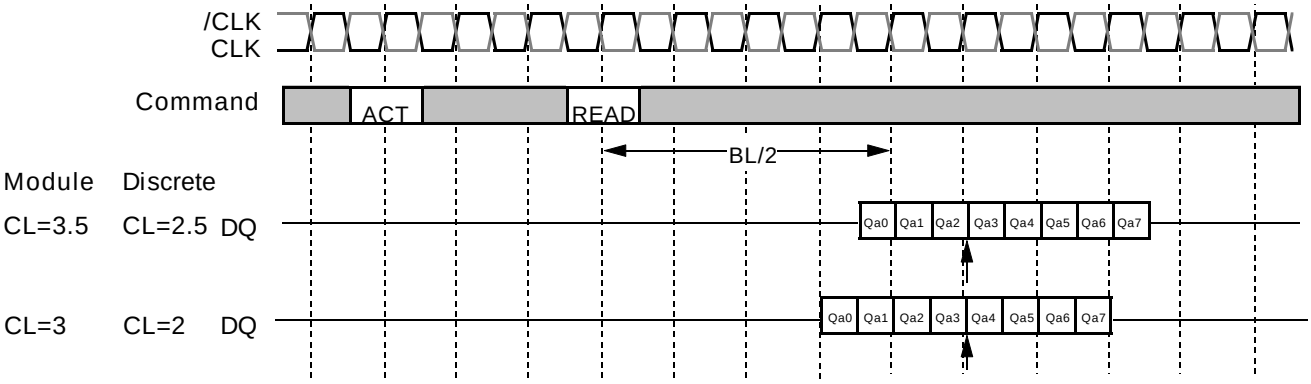
READ with Auto-Precharge (BL=8, CL=2(Discrete))

Module input and output timing.



READ Auto-Precharge Timing (BL=8)

Module input and output timing.

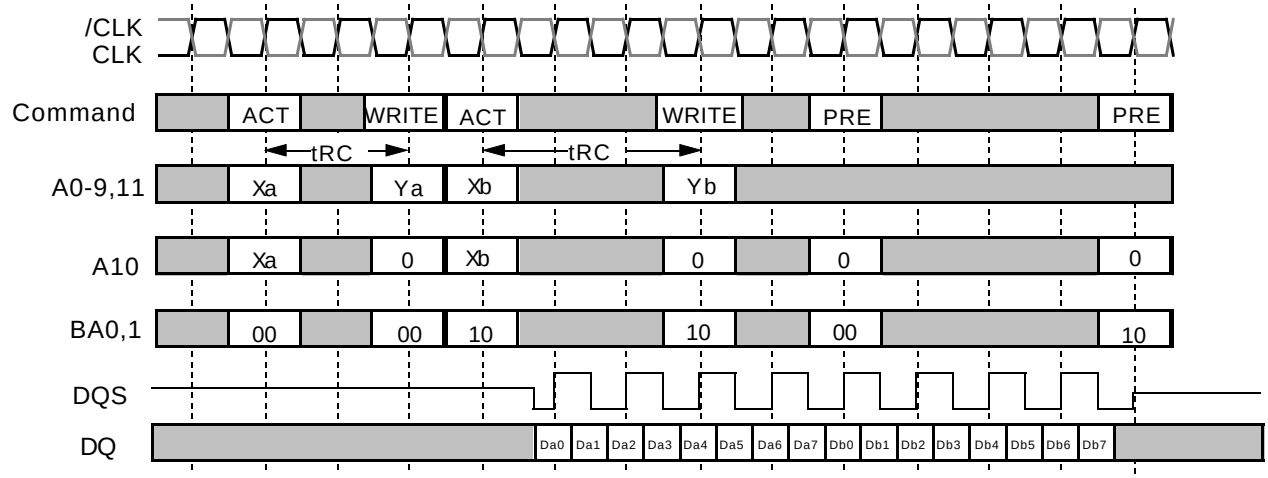


Internal Precharge Start Timing
(In case of module, Precharge start at BL/2+1)

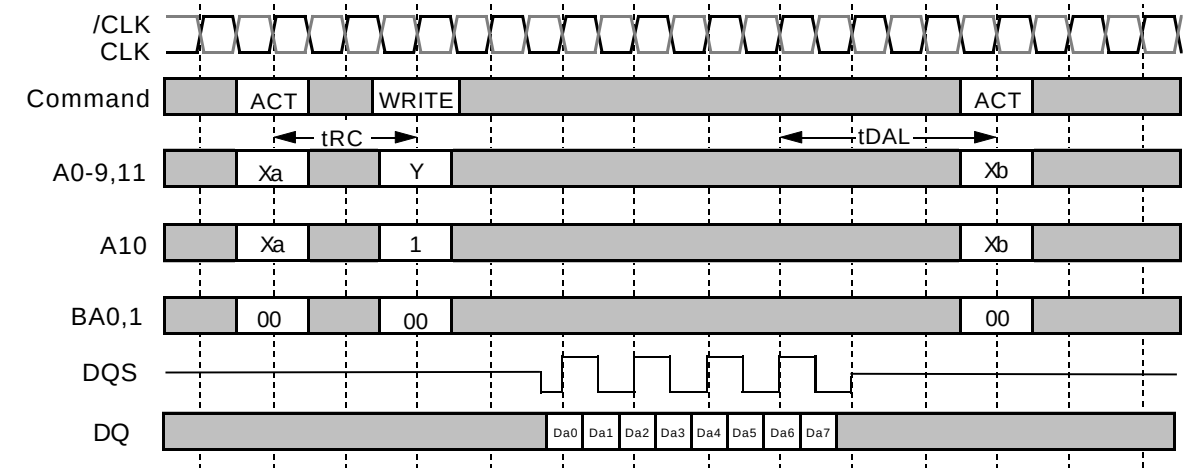
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set from the WRITE command with data strobe input, following (BL-1) data are written into RAM, when the Burst Length is BL. The start address is specified by A11,A9-A0, and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last data to the PRE command, the write recovery time (tWRP) is required. When A10 is high at a WRITE command, the auto-precharge(WRITEA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The next ACT command can be issued after tDAL from the last input data cycle.

Module input and output timing. **Multi Bank Interleaving WRITE (BL=8)**



Module input and output timing. **WRITE with Auto-Precharge (BL=8)**

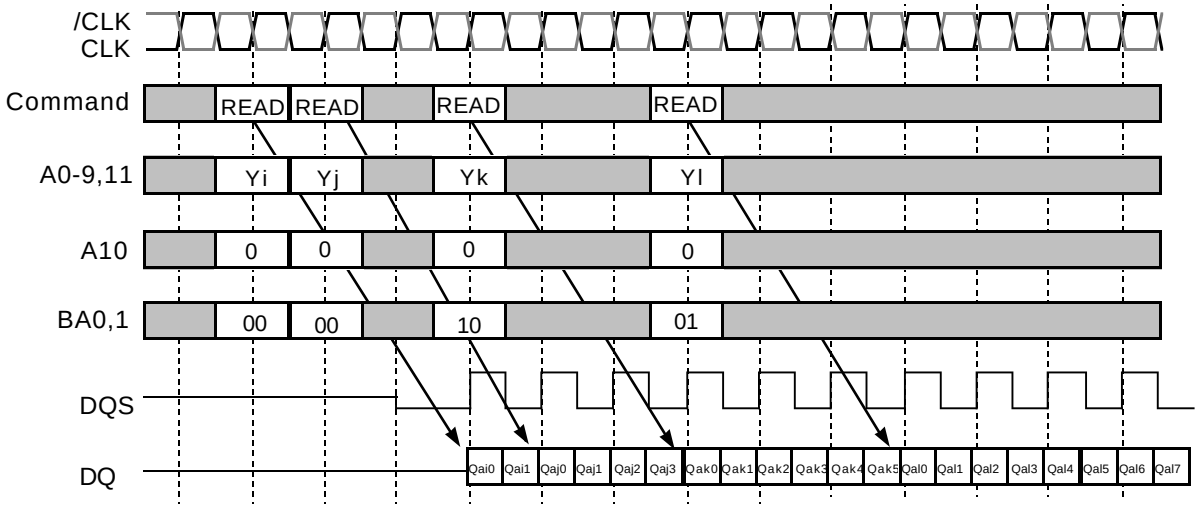


BURST INTERRUPTION
[Read Interrupted by Read]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1CLK.

Module input and output timing.

Read Interrupted by Read (BL=8, CL=2(Discrete))

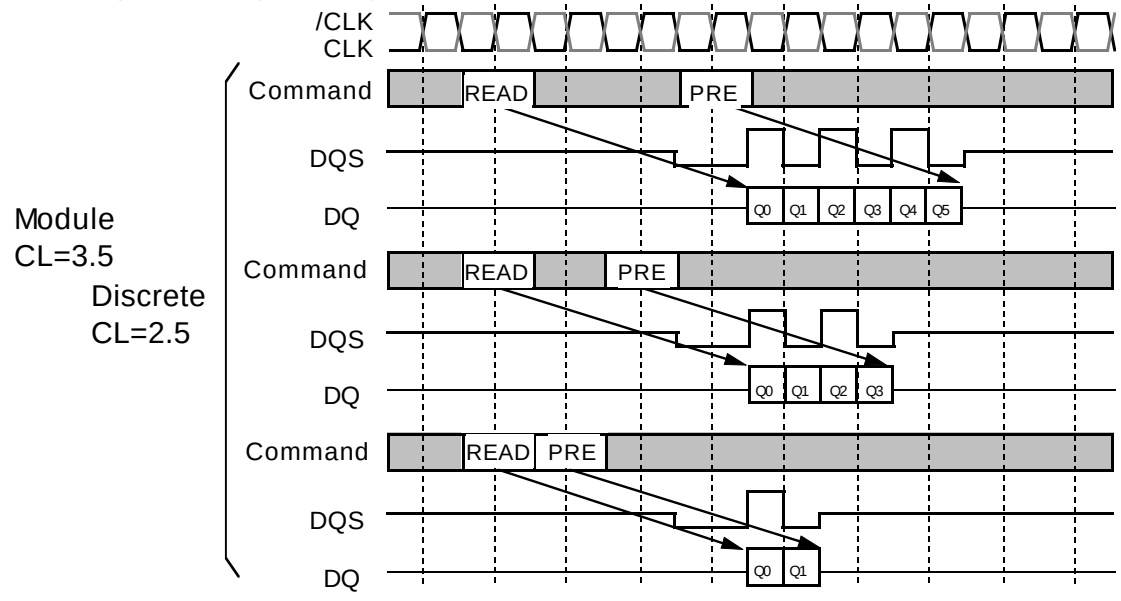


[Read Interrupted by precharge]

Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=8.

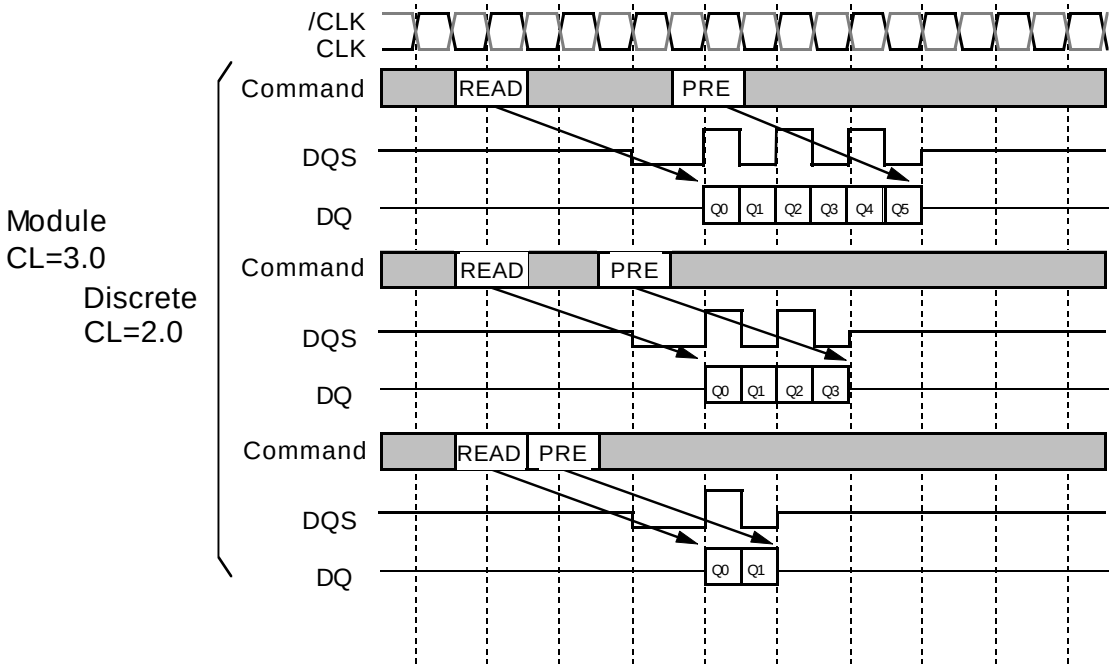
Read Interrupted by Precharge (BL=8)

Module input and output timing.



Read Interrupted by Precharge (BL=8)

Module input and output timing.

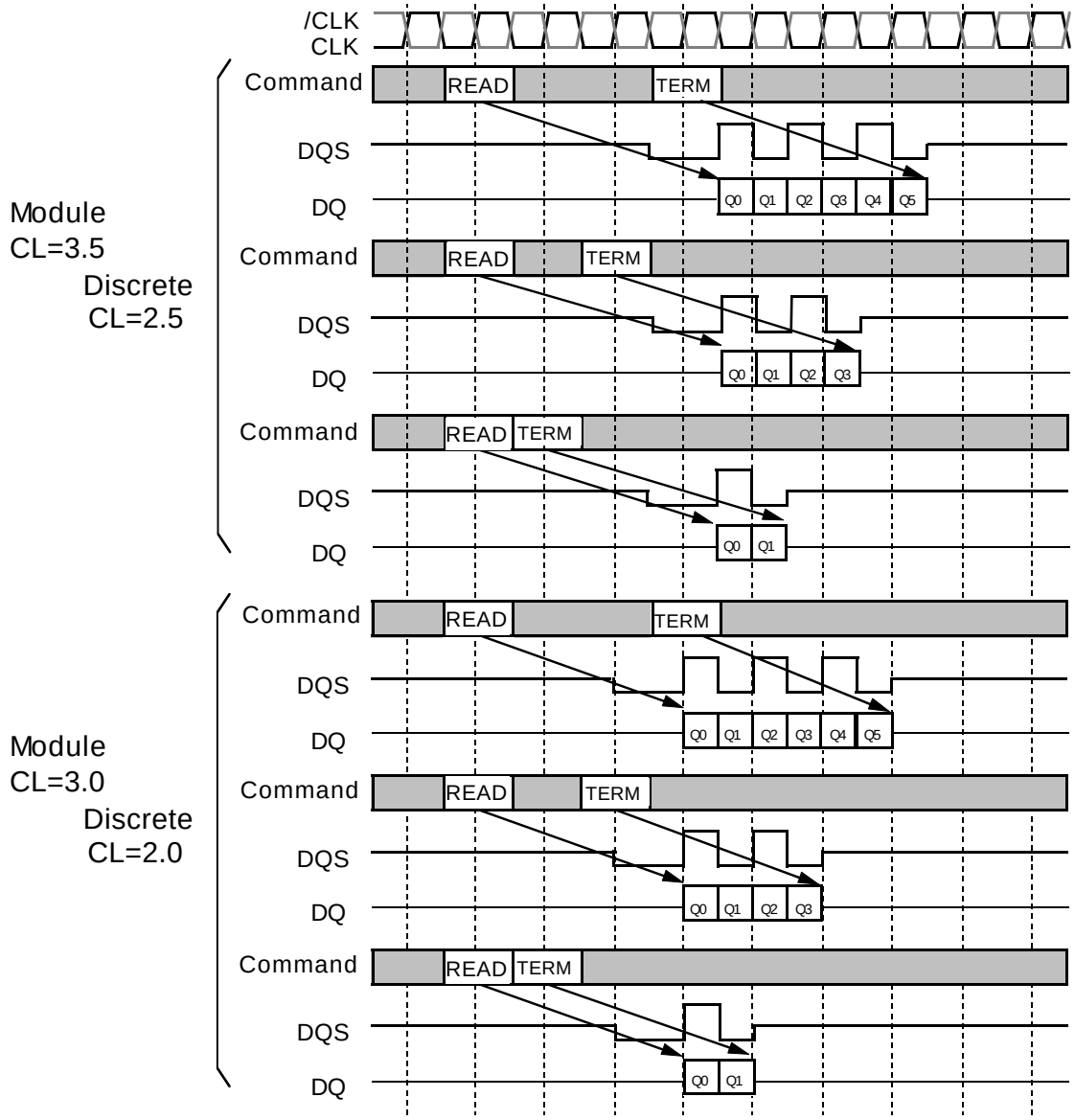


[Read Interrupted by Burst Stop]

Burst read operation can be interrupted by a burst stop command(TERM). READ to TERM interval is minimum 1 CLK. A TERM command to output disable latency is equivalent to the /CAS Latency. As a result, READ to TERM interval determines valid data length to be output. The figure below shows examples of BL=8.

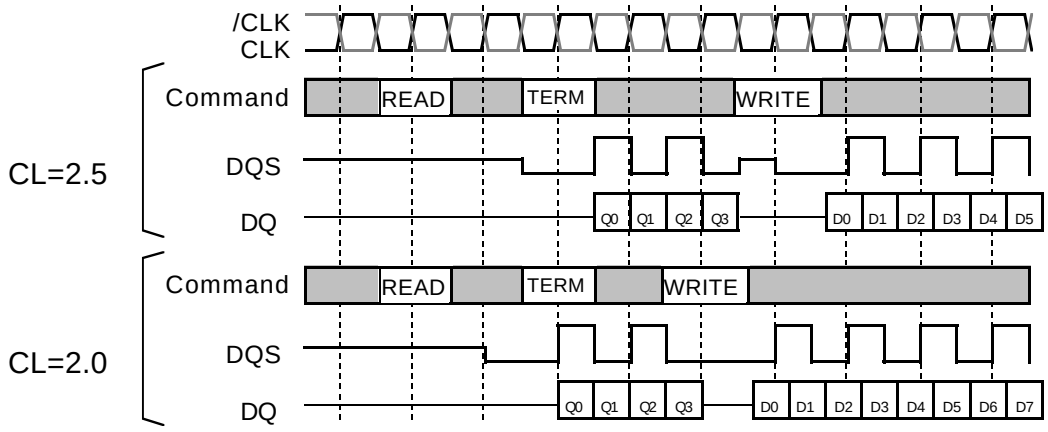
Read Interrupted by TERM (BL=8)

Module input and output timing.



[Read Interrupted by Write with TERM]

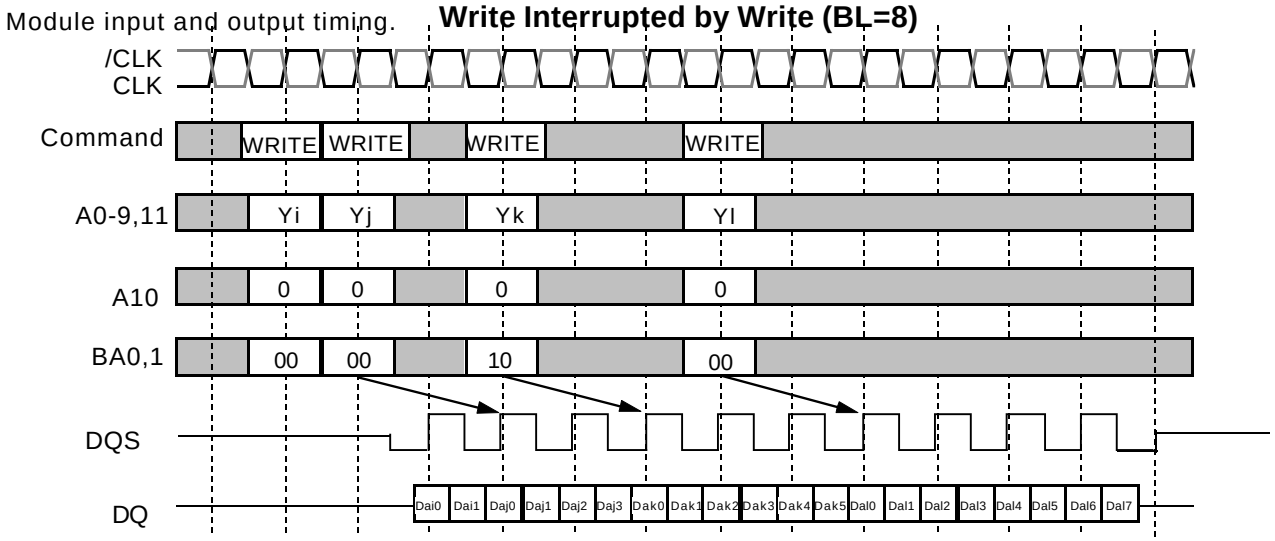
Read Interrupted by TERM (BL=8)



[Write interrupted by Write]

Burst write operation can be interrupted by write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

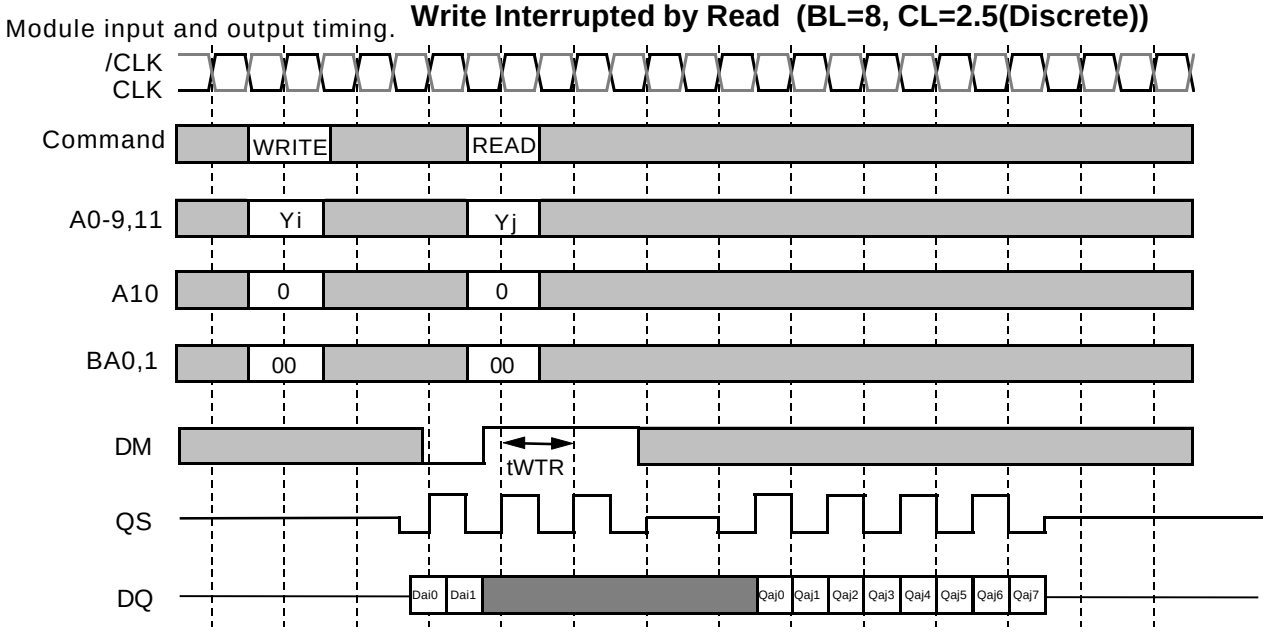
Module input and output timing.



[Write interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. Internal WRITE to READ command interval(tWTR) is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care". tWTR is referenced from the first positive edge after the last data input.

Module input and output timing.

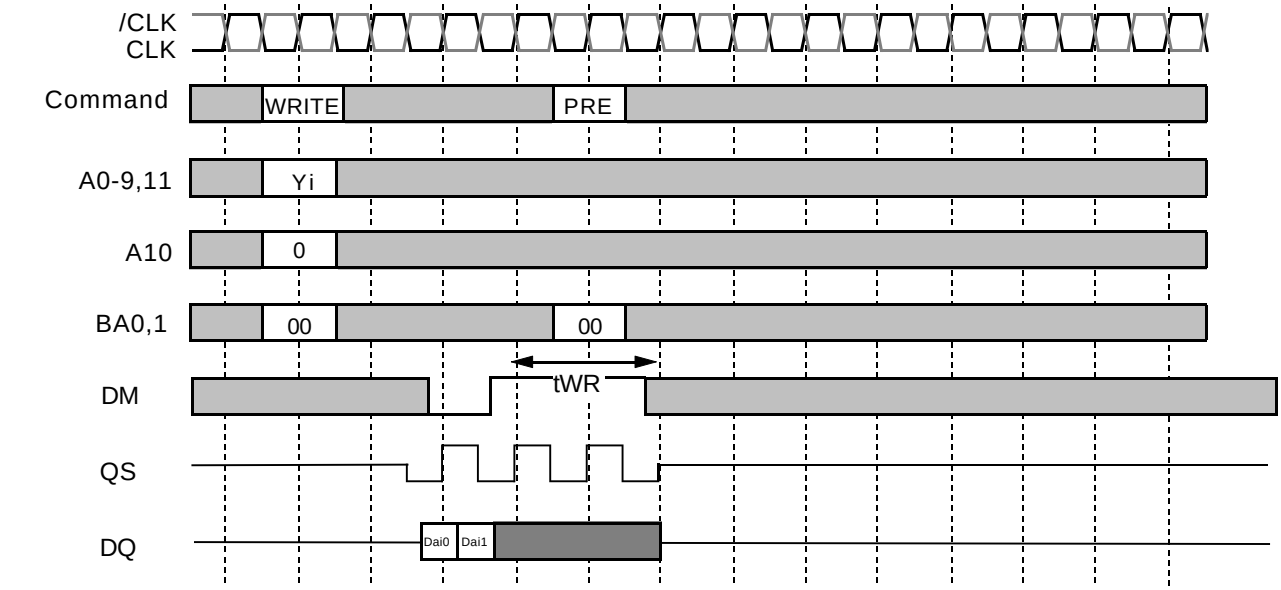


[Write interrupted by Precharge]

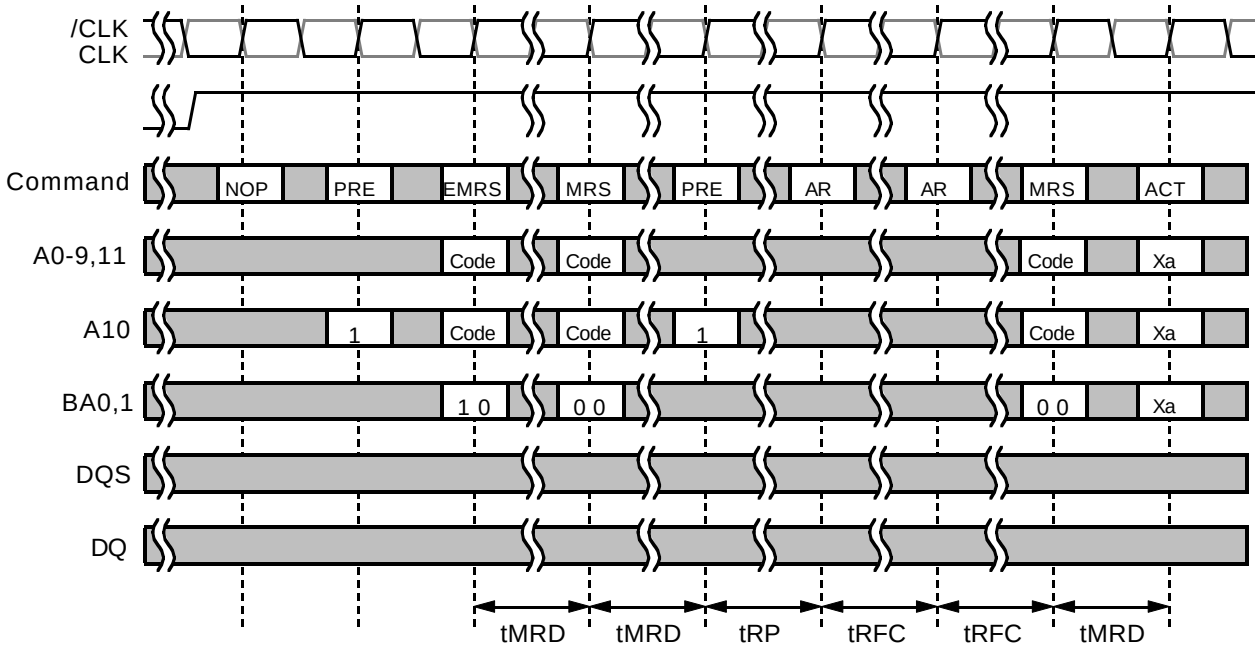
Burst write operation can be interrupted by precharge of the same or all bank. Random column access is allowed. tWR is referenced from the first positive CLK edge after the last data input.

Write Interrupted by Precharge (BL=8, CL=2.5)

Module input and output timing.

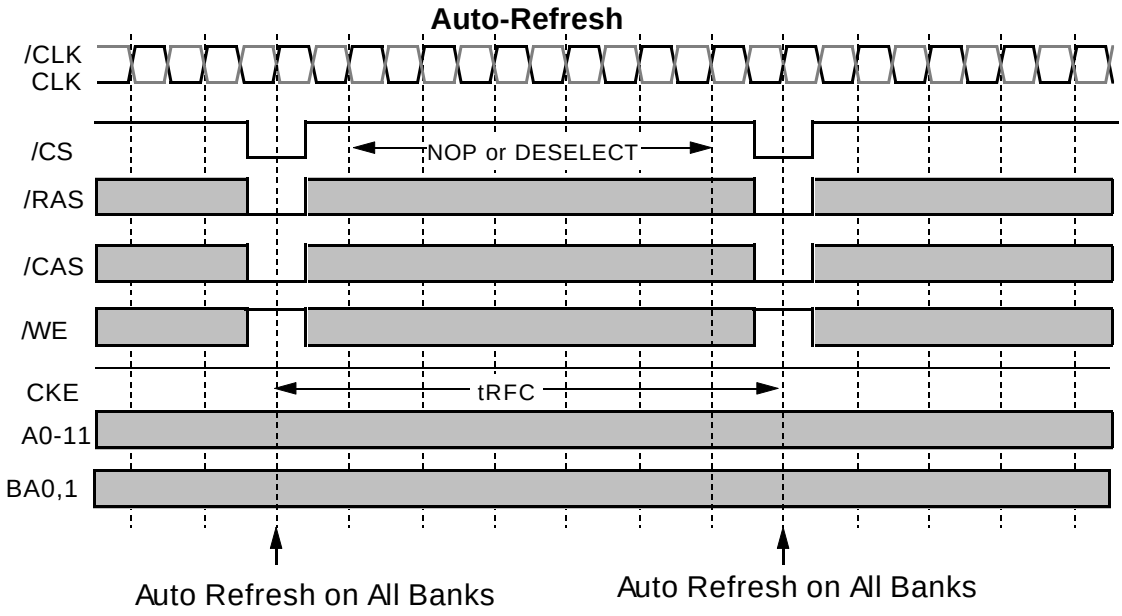


[Initialize and Mode Register sets]



[AUTO REFRESH]

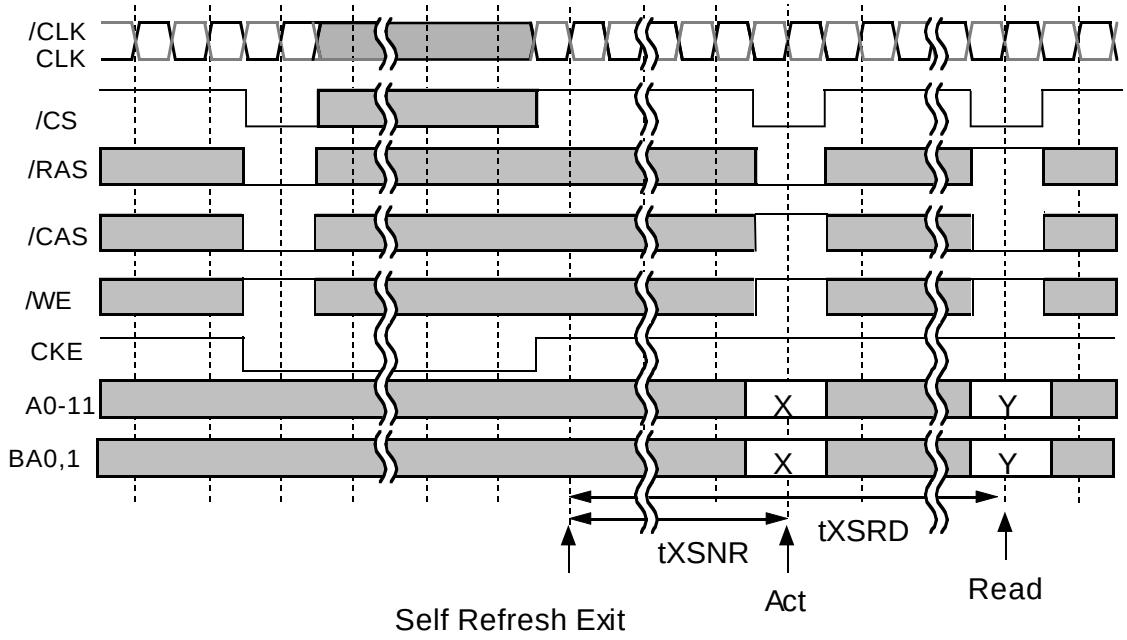
Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L,/WE=CKE=H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 128M bits memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC . Any command must not be supplied to the device before tRFC from the REFA command.



[SELF REFRESH]

Self -refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L,/WE=H,CKE=L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/tXSRD.

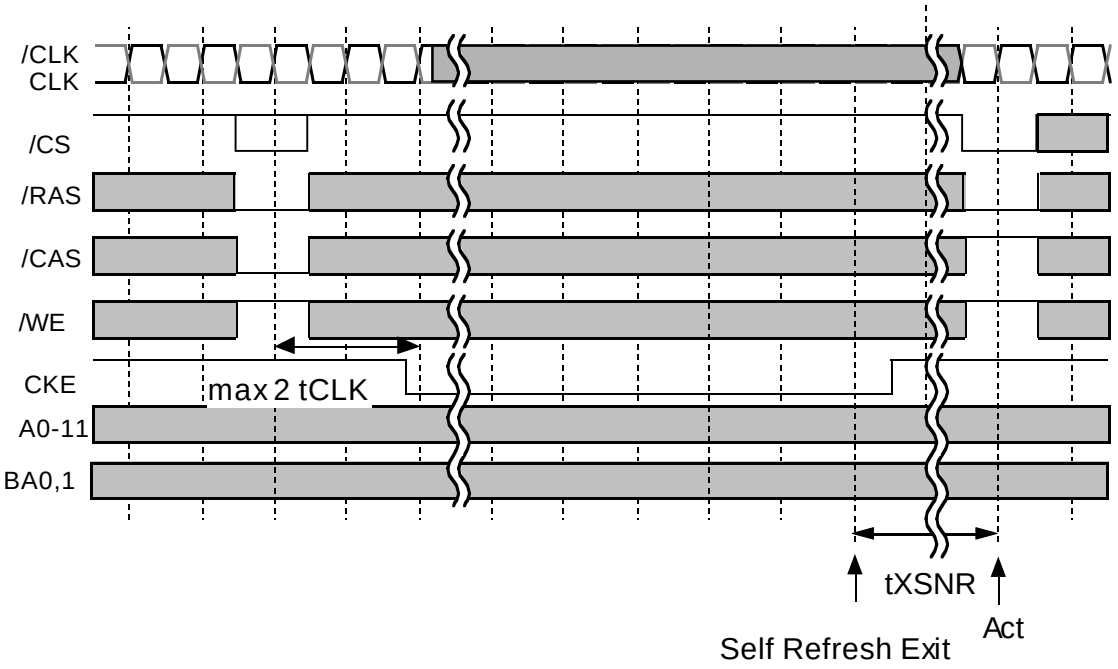
Self-Refresh



[Asynchronous SELF REFRESH]

Asynchronous Self -refresh mode is entered by CKE=L within 2 tCLK after issuing a REFA command (/CS=/RAS=/CAS=L,/WE=H). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/tXSRD.

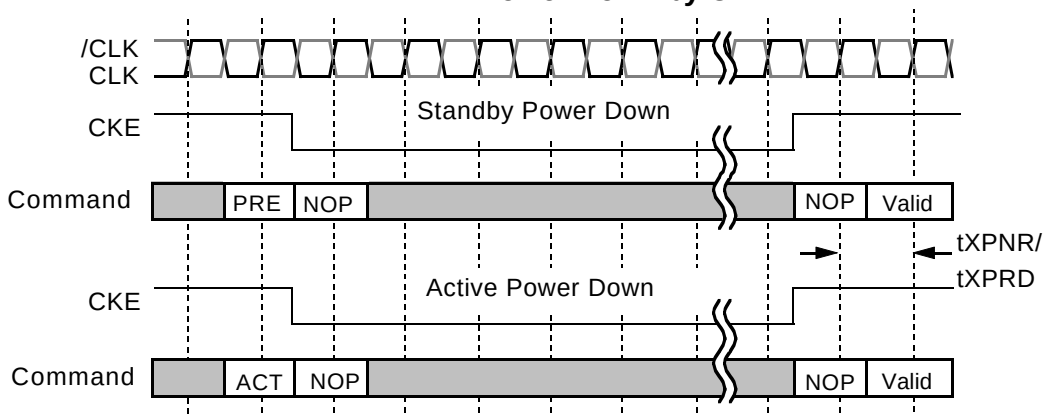
Asynchronous Self-Refresh



[Power DOWN]

The purpose of CLK suspend is power down. CKE is synchronous input except during the self-refresh mode. A command at cycle is ignored. From CKE=H to normal function, DLL recovery time is NOT required in the condition of the stable CLK operation during the power down mode.

Power Down by CKE

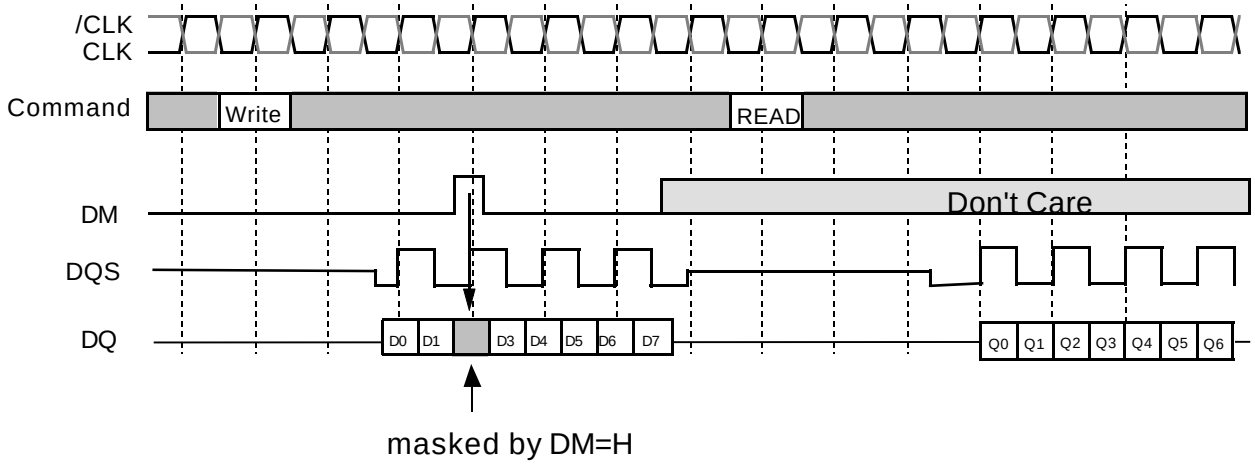


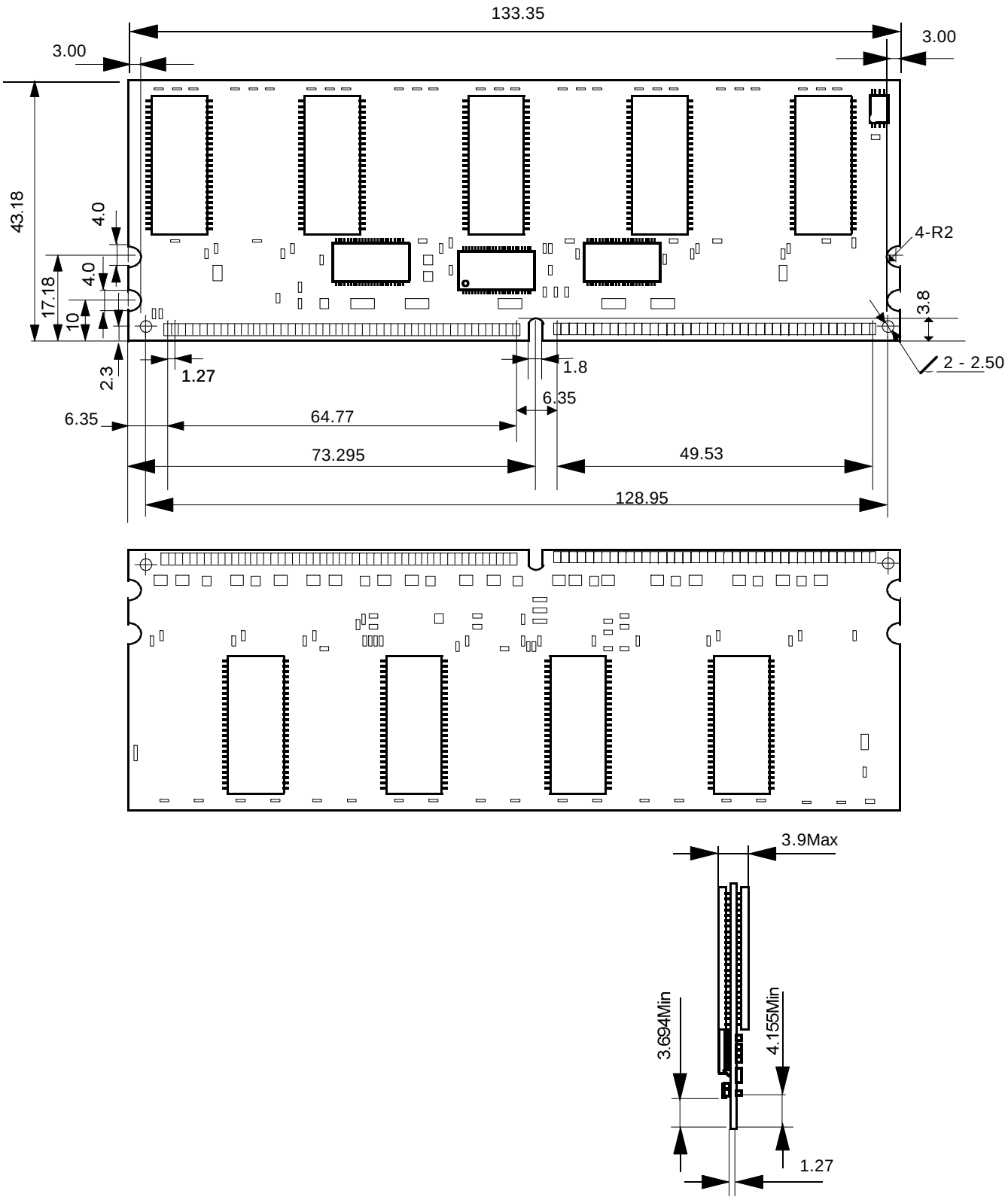
[DM CONTROL]

DM is defined as the data mask for writes. During writes,DM masks input data word by word. DM to write mask latency is 0.

DM Function(BL=8,CL=2(Discrete))

Module input and output timing.




133.35
3.00
3.00
43.18
4.0
17.18
4.0
10
4-R2
3.8
2 - 2.50
2.3
1.27
1.8
6.35
6.35
64.77
73.295
49.53
128.95
3.9Max
3.694Min
4.155Min
1.27

Serial Presence Detect Table I

Byte	Function described		SPD enrty data	SPD DATA(hex)
0	Number of Serial PD Bytes Written during Production		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		SDRAM DDR	07
3	# Row Addresses on this assembly		12	0C
4	# Column Addresses on this assembly		10	0A
5	# Module Banks on this assembly		1BANK	01
6	Data Width of this assembly...		x72	48
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		SSTL2.5V	04
9	SDRAM Cycletime at Max. Supported CAS Latency (CL).	-75	7.5ns	75
	Cycle time for CL=2.5	-10	8.0ns	80
10	SDRAM Access from Clock	-75	±0.75ns	75
	tAC for CL=2.5	-10	±0.8 ns	80
11	DIMM Configuration type (Non-parity,Parity,ECC)		ECC	02
12	Refresh Rate/Type		15.625uS/SR	80
13	SDRAM width,Primary DRAM		x8	08
14	Error Checking SDRAM data width		x8	08
15	MIimum Clock Delay, Random Column Access		1 clock	01
16	Burst Lengths Supported		2, 4, 8	0E
17	Number of Device Banks		4bank	04
18	CAS# Latency		2.0, 2.5	0C
19	CS# Latency		0	01
20	WE Latency		1	02
21	SDRAM Module Attributes		Registered with PLL Differential Clock	26
22	SDRAM Device Attributes:General		VDD± 0.2V	00
23	SDRAM Cycle time(2nd highest CAS latency)	-75	10ns	A0
	Cycle time for CL=2	-10	10ns	A0
24	SDRAM Access form Clock(2nd highest CAS latency)	-75	±0.75ns	75
	tAC for CL=2	-10	±0.8ns	80
25	SDRAM Cycle time(3rd highest CAS latency)	-75	Undefined	00
		-10	Undefined	00
26	SDRAM Access form Clock(3rd highest CAS latency)	-75	Undefined	00
		-10	Undefined	00
27	Minimum Row Precharge Time (tRP)		20ns	50
28	Minimum Row Active to Row Active Delay (tRRD)		15ns	3C
29	RAS to CAS Delay Minv (tRCD)		20ns	50
30	Active to Precharge Min (tRAS)	-75	45ns	2D
		-10	50ns	32

Serial Presence Detect Table II

31	Density of each bank on module		128MByte	20
32	Command and Address signal input setup time	-75	0.9nS	90
		-10	1.2nS	C0
33	Command and Address signal input hold time	-75	0.9nS	90
		-10	1.2nS	C0
34	Data signal input setup time	-75	0.5nS	50
		-10	0.6nS	60
35	Data signal input hold time	-75	0.5nS	50
		-10	0.6nS	60
36-61	Superset Information (may be used in future)		option	00
62	SPD Revision		0	00
63	Checksum for bytes 0-62		Check sum for -75	B4
			Check sum for -10	5A
64-71	Manufactures Jedec ID code per JEP-108E		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Manufacturing Location	XX
73-90	Manufactures Part Number		MH16D72AKLB-75	4D483136443732414B4C422D373520202020
			MH16D72AKLB-10	4D483136443732414B4C422D313020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yyww
95-98	Assembly Serial Number		serial number	ssssssss
99-127	Reserved		Undefined	00
128-255	Open for Customer Use		Undefined	00

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