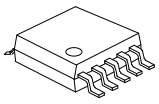
PA4894 **CMOS IC**

1.8 WATT DIFFERENTIAL AUDIO POWER AMPLIFIER WITH SELECTABLE SHUTDOWN



MSOP-10

■ DESCRIPTION

The UTC **PA4894** is a differential audio power amplifier, characterized by its selectable shutdown mode for flexible operation. Shutdown may be enabled by either logic high or low depending on the voltage applied on the SD MODE pin and the shutdown mode features low power consumption.

This device provides customers perfect sound performance by its high quality audio, moreover, less external components and lower power dissipation are required.

Operating with a 5.5V power supply, the UTC **PA4894** is capable of driving an 8.0Ω load at a continuous average output of 1.8W under a 10% THD+N. If it works with a 5.0V voltage under the same load conditions, 1.0W power will be delivered and the distortion will be less than 0.01%.

The UTC **PA4894** incorporates protection circuit to avoid the click and pop noise, which may occur during the transition state between turn-on and turn-off.

The UTC **PA4894** can be directly connected to a battery without an LDO since it has perfect PSRR. The UTC **PA4894** can be configured externally with resistors to provide a controlled gain and with bypass capacitor to provide a controlled turn-on time for more flexibility.

The UTC **PA4894** is suitable for applications, such as portable electronic devices, PDAs and mobile phones.

■ FEATURES

* Differential amplification
* Selectable and low current shutdown mode
* 1.0W/Ch(typ.)into a 8Ω load @5.0V
* Directly connected to the battery due to excellent PSRR
* Operation supply: 2.2 V-5.5 V
* External controlled gain and turn-on time configuration
* Circuits for protection
* Thermal overload protection circuit
* “Click and pop” noise protection circuit
* Halogen Free

■ ORDERING INFORMATION

Ordering Number	Package	Packing
PA4894G-SM2-R	MSOP-10	Tape Reel

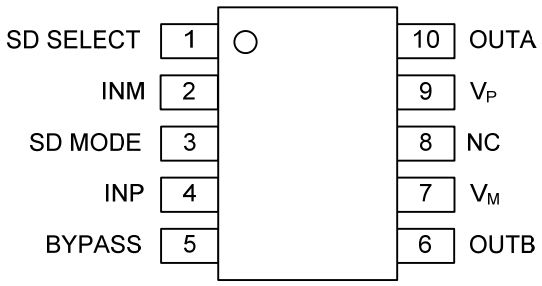
PA4894G-SM2 -R

(1)Packing Type
(2)Package Type
(3)Halogen Free

(1) R: Tape Reel
(2) SM2: MSOP-10
(3) G: Halogen Free

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■ PIN CONFIGURATION

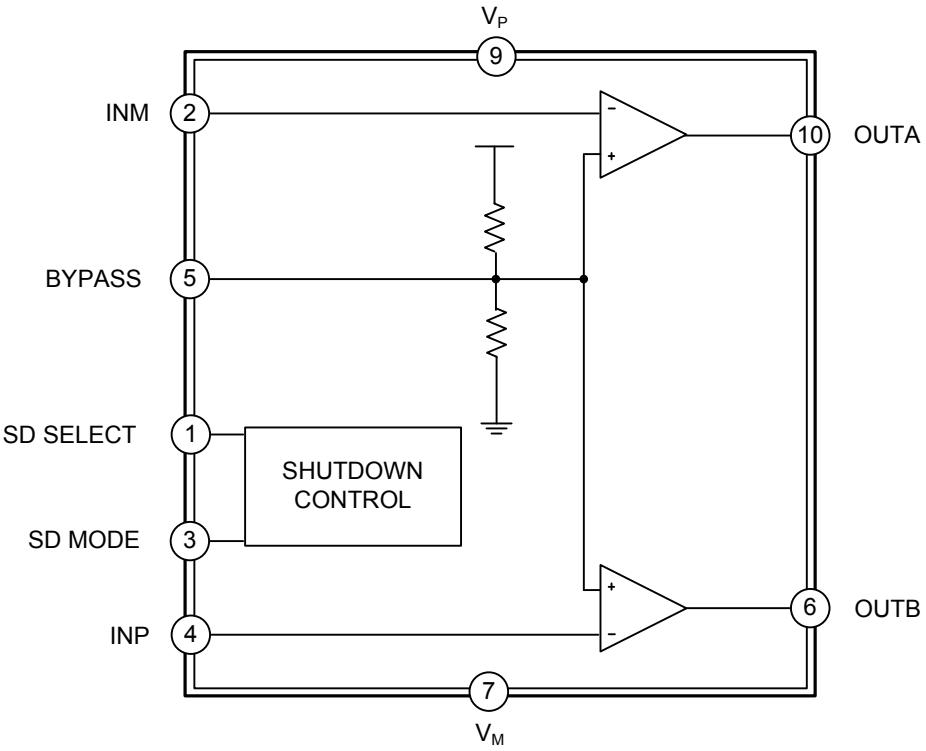


■ PIN DESCRIPTION

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	SD SELECT	O	(Note)
2	INM	I	Negative differential input
3	SD MODE	I	Shutdown high or low selectivity (Note)
4	INP	I	Positive differential input
5	BYPASS	O	Bypass capacitor pin which provides the common mode voltage
6	OUTB	I	Negative BTL output
7	V_M	I	Ground
8	NC	-	No connection
9	V_P	I	Positive analog supply of the cell
10	OUTA	I	Positive BTL output

Note: The SD SELECT pin must be toggled to the same state as the SD MODE pin to force the device in shutdown mode.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_P	6.0	V
Operating Supply Voltage	V_{OPR}	2.2 ~ 5.5	V
Input Voltage	V_{IN}	-0.3 ~ V_{CC} +0.3	V
Max Output Current	I_{OUT}	500	mA
Power Dissipation (Note 2)	P_D	Internally Limited	
Junction Temperature	T_J	150	°C
Operating Temperature (T_A)	T_{OPR}	-40 ~+85	°C
Storage Temperature Range	T_{STG}	−65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	200	°C/W

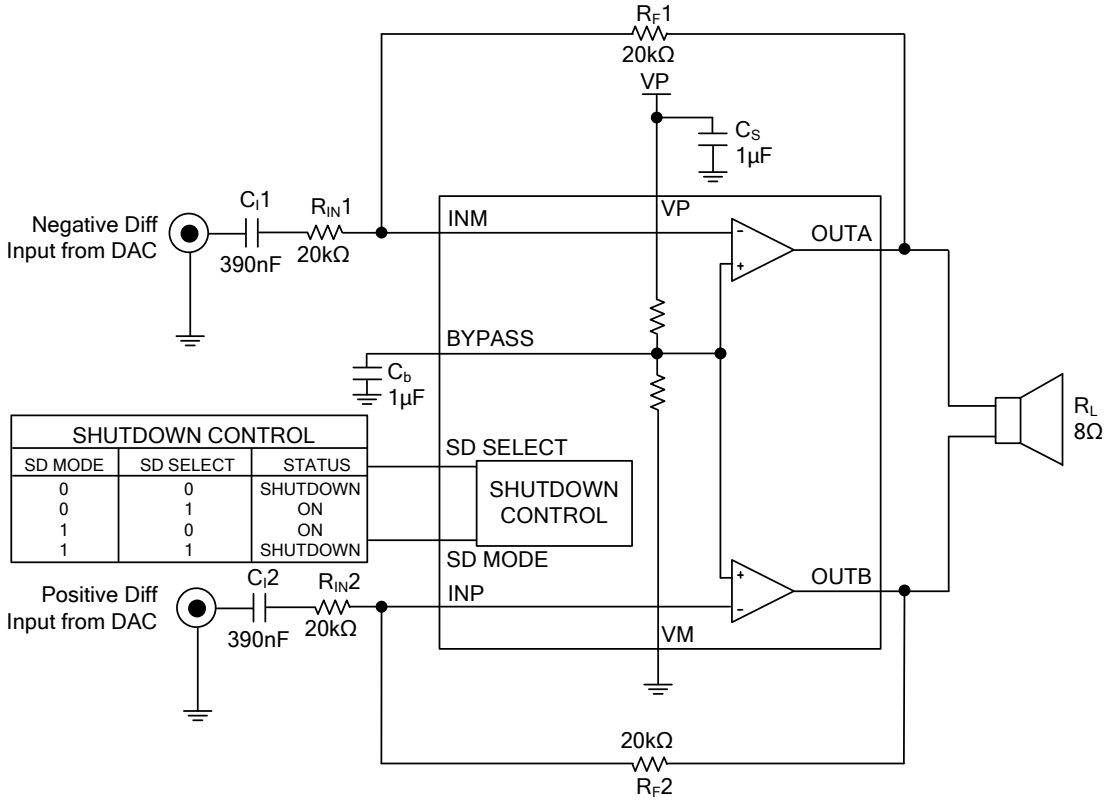
■ ELECTRICAL CHARACTERISTICS (Ta= −40°C~ +85°C, unless otherwise specified).

PARAMETER		SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Common Mode Voltage		V_{CM}					VP/2		V
SD Select Threshold	High	$V_{THD(H)}$				1.4			V
	Low	$V_{THD(L)}$						0.4	V
Output Swing		$V_{O(SW)}$	V_P = 3.0V, R_L= 8.0Ω				2.5		V
			V_P = 5.0V, R_L= 8.0Ω	Ta= 25°C		4.0	4.3		V
				Ta= -40°C ~ +85°C		3.85			V
Output Offset Voltage		$V_{O(OFF)}$	2.2V≤V_P≤5.5V			-30	1.0	30	mV
Supply Quiescent Current		I_Q	V_P = 3.0 V, No Load				1.9		mA
			V_P = 5.0 V, No Load				2.1		mA
			V_P = 3.0 V, 8.0Ω				2.0		mA
			V_P = 5.0 V, 8.0 Ω				2.2	4.0	mA
Shutdown Current		I_{SHDN}	2.2V≤V_P≤5.5V, SDM=SDS=GND	Ta= 25°C			20	600	nA
				Ta= -40°C ~ +85°C				2.0	μA
Turning On Time		T_{WU}	C_{BYP} = 1.0μF				140		ms
Turning Off Time		T_{SD}					20		ms
RMS Output Power		$P_{O(RMS)}$	R_L= 8.0Ω, THD+N<0.1%	V_P = 3.0 V			0.39		W
				V_P = 3.3 V			0.48		W
				V_P = 5.0 V			1.08		W
Power Supply Ratio		PSRR	G=2.0, R_L=8.0Ω, C_{BYP}= 1.0μF, $V_{P(RIPP_PP)}$= 200mV, Input Terminated with 10Ω	F=217 Hz	V_P=5.0V		-80		dB
					V_P=3.0V		-80		dB
				F=1.0 kHz	V_P=5.0V		-85		dB
					V_P=3.0V		-85		dB
Over Temperature Shutdown		OTS					160		°C
Efficiency		η	V_P = 3.0 V, $P_{O(RMS)}$= 380mW				64		%
			V_P = 5.0 V, $P_{O(RMS)}$= 1.0W				63		%
Total Harmonic Distortion		THD	V_P = 3.0V, F = 1.0 kHz, R_L= 8.0Ω, AV= 2.0, P_O= 0.32 W				0.007		%
			V_P = 5.0V, F = 1.0 kHz, R_L= 8.0Ω, AV= 2.0, P_O= 1.0 W				0.006		%

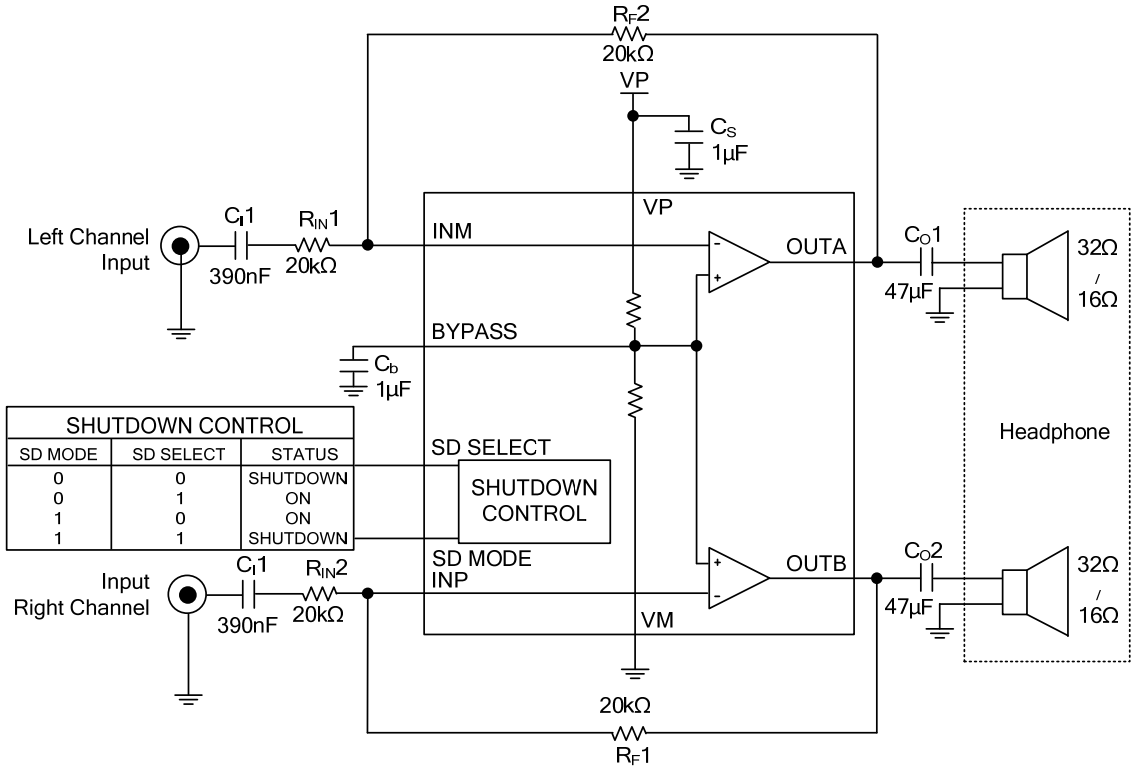
Notes: 1. Min and Max limits are guaranteed by design, test or statistical analysis.
2. See page 8 for a theoretical approach of these parameters.

■ TYPICAL APPLICATION CIRCUIT

Differential Input



Driving Headphone



■ APPLICATION INFORMATION

Detailed Description

The UTC **PA4894** includes two power amplifiers internally. Two of them provide a controlled gain with external components R_{IN} and R_F; the gain is calculated by the ratios of the resistors. The load is driven differentially through OUTA and OUTB outputs. This configuration is saving the use of an output coupling capacitor.

The UTC **PA4894** is operating on a 2.6V to 5.5V power supply, when V_P is 2.6V it delivers 320mW rms output power to 4.0Ω load, and when V_P is 5.0V, it delivered 1.0W rms output power to 8.0Ω load.

Internal Power Amplifier

The internal power amplifier contains output PMOS and NMOS transistors, which is used to deliver the output power of the specifications without clipping. The channel resistance (R_{ON}) of the NMOS and PMOS transistors does not exceed 0.6Ω when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

Turn-On and Turn-Off Transitions

Output power in the load established must be slowly or cut for minimize the click and pop noise during the transitions between turn-on and turn-off conditions. When shutdown mode is over，, the bypass voltage begins to rise exponentially and once the output DC level is around the common mode voltage, the turn-on mode is over.

The turn−on time is determined by the following equation (at 25°C):

$T_{ON} = 0.95 \times R \times C_{BYP}$

(C_{BYP}: bypass capacitor R: internal 150 k resistor with a 25% accuracy)

The turned off operation is as the same as the turn-on operation. Through applying a same logic state on the SD SELECT and SD MODE pins, the system enters this mode. During the shutdown mode, amplifier outputs are connected to the ground to discharge.

Shutdown Function

When SD SELECT and SD MODE pins are in the same logic state, the system enters shutdown mode. This brings flexibility to the design, as the SD MODE pin must be permanently connected to VP or GND on the PCB. In many applications, the output of a microcontroller or microprocessor is connected to the SD SELECT pin, so it is not better to allow this pin float. During the shutdown state, the DC quiescent current has a typical value of 10nA.

Current Limit Circuit

The current limit circuit protects the device from damage from excessive current. The maximum output power of the circuit ($P_{O(RMS)}$ =1.0W, V_P = 5.0V, R_L = 8.0Ω) requires a peak current in the load of 500mA. When short-circuit occurs between both outputs, the current limit in the load is fixed to 800mA for limiting the excessive power consumption.

■ APPLICATION INFORMATION(Cont.)

Thermal Overload Protection

When the temperature of the UTC **PA4894** is higher than160°C for any reasons, the thermal overload protection function turns the amplifiers off until the temperature drop below 140°C.

The UTC **PA4894** is unity gain stable and requires no external components besides gain setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application. Both internal amplifiers are externally configurable (R_F and R_{IN}) with gain configuration.

The differential ended amplifier has two main benefits compared to single-ended:

* The differential ended amplifier will yield 4 times larger the output power on the load at the same conditions compared to a single ended amplifier.

* Output pins (OUTA and OUTB) are biased at the same potential VP/2, which is saving the use of an output coupling capacitor that is required with a single ended amplifier configuration.

The differential closed loop gain of the amplifier is correlated as seen in the following ratio:

$$Avd = \frac{R_F}{R_{IN}} = \frac{V_{O(RMS)}}{V_{IN(RMS)}}$$

$V_{O(RMS)}$: the rms value of the voltage seen by the load
$V_{IN(RMS)}$:the rms value of the input differential signal)

Output power delivered to the load is defined as follows:

$$P_{O(RMS)} = \frac{(V_{O(PEAK)})^2}{2 \times R_L}$$

$V_{O(PEAK)}$ is the peak differential output voltage

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500mA $I_{O(PEAK)} = \frac{V_{O(PEAK)}}{R_L}$

Gain−Setting Resistor Selection (R_{IN} and R_F)

The UTC **PA4894** requires low gain configurations for a better performance. Since the R_{IN} and R_F determine the closed−loop gain of both amplifiers, it is critical to choose both of them.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 ~ 5 is recommended to optimize overall system performance.

22 kΩ input resistor (R_{IN})is recommended.

Input Capacitor Selection (C_{IN})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. A high−pass filter is generated by this capacitor and Rin, and the cut−off frequency is defined by the following fomula:

$$f_C = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage (VP/2) and can increase the turn−on pops.

An input capacitor value between 0.1µ and 0.39µF is sugguested in most applications.

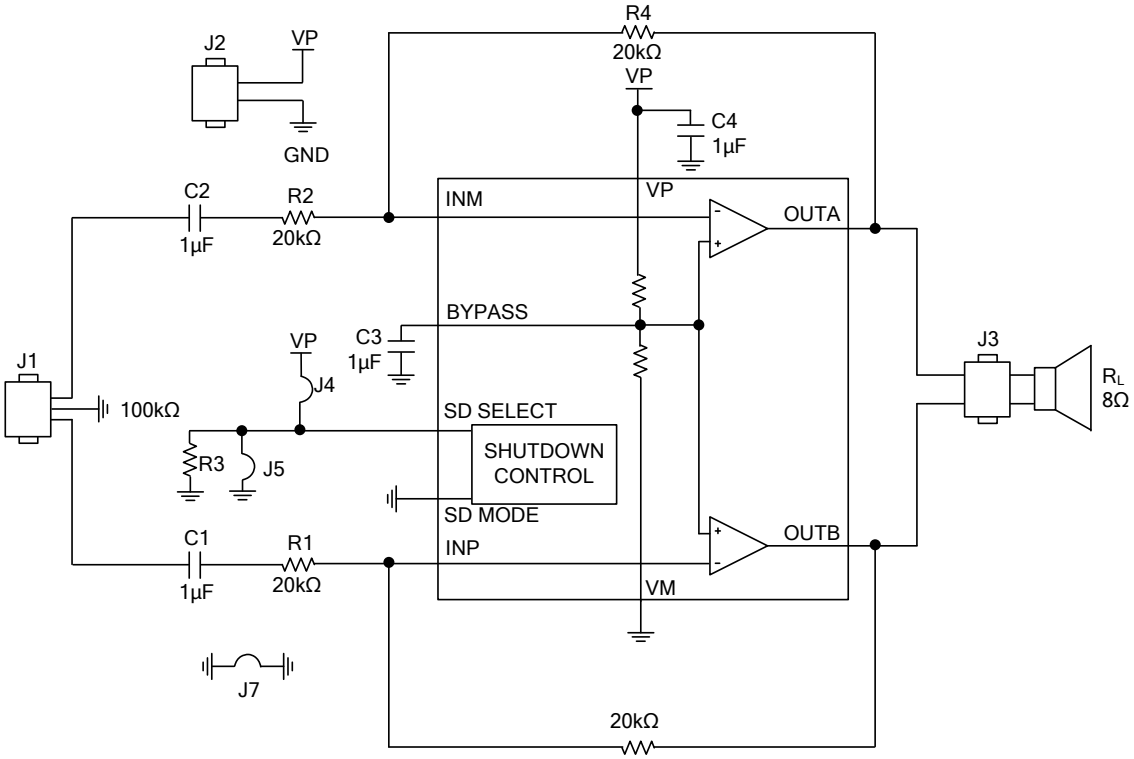
Bypass Capacitor Selection (C_{BYP})

To avoid the pop noise, the bapass capacitor should be chosen prompty. The bypass capacitor determines the rate at which this device starts and it provides half−supply filtering.

A 1.0µF bypass capacitor value (C_{IN}≤ 0.39µF) should produce clickless and popless shutdown transitions. So a 1.0µF bypassing capacitor is recommended to be used.

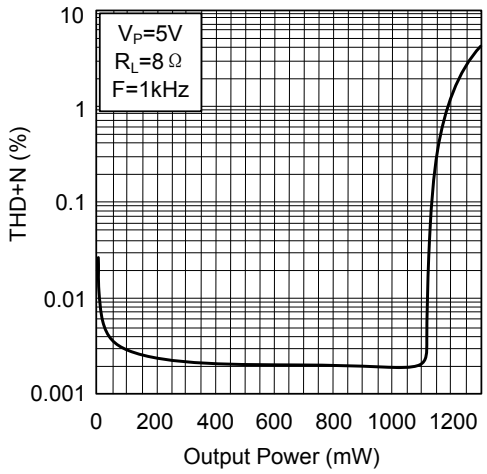
■ APPLICATION INFORMATION(Cont.)

Demo Board Schematic

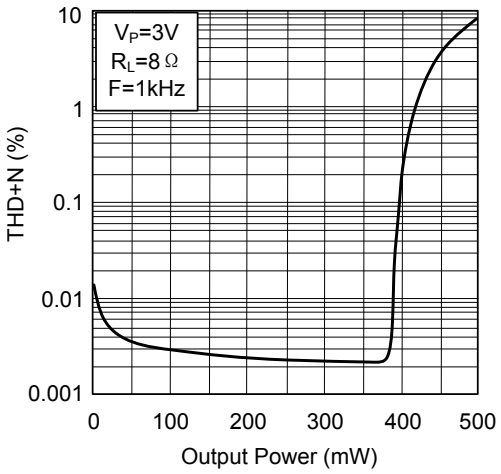


■ TYPICAL CHARACTERISTICS

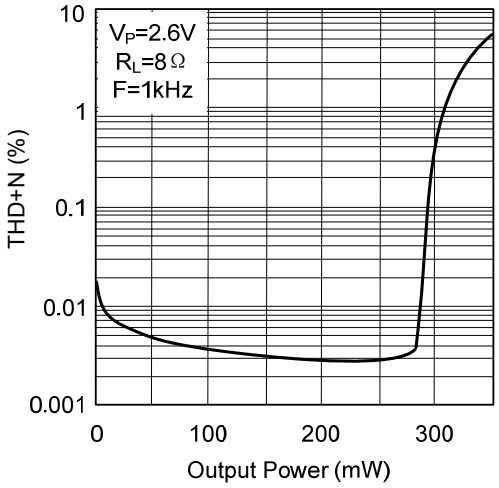
THD+N vs. Output Power



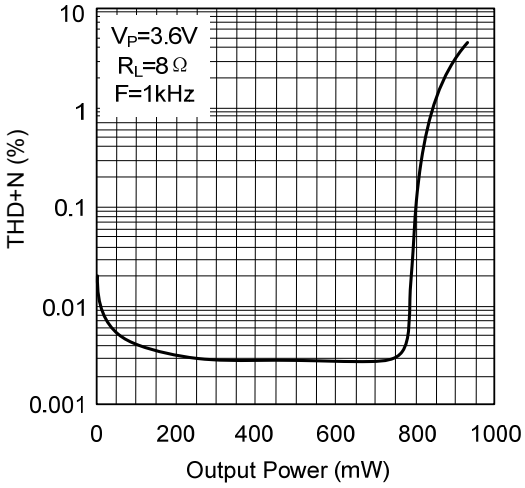
THD+N vs. Output Power



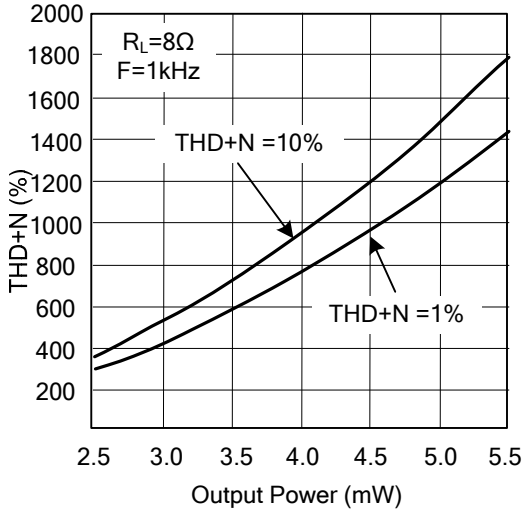
THD+N vs. Output Power



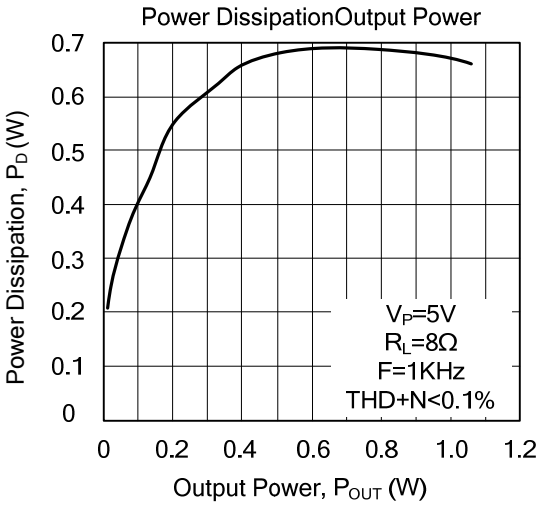
THD+N vs. Output Power

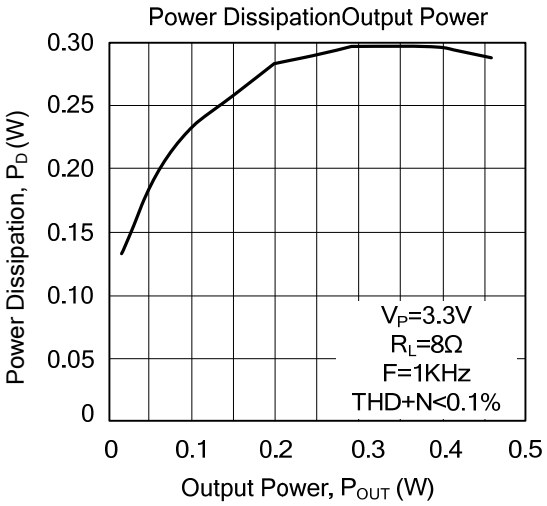


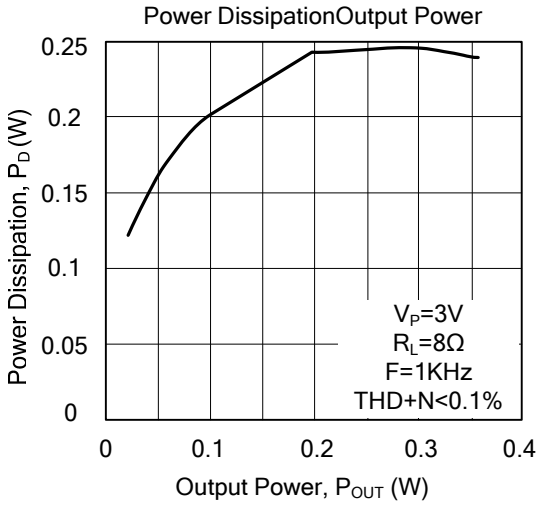
THD+N vs. Output Power

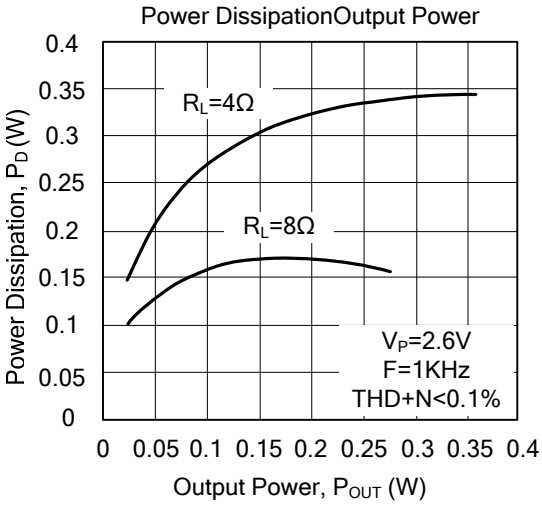


■ TYPICAL CHARACTERISTICS(Cont.)

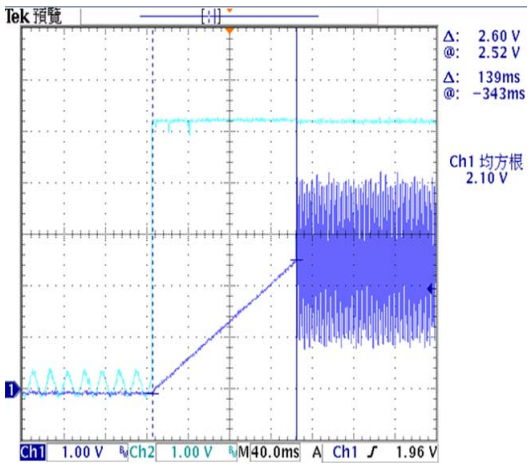




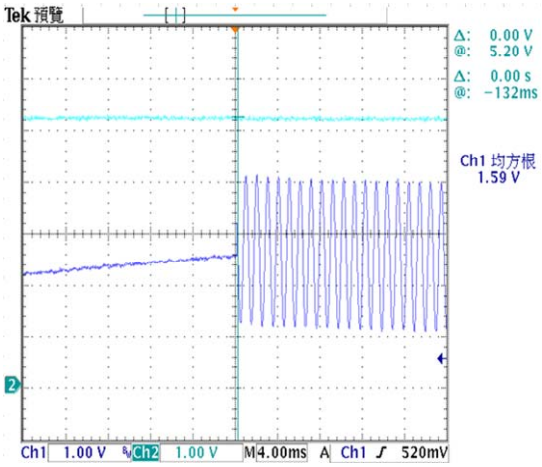




Turning-on Sequence

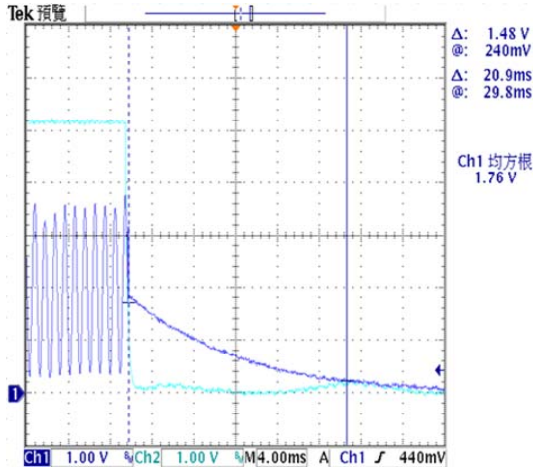


Turning-on Sequence Zoom

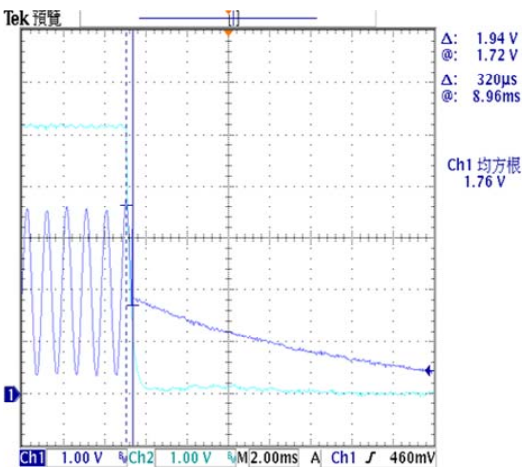


■ TYPICAL CHARACTERISTICS(Cont.)

Turning-off Sequence



Turning-off Sequence Zoom



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