MX23J12840

128M-BIT NAND INTERFACE XtraROM™

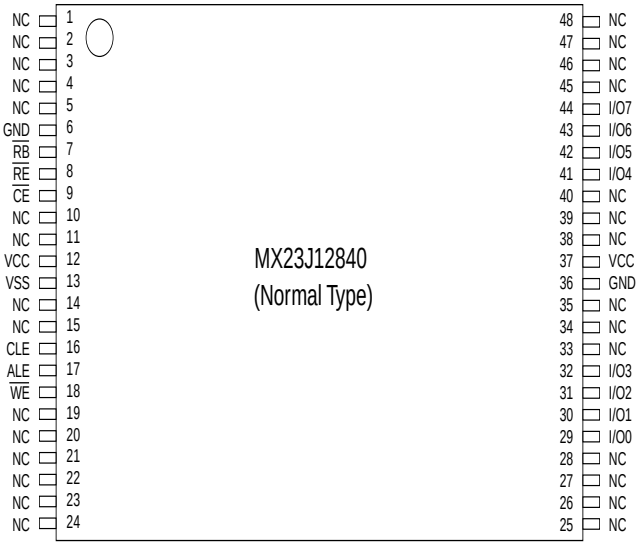
FEATURES

- Word organization
  - (16,777,216 + 1,048,576Note) by 8 bits
- Page size
  - (512 + 16Note) by 8 bits
- Block size
  - (16,384 + 512Note) by 8 bits

  Note : Underlined parts are redundancy and fixed to all FFH.
- Operation mode
  - READ mode (1), READ mode (2), READ mode (3), RESET
- Operating supply voltage : VCC = 2.7~3.6V
- Access Time
  - Memory cell array to starting address : 7 us (MAX.)
  - Read cycle time : 50 ns (MAX.)
  - $\overline{RE}$ access time : 35 ns (MAX.)
- Operating supply current
  - During read : 30 mA (MAX.) (50 ns cycle operation)
  - During standby (CMOS) : 40 uA (MAX.)
- Package Type
  - 48-pin TSOP(I) (12mmx20mm)
- XtraROM™ : factory pre-programmed ROM with Macronix NBit™ technology, supporting short TAT
- Process
  - 0.15um

PIN CONFIGURATIONS

48 TSOP



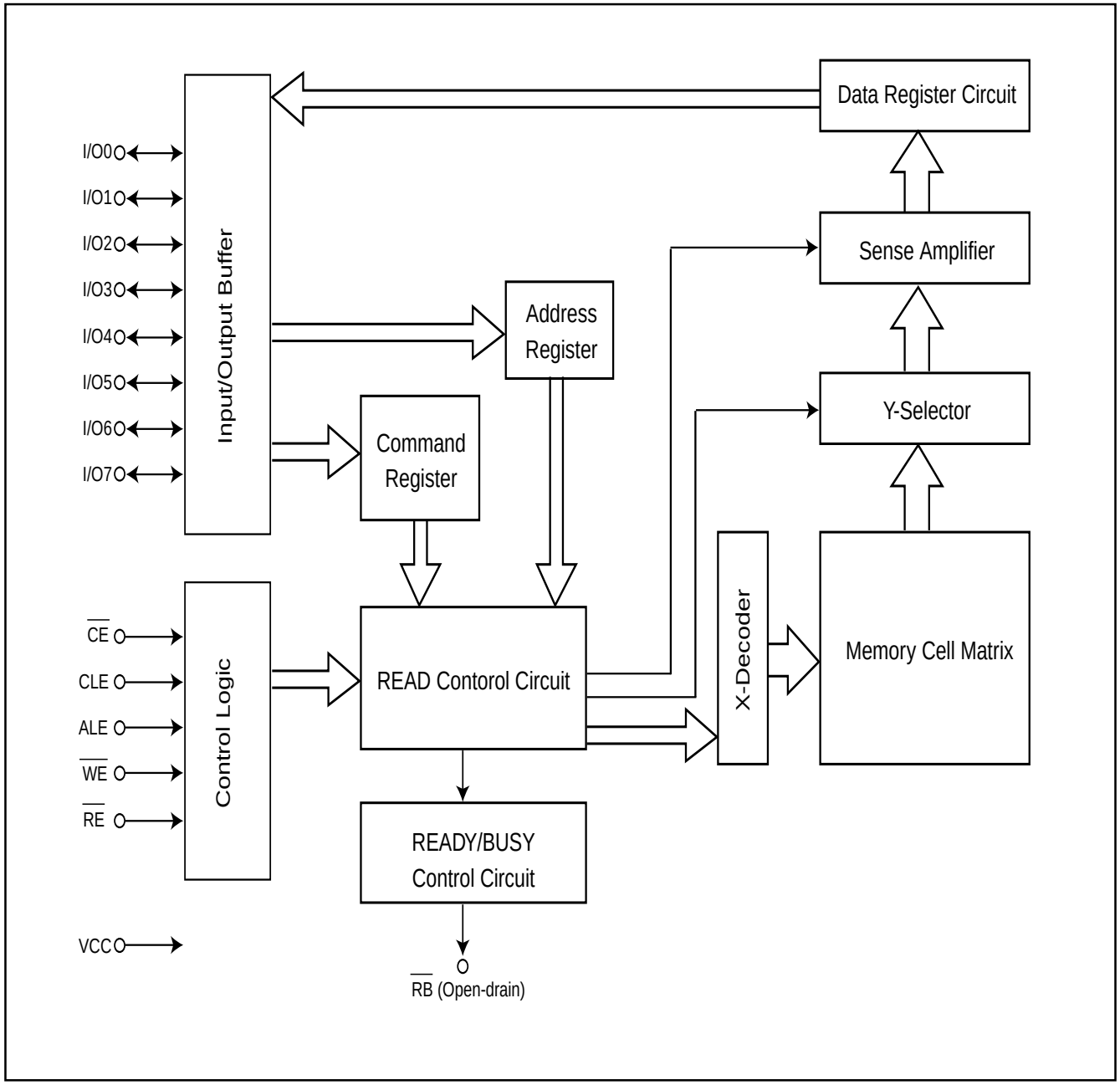
PIN DESCRIPTION

SYMBOL	PIN NAME
I/O0~I/O7	Address Input/Command Inputs/ Data Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
$\overline{CE}$	Chip Enable
$\overline{RB}$	READY, /BUSY pin
VCC	Supply Voltage
NC	No Connection
GND	Ground

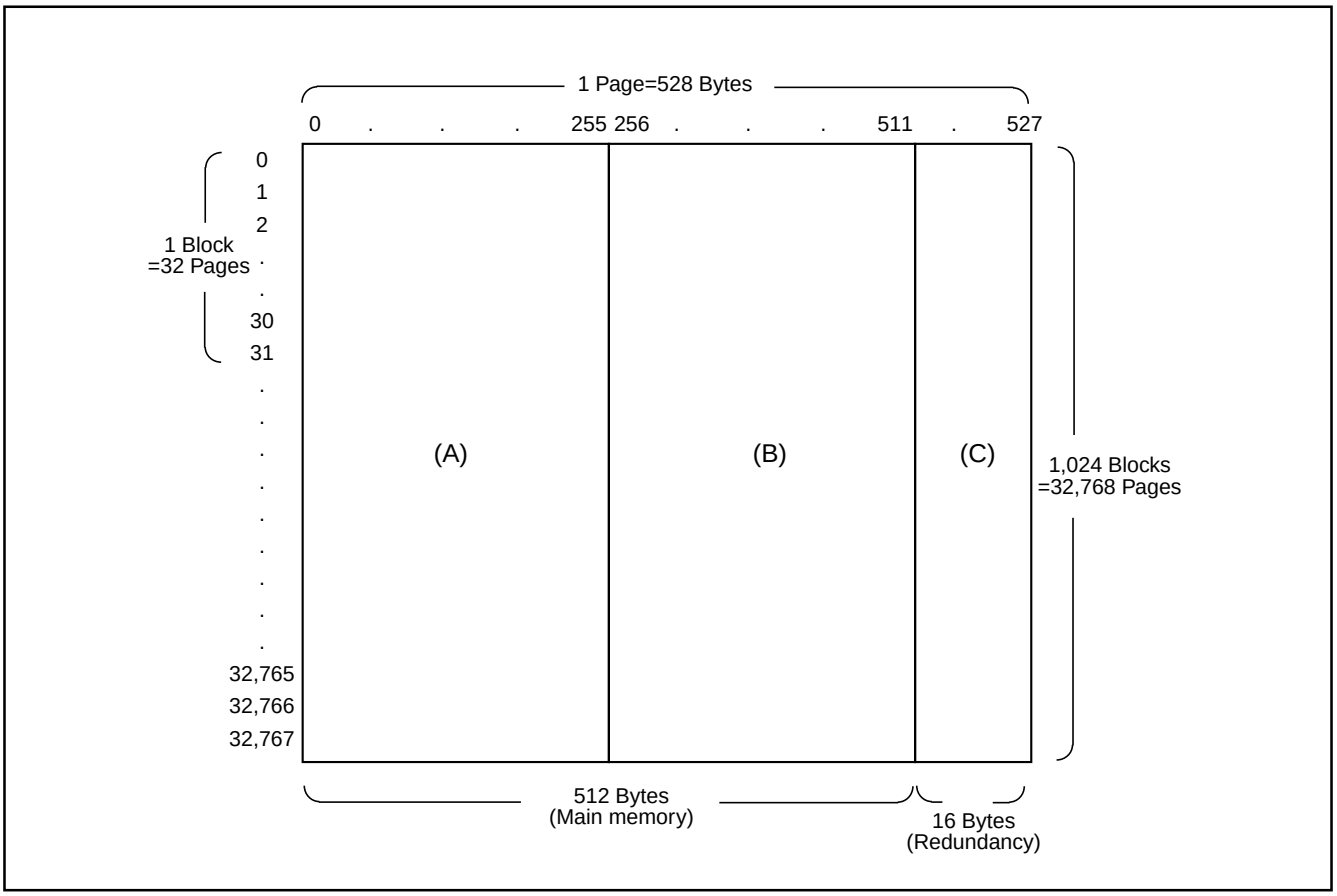
ORDER INFORMATION

Part No.	Package	Grade
MX23J12840TC-50G	48 pin TSOP (Pb-free, RoHS)	Commercial
MX23J12840TC-50	48 pin TSOP	Commercial
MX23J12840TI-50G	48 pin TSOP (Pb-free, RoHS)	Industrial

BLOCK DIAGRAM



MEMORY MAP



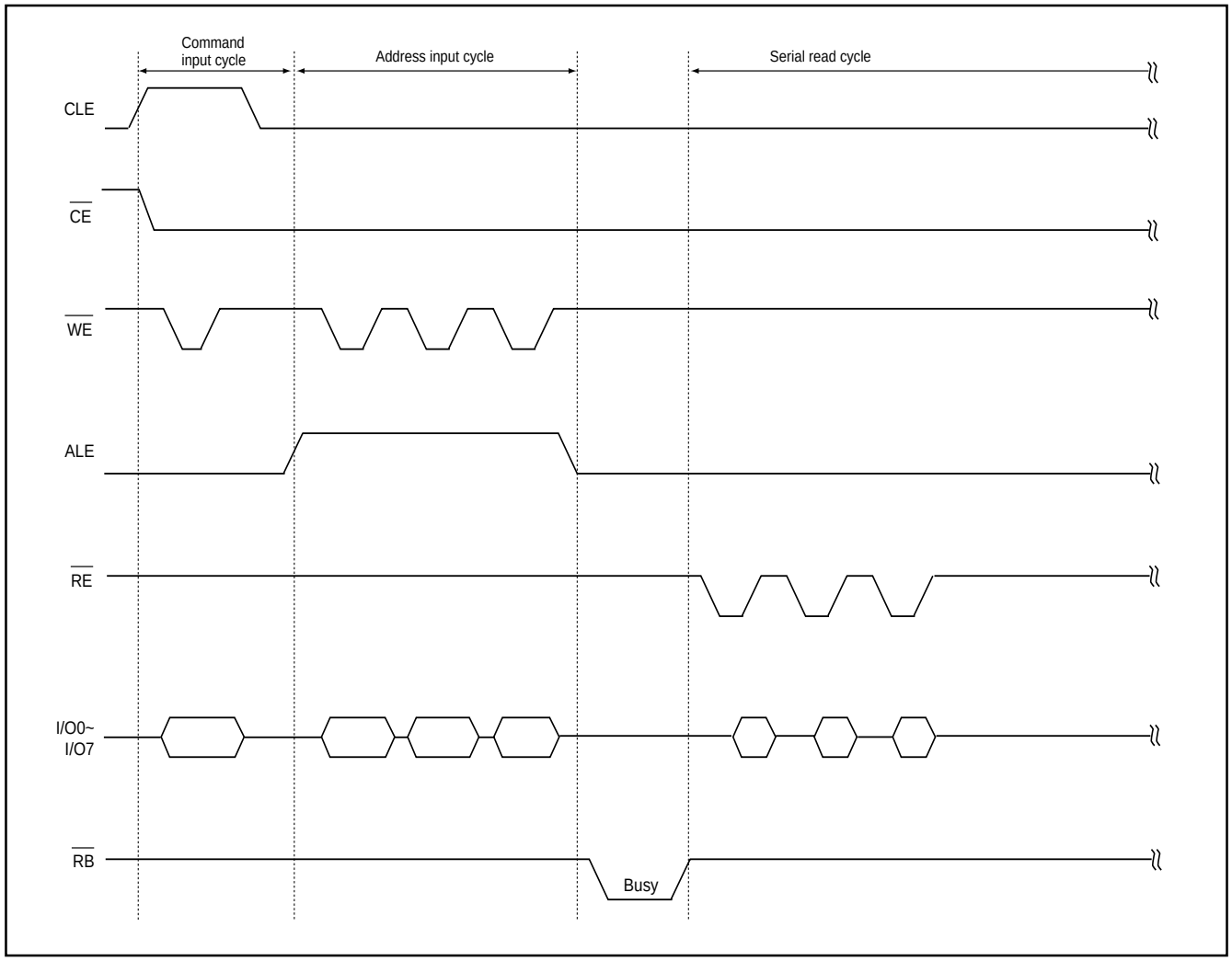
- The start address (SA) during read operation is specified divided into three areas using three types of read commands.
  - In read mode (1), start address (SA) is set in area (A).
  - In read mode (2), start address (SA) is set in area (B).
  - In read mode (3), start address (SA) is set in area (C).

One page consists of a total of 528 bytes broken down into 512 bytes (main memory) and 16 bytes (redundancy). One block consists of 32 pages.

Caution The data of area (C) is redundancy, which is not programmable and is fixed to all FFH.

Operation Modes

Command input, address input, and serial read are all performed from I/O pins, and the respective statuses are controlled by the CLE, ALE, $\overline{WE}$, $\overline{RE}$, and $\overline{CE}$ signals.



Operation mode

Mode	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$
Command input cycle	H	L	L	⌐‾↑	H
Address input cycle	L	H	L	⌐‾↑	H
Serial read cycle	L	L	L	H	↓⌐

Operation mode during serial read

Mode	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 - I/O7
Data output	L	L	L	H	L	Data output
Output Hi-Z	L	L	L	H	H	Hi-Z
Standby	L	L	H	H	x	Hi-Z

Remark ´ : VIH or VIL

Operation Commands

The following six operation settings are possible by inputting commands from I/O pins.

Command	Hex	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Command receivable during Busy
Read mode(1)	00	L	L	L	L	L	L	L	L	
Read mode(2)	01	L	L	L	L	L	L	L	H	
Read mode(3)Note1	50	L	H	L	H	L	L	L	L	
Reset Note2	FF	H	H	H	H	H	H	H	H	○

Notes:
1. The data output in read mode (3) is all FFH.
2. The only command that can be executed when the device is Busy is the reset command. Do not set any of the other commands while the device is Busy.

I/O Pin Correspondence Table during Address Input Cycle (Address Setting)

(1) When 00H or 01H command is set [Read mode (1), Read mode (2)]

Command	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st address cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd address cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd address cycle	X	A23	A22	A21	A20	A19	A18	A17

(2) When 50H command is set [Read mode (3)]

Command	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st address cycle	X	X	X	X	A3	A2	A1	A0
2nd address cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd address cycle	X	A23	A22	A21	A20	A19	A18	A17

Remarks
1. A0 to A23 are internal addresses.
2. Internal address A8 is set internally with command 00H or 01H.
3. When 50H command is set [read mode (3)], the I/O4, I/O5, I/O6, and I/O7 inputs of the 1st address cycle are VIH or VIL.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	VCC		-0.5 to +4.6	V
Input voltage	VI		-0.3 to VCC+0.3	V
Input / Output voltage	VI/O		-0.3 to VCC+0.3 (≤ 4.6)	V
Operating ambient temperature	TA		-40 to 85	°C
Storage temperature	Tstg		-65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (TA = 25° C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI	f = 1 MHz			10	pF
Output capacitance	CO				10	pF

DC Characteristics (TA = -40 to 85° C, VCC = 2.7~3.6V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	VIH		2.0		VCC+0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
High level output voltage	VOH	IOH =-400uA	2.4			V
Low level output voltage	VOL	IOL = 2.1 mA			0.4	V
Input leakage current	ILI	VI = 0 V to VCC			±10	uA
Output leakage current	ILO	VO = 0 V to VCC			±10	uA
Power supply current in read	ICCO1	$\overline{CE}$ = VIL, IOUT =0 mA, tCYCLE = 50 ns			30	mA
Standby current (CMOS)	ICCS2	$\overline{CE}$ = VCC-0.2 V			40	uA
$\overline{RB}$ pin output current	IOL($\overline{RB}$)	VOL = 0.4 V		8		mA

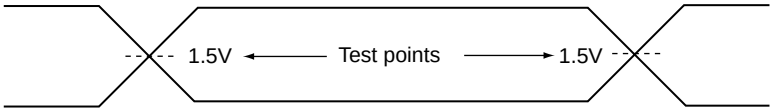
AC Characteristics (TA = -40 to 85° C, VCC = 2.7~3.6V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
CLE setup time	tCLS	0			ns
CLE hold time	tCLH	10			ns
$\overline{CE}$ setup time	tCS	0			ns
$\overline{CE}$ hold time	tCH	10			ns
Write pulse width	tWP	25			ns
ALE setup time	tALS	0			ns
ALE hold time	tALH	10			ns
Data setup time	tDS	20			ns
Data hold time	tDH	10			ns
Write cycle time	tWC	50			ns
$\overline{WE}$ high hold time	tWH	15			ns
Ready to $\overline{RE}$ falling edge	tRR	20			ns
Read pulse width	tRP	35			ns
Read cycle time	tRC	50			ns
$\overline{RE}$ access time (serial data access)	tREA			35	ns
$\overline{CE}$ high hold time for last address in serial read cycle	tCEH	100			ns
$\overline{RE}$ high to output Hi-Z	tRHZ	10		30	ns
$\overline{CE}$ high to output Hi-Z	tCHZ			20	ns
$\overline{RE}$ high hold time	tREH	15			ns
Output Hi-Z to $\overline{RE}$ falling edge	tIR	0			ns
$\overline{WE}$ high to $\overline{RE}$ low	tWHR	30			ns
Memory cell array to starting address	tR			7	us
$\overline{WE}$ high to Busy	tWB			200	ns
ALE low to $\overline{RE}$ low (read cycle)	tAR2	50			ns
$\overline{RE}$ last clock rising edge to Busy (in sequential read)	tRB			200	ns
$\overline{CE}$ high to Ready (when interrupted by $\overline{CE}$ in read mode)	tCRY[Note]			1	us
Device reset time	tRST			6	us

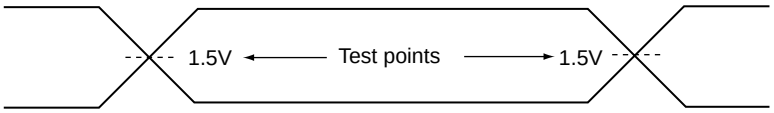
Note :tCRY (time from $\overline{CE}$ to Ready) depends on the pull-up resister of the $\overline{RB}$ pin.

AC Test Conditions

Input Waveform (Rise/Fall Time ≤ 5ns)



Output Waveform

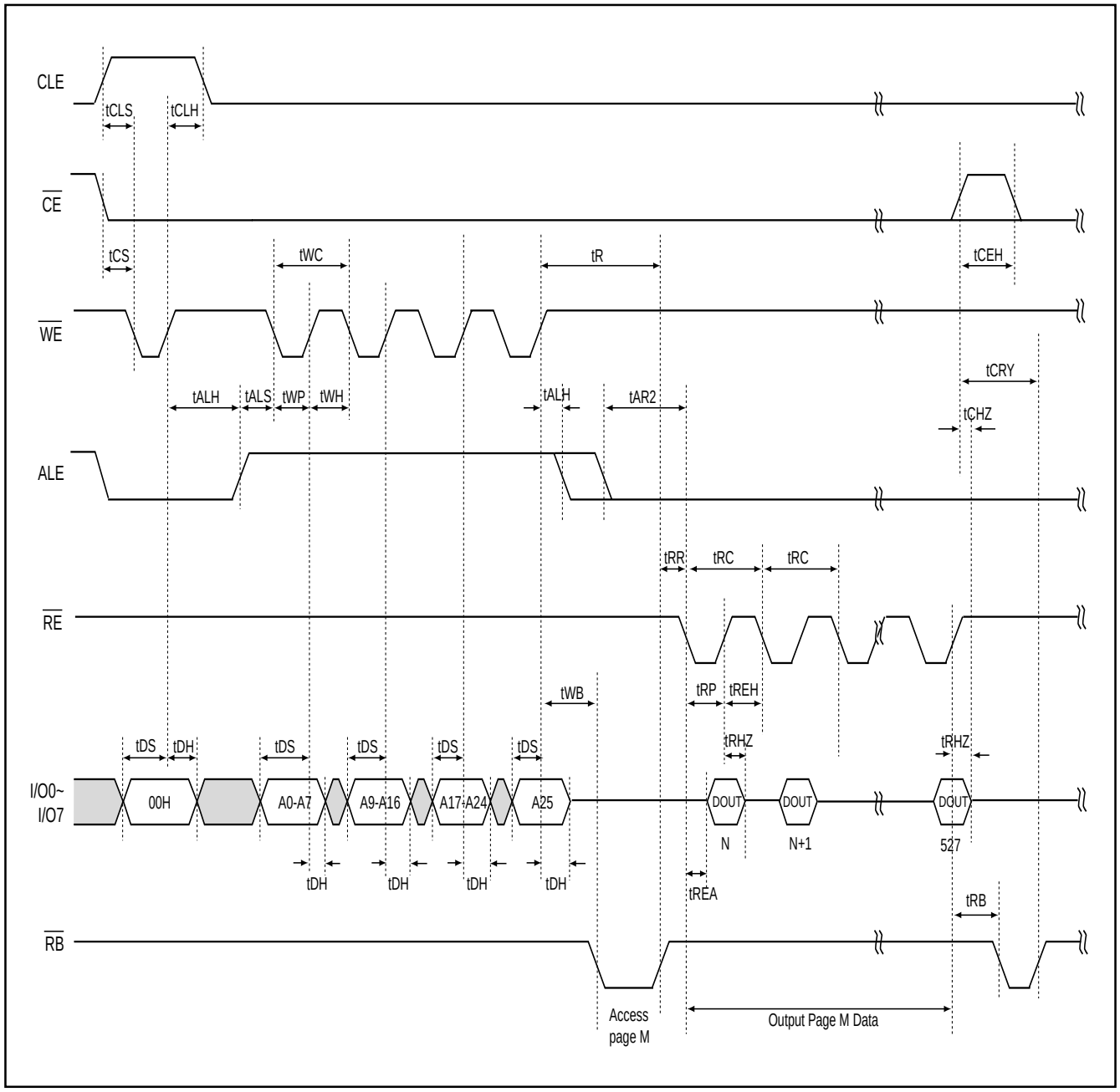


Input Pulse Levels : 0.4 ~ 2.4V

Output Load : 1 TTL + 100pF

READ CYCLE TIMING CHART (1)

(In case of read mode (1))

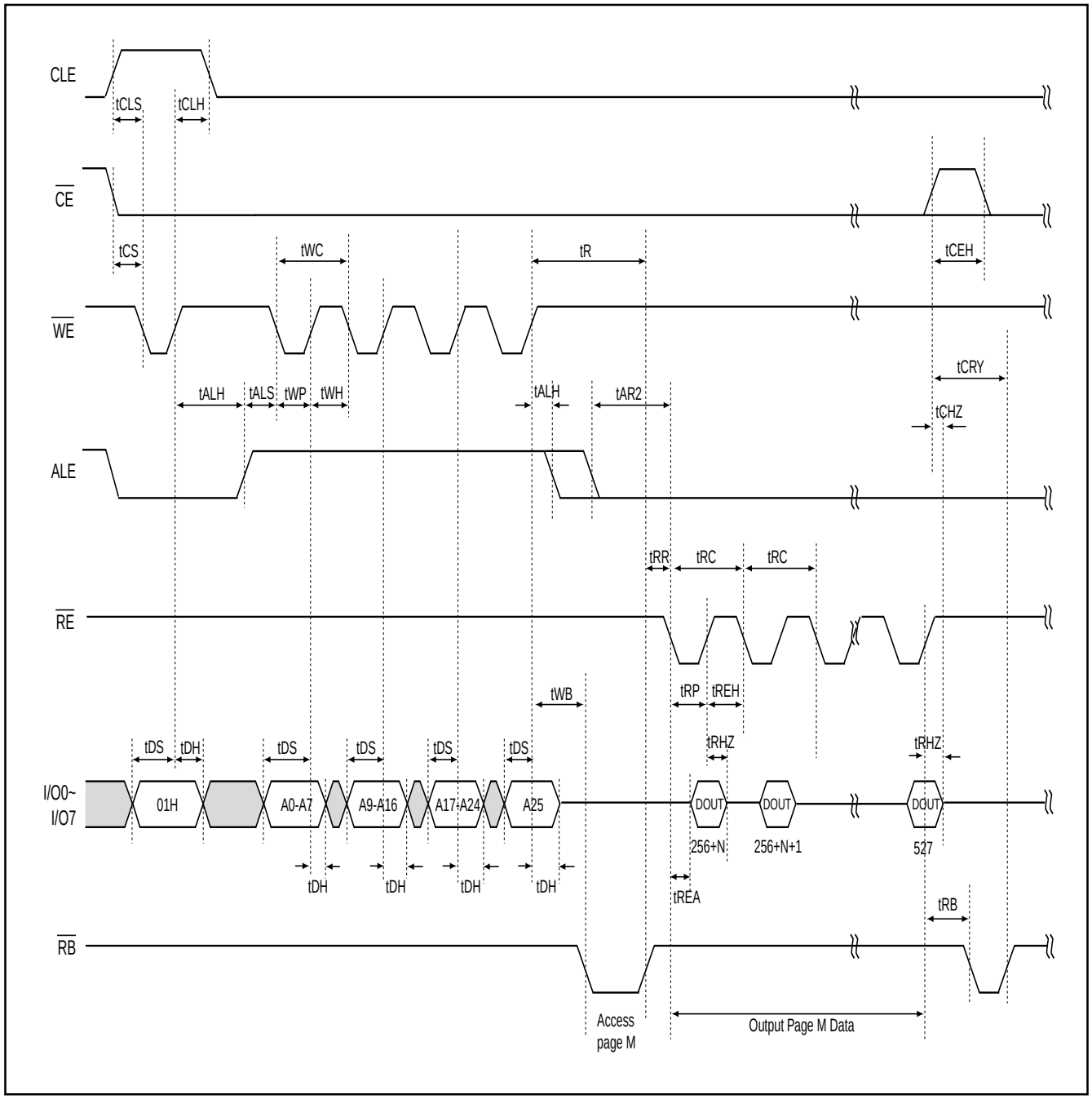


Remarks:

1. Start address (SA) specification when read is performed with command 00H. N: 0 to 255
2. The time (tCRY) from $\overline{CE}$ high level until Busy is cancelled depends on the pull-up register of the $\overline{RB}$ output pin.

READ CYCLE TIMING CHART (2)

(In case of read mode (2))

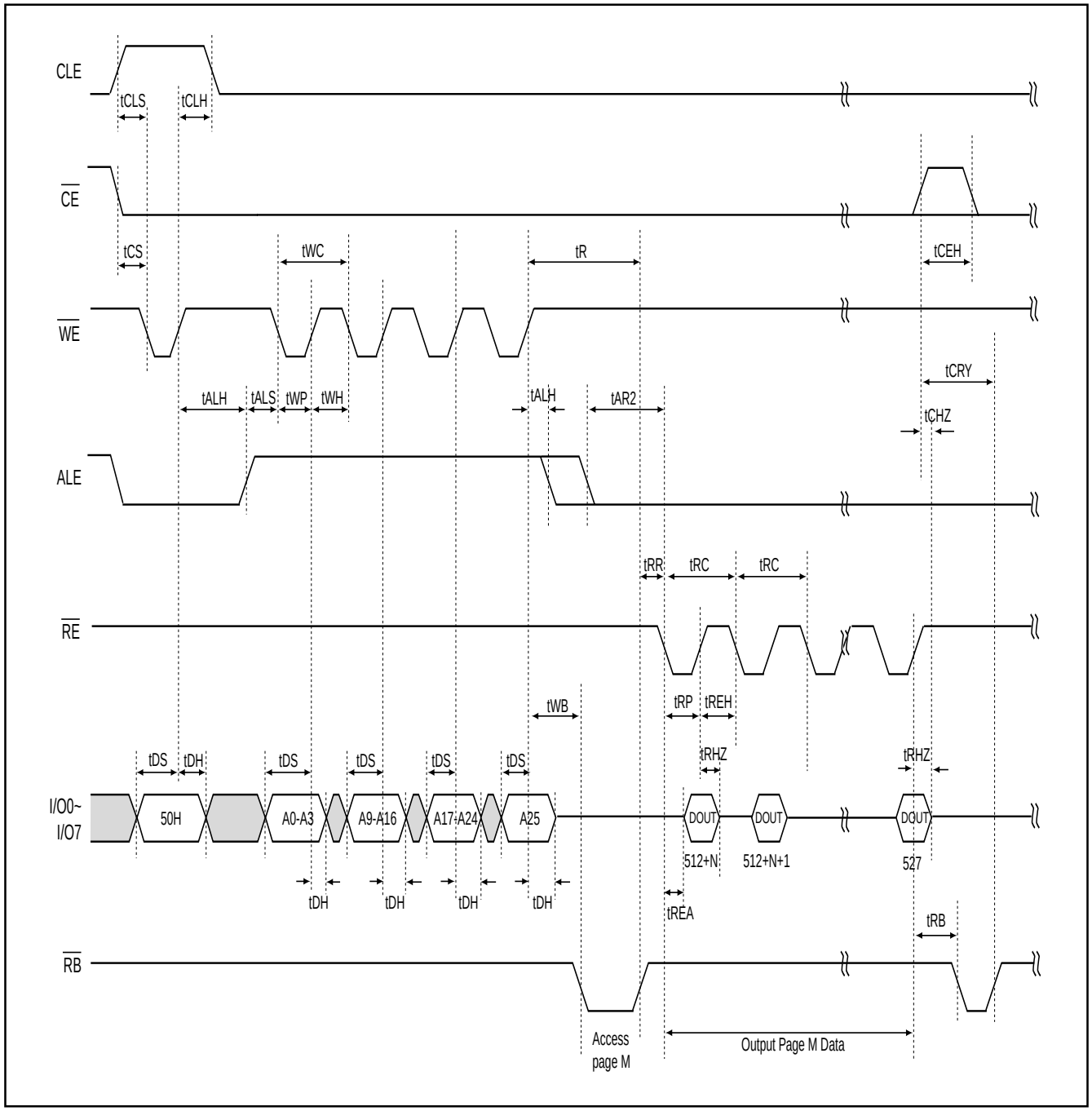


Remarks

1. Start address (SA) specification when read is performed with command 01H. N: 0 to 255
2. The time (tCRY) from $\overline{CE}$ high level until Busy is cancelled depends on the pull-up register of the $\overline{RB}$ output pin.

READ CYCLE TIMING CHART (3)

(In case of read mode (3))

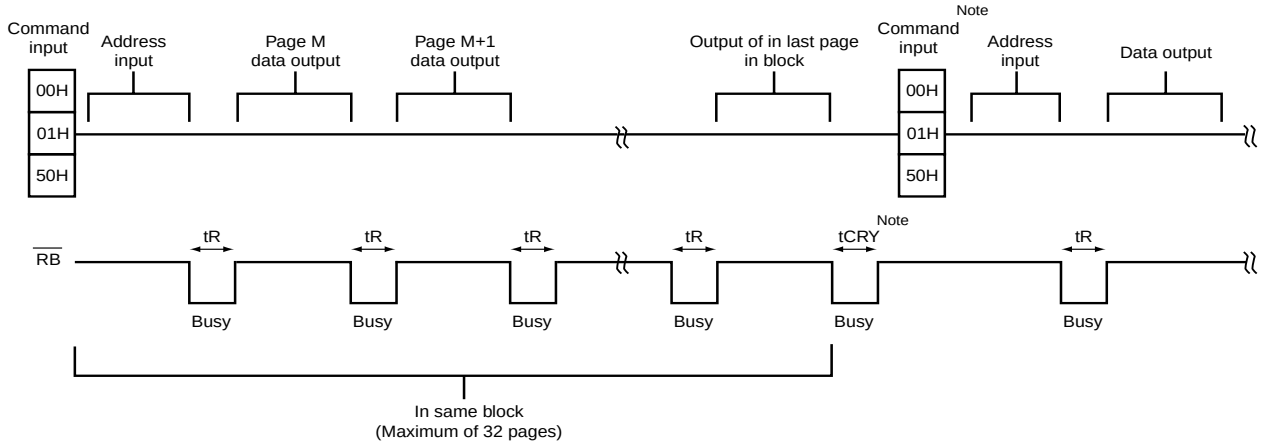


Remarks

1. Start address (SA) specification when read is performed with command 50H. N: 0 to 15
2. The start address of area C (redundancy data) is specified with A0 tp A3 during the 1st address cycle. At this time, A4 to A7 are Don't Care.
3. The time (tCRY) from $\overline{CE}$ high level until Busy is cancelled depends on the pull-up register of the $\overline{RB}$ output pin.

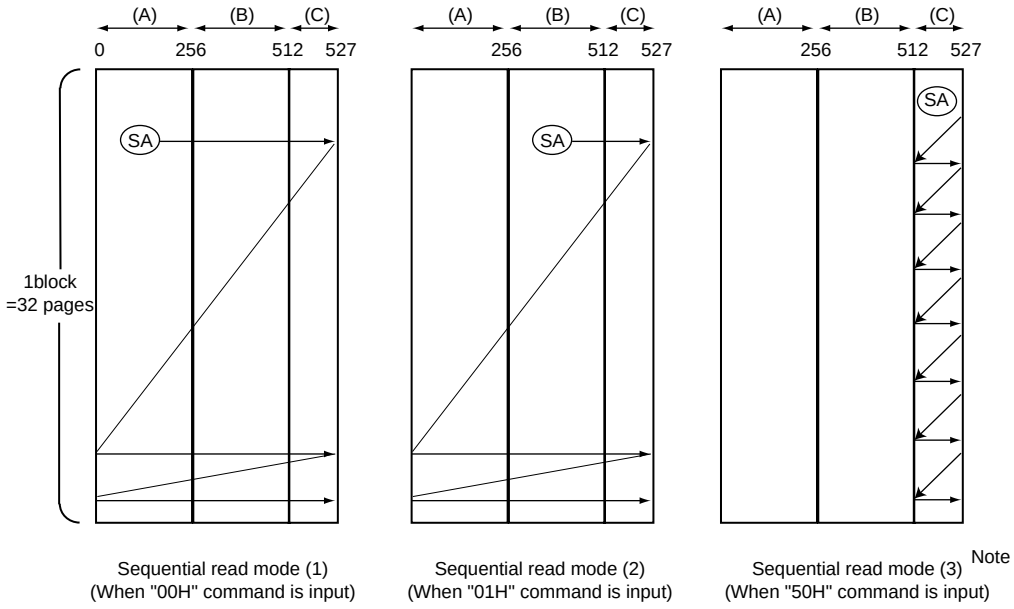
Sequential Read

In read modes (1), (2), and (3), when a command (00H, 01H, 50H) is input and an address specified, if it is in the block that includes the address that was specified first, the address is automatically incremented and the read operation is continuously performed until the last address in the same block, by inputting the RE# clock. At this time, a Busy period (tR) occurs after the last address is accessed in a page.



Note :To perform read again after reading the 527th byte of data of the last page of block, stop the read operation once, and then restart the read operation by inputting again the read command and an address.

Relationship Between Command and Start Address (SA) during Sequential Read

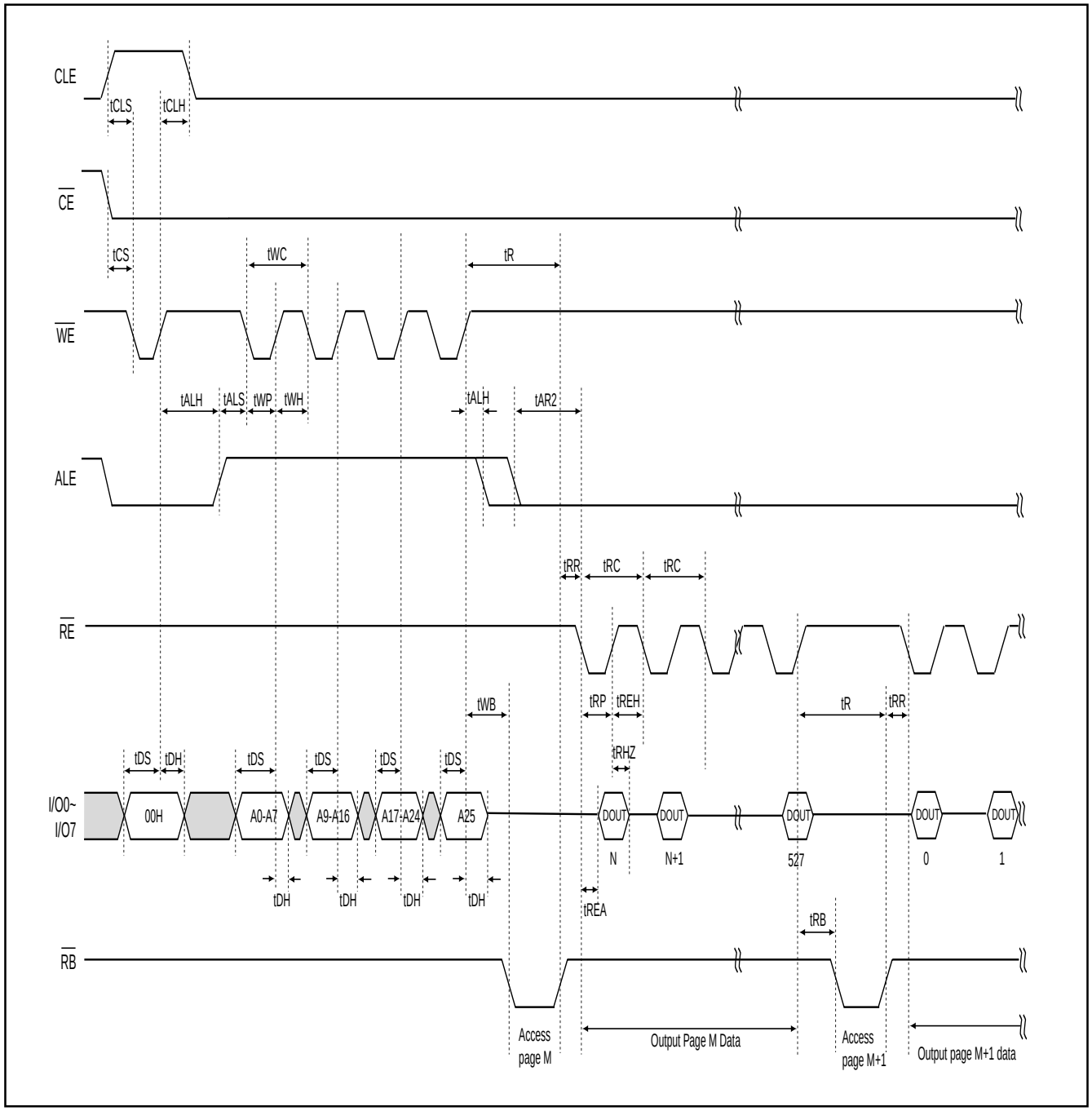


Note : When the "50H" command is set, only the (C) area (redundancy data part) is continuously read.

- When the "00H" command is set, the start address (SA) is set to area (A).
- When the "01H" command is set, the start address (SA) is set to area (B).
- When the "50H" command is set, the start address (SA) is set to area (C).

SEQUENTIAL READ CYCLE TIMING CHART(1)

(In case of read mode (1))

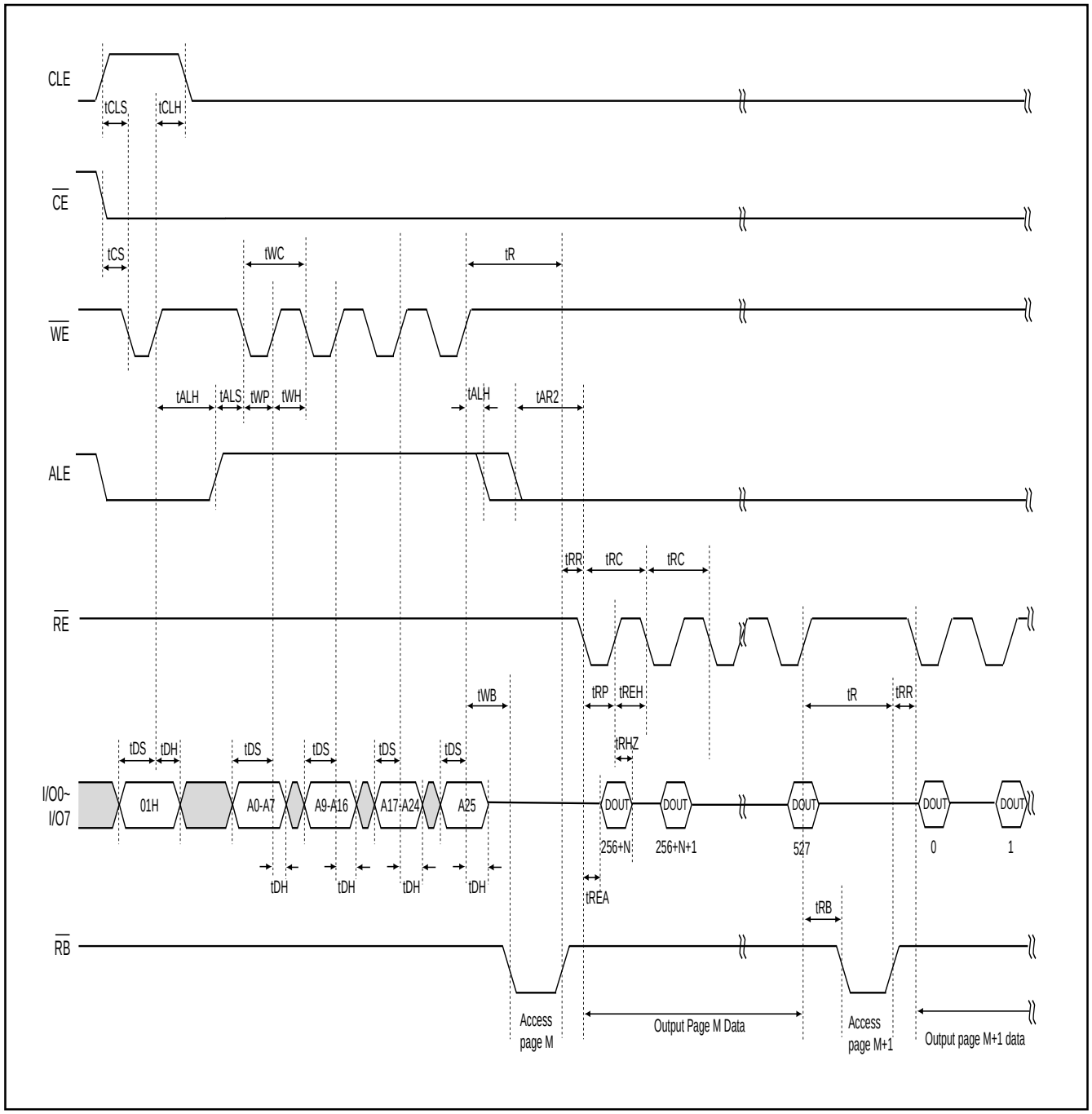


Remarks

1.Start address (SA) specification when read is performed with command 00H. N:0 to 255.

SEQUENTIAL READ CYCLE TIMING CHART(2)

(In case of read mode (2))

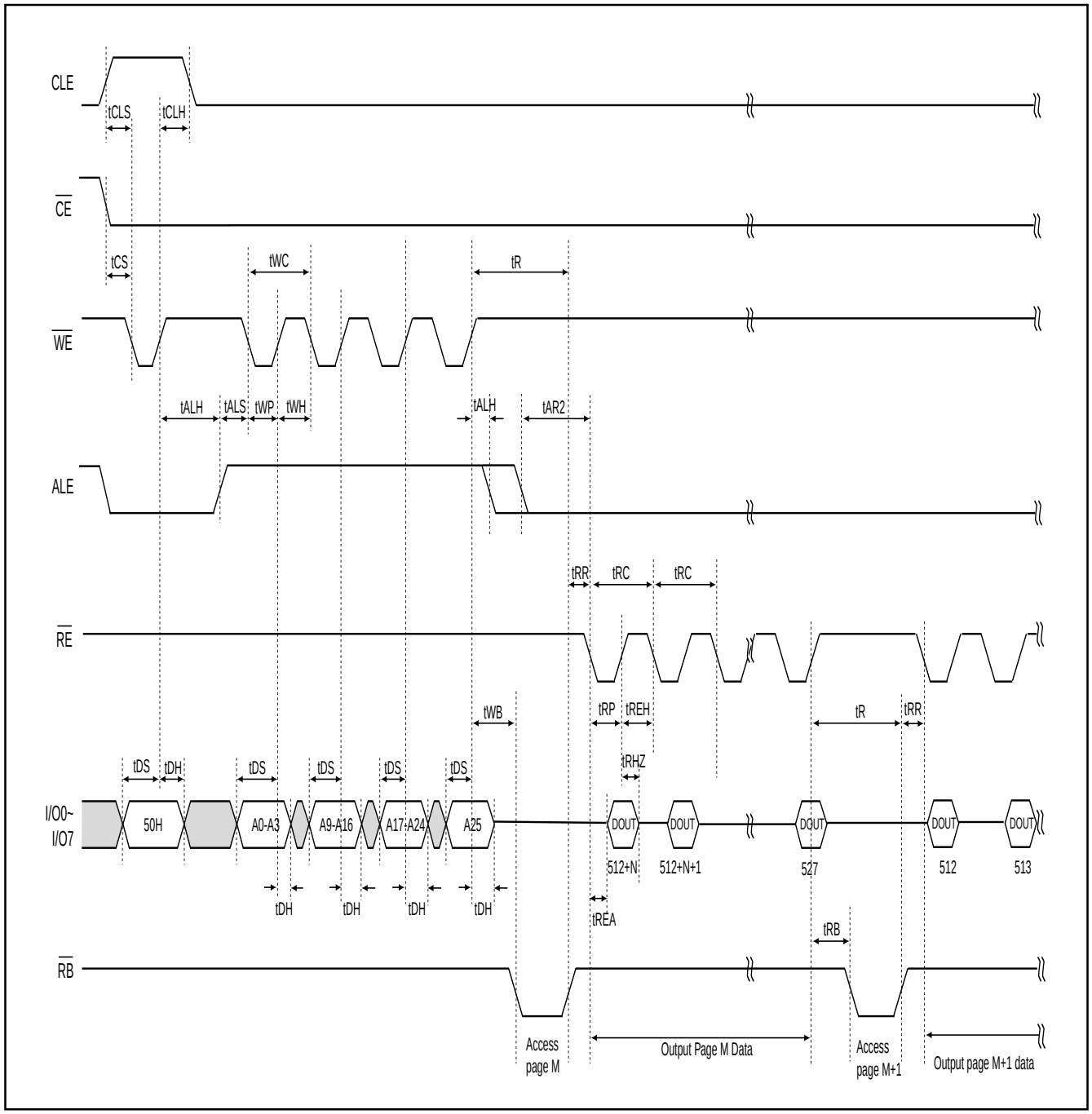


Remarks

1.Start address (SA) specification when read is performed with command 01H. N:0 to 255.

SEQUENTIAL READ CYCLE TIMING CHART(3)

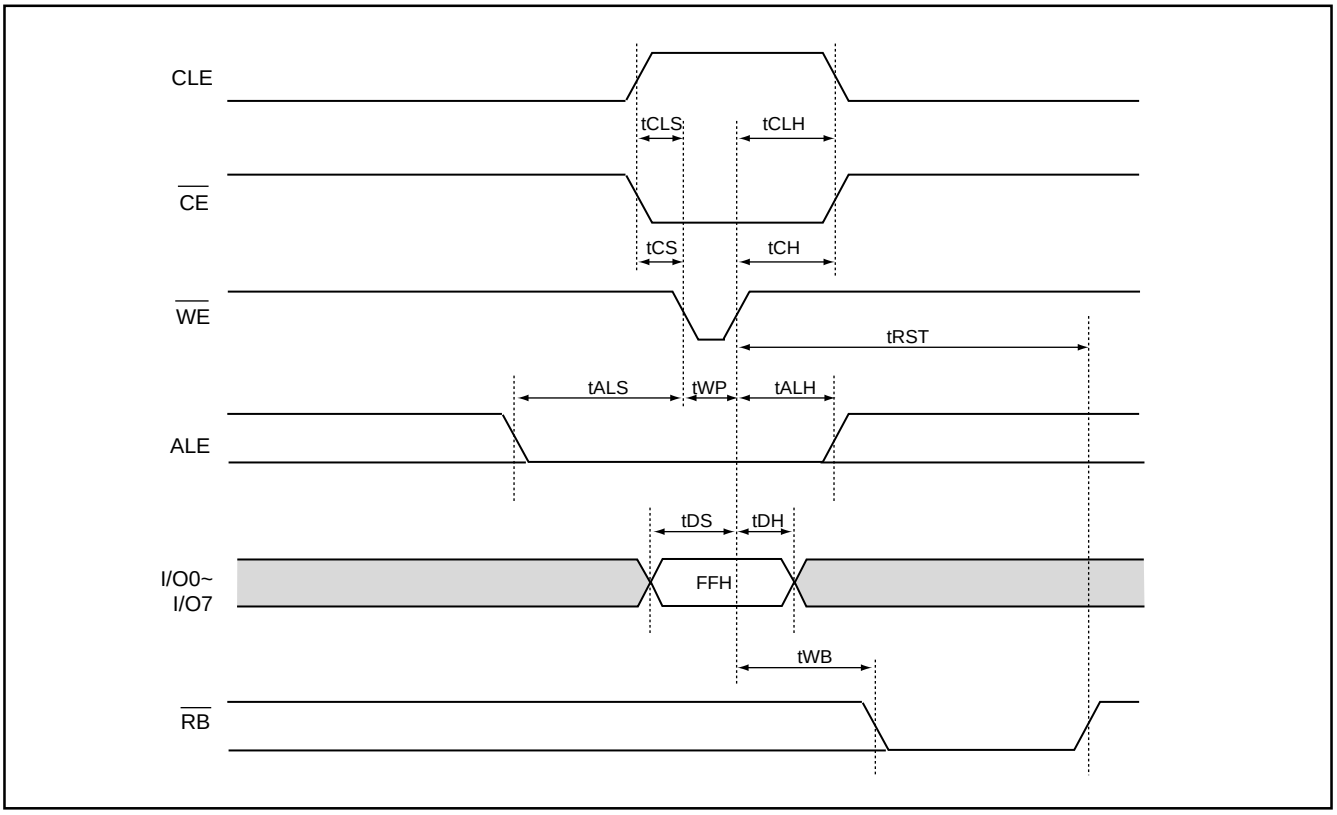
(In case of read mode (3))



Remarks

1.Start address (SA) specification when read is performed with command 50H. N:0 to 15.

Reset Cycle Timing Chart



[Usage Cautions]

(1) Rated operation
Operation using timing other than shown in the timing charts is not guaranteed.

(2) Commands that can be input
The only commands that can be input are 00H, 01H, 50H, and FFH. Do not input any other commands. If other commands are input, the subsequent operation is not guaranteed.

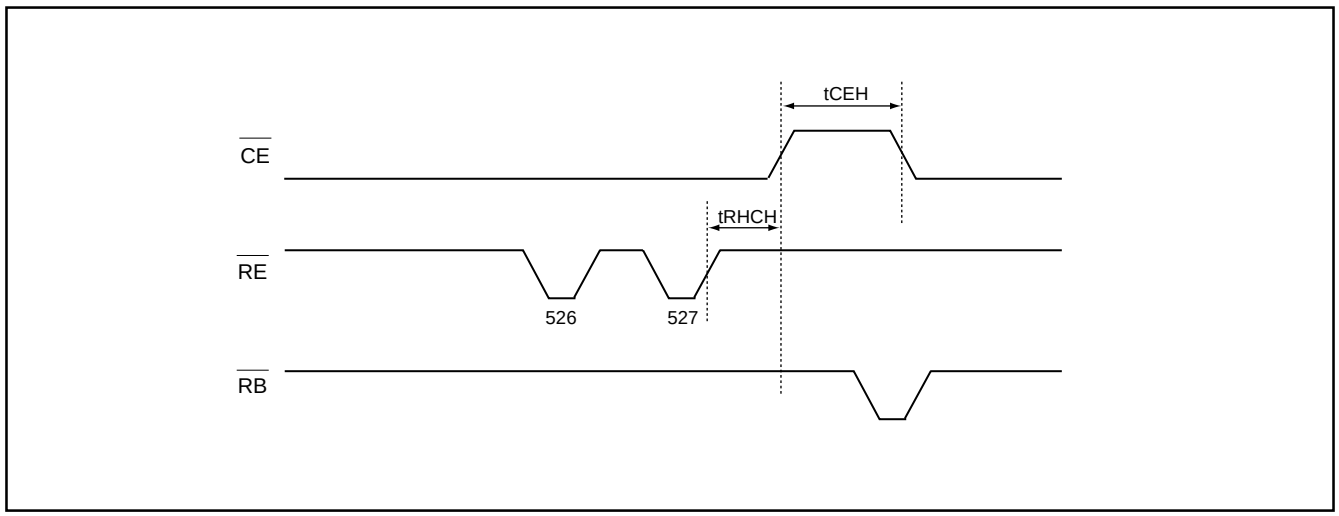
(3) Command limitations during Busy period
Do not input commands other than the reset command (FFH) during the Busy period. If a command is input during the Busy period, the subsequent operation is not guaranteed.

(4) Cautions regarding $\overline{RE}$ clock
- Following the last $\overline{RE}$ clock, do not input the $\overline{RE}$ clock until the $\overline{RB}$ pin changes from Busy to Ready.
- Do not input the $\overline{RE}$ clock other than during data output.

(5) Cautions upon power application
Since the state of the device is undetermined upon power on, input high level to the $\overline{CE}$ pin and execute the reset command following power on.

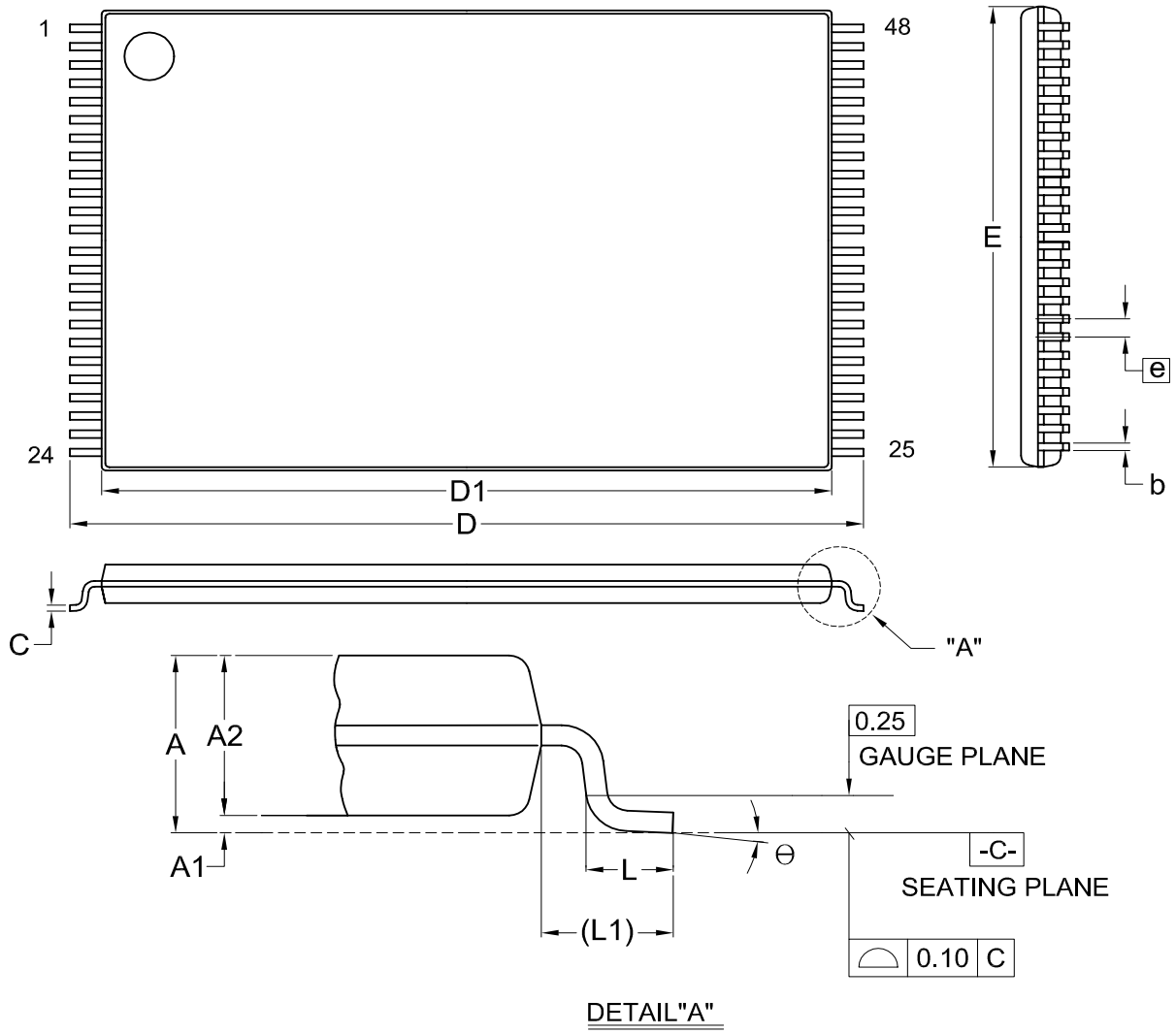
(6) Cautions during read mode
- Perform address input immediately following command input. If address input is done without performing command input first, the correct data cannot be output because the operation mode is undetermined.
- To execute the read mode after the read mode has been stopped with the reset command (FFH) and $\overline{CE}$, input again a command and address.

(7) Busy output following access of last address in page in read mode
After the access to the last address in a page, if the delay (tRHCH) from $\overline{RE}$ to $\overline{CE}$ is 30 ns or less, the Ready status is maintained and Busy is not output by keeping $\overline{CE}$ high level for a set period (tCEH).



PACKAGE INFORMATION

Title: **Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	7	MO-142			12-01-'03

REVISION HISTORY

Revision #	Description	Page	Date
1.0	1. Changed standby current from 100uA to 40uA	P1,6	AUG/16/2005
	2. Removed "Advanced Information"	P1	
1.1	1. Added "Order Information"	P1	SEP/06/2005
1.2	1. Removed tWHC	P7	OCT/28/2005
	2. Modified "Read cycle timing chart" and "Sequential read cycle timing chart"	P9~11 P13~15	

MACRONIX INTERNATIONAL CO., LTD.

Headquarters:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

Europe Office :
TEL:+32-2-456-8020
FAX:+32-2-456-8021

Hong Kong Office :
TEL:+86-755-834-335-79
FAX:+86-755-834-380-78

Japan Office :
Kawasaki Office :
TEL:+81-44-246-9100
FAX:+81-44-246-9105
Osaka Office :
TEL:+81-6-4807-5460
FAX:+81-6-4807-5461

Singapore Office :
TEL:+65-6346-5505
FAX:+65-6348-8096

Taipei Office :
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-262-8887
FAX:+1-408-262-8810

http : //www.macronix.com

MACRONIX INTERNATIONAL CO., LTD. reserves the right to change product and specifications without notice.