AvnetCore: Datasheet

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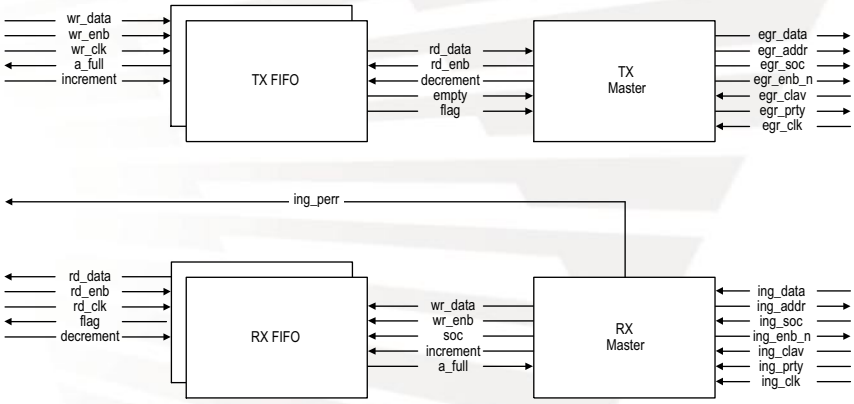
UTOPIA Level 2 Link



Block Diagram

UTOPIA (Universal Test and Operations PHY Interface for ATM) Level 2 defines the interface between the ATM or LINK layer and a Physical Layer (PHY) device. The UTOPIA level 2 standard defines a full duplex interface with a Master/Slave format. The Slave or LINK layer device responds to the requests from the PHY or Master device. The Master performs PHY arbitration and initiates data transfers to and from the Slave. The ATM forum has defined the UTOPIA Level 2 as either 8 or 16 bits in width, at up to 50MHz, supporting an OC12 channel at 622Mbps.

Intended Use:

- ATM Cell Processors
- ATM Switch Fabrics

Features:

- Function compatible with ATM Forum af-phy-0017.000 & af-phy-0039.000
- Asynchronous/synchronous FIFO using RAM
- Up to 31 PHYs supported
- 8/16 bit interfaces supported
- 52/54 byte cells supported
- Simple system side FIFO interface
- Simple system side FIFO interface

Targeted Devices:

- Axcelerator Family

Core Deliverables:

- Netlist Version
  - > Netlist compatible with the Actel Designer place and route tool
  - > Compiled RTL simulation model, compliant with the Actel Libero® environment
- RTL Version
  - > VHDL Source Code
- All
  - > User Guide
  - > Test Bench

Synthesis and Simulation Support:

- Synthesis: Synplicity
- Simulation: Model*Sim*
- Other tools supported upon request

Verification:

- Test Bench
- Test Vectors

Actel CompanionCore

AVNET Memec

Functional Description

This core conforms to the appropriate standard(s). In general, standards do not define the internal user interface, only the external interfaces and protocols. Therefore, Avnet Memec has created a simple FIFO interface to this core for easy user connectivity. This document describes this Avnet Memec created interface. Please consult the appropriate standards document for all external signaling.

TX MASTER

The TX master is responsible for polling the phys and internal queues in order to send cells to the slave device.

Signal	Width	Direction	Description
EGR_CLK	1	Input	25/50 MHz Utopia Clock for all registers in this block
EGR_DATA	8/16	Output	Utopia Data Bus. 8 or 16 bits selectable
EGR_ADDR	5	Output	Utopia Address Bus used for polling
EGR_SOC	1	Output	Utopia Start of Cell signal used to flag the first byte/word in the cell
EGR_ENB_N	1	Output	Utopia Enable signal used for selection
EGR_CLAV	1	Input	Utopia Cell Available signal used to indicate that the phy has room for a cell
EGR_PRTY	1	Output	Utopia Parity used for odd parity on EGR_DATA
RD_DATA	N*8/16	Input	Internal FIFO Bus
RD_ENB	N	Output	Internal FIFO Read Enable Signal
DECREMENT	N	Output	Internal signal used to decrement cell available counter
EMPTY	N	Input	Internal FIFO Empty flag
FLAG	N	Input	Internal signal used to indicate that there is a cell waiting to be sent for this queue

Table 1: TX Master Signal List

TX FIFO

The TX FIFO contains the RAM FIFO and the packet counter block. The packet counter is responsible for generating the cell available flags for the rest of the design. Every time a cell is written into the FIFO increment gets set and the cell count goes up, and when a cell is read decrement is set and the cell count goes down. The cell available “flag” is set when there is at least one cell in the FIFO that needs to be read. The FIFO operates in synchronous and asynchronous systems and can hold 9 cells. There is one FIFO per PHY polled.

Signal	Width	Direction	Description
WR_CLK	1	Input	System Clock for all registers in this block
WR_DATA	N*8/16	Input	Write data bus for FIFO
WR_ENB	N	Input	Write enable signal for FIFO
INCREMENT	N	Input	Increment signal for packet counter block
A_FULL	N	Output	Almost full for FIFO indicates that the FIFO does not have enough room for an additional cell.
RD_CLK	1	Input	Read clock for the FIFO = EGR_CLK for all read registers in this block
RD_DATA	N*8/16	Output	Read data bus for the FIFO
RD_ENB	N	Input	Read enable signal for the FIFO
DECREMENT	N	Input	Decrement signal for packet counter block
EMPTY	N	Output	Indicates when FIFO is empty

Table 2: TX FIFO Signal List

RX MASTER

The RX master is responsible for polling the PHYs and internal queues in order to send cells to the slave device.

Signal	Width	Direction	Description
ING_CLK	1	Input	25/50 MHz Utopia Clock for all registers in this block
ING_DATA	8/16	Input	Utopia Data Bus. 8 or 16 bits selectable
ING_ADDR	5	Output	Utopia Address Bus used for polling
ING_SOC	1	Input	Utopia Start of Cell signal used to flag the first byte/word in the cell
ING_ENB_N	1	Output	Utopia Enable signal used for selection
ING_CLAV	1	Input	Utopia Cell Available signal used to indicate that the phy has a cell is ready for transmission
ING_PRTY	1	Input	Utopia Parity used for odd parity on EGR_DATA
ING_PERR	N	Output	Internal signal used to indicate that a parity error was detected on ING_DATA
WR_DATA	N*8/16	Output	Internal FIFO Bus
WR_ENB	N	Output	Internal FIFO Write Enable Signal
INCREMENT	N	Output	Internal signal used to increment cell available counter
A_FULL	N	Input	Internal FIFO almost full flag indicates that the FIFO cannot accept another cell

Table 3: RX Master Signal List

RX FIFO

The RX FIFO contains the RAM FIFO and the packet counter block. The packet counter is responsible for generating the cell available flags for the rest of the design. Every time a cell is written into the FIFO increment gets set and the cell count goes up, and when a cell is read decrement is set and the cell count goes down. The cell available “flag” is set when there is at least one cell in the FIFO that needs to be read. The FIFO operates in synchronous and asynchronous systems and can hold 9 cells. There is one FIFO per PHY polled. If there is a SOC-SOC error the FIFO will discard all previous data and use the current data as the first byte in the new cell.

Signal	Width	Direction	Description
WR_CLK	1	Input	Write Clock for the FIFO = ING_CLK for all write registers in this block
WR_DATA	N*8/16	Input	Write data bus for FIFO
WR_ENB	N	Input	Write enable signal for FIFO
INCREMENT	N	Input	Increment signal for packet counter block
A_FULL	N	Output	Almost full for FIFO indicates that the FIFO does not have enough room for an additional cell.
RD_CLK	1	Input	System Clock for all read registers in this block
RD_DATA	N*8/16	Output	Read data bus for the FIFO
RD_ENB	N	Input	Read enable signal for the FIFO
DECREMENT	N	Input	Decrement signal for packet counter block
EMPTY	N	Output	Indicates when FIFO is Empty

Table 4: RX FIFO Signal List

DATA FORMATTING

The data will be written into the FIFO in 8/16 bit increments. If the 16-bit Utopia interface is selected then the MSB will be in bits (15:8) and the LSB will be in (7:0).

MSB (15:8)	LSB (7:0)

Figure 1: Data Formatting

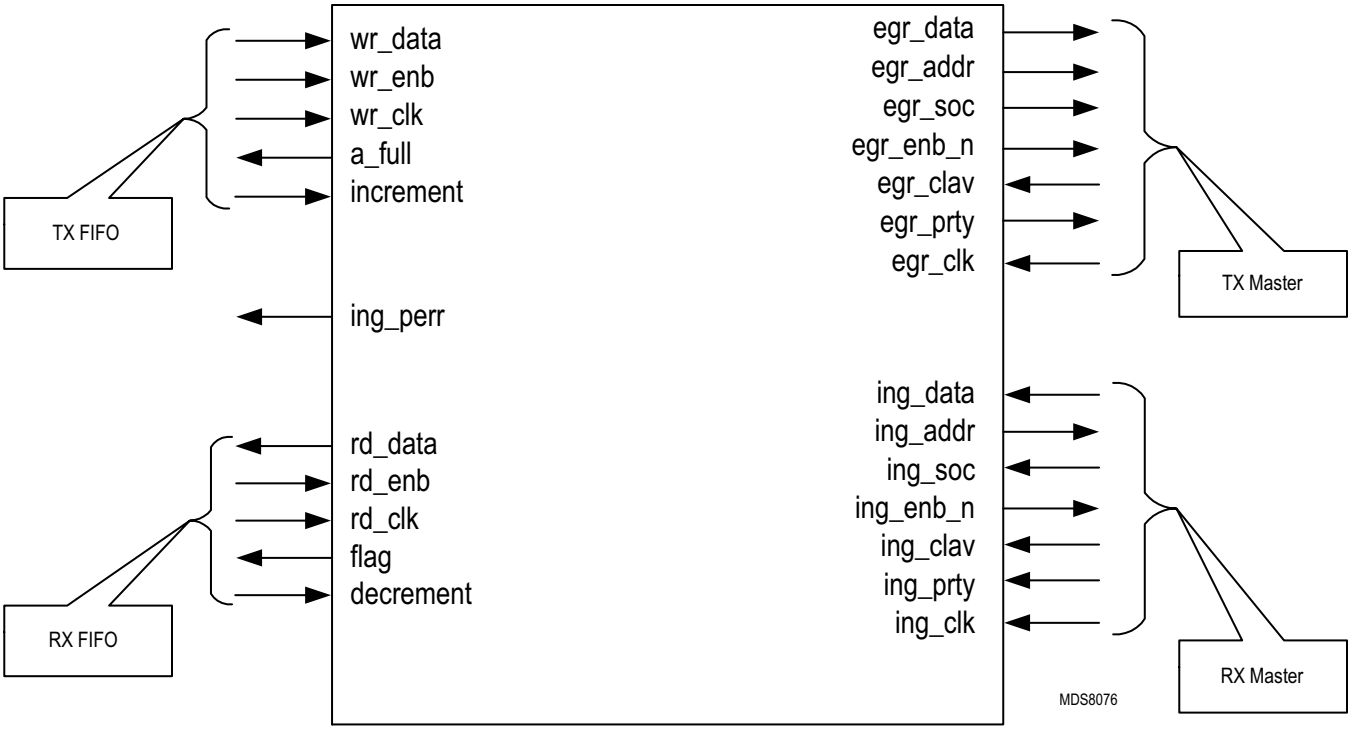


Figure 1: Logic Symbol

Device Requirements

MC-ACT-UL2LINK (UTOPIA Level 2 LINK Interface)					
Device	**Speed Ingress / Egress**	**C cells**	**R cells**	**Tiles**	**RAM's**
A3P250	88 / 88 MHz	-	-	1833 (30%)	4
APA075	77 / 62 MHz	-	-	2163 (70%)	8
AX125	108 / 98 MHz	812 (60%)	640 (95%)	-	4

Table 1: Device Utilization and Performance*

*Note: These numbers obtained with 1 channel and 16-bit data size.

Verification and Compliance

The testbench is self-checking, which means that if there is an error detected in the start word, end word, or payload the testbench will assert one or both of two error signals. This core has also been used successfully in customer designs.

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Width	Direction	Description
WR_DATA	N*8/16	Input	Write data bus for FIFO
WR_ENB	N	Input	Write enable signal for FIFO
WR_CLK	1	Input	System Clock for all registers in this block
A_FULL	N	Output	Almost full for FIFO indicates that the FIFO does not have enough room for an additional cell
INCREMENT	N	Input	Increment signal for packet counter block
ING_PERR	N	Output	Internal signal used to indicate that a parity error was detected on ING_DATA
RD_DATA	N*8/16	Output	Read data bus for the FIFO
RD_ENB	N	Input	Read enable signal for the FIFO
RD_CLK	1	Input	System Clock for all read registers in this block
FLAG	N	Output	Signal used to indicate that there is a cell waiting to be sent for this queue
DECREMENT	N	Input	Decrement signal for packet counter block
EGR_DATA	8/16	Output	Utopia Data Bus, 8 or 16 bits selectable
EGR_ADDR	5	Output	Utopia Address Bus used for polling
EGR_SOC	1	Output	Utopia Start of Cell signal used to flag the first byte/word in the cell
EGR_ENB_N	1	Output	Utopia Enable signal used for selection
EGR_CLAV	1	Input	Utopia Cell Available signal used to indicate that the PHY has room for a cell
EGR_PRTY	1	Output	Utopia Parity used for odd parity on EGR_DATA
EGR_CLK	1	Input	25/50 MHz Utopia Clock for all registers in this block
ING_DATA	8/16	Input	Utopia Data Bus, 8 or 16 bits selectable
ING_ADDR	5	Output	Utopia Address Bus used for polling
ING_SOC	1	Input	Utopia Start of Cell signal used to flag the first byte/word in the cell
ING_ENB_N	1	Output	Utopia Enable signal used for selection
ING_CLAV	1	Input	Utopia Cell Available signal used to indicate that the PHY has a cell is ready for transmission
ING_PRTY	1	Input	Utopia Parity used for odd parity on EGR_DATA
ING_CLK	1	Input	25/50 MHz Utopia Clock for all registers in this block

Table 2: Core I/O Signals

Timing

Since the ATM Forum specification fully defines the line side of the UTOPIA Level 2 interface, timing for that is not replicated here. Instead, only user (FIFO) interface timing information is presented here. The figure below shows the functional timing for FIFO reads and writes.

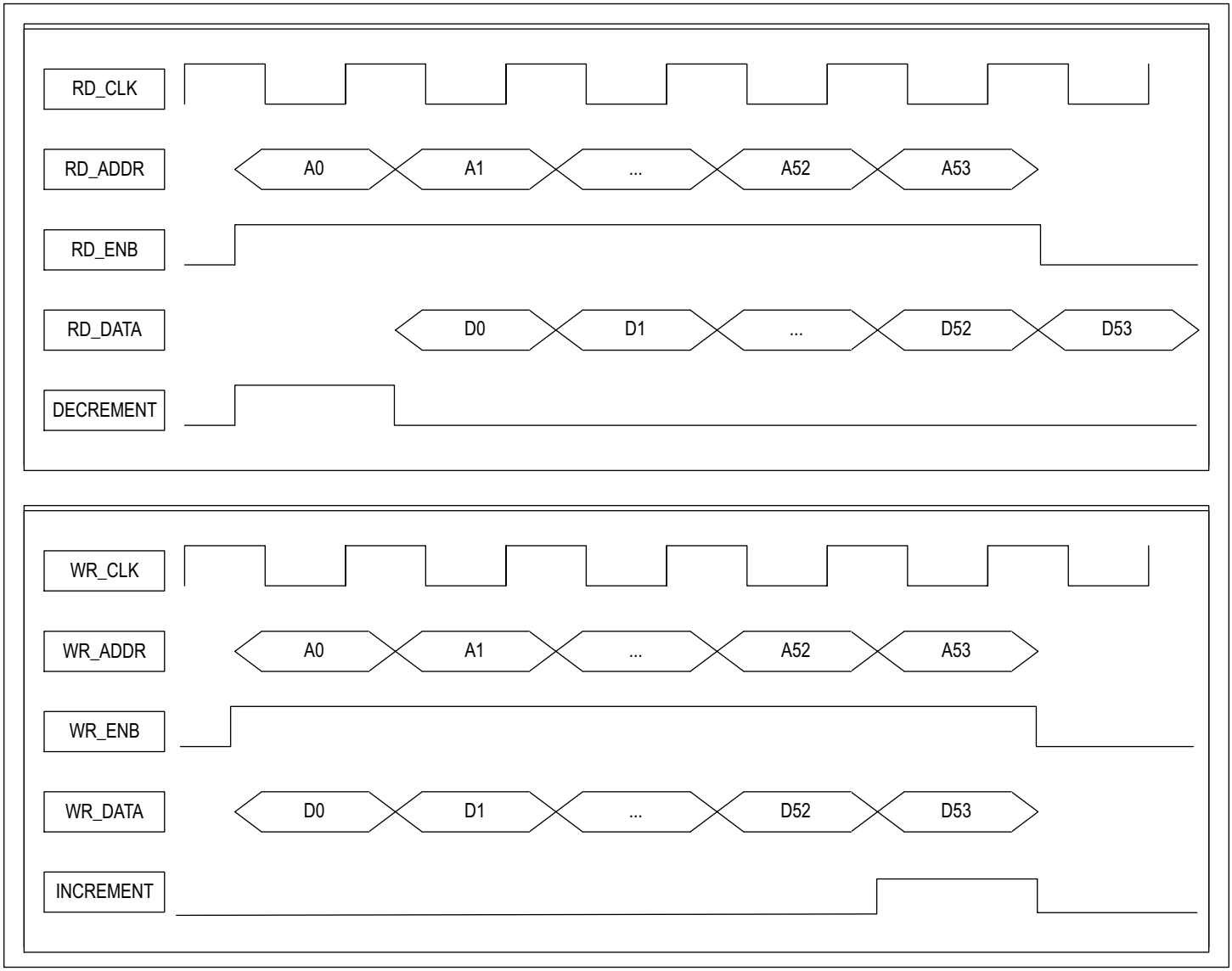


Figure 3: FIFO Timing

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero v2.2 Integrated Design Environment (IDE) and preferably with Synplify and Model*Sim*.

Ordering Information

The CORE is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

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Ordering Information:

Part Number	Hardware	Resale
MC-ACT-UL2LINK-NET	Actel UL2LINK Netlist	Contact for pricing
MC-ACT-UL2LINK-VHDL	Actel UL2LINK VHDL	Contact for pricing

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