2.5 V to 5.5 V, 115 µA, Parallel Interface Single Voltage-Output 8-/10-/12-Bit DACs

AD5330/AD5331/AD5340/AD5341

FEATURES

AD5330: single 8-bit DAC in 20-lead TSSOP
AD5331: single 10-bit DAC in 20-lead TSSOP
AD5340: single 12-bit DAC in 24-lead TSSOP
AD5341: single 12-bit DAC in 20-lead TSSOP
Low power operation: 115 µA @ 3 V, 140 µA @ 5 V
Power-down to 80 nA @ 3 V, 200 nA @ 5 V via $\overline{PD}$ Pin
2.5 V to 5.5 V power supply
Double-buffered input logic
Guaranteed monotonic by design over all codes
Buffered/unbuffered reference input options
Output range: 0 V to V_{REF} or 0 V to 2 × V_{REF}
Power-on reset to 0 V
Simultaneous update of DAC outputs via $\overline{LDAC}$ pin
Asynchronous $\overline{CLR}$ facility
Low power parallel data interface
On-chip rail-to-rail output buffer amplifiers
Temperature range: −40°C to +105°C

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators
Industrial process control

GENERAL DESCRIPTION

The AD5330/AD5331/AD5340/AD5341[1] are single 8-/10-/12-bit DACs. They operate from a 2.5 V to 5.5 V supply consuming just 115 µA at 3 V and feature a power-down mode that further reduces the current to 80 nA. The devices incorporate an on-chip output buffer that can drive the output to both supply rails, but the AD5330, AD5340, and AD5341 allow a choice of buffered or unbuffered reference input.

The AD5330/AD5331/AD5340/AD5341 have a parallel interface. $\overline{CS}$ selects the device and data is loaded into the input registers on the rising edge of $\overline{WR}$.

The GAIN pin allows the output range to be set at 0 V to V_{REF} or 0 V to 2 × V_{REF}.

Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the $\overline{LDAC}$ pin.

An asynchronous $\overline{CLR}$ input is also provided, which resets the contents of the input register and the DAC register to all zeros. These devices also incorporate a power-on reset circuit that ensures that the DAC output powers on to 0 V and remains there until valid data is written to the device.

The AD5330/AD5331/AD5340/AD5341 are available in thin shrink small outline packages (TSSOP).

[1] Protected by U.S. Patent Number 5,969,657.

FUNCTIONAL BLOCK DIAGRAM

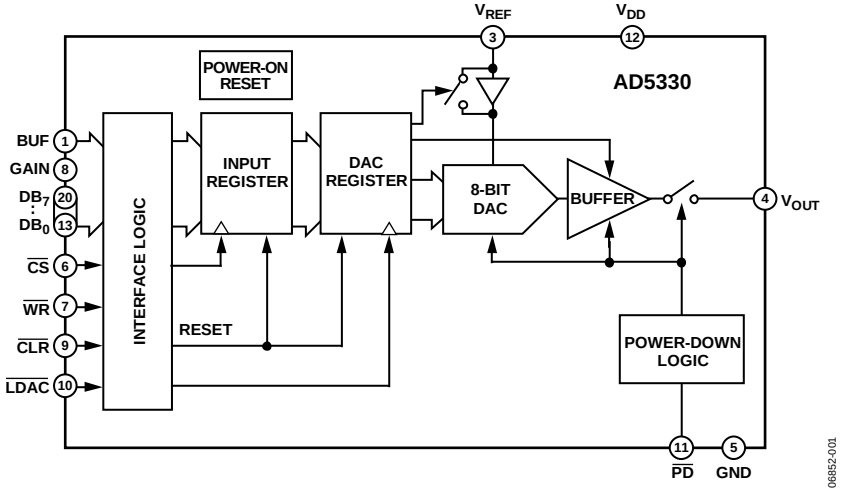


Figure 1. AD5330

Rev. A
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REVISION HISTORY

2/08—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Table 4 ... 16
Replaced Driving V_{DD} from the Reference Voltage Section ... 21
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 25

4/00—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 2 V, R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	B Version[2]				
Parameter[1]	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE[3, 4]					
AD5330					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes
AD5331					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed monotonic by design over all codes
AD5340/AD5341					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSBs	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	
Gain Error		±0.15	±1	% of FSR	
Lower Deadband[5]		10	60	mV	Lower deadband exists only if offset error is negative
Upper Deadband		10	60	mV	V_{DD} = 5 V; upper deadband exists only if $V_{REF} = V_{DD}$
Offset Error Drift[6]		−12		ppm of FSR/°C	
Gain Error Drift[6]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		−60		dB	ΔV_{DD} = ±10%
DAC REFERENCE INPUT[6]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference (AD5330, AD5340, and AD5341)
	0.25		V_{DD}	V	Unbuffered reference
V_{REF} Input Impedance		>10		MΩ	Buffered reference (AD5330, AD5340, and AD5341)
		180		kΩ	Unbuffered reference; gain = 1, input impedance = R_{DAC}
		90		kΩ	Unbuffered reference; gain = 2, input impedance = R_{DAC}
Reference Feedthrough		−90		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[6]					
Minimum Output Voltage[4, 7]		0.001		V min	Rail-to-rail operation
Maximum Output Voltage[4, 7]		V_{DD} − 0.001		V max	
DC Output Impedance		0.5		Ω	
Short-Circuit Current		25		mA	V_{DD} = 5 V
		15		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode; V_{DD} = 5 V
		5		µs	Coming out of power-down mode; V_{DD} = 3 V
LOGIC INPUTS[6]					
Input Current		±1		µA	
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 5 V ± 10%
			0.6	V	V_{DD} = 3 V ± 10%
			0.5	V	V_{DD} = 2.5 V
Input High Voltage, V_{IH}	2.4			V	V_{DD} = 5 V ± 10%
	2.1			V	V_{DD} = 3 V ± 10%
	2.0			V	V_{DD} = 2.5 V
Pin Capacitance		3		pF	

Parameter[1]	B Version[2] Min	Typ	Max	Unit	Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					DACs active and excluding load currents. Unbuffered
V_{DD} = 4.5 V to 5.5 V		140	250	μA	Reference, $V_{IH} = V_{DD}$, V_{IL} = GND
V_{DD} = 2.5 V to 3.6 V		115	200	μA	I_{DD} increases by 50 μA at $V_{REF} > V_{DD} - 100$ mV. In buffered mode, extra current is $(5 + V_{REF}/R_{DAC})$ μA, where R_{DAC} is the resistance of the resistor string.
I_{DD} (Power-Down Mode)					
V_{DD} = 4.5 V to 5.5 V		0.2	1	μA	
V_{DD} = 2.5 V to 3.6 V		0.08	1	μA	

[1] See the Terminology section.
[2] Temperature range: B Version: −40°C to +105°C; typical specifications are at 25°C.
[3] Linearity is tested using a reduced code range: AD5330 (Code 8 to Code 255); AD5331 (Code 28 to Code 1023); AD5340/AD5341 (Code 115 to Code 4095).
[4] DC specifications tested with output unloaded.
[5] This corresponds to x codes. x = deadband voltage/LSB size.
[6] Guaranteed by design and characterization, not production tested.
[7] For the amplifier output to reach its minimum voltage, offset error must be negative. For the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and offset plus gain error must be positive.

AC CHARACTERISTICS[1]

V_{DD} = 2.5 V to 5.5 V. R_L = 2 kΩ to GND, C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[2]	B Version[3] Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time					V_{REF} = 2 V; see Figure 29
AD5330		6	8	μs	¼ scale to ¾ scale change (0x40 to 0xC0)
AD5331		7	9	μs	¼ scale to ¾ scale change (0x100 to 0x300)
AD5340		8	10	μs	¼ scale to ¾ scale change (0x400 to 0xC00)
AD5341		8	10	μs	¼ scale to ¾ scale change (0x400 to 0xC00)
Slew Rate		0.7		V/μs	
Major Code Transition Glitch Energy		6		nV/s	1 LSB change around major carry
Digital Feedthrough		0.5		nV/s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p; unbuffered mode
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p; frequency = 10 kHz

[1] Guaranteed by design and characterization, not production tested.
[2] See the Terminology section.
[3] Temperature range: B Version: −40°C to +105°C; typical specifications are at 25°C.

TIMING CHARACTERISTICS[1, 2, 3]

V_{DD} = 2.5 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Condition/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time.
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ hold time.
t_3	20	ns min	$\overline{WR}$ pulse width.
t_4	5	ns min	Data, GAIN, BUF, HBEN setup time.
t_5	4.5	ns min	Data, GAIN, BUF, HBEN hold time.
t_6	5	ns min	Synchronous mode; $\overline{WR}$ falling to $\overline{LDAC}$ falling.
t_7	5	ns min	Synchronous mode; $\overline{LDAC}$ falling to $\overline{WR}$ rising.
t_8	4.5	ns min	Synchronous mode; $\overline{WR}$ rising to $\overline{LDAC}$ rising.
t_9	5	ns min	Asynchronous mode; $\overline{LDAC}$ rising to $\overline{WR}$ rising.
t_{10}	4.5	ns min	Asynchronous mode; $\overline{WR}$ rising to $\overline{LDAC}$ falling.
t_{11}	20	ns min	$\overline{LDAC}$ pulse width.
t_{12}	20	ns min	$\overline{CLR}$ pulse width.
t_{13}	50	ns min	Time between $\overline{WR}$ cycles.

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] See Figure 2.

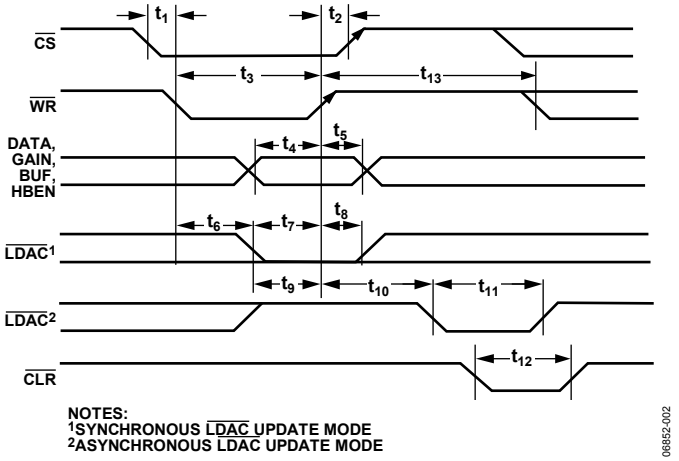


Figure 2. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$ mW
θ_{JA} Thermal Impedance (20-Lead TSSOP)[1]	85°C/W
θ_{JA} Thermal Impedance (24-Lead TSSOP)[1]	80°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec

[1] Thermal resistance (JEDEC 4-layer (2S2P) board).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

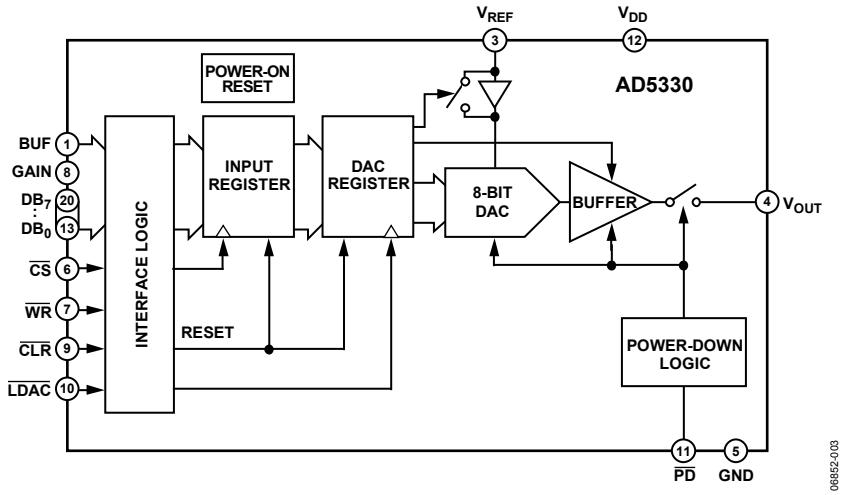


Figure 3. AD5330 Functional Block Diagram

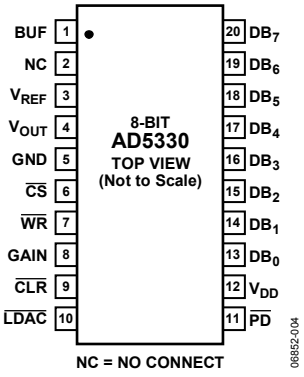


Figure 4. AD5330 Pin Configuration

Table 5. AD5330 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BUF	Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
2	NC	No Connect.
3	V_{REF}	Reference Input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to $2 \times V_{REF}$.
9	$\overline{CLR}$	Asynchronous active low control input that clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
13 to 20	DB_0 to DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.

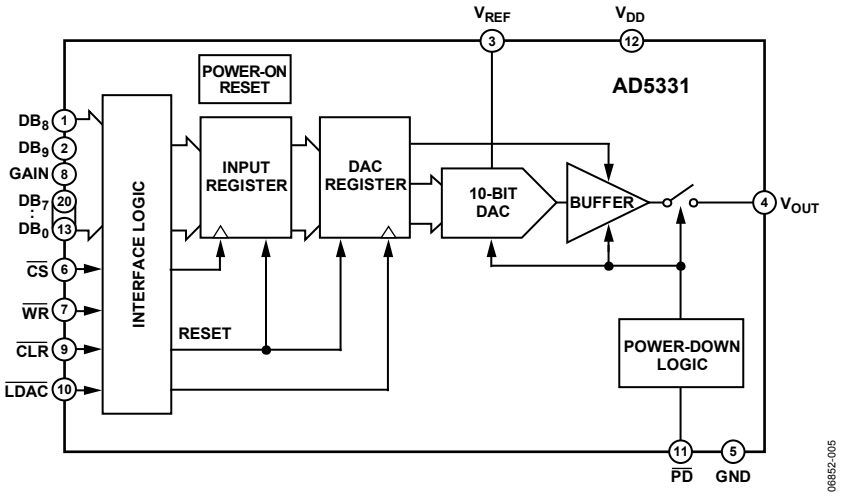


Figure 5. AD5331 Functional Block Diagram

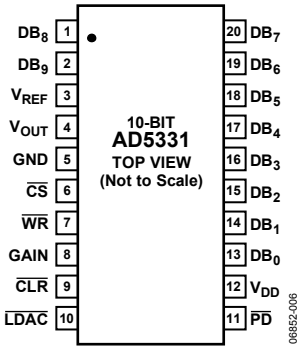


Figure 6. AD5331 Pin Configuration

Table 6. AD5331 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DB_8	Parallel Data Input.
2	DB_9	Most Significant Bit of Parallel Data Input.
3	V_{REF}	Unbuffered Reference Input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to $2 \times V_{REF}$.
9	$\overline{CLR}$	Active low control input that clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
13 to 20	DB_0 to DB_7	Eight Parallel Data Inputs.

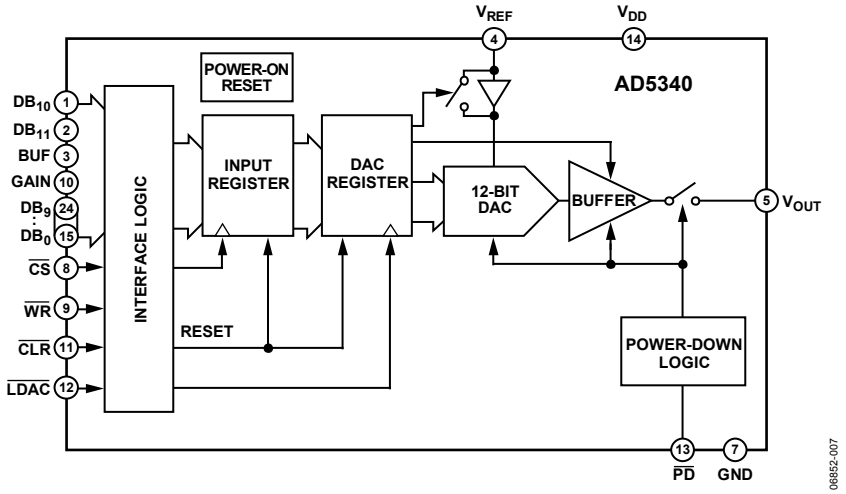


Figure 7. AD5340 Functional Block Diagram

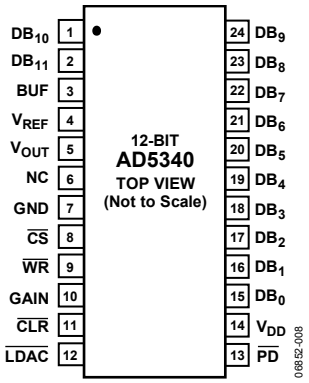


Figure 8. AD5340 Pin Configuration

Table 7. AD5340 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DB_{10}	Parallel Data Input.
2	DB_{11}	Most Significant Bit of Parallel Data Input.
3	BUF	Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
4	V_{REF}	Reference Input.
5	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
6	NC	No Connect.
7	GND	Ground reference point for all circuitry on the part.
8	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
9	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
10	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to $2 \times V_{REF}$.
11	$\overline{CLR}$	Asynchronous active low control input that clears all input registers and DAC registers to zero.
12	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
13	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
14	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
15 to 24	DB_0 to DB_9	Ten Parallel Data Inputs.

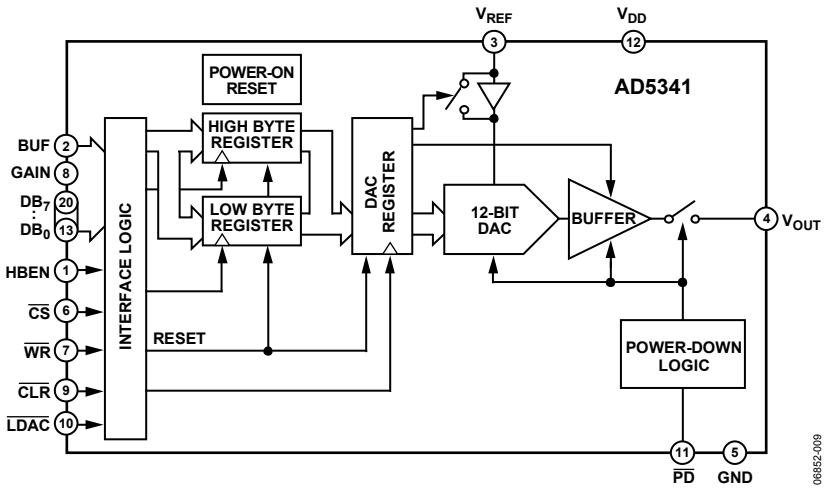


Figure 9. AD5341 Functional Block Diagram

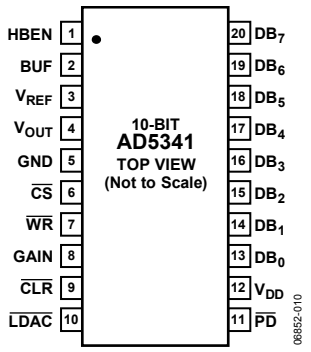


Figure 10. AD5341 Pin Configuration

Table 8. AD5341 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	HBEN	High Byte Enable Pin. This pin is used when writing to the device to determine if data is written to the high byte register or the low byte register.
2	BUF	Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
3	V_{REF}	Reference Input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}.
9	$\overline{CLR}$	Asynchronous active low control input that clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
13 to 20	DB_0 to DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. Typical INL vs. code plots can be seen in Figure 14, Figure 15, and Figure 16.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL vs. code plots can be seen in Figure 17, Figure 18, and Figure 19.

Gain Error
This is a measure of the span error of the DAC (including any error in the gain of the buffer amplifier). It is the deviation in slope of the actual DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range. This is illustrated in Figure 11.

Offset Error
This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range. If the offset voltage is positive, the output voltage is still positive at zero input code. This is shown in Figure 12. Because the DACs operate from a single supply, a negative offset cannot appear at the output of the buffer amplifier. Instead, there is a code close to zero at which the amplifier output saturates (amplifier footroom). Below this code, there is a deadband over which the output voltage does not change. This is illustrated in Figure 13.

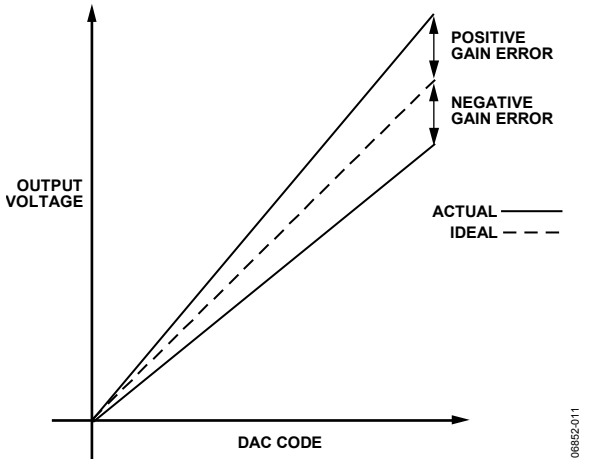


Figure 11. Gain Error

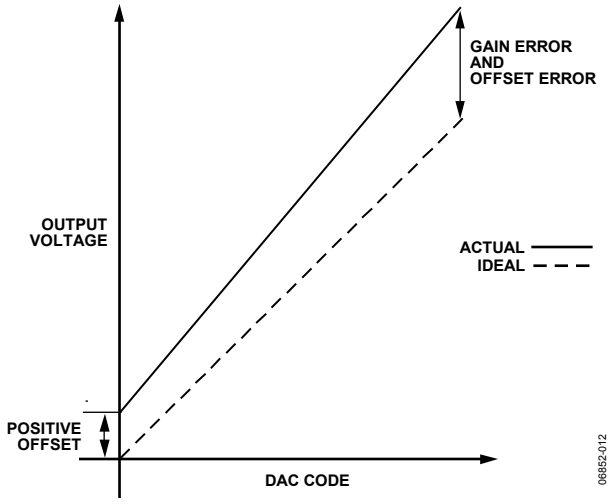


Figure 12. Positive Offset Error and Gain Error

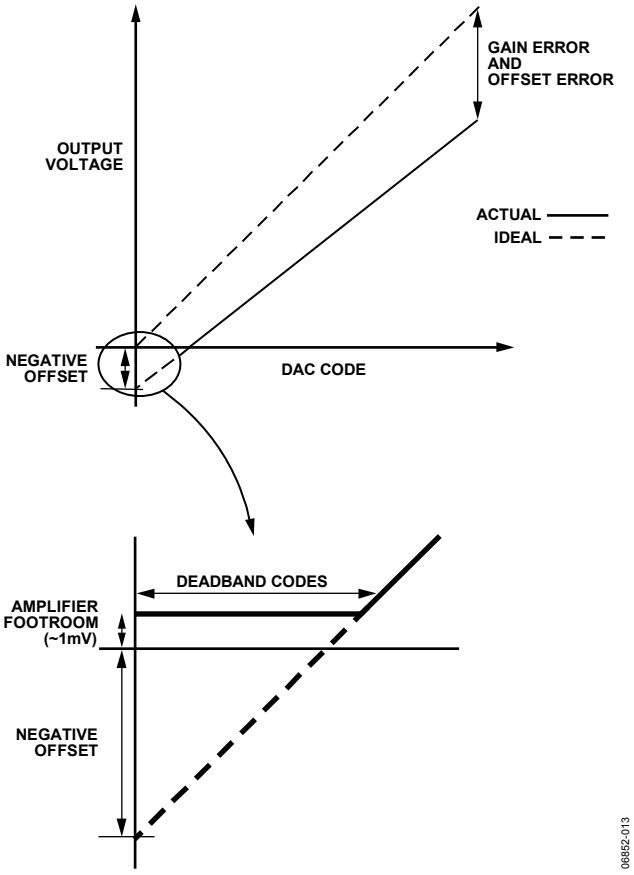


Figure 13. Negative Offset Error and Gain Error

Offset Error Drift
This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Power-Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

Reference Feedthrough
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Major-Code Transition Glitch Energy
Major-code transition glitch energy is the energy of the impulse injected into the analog output when the DAC changes state. It is normally specified as the area of the glitch in nV/s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 … 11 to 100 … 00 or 100 … 00 to 011 … 11).

Digital Feedthrough
Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device; it is measured when the DAC is not being written to ($\overline{\text{CS}}$ held high). It is specified in nV/s and is measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s and vice versa.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with a full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

TYPICAL PERFORMANCE CHARACTERISTICS

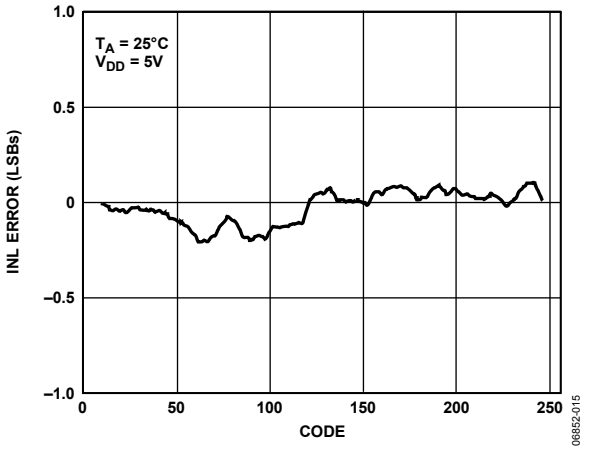


Figure 14. AD5330 Typical INL Plot

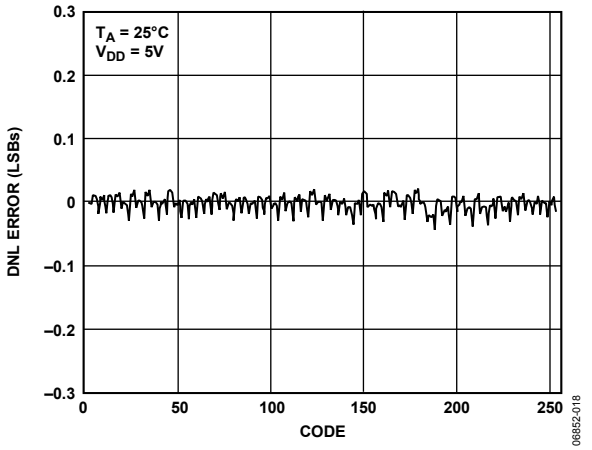


Figure 17. AD5330 Typical DNL Plot

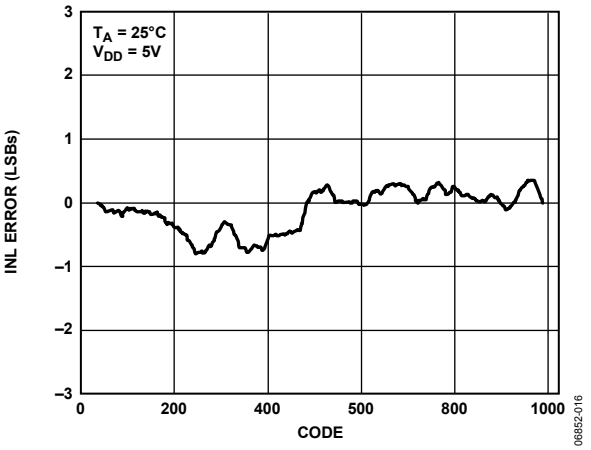


Figure 15. AD5331 Typical INL Plot

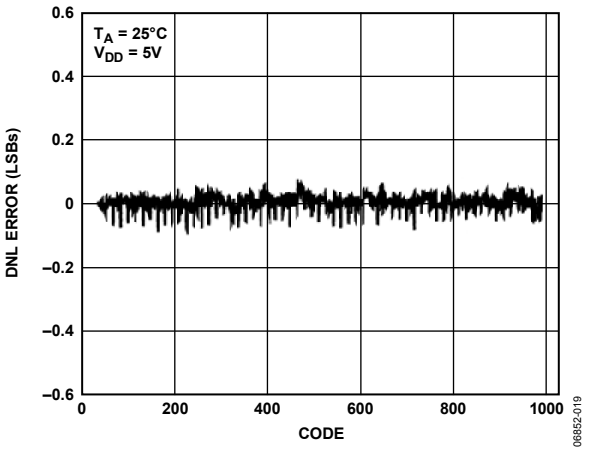


Figure 18. AD5331 Typical DNL Plot

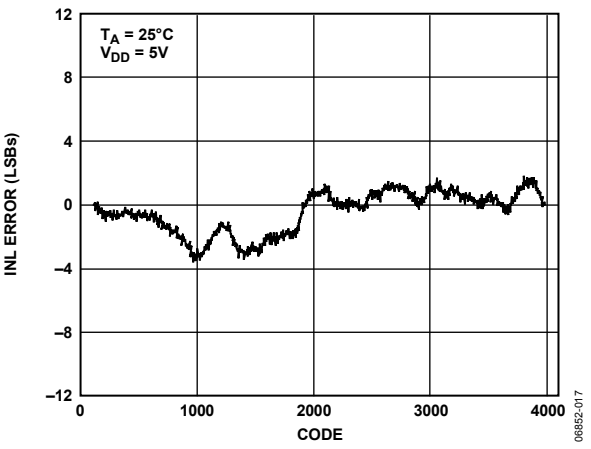


Figure 16. AD5340/AD5341 Typical INL Plot

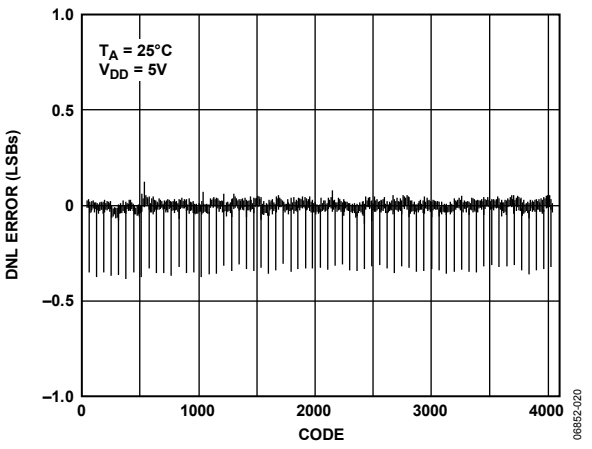


Figure 19. AD5340/AD5341 Typical DNL Plot

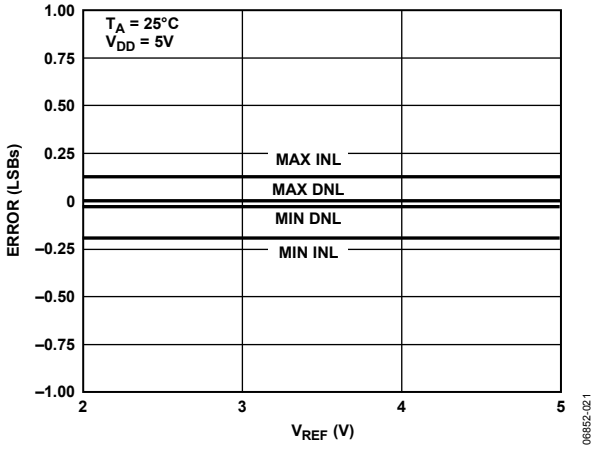


Figure 20. AD5330 INL and DNL Error vs. V_{REF}

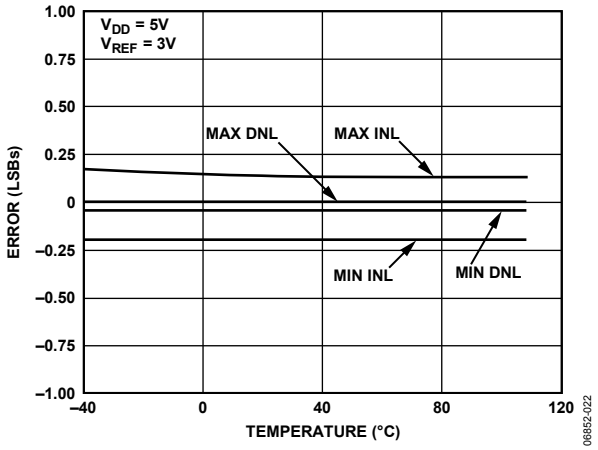


Figure 21. AD5330 INL Error and DNL Error vs. Temperature

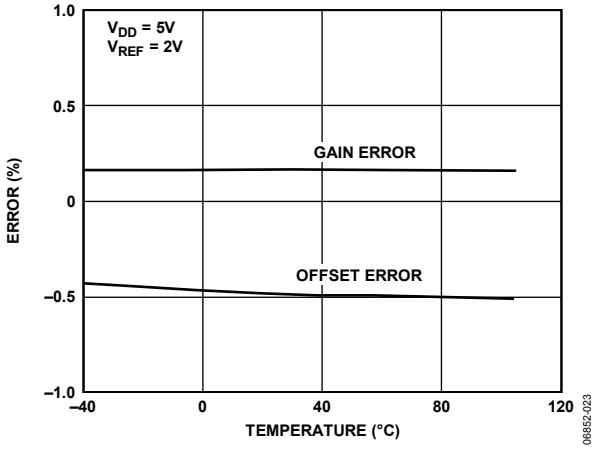


Figure 22. AD5330 Offset Error and Gain Error vs. Temperature

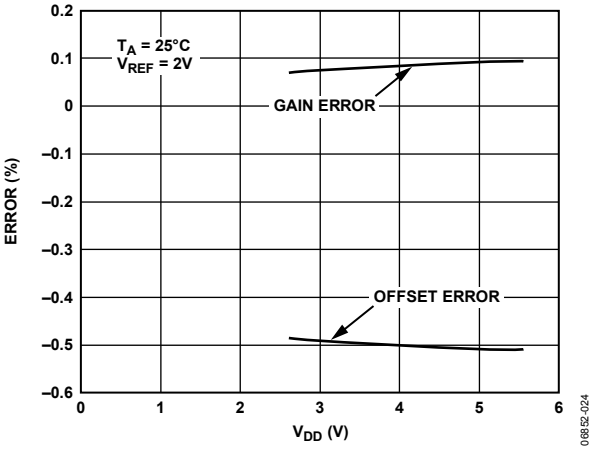


Figure 23. Offset Error and Gain Error vs. V_{DD}

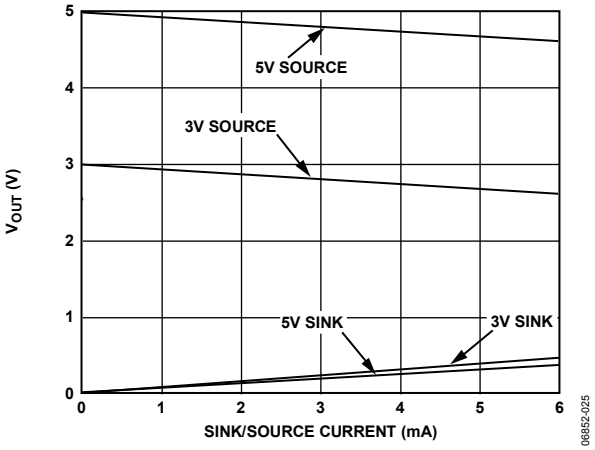


Figure 24. V_{OUT} Source and Sink Current Capability

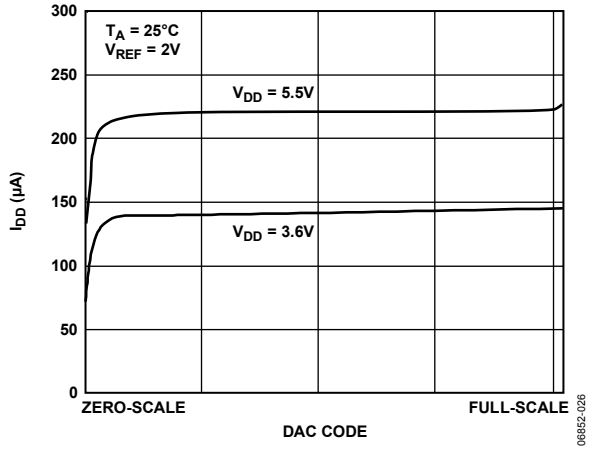


Figure 25. Supply Current vs. DAC Code

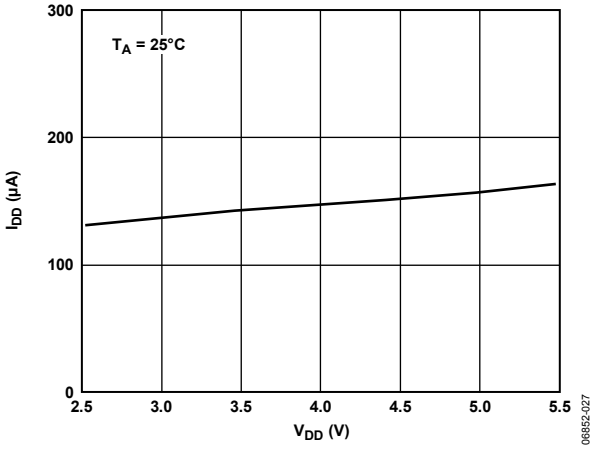


Figure 26. Supply Current vs. Supply Voltage

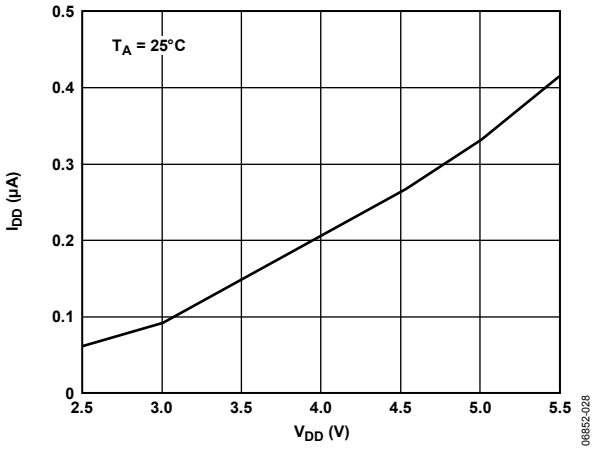


Figure 27. Power-Down Current vs. Supply Voltage

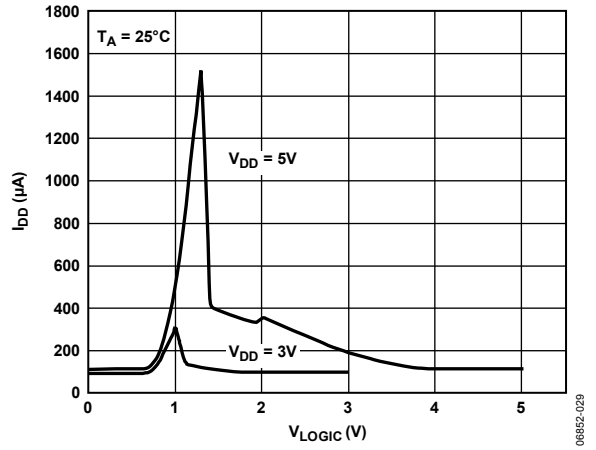


Figure 28. Supply Current vs. Logic Input Voltage

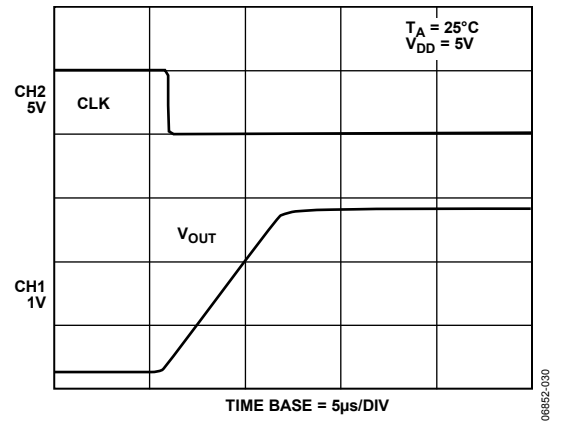


Figure 29. Half-Scale Settling (¼ to ¾ Scale Code Change)

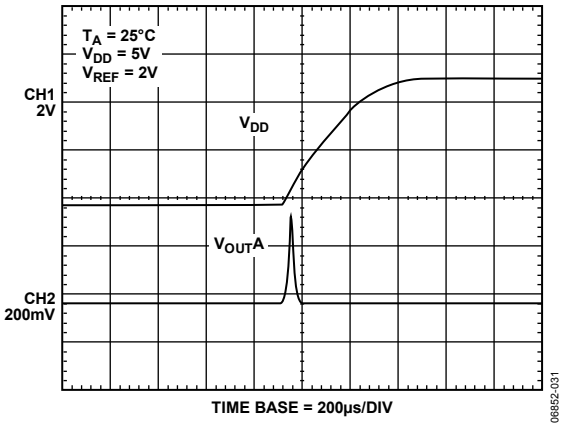


Figure 30. Power-On Reset to 0 V

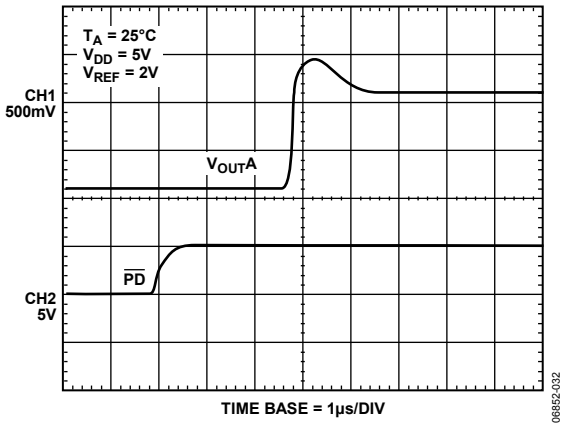


Figure 31. Exiting Power-Down to Midscale

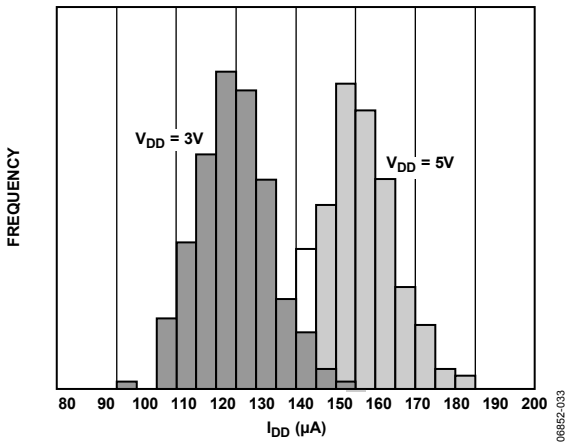


Figure 32. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

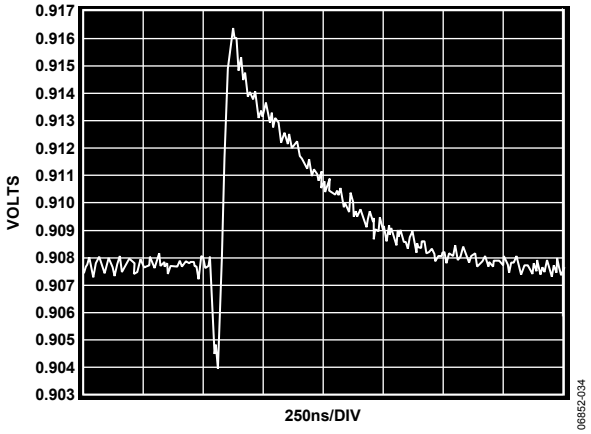


Figure 33. AD5340 Major-Code Transition Glitch Energy

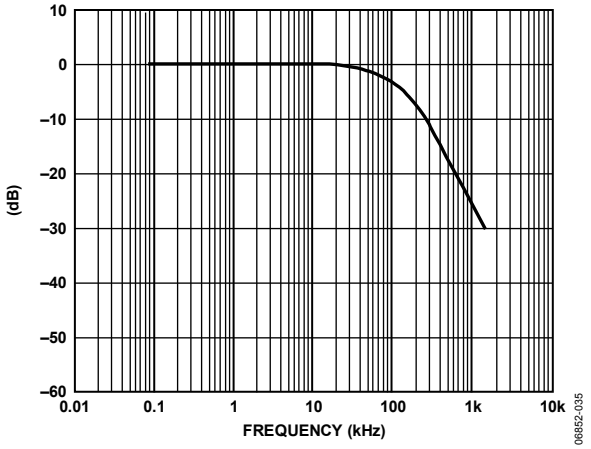


Figure 34. Multiplying Bandwidth (Small-Signal Frequency Response)

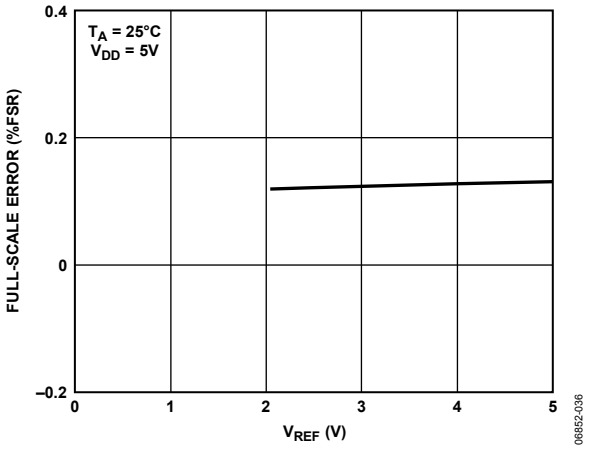


Figure 35. Full-Scale Error vs. V_{REF}

THEORY OF OPERATION

The AD5330/AD5331/AD5340/AD5341 are single resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits, respectively. They are written to using a parallel interface. They operate from single supplies of 2.5 V to 5.5 V and the output buffer amplifiers offer rail-to-rail output swing. The AD5330, AD5340, and AD5341 have a reference input that can be buffered to draw virtually no current from the reference source. The reference input of the AD5331 is unbuffered. The devices have a power-down feature that reduces current consumption to only 80 nA @ 3 V.

DIGITAL-TO-ANALOG SECTION

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 36 shows a block diagram of the DAC architecture. Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \times Gain$$

where:
D is the decimal equivalent of the binary code, which is loaded to the DAC register:

0 to 255 for AD5330 (8 Bits)
0 to 1023 for AD5331 (10 Bits)
0 to 4095 for AD5340/AD5341 (12 Bits)

N is the DAC resolution.
Gain is the output amplifier gain (1 or 2).

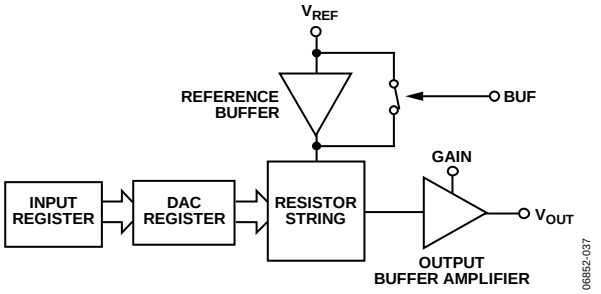


Figure 36. Single DAC Channel Architecture

RESISTOR STRING

The resistor-string section is shown in Figure 37. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

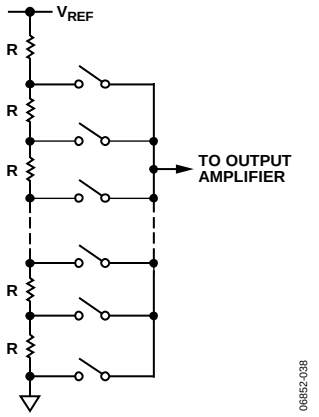


Figure 37. Resistor String

DAC REFERENCE INPUT

There is a reference input pin for the DAC. The reference input is buffered on the AD5330, AD5340, and AD5341 but can be configured as unbuffered also. The reference input of the AD5331 is unbuffered. The buffered/unbuffered option is controlled by the BUF pin.

In buffered mode (BUF = 1), the current drawn from an external reference voltage is virtually zero because the impedance is at least 10 MΩ. The reference input range is 1 V to 5 V with a 5 V supply.

In unbuffered mode (BUF = 0), the user can have a reference voltage as low as 0.25 V and as high as V_{DD} because there is no restriction due to headroom and footroom of the reference amplifier. The impedance is still large at typically 180 kΩ for 0 V to V_{REF} mode and 90 kΩ for 0 V to 2 × V_{REF} mode. If there is an external buffered reference (for example, REF192), there is no need to use the on-chip buffer.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on V_{REF}, GAIN, the load on V_{OUT}, and offset error.

If a gain of 1 is selected (GAIN = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (GAIN = 1), the output range is 0.001 V to 2 × V_{REF}. However, because of clamping, the maximum output is limited to V_{DD} – 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or 2 kΩ to V_{DD} in parallel with 500 pF to GND or 500 pF to V_{DD}. The source and sink capabilities of the output amplifier can be seen in Figure 24.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at eight bits) of 6 μs with the output unloaded (see Figure 29).

PARALLEL INTERFACE

The AD5330, AD5331, and AD5340 load their data as a single 8-, 10-, or 12-bit word, while the AD5341 loads data as a low byte of eight bits and a high byte containing four bits.

DOUBLE-BUFFERED INTERFACE

The AD5330/AD5331/AD5340/AD5341 DACs all have double-buffered interfaces consisting of an input register and a DAC register. DAC data, BUF, and GAIN inputs are written to the input register under the control of chip select ($\overline{CS}$) and write ($\overline{WR}$).

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register may change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it. The gain and buffer control signals are also double-buffered and are only updated when $\overline{LDAC}$ is taken low.

Double-buffering is also useful where the DAC data is loaded in two bytes, as in the AD5341, because it allows the whole data word to be assembled in parallel before updating the DAC register. This prevents spurious outputs that can occur if the DAC register is updated with only the high byte or the low byte.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC register is filled with the contents of the input register. In the case of the AD5330/AD5331/AD5340/AD5341, the parts only update the DAC register if the input register has been changed since the last time the DAC register was updated. This removes unnecessary crosstalk.

CLEAR INPUT ($\overline{CLR}$)

$\overline{CLR}$ is an active low, asynchronous clear that resets the input and DAC registers.

CHIP SELECT INPUT ($\overline{CS}$)

$\overline{CS}$ is an active low input that selects the device.

WRITE INPUT ($\overline{WR}$)

$\overline{WR}$ is an active low input that controls writing of data to the device. Data is latched into the input register on the rising edge of $\overline{WR}$.

LOAD DAC INPUT ($\overline{LDAC}$)

$\overline{LDAC}$ transfers data from the input register to the DAC register (and therefore updates the outputs). Use of the $\overline{LDAC}$ function enables double-buffering of the DAC data, GAIN, and BUF. There are two $\overline{LDAC}$ modes: synchronous mode and asynchronous mode.

In synchronous mode, the DAC register is updated after new data is read in on the rising edge of the $\overline{WR}$ input. $\overline{LDAC}$ can be tied permanently low or pulsed, as shown in Figure 2.

In asynchronous mode, the outputs are not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low, the DAC register is updated with the contents of the input register.

HIGH BYTE ENABLE INPUT (HBEN)

High byte enable is a control input on the AD5341 only. It determines if data is written to the high byte input register or the low byte input register.

The low data byte of the AD5341 consists of Data Bits [0:7] at the data inputs DB_0 to DB_7, whereas the high byte consists of Data Bits [8:11] at the data inputs DB_0 to DB_3, as shown in Figure 38. DB_4 to DB_7 are ignored during a high byte write, but they can be used for data to set up the reference input as buffered/unbuffered, and buffer amplifier gain (see Figure 42).



Figure 38. Data Format for AD5341

POWER-ON RESET

The AD5330/AD5331/AD5340/AD5341 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is

- Normal operation
- Reference input unbuffered
- 0 V to V_{REF} output range
- Output voltage set to 0 V

Both input and DAC registers are filled with zeros and remain as such until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

POWER-DOWN MODE

The AD5330/AD5331/AD5340/AD5341 have low power consumption, dissipating only 0.35 mW with a 3 V supply and 0.7 mW with a 5 V supply. Power consumption can be further reduced when the DAC is not in use by putting it into power-down mode, which is selected by taking Pin $\overline{PD}$ low.

When the $\overline{PD}$ pin is high, the DAC works normally with a typical power consumption of 140 μA at 5 V (115 μA at 3 V). In power-down mode, however, the supply current falls to 200 nA at 5 V (80 nA at 3 V) when the DAC is powered down. Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the output is three-state while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. The output stage is illustrated in Figure 39.

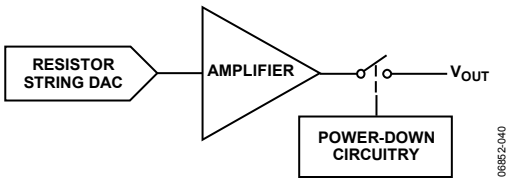


Figure 39. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs when V_{DD} = 3 V. This is the time from a rising edge on the $\overline{PD}$ pin to when the output voltage deviates from its power-down voltage (see Figure 31).

Table 9. AD5330/AD5331/AD5340 Truth Table[1]

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	Function
1	1	1	X	No data transfer
1	1	X	1	No data transfer
0	X	X	X	Clear all registers
1	1	0	0→1	Load input register
1	0	0	0→1	Load input register and DAC register
1	0	X	X	Update DAC register

[1] X = don't care.

Table 10. AD5341 Truth Table[1]

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	HBEN	Function
1	1	1	X	X	No data transfer
1	1	X	1	X	No data transfer
0	X	X	X	X	Clear all registers
1	1	0	0→1	0	Load low byte input register
1	1	0	0→1	1	Load high byte input register
1	0	0	0→1	0	Load low byte input register and DAC register
1	0	0	0→1	1	Load high byte input register and DAC register
1	0	X	X	X	Update DAC register

[1] X = don't care.

SUGGESTED DATABUS FORMATS

In most applications, GAIN and BUF are hard-wired. However, if more flexibility is required, they can be included in a databus. This enables the user to software program GAIN, giving the option of doubling the resolution in the lower half of the DAC range. In a bused system, GAIN and BUF can be treated as data inputs because they are written to the device during a write operation and take effect when $\overline{\text{LDAC}}$ is taken low. This means that the reference buffers and the output amplifier gain of multiple DAC devices can be controlled using common GAIN and BUF lines.

In the case of the AD5330, this means that the databus must be wider than eight bits. The AD5331 and AD5340 databuses must be at least 10 bits and 12 bits wide, respectively, and are best suited to a 16-bit databus system.

Examples of data formats for putting GAIN and BUF on a 16-bit databus are shown in Figure 40. Note that any unused bits above the actual DAC data can be used for BUF and GAIN. DAC devices can be controlled using common GAIN and BUF lines.

AD5330

BUF	GAIN	X	X	X	X	X	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

AD5331

BUF	GAIN	X	X	X	X	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

AD5340

BUF	GAIN	X	X	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

X = UNUSED BIT

06852-041

Figure 40. GAIN and BUF Data on a 16-Bit Bus

The AD5341 is a 12-bit device that uses byte load, so only four bits of the high byte are actually used as data. Two of the unused bits can be used for GAIN and BUF data by connecting them to the GAIN and BUF inputs; for example, Bit 6 and Bit 7, as shown in Figure 41 and Figure 42.

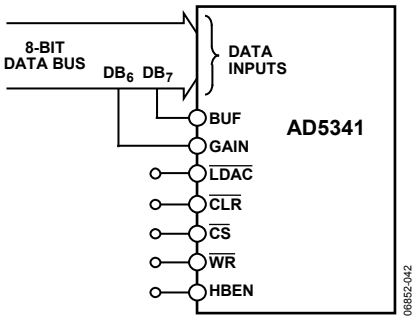


Figure 41. AD5341 Data Format for Byte Load with GAIN and BUF Data on 8-Bit Bus

In this case, the low byte is written to first in a write operation with HBEN = 0. Bit 6 and Bit 7 of DAC data are written into GAIN and BUF registers but have no effect. The high byte is then written to. Only the lower four bits of data are written into the DAC high byte register, so Bit 6 and Bit 7 can be GAIN and BUF data.

$\overline{\text{LDAC}}$ is used to update the DAC, GAIN, and BUF values.

HIGH BYTE

BUF	GAIN	X	X	DB_{11}	DB_{10}	DB_9	DB_8

LOW BYTE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

X = UNUSED BIT

06852-043

Figure 42. AD5341 with GAIN and BUF Data on 8-Bit Bus

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUITS

The AD5330/AD5331/AD5340/AD5341 can be used with a wide range of reference voltages, especially if the reference inputs are configured to be unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of 0.25 V to V_{DD}. More typically, these devices can be used with a fixed, precision reference voltage. Figure 43 shows a typical setup for the devices when using an external reference connected to the unbuffered reference inputs. If the reference inputs are unbuffered, the reference input range is from 0.25 V to V_{DD}, but if the on-chip reference buffers are used, the reference range is reduced. Suitable references for 5 V operation are the AD780 and REF192. For 2.5 V operation, a suitable external reference is the AD589, a 1.23 V band gap reference.

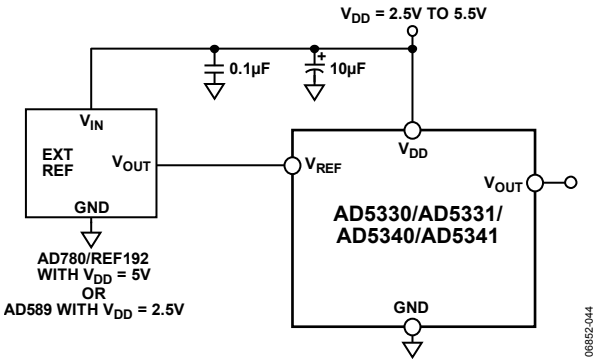


Figure 43. AD5330/AD5331/AD5340/AD5341 Using External Reference

DRIVING V_{DD} FROM THE REFERENCE VOLTAGE

If an output range of 0 V to V_{DD} is required, the simplest solution is to connect the reference inputs to V_{DD}. Because this supply may not be very accurate and may be noisy, the devices can be powered from the reference voltage, for example using a 5 V reference such as the ADP667, as shown in Figure 44.

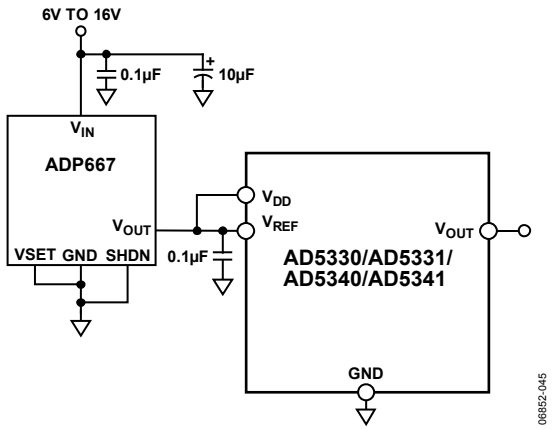


Figure 44. Using an ADP667 as Power and Reference to AD5330/AD5331/AD5340/AD5341

BIPOLAR OPERATION USING THE AD5330/AD5331/ AD5340/AD5341

The AD5330/AD5331/AD5340/AD5341 are designed for single-supply operation, but bipolar operation is achievable using the circuit shown in Figure 45. The circuit shown has been configured to achieve an output voltage range of –5 V < V_O < +5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = [(1 + R4/R3) \times (R2/(R1 + R2) \times (2 \times V_{REF} \times D/2^N)] - R4 \times V_{REF}/R3$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the DAC resolution.
V_{REF} is the reference voltage input.

with:
V_{REF} = 2.5 V.
R1 = R3 = 10 kΩ.
R2 = R4 = 20 kΩ and V_{DD} = 5 V.
$V_O = (10 \times D/2^N) - 5$.

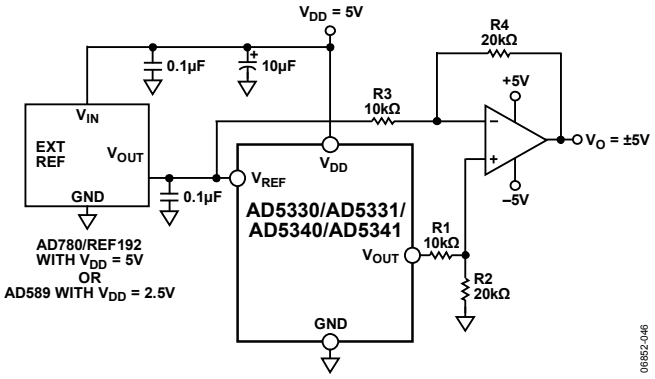


Figure 45. Bipolar Operation using the AD5330/AD5331/AD5340/AD5341

DECODING MULTIPLE AD5330/AD5331/ AD5340/AD5341

The $\overline{CS}$ pin on these devices can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same data and $\overline{WR}$ pulses, but only $\overline{CS}$ to one of the DACs is active at any one time, so data is only written to the DAC whose $\overline{CS}$ is low. If multiple AD5341s are being used, a common HBEN line is also required to determine if the data is written to the high byte or low byte register of the selected DAC.

The 74HC139 is used as a 2-line to 4-line decoder to address any of the DACs in the system. To prevent timing errors, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 46 shows a diagram of a typical setup for decoding multiple devices in a system. Once data has been written sequentially to all DACs in

a system, all the DACs can be updated simultaneously using a common $\overline{\text{LDAC}}$ line. A common $\overline{\text{CLR}}$ line can also be used to reset all DAC outputs to zero.

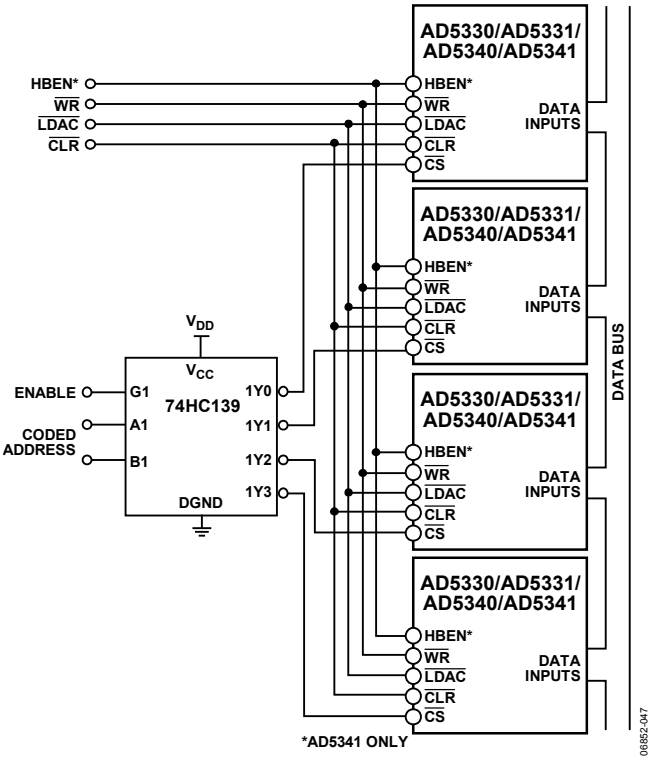


Figure 46. Decoding Multiple DAC Devices

PROGRAMMABLE CURRENT SOURCE

Figure 47 shows the AD5330/AD5331/AD5340/AD5341 used as the control element of a programmable current source. In this example, the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the 470 Ω adjustment potentiometer, which gives an adjustment of about ±5%. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both having rail-to-rail operation on their outputs. The current for any digital input code and resistor value can be calculated as follows:

$$I = G \times V_{REF} \times \frac{D}{(2^N \times R)} \text{mA}$$

where:
G is the gain of the buffer amplifier (1 or 2).
D is the digital equivalent of the digital input code.
N is the DAC resolution (8, 10, or 12 bits).
R is the sum of the resistor plus adjustment potentiometer in kilo ohms.

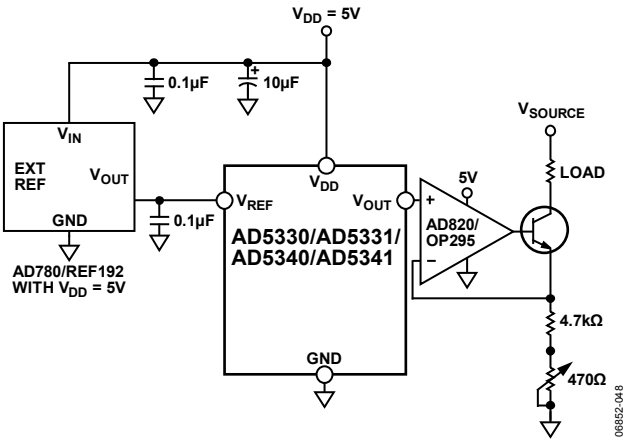


Figure 47. Programmable Current Source

POWER SUPPLY BYPASSING AND GROUNDING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5330/AD5331/AD5340/AD5341 are mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the device is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as closely as possible to the device. The AD5330/AD5331/AD5340/AD5341 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

Table 11. Overview of AD53xx Parallel Devices

Part No.	Resolution Bits	DNL	No. of V_{REF} Pins	Settling Time	Additional Pin Functions				Package	No. of Pins
					BUF	GAIN	HBEN	$\overline{CLR}$		
Singles										
AD5330	8	±0.25	1	6 µs	BUF	GAIN		$\overline{CLR}$	TSSOP	20
AD5331	10	±0.5	1	7 µs		GAIN		$\overline{CLR}$	TSSOP	20
AD5340	12	±1.0	1	8 µs	BUF	GAIN		$\overline{CLR}$	TSSOP	24
AD5341	12	±1.0	1	8 µs	BUF	GAIN	HBEN	$\overline{CLR}$	TSSOP	20
Duals										
AD5332	8	±0.25	2	6 µs				$\overline{CLR}$	TSSOP	20
AD5333	10	±0.5	2	7 µs	BUF	GAIN		$\overline{CLR}$	TSSOP	24
AD5342	12	±1.0	2	8 µs	BUF	GAIN		$\overline{CLR}$	TSSOP	28
AD5343	12	±1.0	1	8 µs			HBEN	$\overline{CLR}$	TSSOP	20
Quads										
AD5334	8	±0.25	2	6 µs		GAIN		$\overline{CLR}$	TSSOP	24
AD5335	10	±0.5	2	7 µs			HBEN	$\overline{CLR}$	TSSOP	24
AD5336	10	±0.5	4	7 µs		GAIN		$\overline{CLR}$	TSSOP	28
AD5344	12	±1.0	4	8 µs					TSSOP	28

Table 12. Overview of AD53xx Serial Devices

Part No.	Resolution Bits	No. of DACs	DNL	Interface	Settling Time	Package	No of Pins
Singles							
AD5300	8	1	±0.25	SPI	4 µs	SOT-23, MSOP	6, 8
AD5310	10	1	±0.5	SPI	6 µs	SOT-23, MSOP	6, 8
AD5320	12	1	±1.0	SPI	8 µs	SOT-23, MSOP	6, 8
AD5301	8	1	±0.25	2-Wire	6 µs	SOT-23, MSOP	6, 8
AD5311	10	1	±0.5	2-Wire	7 µs	SOT-23, MSOP	6, 8
AD5321	12	1	±1.0	2-Wire	8 µs	SOT-23, MSOP	6, 8
Duals							
AD5302	8	2	±0.25	SPI	6 µs	MSOP	10
AD5312	10	2	±0.5	SPI	7 µs	MSOP	10
AD5322	12	2	±1.0	SPI	8 µs	MSOP	10
AD5303	8	2	±0.25	SPI	6 µs	TSSOP	16
AD5313	10	2	±0.5	SPI	7 µs	TSSOP	16
AD5323	12	2	±1.0	SPI	8 µs	TSSOP	16
Quads							
AD5304	8	4	±0.25	SPI	6 µs	MSOP, LFCSP	10
AD5314	10	4	±0.5	SPI	7 µs	MSOP, LFCSP	10
AD5324	12	4	±1.0	SPI	8 µs	MSOP, LFCSP	10
AD5305	8	4	±0.25	2-Wire	6 µs	MSOP	10
AD5315	10	4	±0.5	2-Wire	7 µs	MSOP	10
AD5325	12	4	±1.0	2-Wire	8 µs	MSOP	10
AD5306	8	4	±0.25	2-Wire	6 µs	TSSOP	16
AD5316	10	4	±0.5	2-Wire	7 µs	TSSOP	16
AD5326	12	4	±1.0	2-Wire	8 µs	TSSOP	16
AD5307	8	4	±0.25	SPI	6 µs	TSSOP	16
AD5317	10	4	±0.5	SPI	7 µs	TSSOP	16
AD5327	12	4	±1.0	SPI	8 µs	TSSOP	16

OUTLINE DIMENSIONS

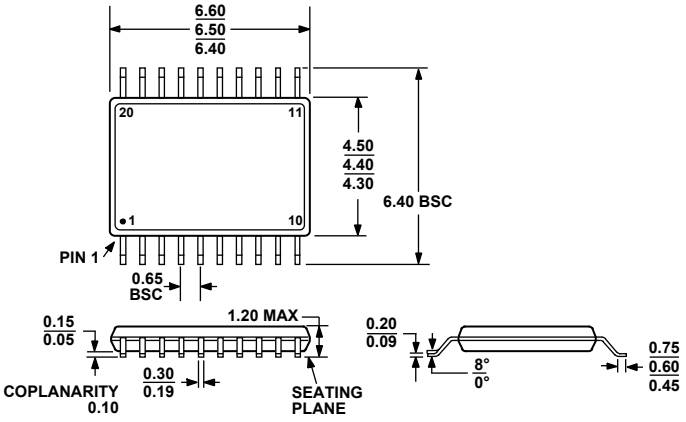


Figure 48. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

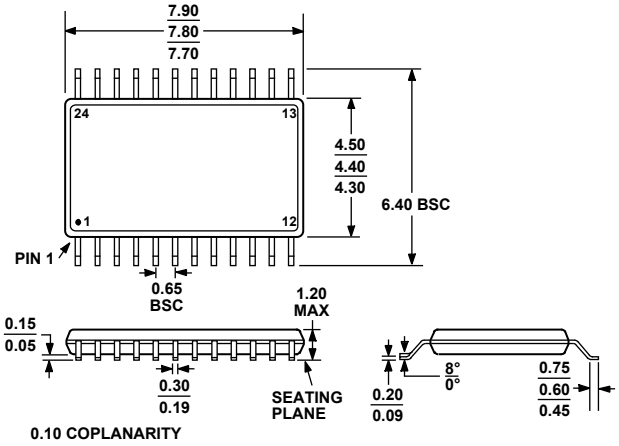


Figure 49. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5330BRU	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5330BRU-REEL	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5330BRU-REEL7	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5330BRUZ[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5330BRUZ-REEL[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5330BRUZ-REEL7[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5331BRU	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5331BRU-REEL	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5331BRU-REEL7	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5331BRUZ[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5331BRUZ-REEL[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5331BRUZ-REEL7[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5340BRU	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD5340BRU-REEL	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD5340BRU-REEL7	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD5340BRUZ[1]	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD5340BRUZ-REEL[1]	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD5340BRUZ-REEL7[1]	–40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD5341BRU	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5341BRU-REEL	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5341BRU-REEL7	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5341BRUZ[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5341BRUZ-REEL[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5341BRUZ-REEL7[1]	–40°C to +105°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20

[1] Z = RoHS Compliant Part.

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