# MAS9560

## Stereo Audio Driver DAC

This is preliminary information on a new product under development. Micro Analog Systems Oy reserves the right to make any changes without notice.




- **16-Bit Stereo Audio DAC**
- **Stereo Headphone Drivers**
- **Mono Earpiece Driver**
- **Mono Loudspeaker Driver**
- **Mixing of Analog and Digital Audio Signals**
- **Integrated LDO**
- **Flexible Power Down Control**

## DESCRIPTION

The MAS9560 Stereo Audio DAC chip is specially intended to audio applications in portable devices. It has both analog and digital inputs for audio data thus enabling the mixing of signals. MAS9560 is equipped with integrated high performance LDO, which ensures high quality of output signal even in noisy power supply environment. MAS9560 has three audio outputs (for headphone, earpiece and loudspeaker) making it an ideal choice for space critical applications. Since current consumption is a critical factor in portable devices, MAS9560 has flexible power down control enabling the shutting down of the parts of the circuit that are not in use.

## FEATURES

- 16-Bit Stereo Audio DAC
- Stereo Headphone Drivers (25 mW)
- Mono Earpiece Driver (100 mW)
- Mono Loudspeaker Driver (410 mW)
- -50 dB to 32 dB Analog Volume Control
- Mute for All Volume Controls
- Analog and Digital Signal Mixing
- Integrated LDO
- Flexible Power Down Control
- Audio Sample Rates from 8 kHz to 48 kHz
- $I^2C$/SPI Compatible Serial Control Port
- $I^2S$ Digital Audio Interface
- Supply Voltage Range 2.7 V to 5.5 V
- Digital I/O Voltage Range 1.8 V to 5.5 V
- Package QFN 6x6 40ld
- Compatible with DAC3560C

## APPLICATIONS

- Portable devices with sophisticated audio functions:
  - Cell Phones
  - PDAs
  - MP3 players with integrated AM/FM radio

## BLOCK DIAGRAM

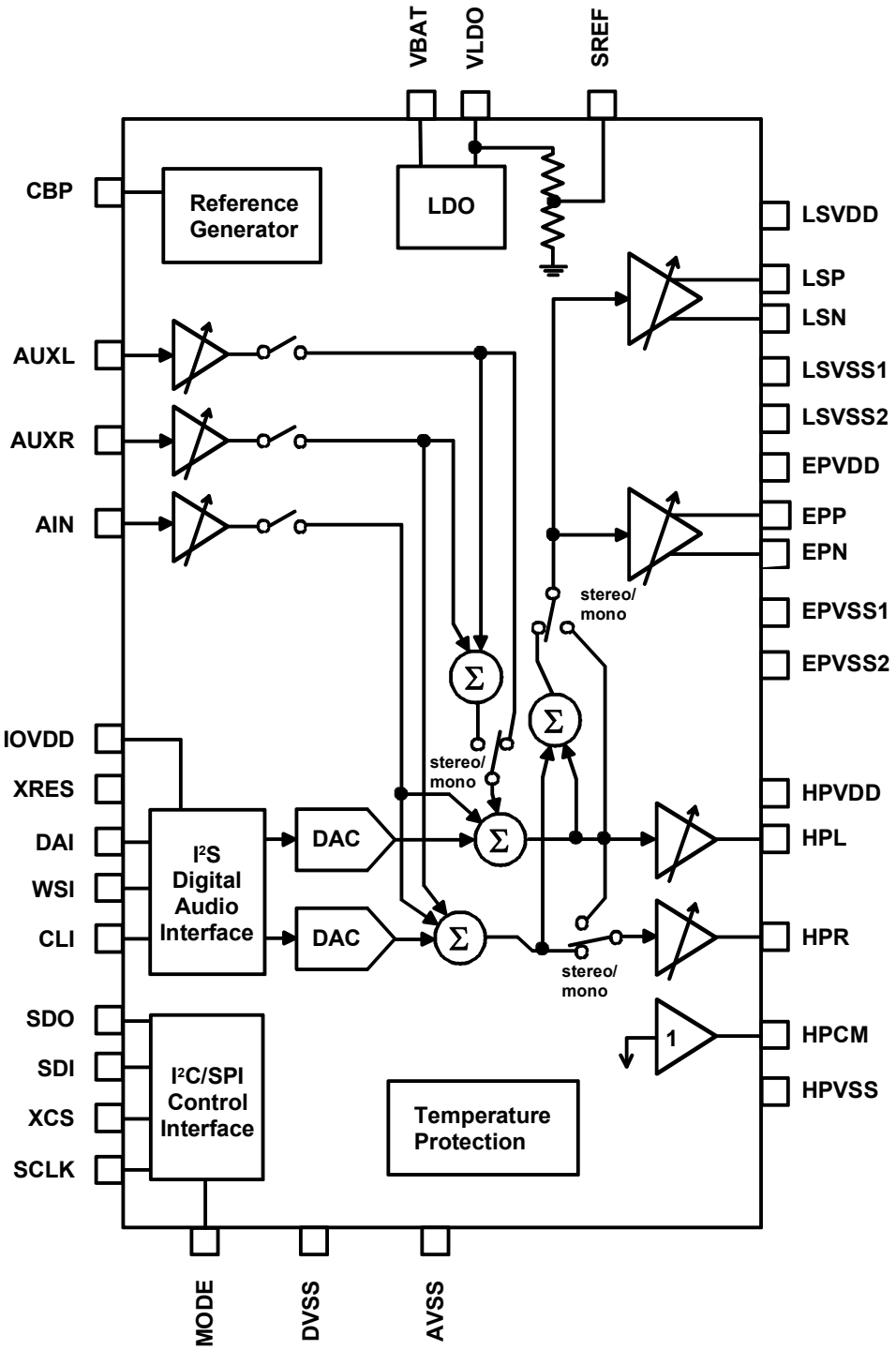



**Figure 1**. Block diagram of MAS9560

## DETAILED BLOCK DESCRIPTION

### ◆ DAC

MAS9560 contains two digital-to-analog converters (DACs), which values are set through $I^2S$ bus (see $I^2S$ section for further description). The sampling rate of DACs is defined by WSI or CLI. In over sampling mode the sampling frequency is the frequency of CLI pin divided by four ($f_{CLI}/4$). WSI is used as a sampling clock in default mode.

### ◆ Audio Drivers

MAS9560 contains three audio drivers, all of which can be used simultaneously or separately. One driver is for loudspeaker, one for earpiece and one for headphone. The two latter ones have analog volume control from –30 dB gain to +6 dB gain in 1.5 dB steps, whereas the control range for loudspeaker driver is from –30 dB to +12 dB in 1.5 dB steps (see Control Register section p.18) The main features of each driver is as follows:

- Loudspeaker Driver: mono, differential output, output power: 410 mW @ $V_{DD}$ = 2.7 V, 1100 mW @ $V_{DD}$ = 5.0 V
- Earpiece Driver: mono, differential output, output power: 100 mW @ $V_{DD}$ = 2.7 V, 300 mW @ $V_{DD}$ = 5.0 V
- Headphone Driver: stereo, single-ended output, output power: 25 mW @ $V_{DD}$ = 2.7 V, 80 mW @ $V_{DD}$ = 5.0 V

All the drivers are short-circuit protected.

### ◆ Digital Audio Interface

Inter-IC Sound ($I^2S$) bus is a 3-wire serial interface for transmission of 2-channel (stereo) Pulse Code Modulation digital data between MAS9560 and external digital audio source, for example MP3 player.

### ◆ LDO Voltage Regulator

MAS9560 has integrated low dropout voltage regulator, which output voltage is fixed 2.86 V. In power supply noisy environments the usage of this LDO in powering headphone and earpiece drivers improves the PSRR of these drivers to 100 dB and over. 10 nF bypass capacitor can be connected to CBP pin further improving the performance. In case LDO is not used (non-LDO mode) its output pin (VLDO) must be connected to external voltage source since it is supplying power for analog front-end.

The integrated LDO can also be disabled by using Mode-Control-Register.

### ◆ Reference Block

The reference block, which provides reference level for analog audio signals, has two modes:

- LDO mode: Audio reference level = VLDO/2. (SREF pin). This is half of integrated voltage regulator's output voltage.
- Non-LDO mode: Audio reference level = VLDO/2. VLDO should be connected to VBAT in Non-LDO mode.

### ◆ $I^2C$/SPI Control Interface

MAS9560 has many user selectable options. These selections are mainly made by using registers, which are programmed via one of the two standard control interface protocols: $I^2C$ or SPI. The used control interface type is selected with MODE pin.

### ◆ Registers

MAS9560 has 11 on-chip registers, which byte length is 8 bits. Reset register is write-only, all other registers permit read and write access.

### ◆ Power Management

MAS9560 has Block Control Register, which allows separate blocks to be turned on and off independently. This can be used to reduce power consumption, since typically all the blocks are not needed at the same time. If, for example, only loudspeaker is used as an output, the drivers for earpiece and headphone can be disabled.
Additionally MAS9560 has Mode Control Register, which can be used to select operating mode for MAS9560. These four modes are as follows:

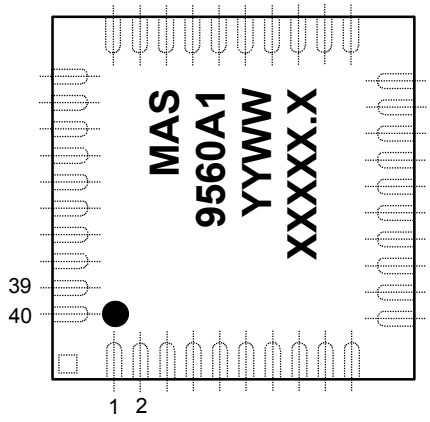
- Zero Power, where all digital and analog blocks are in power down mode. This is a default mode after startup.
- Analog stand-by, which is intended to be used as a wait state when starting the device. The purpose of this operating mode is to suppress audible plops caused by abrupt amplification changes when blocks in audio chain are waking up.
- Aux to Line, where DACs are disabled and only analog signaling is used.
- Full Power, where all blocks are active.

### ◆ Temperature Protection

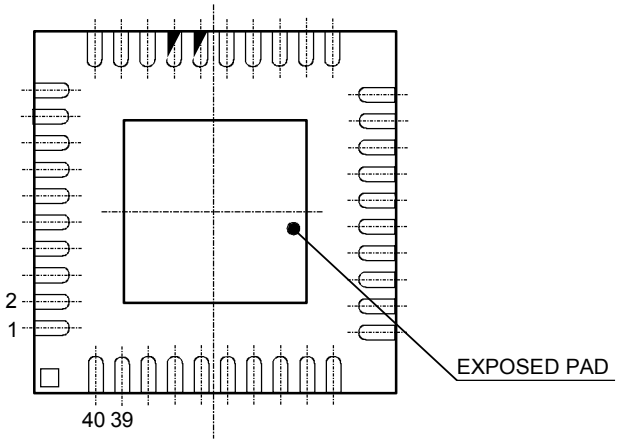
MAS9560 is equipped with over temperature protection.

## PIN CONFIGURATION

**QFN 6x6 40ld**




**TOP VIEW**




**BOTTOM VIEW**

Top Marking Information:
YYWW = Year, Week
XXXXX.X = Lot Number

## PIN DESCRIPTION

G = Ground, I = Input, O = Output, P = Power

| Pin Name | Pin Number | Type | Function |
|---|---|---|---|
| VBAT | 1 | P | Power Supply Voltage |
| LSVSS1 | 2 | G | GND for Loudspeaker Driver |
| LSP | 3 | O | Loudspeaker Differential Output (Positive) |
| LSVDD | 4 | P | Power Supply Voltage for Loudspeaker Driver |
| LSN | 5 | O | Loudspeaker Differential Output (Negative) |
| LSVSS2 | 6 | G | GND for Loudspeaker Driver |
| N/C | 7 | - | Not Connected |
| DVSS | 8 | G | Digital GND |
| MODE | 9 | I | Control Interface ($I^2C$ / SPI) Selection |
| IOVDD | 10 | P | Digital I/O Power Supply Voltage |
| SDI | 11 | I/O | SPI Data In or $I^2C$ Data In/Out |
| SCLK | 12 | I | SPI or $I^2C$ Clock Signal |
| SDO | 13 | O | SPI Data Out |
| XCS | 14 | I | SPI Chip Select |
| DAI | 15 | I | $I^2S$ Data In |
| WSI | 16 | I | $I^2S$ Word Strobe Input |
| CLI | 17 | I | $I^2S$ Clock Signal |
| XRES | 18 | I | Reset Input |
| N/C | 19 | - | Not Connected |
| N/C | 20 | - | Not Connected |
| AIN | 21 | I | Analog Input (Mono) |

| Pin Name | Pin Number | Type | Function |
|---|---|---|---|
| AUXL | 22 | I | Analog Auxiliary (AUX) Input Left Channel (Stereo) |
| AUXR | 23 | I | Analog Auxiliary (AUX) Input Right Channel (Stereo) |
| HPCM | 24 | O | Headphone Common Output |
| HPVSS | 25 | G | GND for Headphone Driver |
| HPL | 26 | O | Headphone Output (Left Channel) |
| HPR | 27 | O | Headphone Output (Right Channel) |
| HPVDD | 28 | P | Power Supply Voltage for Headphone Driver |
| N/C | 29 | - | Not Connected |
| SREF | 30 | O | Audio Signal Reference Level |
| CBP | 31 | I | Pin for LDO Bypass Capacitor |
| EPVSS2 | 32 | G | Earpiece Ground |
| EPN | 33 | O | Earpiece Differential Output (Negative) |
| EPVDD | 34 | P | Power Supply for Earpiece Driver |
| EPP | 35 | O | Earpiece Differential Output (Positive) |
| EPVSS1 | 36 | G | GND for Earpiece Driver |
| AVSS | 37 | G | Analog Ground |
| N/C | 38 | - | Not Connected |
| N/C | 39 | - | Not Connected |
| VLDO (AVDD) | 40 | P | LDO Output (Analog Power Supply) |
| Exposed Pad | | | Exposed pad should be soldered to GND layer to improve heat dissipation |

**Note**: Pins EPVDD and HPVDD have to be connected to VLDO pin.

## DETAILED PIN DESCRIPTIONS

**◆ Power supply pins**

The power supply of MAS9560 is divided into functional sections so that:

- DVSS is connected internally with all digital parts
- IOVDD and DVSS are connected internally with all digital inputs and outputs
- DVSS is ground connection for all digital parts
- All GND pins are internally connected together
- LSVDD and VBAT are internally connected together

Other power supply pins should be connected as follows:

- VLDO should be connected to VBAT in non-LDO mode. If LDO mode is selected, VLDO is the output of LDO.
- HPVDD and EPVDD can be driven by VLDO in LDO mode to reduce power supply noise
- HPVSS, EPVSS, LSVSS must be connected to analog ground (AVSS). The pins are internally connected together.

## ABSOLUTE MAXIMUM RATINGS

All voltages with respect to ground.

| Parameter | Symbol | Pin Name | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage (VBAT and LSVDD are internally connected together) | $V_{BAT}$ | VBAT, LSVDD | -0.3 | 6 | V |
| Voltage Range for Other Pins | | | -0.3 | VBAT + 0.3 | V |
| ESD Rating (HBM) | | | | 2 | kV |
| Junction Temperature | $T_{Jmax}$ | | | +175 (limited) | °C |
| Storage Temperature | $T_S$ | | -55 | +150 | °C |
| Power Dissipation ($T_A$ = +85°C) (Exposed pad soldered to PCB) | | | | 1.2 | W |

Stresses beyond those listed may cause permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

## RECOMMENDED OPERATING CONDITIONS

All voltages with respect to ground.

| Parameter | Symbol | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Junction Temperature | $T_J$ | | | -40 | | +125 | °C |
| Operating Ambient Temperature | $T_A$ | | | -40 | | +85 | °C |
| Master Supply Voltage | | VBAT, LSVDD | LDO mode, VBAT and LSVDD internally connected | 3.0 | 3.6 | 5.5 | V |
| Master Supply Voltage | | VBAT, LSVDD, VLDO, EPVDD, HPVDD | Non-LDO mode, VBAT and LSVDD internally connected | 2.7 | 3.6 | 5.5 | V |
| Analog Operating Supply Voltage | $V_{BAT}$ | VBAT, LSVDD | Internally connected together | 2.7 | | 5.5 | |
| | | VLDO, HPVDD, EPVDD | | 2.7 | | $V_{BAT}$ | V |
| Digital Interface Voltage | $IO_V_{DD}$ | IOVDD | | 1.5 | | $V_{BAT}$ | V |
| Earpiece Supply Voltage | | EPVDD | | 2.7 | | $V_{BAT}$ | V |
| Headphone Supply Voltage | | HPVDD | | 2.7 | | $V_{BAT}$ | V |

## RECOMMENDED EXTERNAL COMPONENTS

| Parameter | Symbol | Pin Name | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| LDO Output Capacitance | $C_{L_LDO}$ | VLDO | 0.23 | | $C_{IN_LDO}$ | µF | 1. Ceramic and film capacitors can be used.<br>2. The value of $C_{L\ LDO}$ should be smaller than or equal to the value of $C_{IN\ LDO}$. |
| Effective Series Resistance | ESR | | 0.01 | | 3 | Ohm | 1. When within this range, stable with all $I_{OUT}$ = 0 mA…150 mA values. |
| LDO Bypass Capacitance (Optional: if $C_{BYPASS}$ is not used, noise performance and PSRR decline, but rise time is improved.) | $C_{BP_LDO}$ | CBP | | 0.01 | | µF | 1. Ceramic and film capacitors are best suited. For maximum output voltage accuracy DC leakage current through capacitor should be kept as low as possible. In any case DC leakage current must be below 100 nA. |
| LDO Input Capacitance | $C_{IN_LDO}$ | VBAT | 0.5 | | | µF | 1. A big enough input capacitance is needed to prevent possible impedance interactions between the supply and LDO.<br>2. Ceramic, tantalum, and film capacitors can be used. If a tantalum capacitor is used, it should be checked that the surge current rating is sufficient for the application.<br>3. In the case that the inductance between a **battery** and LDO is very small (< 0.1 µH), a 0.47 µF input capacitor is sufficient.<br>4. The value of $C_{IN_LDO}$ should not be smaller than the value of $C_{L\ LDO}$. |
| When selecting capacitors, tolerance and temperature coefficient must be considered to **make sure that the capacitance and resistance are between the above specified limits in all potential operating conditions**. | | | | | | | |
| Analog Input Coupling Capacitor | $C_{AIN}$, $C_{AUXL}$, $C_{AUXR}$ | AUXL, AUXR, AIN | | 470 | | nF | 1. Affects on input signal's pass band frequence. |
| SREF Bypass Capacitor | $C_{SREF}$ | SREF | | 3.3 | | µF | 1. A too small value capacitor cannot effectively prevent disturbance from getting to signal ground. |
| Load Resistance: Headphone | $R_{L_HP}$ | HPR, HPL, HPCM | 16 | 32 | | ohm | |
| Load Resistance: Earpiece | $R_{L_EP}$ | EPP, EPN | 16 | 32 | | ohm | |
| Load Resistance: Loudspeaker | $R_{L_S}$ | LSP, LSN | 4 | 8 | | ohm | |

## ELECTRICAL CHARACTERISTICS IN LDO MODE

### ◆ Integrated LDO Characteristics

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, , typical values at $T_A$ = +27°C, $I_{OUT}$ = 1.0 mA, $C_{IN_LDO}$ = 1.0 µF, $C_{L_LDO}$ = 1.0 µF, $C_{BP_LDO}$ = 10 nF, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | VLDO | Operational Mode | 2.75 | 2.86 | 2.95 | V |
| | | Standby Mode, LDO not bypassed | | 2.86 | | |
| | | Standby Mode, LDO bypassed | | $V_{BAT}$ | | |
| | | Zero Power Mode, LDO not bypassed | | 0 | | |
| | | Zero Power Mode, LDO bypassed | | $V_{BAT}$ | | |
| Dropout Voltage | VLDO | $I_{OUT}$ = 1 mA<br>$I_{OUT}$ = 50 mA<br>$I_{OUT}$ = 150 mA | | 1.7<br>70<br>200 | | mV |
| Continuous Output Current | VLDO | | 0 | | 150 | mA |
| Short Circuit Current | VLDO | $R_L$ = 0 Ω | 200 | 450 | 675 | mA |
| Peak Output Current | VLDO | $V_{OUT}$ > 95%* $V_{OUT(NOM)}$ | | 410 | | mA |
| Line Regulation | VLDO | 3.6 V < VBAT < 5.3 V,<br>$I_{OUT}$ = 60 mA | | 0.7 | | mV |
| Load Regulation | VLDO | $I_{OUT}$ = 1 mA to 50 mA<br>$I_{OUT}$ = 1 mA to 150 mA | | 5<br>10 | | mV |
| Output Noise Voltage | VLDO | 300 Hz < f < 50 kHz<br>$C_{BP_LDO}$ = 10 nF<br>w/o $C_{BP_LDO}$ | | 20<br>110 | | µVrms |
| Noise Density | VLDO | $I_{OUT}$ = 50 mA,<br>f = 1 kHz | | 100 | | $nV/\sqrt{Hz}$ |
| PSRR | VLDO | f = 1 kHz<br>f = 10 kHz<br>f = 100 kHz | | 67<br>65<br>48 | | dB |
| Rise Time (10%… 90%) | VLDO | $I_{OUT}$ = 30mA<br>$C_{BP_LDO}$ = 10 nF<br>w/o $C_{BP_LDO}$ | | 4<br>16 | | ms<br>µs |
| Overshoot | VLDO | w/o $C_{BP_LDO}$ | | 3 | 10 | % |
| Start-up Delay (From the time LDO is enabled via register until VLDO is 90% of the nominal $V_{OUT}$) | VLDO | w/o $C_{BP_LDO}$ | | 17 | | µs |
| Thermal Protection/ Threshold High | | | 145 | 160 | 175 | °C |
| Thermal Protection/ Threshold Low | | | 135 | 150 | 165 | °C |

The hysteresis of 10°C prevents the device from turning on too soon after thermal shut-down.

### ◆ Analog Audio Inputs (AIN, AUXL, AUXR) in LDO mode

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86 V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Input Range | AIN, AUXL, AUXR | | | 2.05 | | $V_{PP}$ |
| Input Clipping Level | AIN, AUXL, AUXR | | | | VLDO | V |
| Input Resistance | AIN, AUXL, AUXR | Gain = -20 dB | | 23 | | kΩ |
| | | Gain = 0 dB | | 14 | | |
| | | Gain = +20 dB | | 3 | | |
| Gain Setting Range | AIN, AUXL, AUXR | | -20 | | 20 | dB |
| Gain Step Size | AIN, AUXL, AUXR | | 1.5 | 2 | 2.5 | dB |
| Absolute Gain Error | AIN, AUXL, AUXR | | -1.2 | 0 | 1.2 | dB |

### ◆ Analog Audio Outputs (Headphone, Earpiece, Loudspeaker) in LDO mode

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86 V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Volume Range (Headphone and Earpiece) | HPL,HPR,EPP,EPN | | -30 | | 6 | dB |
| Volume Range (Loudspeaker) | LSP,LSN | | -30 | | 12 | dB |
| Volume Control Step Size | HPL,HPR,EPP,EPN,LSP,LSN | | 1.0 | 1.5 | 2.0 | dB |
| Headphone Output Power | HPL, HPR, (HPCM) | THD < 0.1%, f = 1 kHz, $R_L$ = 32 Ω | | 25 (25) | | mW |
| Earpiece Output Power | EPP, EPN | THD < 0.2%, f = 1 kHz, $R_L$ = 32 Ω | | 100 | | mW |
| Loudspeaker Output Power | LSP, LSN | THD < 1%, f = 1 kHz, $R_L$ = 8 Ω | | 410 | | mW |
| Headphone Short Circuit Current | HPL, HPR, HPCM, VLDO, AVSS | | 250 | 350 | 450 | mA |
| Earpiece Short Circuit Current | EPP, EPN, VLDO, AVSS | | 250 | 350 | 450 | mA |
| Loudspeaker Short Circuit Current | LSP, LSN | | 800 | 1000 | | mA |
| Headphone and Earpiece Output Signal Reference Level | HPL, HPR, HPCM, EPP, EPN | SREF settled | | VLDO/2 | | V |
| Loudspeaker Output Signal Reference Level | LSP, LSN | SREF settled | | LSVDD/2 | | V |

### ◆ Dynamic Performance in LDO mode

LSVDD = VBAT = 3.6 V, EPVDD = HPVDD = VLDO = 2.86 V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|---|
| Headphone Full Scale Output Level | HPL,HPR, HPCM | No load, Volumes = 0 dB | | | 2.04 | | Vpp |
| Earpiece Full Scale Output Level | EPP, EPN | No load, Volumes = 0 dB | | | 4.08 | | Vpp |
| Loudspeaker Full Scale Output Level | LSP,LSN | No load, Volumes = 0 dB | | | 4.08 | | Vpp |
| Absolute 0 dB Gain, Analog In to Analog Out (unweighted), DAC off | AIN, AUXL, AUXR, HPL, HPR, HPCM, EPP, EPN, LSP, LSN | Analog to Headphone | | -1.2 | 0 | +1.2 | dB |
| | | Analog to Earpiece | | -1.2 | 0 | +1.2 | |
| | | Analog to Loudspeaker | | -1.2 | 0 | +1.2 | |
| Mute Level | AIN, AUXL, AUXR, HPL, HPR, HPCM, EPP, EPN, LSP, LSN | Headphone | | -40 | -75 | | dB |
| | | Earpiece | | -40 | -75 | | |
| | | Loudspeaker | | -40 | -75 | | |
| | | Analog Input (AIN) | | -40 | -60 | | |
| | | Auxiliary Input (AUXL, AUXR) | | -40 | -65 | | |
| Dynamic Range, Digital In to Analog Out (unweighted) | HPL, HPR, (HPCM) | $f_{SAMPLE}$ = 48 kHz with 16-bit data, Bandwidth = 20 Hz… 20 kHz | DAC to Headphone | | 81 | | dB |
| | EPP, EPN | | DAC to Earpiece | | 76 | | dB |
| | LSP, LSN | | DAC to Loudspeaker | | 76 | | dB |
| Dynamic Range, Digital In to Analog Out (A-weighted) | HPL, HPR, (HPCM) | $f_{SAMPLE}$ = 48 kHz with 16-bit data, Bandwidth = 20 Hz… 20 kHz | DAC to Headphone | | 86 | | dB |
| | EPP, EPN | | DAC to Earpiece | | 82 | | dB |
| | LSP, LSN | | DAC to Loudspeaker | | 82 | | dB |
| Dynamic Range, Analog In to Analog Out (unweighted) | AIN, AUXL, AUXR, HPL, HPR, HPCM, | DAC off, Analog to Headphone | | | 92 | | dB |
| | AIN, AUXL, AUXR, EPP,EPN | DAC off, Analog to Earpiece | | | 89 | | dB |
| | AIN, AUXL, AUXR, LSP, LSN | DAC off, Analog to Loudspeaker | | | 82 | | dB |

| | | | | | | |
|---|---|---|---|---|---|---|
| Dynamic Range, Analog In to Analog Out (A-weighted) | AIN, AUXL, AUXR, HPL, HPR, HPCM, | DAC off, Analog to Headphone | | 95 | | dB |
| | AIN, AUXL, AUXR, EPP, EPN | DAC off, Analog to Earpiece | | 86 | | dB |
| | AIN, AUXL, AUXR, LSP, LSN | DAC off, Analog to Loudspeaker | | 85 | | dB |
| Headphone THD + Noise | HPL, HPR, (HPCM) | f = 50 Hz... 20 kHz, $R_L$ = 32 Ω, Pout = 15 mW | | -65 (-63) | | dB |
| Earpiece THD + Noise | EPP, EPN | f = 150 Hz... 20 kHz, $R_L$ = 32 Ω, Pout = 50 mW | | -55 | | dB |
| Loudspeaker THD + Noise | LSP, LSN | f = 150 Hz... 20 kHz, $R_L$ = 8 Ω, Pout = 200 mW | | -58 | | dB |
| Mute Level | HPL, HPR, (HPCM), EPP, EPN, LSP, LSN | | | -73 | | dB |
| Headphone PSRR | HPL, HPR, HPCM, VBAT | f = 1.0 kHz, VBAT ≥ 3.1 V, $R_L$ = 32 Ω, Vripple = 0.5 Vpp, Zero audio signal | | 120 | | dB |
| Earpiece PSRR | EPP, EPN, VBAT | f = 1.0 kHz, VBAT ≥ 3.1 V, $R_L$ = 32 Ω, Vripple = 0.5 Vpp, Zero audio signal | | 120 | | dB |
| Loudspeaker PSRR | LSVDD, LSP, LSN | f = 1.0 kHz, LSVDD ≥ 3.1 V, $R_L$ = 8 Ω, Vripple = 0.5 Vpp, Zero audio signal | 40 | 63 | | dB |

## ◆ Current Consumption

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, , typical values at $T_A$ = +27°C, $I_{OUT}$ = 1.0 mA, $C_{IN_LDO}$ = 1.0 µF, $C_{L_LDO}$ = 1.0 µF, $C_{BP_LDO}$ = 10 nF, unless otherwise noted

| Control Bits | VBAT | Current measurement test setup | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Mono | | | | x | x | x | x | | | |
| DAC | | x | x | x | x | | | | | x |
| AIN | | | | | | x | x | | | x |
| AUX | | | | | | | | x | x | x |
| LS | | | | x | | x | | | | x |
| EP | | | | | x | | x | | | x |
| HPR | | x | x | | | | | x | x | x |
| HPL | | x | x | | | | | x | x | x |
| HPC | | | x | | | | | | x | x |
| | | | | | | | | | | |
| Typical Current [mA] | 3.00 V | 3.1 | 5.4 | 8.4 | 4.6 | 9.0 | 4.9 | 5.8 | 7.1 | 19 |
| | 3.60 V | 3.1 | 5.5 | 12 | 4.6 | 13 | 4.9 | 5.8 | 7.1 | 22 |
| | 5.50 V | 3.1 | 5.3 | 37 | 4.6 | 37 | 4.9 | 5.8 | 7.1 | 47 |
| Maximum Current [mA] | 3.00 V | 7.5 | 10 | 20 | 7 | 20 | 8 | 10 | 12 | 40 |
| | 3.60 V | 7.5 | 10 | 25 | 7 | 25 | 8 | 10 | 12 | 40 |
| | 5.50 V | 7.5 | 10 | 70 | 7 | 70 | 8 | 10 | 12 | 80 |

**Note:** Above values measured with following loads: loudspeaker LSP-LSN 22 ohm (nominal load 8 ohm cannot be used in testing due to tester limitations), earphone EPP-EPN 32 ohm, HPR-HPCM 32 ohm, HPL-HPCM 32 ohm.

## ELECTRICAL CHARACTERISTICS IN NON-LDO MODE

### ◆ Analog Audio Inputs (AIN, AUXL, AUXR) in non-LDO mode

LSVDD = VBAT = EPVDD = HPVDD = VLDO = 2.7 V...5.5 V (non-LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Full Scale Input Level | AIN, AUXL, AUXR | Volumes = 0 dB | | 0.715 x VLDO | VLDO | Vpp |
| Input Clipping Level | AIN, AUXL, AUXR | | | | VLDO | V |
| Input Resistance | AIN, AUXL, AUXR | Gain = -20 dB | | 23 | | kΩ |
| | | Gain = 0 dB | | 14 | | |
| | | Gain = +20 dB | | 3 | | |
| Gain Setting Range | AIN, AUXL, AUXR | | -20 | | 20 | dB |
| Gain Step Size | AIN, AUXL, AUXR | | 1.5 | 2 | 2.5 | dB |
| Absolute Gain Error | AIN, AUXL, AUXR | | -1.2 | 0 | 1.2 | dB |

### ◆ Analog Audio Outputs (Headphone, Earpiece, Loudspeaker) in non-LDO mode

LSVDD = VBAT = EPVDD = HPVDD = VLDO = 2.7 V...5.5 V (non-LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Headphone Output Power | HPL, HPR, HPCM | HPVDD = 5.5 V, THD < 0.1%, f = 1 kHz, $R_L$ = 32 Ω | | 80 | | mW |
| Earpiece Output Power | EPP, EPN | EPVDD = 5.5 V, THD < 0.2%, f = 1 kHz, $R_L$ = 32 Ω | | 300 | | mW |
| Loudspeaker Output Power | LSP, LSN | LSVDD = 5.5 V, THD < 1%, f = 1 kHz, $R_L$ = 8 Ω | | 1100 | | mW |
| Headphone and Earpiece Output Signal Reference Level | EPP, EPN, HPL, HPR, HPCM | SREF settled | | VLDO/2 | | V |
| Loudspeaker Output Signal Reference Level | LSP, LSN | SREF settled | | VBAT/2 | | V |

### ◆ Dynamic Performance in non-LDO mode

LSVDD = VBAT = EPVDD = HPVDD = VLDO = 3.6 V (non-LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Headphone Full Scale Output Level | HPL, HPR | No load, Volumes = 0 dB | | | HPVDD | Vpp |
| Earpiece Full Scale Output Level | EPP, EPN | No load, Volumes = 0 dB | | | EPVDD | Vpp |
| Loudspeaker Full Scale Output Level | LSP, LSN | No load, Volumes = 0 dB | | | LSVDD | Vpp |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Dynamic Range, Digital In to Analog Out (unweighted) | HPL, HPR, (HPCM) | $f_{SAMPLE}$ = 48 kHz with 16-bit data, Bandwidth = 20 Hz… 20 kHz | DAC to Headphone | | 82 | | dB |
| | EPP, EPN | | DAC to Earpiece | | 76 | | dB |
| | LSP, LSN | | DAC to Loudspeaker | | 76 | | dB |
| Dynamic Range, Digital In to Analog Out (A-weighted) | HPL, HPR, (HPCM) | $f_{SAMPLE}$ = 48 kHz with 16-bit data, Bandwidth = 20 Hz… 20 kHz | DAC to Headphone | | 86 | | dB |
| | EPP, EPN | | DAC to Earpiece | | 82 | | dB |
| | LSP, LSN | | DAC to Loudspeaker | | 82 | | dB |
| Dynamic Range, Analog In to Analog Out (unweighted) | AIN, AUXL, AUXR, HPL, HPR, HPCM | DAC off , Analog to HP | | | 84 | | dB |
| | AIN, AUXL, AUXR, EPP, EPN | DAC off, Analog to EP | | | 92 | | dB |
| | AIN, AUXL, AUXR, LSP, LSN | DAC off, Analog to LS | | | 92 | | dB |
| Dynamic Range, Analog In to Analog Out (A-weighted) | AIN, AUXL, AUXR, HPL, HPR, HPCM | DAC off, Analog to HP | | | 86 | | dB |
| | AIN, AUXL, AUXR, EPP, EPN | DAC off, Analog to EP | | | 96 | | dB |
| | AIN, AUXL, AUXR, LSP, LSN | DAC off, Analog to LS | | | 96 | | dB |
| Headphone THD + Noise | HPL, HPR, (HPCM) | f = 50 Hz... 20 kHz, $R_L$ = 32 Ω, Pout = 15 mW | VBAT = 2.7 V | | -62 (-61) | | dB |
| | | | VBAT = 3.6 V | | -66 (-66) | | |
| | | | VBAT = 5.0 V | | -68 (-68) | | |
| Earpiece | EPP, | f = 150 Hz... 20 kHz, | VBAT = 2.7 V | | -54 | | dB |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THD + Noise | EPN | $R_L$ = 32 Ω,<br>Pout = 50 mW | VBAT = 3.6 V | | -62 | | |
| | | | VBAT = 5.0 V | | -68 | | |
| Loudspeaker<br>THD + Noise | LSP,<br>LSN | f = 150 Hz... 20 kHz,<br>$R_L$ = 8 Ω,<br>Pout = 200 mW | VBAT = 2.7 V | | -56 | | mW |
| | | | VBAT = 3.6 V | | -58 | | |
| | | | VBAT = 5.0 V | | -62 | | |
| Mute Level | HPL,<br>HPR,<br>(HPCM),<br>EPP,<br>EPN,<br>LSP,<br>LSN | | | | -75 | | dB |
| Headphone PSRR | HPL,<br>HPR,<br>HPCM,<br>VBAT | f = 1.0 kHz, VBAT ≥ 3.1 V, $R_L$ = 32 Ω,<br>Vripple = 0.5 Vpp, Zero audio signal | | | 54 | | dB |
| Earpiece PSRR | EPP,<br>EPN,<br>VBAT | f = 1.0 kHz, VBAT ≥ 3.1 V, $R_L$ = 32 Ω,<br>Vripple = 0.5 Vpp, Zero audio signal | | | 69 | | dB |
| Loudspeaker PSRR | LSVDD,<br>LSP,<br>LSN | f = 1.0 kHz, LSVDD ≥ 3.1 V, $R_L$ = 8 Ω,<br>Vripple = 0.5 Vpp, Zero audio signal | | 40 | 63 | | dB |

◆ Definitions

**Dynamic Range:** Dynamic range means the difference between the highest and lowest levels of the signal. Due to the fact that the dynamic range of a loudspeaker (or similar) would significantly affect the dynamic range measurement of MAS9560, the following has been made: THD+N has been measured at –60 dB, and dynamic range has been derived of that by adding 60 dB to that value. For example THD+N = -30 dB → Dynamic range = 90 dB.

**THD+N:** Total Harmonic Distortion + Noise

## CONTROL INTERFACES

MAS9560 registers (detailed description below) are controlled either via I²C- or SPI bus. On-chip DAC data is written using I²S-bus.

| Pin | Bus | Function |
|---|---|---|
| MODE | I²C/SPI | Select I²C (MODE=1) or SPI (MODE=0) |
| SCLK | I²C /SPI | Serial Data Clock for I²C and SPI |
| SDI | I²C /SPI | Serial Data I/O for I²C and input for SPI |
| SDO | SPI | Serial Data Output for SPI |
| XCS | SPI | Chip Select for SPI (active low) |
| DAI | I²S | Serial Data input for I²S |
| WSI | I²S | Frame Identification for I²S |
| CLI | I²S | Serial Data Clock for I²S |

◆ I²C Description

I²C – bus is selected by setting pin MODE = 1. I²C - bus is a 2-wire serial interface, so two lines, a serial data line (SDI) and serial clock line (SCLK), are required. MAS9560 data line is bi-directional for data acknowledge and transmit, but clock line is just a receiver, i.e., the clock is gotten from the master. Default state for both lines is high, since all devices connected on the bus form together an AND-function because of pull-up resistors.

A master is controlling the bus, enabling clock and giving start and stop requests, so data transfer for MAS9560 is started with start-pulse given by a master device. As the master is changing SDI level from high to low while SCLK is high, this action is recognized as the start pulse. Stop pulse is similarly created: when SCLK is high SDI level is changed from low to high. During the data transition data line (SDI) level may not change when clock (SCLK) is high, because this is interpreted either as start or stop pulse.

Data is transmitted in bytes, one byte is 8-bit long. Several bytes can be sent one by one until the master gives stop signal.

I²C data format is shown in table 1 below. The first byte in I²C data after start pulse specifies unique device code and transfer mode. Device code is specified by 7 bits and is 1001 101 for MAS9560, last (8th) bit selects read/write-mode (r/w): high for read and low for write. After first byte is read, MAS9560 acknowledges it by pulling data line (SDI) down, keeping data line down and releasing the line only after the master driven clock line (SCLK) is again pulled down.

After the device specific code MAS9560 is set as receiver for data as described above, sub-address is given as a second byte. This addresses the initial register number, and the following byte is the data which is written to the register. In case the fourth byte is written (and no stop bit is given), MAS9560 changes to increment mode and this fourth byte is written to a following register. All registers can be written by one start-stop sequence. On-chip incremental counter is just 4-bits long. Incrementing stops at address 0x0F to prevent overflow. In write mode MAS9560 gives acknowledge pulse after every byte.

I²C bus can also be used to read register values. In this case a sequence is as follows: First byte 1001 1010 is written after start pulse (MAS9560 acknowledges) after which register address is given, which is acknowledged by device. Next a new start pulse is given by the master and byte 1001 1011 is acknowledged by MAS9560, after which register (specified in initial sequence) data is written to data bus (MSB first). After that MAS9560 gives NAK (no acknowledge) signal which continues until ACK (acknowledge) or STOP signal is given by the master. In case ACK signal is given, the incremental mode of MAS9560 is enabled and next register data is written to SDI bus by MAS9560. The data is again followed by NAK signal, and the reading sequence can be repeated or stopped.

Values of unspecified bits in registers with less than 8-bits are not set to any initial value, and their value can vary from time to time.

| 1st byte | | 2nd byte | 3rd byte | 4th byte |
|---|---|---|---|---|
| device id | r/w | Register address | code | code |
| 1001 101 | 1/0 | 0000 a3 a2 a1 a0 | xxxx xxxx | xxxx xxxx |
| Called as ***DW*** when Write | | | | |
| Called as ***DR*** when Read | | | | |

**Table 1.** $I^2C$ Data Format

◆ SPI Description

Serial Peripheral Interface (SPI) bus is a 4-wire serial communication interface between a master and a slave device. SPI bus is selected by setting MODE pin to low. SCLK pin is clock, XCS pin chip select, SDI data pin and SDO data out pin. Data writing is started with pulling device specific XCS pin low, and first bit (MSB) is written at next SCLK rising edge.

The first byte defines register address and whether data will be read or write, see table 2 below. Bit 5: Read = 1 and Write = 0. Note that incremental mode stops at address 0x0F to prevent address overflow and device reset.

The following byte written to SDI is either register input data (write mode) or it is ignored (read mode). In the read mode the selected register's data can be read from SDO pin at SCLK falling edge. Data transfer stops with rising XCS pin.

In case XCS pin is held low after two first bytes, the increment mode is enabled and the following written/read bytes can be transferred to/from the next registers. SDO output is at the high impedance state when MAS9560 is not in read mode.

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Function | x | x | R/W | x | A3 | A2 | A1 | A0 |

**Table 2.** SPI first byte

◆ $I^2S$ Description

Inter-IC Sound ($I^2S$) bus is a 3-wire serial interface for transmission of 2-channel (stereo) Pulse Code Modulation digital data for DACs. Data is sent in 2's complement format MSB first. The receiver ignores extra bits from the transmitter, if more than 16 bits are transmitted. In case byte length is less than 16 bits, data is still 2's complement and unspecified bits are set to zero.

Word Select pin (WSI-pin) can be configured in MAS9560. The default setting is: WSI = '0' when data for Channel 1 (left channel) is read, and WSI = '1' when Channel 2 (right channel) is read. This can be changed with POL byte (see register description for $I^2S$ Interface Control Register – p. 17).

Left justified format varies also depending on the delay before the first data byte. Default delay is one clock pulse, but this delay can be configured with DEL bit.

MAS9560 supports only Left-Justified Format.

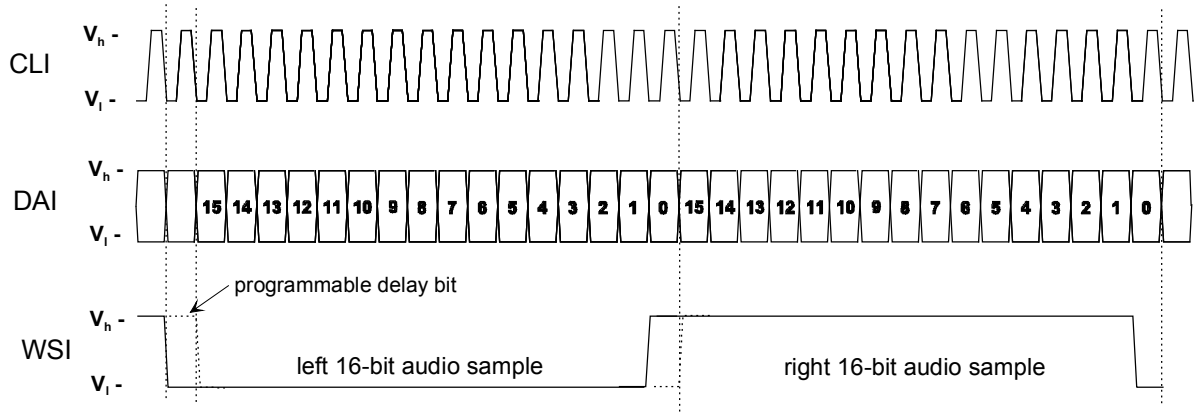



**Figure 1**. I²S Bus

◆ Resetting Registers

When I²C is used:
First register 0x00 is the reset register, writing to which will set all registers to default values. Writing to register 0x00 sets default values to all registers, after which following data will be written to registers as incrementing starts. However, note that when starting data write with the reset sequence, the byte following the reset address is unused and the byte after that is written to register 0x01 (DW-byte, Reset-address-byte, unused data byte, data byte for register 0x01). On-chip incremental counter is 4-bits long: at address 0x0F incrementing stops.

When SPI is used:
Writing to the first register (0x00) resets all registers. In case writing sequence is started with reset, the byte following the reset address is unused, similarly to I²C-mode.

Register reset can be performed externally by setting XRESET pin low.

## CONTROL REGISTERS

MAS9560 has 11 on-chip registers, which are controlled through I²C- or SPI-bus (see section Control Interfaces above). Register byte length is 8 bits for all registers, however, some bits are unused and their value is not set and can vary (they are non-repeatable). Reset register is write-only, all other registers permit read and write access.

◆ **Register Map**

| Sub-Address | Register |
|---|---|
| 0x00 | Reset Register |
| 0x01 | Block Control Register |
| 0x02 | Mode Control Register |
| 0x03 | I²S-Interface Control Register |
| 0x04 | Left Headphone Volume Control |
| 0x05 | Right Headphone Volume Control |
| 0x06 | Earpiece Volume Control |
| 0x07 | Loudspeaker Volume Control |
| 0x08 | Left Input Aux Gain Control |
| 0x09 | Right Input Aux Gain Control |
| 0x0A | Ain Input Gain Control |
| 0x0B… 0x0F | Unused |

◆ **Register Description**

| Name | Sub-Address | Direction | Default after Reset | Function |
|---|---|---|---|---|
| **Reset Register** | 0x00 | Write | 0x00 | |
| Reset | 0xXX | Write | X | Writing to the register clears all internal registers to their default reset values.<br>Register value cannot be read. |
| **Block Control Register** | 0x01 | R/W | 0x00 | Ignored, if Standby or Zero Power Mode |
| PDAC | 0x01[7] | R/W | 0 | DAC power: 1 = on, 0 = off |
| PAIN | 0x01[6] | R/W | 0 | AIN power: 1 = on, 0 = off |
| PAUX | 0x01[5] | R/W | 0 | AUX power: 1 = on, 0 = off |
| PL | 0x01[4] | R/W | 0 | Loudspeaker driver power: 1 = on, 0 = off |
| PE | 0x01[3] | R/W | 0 | Earpiece driver power: 1 = on, 0 = off |
| PRH | 0x01[2] | R/W | 0 | Right Headphone driver power:<br>1 = on, 0 = off |
| PLH | 0x01[1] | R/W | 0 | Left Headphone driver power:<br>1 = on, 0 = off |
| PCH | 0x01[0] | R/W | 0 | Common Headphone driver power:<br>1 = on, 0 = off |
| **Mode Control Register** | 0x02 | R/W | 0x00 | |
| - | 0x02[7:5] | - | - | Unused |
| BYPLDO | 0x02[4] | R/W | 0 | Bypass LDO (in non-LDO mode only):<br>1 = on (bypass LDO with 100 ohm on-chip resistor connected between VLDO and VBAT)<br>0 = off (LDO not bypassed, so on-chip resistor not connected between VLDO and VBAT) |
| SNLDOM | 0x02[3] | R/W | 0 | Select Non-LDO mode: 1 = on, 0 = off<br>LDO is always disabled at Zero Power Mode |
| SMM | 0x02[2] | R/W | 0 | Select Stereo/Mono mode:<br>1 = Mono, 0 = Stereo<br>In Mono Mode AUXL and AUXR are combined together and only left channel DAC signal is used. |

| | | | | |
|---|---|---|---|---|
| PM | 0x02[1:0] | R/W | 00 | Power Mode [1:0]<br>00 Zero Power Mode<br>01 Standby Mode<br>11 Operating Mode<br>10 Undefined (do not use) |
| **$I^2S$ Control Register** | 0x03 | R/W | 0x00 | |
| - | 0x03[7:5] | - | - | Unused |
| POL | 0x03[4] | R/W | 0 | Invert Word Strobe Input (WSI) polarity:<br>POL = 0 -> Left Channel @ WSI = 0<br>POL = 1 -> Right Channel @ WSI = 0 |
| DEL | 0x03[3] | R/W | 0 | Delayed Bit: 1 = Delay, 0 = no Delay |
| SR | 0x03[2:0] | R/W | 000 | Sample Rate [2:0]<br>000, 110 or 111: sample rate defined by WSI, DAC data not filtered.<br>SR[2:0] LP Filter –3dB frequency:<br>001 $f_{CLI}$/128 * 0.65<br>010 $f_{CLI}$/64 * 0.65<br>011 $f_{CLI}$/32 * 0.65<br>100 $f_{CLI}$/16 * 0.65<br>101 $f_{CLI}$/8 * 0.65<br>$f_{CLI}$ refers to I2S clock (CLI pin) frequency.<br>The above mentioned SR[2:0] register bits allow filtering the DAC output by setting the filter frequency.<br>An example: DAC data is given in stereo mode as 16 bit data. Sampling frequency WSI = 8 kHz, and CLI frequency is 2*16*8 kHz (2 channels, 16 bit each, 8 kHz sampling freq). Highest signal frequency is 4 kHz (according to Nyqvist theorem), and thus low pass filtering can be set to 4 kHz. Now SR[2:0] = 011, which sets –3 dB frequency to 5.2 kHz (= 2*16*8 kHz / 32*0.65). |
| **Left Headphone Volume Register** | 0x04 | R/W | 0 | |
| - | 0x04[7:5] | - | - | Unused |
| LHV | 0x04[4:0] | R/W | 00000 | LHV[4:0] Left Headphone volume gain<br>00000 Mute<br>00001 -30 dB<br>... in steps of 1.5 dB<br>11001...11111 6 dB |

| | | | | |
|---|---|---|---|---|
| **Right Headphone Volume Register** | 0x05 | R/W | 0 | |
| - | 0x05[7:5] | - | - | Unused |
| RHV | 0x05[4:0] | R/W | 00000 | RHV[4:0] Right Headphone volume gain<br>00000 Mute<br>00001 -30 dB<br>... in steps of 1.5 dB<br>11001...11111 6 dB |
| **Earpiece Volume Register** | 0x06 | R/W | 0 | |
| - | 0x06[7:5] | - | - | Unused |
| EV | 0x06[4:0] | R/W | 00000 | EV[4:0] Earpiece volume gain<br>00000 Mute<br>00001 -30 dB<br>... in steps of 1.5 dB<br>11001...11111 6 dB |
| **Loudspeaker Volume Register** | 0x07 | R/W | 0 | |
| - | 0x07[7:5] | - | - | Unused |
| LV | 0x07[4:0] | R/W | 00000 | LV[4:0] Loudspeaker volume gain<br>00000 Mute<br>00001 -30 dB<br>... in steps of 1.5 dB<br>11101...11111 12 dB |
| **Left AUX Gain Register** | 0x08 | R/W | 0 | |
| - | 0x08[7:5] | - | - | Unused |
| ALV | 0x08[4:0] | R/W | 00000 | ALV[4:0] Left AUX pre-amplifier gain<br>00000 Mute<br>00001 -20 dB<br>... in steps of 2 dB<br>10101...11111 20 dB |

| **Right AUX Gain Register** | 0x09 | R/W | 0 | |
|---|---|---|---|---|
| - | 0x09[7:5] | - | - | Unused |
| ARV | 0x09[4:0] | R/W | 00000 | ARV[4:0] Right AUX pre-amplifier gain<br>00000 Mute<br>00001 -20 dB<br>... in steps of 2 dB<br>10101...11111 20 dB |
| **AIN Gain Register** | 0x0A | R/W | 0 | |
| - | 0x0A[7:5] | - | - | Unused |
| AIV | 0x0A[4:0] | R/W | 00000 | AIV[4:0] AIN pre-amplifier gain<br>00000 Mute<br>00001 -20 dB<br>... in steps of 2 dB<br>10101...11111 20 dB |

**Note:** Unused register bit values are undefined.

## I²C BUS TIMING

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Input Low Voltage | SCLK, SDI | | | | tbd | IOVDD |
| Input High Voltage | SCLK, SDI | | tbd | | | IOVDD |
| Start Condition Setup Time | SCLK, SDI | | tbd | | | ns |
| Stop Condition Setup Time | SCLK, SDI | | tbd | | | ns |
| Data Setup Time before clock rising edge | SCLK, SDI | | tbd | | | ns |
| Data Hold Time after clock falling edge | SCLK, SDI | | tbd | | | ns |
| Clock Low Pulse Time | SCLK | | tbd | | | ns |
| Clock High Pulse Time | SCLK | | tbd | | | ns |
| Bus Frequency | SCLK | | | | tbd | MHz |
| Data Output Low Voltage | SCLK, SDI | $I_{LOAD}$ = 3 mA | | | tbd | V |
| Data Output High Leakage Current | SCLK, SDI | $V_{SDI}$ = 5 V | | | tbd | µA |
| Data Output Hold Time after clock falling edge | SCLK, SDI | | tbd | | | ns |
| Data Output Setup Time before clock rising edge | SCLK, SDI | $f_{I2C}$ = 1MHz | tbd | | | ns |

## SPI BUS TIMING

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Input Low voltage | SDI, SCLK | | | | tbd | IOVDD |
| Input High voltage | | | tbd | | | IOVDD |
| Input Impedance | | | | | tbd | pF |
| Input Leakage Current | | 0 V < Input < IOVDD | tbd | | tbd | µA |
| Input Setup Time before clock rising edge | SDI, XCS | | Tbd | | | ns |
| Input Hold Time after clock falling edge | SDI, XCS | | Tbd | | | ns |
| Output Low Voltage | SDO | $I_{LOAD}$ = 0.5 mA, IOVDD = 1.8 V | | | tbd | V |
| Output High Voltage | SDO | $I_{LOAD}$ = -0.5 mA, IOVDD = 1.8 V | tbd | | | V |
| Clock Frequency, read access | SCLK, SDI, SDO | $C_{LOAD}$ = 20 pF, IOVDD = 3.3 V | | tbd | tbd | MHz |
| Clock Frequency, read access | SCLK, SDI, SDO | $C_{LOAD}$ = 20 pF, IOVDD = 1.8 V | | tbd | tbd | MHz |
| Clock Frequency, write access | SCLK, SDI | $C_{LOAD}$ = 20 pF, IOVDD = 3.3 V | | tbd | tbd | MHz |
| Clock Frequency, write access | SCLK, SDI | $C_{LOAD}$ = 20 pF, IOVDD = 1.8 V | | tbd | tbd | MHz |

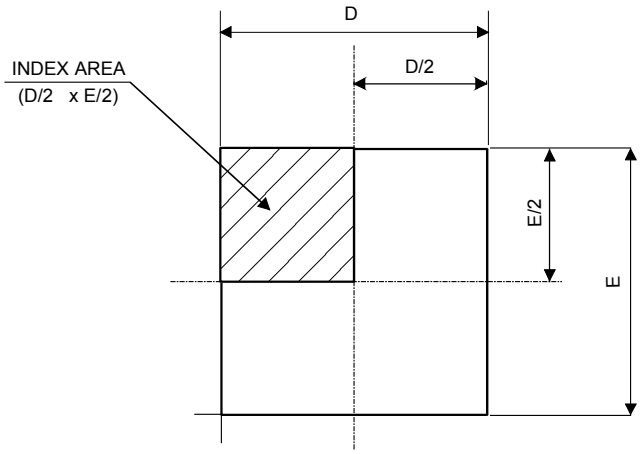
## I²S BUS TIMING

LSVDD = VBAT = 3.6V, EPVDD = HPVDD = VLDO = 2.86V (LDO-mode), -40°C ≤ $T_A$ ≤ +85°C, typical values at $T_A$ = +27°C, unless otherwise noted

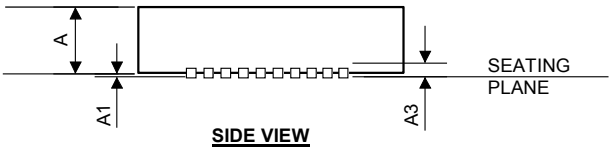
| Parameter | Pin Name | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Input Low Voltage | DAI, CLI, WSI | | | | tbd | IOVDD |
| Input High voltage | | | tbd | | | IOVDD |
| Input Impedance | | | | | tbd | pF |
| Input Leakage Current | | 0 V < Input < IOVDD | tbd | | tbd | µA |
| Input Setup Time before clock rising edge | DAI, WSI | | tbd | | | ns |
| Input Hold Time after clock falling edge | DAI, WSI | | tbd | | | ns |
| Clock Frequency (Note 1) | CLI, DAI | | | | tbd | MHz |

**Note 1:** I²S clock (CLI) frequency ratio will affect to DAC sampling in oversampling mode. See Control Register description (p. 18)

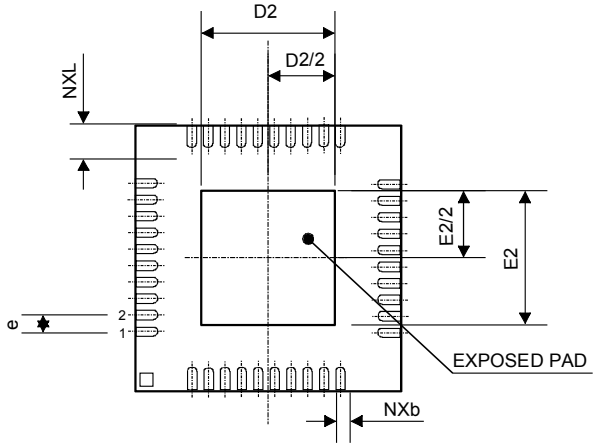
## PACKAGE (QFN 6x6 40ld) OUTLINE




**TOP VIEW**




**SIDE VIEW**




**BOTTOM VIEW**

| Parameter | Typ | Unit |
|---|---|---|
| D | 6 | mm |
| E | 6 | mm |
| A | 0.9 | mm |
| A1 | 0.02 | mm |
| D2 | 4.15 | mm |
| E2 | 4.15 | mm |
| e | 0.5 | mm |
| NXb | 0.23 | mm |

## SOLDERING INFORMATION

TBD

## EMBOSSED TAPE SPECIFICATIONS

TBD

## REEL SPECIFICATIONS

TBD

## ORDERING INFORMATION

| Product Code | Product | Package | Comments |
|---|---|---|---|
| MAS9560A1 | Stereo Audio Driver DAC | QFN 6x6 40ld | |

## LOCAL DISTRIBUTOR

## MICRO ANALOG SYSTEMS OY CONTACTS


| | |
|---|---|
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