



TF2007U

Half-Bridge Gate Driver

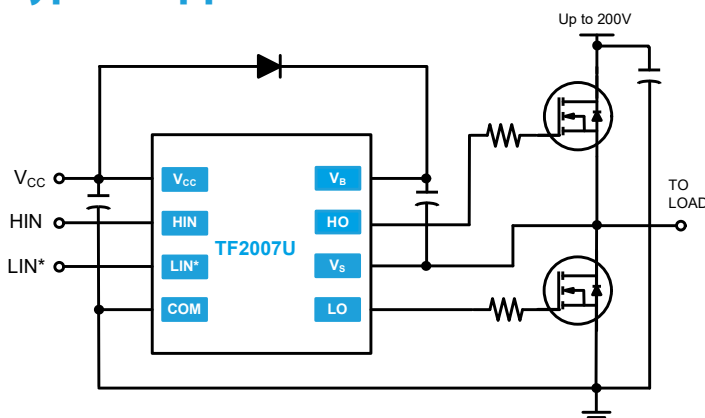
Features

- Floating high-side driver in bootstrap operation to 200V
- Drives two N-channel MOSFETs or IGBTs in a half bridge configuration
- Designed for enhanced performance in noisy motor applications
- 290mA source/600mA sink output current capability
- Outputs tolerant to negative transients
- Internal dead time of 420ns to protect MOSFETs
- Wide low side gate driver supply voltage: 10V to 20V
- Logic input (HIN and LIN*) 3.3V capability
- Schmitt triggered logic inputs
- Undervoltage lockout for V_{CC} (logic and low side supply)
- Extended temperature range: -40°C to +125°C

Applications

- Motor Controls
- DC-DC Converters
- AC-DC Inverters
- Motor Drives

Typical Application

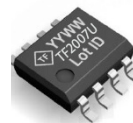


Description

The TF2007U is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductors's high voltage process enables the TF2007U high side to switch to 200V in a bootstrap operation.

The TF2007U logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. TF2007U has a fixed internal deadtime of 420ns (typical).

The TF2007U is offered in a SOIC-8(N) package and operates over an extended -40 °C to +125 °C temperature range.



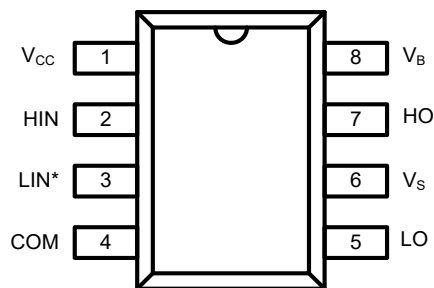
SOIC-8(N)

Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2007U-TAU	SOIC-8(N)	Tube / 100	YYWW TF2007U
TF2007U-TAH	SOIC-8(N)	T&R / 2500	Lot ID

Pin Diagrams



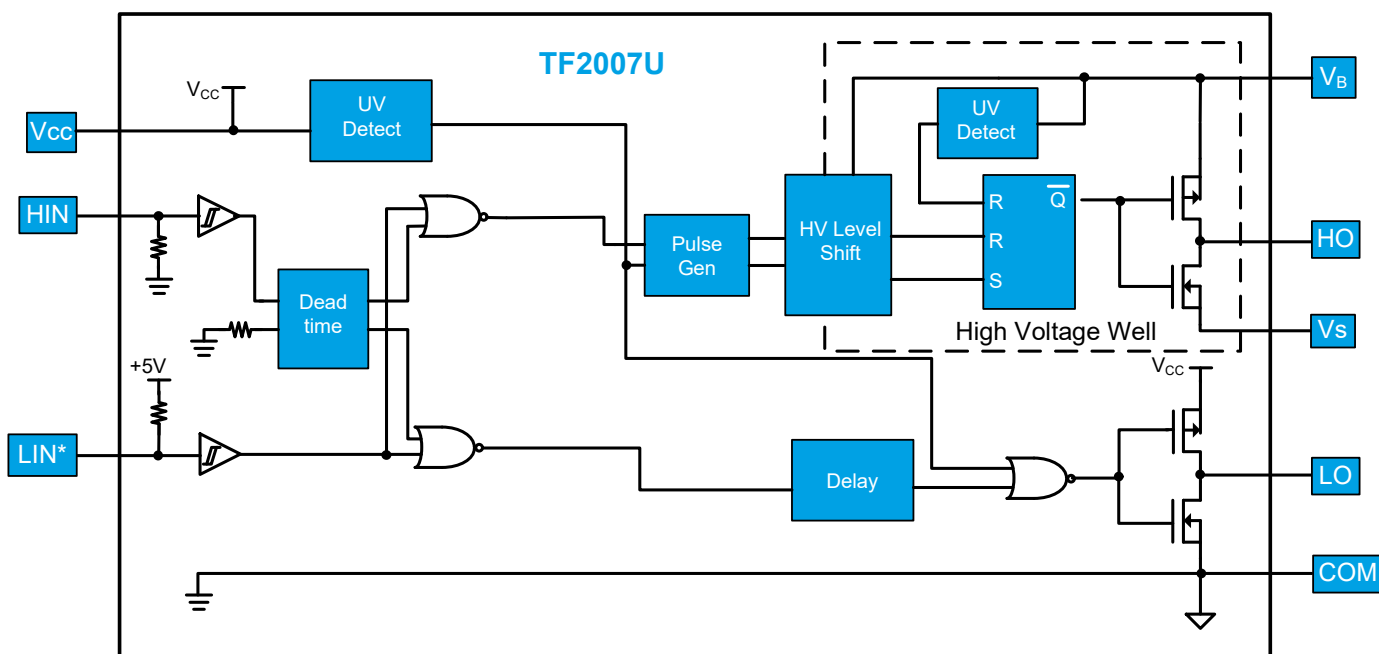
Top View: SOIC-8

TF2007U

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
V_{CC}	1	Logic and low side supply
HIN	2	Logic input for high-side gate driver output in phase with HO
LIN*	3	Logic input for low-side gate driver output out of phase with LO
COM	4	Low-side and logic return
LO	5	Low-side gate drive output
V_S	6	High-side floating supply return
HO	7	High-side gate drive output
V_B	8	High-side floating supply

Functional Block Diagram





Half-Bridge Gate Driver

Absolute Maximum Ratings (NOTE1)

V_B - High side floating supply voltage.....-0.3V to +224V
 V_S - High side floating supply offset voltage... V_B -24V to V_B +0.3V
 V_{HO} - High side floating output voltage..... V_S -0.3V to V_B +0.3V
 dV_S/dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low-side fixed supply voltage.....-0.3V to +24V
 V_{LO} - Low-side output voltage.....-0.3V to V_{CC} +0.3V
 V_{IN} - Logic input voltage (HIN and LIN*).....-0.3V to V_{CC} +0.3V

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

P_D - Package power dissipation at $T_A \leq 25^\circ\text{C}$
 SOIC-8.....0.625W

SOIC-8(N) Thermal Resistance (NOTE2)

θ_{JA}200 $^\circ\text{C}/\text{W}$

T_J - Junction operating temperature.....+150 $^\circ\text{C}$

T_L - Lead Temperature (soldering, 10 seconds).....+300 $^\circ\text{C}$

T_{stg} - Storage temperature-55 to 150 $^\circ\text{C}$

NOTE2 When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	NOTE3	200	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN*)	0	5	V
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

NOTE3 Logic operational for V_S of -5V to +200V.



DC Electrical Characteristics (NOTE4)

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" (HIN) & Logic "0" (LIN*) input voltage	$V_{CC} = 10V$ to $20V$	2.5			V
V_{IL}	Logic "0" (HIN) & Logic "1" (LIN*) input voltage	NOTE 5			0.8	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2mA$		0.05	0.2	
V_{OL}	Low level output voltage, V_O	$I_O = 2mA$		0.02	0.1	
I_{LK}	Offset supply leakage current	$V_B = V_S = 200V$			50	μA
I_{BSQ}	Quiescent V_{BS} supply current	$V_{IN} = 0V$ or $5V$		7		
I_{CCQ}	Quiescent V_{CC} supply current	$V_{IN} = 0V$ or $5V$		350	500	
I_{IN+}	Logic "1" input bias current	$HIN = 5V, LIN^* = 0V$		3	10	
I_{IN-}	Logic "0" input bias current	$HIN = 0V, LIN^* = 5V$			5	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8.0	8.9	9.8	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold			6.3		V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold			5.2		V
I_{O+}	Output high short circuit pulsed current	$V_O = 0V, PW \leq 10 \mu s$	130	290		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15V, PW \leq 10 \mu s$	270	600		

NOTE4 The V_{IH} , V_{IL} , and I_{IN} parameters are applicable to the two logic input pins: HIN and LIN*. The V_O and I_O parameters are applicable to the respective output pins: HO and LO

NOTE5 For optimal operation, it is recommended that the input pulse (to HIN and LIN*) should have an amplitude of 2.5V minimum with a pulse width of 800ns minimum.



AC Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $C_L = 1000pF$, and $T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propagation delay	$V_S = 0V$		100	200	ns
t_{off}	Turn-off propagation delay	$V_S = 200V$		100	200	
t_{DM}	Delay matching, HS & LS turn-on/turn-off				50	
t_r	Turn-on rise time	$V_S = 0V$		70	150	
t_f	Turn-off fall time			35	90	
t_{DT}	Deadtime: $t_{DT LO-HO}$ & $t_{DT HO-LO}$		300	420	650	



Timing Waveforms

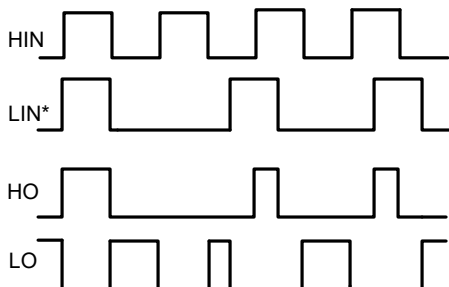


Figure 1. Input / Output Timing Diagram

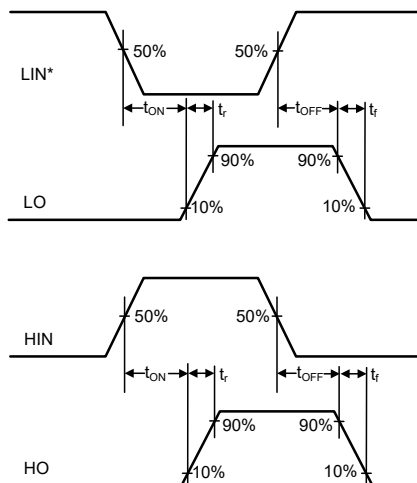


Figure 2. Switching Time Waveform Definitions

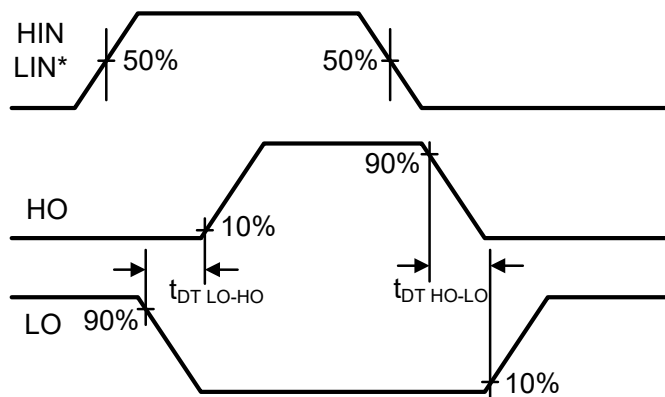
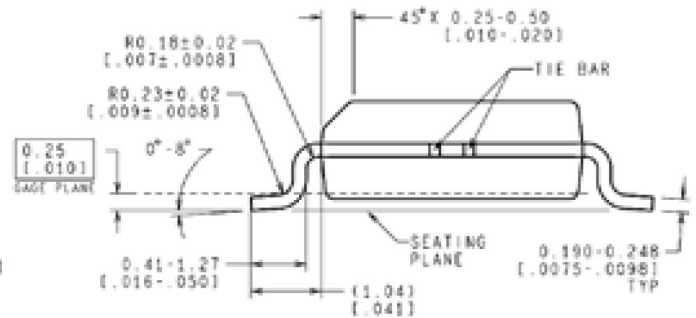
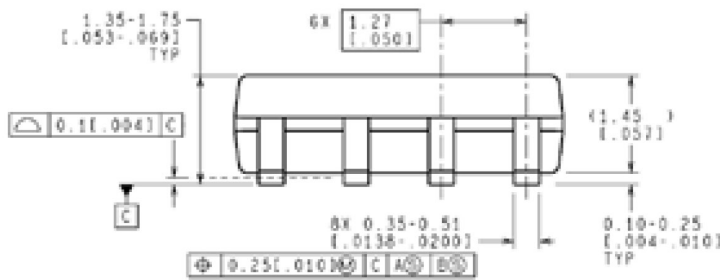
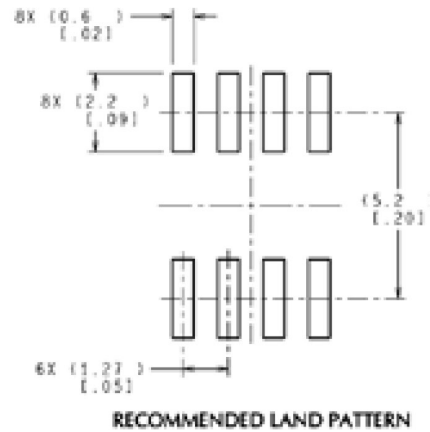
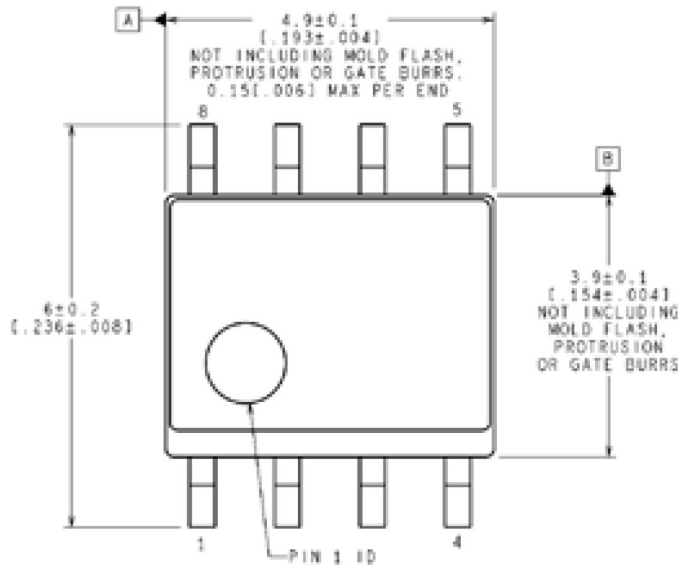


Figure 3. Deadtime Waveform Definitions



Package Dimensions (SOIC-8 N)

Please contact support@telefunkensemi.com for package availability.



NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [] ARE INCHES
DIMENSIONS IN () FOR REFERENCE ONLY



Revision History

Rev.	Change	Owner	Date
1.0	First release, AI datasheet	Keith Spaulding	2/5/2019
1.1	Addition of Note 5	Duke Walton	2/7/2020

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