National Semiconductor

July 2007

DS15EA101
0.15 to 1.5 Gbps Adaptive Cable Equalizer with LOS Detection

General Description

The DS15EA101 is an adaptive equalizer optimized for equalizing data transmitted over copper cables. The DS15EA101 operates over a wide range of data rates from 150 Mbps to 1.5+ Gbps and automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 35 dB at 750 MHz.

The DS15EA101 allows either single-ended or differential input drive. This enables equalization of coaxial cables as well as differential twin-ax and twisted pair cables.

Additional features include an LOS output and an output enable which, when tied together, disable the output when no signal is present.

The DS15EA101 is powered from a single 3.3V supply and consumes 210 mW at 1.5 Gbps. It operates over the full −40°C to +85°C industrial temperature range and is available in a space saving 4 x 4 mm LLP-16 package which allows for high density placement of components in multi-channel applications.

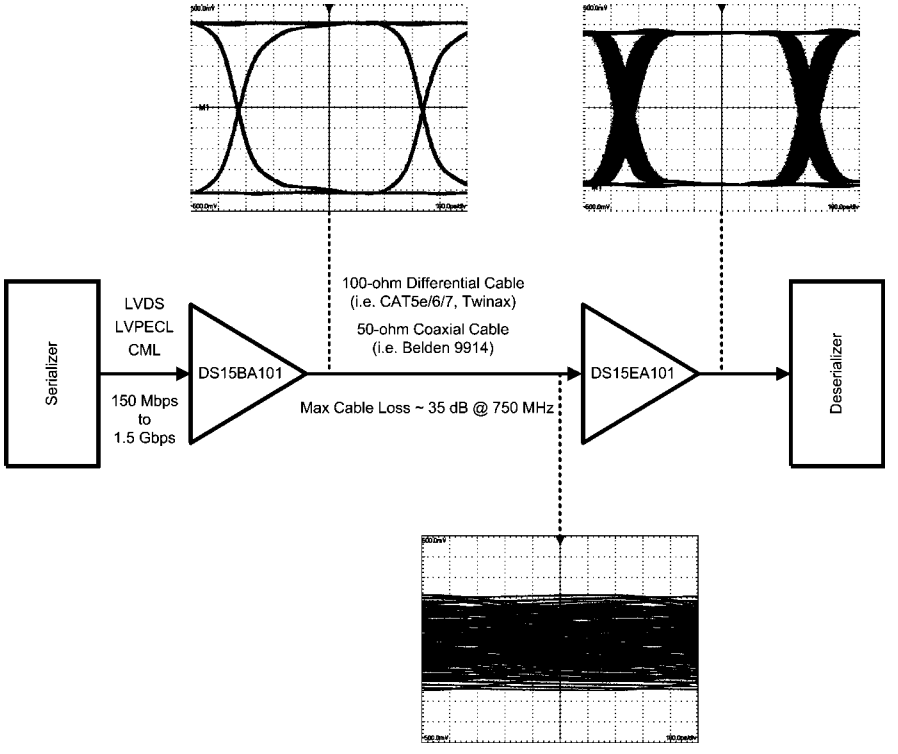
Features

- Automatic equalization of coaxial, twin-ax and twisted pair cables
- High data rates: 150 Mbps to 1.5+ Gbps
- Up to 35 dB of boost at 750 MHz
- LOS detection and output enable
- Single-ended or differential input
- 50Ω differential outputs
- Low power operation, 210 mW (typ) at 1.5 Gbps
- Industrial -40°C to +85°C temperature
- Space-saving 4 x 4 mm LLP-16 package

Applications

- Cable extention applications
- Security cameras
- Remote LCDs and LED panels
- Data recovery equalization

Typical Application



20201701

Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.5V to 3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance	
θ_{JA}SQA16A	+42.1°C/W
θ_{JC} SQA16A	+8.2°C/W
ESD Rating (HBM)	8 kV
ESD Rating (MM)	250V

Recommended Operating Conditions

Supply Voltage (VCC)	3.3V ±5%
Input Coupling Capacitance	1.0 µF
Loop Capacitor (Connected between CAP+ and CAP-)	1.0 µF
Operating Free Air Temperature (T_A)	-40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2, 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CM}	Input Common Mode Voltage		IN+, IN-		1.9		V
V_{ID}	Input Voltage	At DS15EA101 input (Notes 4, 6)		720	800	950	mV_{P-P}
V_{OS}	Output Common Mode Voltage		OUT+, OUT-		V_{CC} – V_{OUT}/2		V
V_{OUT}	Output Voltage Swing	50Ω load, differential			750		mV_{P-P}
V_{LOS}	LOS Output Voltage	Valid signal not present	LOS	2.6			V
		Valid signal present				0.4	V
$V_{IN(EN)}$	$\overline{EN}$ Input Voltage	Min to disable outputs	$\overline{EN}$	3.0			V
		Max to enable outputs				0.8	V
I_{CC}	Supply Current	(Note 7)			63	77	mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{IN}	Input Data Rate		IN+, IN-	150		1500	Mbps
t_{TRJ}	Total Residual Jitter @ BER-12 (Note 8)	1.5 Gbps 25m CAT5e (Belden 1700A), (Note 3)			0.25		UI
		1.0 Gbps 50m CAT5e (Belden 1700A), (Note 3)			0.25		UI
		0.5 Gbps 100m CAT5e (Belden 1700A), (Note 3)			0.25		UI
		1.5 Gbps 50m CAT7 (Siemon Tera), (Note 3)			0.25		UI
		1.5 Gbps 75m CAT7 (Siemon Tera), (Note 3)			0.30		UI
		1.0 Gbps 100m CAT7 (Siemon Tera), (Note 3)			0.40		UI
		1.5 Gbps 200m Belden 9914, (Note 3)			0.25		UI
tTLH	Transition Time from Low to High	20% – 80%, (Note 4)	OUT+, OUT-		100	220	ps
tTHL	Transition Time from High to Low	20% – 80%, (Note 4)			100	220	ps
R_{OUT}	Output Resistance	single-ended, (Note 5)			50		Ω

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to 0 volts.

Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Note 4: Specification is guaranteed by characterization.

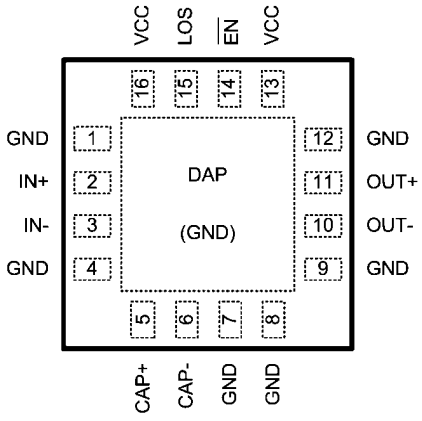
Note 5: Specification is guaranteed by design.

Note 6: The maximum input voltage amplitude assumes a DC-balanced signal.

Note 7: Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased.

Note 8: The total residual jitter at BER-12 was calculated as DJ+14.1xRJ, where DJ is deterministic jitter and RJ is random jitter. The jitter is expressed as a portion of a unit interval (UI). One UI is a reciprocal of a bit rate (or data rate). For example, a 1.5 Gbps (gigabit per second) signal has 1 / (1.5 Gb/s) = 666.67 ps (picosecond) unit interval. A 0.25 UI jitter is equivalent to 0.25 x 666.67 ps = 166.67 ps.

Connection Diagram



16-Pad LLP
Order Number DS15EA101SQ
See NS Package Number SQA16A

Pin Descriptions

Pin #	Name	Description
1	GND	Ground pin.
2	IN+	Non-inverting input pin.
3	IN-	Inverting input pin.
4	GND	Ground pin.
5	CAP+	Loop filter positive pin.
6	CAP-	Loop filter negative pin.
7	GND	Ground pin.
8	GND	Ground pin.
9	GND	Ground pin.
10	OUT-	Inverting output pin.
11	OUT+	Non-inverting output pin.
12	GND	Ground pin.
13	VCC	Power supply pin.
14	$\overline{EN}$	Output enable pin.
15	LOS	Los of signal circuitry output pin.
16	VCC	Power supply pin.

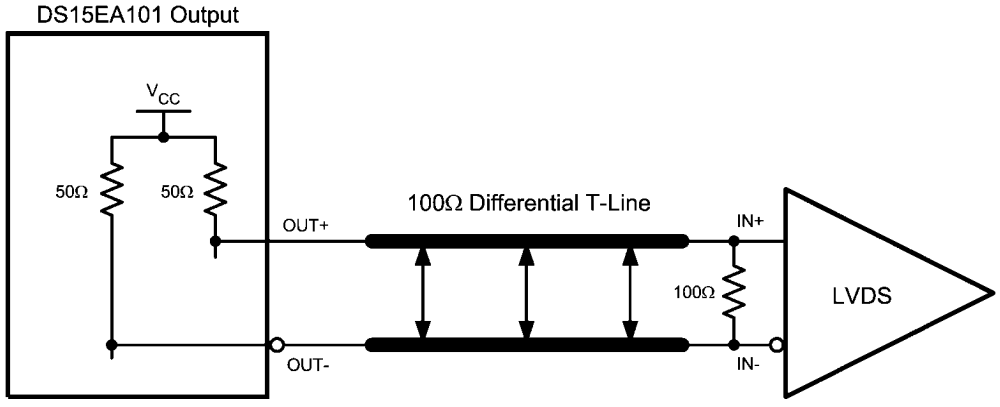
Device Operation

INPUT INTERFACING

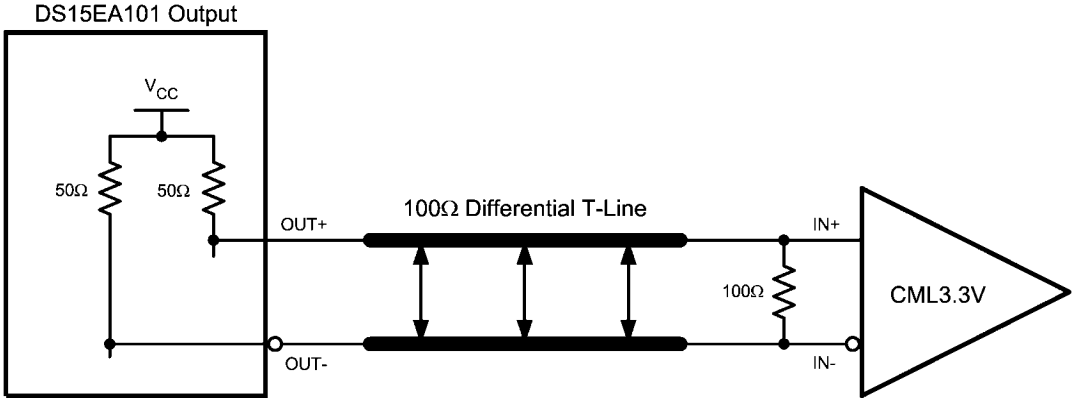
The DS15EA101 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported. If the signal is differential, its amplitude must be 800 mVp-p ±10% (400 mV single-ended). If the signal is single-ended, its amplitude must be 800 mV ±10%.

OUTPUT INTERFACING

The DS15EA101 uses current mode outputs. They are internally terminated with 50Ω. The following two figures illustrate typical DC-coupled interface to common differential receivers and assume that the receivers have high impedance inputs. While most receivers have an input common mode voltage range that can accomodate CML signals, it is recommended to check respective receiver's datasheet prior to implementing the suggested interface implementations.



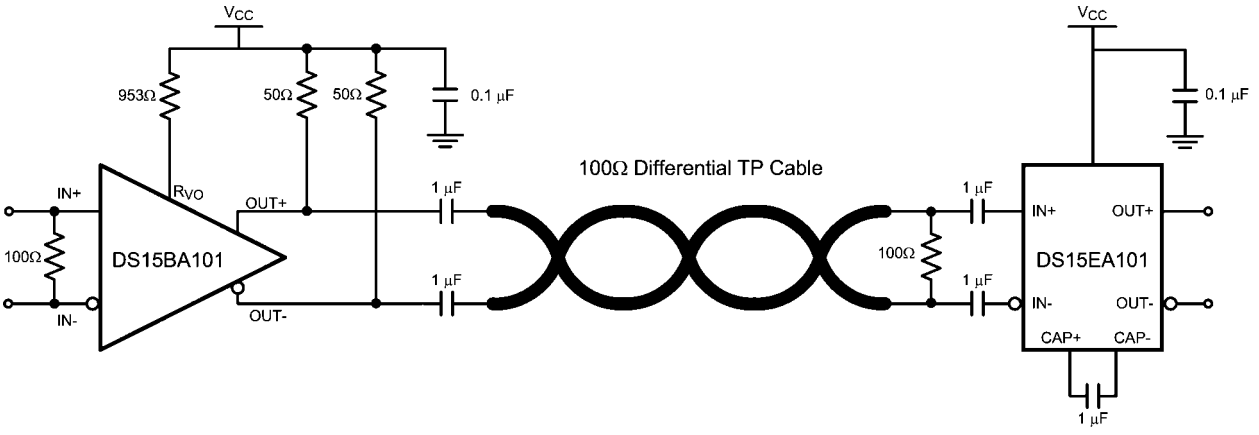
Typical DS15EA101 Output DC-Coupled Interface to an LVDS Receiver



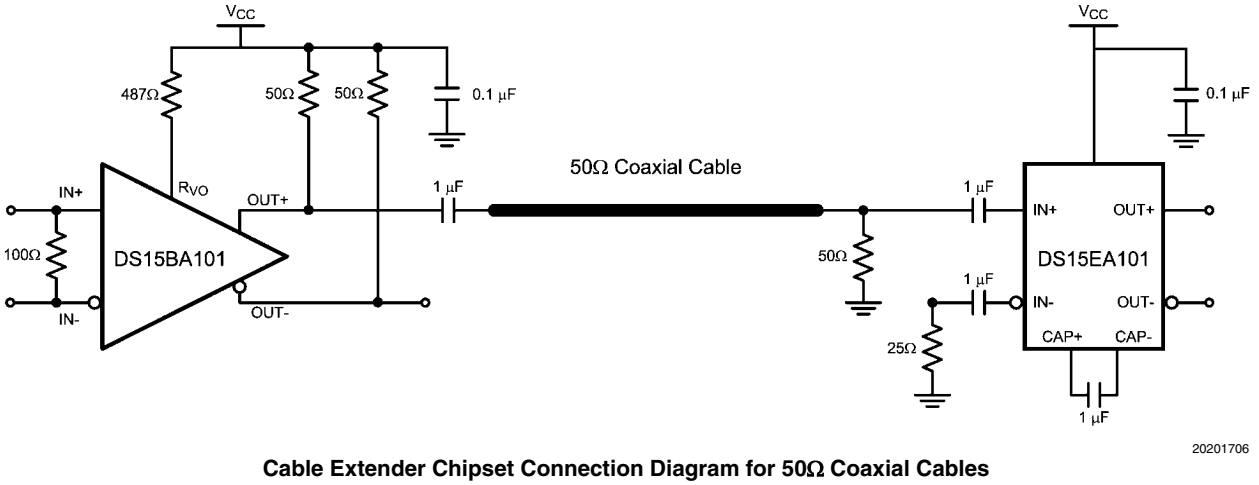
Typical DS15EA101 Output DC-Coupled Interface to a CML Receiver

CABLE EXTENDER APPLICATION

The DS15EA101 together with the DS15BA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and field programmable gate arrays (FPGAs) over 100Ω differential (i.e. CAT5e/6/7 and twinax) and 50Ω coaxial cables. Setting correct DS15BA101 output amplitude and proper cable termination are keys for optimal operation. The following two figures show recommended chipset configuration for 100Ω differential and 50Ω coaxial cables.



Cable Extender Chipset Connection Diagram for 100Ω Differential Cables

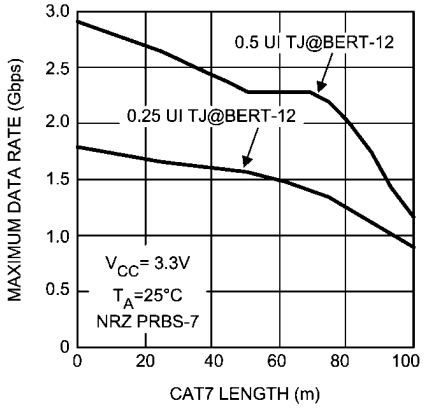


Cable Extender Chipset Connection Diagram for 50Ω Coaxial Cables

REFERENCE DESIGN

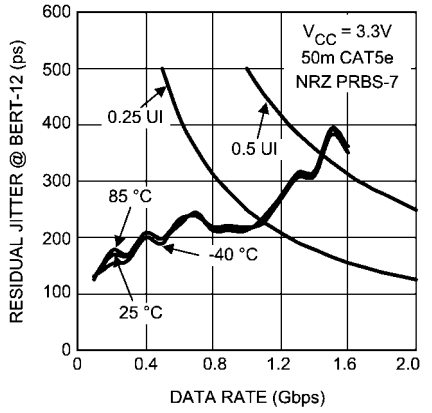
There is a complete reference design (P/N: DriveCable02EVK) available for evaluation of the cable extender chipset (DS15BA101 and DS15EA101). Fore more information visit http://www.national.com/appinfo/lvds/drivecable02evk.html.

Typical Performance



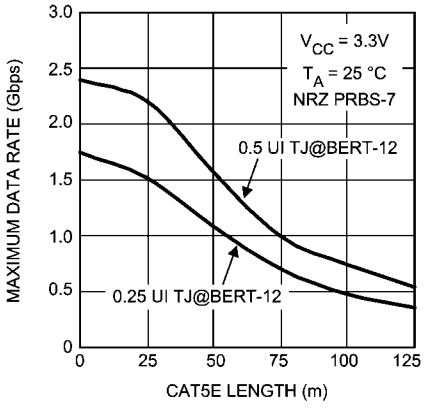
20201710

Maximum Data Rate as a Function of CAT7 (Siemon CAT7 Tera) Length



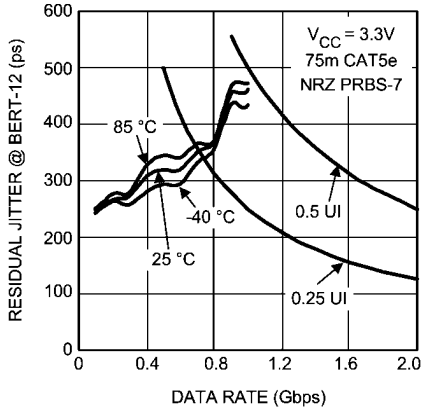
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Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 50m CAT5e



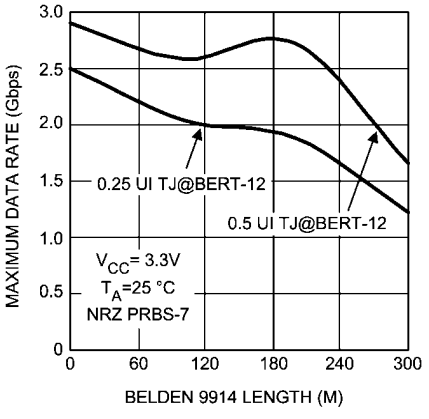
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Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length



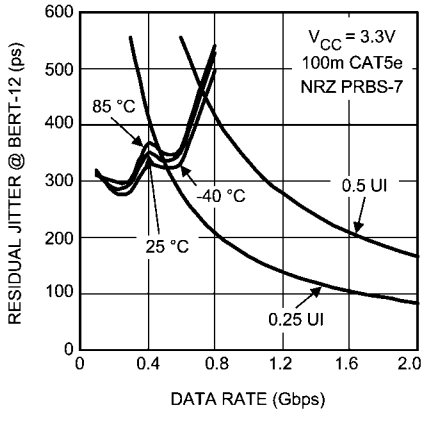
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Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 75m CAT5e



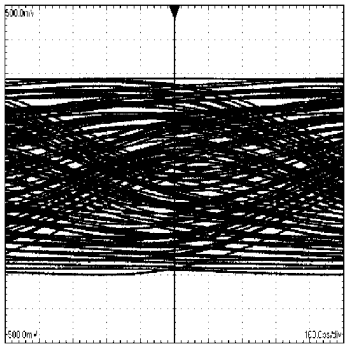
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Maximum Data Rate as a Function of 50Ω Coaxial (Belden 9914) Length



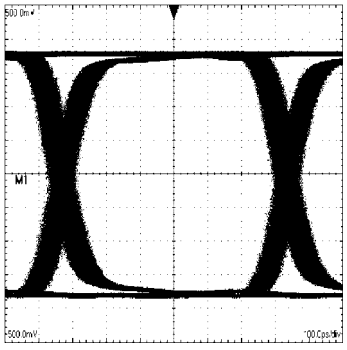
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Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 100m CAT5e



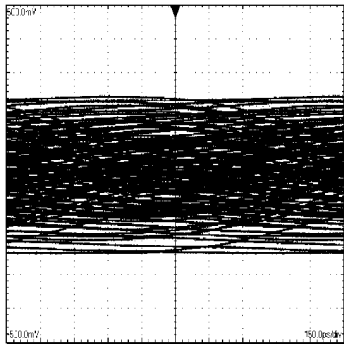
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A 1.5 Gbps NRZ PRBS-7 After 25m CAT5e
V:100 mV / DIV, H:100 ps / DIV



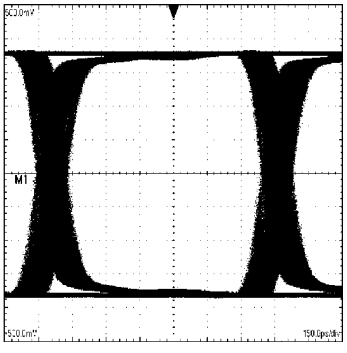
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An Equalized 1.5 Gbps NRZ PRBS-7 After 25m CAT5e
V:100 mV / DIV, H:100 ps / DIV



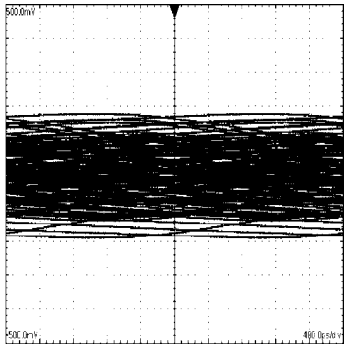
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A 1.0 Gbps NRZ PRBS-7 After 50m CAT5e
V:100 mV / DIV, H:150 ps / DIV



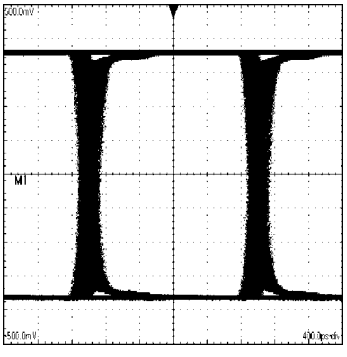
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An Equalized 1.0 Gbps NRZ PRBS-7 After 50m CAT5e
V:100 mV / DIV, H:150 ps / DIV



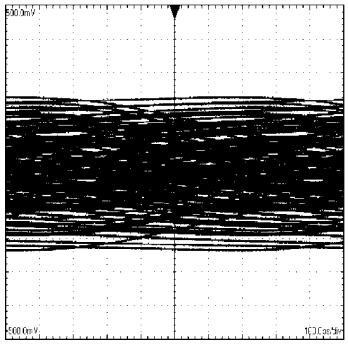
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A 0.5 Gbps NRZ PRBS-7 After 100m CAT5e
V:100 mV / DIV, H:400 ps / DIV



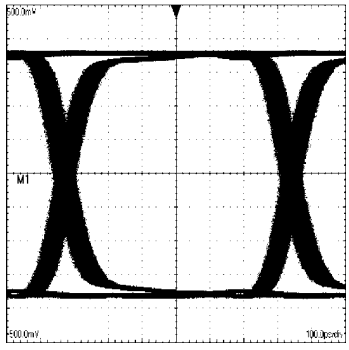
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An Equalized 0.5 Gbps NRZ PRBS-7 After 100m CAT5e
V:100 mV / DIV, H:400 ps / DIV



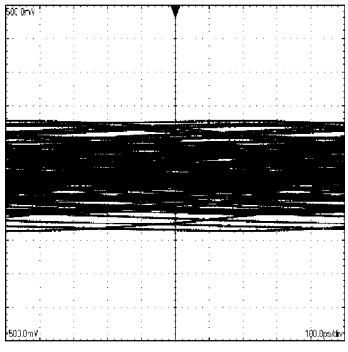
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A 1.5 Gbps NRZ PRBS-7 After 50m CAT7
V:100 mV / DIV, H:100 ps / DIV



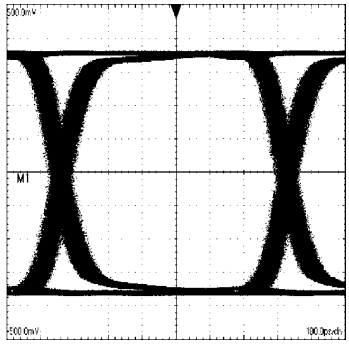
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An Equalized 1.5 Gbps NRZ PRBS-7 After 50m CAT7
V:100 mV / DIV, H:100 ps / DIV



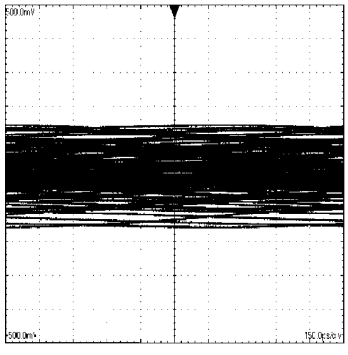
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A 1.5 Gbps NRZ PRBS-7 After 75m CAT7
V:100 mV / DIV, H:100 ps / DIV



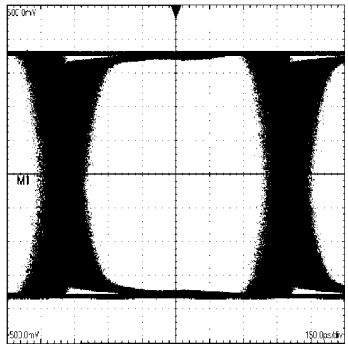
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An Equalized 1.5 Gbps NRZ PRBS-7 After 75m CAT7
V:100 mV / DIV, H:100 ps / DIV



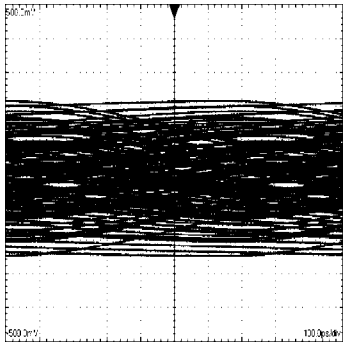
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A 1.0 Gbps NRZ PRBS-7 After 100m CAT7
V:100 mV / DIV, H:150 ps / DIV



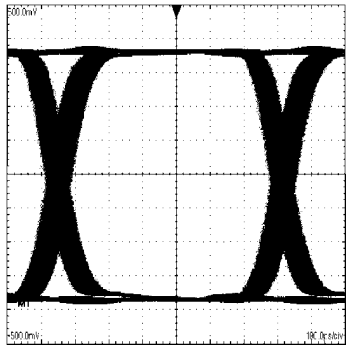
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An Equalized 1.0 Gbps NRZ PRBS-7 After 100m CAT7
V:100 mV / DIV, H:150 ps / DIV



20201732

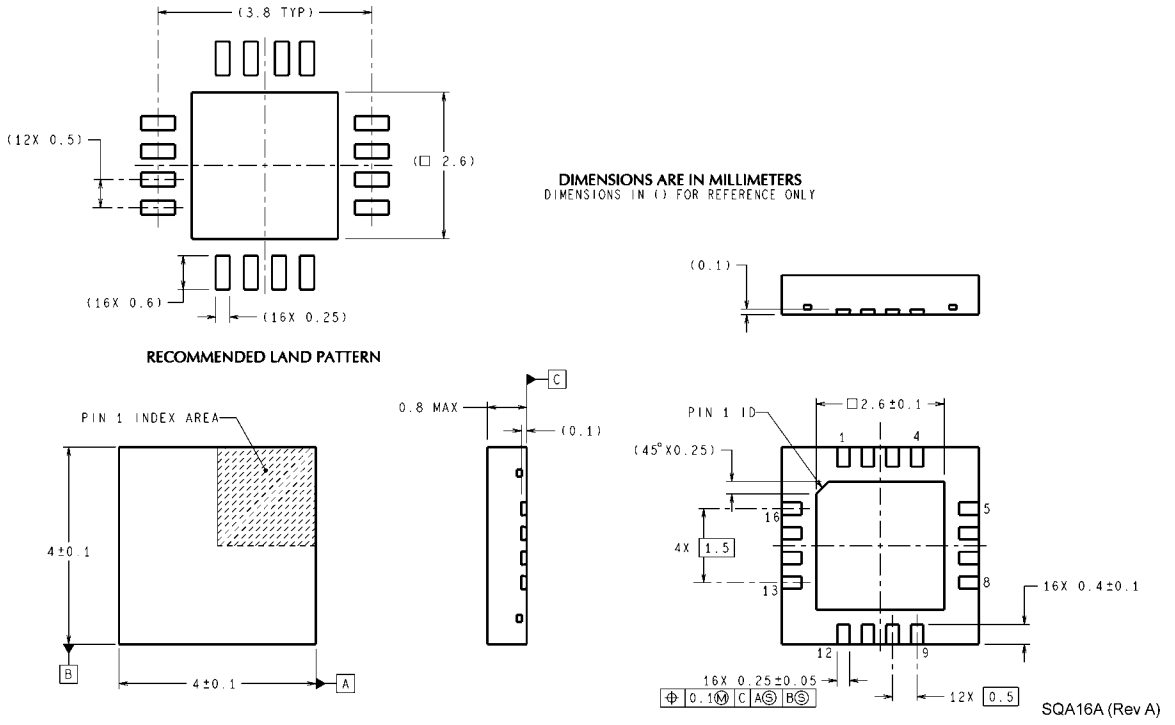
A 1.5 Gbps NRZ PRBS-7 After 200m Belden 9914
V:100 mV / DIV, H:100 ps / DIV



20201733

An Equalized 1.5 Gbps NRZ PRBS-7 After 200m Belden 9914, V:100 mV / DIV, H:100 ps / DIV

Physical Dimensions inches (millimeters) unless otherwise noted



16-Pin LLP
Order Number DS15EA101SQ
NS Package Number SQA16A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

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