

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max $T_A = +25^\circ C$ (Notes 7 & 9)
Q1	40V	45m Ω @ $V_{GS} = 10V$	5.8A
		60m Ω @ $V_{GS} = 4.5V$	4.2A
Q2	-40V	45m Ω @ $V_{GS} = -10V$	-5.8A
		60m Ω @ $V_{GS} = -4.5V$	-4.2A

Description and Applications

This MOSFET is designed to meet the stringent requirements of Automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

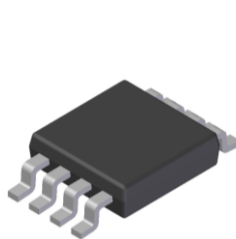
- 3-Phase BLDC Motor
- CCFL Backlighting

Features and Benefits

- Matched N & P $R_{DS(ON)}$ – Minimizes Power Losses
- Fast Switching – Minimizes Switching Losses
- Dual Device – Reduces PCB Area
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability PPAP Capable (Note 4)**

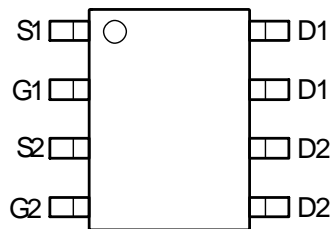
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.074 grams (Approximate)

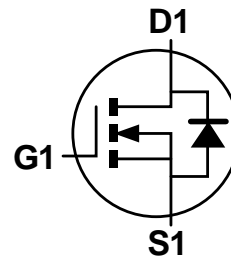


Top View

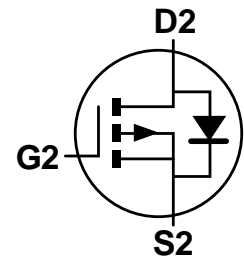
SO-8



Top View



Equivalent Circuit

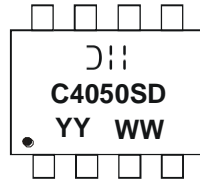


Ordering Information (Note 5)

Part Number	Case	Packaging
DMC4050SSDQ-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to http://www.diodes.com/quality/product_compliance_definitions/.
 5. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



D I = Manufacturer's Marking
 C4050SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY= Year (ex: 16 = 2016)
 WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

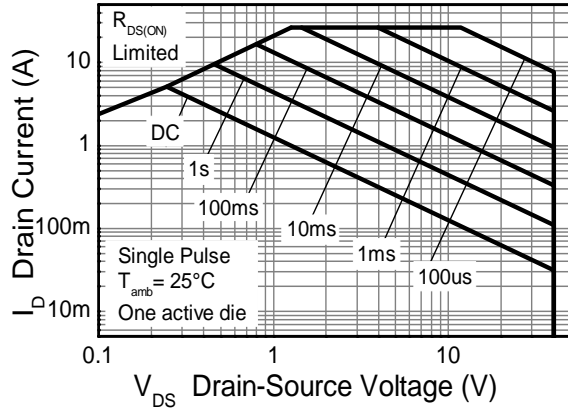
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage		V _{DSS}	40	-40	V
Gate-Source Voltage		V _{GSS}	±20	±20	
Continuous Drain Current	V _{GS} = 10V	(Notes 7 & 9)	5.8	-5.8	A
		T _A = +70°C (Notes 7 & 9)	4.38	-4.52	
		(Notes 6 & 9)	4.2	-4.2	
		(Notes 6 & 10)	5.3	-5.3	
Pulsed Drain Current	V _{GS} = 10V	I _{DM}	24.1	-24.9	
Continuous Source Current (Body Diode)		I _S	2.5	-2.5	
Pulsed Source Current (Body Diode)		I _{SM}	24.1	-24.9	

Thermal Characteristics

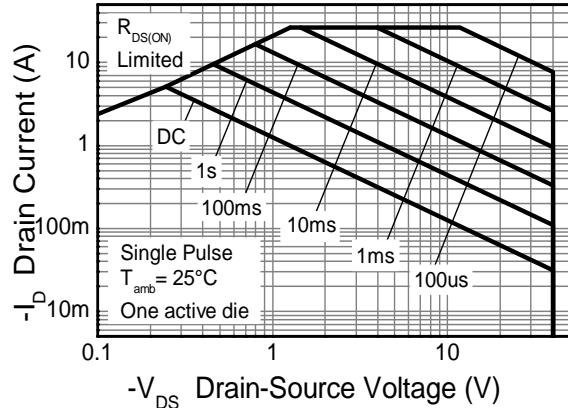
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 6 & 9)	P _D	1.25	10	W
	(Notes 6 & 10)		1.8	14.3	
	(Notes 7 & 9)		2.14	17.2	
Thermal Resistance, Junction to Ambient	(Notes 6 & 9)	R _{θJA}	100		°C/W
	(Notes 6 & 10)		70		
	(Notes 7 & 9)		58		
Thermal Resistance, Junction to Lead		R _{θJL}	51		
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150		°C

- Notes:
- For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - Same as Note (6), except the device is measured at t ≤ 10 sec.
 - Same as Note (6), except the device is pulsed with D = 0.02 and pulse width 300µs.
 - For a dual device with one active die.
 - For a device with two active die running at equal power.
 - Thermal resistance from junction to solder-point (at the end of the drain lead).

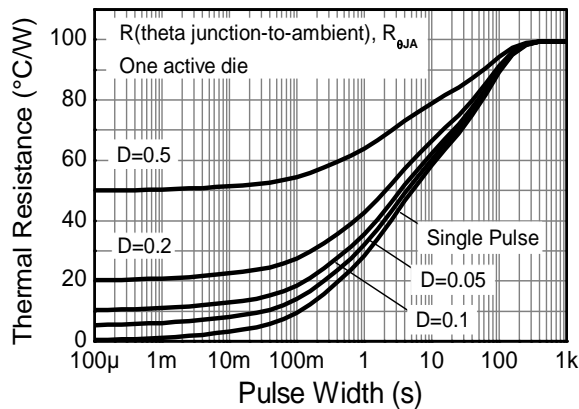
Thermal Characteristics (Continued)



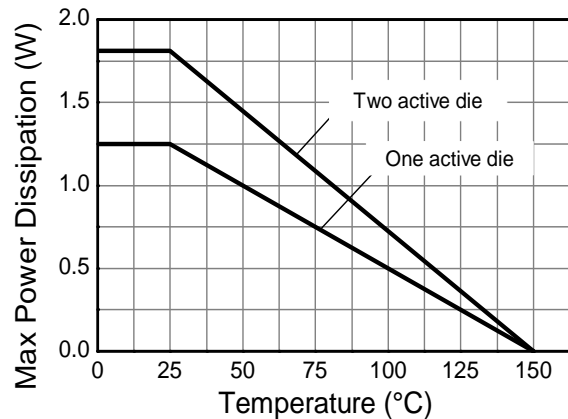
N-channel Safe Operating Area



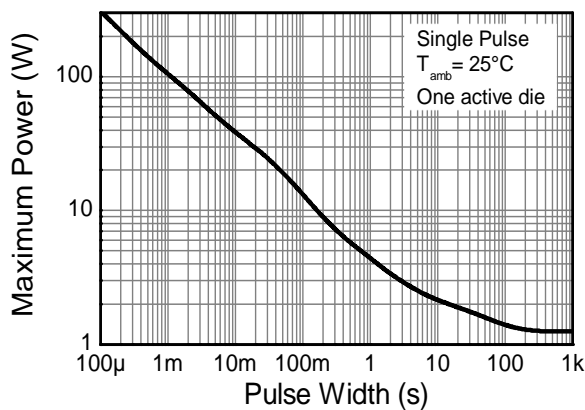
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics (Q1 N-Channel) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 12)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1.0	μA	V _{DS} = 40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 12)						
Gate Threshold Voltage	V _{GS(TH)}	0.8	1.3	1.8	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	20	45	mΩ	V _{GS} = 10V, I _D = 3A
			33	60		V _{GS} = 4.5V, I _D = 3A
Forward Transfer Admittance	Y _{FS}	—	12.6	—	S	V _{DS} = 5V, I _D = 3A
Diode Forward Voltage (Note 12)	V _{SD}	—	0.7	1.0	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 13)						
Input Capacitance	C _{ISS}	—	1,790.8	—	pF	V _{DS} = 20V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{OSS}	—	160.6	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	120.5	—	pF	
Gate Resistance	R _G	—	1.03	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _G	—	37.56	—	nC	V _{GS} = 10V, V _{DS} = 20V, I _D = 3A
Gate-Source Charge	Q _{GS}	—	7.8	—	nC	
Gate-Drain Charge	Q _{GD}	—	6.6	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	8.08	—	ns	V _{GS} = 10V, V _{DS} = 20V, I _D = 3A
Turn-On Rise Time	t _R	—	15.14	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	24.29	—	ns	
Turn-Off Fall Time	t _F	—	5.27	—	ns	

Electrical Characteristics (Q2 P-Channel) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 12)						
Drain-Source Breakdown Voltage	BV _{DSS}	-40	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1.0	μA	V _{DS} = -40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 12)						
Gate Threshold Voltage	V _{GS(TH)}	-0.8	-1.3	-1.8	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	28	45	mΩ	V _{GS} = -10V, I _D = -3A
			30	60		V _{GS} = -4.5V, I _D = -3A
Forward Transfer Admittance	Y _{FS}	—	16.6	—	S	V _{DS} = -5V, I _D = -3A
Diode Forward Voltage (Note 12)	V _{SD}	—	-0.7	-1.0	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 13)						
Input Capacitance	C _{ISS}	—	1,643.17	—	pF	V _{DS} = -20V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{OSS}	—	179.13	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	127.82	—	pF	
Gate Resistance	R _G	—	6.43	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _G	—	33.66	—	nC	V _{GS} = -10V, V _{DS} = -20V, I _D = -3A
Gate-Source Charge	Q _{GS}	—	5.54	—	nC	
Gate-Drain Charge	Q _{GD}	—	7.30	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	6.85	—	ns	V _{GS} = -10V, V _{DS} = -20V, I _D = -3A
Turn-On Rise Time	t _R	—	14.72	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	53.65	—	ns	
Turn-Off Fall Time	t _F	—	30.86	—	ns	

Notes: 12. Short duration pulse test used to minimize self-heating effect.
13. Guaranteed by design. Not subject to production testing.

Typical Characteristics (Q1 N-Channel)

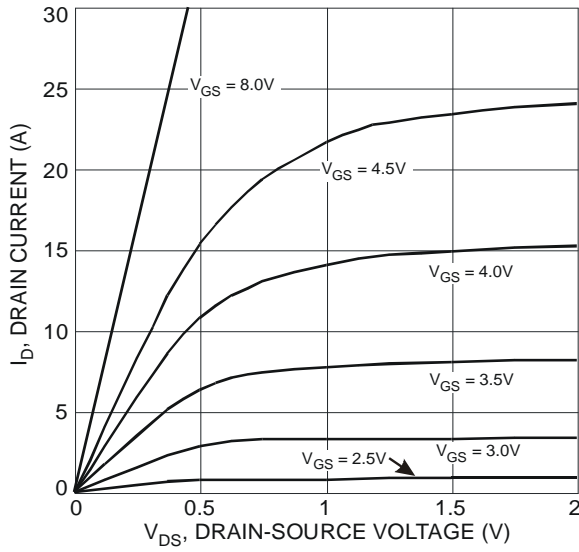


Fig. 1 Typical Output Characteristic

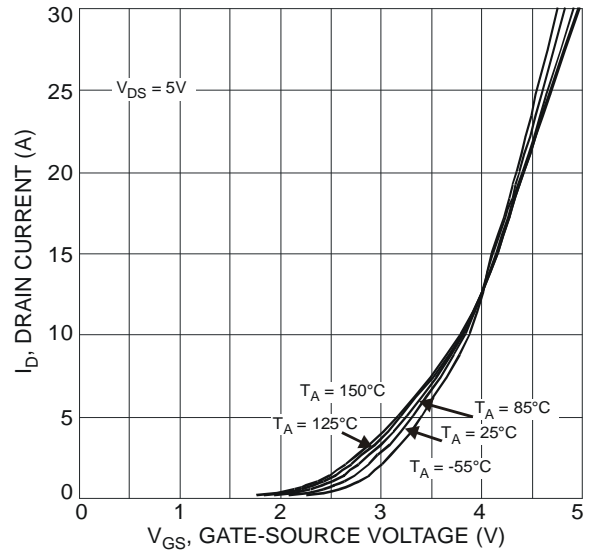


Fig. 2 Typical Transfer Characteristic

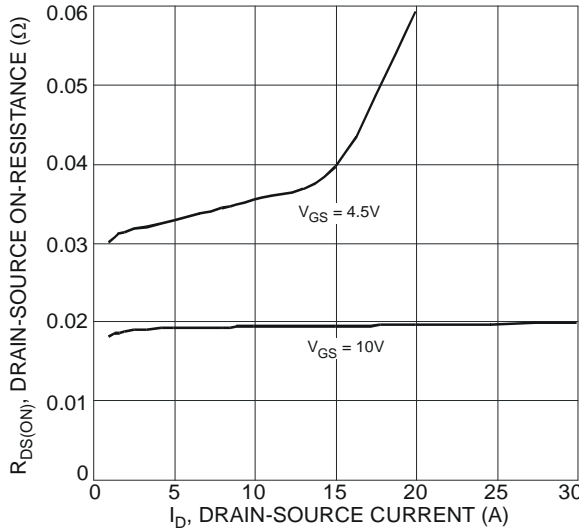


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

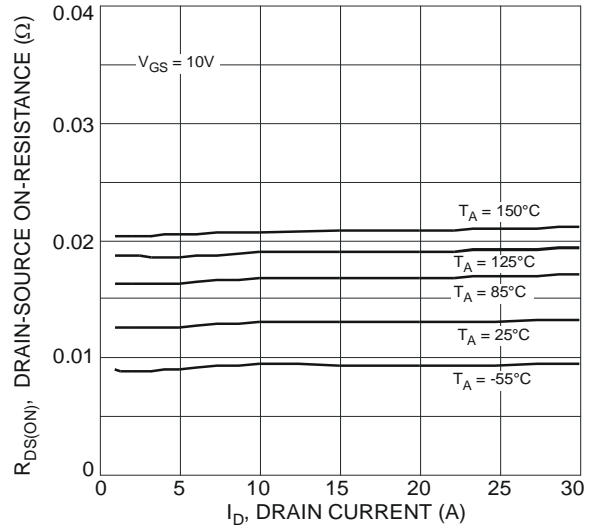


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

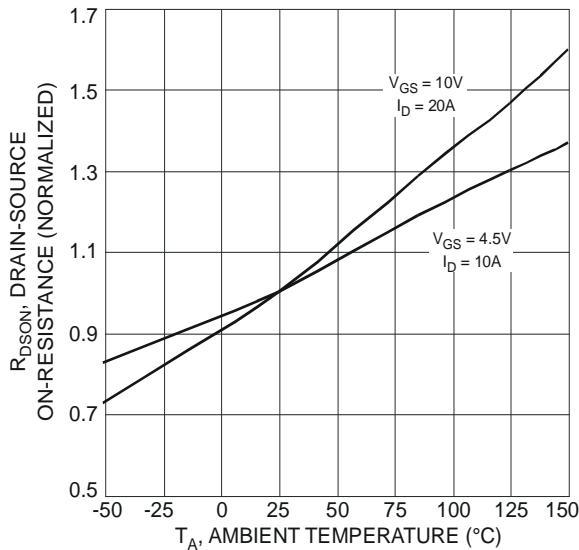


Fig. 5 On-Resistance Variation with Temperature

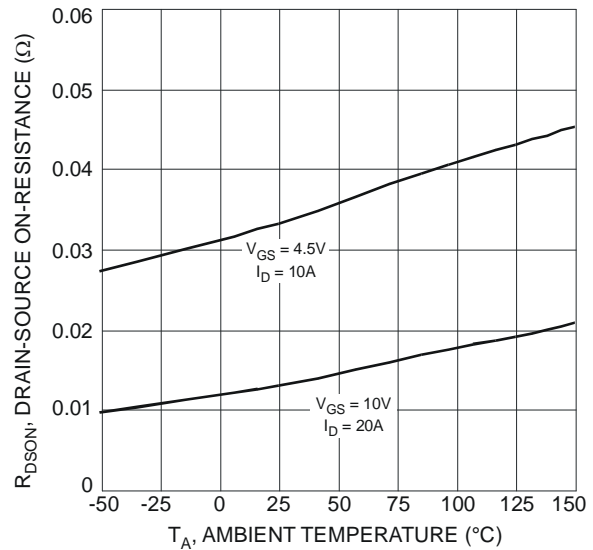


Fig. 6 On-Resistance Variation with Temperature

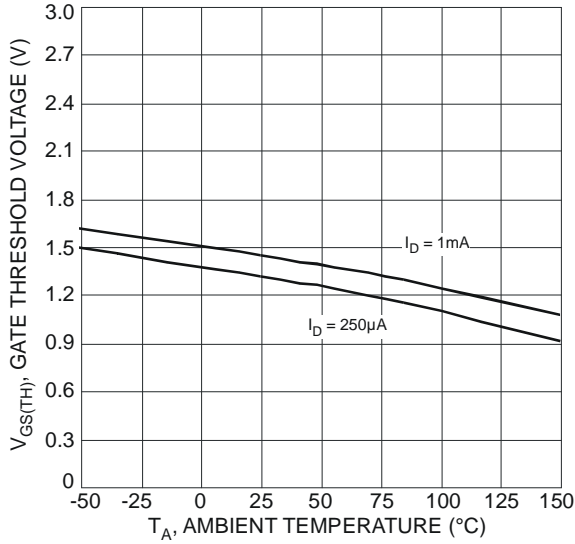


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

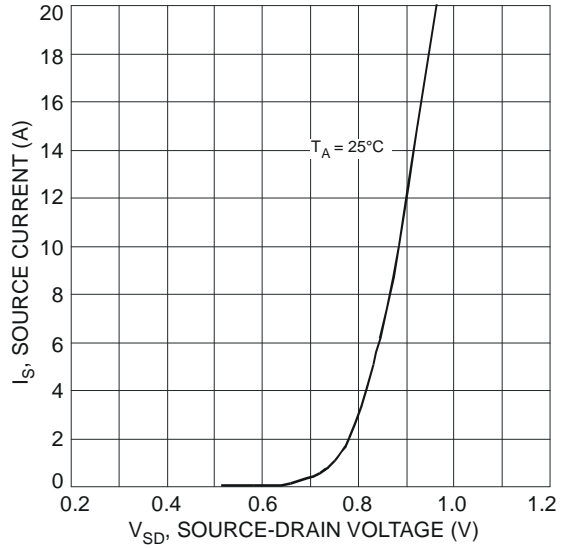


Fig. 8 Diode Forward Voltage vs. Current

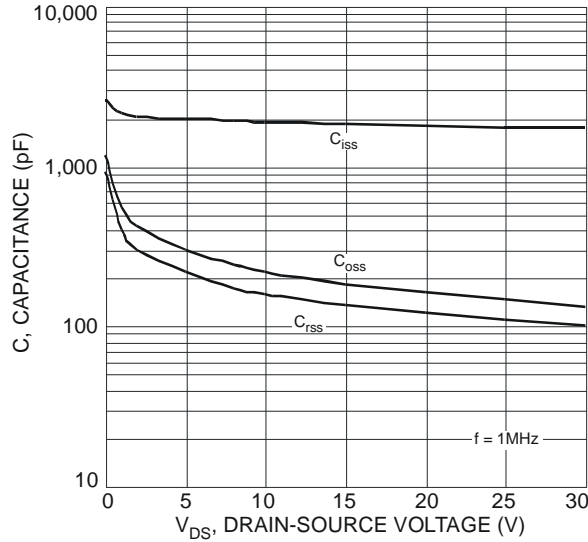


Fig. 9 Typical Total Capacitance

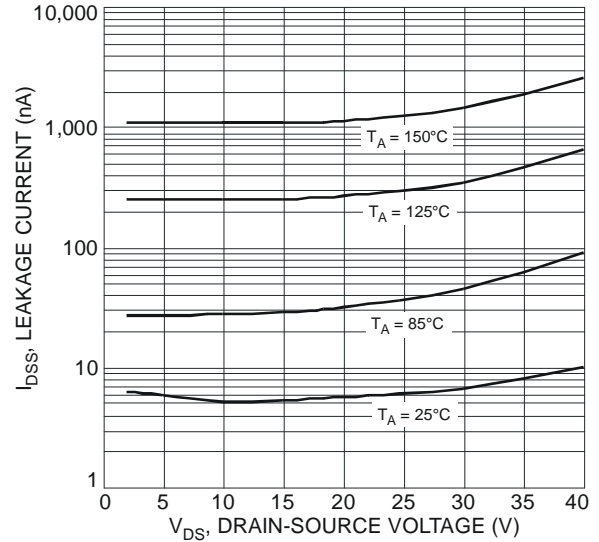


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

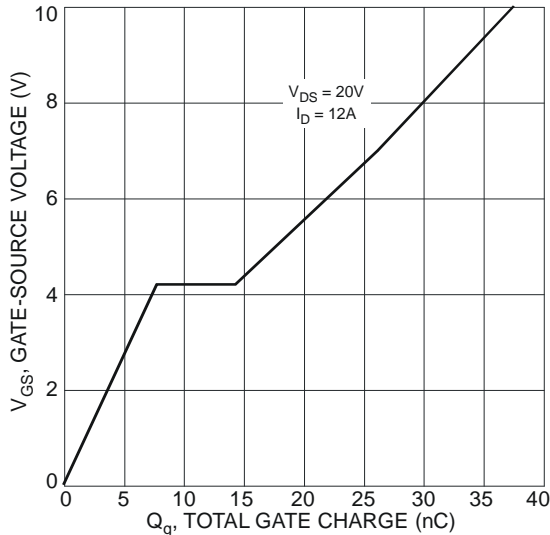


Fig. 11 Gate-Charge Characteristics

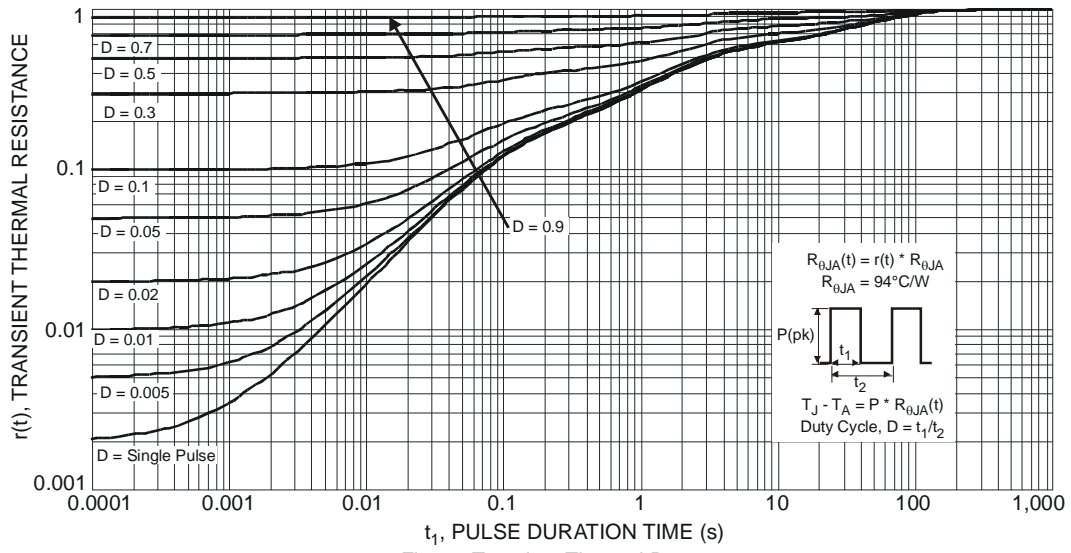


Fig. 12 Transient Thermal Response

Typical Characteristics (Q2 P-Channel)

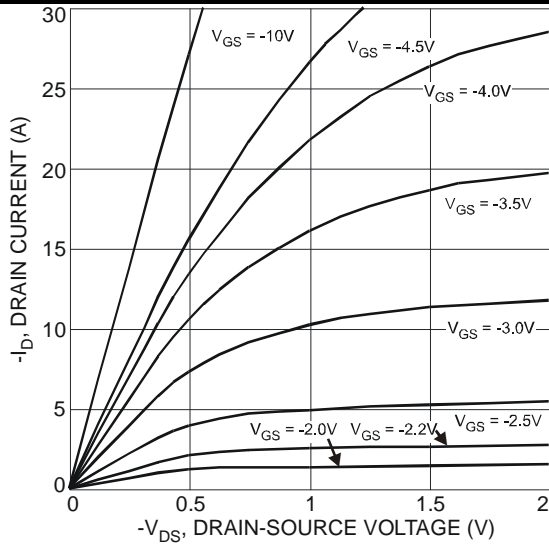


Fig. 13 Typical Output Characteristic

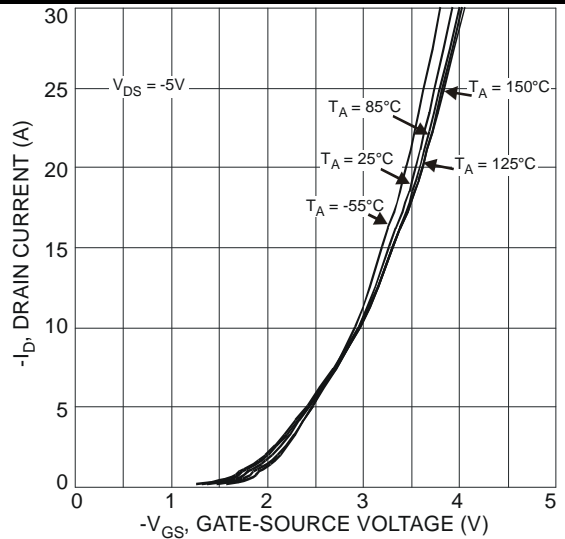


Fig. 14 Typical Transfer Characteristic

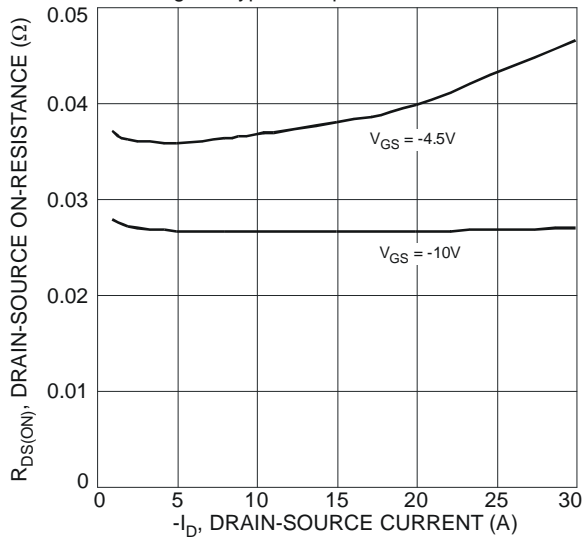


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

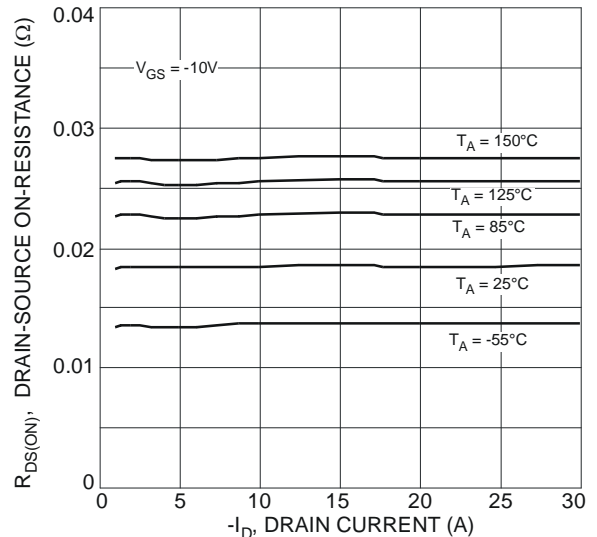


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

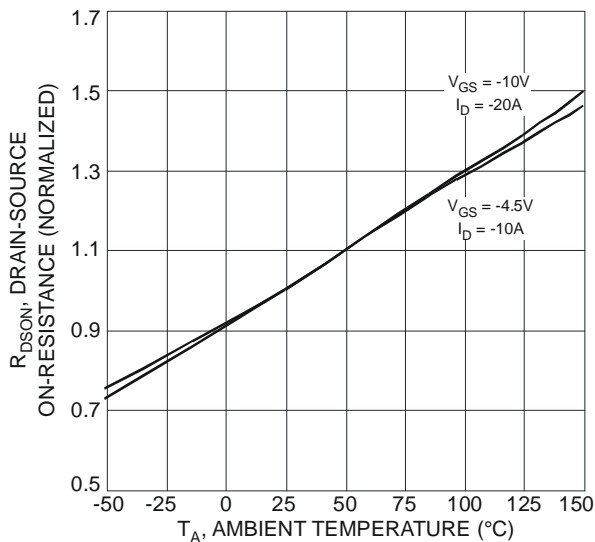


Fig. 17 On-Resistance Variation with Temperature

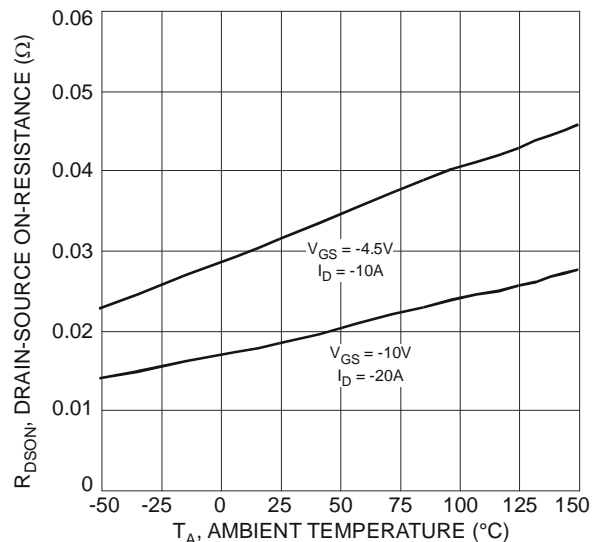


Fig. 18 On-Resistance Variation with Temperature

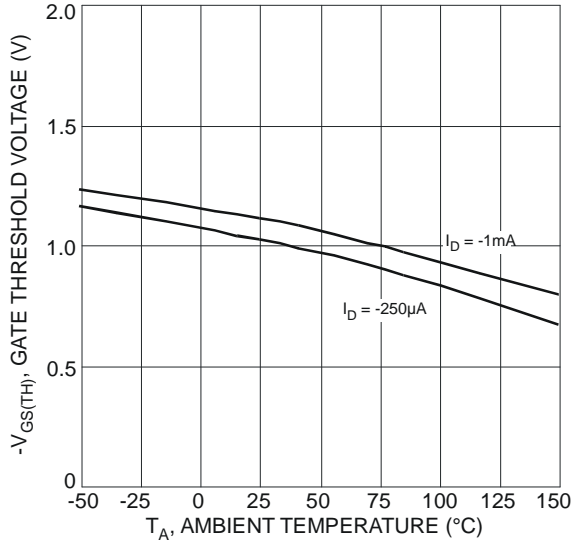


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

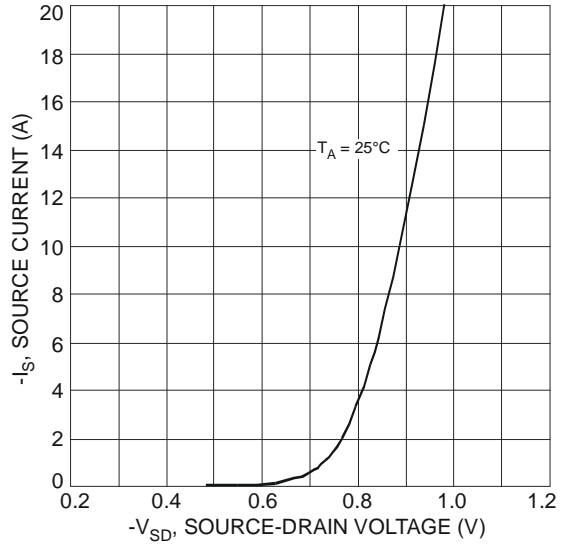


Fig. 20 Diode Forward Voltage vs. Current

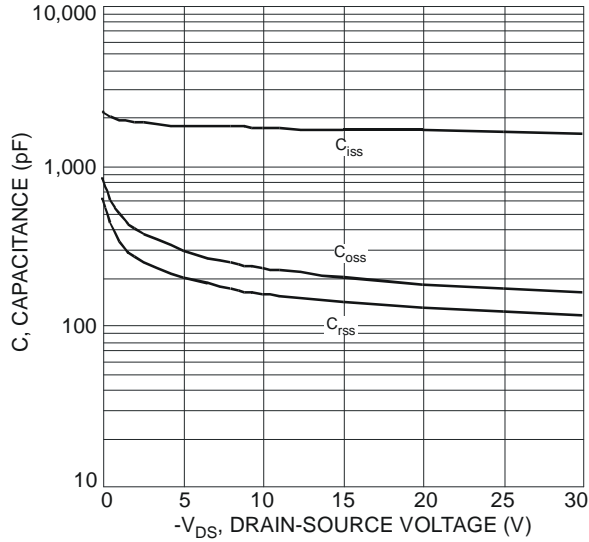


Fig. 21 Typical Total Capacitance

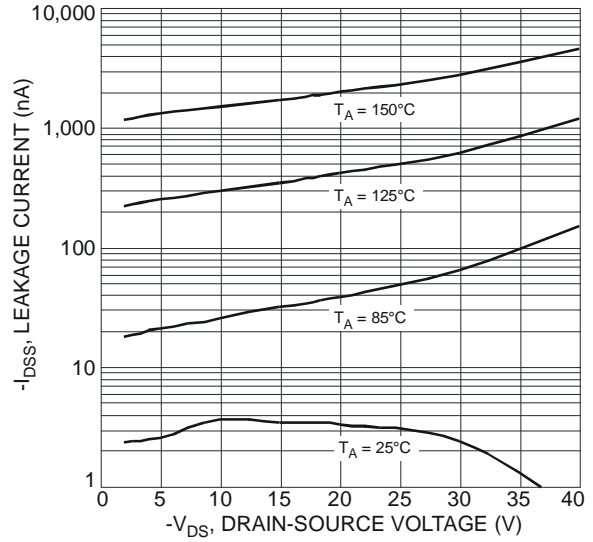


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

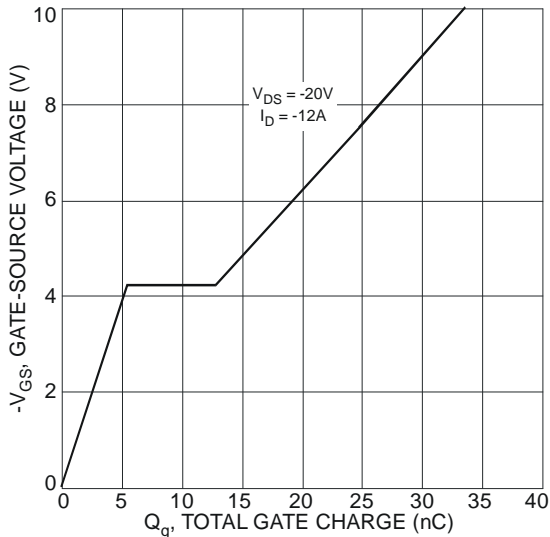


Fig. 23 Gate-Charge Characteristics

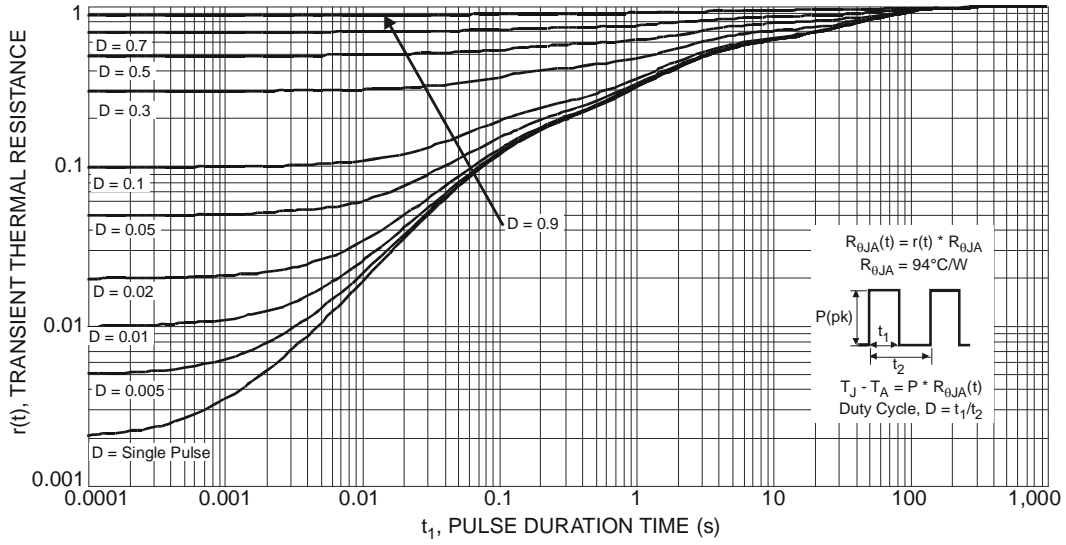
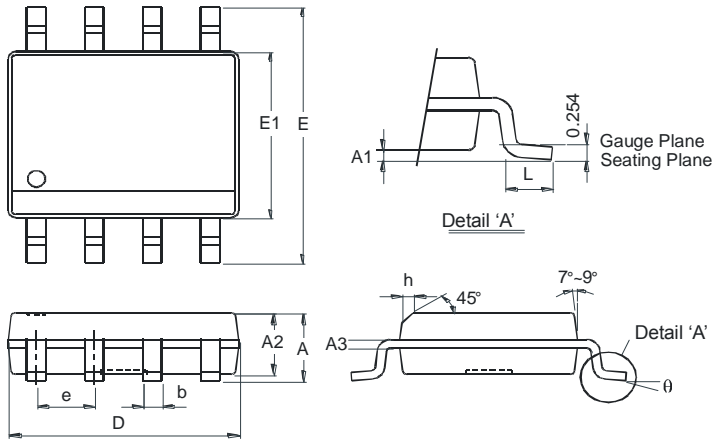


Fig. 24 Transient Thermal Response

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8

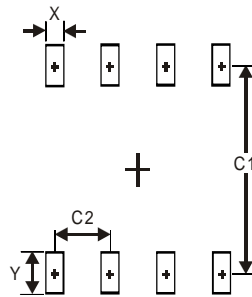


SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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