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9-1	9-1	Corrected text in 1st paragraph : PCON/PCON1 have differert addr.
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Ch.12	Ch.11	Improved index with bold page numbers for main reference pages
several	several	Writing errors corrected

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1 Introduction

The C504 is a modified and extended version of the C501 Microcontroller. Its enhanced functionality, especially the capture compare unit (CCU), allows to use the MCU in motor control applications. Further, the C504 is compatible with the SAB 80C52/C501 microcontrollers and can replace it in existing applications.

The C504-2R contains a non-volatile 16K×8 read-only program memory, a volatile on-chip 512×8 read/write data memory, four 8-bit wide ports, three 16-bit timers/counters, a 16-bit capture/ compare unit, a 10-bit compare timer, a twelve source, two priority level interrupt structure, a serial port, versatile fail save mechanisms, on-chip emulation support logic, and a genuine 10-bit A/D converter. The C504-L is identical to the C504-2R, except that it lacks the on-chip program memory The C504-2E is the OTP version in the C504 microcontroller with a 16Kx8 one-time programmable (OTP) program memory.The term C504 refers to all versions within this documentation unless otherwise noted.

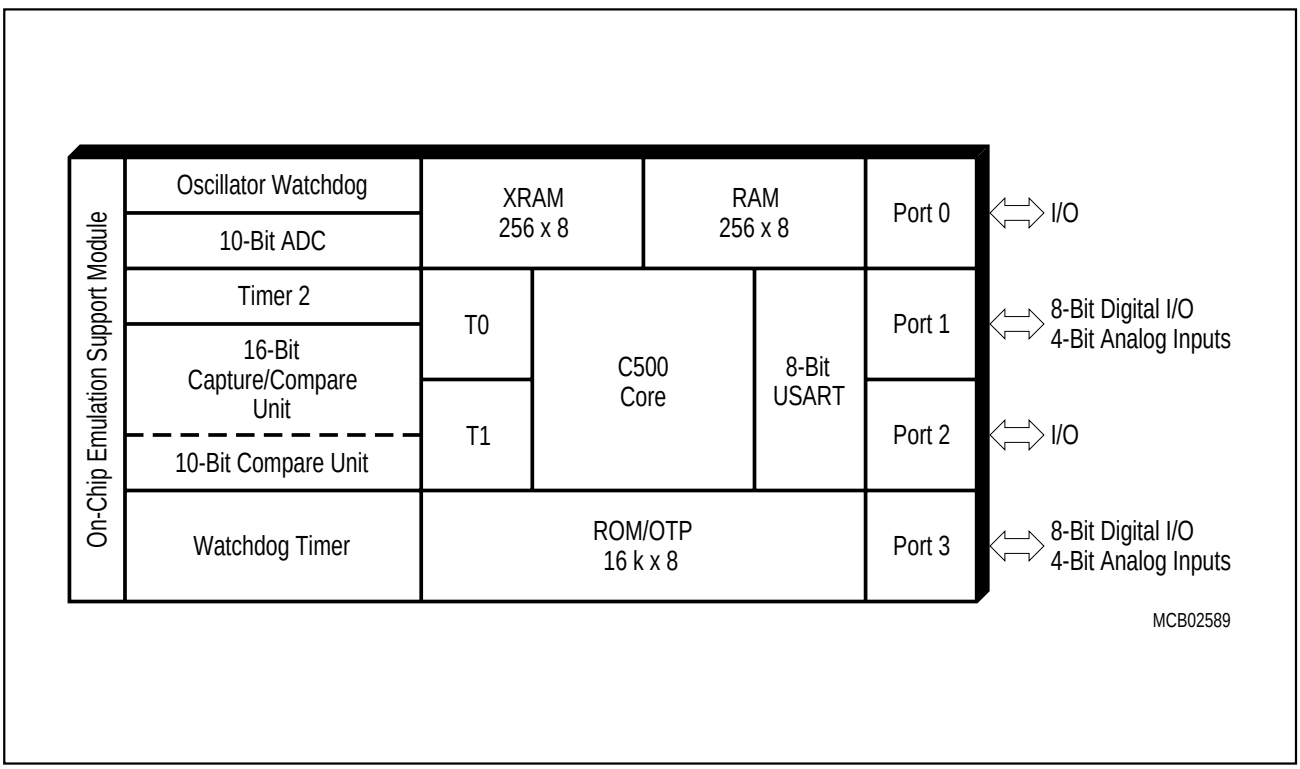


Figure 1-1
C504 Functional Units

Listed below is a summary of the main features of the C504:

- Fully compatible to standard 8051 microcontroller
- Up to 40 MHz external operating frequency
- 16K byte on-chip program memory
  - C504-2R: ROM version (with optional ROM protection)
  - C504-2E: programmable OTP version
  - C504-L : without on-chip program memory)
  - alternatively up to 64K byte external program memory
- 256×8 RAM
- 256×8 XRAM
- Four 8-bit ports, (2 ports with mixed analog/digital I/O capability)
- Three 16-bit timers/counters (timer 2 with up/down counter feature)
- Capture/compare unit for PWM signal generation and signal capturing
  - 3-channel, 16-bit capture/compare unit
  - 1-channel, 10-bit compare unit
- USART
- 10-bit A/D Converter with 8 multiplexed inputs
- Twelve interrupt sources with two priority levels
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- M-QFP-44 package
- Temperature ranges: SAB-C504 T_A : 0 to 70°C
  SAF-C504 T_A : – 40 to 85°C
  SAH-C504 T_A : – 40 to 110°C (max. operating frequency.: TBD)
  SAK-C504 T_A : – 40 to 125°C (max. operating frequency.: 12 MHz)

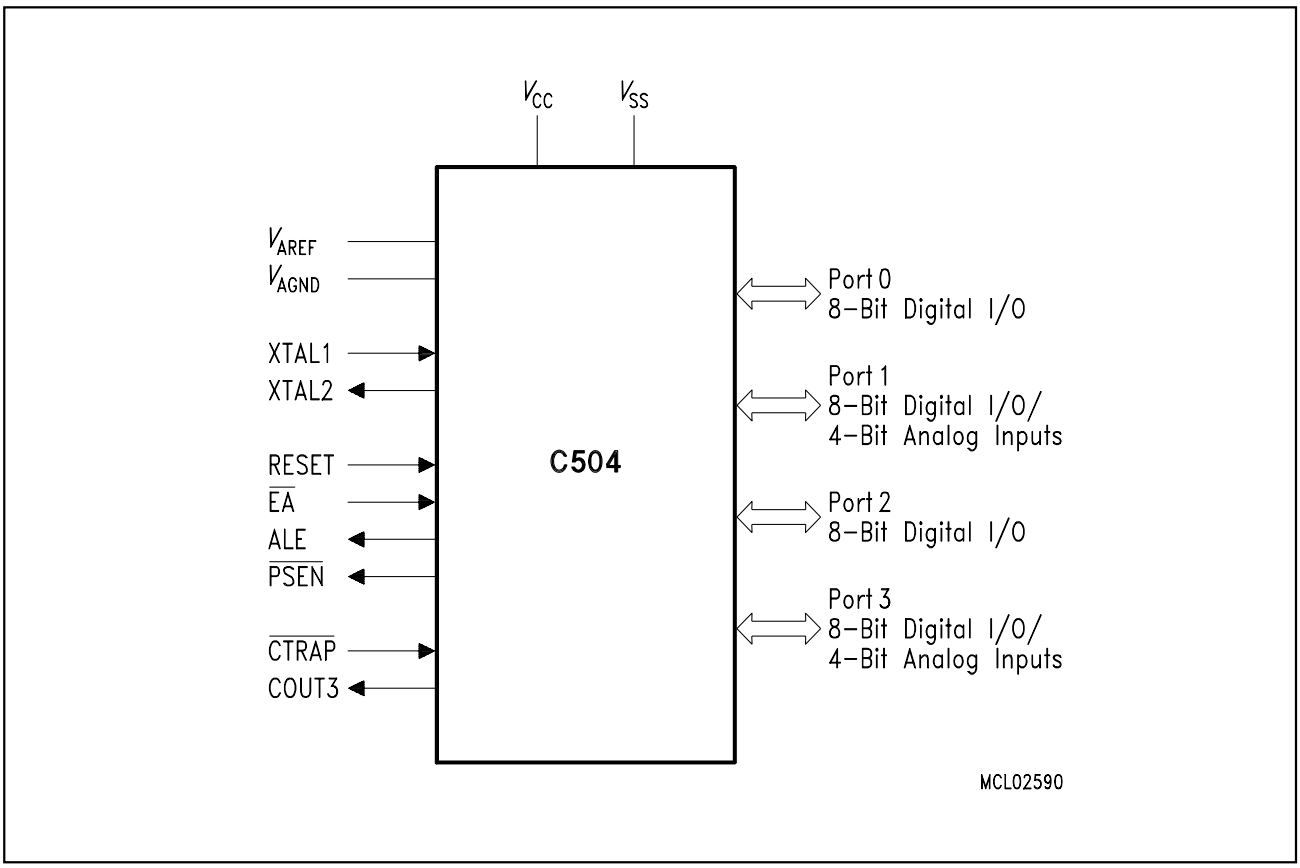


Figure 1-2
Logic Symbol

1.1 Pin Configuration

This section describes the pin configration of the C504 in the P-MQFP-44 package.

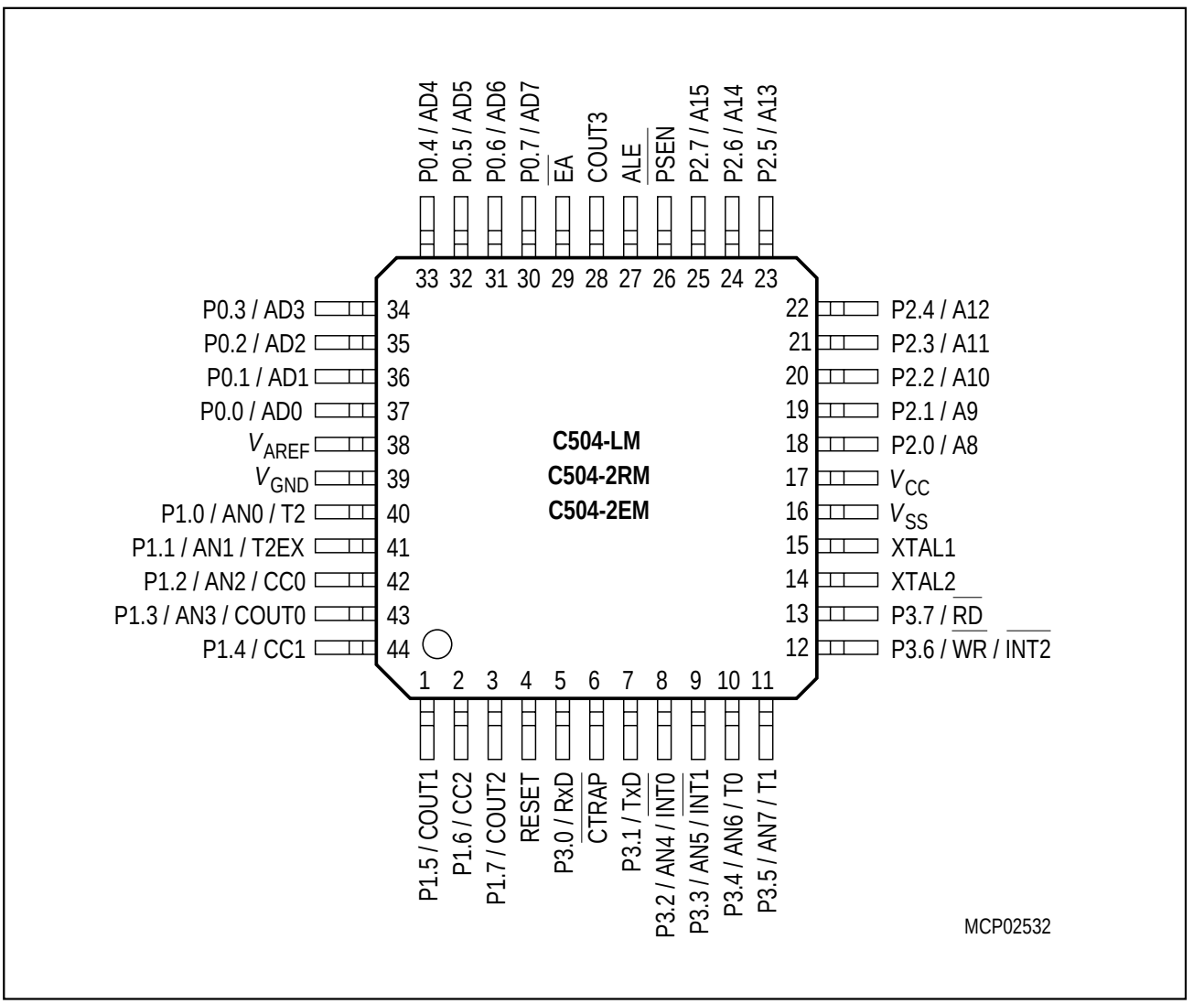


Figure 1-3
Pin Configuration (top view)

1.2 Pin Definitions and Functions

This section describes all external signals of the C504 with its function.

Table 1-1
Pin Definitions and Functions

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
P1.0-P1.7	40-44, 1-3	I/O	**Port 1** is an 8-bit bidirectional port. Port pins can be used for digital input/output. P1.0 - P1.3 can also be used as analog inputs of the A/D-converter. As secondary digital functions, port 1 contains the timer 2 pins and the capture/compare inputs/outputs. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. The functions are assigned to the pins of port 1 as follows: 40 P1.0 / AN0 / T2 Analog input channel 0 / input to counter 2 41 P1.1 / AN1 / T2EX Analog input channel 1 / capture/reload trigger of timer 2 / up-down count 42 P1.2 / AN2 / CC0 Analog input channel 2 / input/output of capture/compare channel 0 43 P1.3 / AN3 / COUT0 Analog input channel 3 / output of capture/compare channel 0 44 P1.4 / CC1 Input/output of capture/compare channel 1 1 P1.5 / COUT1 Output of capture/compare channel 1 2 P1.6 / CC2 Input/output of capture/compare channel 2 3 P1.7 / COUT2 Output of capture/compare channel 2
RESET	4	I	**RESET** A high level on this pin for the duration of two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

*) I = Input
O = Output

Table 1-1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit bidirectional port. P3.0 (R×D) and P3.1 (T×D) operate as defined for the C501. P3.2 to P3.7 contain the external interrupt inputs, timer inputs, input and as an additional optinal function four of the analog inputs of the A/D-converter. Port 3 pins are assigned to be used as analog inputs by the bits of SFR P3ANA. P3.6/$\overline{WR}$ can be assigned as a third interrupt input. The functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / AN4 / $\overline{INT0}$ — Analog input channel 4 / external interrupt 0 input / timer 0 gate control input
	9		P3.3 / AN5 / $\overline{INT1}$ — Analog input channel 5 / external interrupt 1 input / timer 1 gate control input
	10		P3.4 / AN6 / T0 — Analog input channel 6 / timer 0 counter input
	11		P3.5 / AN7 / T1 — Analog input channel 7 / timer 1 counter input
	12		P3.6 / $\overline{WR}$ / $\overline{INT2}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory / external interrupt 2 input
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory
$\overline{CTRAP}$	6	I	**CCU Trap Input** With $\overline{CTRAP}$ = low the compare outputs of the CAPCOM unit are switched to the logic level as defined in the COINI register (if they are enabled by the bits in SFR TRCON). $\overline{CTRAP}$ is an input pin with an internal pullup resistor. For power saving reasons, the signal source which drives the $\overline{CTRAP}$ input should be at high or floating level during power-down mode.

*) I = Input
O = Output

Table 1-1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
XTAL2	14	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	18-25	I/O	**Port 2** is a bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	26	O	The **$\overline{\text{Program Store Enable}}$** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access. When instructions are executed from internal ROM ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON.

*) I = Input
O = Output

Table 1-1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
COUT3	28	O	**10-Bit compare channel output** This pin is used for the output signal of the 10-bit compare timer 2 unit. COUT3 can be disabled and set to a high or low state.
$\overline{EA}$	29	I	**$\overline{External\ Access}$ Enable** When held at high level, instructions are fetched from the internal ROM (C504-2R only) when the PC is less than 4000_H.When held at low level, the C504 fetches all instructions from external program memory. For the C504-L this pin must be tied low.
P0.0-P0.7	30-37	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup resistors when issuing 1 s. Port 0 also outputs the code bytes during program verification in the C504-2R. External pullup resistors are required during program (ROM) verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{CC}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

2 Fundamental Structure

The C504 basically is fully compatible to the architecture of the standard 8051 microcontroller family. Especially it is functionally upward compatible with the SAB 80C52/C501 microcontrollers. While maintaining all architectural and operational characteristics of the SAB 80C52/C501, the C504 incorporates a genuine 10-bit A/D Converter, a capture/compare unit, a XRAM data memory as well as some enhancements in the Timer 2 and Fail Save Mechanism Unit. **Figure 2-1** shows a block diagram of the C504.

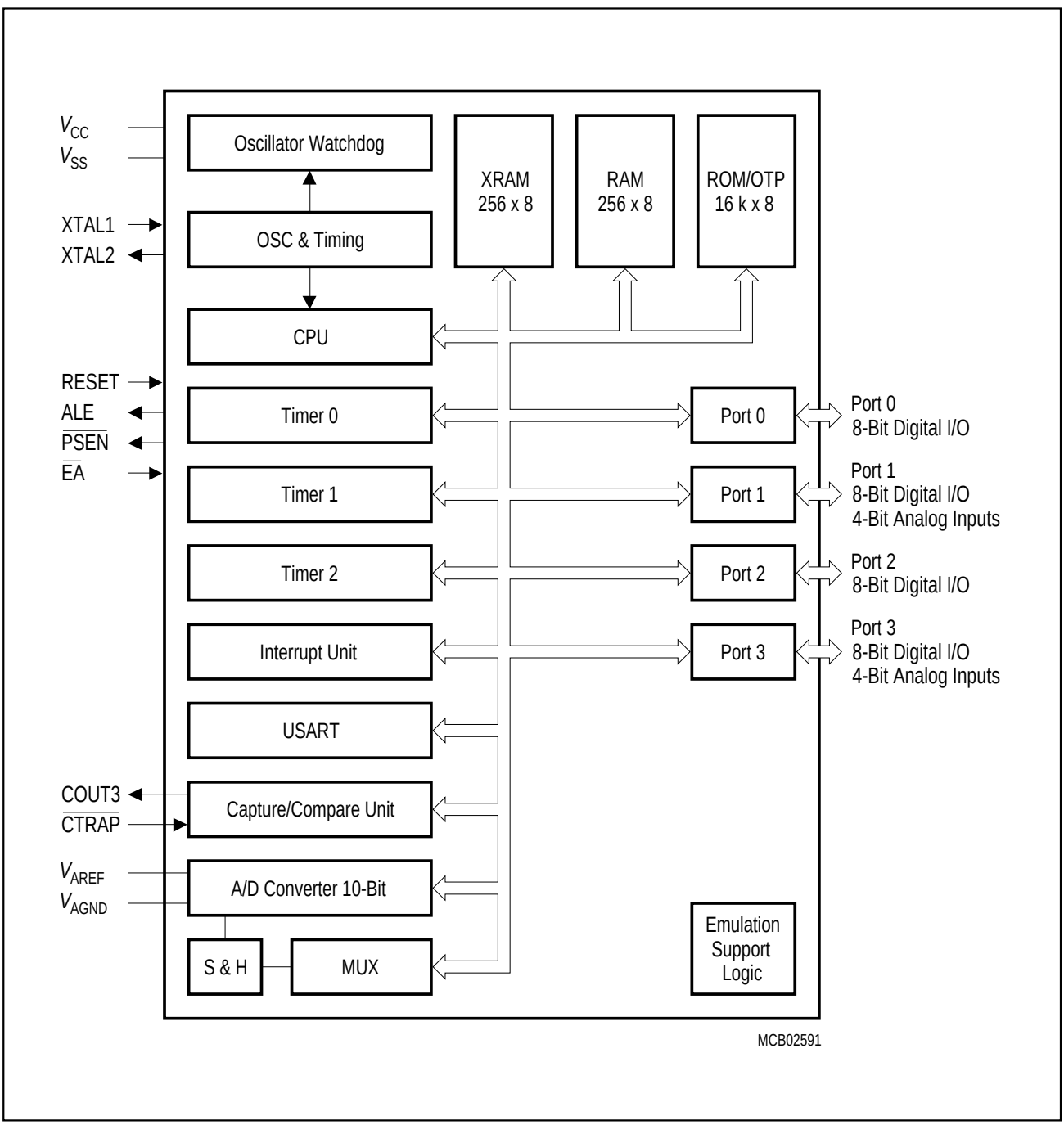


Figure 2-1
Block Diagram of the C504

2.1 CPU

The C504 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12-MHz crystal, 58% of the instructions execute in 1.0 µs (40 MHz: 300 ns).
The CPU (Central Processing Unit) of the C504 consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.
The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), an A register, B register and PSW register.
The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, substract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, completement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (or its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

Accumulator

ACC is the symbol for the accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A.

Program Status Word

The Program Status Word (PSW) contains several status bits that reflect the current state of the CPU.

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

B Register

The B register is used during multiply and divide and serves as both source and destination. For other instructions it can be treated as another scratch pad register.

Stack Pointer

The stack pointer (SP) register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions and decremented after data is popped during a POP and RET (RETI) execution, i.e. it always points to the last valid stack byte. While the stack may reside anywhere in the on-chip RAM, the stack pointer is initialized to 07_H after a reset. This causes the stack to begin a location = 08_H above register bank zero. The SP can be read or written under software control.

2.2 CPU Timing

A machine cycle consists of 6 states (12 oscillator periods). Each state is divided into a phase 1 half, during which the phase 1 clock is active, and a phase 2 half, during which the phase 2 clock is active. Thus, a machine cycle consists of 12 oscillator periods, numbered S1P1 (state 1, phase 1) through S6P2 (state 6, phase 2). Each state lasts for two oscillator periods. Typically, arithmetic and logically operations take place during phase 1 and internal register-to-register transfers take place during phase 2.

The diagrams in **figure 2-2** show the fetch/execute timing related to the internal states and phases. Since these internal clock signals are not user-accessible, the XTAL2 oscillator signals and the ALE (address latch enable) signal are shown for external reference. ALE is normally activated twice during each machine cycle: once during S1P2 and S2P1, and again during S4P2 and S5P1.

Executing of a one-cycle instruction begins at S1P2, when the op-code is latched into the instruction register. If it is a two-byte instruction, the second reading takes place during S4 of the same machine cycle. If it is a one-byte instruction, there is still a fetch at S4, but the byte read (which would be the next op-code) is ignored (discarded fetch), and the program counter is not incremented. In any case, execution is completed at the end of S6P2.

Figures 2-2 (a) and **(b)** show the timing of a 1-byte, 1-cycle instruction and for a 2-byte, 1-cycle instruction.

Most C504 instructions are executed in one cycle. MUL (multiply) and DIV (divide) are the only instructions that take more than two cycles to complete; they take four cycles. Normally two code bytes are fetched from the program memory during every machine cycle. The only exception to this is when a MOVX instruction is executed. MOVX is a one-byte, 2-cycle instruction that accesses external data memory. During a MOVX, the two fetches in the second cycle are skipped while the external data memory is being addressed and strobed. **Figure 2-2 (c)** and **(d)** show the timing for a normal 1-byte, 2-cycle instruction and for a MOVX instruction.

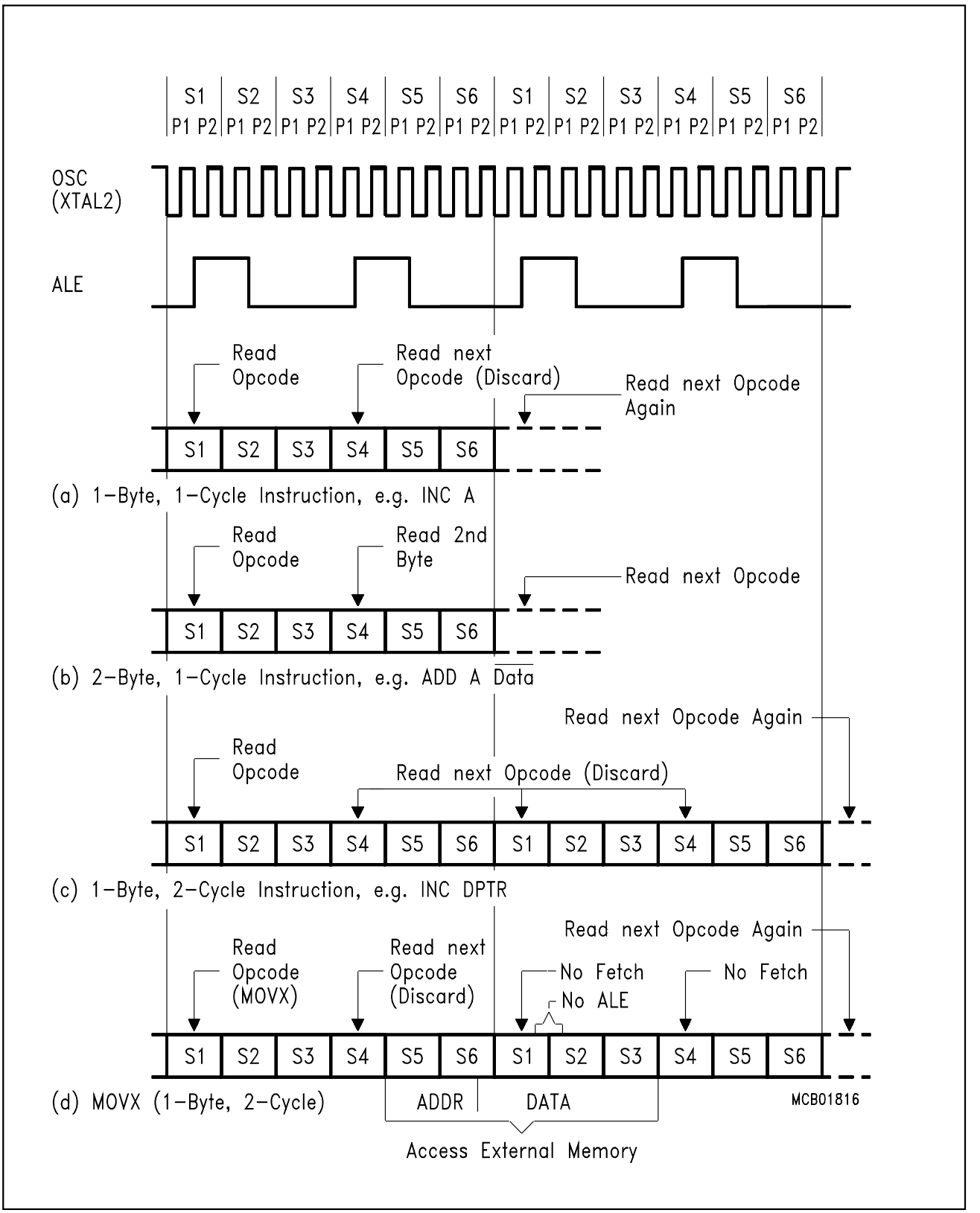


Figure 2-2
Fetch Execute Sequence

3 Memory Organization

The C504 CPU manipulates operands in the following four address spaces:

- up to 64 Kbyte of internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- a 128 byte special function register area

Figure 3-1 illustrates the memory address spaces of the C504.

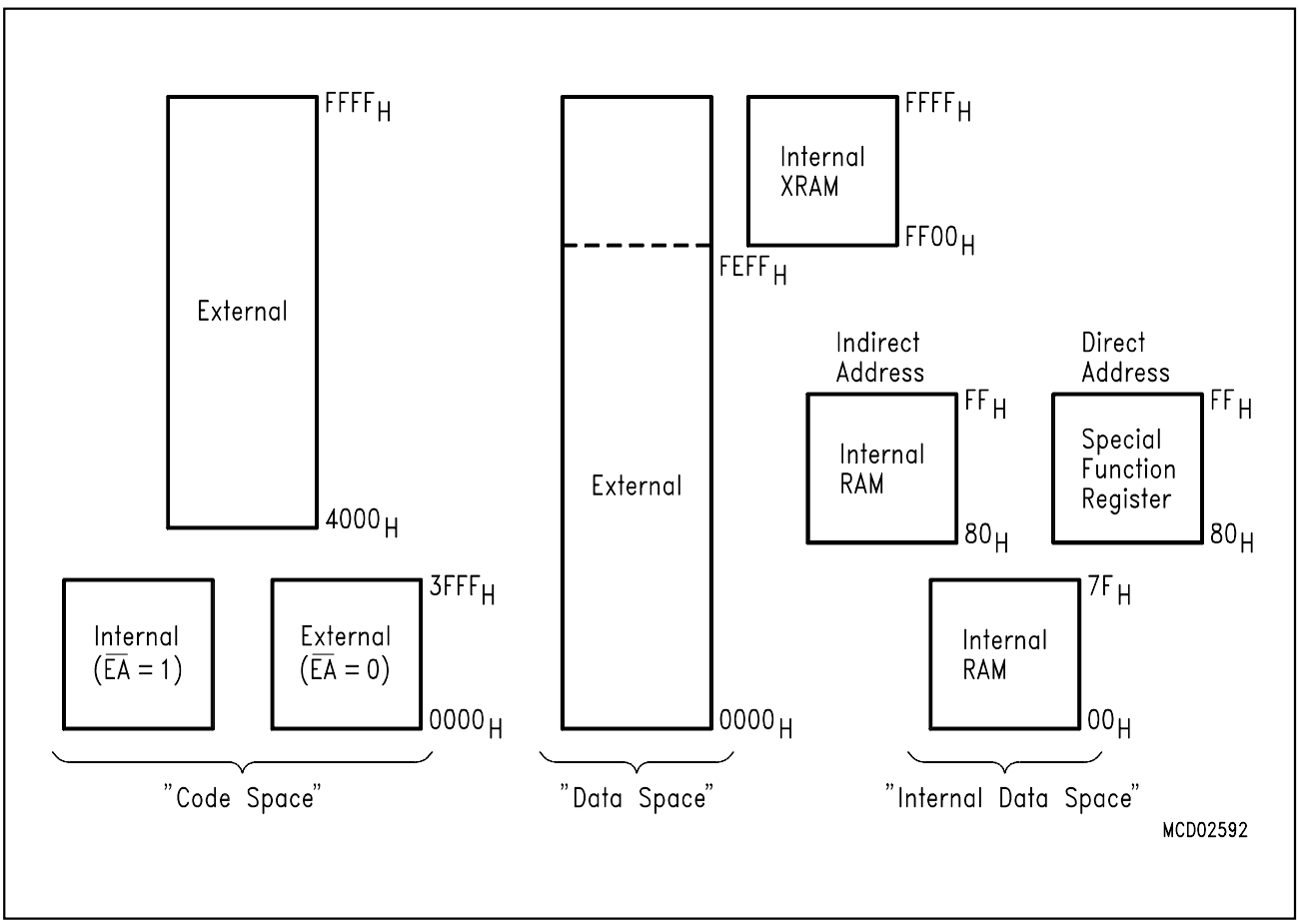


Figure 3-1
C504 Memory Map

3.1 Program Memory, "Code Space"

The C504-2R has 16 Kbytes of read-only program memory, while the C504-L has no internal program memory. The C504-2E provides 16 Kbytes of OTP program memory. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the C504 executes out of internal ROM unless the program counter address exceeds $3FFF_H$. Locations 4000_H through $FFFF_H$ are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the C504 fetches all instructions from the external program memory.

3.2 Data Memory, "Data Space"

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks : the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing. Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through $1F_H$ in the lower RAM area. The next 16 bytes, locations 20_H through $2F_H$, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.

The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

3.3 General Purpose Registers

The lower 32 locations of the internal RAM are assigned to four banks with eight general purpose registers (GPRs) each. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in chapter 2). This allows fast context switching, which is useful when entering subroutines or interrupt service routines.

The 8 general purpose registers of the selected register bank may be accessed by register addressing. With register addressing the instruction op code indicates which register is to be used. For indirect addressing R0 and R1 are used as pointer or index register to address internal or external memory (e.g. MOV @R0).

Reset initializes the stack pointer to location 07_H and increments it once to start from location 08_H which is also the first register (R0) of register bank 1. Thus, if one is going to use more than one register bank, the SP should be initialized to a different location of the RAM which is not used for data storage.

3.4 XRAM Operation

The XRAM in the C504 is a memory area that is logically located at the upper end of the external memory space, but is integrated on the chip. Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

The C504 maps 256 bytes of the external data space into the on-chip XRAM. Especially when using the 8-bit addressing modes this could prevent access to the external memory extension and might induce problems when porting software. Therefore, it is possible to enable and disable the on-chip XRAM using the bit XMAP in SFR SYSCON. When the XRAM is disabled (default after reset), all external data memory accesses will go to the external data memory area.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX10XXX0_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	–	–	–	XMAP	SYSCON

The functions of the shaded bits are not described in this section.

Bit	Function
–	Not implemented. Reserved for future use.
XMAP	Enable XRAM XMAP=0 : XRAM disabled. XMAP=1 : XRAM enabled. If XRAM is enabled, 8-bit MOVX instructions using Ri always access the internal XRAM and do not generate external bus cycles. If XRAM is enabled, 16-bit MOVX instructions using DPTR, access the XRAM if the address is in the range of $FF00_H$ to $FFFF_H$ and do not generate external bus cycles in this address range.

3.4.1 Reset Operation of the XRAM

The content of the XRAM is not affected by a reset. After power-up the content is undefined, while it remains unchanged during and after a reset as long as the power supply is not turned off. If a reset occurs during a write operation to XRAM, the content of a XRAM memory location depends on the cycle in which the active reset signal is detected (MOVX is a 2-cycle instruction):

Reset during 1st cycle : The new value will not be written to XRAM. The old value is not affected.
Reset during 2nd cycle : The old value in XRAM is overwritten by the new value.

After reset the access to the XRAM is disabled (bit XMAP of SYSCON = 0).

3.4.2 Accesses to XRAM using the DPTR (16-bit Addressing Mode)

The XRAM can be accessed by two read/write instructions, which use the 16-bit DPTR for indirect addressing. These instructions are:

- MOVX A, @DPTR (Read)
- MOVX @DPTR, A (Write)

Using these instructions with the XRAM disabled implies, that port 0 is used as address low/data bus, port 2 for high address output, and two lines of port 3 (P3.6/$\overline{WR}$/$\overline{INT2}$, P3.7/$\overline{RD}$) for control to access up to 64 KB of external memory. If the XRAM is enabled and if the effective address stored in DPTR is in the range of 0000_H to $FEFF_H$, these instruction will access external memory.

If XRAM is enabled and if the address is within $FF00_H$ to $FFFF_H$, the physically internal XRAM of the C504 will be accessed. External memory, which is located in this address range, cannot be accessed in this case because no external bus cycles will generated. Therefore port 0, 2 and 3 can be used as general purpose I/O if only the XRAM memory space is addressed by the user program.

3.4.3 Accesses to XRAM using the Registers R0/R1 (8-bit Addressing Mode)

The C504 architecture provides also instructions for accesses to external data memory and XRAM which use an 8-bit address (indirect addressing with registers R0 or R1). These instructions are:

- MOVX A, @Ri (Read)
- MOVX @Ri, A (Write)

Using these instructions with the XRAM disabled implies, that port 0 is used as address/data bus, port 2 for high address output, and two lines of port 3 (P3.6/$\overline{WR}$/$\overline{INT2}$, P3.7/$\overline{RD}$) for control. Normally these instructions are used to access 256 byte pages of external memory.

If the XRAM is enabled these instruction will only access the internal XRAM. External memory cannot be accessed in this case because no external bus cycle will be generated. Therefore port 0, 2 and 3 can be used as standard I/O, if only the internal XRAM is used.

3.5 Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. Three special function registers of the C504 (PCON1, P1ANA, P3ANA) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers of the C504 are located in the standard special function register area.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX10XXX0_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	–	–	–	XMAP	SYSCON

The functions of the shaded bits are not described in this section.

Bit	Function
–	Not implemented. Reserved for future use.
RMAP	Special function register map bit RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.

As long as bit RMAP is set, mapped special function registers can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set by software, respectively each.

There are also 128 directly addressable bits available within each SFR area (standard and mapped SFR area). All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 63 special function register (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C504 are listed in **table 3-1** and **table 3-2**. In **table 3-1** they are organized in groups which refer to the functional blocks of the C504. **Table 3-2** illustrates the contents of the SFRs in numeric order of their addresses.

Table 3-1
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** 1)	00_H
	B	B-Register	**$F0_H$** 1)	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$D0_H$** 1)	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON	System Control Register	$B1_H$	$XX10XXX0_B$ 3)
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** 1)	$0X000000_B$ 3)
	IEN1	Interrupt Enable Register 1	$A9_H$	$XX000000_B$ 3)
	CCIE 2)	Capture/Compare Interrupt Enable Reg.	$D6_H$	00_H
	IP0	Interrupt Priority Register 0	**$B8_H$** 1)	$XX000000_B$ 3)
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$ 3)
	ITCON	Interrupt Trigger Condition Register	$9A_H$	00101010_B
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P1ANA 2)	Port 1 Analog Input Selection Register	**90_H** 1) 4)	$XXXX1111_B$ 3)
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P3ANA 2)	Port 3 Analog Input Selection Register	**$B0_H$** 1) 4)	$XX1111XX_B$ 3)
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** 1	$XX000000_B$ 3)
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$ 3)
	ADDATH	A/D Converter Data Register High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Register Low Byte	DA_H	$00XXXXXX_B$ 3)
	P1ANA 2)	Port 1 Analog Input Selection Register	90_H 4)	$XXXX1111_B$ 3)
	P3ANA 2)	Port 3 Analog Input Selection Register	$B0_H$ 4)	$XX1111XX_B$ 3)
Serial Channels	PCON 2)	Power Control Register	87_H	$000X0000_B$
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3-1
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
	T2MOD	Timer 2 Mode Register	$C9_H$	$XXXXXXX0_B$ [3]
	RC2H	Timer 2 Reload Capture Register, High Byte	CB_H	00_H
	RC2L	Timer 2 Reload Capture Register, Low Byte	CA_H	00_H
	TH2	Timer 2 High Byte	CD_H	00_H
	TL2	Timer 2 Low Byte	CC_H	00_H
Capture / Compare Unit	CT1CON	Compare timer 1 control register	$E1_H$	00010000_B
	CCPL	Compare timer 1 period register, low byte	DE_H	00_H
	CCPH	Compare timer 1 period register, high byte	DF_H	00_H
	CT1OFL	Compare timer 1 offset register, low byte	$E6_H$	00_H
	CT1OFH	Compare timer 1 offset register, high byte	$E7_H$	00_H
	CMSEL0	Capture/compare mode select register 0	$E3_H$	00_H
	CMSEL1	Capture/compare mode select register 1	$E4_H$	00_H
	COINI	Compare output initialization register	$E2_H$	FF_H
	TRCON	Trap enable control register	CF_H	00_H
	CCL0	Capture/compare register 0, low byte	$C2_H$	00_H
	CCH0	Capture/compare register 0, high byte	$C3_H$	00_H
	CCL1	Capture/compare register 1, low byte	$C4_H$	00_H
	CCH1	Capture/compare register 1, high byte	$C5_H$	00_H
	CCL2	Capture/compare register 2, low byte	$C6_H$	00_H
	CCH2	Capture/compare register 2, high byte	$C7_H$	00_H
	CCIR	Capture/compare interrupt request flag reg.	$E5_H$	00_H
	CCIE [2]	Capture/compare interrupt enable register	$D6_H$	00_H
	CT2CON	Compare timer 2 control register	$C1_H$	00010000_B
	CP2L	Compare timer 2 period register, low byte	$D2_H$	00_H
	CP2H	Compare timer 2 period register, high byte	$D3_H$	$XXXXXX00_B$ [3]
	CMP2L	Compare timer 2 compare register, low byte	$D4_H$	00_H
	CMP2H	Compare timer 2 compare register, high byte	$D5_H$	$XXXXXX00_B$ [3)]
	BCON	Block commutation control register	$D7_H$	00_H
Watchdog	WDCON	Watchdog Timer Control Register	**$C0_H$** [1]	$XXXX0000_B$ [3]
	WDTREL	Watchdog Timer Reload Register	86_H	00_H
Power Save Mode	PCON [2]	Power Control Register	87_H	$000X0000_B$ [3]
	PCON1	Power Control Register 1	88_H [4]	$0XXXXXXX_B$ [3]

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3-2
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	$000X\text{-}0000_B$	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [2)3)]	PCON1	$0XXX\text{-}XXXX_B$	EWPD	–	–	–	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	.7	.6	.5	.4	.3	.2	T2EX	T2
90_H [2)3)]	P1ANA	$XXXX\text{-}1111_B$	–	–	–	–	EAN3	EAN2	EAN1	EAN0
98_H [2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9A_H$	ITCON	$0010\text{-}1010_B$	IT2	IE2	I2ETF	I2ETR	I1ETF	I1ETR	I0ETF	I0ETR
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2)]	IEN0	$0X00\text{-}0000_B$	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IEN1	$XX00\text{-}0000_B$	–	–	ECT1	ECCM	ECT2	ECEM	EX2	EADC

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3-2
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$ [2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD	RxD
$B0_H$ [2)3)]	P3ANA	$XX11\text{-}11XX_B$	–	–	EAN7	EAN6	EAN5	EAN4	–	–
$B1_H$	SYSCON	$XX10\text{-}XXX0_B$	–	–	EALE	RMAP	–	–	–	XMAP
$B8_H$ [2)]	IP0	$XX00\text{-}0000_B$	–	–	PT2	PS	PT1	PX1	PT0	PX0
$B9_H$	IP1	$XX00\text{-}0000_B$	–	–	PCT1	PCCM	PCT2	PCEM	PX2	PADC
$C0_H$ [2)]	WDCON	$XXXX\text{-}0000_B$	–	–	–	–	OWDS	WDTS	WDT	SWDT
$C1_H$	CT2CON	$0001\text{-}0000_B$	CT2P	ECT2O	STE2	CT2 RES	CT2R	CLK2	CLK1	CLK0
$C2_H$	CCL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$ [2)]	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
$C9_H$	T2MOD	$XXXX\text{-}XXX0_B$	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CF_H	TRCON	00_H	TRPEN	TRF	TREN5	TREN4	TREN3	TREN2	TREN1	TREN0
$D0_H$ [2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D2_H$	CP2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3-2
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D3_H$	CP2H	XXXX. $XX00_B$	–	–	–	–	–	–	.1	.0
$D4_H$	CMP2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CMP2H	XXXX. $XX00_B$	–	–	–	–	–	–	.1	.0
$D6_H$	CCIE	00_H	ECTP	ECTC	CC2 FEN	CC2 REN	CC1 FEN	CC1 REN	CC0 FEN	CC0 REN
$D7_H$	BCON	00_H	BCMP BCEM	PWM1	PWM0	EBCE	BCERR	BCEN	BCM1	BCM0
$D8_H$ [2)]	ADCON0	XX00- 0000_B	–	–	IADC	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	00XX- $XXXX_B$	.1	.0	–	–	–	–	–	–
DC_H	ADCON1	01XX- $X000_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
DE_H	CCPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
DF_H	CCPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E0_H$ [2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E1_H$	CT1CON	0001- 0000_B	CTM	ETRP	STE1	CT1 RES	CT1R	CLK2	CLK1	CLK0
$E2_H$	COINI	FF_H	COUT 3I	COUT XI	COUT 2I	CC2I	COUT 1I	CC1I	COUT 0I	CC0I
$E3_H$	CMSEL0	00_H	CMSEL 13	CMSEL 12	CMSEL 11	CMSEL 10	CMSEL 03	CMSEL 02	CMSEL 01	CMSEL 00
$E4_H$	CMSEL1	00_H	ESMC	NMCS	0	0	CMSEL 23	CMSEL 22	CMSEL 21	CMSEL 20
$E5_H$	CCIR	00_H	CT1FP	CT1FC	CC2F	CC2R	CC1F	CC1R	CC0F	CC0R
$E6_H$	CT1OFL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E7_H$	CT1OFH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$ [2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers

Table 3-2
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FC_H 3) 4)	VR0	$C5_H$	1	1	0	0	0	1	0	1
FD_H 3) 4)	VR1	04_H 5) 84_H 5)	0 1	0	0	0	0	1	0	0
FE_H 3) 4)	VR2	6)	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
4) These SFRs are read-only registers.
5) 04_H is valid for the C504-2R, 84_H is valid for the C504-2E,
6) The content of this SFR varies with the actual step of the C504 (see also table 10-4 in chapter 10).

4 External Bus Interface

The C504 allows for external memory expansion. To accomplish this, the external bus interface common to most 8051-based controllers is employed.

4.1 Accessing External Memory

It is possible to distinguish between accesses to external program memory and external data memory or other peripheral components respectively. This distinction is made by hardware: accesses to external program memory use the signal $\overline{\text{PSEN}}$ (program store enable) as a read strobe. Accesses to external data memory use RD and WR to strobe the memory (alternate functions of P3.7 and P3.6). Port 0 and port 2 (with exceptions) are used to provide data and address signals. In this section only the port 0 and port 2 functions relevant to external memory accesses are described.

Fetches from external program memory always use a 16-bit address. Accesses to external data memory can use either a 16-bit address (MOVX @DPTR) or an 8-bit address (MOVX @Ri).

Role of P0 and P2 as Data/Address Bus

When used for accessing external memory, port 0 provides the data byte time-multiplexed with the low byte of the address. In this state, port 0 is disconnected from its own port latch, and the address/ data signal drives both FETs in the port 0 output buffers. Thus, in this application, the port 0 pins are not open-drain outputs and do not require external pullup resistors.

During any access to external memory, the CPU writes FF_H to the port 0 latch (the special function register), thus obliterating whatever information the port 0 SFR may have been holding.

Whenever a 16-bit address is used, the high byte of the address comes out on port 2, where it is held for the duration of the read or write cycle. During this time, the port 2 lines are disconnected from the port 2 latch (the special function register).

Thus the port 2 latch does not have to contain 1s, and the contents of the port 2 SFR are not modified.

If an 8-bit address is used (MOVX @Ri), the contents of the port 2 SFR remain at the port 2 pins throughout the external memory cycle. This will facilitate paging. It should be noted that, if a port 2 pin outputs an address bit that is a 1, strong pullups will be used for the entire read/write cycle and not only for two oscillator periods.

Timing

The timing of the external bus interface, in particular the relationship between the control signals ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ and information on port 0 and port 2, is illustrated in **figure 4-1 a)** and **b)**.

Data memory: in a write cycle, the data byte to be written appears on port 0 just before WR is activated and remains there until after WR is deactivated. In a read cycle, the incoming byte is accepted at port 0 before the read strobe is deactivated.

Program memory: Signal $\overline{PSEN}$ functions as a read strobe.

External Program Memory Access

The external program memory is accessed under two conditions:

- whenever signal $\overline{EA}$ is active: or
- whenever the program counter (PC) contains a number that is larger than $3FFF_H$.

This requires the ROM-less version C504-L to have $\overline{EA}$ wired low to allow the lower 16K program bytes to be fetched from external memory.

When the CPU is executing out of external program memory, all 8 bits of port 2 are dedicated to an output function and may not be used for general-purpose I/O. The contents of the port 2 SFR however is not affected. During external program memory fetches port 2 lines output the high byte of the PC, and during accesses to external data memory they output either DPH or the port 2 SFR (depending on whether the external data memory access is a MOVX @DPTR or a MOVX @Ri).

Since the C504-L has no internal program memory, accesses to program memory are always external, and port 2 is at all times dedicated to output the high-order address byte. This means that port 0 and port 2 of the C504-L can never be used as general-purpose I/O. This also applies to the C504-2R or C504-2E when they operat only with an external program memory.

4.2 $\overline{PSEN}$, Program Store Enable

The read strobe for external fetches is $\overline{PSEN}$. $\overline{PSEN}$ is not activated for internal fetches. When the CPU is accessing external program memory, $\overline{PSEN}$ is activated twice every cycle (except during a MOVX instruction) no matter whether or not the byte fetched is actually needed for the current instruction. When $\overline{PSEN}$ is activated its timing is not the same as for RD. A complete RD cycle, including activation and deactivation of ALE and RD, takes 12 oscillator periods. A complete PSEN cycle, including activation and deactivation of ALE and PSEN takes 6 oscillator periods. The execution sequence for these two types of read cycles is shown in **figure 4-1 a)** and **b)**.

4.3 Overlapping External Data and Program Memory Spaces

In some applications it is desirable to execute a program from the same physical memory that is used for storing data. In the C504 the external program and data memory spaces can be combined by AND-ing PSEN and RD. A positive logic AND of these two signals produces an active low read strobe that can be used for the combined physical memory. Since the PSEN cycle is faster than the RD cycle, the external memory needs to be fast enough to adapt to the PSEN cycle.

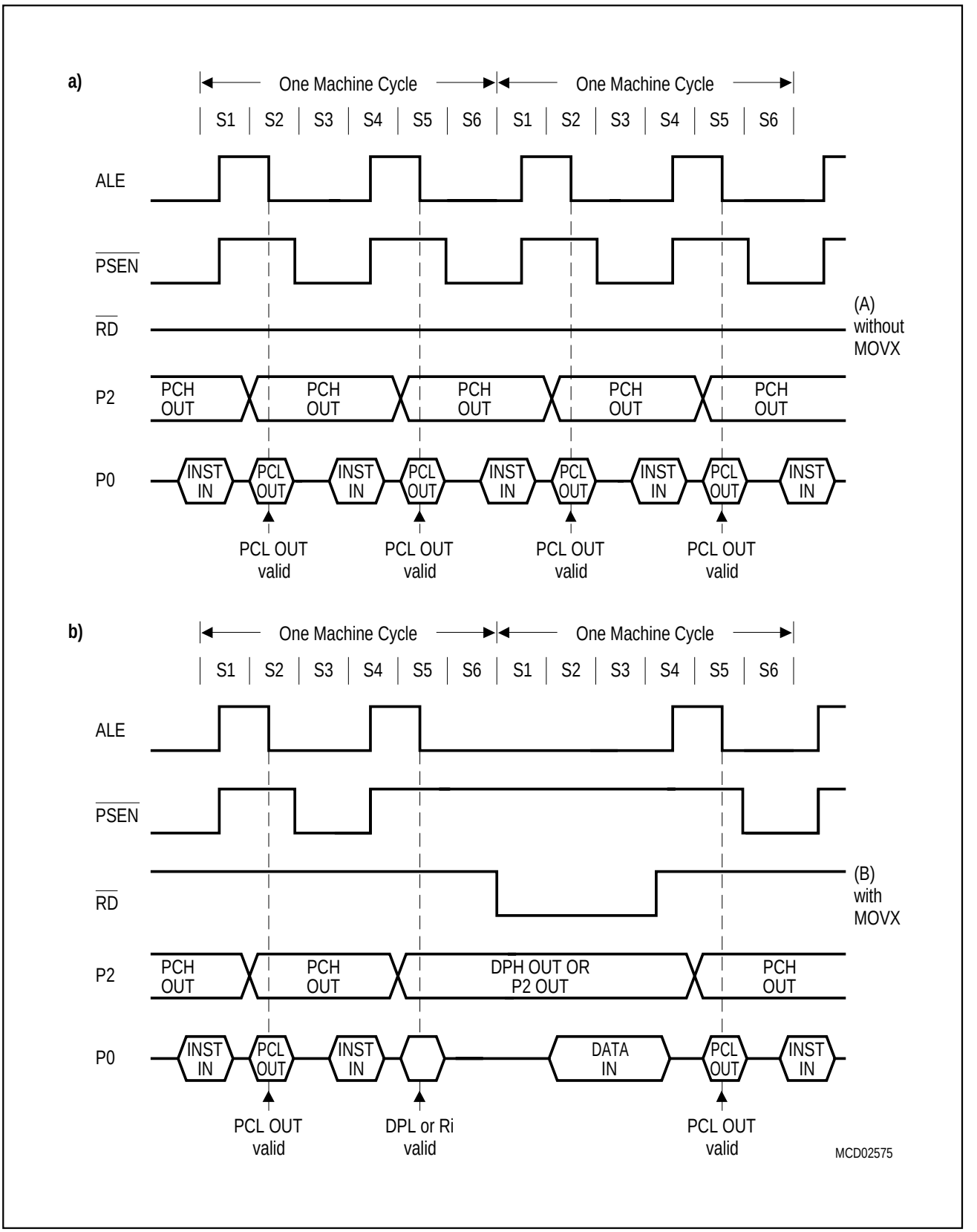


Figure 4-1
External Program Memory Execution

4.4 ALE, Address Latch Enable

The main function of ALE is to provide a properly timed signal to latch the low byte of an address from P0 into an external latch during fetches from external memory. The address byte is valid at the negative transition of ALE. For that purpose, ALE is activated twice every machine cycle. This activation takes place even if the cycle involves no external fetch. The only time no ALE pulse comes out is during an access to external data memory when RD/WR signals are active. The first ALE of the second cycle of a MOVX instruction is missing (see **figure 4-1 b**). Consequently, in any system that does not use data memory, ALE is activated at a constant rate of 1/6 of the oscillator frequency and can be used for external clocking or timing purposes.

The C504 allows to switch off the ALE output signal. If the internal ROM is used ($\overline{EA}$=1) and ALE is switched off by EALE=0, ALE will only go active during external data memory accesses (MOVX instructions) and code memory accesses with an address greater than $3FFF_H$ (external code memory fetches). If $\overline{EA}$=0, the ALE generation is always enabled and the bit EALE has no effect.

After a hardware reset the ALE generation is enabled.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX10XXX0_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	–	–	–	XMAP	SYSCON

The function of the shaded bit is not described in this section.

Bit	Function
–	Not implemented. Reserved for future use.
EALE	Enable ALE output EALE = 0 : ALE generation is disabled; disables ALE signal generation during internal code memory accesses ($\overline{EA}$=1). With $\overline{EA}$=1, ALE is automatically generated at MOVX instructions and code memory accesses with an address greater $3FFF_H$. EALE = 1 : ALE generation is enabled If $\overline{EA}$=0, the ALE generation is always enabled and the bit EALE has no effect on the ALE generation.

4.5 Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.
Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

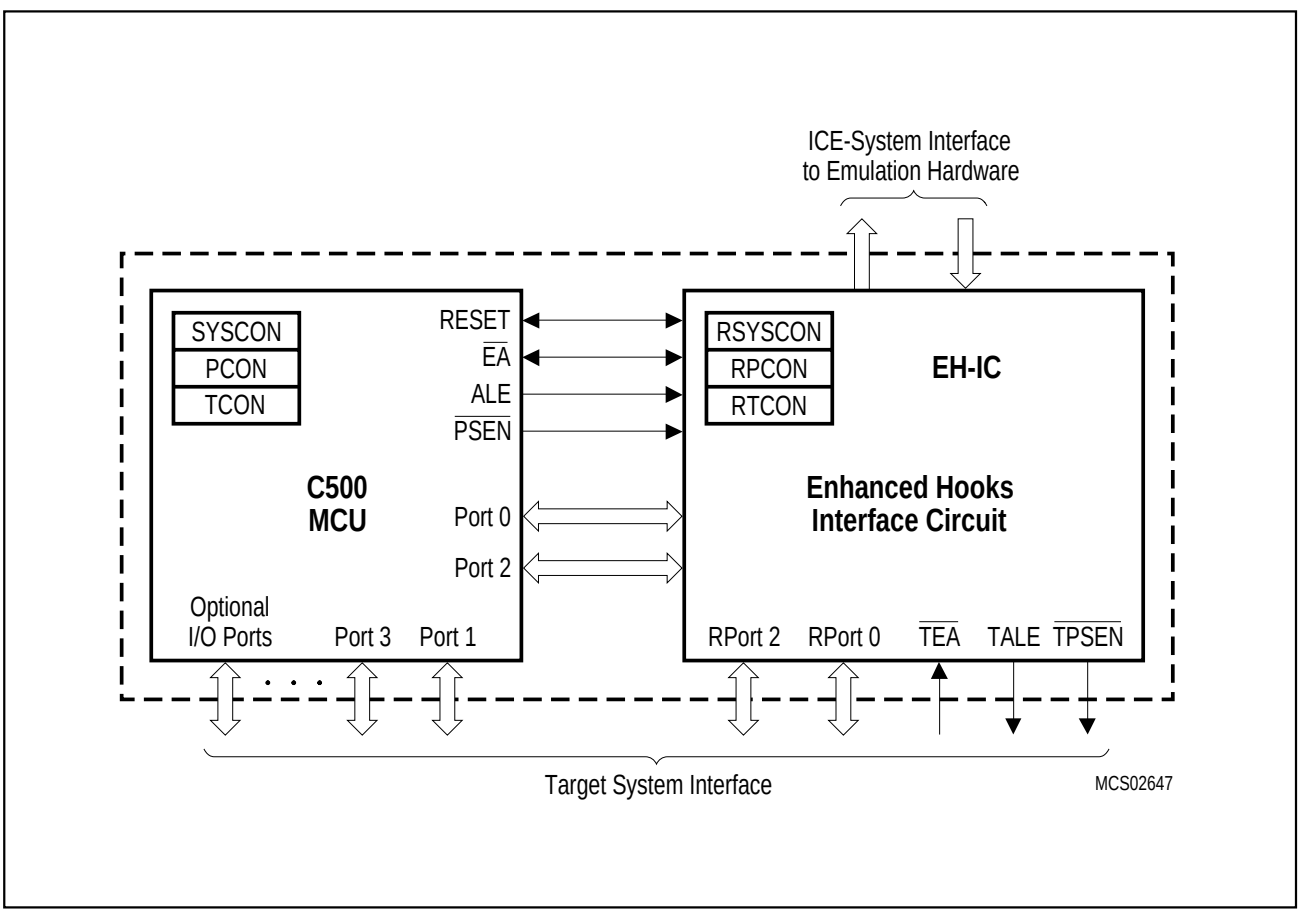


Figure 4-2
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

4.6 ROM/OTP Protection for C504-2R / C504-2E

The C504-2R ROM version allows to protect the content of the internal ROM against read out by non authorized people. The type of ROM protection (protected or unprotected) is fixed with the ROM mask. Therefore, the customer of a C504-2R ROM version has to define whether ROM protection has to be selected or not.

The C504-2E OTP version allows also program memory protection in several levels (see chapter 10.6). The program memory protection for the C504-2E can be activated after programming of the device.

The C504-2R devices, which operate from internal ROM, are always checked for correct ROM content during production test. Therefore, unprotected and also protected ROMs must provide a procedure to verify the ROM content. In ROM verification mode 1, which is used to verify unprotected ROMs, a ROM address is applied externally to the C504-2R and the ROM data byte is output at port 0. ROM verification mode 2, which is used to verify ROM protected devices, operates different: ROM addresses are generated internally and the expected data bytes must be applied externally to the device (by the manufacturer or by the customer) and are compared internally with the data bytes from the ROM. After 16 byte verify operations the state of the P3.5 pin shows whether the last 16 bytes have been verified correctly.

This mechanism provides a very high security of ROM protection. Only the owner of the ROM code and the manufacturer who know the content of the ROM can read out and verify it with less effort.

4.6.1 Unprotected ROM Mode

If the ROM is unprotected, the ROM verification mode 1 as shown in **figure 4-3** is used to read out the content of the ROM (see also the AC specifications in chapter 10, not valid for C504-2E).

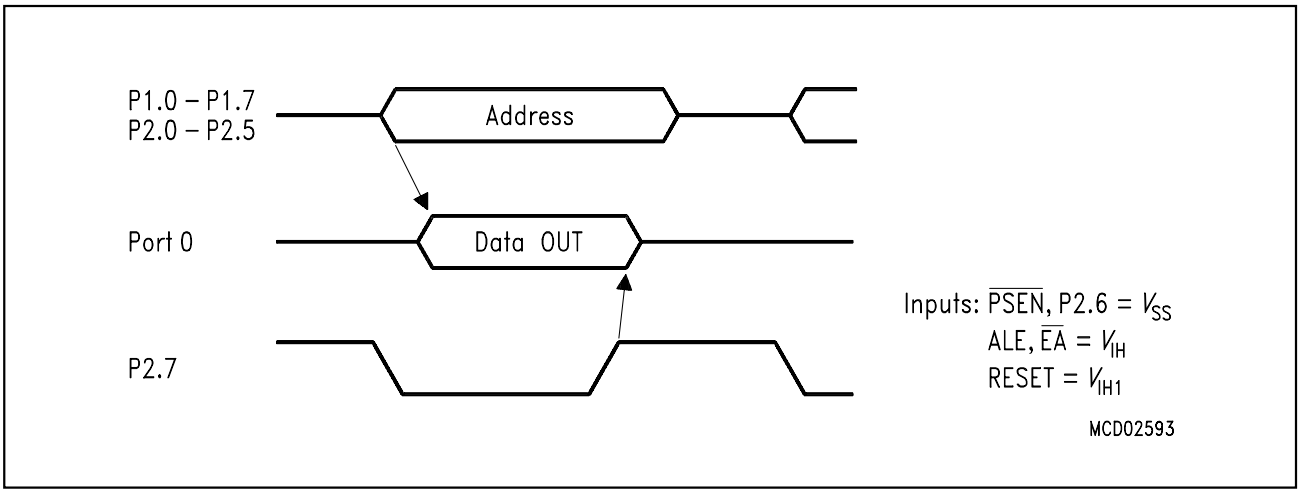


Figure 4-3
ROM Verification Mode 1

ROM verification mode 1 is selected if the inputs $\overline{\text{PSEN}}$, ALE, $\overline{\text{EA}}$, and RESET are put to the specified logic level. P2.6 and P2.7 must be held at low level. Whenever the 14-bit address of the internal ROM byte to be read is applied to the port 1 and port 2, after a delay time, port 0 outputs the content of the addressed internal program memory cell. In ROM verification mode 1, the C504-2R must be provided with a system clock at the XTAL pins and pullup resistors on the port 0 lines.

4.6.2 Protected ROM/OTP Mode

If the C504-2R ROM is protected by mask (or C504-2E OTP in protection level 1), the ROM/OTP verification mode 2 as shown in **figure 4-4** is used to verify the content of the ROM/OTP. The detailed timing characteristics of the ROM/OTP verification mode is shown in the AC specifications (chapter 11).

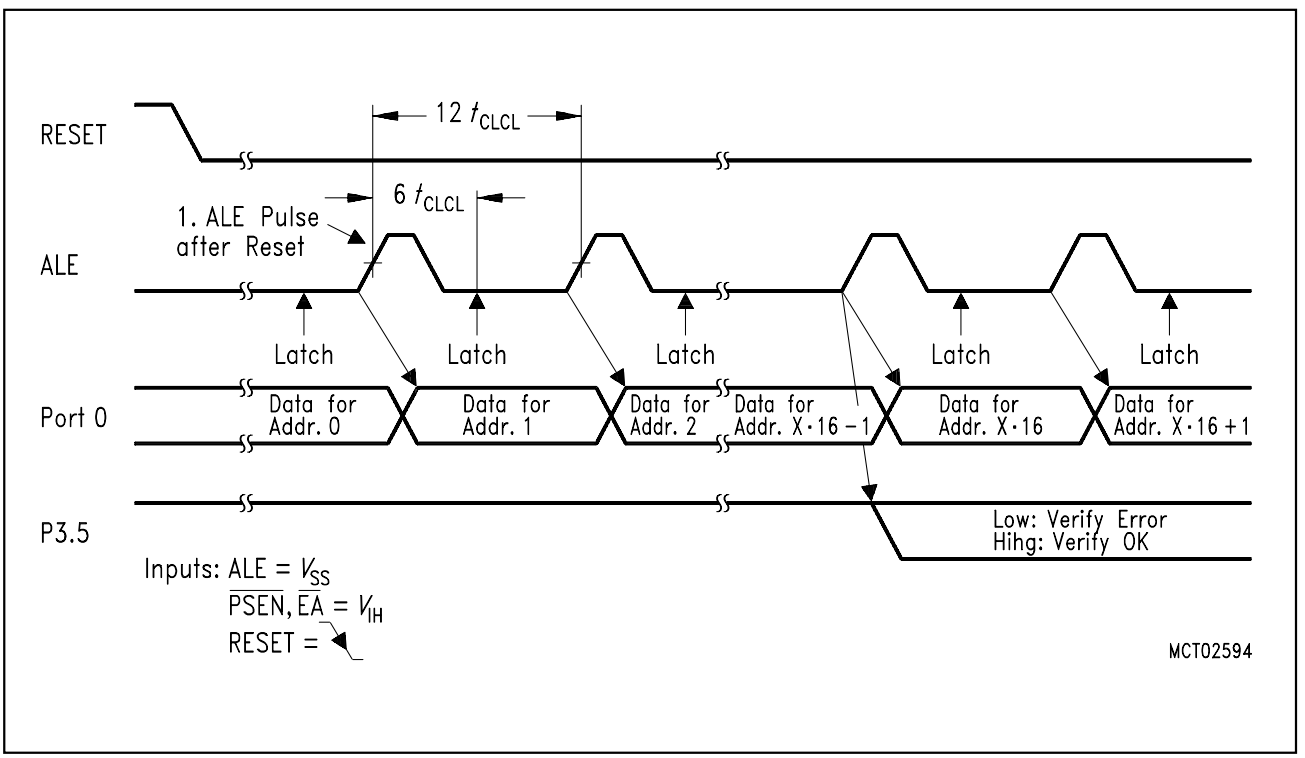


Figure 4-4
ROM Verification Mode 2

ROM/OTP verification mode 2 is selected if the inputs $\overline{PSEN}$, $\overline{EA}$, and ALE are put to the specified logic levels. With RESET going inactive, the ROM/OTP verification mode 2 sequence is started. The C504 outputs an ALE signal with a period of 12 t_{CLCL} and expects data bytes at port 0. The data bytes at port 0 are assigned to the ROM addresses in the following way:

1. Data Byte = content of internal ROM/OTP address 0000_H
2. Data Byte = content of internal ROM/OTP address 0001_H
3. Data Byte = content of internal ROM/OTP address 0002_H
:
16. Data Byte = content of internal ROM/OTP address 000FH
:

The C504 does not output any address information during the ROM/OTP verification mode 2. The first data byte to be verified is always the byte which is assigned to the internal ROM address 0000_H and must be put onto the data bus with the falling edge of RESET. With each following ALE pulse the ROM/OTP address pointer is internally incremented and the expected data byte for the next ROM address must be delivered externally.

Between two ALE pulses the data at port 0 is latched (at 6 t_{CLCL} after ALE rising edge) and compared internally with the ROM/OTP content of the actual address. If an verify error is detected, the error condition is stored internally. After each 16th data byte the cumulated verify result (pass or fail) of the last 16 verify operations is output at P3.5. P3.5 is always set or cleared after each 16 byte block of the verify sequence. In ROM/OTP verification mode 2, the C504 must be provided with a system clock at the XTAL pins.

Figure 4-5 shows an application example of a external circuitry which allows to verify a protected ROM/OTP inside the C504 in ROM/OTP verification mode 2. With RESET going inactive, the C504 starts the ROM/OTP verify sequence. Its ALE is clocking an 14-bit address counter. This counter generates the addresses for an external EPROM which is programmed with the content of the internal (protected) ROM/OTP. The verify detect logic typically displays the state of the verify error output P3.5. P3.5 can be latched with the falling edge of ALE.

When the last byte of the internal ROM/OTP has been handled, the C504 starts generating a $\overline{\text{PSEN}}$ signal. This signal or the CY signal of the address counter indicate to the verify detect logic the end of the internal ROM/OTP verification.

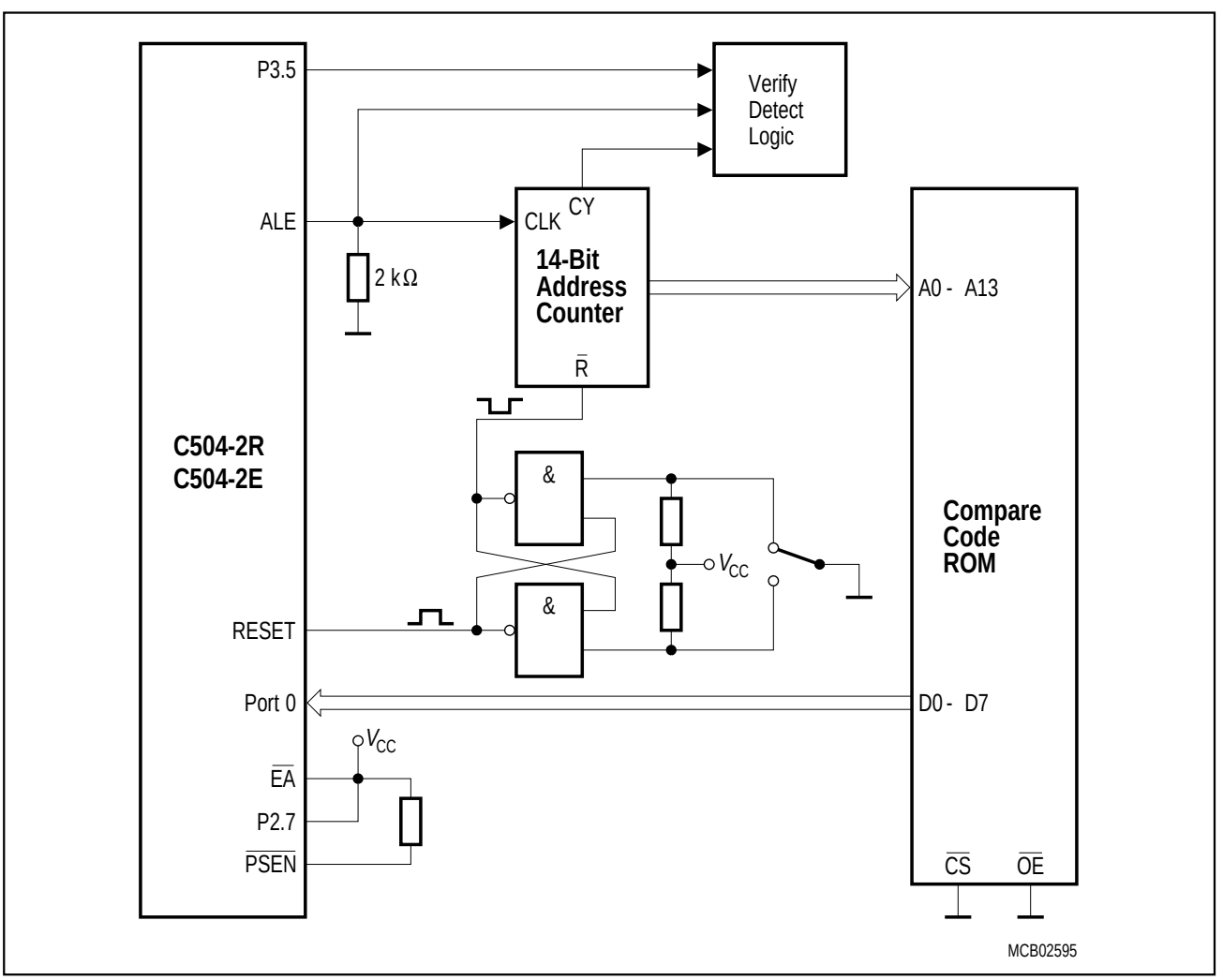


Figure 4-5
ROM/OTP Verification Mode 2 - External Circuitry Example

5 Reset and System Clock Operation

5.1 Hardware Reset Operation

The hardware reset function incorporated in the C504 allows an easy automatic start-up at a minimum of additional hardware and forces the controller to a predefined default state. The hardware reset function can also be used during normal operation in order to restart the device. This is particularly done when the power-down mode is to be terminated.

Additionally to the hardware reset, which is applied externally to the C504, there are two internal reset sources, the watchdog timer and the oscillator watchdog. The chapter at hand only deals with the external hardware reset.

The reset input is an active high input. An internal Schmitt trigger is used at the input for noise rejection. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycle (24 oscillator periods) while the oscillator is running. With the oscillator running the internal reset is executed during the second machine cycle and is repeated every cycle until RESET goes low again.

During reset, pins ALE and $\overline{\text{PSEN}}$ are configured as inputs and should not be stimulated externally. (An external stimulation at these lines during reset activates several test modes which are reserved for test purposes. This in turn may cause unpredictable output operations at several port pins).

At the reset pin, a pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{CC} is applied by connecting the reset pin to V_{CC} via a capacitor. After V_{CC} has been turned on, the capacitor must hold the voltage level at the reset pin for a specific time to effect a complete reset.

The time required for a reset operation is the oscillator start-up time plus 2 machine cycles, which, under normal conditions, must be at least 10 - 20 ms for a crystal oscillator. This requirement is typically met using a capacitor of 4.7 to 10 µF. The same considerations apply if the reset signal is generated externally (**figure 5-1 b**). In each case it must be assured that the oscillator has started up properly and that at least two machine cycles have passed before the reset signal goes inactive.

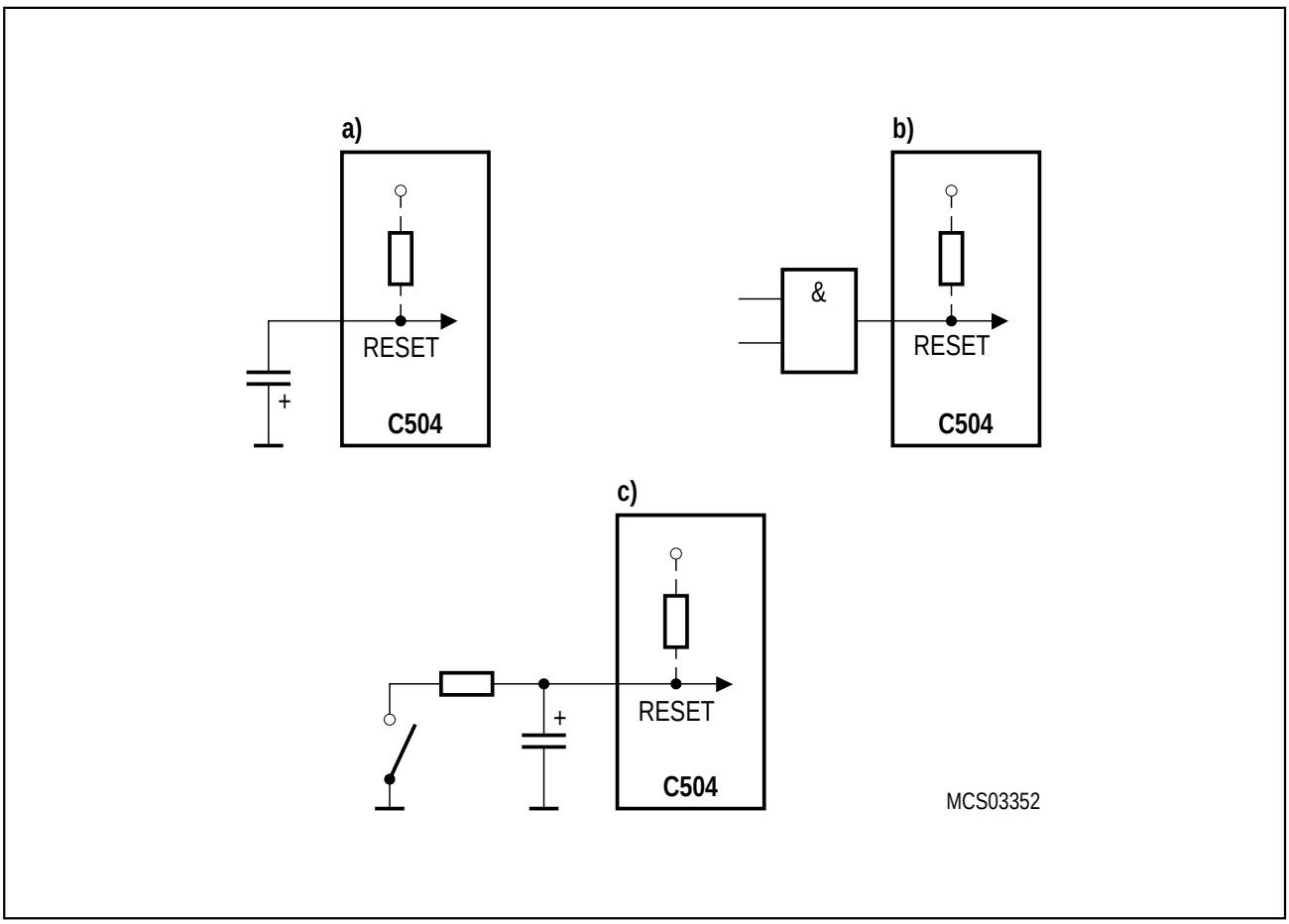


Figure 5-1
Reset Circuitries

A correct reset leaves the processor in a defined state. The program execution starts at location 0000_H. After reset is internally accomplished the port latches of ports 0, 1, 2, and 3 default in FF_H. This leaves port 0 floating, since it is an open drain port when not used as data/address bus. All other I/O port lines (ports 1 to 3) output a one (1).

The contents of the internal RAM and XRAM of the C504 is not affected by a reset. After power-up the contents are undefined, while it remains unchanged during a reset if the power supply is not turned off.

5.2 Fast Internal Reset after Power-On

The C504 uses the oscillator watchdog unit for a fast internal reset procedure after power-on. **Figure 5-1** shows the power-on sequence under control of the oscillator watchdog.

Normally the devices of the 8051 family enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 10 ms). During this time period the pins have an undefined state which could have severe effects especially to actuators connected to port pins.

In the C504 the oscillator watchdog unit avoids this situation. In this case, after power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 microseconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is detected the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state (see **figure 5-2**).

Under worst case conditions (fast V_{CC} rise time - e.g. 1µs, measured from V_{CC} = 4.25 V up to stable port condition), the delay between power-on and the correct port reset state is:

- Typ.: 18 µs
- Max.: 34 µs

The RC oscillator will already run at a V_{CC} below 4.25V (lower specification limit). Therefore, at slower V_{CC} rise times the delay time will be less than the two values given above.

After the on-chip oscillator has finally started, the oscillator watchdog detects the correct function; then the watchdog still holds the reset active for a time period of max. 768 cycles of the RC oscillator clock in order to allow the oscillation of the on-chip oscillator to stabilize (**figure 5-2, II**). Subsequently the clock is supplied by the on-chip oscillator and the oscillator watchdog's reset request is released (**figure 5-2, III**). However, an externally applied reset still remains active (**figure 5-2, IV**) and the device does not start program execution (**figure 5-2, V**) before the external reset is also released.

Although the oscillator watchdog provides a fast internal reset it is additionally necessary to apply the external reset signal when powering up. The reasons are as follows:

- Termination of Software Power-Down Mode
- Reset of the status flag OWDS that is set by the oscillator watchdog during the power up sequence.

Using a crystal or ceramic resonator for clock generation, the external reset signal must be hold active at least until the on-chip oscillator has started and the internal watchdog reset phase is completed (after phase III in **figure 5-2**). When an external clock generator is used, phase II is very short. Therefore, an external reset time of typically 1 ms is sufficient in most applications.

Generally, for reset time generation at power-on an external capacitor can be applied to the RESET pin.

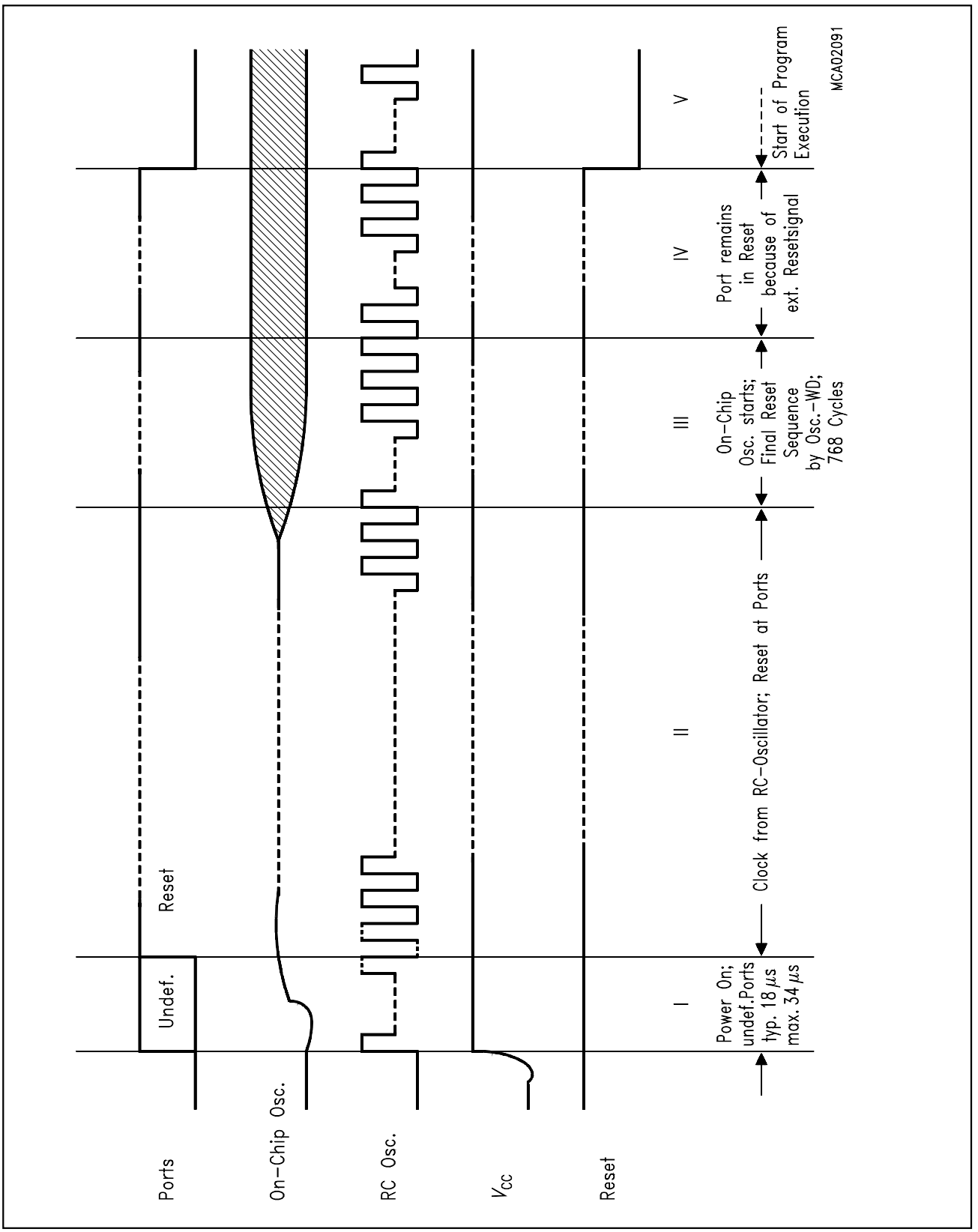


Figure 5-2
Power-On Reset Timing of the C504

5.3 Hardware Reset Timing

This section describes the timing of the hardware reset signal.

The input pin RESET is sampled once during each machine cycle. This happens in state 5 phase 2. Thus, the external reset signal is synchronized to the internal CPU timing. When the reset is found active (high level) the internal reset procedure is started. It needs two complete machine cycles to put the complete device to its correct reset state, i.e. all special function registers contain their default values, the port latches contain 1's etc. Note that this reset procedure is also performed if there is no clock available at the device. (This is done by the oscillator watchdog, which provides an auxiliary clock for performing a perfect reset without clock at the XTAL1 and XTAL2 pins). The RESET signal must be active for at least one machine cycle; after this time the C504 remains in its reset state as long as the signal is active. When the signal goes inactive this transition is recognized in the following state 5 phase 2 of the machine cycle. Then the processor starts its address output (when configured for external ROM) in the following state 5 phase 1. One phase later (state 5 phase 2) the first falling edge at pin ALE occurs.

Figure 5-3 shows this timing for a configuration with $\overline{EA}$ = 0 (external program memory). Thus, between the release of the RESET signal and the first falling edge at ALE there is a time period of at least one machine cycle but less than two machine cycles.

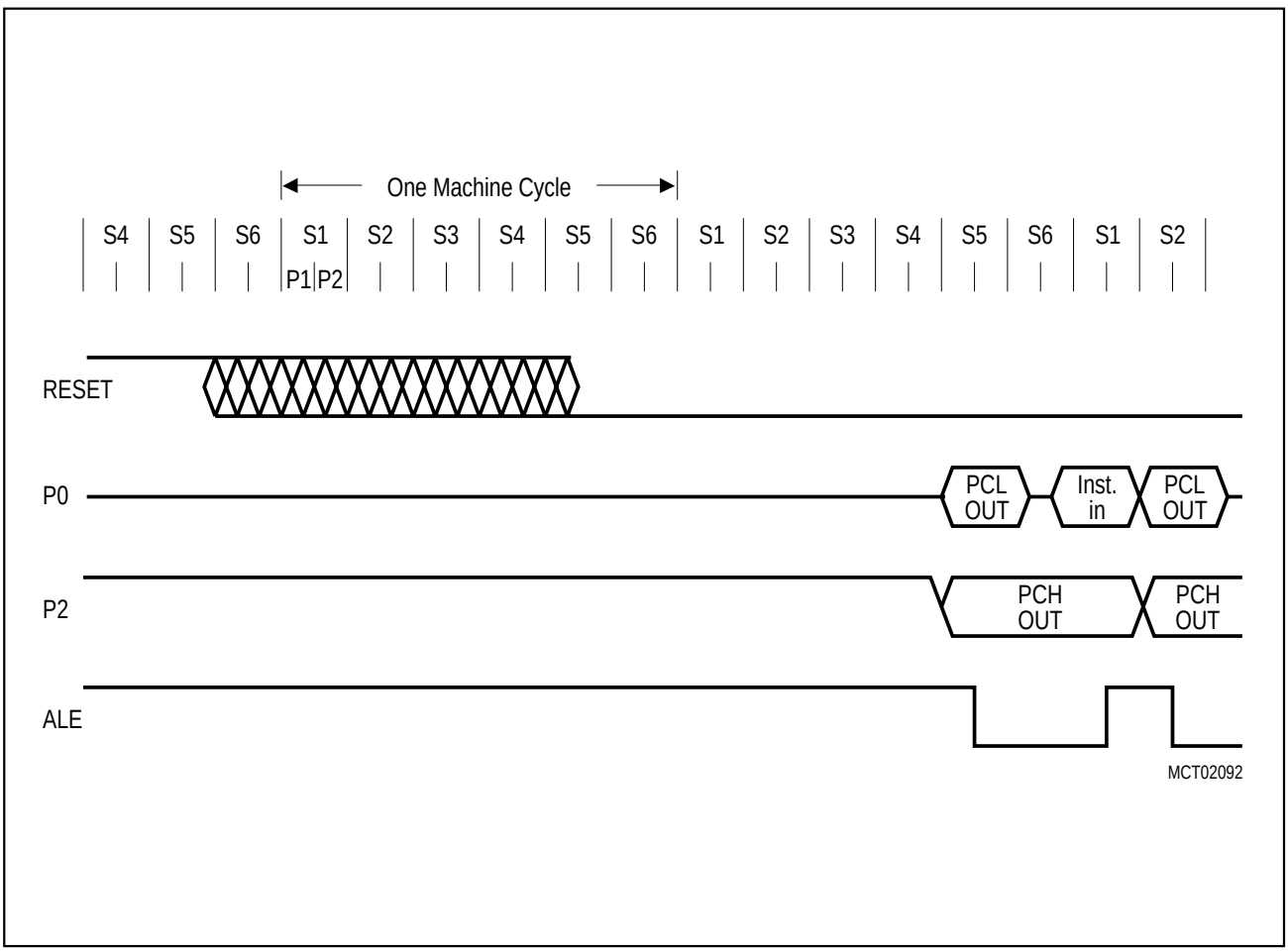


Figure 5-3
CPU Timing after Reset

5.4 Oscillator and Clock Circuit

XTAL1 and XTAL2 are the input and output of a single-stage on-chip inverter which can be configured with off-chip components as a pierce oscillator. The oscillator, in any case, drives the internal clock generator. The clock generator provides the internal clock signals to the chip. These signals define the internal phases, states and machine cycles.

Figure 5-4 shows the recommended oscillator circuit.

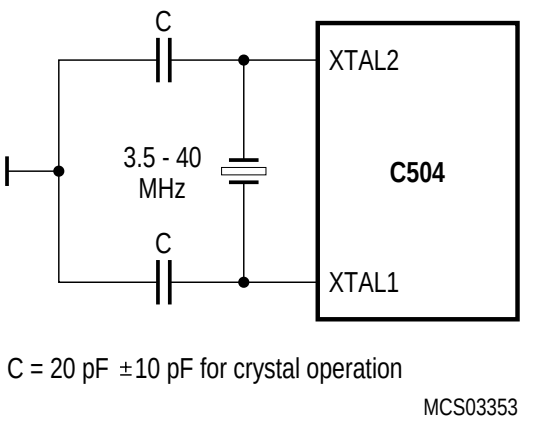


Figure 5-4
Recommended Oscillator Circuit

In this application the on-chip oscillator is used as a crystal-controlled, positive-reactance oscillator (a more detailed schematic is given in **figure 5-5**). It is operated in its fundamental response mode as an inductive reactor in parallel resonance with a capacitor external to the chip. The crystal specifications and capacitances are non-critical. In this circuit 20 pF can be used as single capacitance at any frequency together with a good quality crystal. A ceramic resonator can be used in place of the crystal in cost-critical applications. If a ceramic resonator is used, the two capacitors normally have different values depending on the oscillator frequency. We recommend consulting the manufacturer of the ceramic resonator for value specifications of these capacitors.

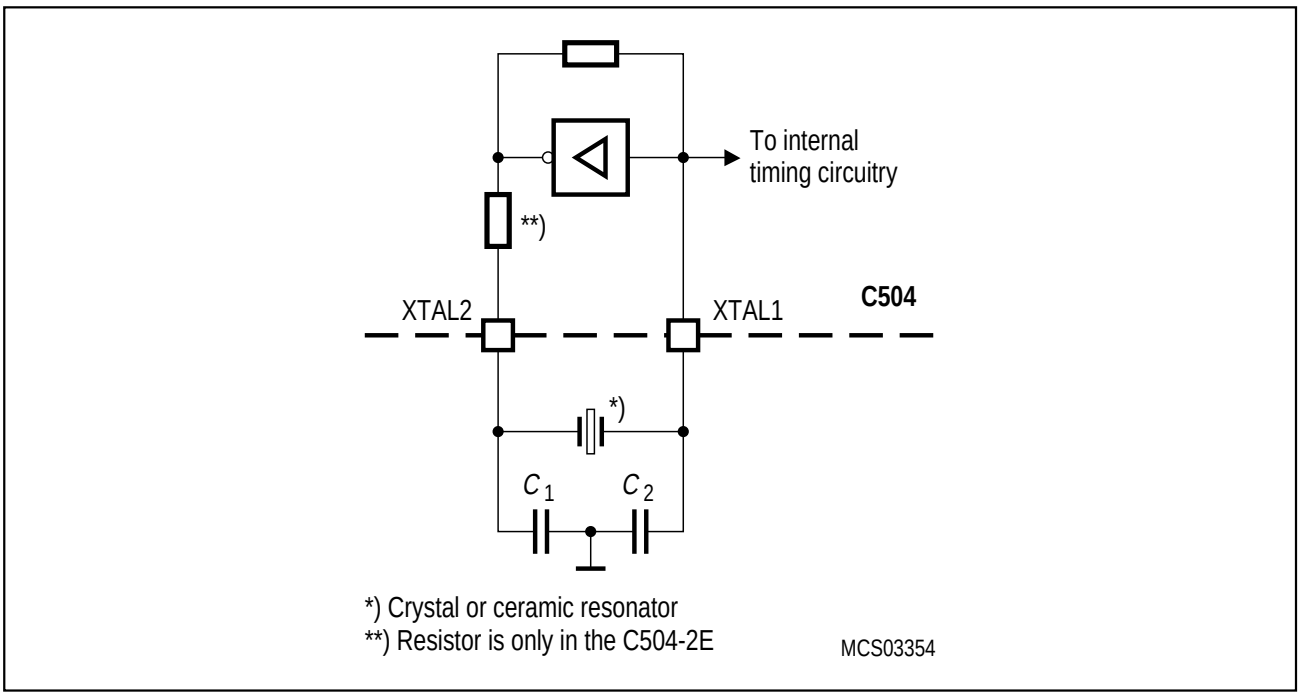


Figure 5-5
On-Chip Oscillator Circuiry

To drive the C504 with an external clock source, the external clock signal has to be applied to XTAL1, as shown in **figure 5-6**. XTAL2 has to be left unconnected. A pullup resistor is suggested (to increase the noise margin), but is optional if V_{OH} of the driving gate corresponds to the V_{IH2} specification of XTAL1.

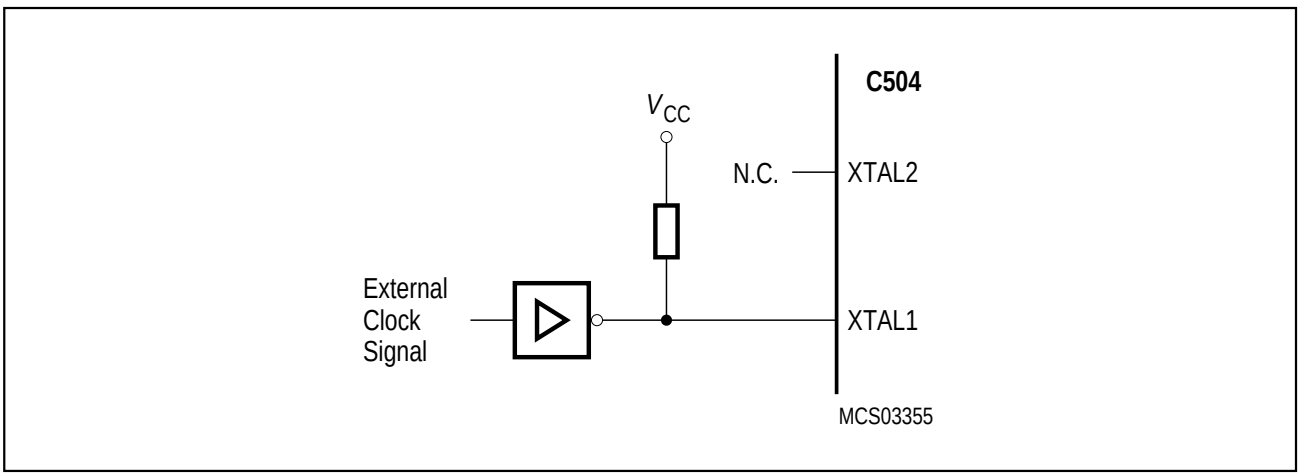


Figure 5-6
External Clock Source

6 On-Chip Peripheral Components

6.1 Parallel I/O

The C504 has four 8-bit I/O ports. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 3 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 3 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

6.1.1 Port Structures

The C504 generally allows digital I/O on 32 lines grouped into 4 bidirectional 8-bit ports. Each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0-P3 are performed via their corresponding special function registers. Depending on the specific ports, multiple functions are assigned to the port pins. Therefore, the parallel I/O ports of the C504 can be grouped into five different types which are listed in **table 6-1**.

Table 6-1
C504 Port Structures

Type	Description
A	Standard digital I/O ports which can be also used for external address/data bus.
B	Standard multifunctional digital I/O port lines
C	Mixed digital/analog I/O port lines with programmable analog input function
D	Standard digital I/O port lines with push-pull drive capability
E	Mixed digital/analog I/O port lines with push-pull drive capability and programmable analog input function

Type A and B port pins are standard C501 compatible I/O port lines, which can be used for digital I/O. The type A ports (port 0 and port 2) are also designed for accessing external data or program memory. Type B port lines are located at port 3 and provide alternate functions for the serial interface or are used as control outputs during external data memory accesses.

The C504 provides eight analog input lines which are realized as mixed digital/analog inputs. The 8 analog inputs are split into two groups of four inputs each. Four analog inputs AN0-AN3 are located at the port 1 pins P1.0 to P1.3 and the other four analog inputs AN4-AN7 are located at the port 3 pins P3.2 to P3.5 (type C and type E port lines). After reset, all analog inputs are disabled and the related pins of port 1 and 3 are configured as digital inputs. The analog function of the specific port 1 and port 3 pins is enabled by bits in the SFRs P1ANA and P3ANA. Writing a 0 to a bit position of P1ANA or P3ANA assigns the corresponding pin to operate as analog input.

Note: P1ANA and P3ANA are mapped SFRs and can be only accessed if bit RMAP in SFR SYSCON is set (description see chapter 6.5.4).

Type D and E port lines can be switched to push-pull drive capability when they are used as compare outputs of the CAPCOM unit.

As already mentioned, port 1 and 3 are provided for multiple alternate functions. These second and third functions of the port 1 and 3 lines are listed in **table 6-2**:

Table 6-2
Alternate Functions of Port 1 and 3

Port	Second / third Function	Port Type	Function
P1.0	AN0 / T2	C	Analog input channel 0 / input to counter 2
P1.1	AN1 / T2EX	C	Analog input channel 1 / capture-reload trigger of timer 2 / up down count
P1.2	AN2 / CC0	E	Analog input channel 2 / CAPCOM channel 0 input/output
P1.3	AN3 / COUT0	E	Analog input channel 3 / CAPCOM channel 0 output
P1.4	CC1	D	CAPCOM channel 1 input/output
P1.5	COUT1	D	CAPCOM channel 1 output
P1.6	CC2	D	CAPCOM channel 2 input/output
P1.7	COUT2	D	CAPCOM channel 2 output
P3.0	RxD	B	Serial port's receiver data input (asynchronous) or data input/ output (synchronous)
P3.1	TxD	B	Serial port's transmitter data output (asynchronous) or data clock output (synchronous)
P3.2	AN4 / $\overline{\text{INT0}}$	C	Analog input channel 4 / External interrupt 0 input, timer 0 gate control
P3.3	AN5 / $\overline{\text{INT1}}$	C	Analog input channel 5 / External interrupt 1 input, timer 1 gate control
P3.4	AN6 / T0	C	Analog input channel 6 / Timer 0 external counter input
P3.5	AN7 / T1	C	Analog input channel 7 / Timer 1 external counter input
P3.6	$\overline{\text{WR}}$ / $\overline{\text{INT2}}$	B	External data memory write strobe / External interrupt 2 input
P3.7	$\overline{\text{RD}}$	B	External data momory read strobe

Prior to the description of the port type specific port configurations the general port structure is described in the next section.

6.1.2 Standard I/O Port Circuitry

Figure 6-1 shows a functional diagram of a typical bit latch and I/O buffer, which is the core of each of the four I/O-ports. The bit latch (one bit in the port's SFR) is represented as a type-D flip-flop, which will clock in a value from the internal bus in response to a "write-to-latch" signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a "read-latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read-pin" signal from the CPU. Some instructions that read from a port (i.e. from the corresponding port SFR P0, P2, P3) activate the "read-latch" signal, while others activate the "read-pin" signal.

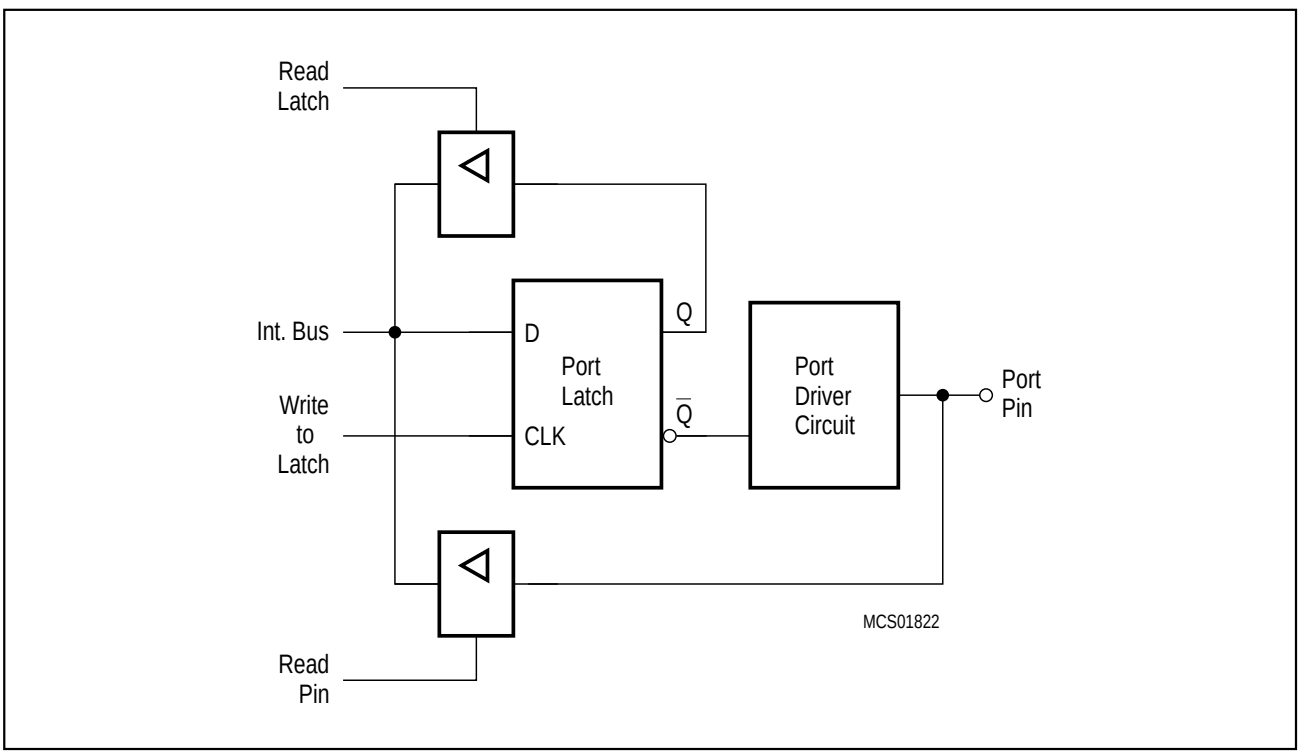


Figure 6-1
Basic Structure of a Port Circuitry

Port 1, 2 and 3 output drivers have internal pullup FET's (see **figure 6-2**). Each I/O line can be used independently as an input or output. To be used as an input, the port bit must contain a one (1) (that means for **figure 6-2**: Q=0), which turns off the output driver FET n1. Then, for ports 1, 2 and 3, the pin is pulled high by the internal pullups, but can be pulled low by an external source. When externally pulled low the port pins source current (I_{IL} or I_{TL}). For this reason these ports are sometimes called "quasi-bidirectional".

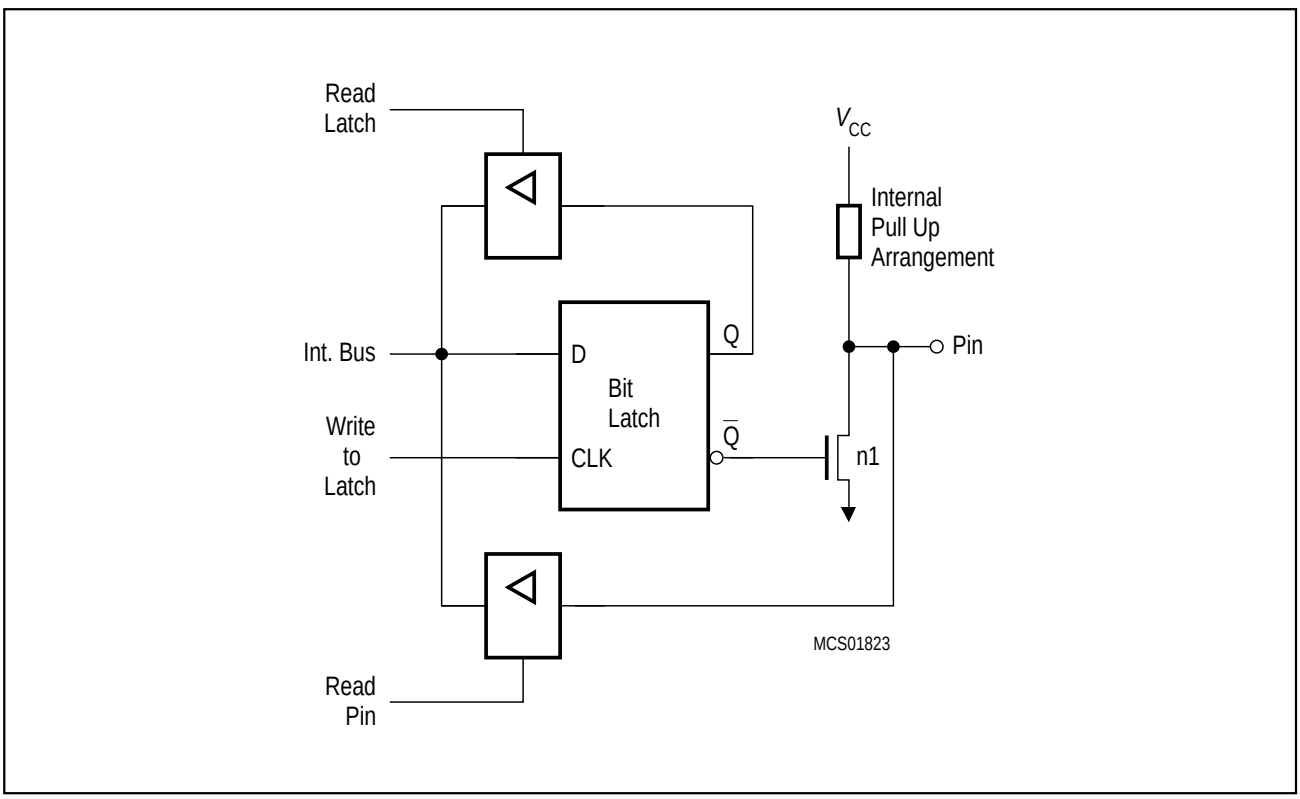


Figure 6-2
Basic Output Driver Circuit of Ports 1, 2 and 3

6.1.2.1 Port 0 Circuitry

Port 0, in contrast to ports 1, 2 and 3, is considered as "true" bidirectional, because the port 0 pins float when configured as inputs. Thus, this port differs in not having internal pullups. The pullup FET in the P0 output driver (see **figure 6-3**) is used only when the port is emitting 1 s during the external memory accesses. Otherwise, the pullup is always off. Consequently, P0 lines that are used as output port lines are open drain lines. Writing a "1" to the port latch leaves both output FETs off and the pin floats. In that condition it can be used as high-impedance input. If port 0 is configured as general I/O port and has to emit logic high-level (1), external pullups are required.

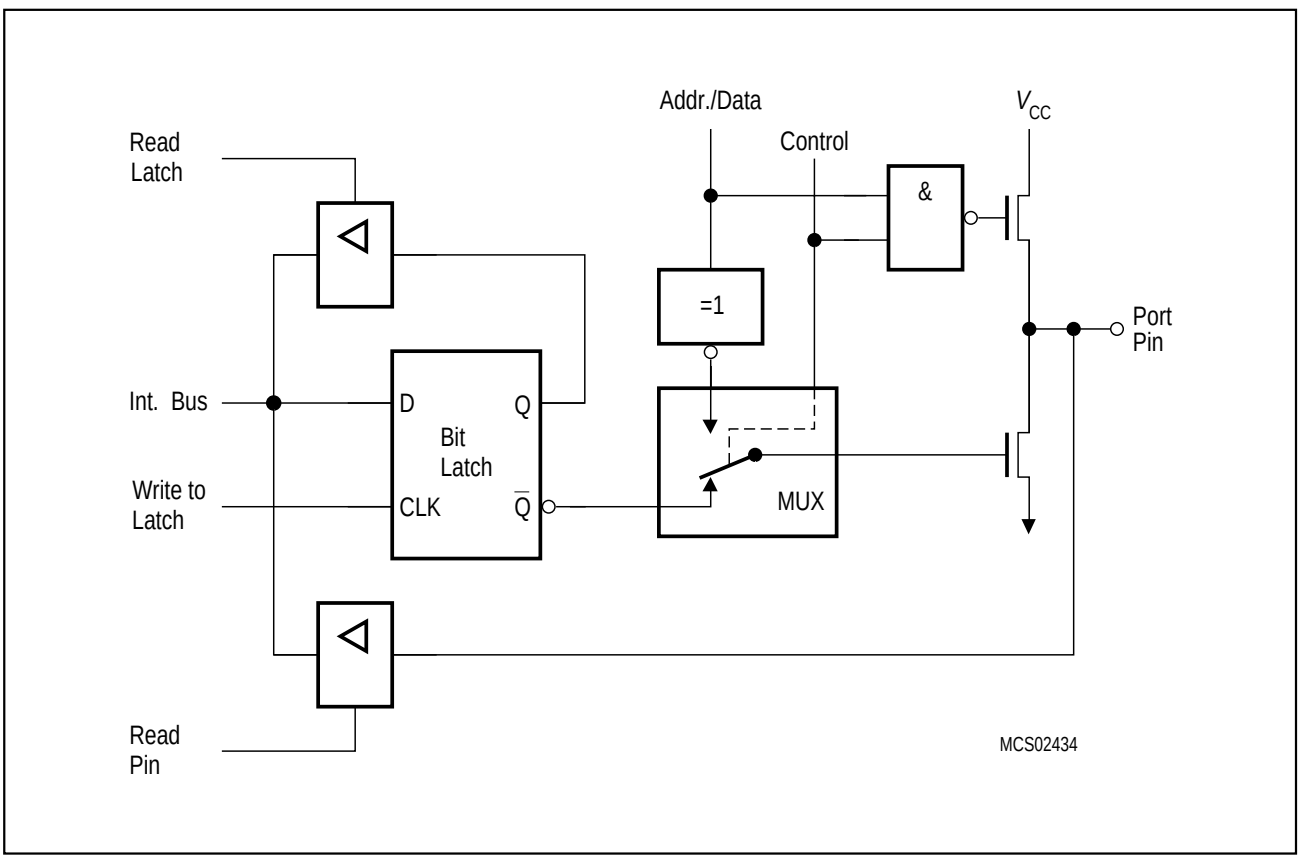


Figure 6-3
Port 0 Circuitry

6.1.2.2 Port 1 and Port 3 Circuitry

The pins of ports 1 and 3 are multifunctional. They are port pins and also serve to implement special features as listed in **table 6-2**.

Figure 6-4 shows a functional diagram of a port latch with alternate function. To pass the alternate function to the output pin and vice versa, however, the gate between the latch and driver circuit must be open. Thus, to use the alternate input or output functions, the corresponding bit latch in the port SFR has to contain a one (1); otherwise the pulldown FET is on and the port pin is stuck at 0. After reset all port latches contain ones (1).

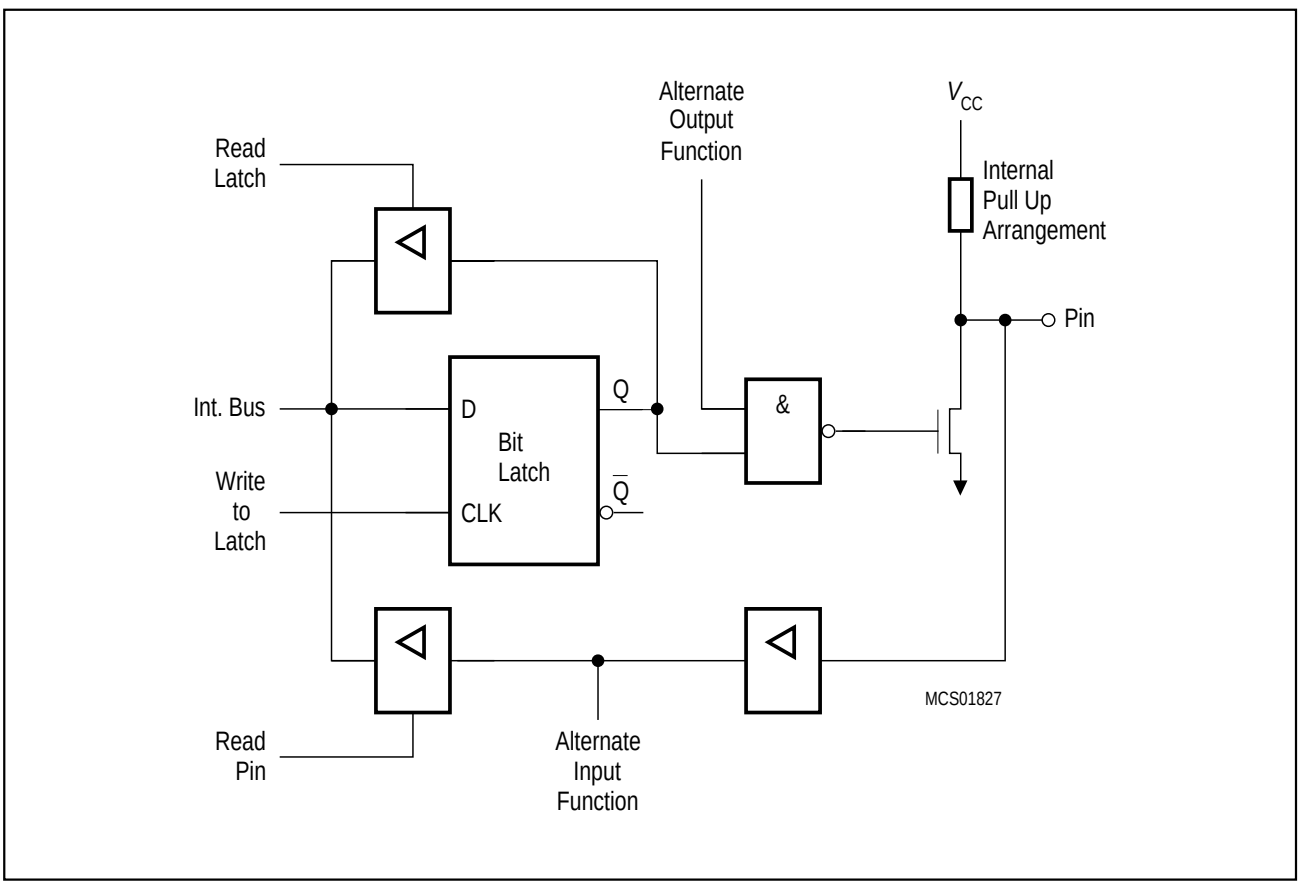


Figure 6-4
Ports 1 and 3

6.1.2.3 Port 2 Circuitry

As shown in **figure 6-3** and below in **figure 6-5**, the output drivers of ports 0 and 2 can be switched to an internal address or address/data bus for use in external memory accesses. In this application they cannot be used as general purpose I/O, even if not all address lines are used externally. The switching is done by an internal control signal dependent on the input level at the EA pin and/or the contents of the program counter. If the ports are configured as an address/data bus, the port latches are disconnected from the driver circuit. During this time, the P2 SFR remains unchanged while the P0 SFR has 1's written to it. Being an address/data bus, port 0 uses a pullup FET as shown in **figure 6-5**. When a 16-bit address is used, port 2 uses the additional strong pullups p1 (**figure 6-6**) to emit 1's for the entire external memory cycle instead of the weak ones (p2 and p3) used during normal port activity.

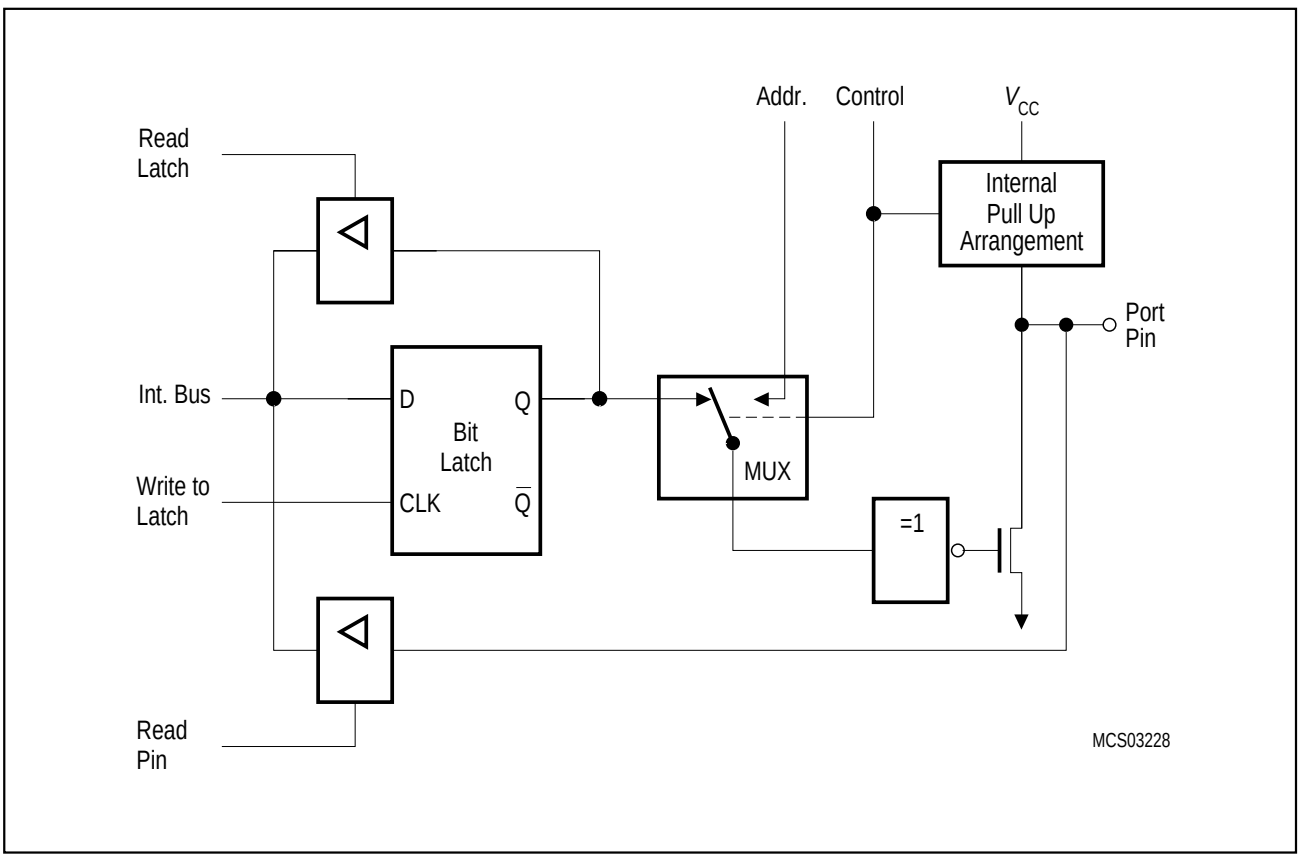


Figure 6-5
Port 2 Circuitry

If no external bus cycles are generated using data or code memory accesses, port 0 can be used for I/O functions. Note : during MOVX accesses to the internal XRAM no external bus cycles are generated.

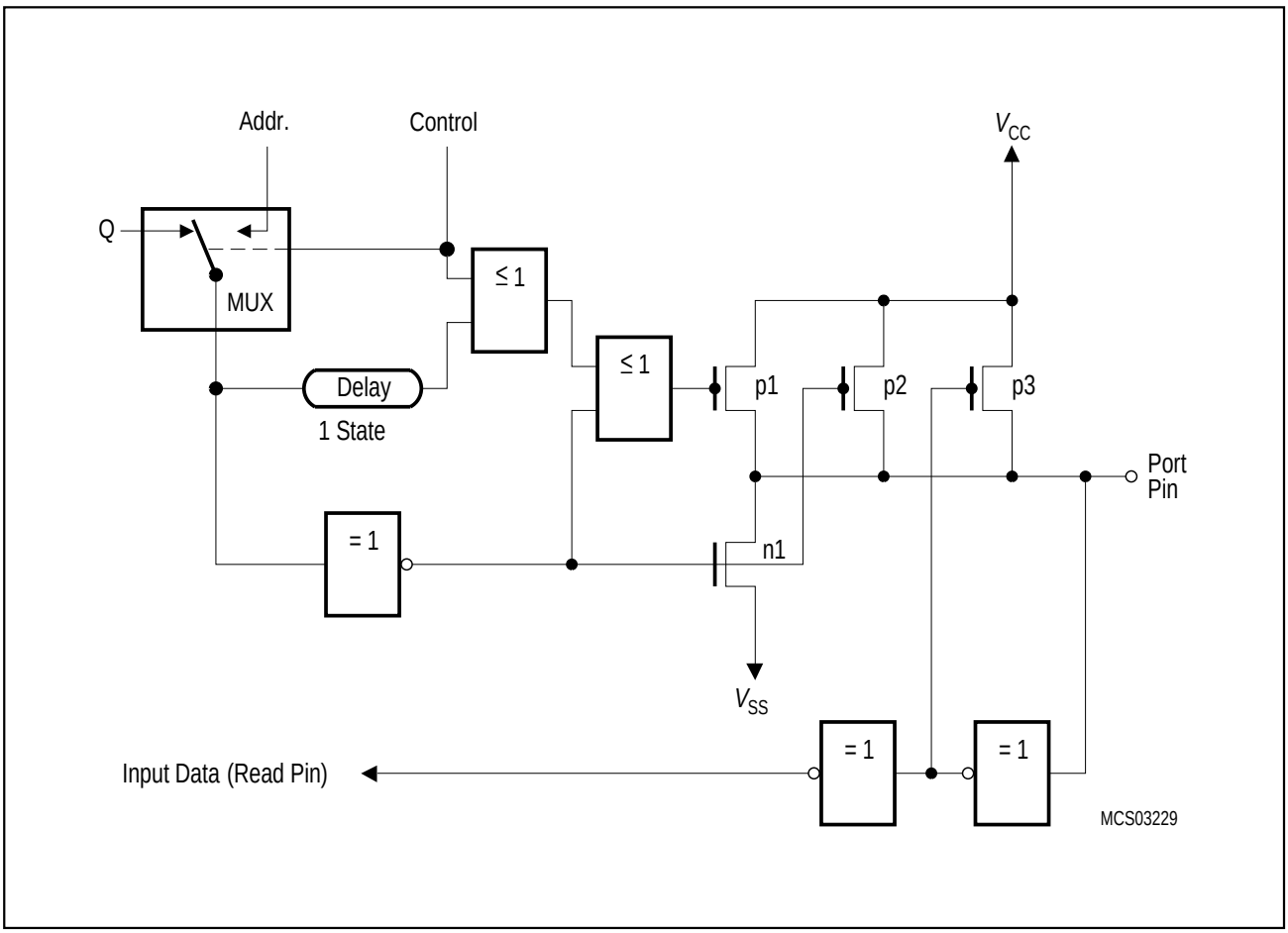


Figure 6-6
Port 2 Pull-up Arrangement

Port 2 in I/O function works similar to the standard port driver circuitry whereas in address output function it works similar to Port 0 circuitry.

6.1.3 Detailed Output Driver Circuitry

In fact, the pullups mentioned before and included in **figure 6-2, 6-4** and **6-5** are pullup arrangements. The differences of the port types available in the C504 is described in the next sections.

6.1.3.1 Type B Port Driver Circuitry

Figure 6-7 shows the output driver circuit of the type B multifunctional digital I/O port lines. The basic circuitry of these ports is shown in **figure 6-4**.The pullup arrangement of type B port lines has one n-channel pulldown FET and three pullup FETs:

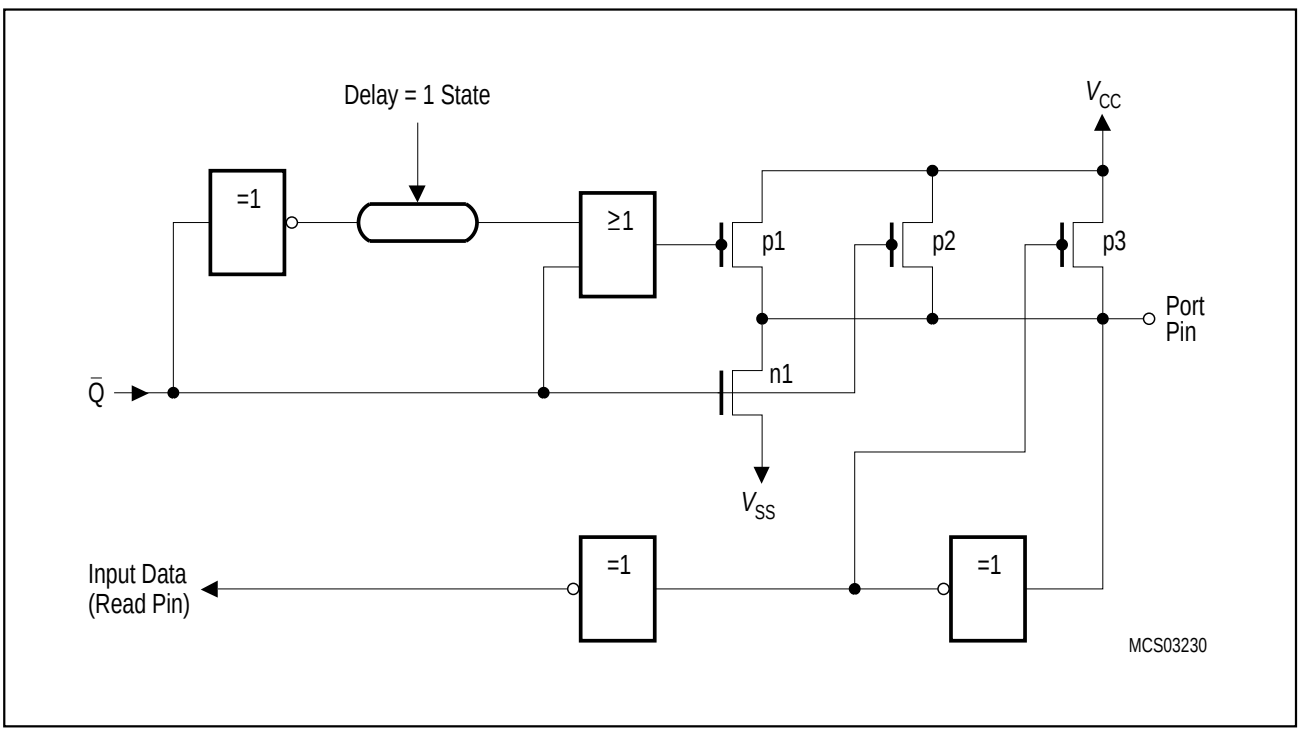


Figure 6-7
Driver Circuit of Type B Port Pins

- The **pulldown FET n1** is of n-channel type. It is a very strong driver transistor which is capable of sinking high currents (I_{OL}); it is only activated if a "0" is programmed to the port pin. A short circuit to V_{CC} must be avoided if the transistor is turned on, since the high current might destroy the FET. This also means that no “0“ must be programmed into the latch of a pin that is used as inpu.
- The **pullup FET p1** is of p-channel type. It is activated for one state (S1) if a 0-to-1 transition is programmed to the port pin, i.e. a "1" is programmed to the port latch which contained a "0". The extra pullup can drive a similar current as the pulldown FET n1. This provides a fast transition of the logic levels at the pin.
- The **pullup FET p2** is of p-channel type. It is always activated when a "1" is in the port latch, thus providing the logic high output level. This pullup FET sources a much lower current than p1; therefore the pin may also be tied to ground, e.g. when used as input with logic low input level.

– The **pullup FET p3** is of p-channel type. It is only activated if the voltage at the port pin is higher than approximately 1.0 to 1.5 V. This provides an additional pullup current if a logic high level shall be output at the pin (and the voltage is not forced lower than approximately 1.0 to 1.5 V). However, this transistor is turned off if the pin is driven to a logic low level, e.g when used as input. In this configuration only the weak pullup FET p2 is active, which sources the current I_{IL} . If, in addition, the pullup FET p3 is activated, a higher current can be sourced (I_{TL}). Thus, an additional power consumption can be avoided if port pins are used as inputs with a low level applied. However, the driving capability is stronger if a logic high level is output.

The described activating and deactivating of the four different transistors translates into four states the pins can be:

– input low state (IL), p2 active only
– input high state (IH) = steady output high state (SOH) p2 and p3 active
– forced output high state (FOH), p1, p2 and p3 active
– output low state (OL), n1 active

If a pin is used as input and a low level is applied, it will be in IL state, if a high level is applied, it will switch to IH state.

If the latch is loaded with "0", the pin will be in OL state.

If the latch holds a "0" and is loaded with "1", the pin will enter FOH state for two cycles and then switch to SOH state. If the latch holds a "1" and is reloaded with a "1" no state change will occur.

At the beginning of power-on reset the pins will be in IL state (latch is set to "1", voltage level on pin is below of the trip point of p3). Depending on the voltage level and load applied to the pin, it will remain in this state or will switch to IH (=SOH) state.
If it is used as output, the weak pull-up p2 will pull the voltage level at the pin above p3's trip point after some time and p3 will turn on and provide a strong "1". Note, however, that if the load exceeds the drive capability of p2 (I_{IL}), the pin might remain in the IL state and provide a week "1" until the first 0-to-1 transition on the latch occurs. Until this the output level might stay below the trip point of the external circuitry.

The same is true if a pin is used as bidirectional line and the external circuitry is switched from outpout to input when the pin is held at "0" and the load then exceeds the p2 drive capabilities.

If the load exceeds I_{IL} the pin can be forced to "1" by writing a "0" followed by a "1" to the port pin.

6.1.3.2 Type C Port Driver Circuitry

Figure 6-8 shows the port driver circuit of the type C mixed digital/analog I/O port lines of the C504. The analog function is selected by the bits in the SFRs P1ANA and P3ANA.

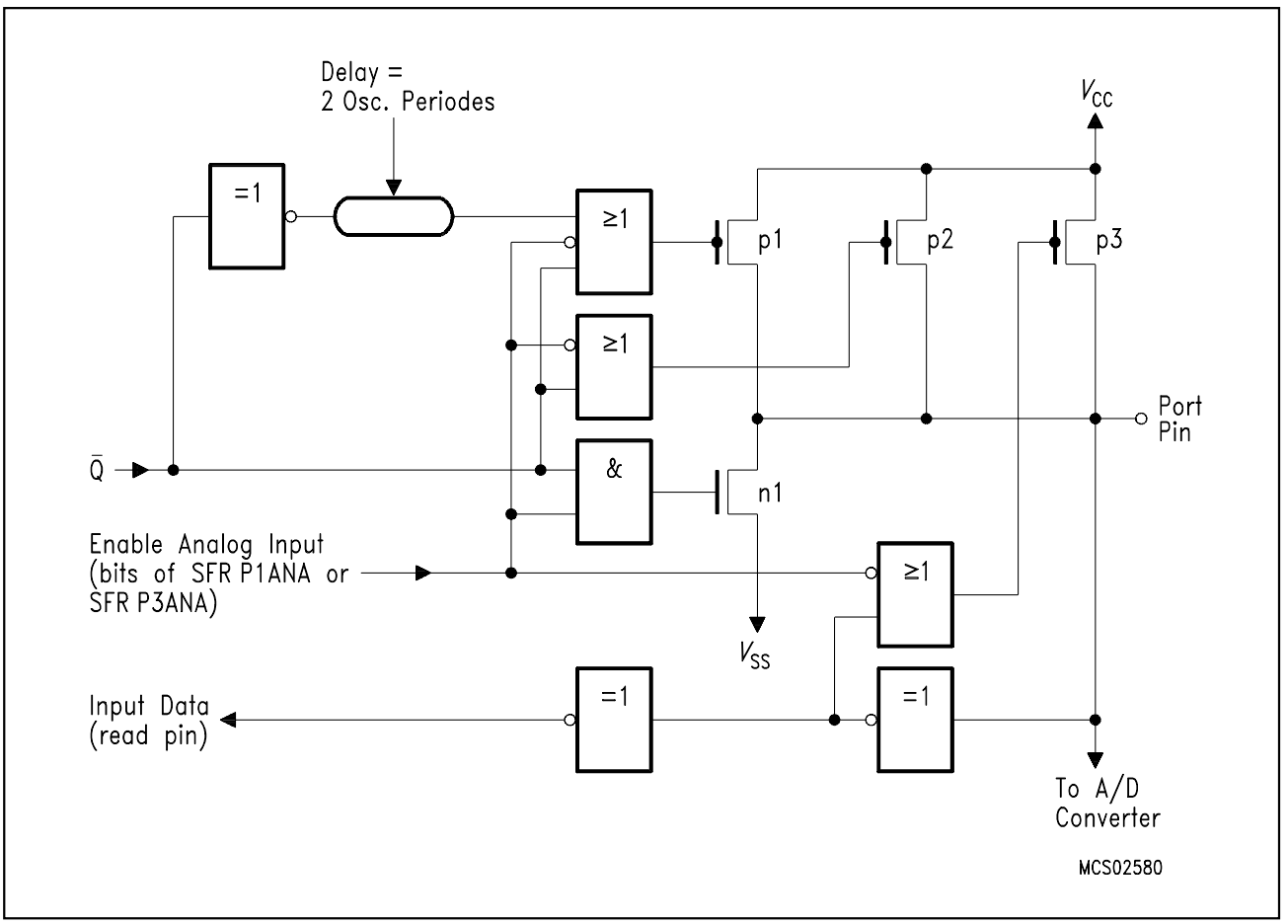


Figure 6-8
Driver Circuit of Type C Port Pins

6.1.3.3 Type D Port Driver Circuitry

The driver and control structure of the port pins used for compare output functions have a port structure which allows a true push-pull output driving capability (Type D). This output driver characteristic is only enabled/used when the corresponding port lines are used as compare outputs. The analog function is selected by the bits in the SFRs P1ANA and P3ANA.

The push-pull port structure is illustrated in **figure 6-9**.

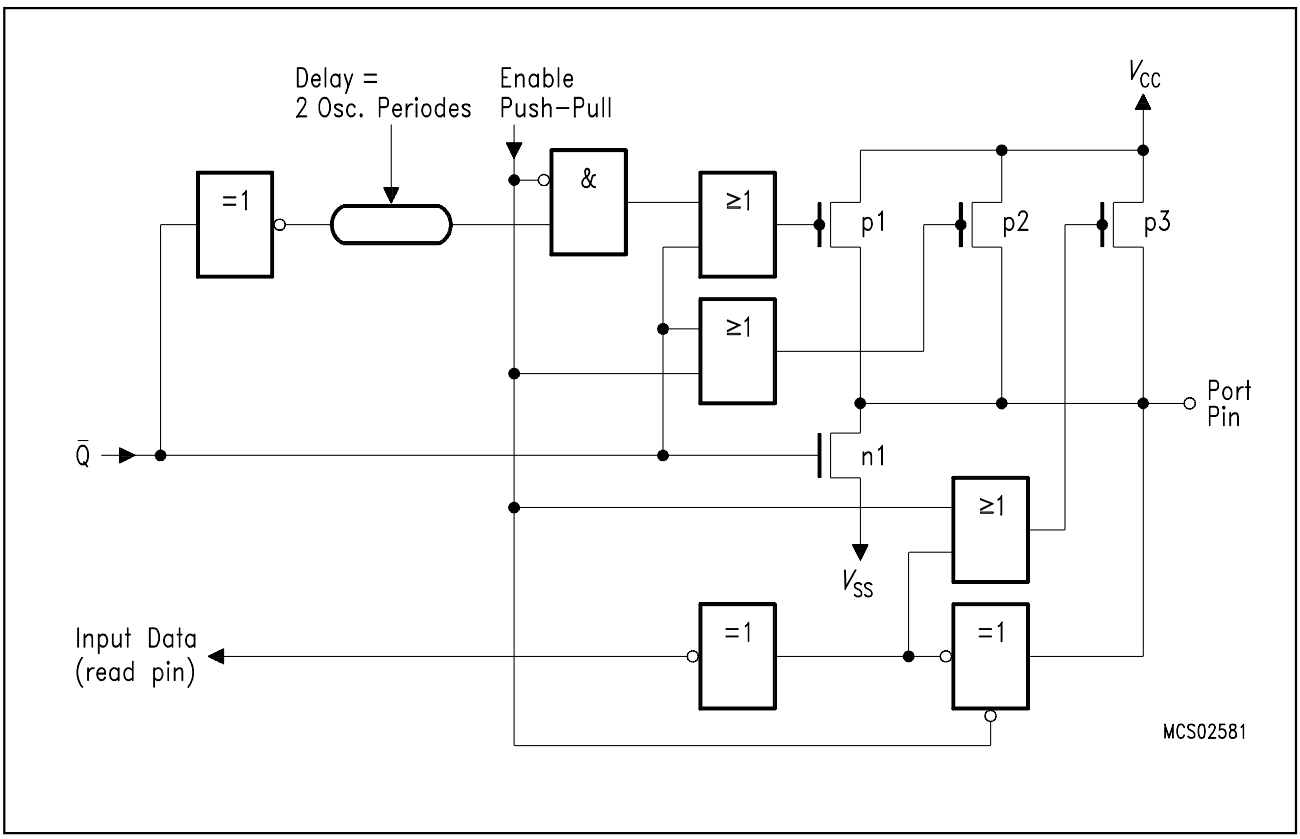


Figure 6-9
Driver Circuit of Type D Port Pins

6.1.3.4 Type E Port Driver Circuitry

The type E ports are a combination of type C and type D port drivers. They combine push-pull driving characteristic with the capability to select the port pin for analog input function. The push-pull driver characteristic is only enabled/used when the corresponding port lines are used as compare outputs. The analog function is selected by the bits in the SFRs P1ANA and P3ANA.

The push-pull mixed digital/analog port structure is illustrated in **figure 6-10**.

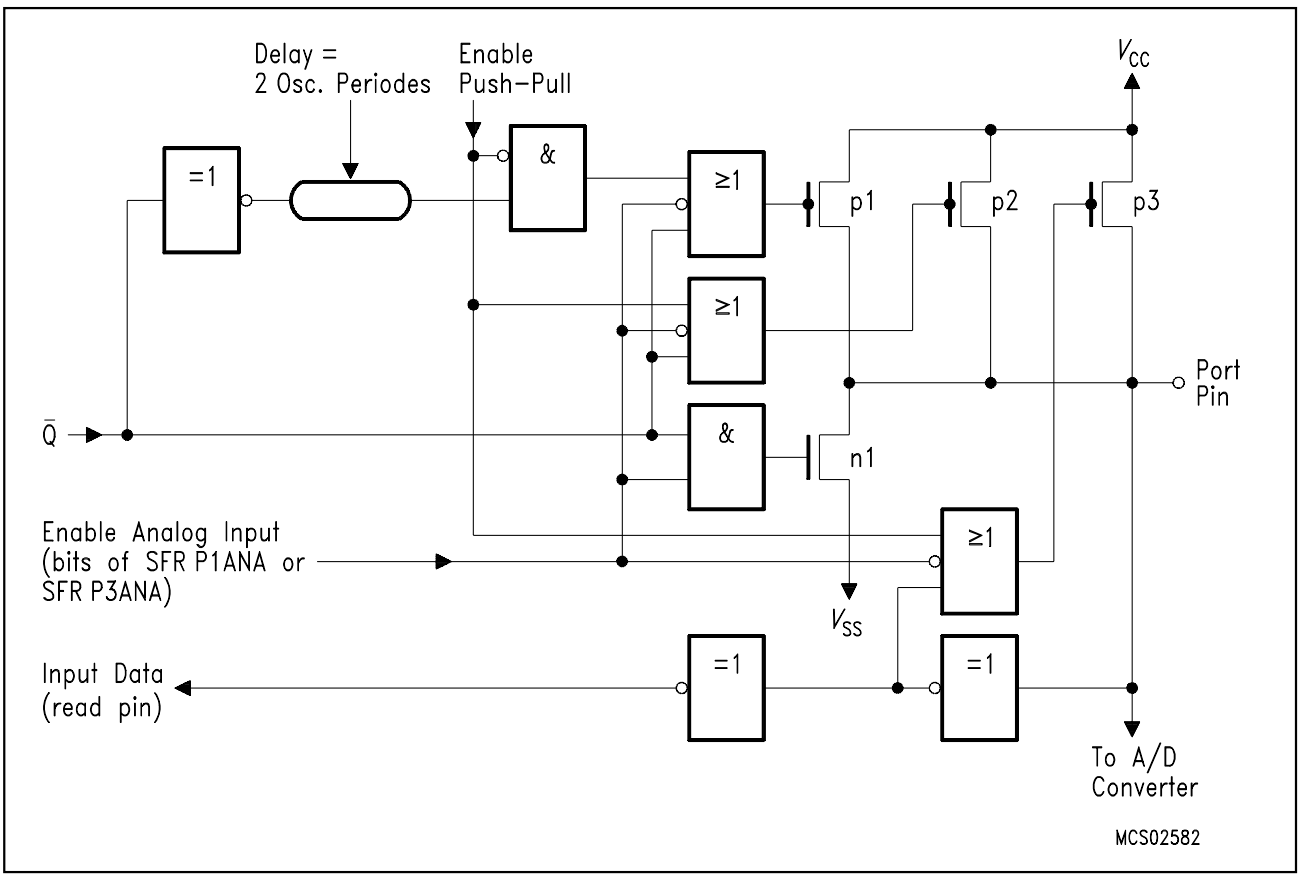


Figure 6-10
Driver Circuit of Type E Port Pins

6.1.4 Port Timing

When executing an instruction that changes the value of a port latch, the new value arrives at the latch during S6P2 of the final cycle of the instruction. However, port latches are only sampled by their output buffers during phase 1 of any clock period (during phase 2 the output buffer holds the value it noticed during the previous phase 1). Consequently, the new value in the port latch will not appear at the output pin until the next phase 1, which will be at S1P1 of the next machine cycle.

When an instruction reads a value from a port pin (e.g. MOV A, P1) the port pin is actually sampled in state 5 phase 1 or phase 2 depending on port and alternate functions. **Figure 6-11** illustrates this port timing. It must be noted that this mechanism of sampling once per machine cycle is also used if a port pin is to detect an "edge", e.g. when used as counter input. In this case an "edge" is detected when the sampled value differs from the value that was sampled the cycle before. Therefore, there must be met certain requirements on the pulse length of signals in order to avoid signal "edges" not being detected. The minimum time period of high and low level is one machine cycle, which guarantees that this logic level is noticed by the port at least once.

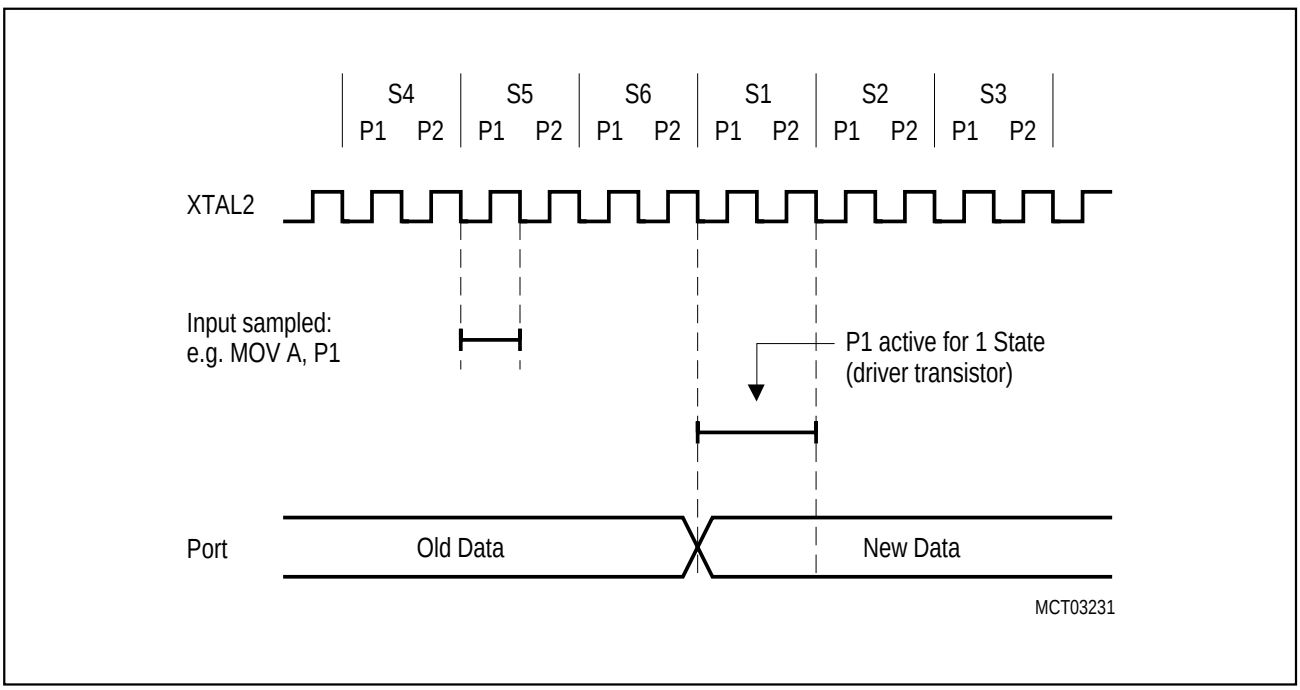


Figure 6-11
Port Timing

6.1.5 Port Loading and Interfacing

The output buffers of ports 2 and 3 can drive TTL inputs directly. The maximum port load which still guarantees correct logic output levels can be looked up in the DC characteristics in the Data Sheet of the C504. The corresponding parameters are V_{OL} and V_{OH}.

The same applies to port 0 output buffers. They do, however, require external pullups to drive floating inputs, except when being used as the address/data bus.

When used as inputs it must be noted that the ports 2 and 3 are not floating but have internal pullup transistors. The driving devices must be capable of sinking a sufficient current if a logic low level shall be applied to the port pin (the parameters I_{TL} and I_{IL} in the DC characteristics specify these currents). Port 0 as well as the input only port 1, however, have floating inputs when used for digital input.

6.1.6 Read-Modify-Write Feature of Ports 2 and 3

Some port-reading instructions read the latch and others read the pin. The instructions reading the latch rather than the pin read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write"- instructions, which are listed in **table 6-3**. If the destination is a port or a port pin, these instructions read the latch rather than the pin. Note that all other instructions which can be used to read a port, exclusively read the port pin. In any case, reading from latch or pin, resp., is performed by reading the SFR P0, P2 and P3; for example, "MOV A, P3" reads the value from port 3 pins, while "ANL P3, #0AAH" reads from the latch, modifies the value and writes it back to the latch.

It is not obvious that the last three instructions in **table 6-3** are read-modify-write instructions, but they are. The reason is that they read the port byte, all 8 bits, modify the addressed bit, then write the complete byte back to the latch.

Table 6-3
"Read-Modify-Write"-Instructions

Instruction	Function
ANL	Logic AND; e.g. ANL P1, A
ORL	Logic OR; e.g. ORL P2, A
XRL	Logic exclusive OR; e.g. XRL P3, A
JBC	Jump if bit is set and clear bit; e.g. JBC P1.1, LABEL
CPL	Complement bit; e.g. CPL P3.0
INC	Increment byte; e.g. INC P4
DEC	Decrement byte; e.g. DEC P5
DJNZ	Decrement and jump if not zero; e.g. DJNZ P3, EL
MOV Px.y,C	Move carry bit to bit y of port x
CLR Px.y	Clear bit y of port x
SETB Px.y	Set bit y of port x

The reason why read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a "1" is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transitor (approx. 0.7 V, i.e. a logic low level!) and interpret it as "0". For example, when modifying a port bit by a SETB or CLR instruction, another bit in this port with the above mentioned configuration might be changed if the value read from the pin were written back to the latch. However, reading the latch rater than the pin will return the correct value of "1".

6.2 Timers/Counters

The C504 contains three 16-bit timers/counters which are useful in many applications for timing and counting.

In "timer" function, the register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the counter rate is 1/12 of the oscillator frequency.

In "counter" function, the register is incremented in response to a 1-to-0 transition (falling edge) at its corresponding external input pin, T0 or T1 (alternate functions of P3.4 and P3.5, resp.). In this function the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

6.2.1 Timer/Counter 0 and 1

Timer / counter 0 and 1 of the C504 are fully compatible with timer / counter 0 and 1 of the C501 and can be used in the same four operating modes:

Mode 0: 8-bit timer/counter with a divide-by-32 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count. The effect is the same as setting TR1 = 0.

External inputs INT0 and INT1 can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Each timer consists of two 8-bit registers (TH0 and TL0 for timer/counter 0, TH1 and TL1 for timer/counter 1) which may be combined to one timer configuration depending on the mode that is established. The functions of the timers are controlled by two special function registers TCON and TMOD.

In the following descriptions the symbols TH0 and TL0 are used to specify the high-byte and the low-byte of timer 0 (TH1 and TL1 for timer 1, respectively). The operating modes are described and shown for timer 0. If not explicitly noted, this applies also to timer 1.

6.2.1.1 Timer/Counter 0 and 1 Registers

Totally six special function registers control the timer/counter 0 and 1 operation :

- TL0/TH0 and TL1/TH1 - counter registers, low and high part
- TCON and TMOD - control and mode select registers

Special Function Register TL0 (Address $8A_H$) **Reset Value : 00_H**
Special Function Register TH0 (Address $8C_H$) **Reset Value : 00_H**
Special Function Register TL1 (Address $8B_H$) **Reset Value : 00_H**
Special Function Register TH1 (Address $8D_H$) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$8A_H$	.7	.6	.5	.4	.3	.2	.1	.0	TL0
$8C_H$	.7	.6	.5	.4	.3	.2	.1	.0	TH0
$8B_H$	.7	.6	.5	.4	.3	.2	.1	.0	TL1
$8D_H$	.7	.6	.5	.4	.3	.2	.1	.0	TH1

Bit	Function	
TLx.7-0 x=0-1	Timer/counter 0/1 low register	
	Operating Mode	**Description**
	0	"TLx" holds the 5-bit prescaler value.
	1	"TLx" holds the lower 8-bit part of the 16-bit timer/counter value.
	2	"TLx" holds the 8-bit timer/counter value.
	3	TL0 holds the 8-bit timer/counter value; TL1 is not used.
THx.7-0 x=0-1	Timer/counter 0/1 high register	
	Operating Mode	**Description**
	0	"THx" holds the 8-bit timer/counter value.
	1	"THx" holds the higher 8-bit part of the 16-bit timer/counter value
	2	"THx" holds the 8-bit reload value.
	3	TH0 holds the 8-bit timer value; TH1 is not used.

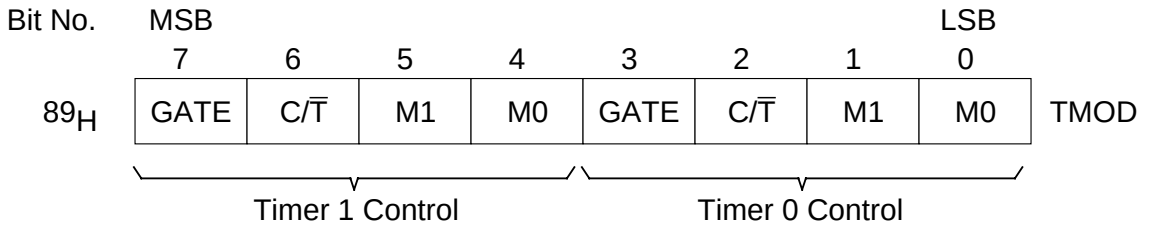
Special Function Register TCON (Address 88_H) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
	$8F_H$	$8E_H$	$8D_H$	$8C_H$	$8B_H$	$8A_H$	89_H	88_H	
88_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	TCON

The shaded bits are not used in controlling timer/counter 0 and 1.

Bit	Function
TR0	Timer 0 run control bit Set/cleared by software to turn timer/counter 0 ON/OFF.
TF0	Timer 0 overflow flag Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	Timer 1 run control bit Set/cleared by software to turn timer/counter 1 ON/OFF.
TF1	Timer 1 overflow flag Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.

Special Function Register TMOD (Address 89_H) **Reset Value : 00_H**



Bit	Function
GATE	Gating control When set, timer/counter "x" is enabled only while "INT x" pin is high and "TRx" control bit is set. When cleared timer "x" is enabled whenever "TRx" control bit is set.
C/$\overline{T}$	Counter or timer select bit Set for counter operation (input from "Tx" input pin). Cleared for timer operation (input from internal system clock).
M1 M0	Mode select bits

M1	M0	Function
0	0	8-bit timer/counter: "THx" operates as 8-bit timer/counter "TLx" serves as 5-bit prescaler
0	1	16-bit timer/counter. "THx" and "TLx" are cascaded; there is no prescaler
1	0	8-bit auto-reload timer/counter. "THx" holds a value which is to be reloaded into "TLx" each time it overflows
1	1	Timer 0 : TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer only controlled by timer 1 control bits. Timer 1 : Timer/counter 1 stops

6.2.1.2 Mode 0

Putting either timer/counter 0,1 into mode 0 configures it as an 8-bit timer/counter with a divide-by-32 prescaler. **Figure 6-12** shows the mode 0 operation.

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1's to all 0's, it sets the timer overflow flag TF0. The overflow flag TF0 then can be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or INT0 = 1 (setting Gate = 1 allows the timer to be controlled by external input INT0, to facilitate pulse width measurements). TR0 is a control bit in the special function register TCON; Gate is in TMOD.

The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 0 operation is the same for timer 0 as for timer 1. Substitute TR0, TF0, TH0, TL0 and INT0 for the corresponding timer 1 signals in **figure 6-12**. There are two different gate bits, one for timer 1 (TMOD.7) and one for timer 0 (TMOD.3).

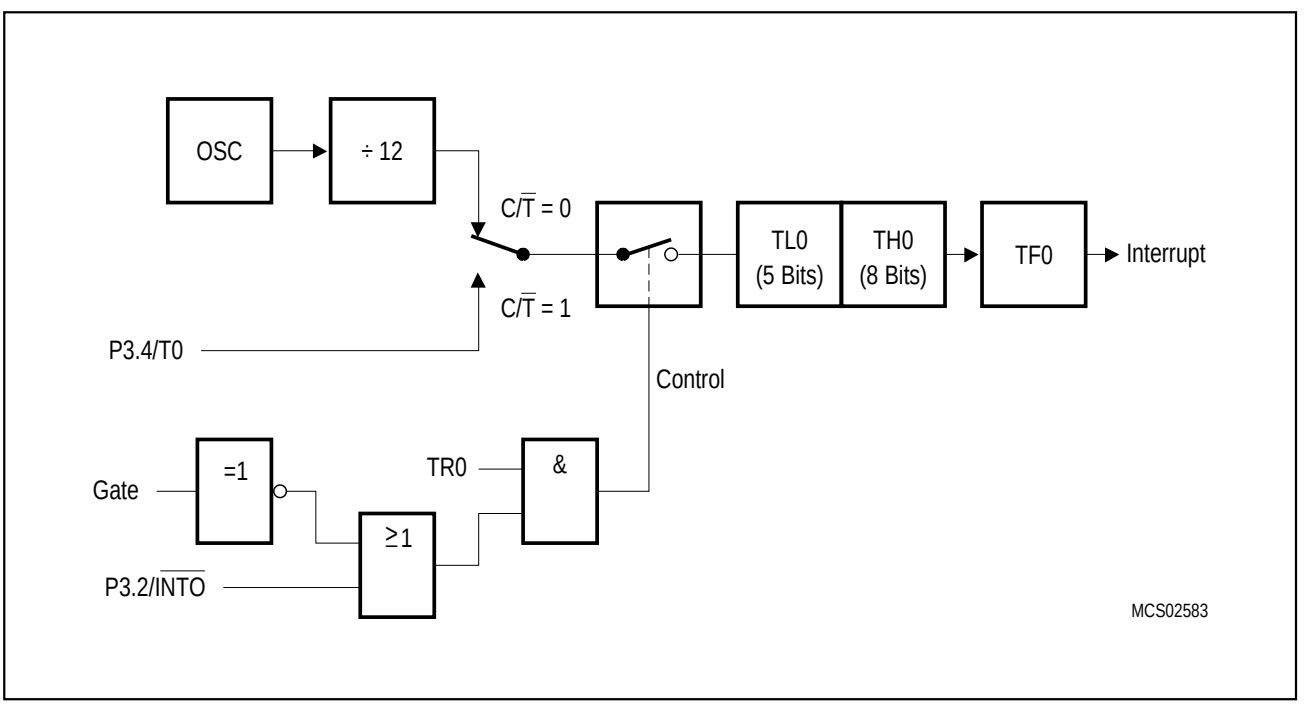


Figure 6-12
Timer/Counter 0, Mode 0: 13-Bit Timer/Counter

6.2.1.3 Mode 1

Mode 1 is the same as mode 0, except that the timer register is running with all 16 bits. Mode 1 is shown in **figure 6-13**.

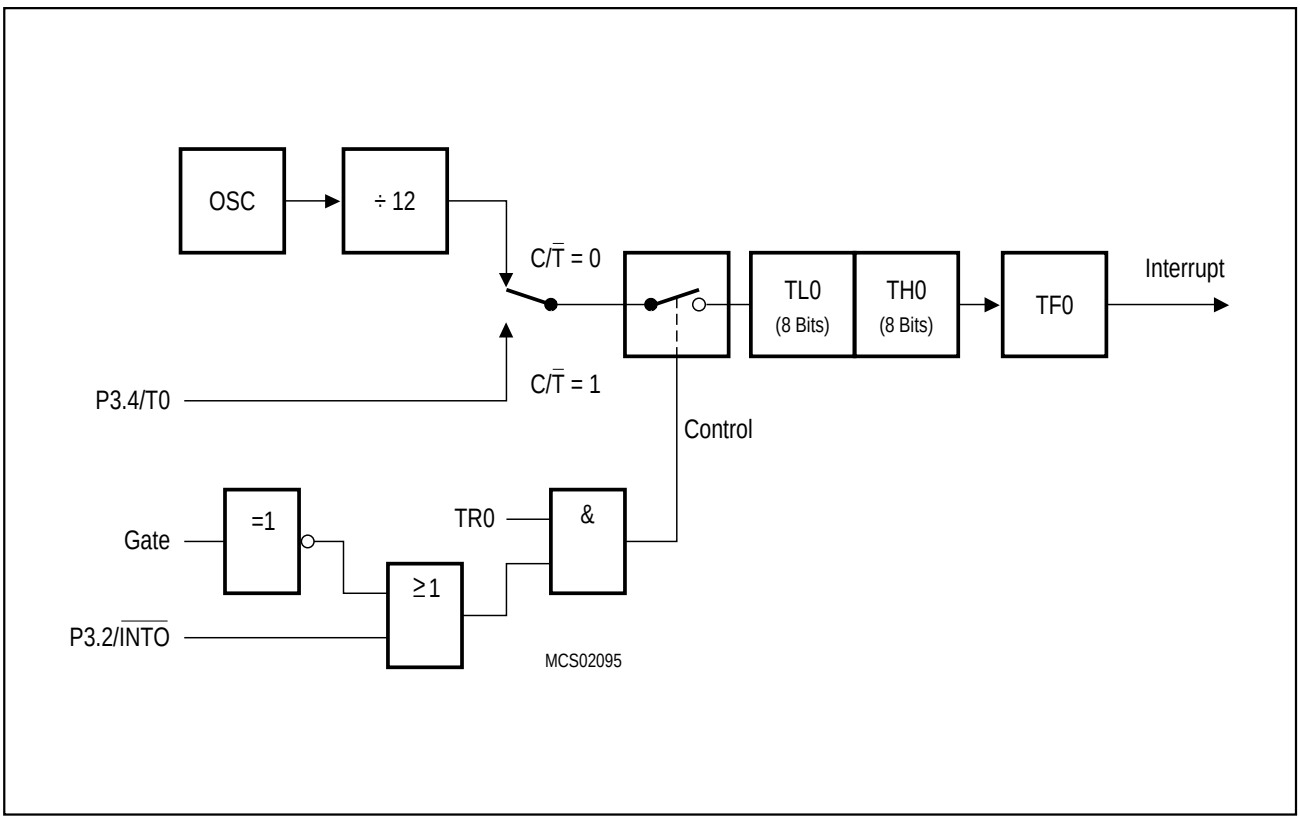


Figure 6-13
Timer/Counter 0, Mode 1: 16-Bit Timer/Counter

6.2.1.4 Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload, as shown in **figure 6-14**. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

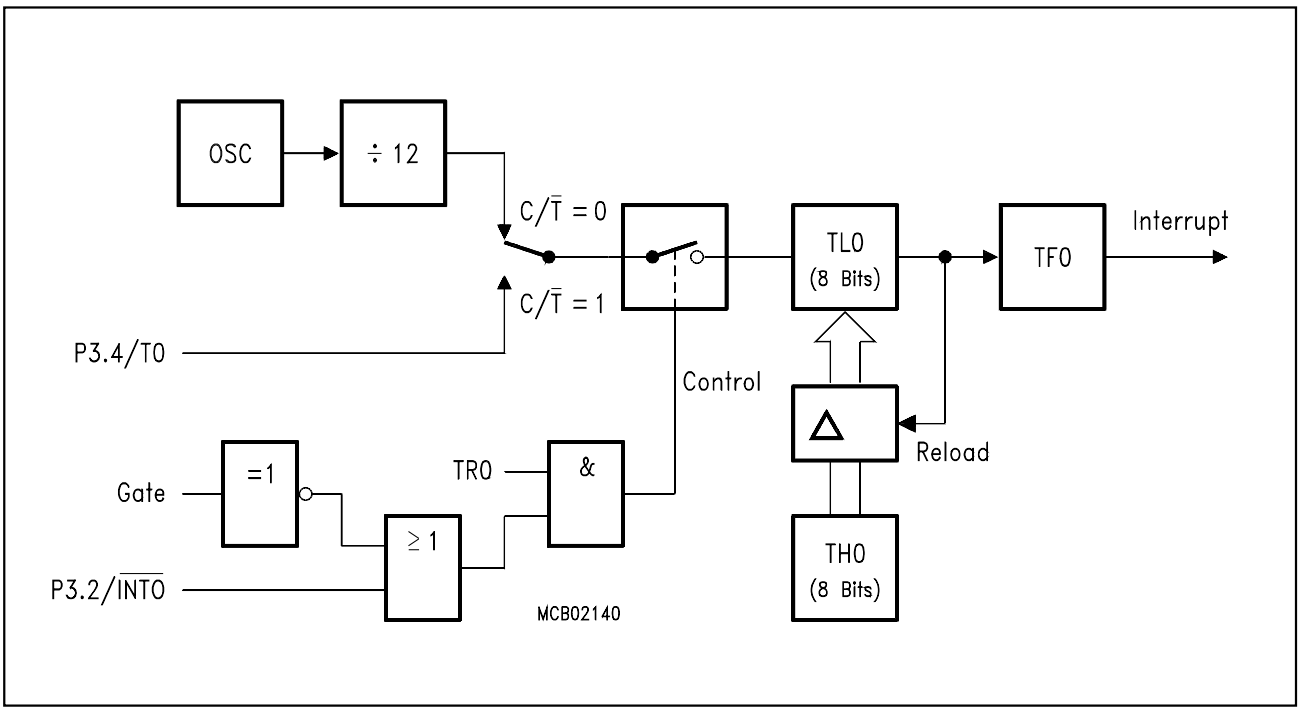


Figure 6-14
Timer/Counter 0,1, Mode 2: 8-Bit Timer/Counter with Auto-Reload

6.2.1.5 Mode 3

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in mode 3 simply holds its count. The effect is the same as setting TR1=0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. The logic for mode 3 on timer 0 is shown in **figure 6-15**. TL0 uses the timer 0 control bits: C/T, Gate, TR0, INT0 and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial channel as a baud rate generator, or in fact, in any application not requiring an interrupt from timer 1 itself.

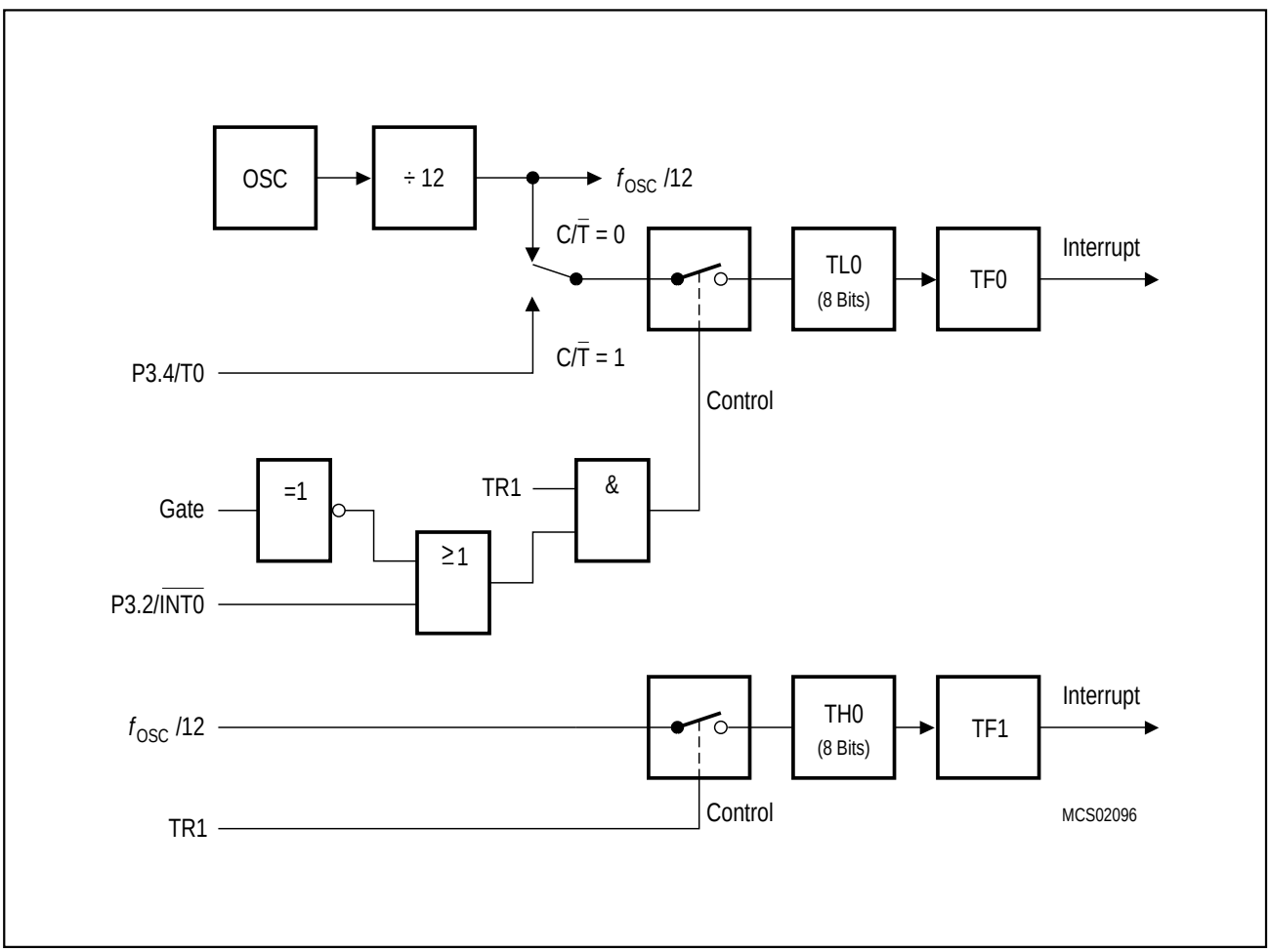


Figure 6-15
Timer/Counter 0, Mode 3: Two 8-Bit Timers/Counters

6.2.2 Timer/Counter 2

Timer 2 is a 16-bit timer / counter which can operate as timer or counter. It has three operating modes:

- 16-bit auto-reload mode (up or down counting)
- 16-bit capture mode
- Baudrate generator (see 6.4.3 “Baud Rates“)

The modes are selected by bits in the SFR T2CON as shown in **table 6-4**:

Table 6-4
Timer/Counter 2 - Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	Mode
0	0	1	16-bit auto-reload
0	1	1	16-bit capture
1	X	1	Baud rate generator
X	X	0	(OFF)

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2 (P1.0). In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

6.2.2.1 Timer/Counter 2 Registers

Totally six special function registers control the timer/counter 0 and 1 operation :

- TL2/TH2 and RC2L/RC2H - counter and reload/capture registers, low and high part
- T2CON and T2MOD - control and mode select registers

Special Function Register TL2 (Address CC_H) **Reset Value : 00_H**
Special Function Register TH2 (Address CD_H) **Reset Value : 00_H**
Special Function Register RC2L (Address CA_H) **Reset Value : 00_H**
Special Function Register RC2H (Address CB_H) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
CC_H	.7	.6	.5	.4	.3	.2	.1	.0	TL2
CD_H	.7	.6	.5	.4	.3	.2	.1	.0	TH2
CA_H	.7	.6	.5	.4	.3	.2	.1	.0	RC2L
CB_H	.7	.6	.5	.4	.3	.2	.1	.0	RC2H

Bit	Function
TL2.7-0	Timer 2 value low byte The TL2 register holds the 8-bit low part of the 16-bit timer 2 count value.
TH2.7-0	Timer 2 value high byte The TH2 register holds the 8-bit high part of the 16-bit timer 2 count value.
RC2L.7-0	Reload / capture timer 2 register low byte RC2L holds the 8-bit low byte of the 16-bit timer 2 reload or capture value.
RC2H.7-0	Reload / capture timer 2 register high byte RC2H holds the 8-bit high byte of the 16-bit timer 2 reload or capture value.

Special Function Register T2CON (Address $C8_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	7	6	5	4	3	2	1	0	
	CF_H	CE_H	CD_H	CC_H	CB_H	CA_H	$C9_H$	$C8_H$	
$C8_H$	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	T2CON

Bit	Function
TF2	Timer 2 Overflow Flag Set by a timer 2 overflow. Must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 External Flag Set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1, SFR T2MOD)
RCLK	Receive Clock Enable When set, causes the serial port to use timer 2 overflow pulses for its receive clock in serial port modes 1 and 3. RCLK = 0 causes timer 1 overflows to be used for the receive clock.
TCLK	Transmit Clock Enable When set, causes the serial port to use timer 2 overflow pulses for its transmit clock in serial port modes 1 and 3. TCLK = 0 causes timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 External Enable When set, allows a capture or reload to occur as a result of a negative transition on pin T2EX (P1.1) if timer 2 is not being used to clock the serial port. EXEN2 = 0 causes timer 2 to ignore events at T2EX.
TR2	Start / Stop Control for Timer 2 TR2 = 1 starts timer 2.
C/$\overline{T2}$	Timer or Counter Select for Timer 2 C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture /Reload Select CP/$\overline{RL2}$ = 1 causes captures to occur an negative transitions at pin T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when timer 2 overflows or negative transitions occur at pin T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on timer 2 overflow.

Special Function Register T2MOD (Address $C9_H$) **Reset Value : XXXX XXX0_B**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$C9_H$	–	–	–	–	–	–	–	DCEN	T2MOD

Bit	Function
–	Not implemented, reserved for future use.
DCEN	When set, this bit allows timer 2 to be configured as an up/down counter.

6.2.2.1 Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by a bit named DCEN (Down Counter Enable, SFR T2MOD, $0C9_H$). When DCEN is set, timer 2 can count up or down depending on the value of pin T2EX (P1.1).

Figure 6-16 shows timer 2 automatically counting up when DCEN = 0. In this mode there are two options selectable by bit EXEN2 in SFR T2CON.

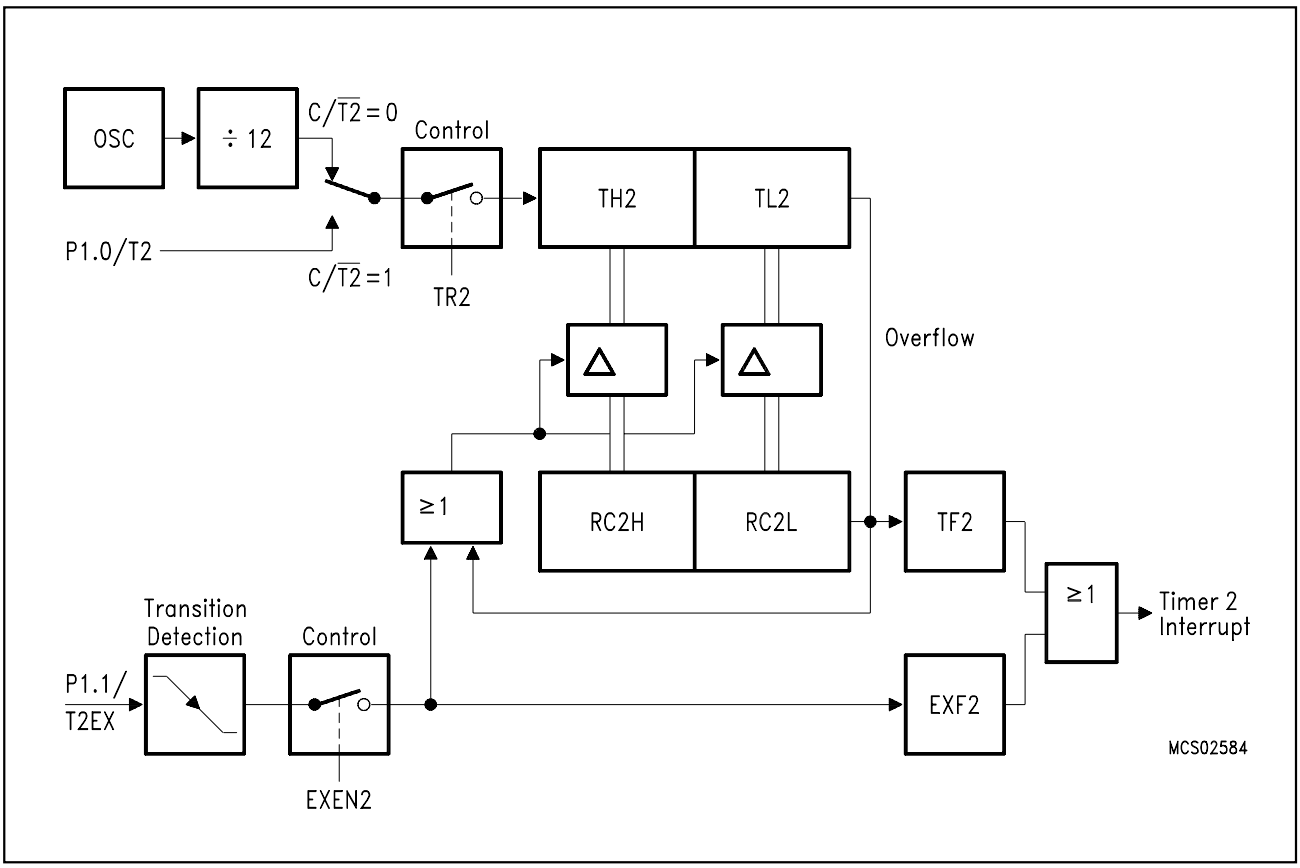


Figure 6-16
Timer 2 Auto-Reload Mode (DCEN = 0)

If EXEN2 = 0, timer 2 counts up to $FFFF_H$ and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RC2H and RC2L. The values in RC2H and RC2L are preset by software.

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at the external input T2EX (P1.1). This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an timer 2 interrupt if enabled.

Setting the DCEN bit enables timer 2 to count up or down as shown in **figure 6-17**. In this mode the T2EX pin controls the direction of count.

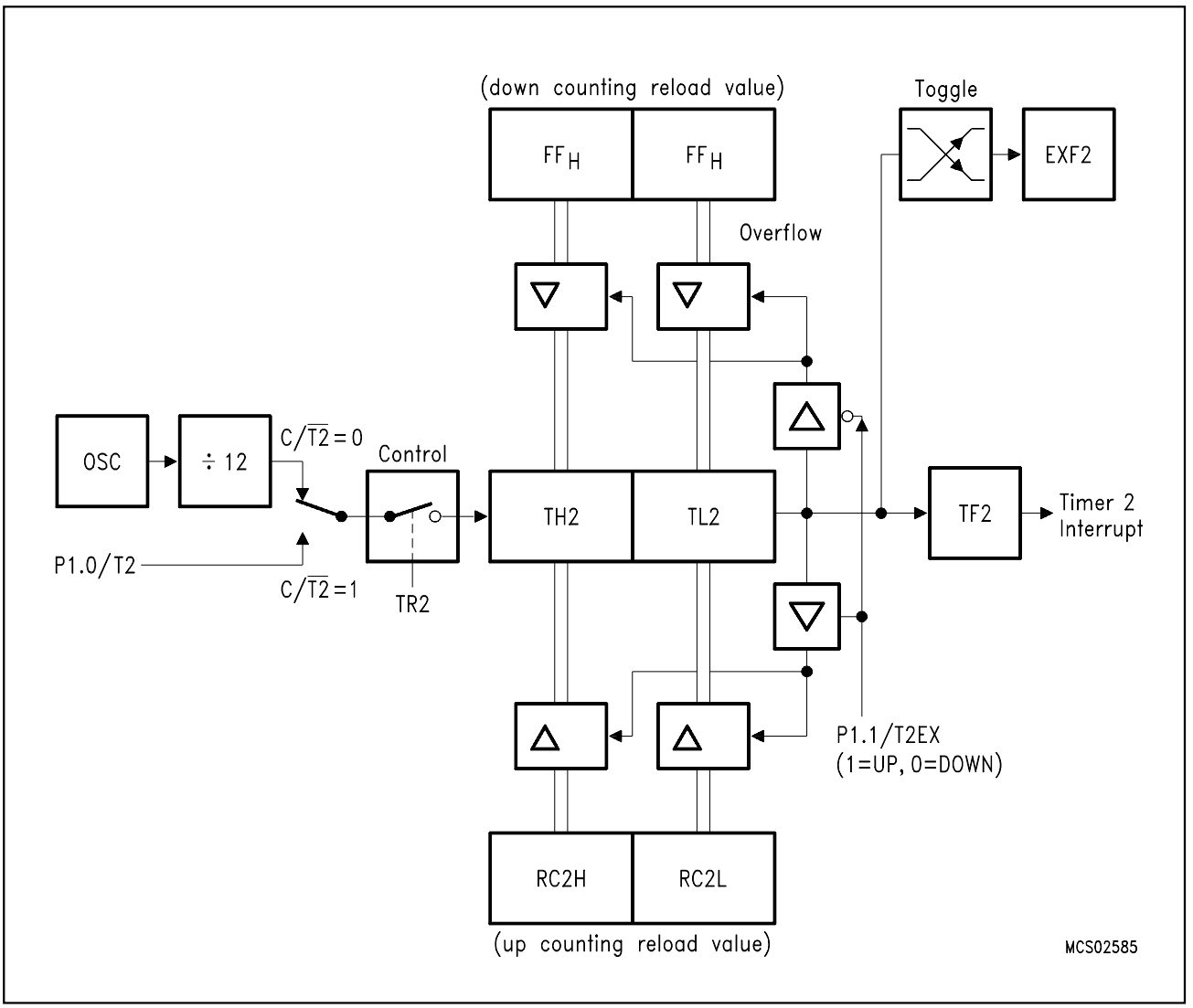


Figure 6-17
Timer 2 Auto-Reload Mode (DCEN = 1)

A logic 1 at T2EX makes timer 2 count up. The timer will overflow at $FFFF_H$ and set the TF2 bit. This overflow also causes the 16-bit value in RC2H and RC2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes timer 2 count down. Now the timer underflows when TH2 and TL2 equal the values stored in RC2H and RC2L. The underflow sets the TF2 bit and causes $FFFF_H$ to be reloaded into the timer registers. The EXF2 bit toggles whenever timer 2 overflows or underflows. This bit can be used as a 17th bit of resolution if desired. In this operating mode, EXF2 does not flag an interrupt.

Note: P1.1/T2EX is sampled during S5P2 of every machine cycle. The next increment/decrement of timer 2 will be done during S3P1 in the next cycle.

6.2.2.2 Capture

In the capture mode there are two options selected by bit EXEN2 in SFR T2CON.

If EXEN2 = 0, timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in SFR T2CON. This bit can be used to generate an interrupt.

If EXEN2 = 1, timer 2 still does the above, but with added feature that a 1-to-0 transition at external input T2EX causes the current value in TH2 and TL2 to be captured into RC2H and RC2L, respectively. In addition, the transition at T2EX causes bit EXF2 in SFR T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in **figure 6-18**.

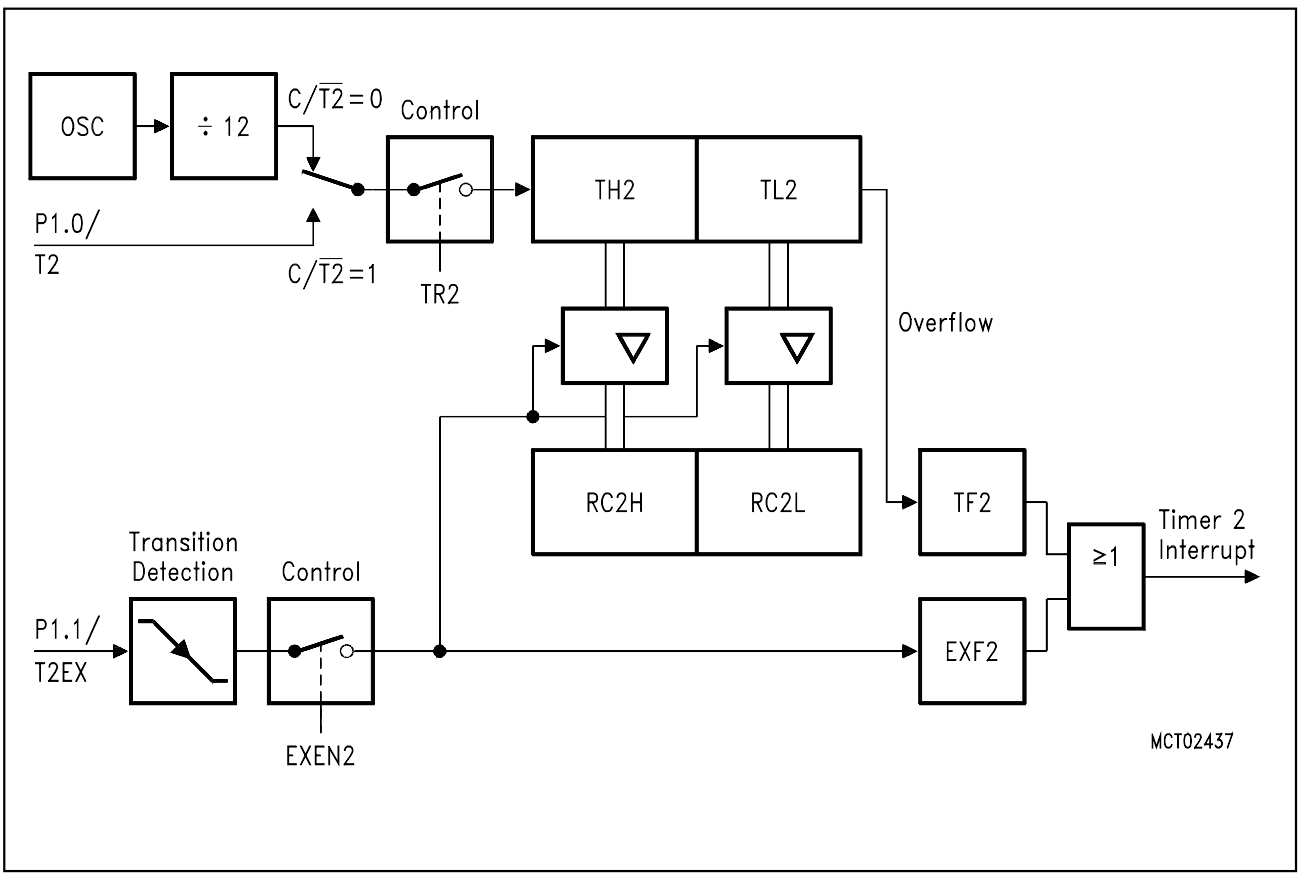


Figure 6-18
Timer 2 in Capture Mode

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1 in SFR T2CON. It will be described in conjunction with the serial port.

6.3 Capture / Compare Unit (CCU)

The Capture / Compare Unit (CCU) of the C504 has been designed for applications which have a demand for digital signal generation and/or event capturing (e.g. pulse width modulation, pulse width measuring). It consists of a 16-bit 3-channel capture/compare unit (CAPCOM) and a 10-bit 1-channel compare unit (COMP).

In compare mode, the CAPCOM unit provides two output signals per channel, which can have inverted signal polarity and non-overlapping pulse transitions. The COMP unit can generate a single PWM output signal and is further used to modulate the CAPCOM output signals. For motor control applications, both units (CAPCOM and COMP) may generate versatile multichannel PWM signals. For brushless DC motors dedicated control modes are supported which are either controlled by software or by hardware (hall sensors).

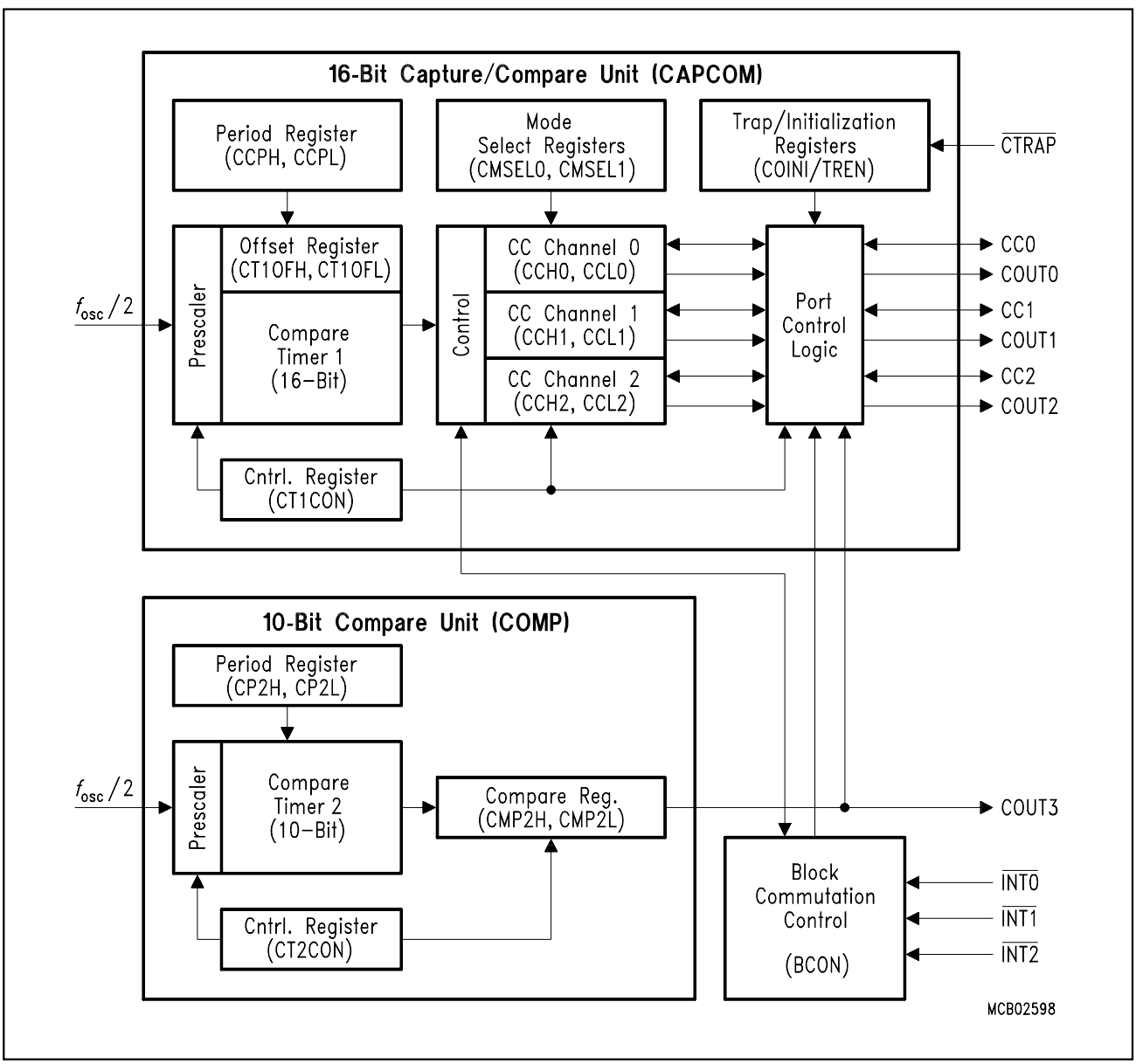


Figure 6-18
Block Diagram of the Capture/Compare Unit CCU

6.3.1 General Capture/Compare Unit Operation

The compare timer 1 and 2 are free running, processor clock coupled 16-bit / 10-bit timers which have each a count rate with a maximum of $f_{OSC}/2$ up to $f_{OSC}/256$. The compare timer operations with its possible compare output signal waveforms are shown in **figure 6-19**.

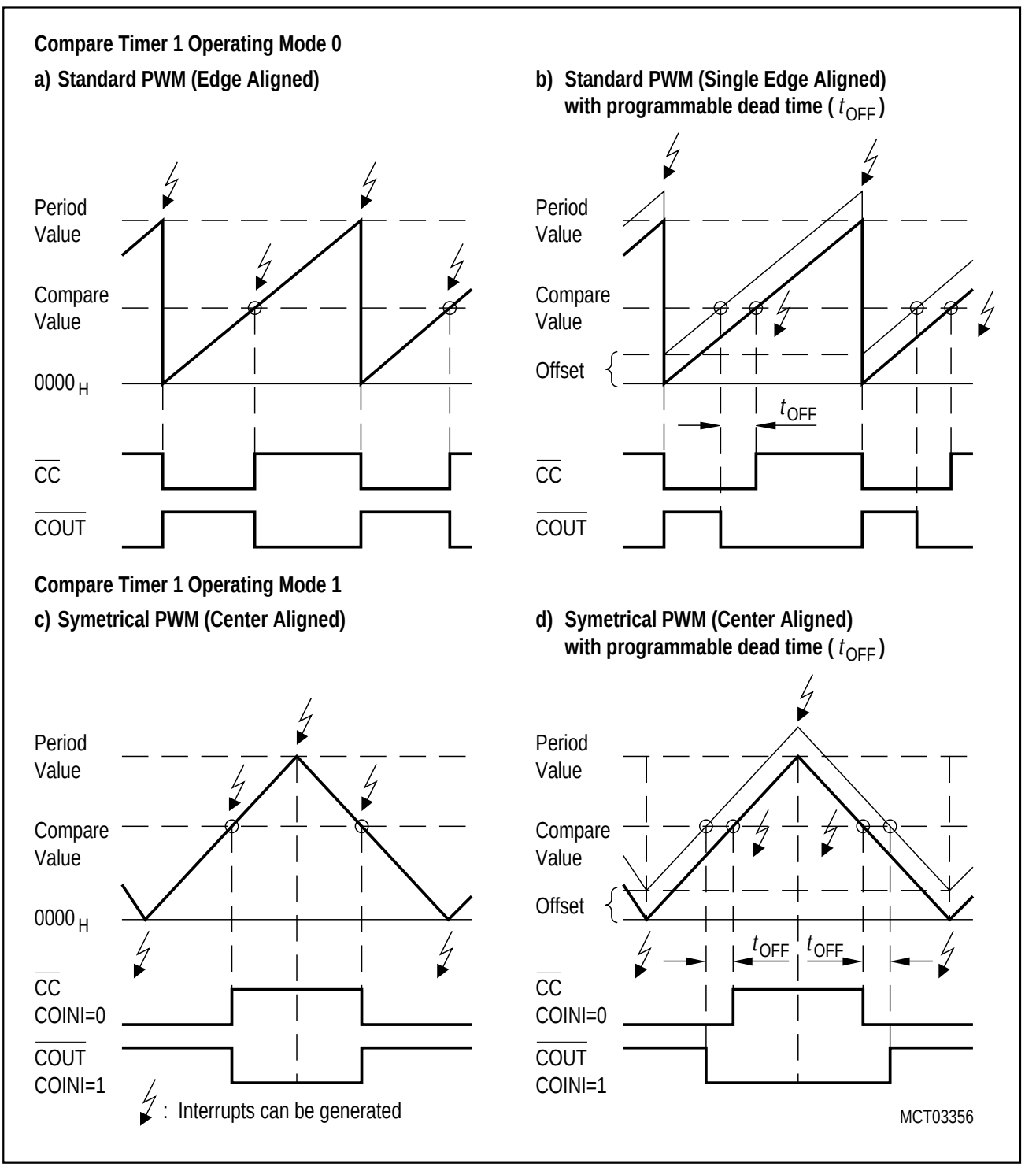


Figure 6-19
Basic Operating Modes of the CAPCOM Unit

Both compare timers start counting upwards from 0000_H up to a count value stored in the period registers. If the value stored in the period register is reached, they are reset (operating mode 0, both compare timers) or the count direction is changed from up-counting to down-counting (operating mode 1, only compare timer 1). Using operating mode 0, edge aligned PWM signals can be generated. Using operating mode 1, center aligned PWM signals can be generated. Compare timer 1 can be programmed for both operating modes while compare timer 2 always works in operating mode 0 with one output signal COUT3. **Figure 6-19 a)** and **c)** shows the function of these basic operating modes.

Compare timer 1 has an additional 16-bit offset register, which consists of the high byte stored in CT1OFH and the low byte stored in CT1OFL. If the value stored in CT1OFF is 0, the compare timer operates as shown in **figure 6-19 a)** and **c)**. If the value stored in CT1OFF is not zero, the compare timer operates as shown in **figure 6-19 b)** and **d)**. In operating mode 0, compare timer 1 is always reset after its value has been equal to the value stored in period register. In operating mode 1, the count direction of the compare timer is changed from up- to down-counting when its value has reached the value stored in the period register. The count direction is changed from down- to up-counting when the compare timer value has reached 0000_H. Generally, the compare outputs CCx are always assigned to a match condition with the compare timer value directly while the compare outputs COUTx are assigned to a match condition with the compare timer value plus the offset value. Therefore, signal waveforms with non-overlapping signal transitions as shown in **figure 6-19 b)** and **d)** can be generated.
Further, the initial logic output level of the CAPCOM channel outputs when used in compare mode can be selected. This allows to generate waveforms with inverting signal polarities.
In capture mode of the CAPCOM unit, the value of compare timer 1 is stored in the capture registers if a signal transition occurs at pins CCx.

The compare unit COMP is a 10-bit compare unit which can be used to generate a pulse width modulated signal. This PWM output signal drives the output pin COUT3. In burst mode and in the PWM modes the output of the COMP unit can be switched to the COUTx outputs.

The block commutation control logic allows to generate versatile multi-channel PWM output signals. In one of theses modes, the block commutation mode, signal transitions at the three external interrupt inputs are used to trigger the PWM signal generation logic. Depending on these signal transitions, the six I/O lines of the CAPCOM unit, which are decoupled in block commutation mode from the three capture/compare channels, are driven as static or PWM modulated outputs. CAPCOM channel 0 can be used in block commutation mode for a capture operation (speed measurement) which is triggered by each transition at the external interrupt inputs.
Further, the multi-channel PWM mode signal generation can be also triggered by the period of compare timer 1. These operating modes are referenced as multi-channel PWM modes.

Using the $\overline{\text{CTRAP}}$ input signal of the C504, the compare outputs can be put immediately into their passive state (defined in COINI register) and released again.

The CCU unit has four main interrupt sources with their specific interrupt vectors. Interrupts can be generated at the compare timer 1 period match or count-change events, at the compare timer 2 period match event, at a CAPCOM compare match or capture event, and at a CAPCOM emergency event. An emergency event occurs if an active $\overline{\text{CTRAP}}$ signal is detected or if an error condition in block commutation mode is detected. All interrupt sources can be enabled/disabled individually.

6.3.2 CAPCOM Unit Operation

6.3.2.1 CAPCOM Unit Clocking Scheme

The CAPCOM unit is basically controlled by the 16-bit compare timer 1. Compare timer 1 is the timing base for all compare and capture capabilities of the CAPCOM unit. The input clock for compare timer 1 is directly coupled to the system clock of the C504. Its frequency can be selected via three bits of the CT1CON register in a range of $f_{OSC}/2$ up to $f_{OSC}/256$.

For the understanding of the following timing diagrams, **figure 6-20** shows the internal clocking scheme of the CAPCOM unit. The internal input clock of the CAPCOM unit is a symmetrical clock with 50% duty cycle. The clock transitions (edges) of the CAPCOM internal input clock are used for different actions: at clock edge 1 the compare timer 1 is clocked to the next count value, and with clock edge 2 the compare outputs CCx and COUTx are toggled/set to the new logic level if required.

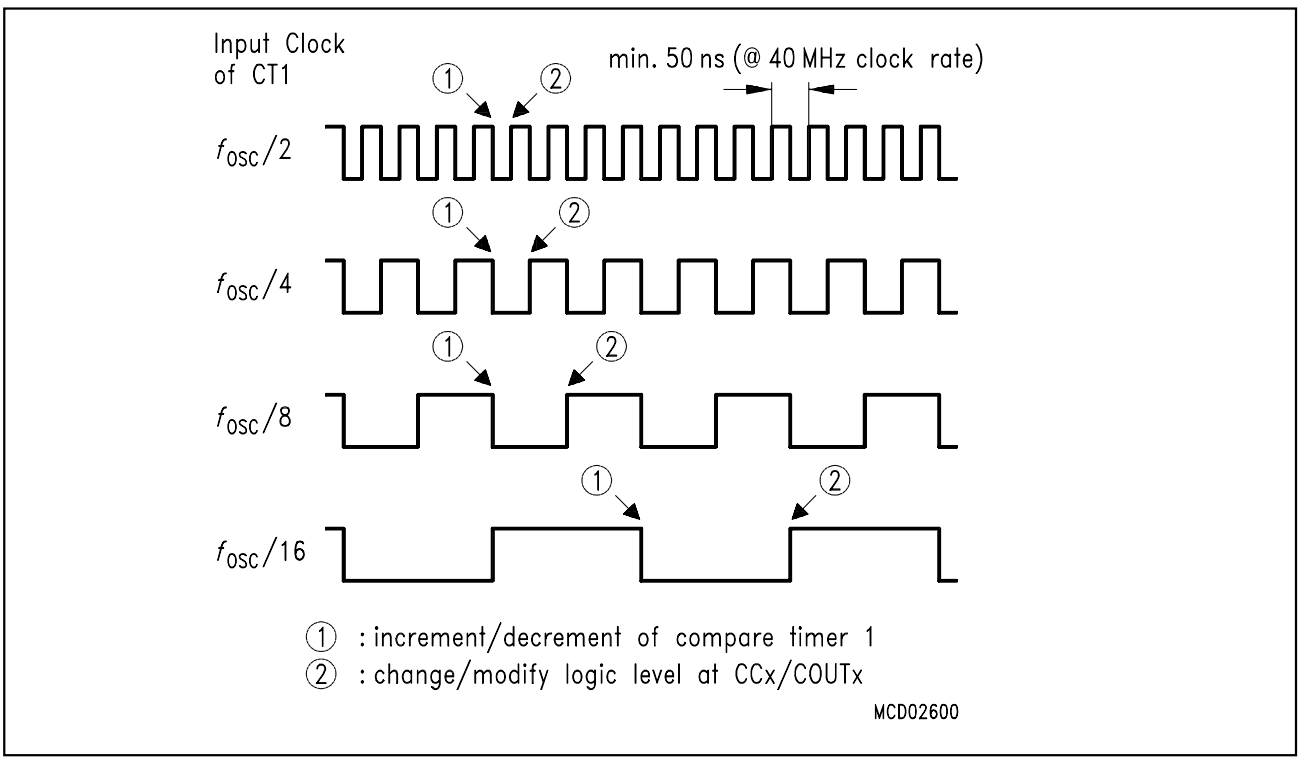


Figure 6-20
CAPCOM Unit Clocking Scheme

Generally, the CAPCOM clocking scheme shown above is also valid for the COMP (compare timer 2) unit.

6.3.2.2 CAPCOM Unit Operating Mode 0

Figure 6-21 shows the CAPCOM unit timing in operating mode 0 in detail.

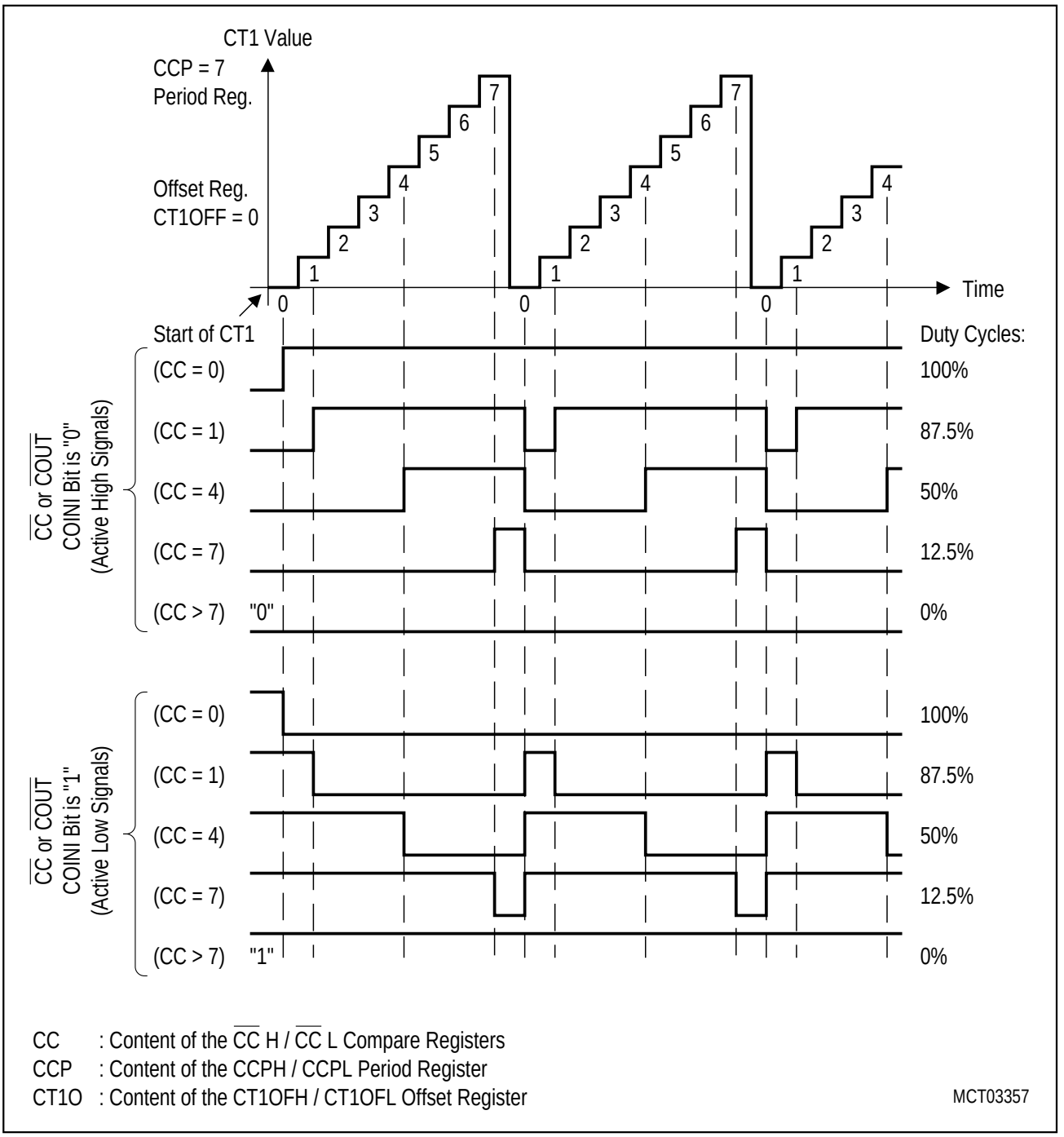


Figure 6-21
Compare Timer 1 Mode 0

In the example above compare timer 1 counts from 0000_H up to 0007_H (value stored in CCPH/ CCPL). The offset registers CT1OFH/CT1OFL have a value of 0000_H. If programmed in compare mode, two output signals are assigned to the related CAPCOM channel x : CCx and COUTx. The mode select bits in the SFRs CMSEL0 and CMSEL1 define which of these two outputs will be

controlled by the CAPCOM channel. In **figure 6-21** only the CCx signal is shown, but the same or the inverted waveform can be generated at the COUTx outputs.

After reset all CCx/COUTx pins are at high level, driven by a weak pullup. With the programming of the CMSEL1 or CMSEL0 registers, all affected compare outputs are switched to push-pull mode and start driving an initial level which is defined by the bits in SFR COINI. In **figure 6-21** the upper five waveforms are assigned to a CCx pin with the appropriate bit in COINI cleared while the lower five waveforms are assigned to a CCx pin with the appropriate bit in COINI set.

When the count value of the compare timer 1 is incremented and the new value matches with the value stored in the corresponding compare register, the related compare output changes its logic state. When the compare timer is reset to 0000_H the related compare output changes its logic state again. With the scheme shown in **figure 6-21** output waveforms with duty cycles between 0% and 100% can be generated. For a compare register value of 0000_H the output will remain at high level (COINI bit = 0) or low level (COINI bit = 1) representing a duty cycle of 100%. If the value stored in the compare register is higher than the value of the period register, a low level (COINI bit = 0) or high level (COINI bit = 1) corresponds to a duty cycle of 0%.

Figure 6-22 shows the waveform generation in operating mode 0 when the offset register has a value which is not equal 0000_H (example: CT1OFH/CT1OFL = 0002_H). Using compare timer 1 with an offset value not equal 0 is used to generate single edge aligned signals with a constant delay between one of the two signal transitions.

Compare timer 1 always counts from 0000_H up to the value stored in CCP, also if the value in the offset register is not equal 0. With reset (count value 0000_H) of the compare timer 1 the CCx and COUTx will always change their logic state. During the up-counting phase CCx will change the logic state when the compare timer value is equal to the compare register value and COUTx will change the logic state when the compare timer value plus the offset value matches the value stored in the compare register.

In **figure 6-22** the waveforms **a)** and **b)** show an example for a waveform of two signals with a constant delay of their rising edge. A compare register value of 3 is assumed. Using inverted signal polarity (SFR COINI), signal **c)** can be generated at COUTx. If the value in the offset register plus the value of the period register is less than or equal to the value stored in the compare register, a static “1“ or a static “0“ (depending on COINI content) will be generated at COUTx (see **figure 6-22 d)** and **e)**). Therefore, CCx will also stay at a static level if the compare register value is greater than the value stored in the period register.

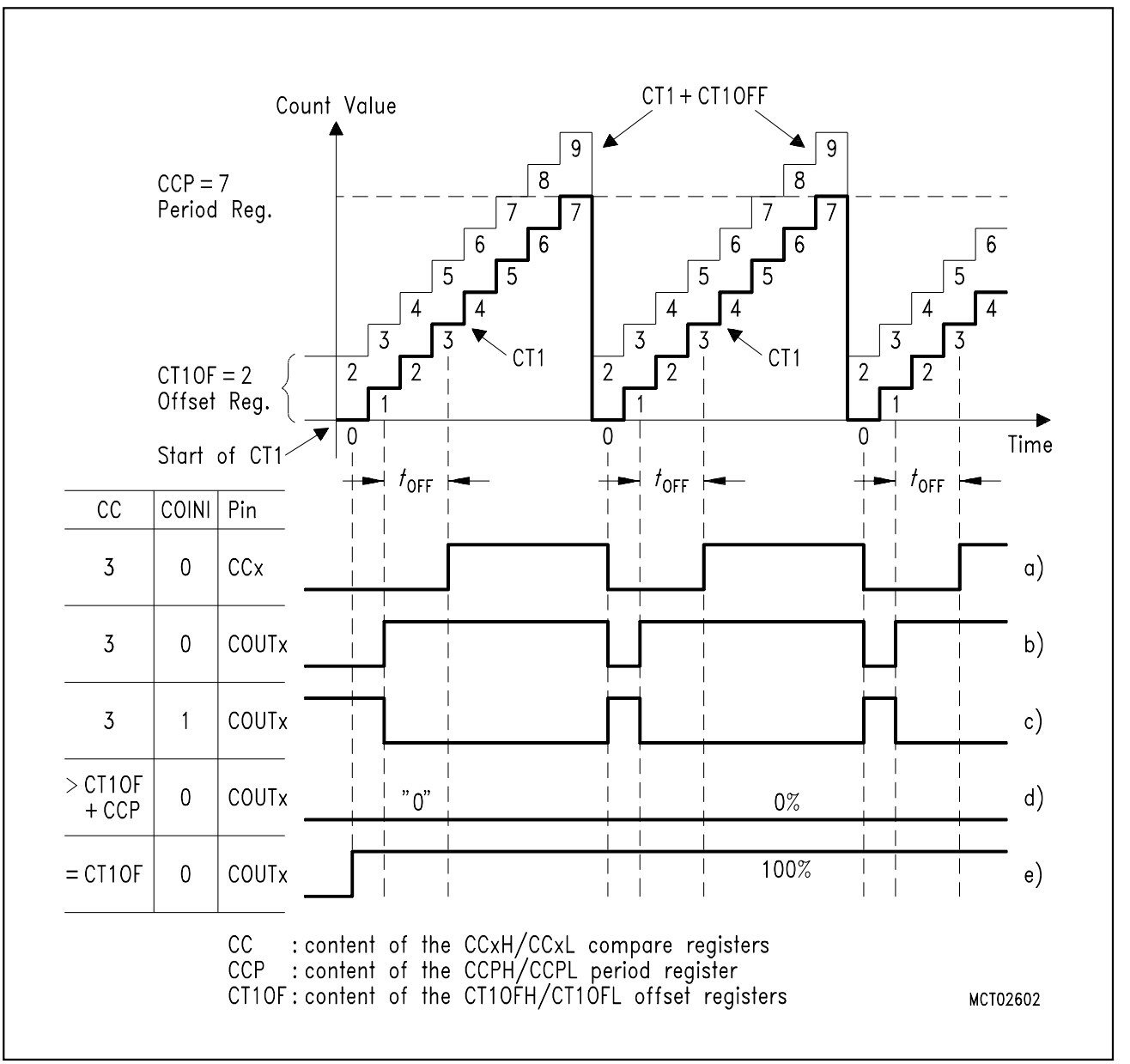


Figure 6-22
Compare Timer 1 with Offset not equal 0 - Mode 0

6.3.2.3 CAPCOM Unit Operating Mode 1

Using compare timer 1 in operating mode 1, two symmetric output signals with constant dead time t_{OFF} at each signal transition can be generated per channel. **Figure 6-23** shows the operating mode 1 timing in detail.

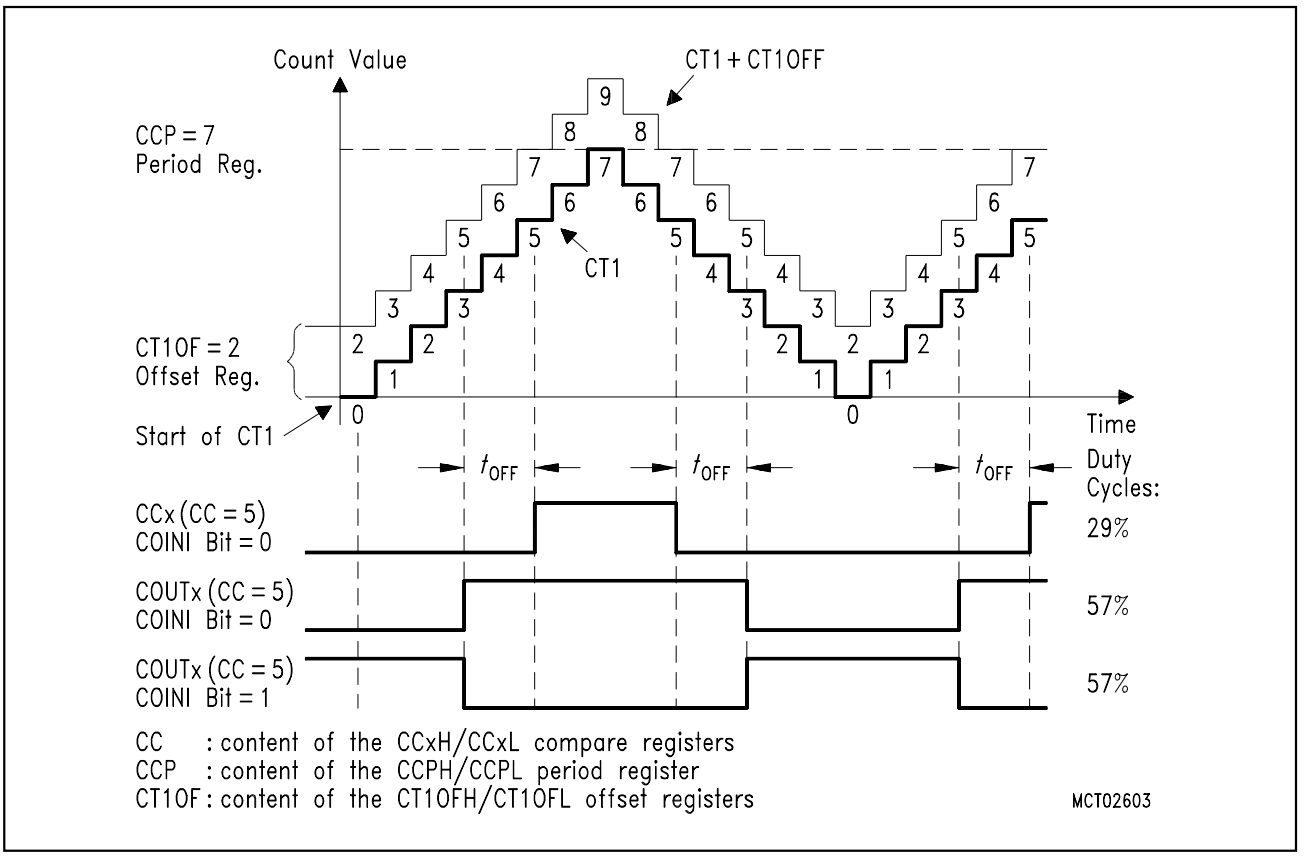


Figure 6-23
Compare Timer 1 with Offset # 0 (Dead Time) - Mode 1

In the example above compare timer 1 counts from 0000_H up to 0007_H (value stored in period register CCPH/CCPL) and then counts down again to 0000_H. The maximum and minimum (0000_H) values of the compare timer 1 occur always once in the count value sequence. In the example shown in **figure 6-23**, the offset registers have a value of 0002_H.

With the programming of the CMSEL1 or CMSEL0 registers, all affected compare outputs are switched to push-pull mode and start driving an initial level which is defined by the bits in SFR COINI.

Equal to operating mode 0, two compare output signals are assigned to the related CAPCOM channel: CCx and COUTx. The compare outputs CCx change their state if a match of compare timer 1 content and the corresponding compare register occurs. The compare outputs COUTx change their state when a match of compare timer 1 content plus the value stored in the offset registers and the corresponding compare register has occurred. If the value in the offset register plus the value of the period register is less than or equal to the value stored in the compare register, a static “1“ or a static “0“ (depending on COINI content) will be generated at COUTx. In the same way, CCx will also stay at a static level is the compare register value is greater than the value stored in the period register.

6.3.2.4 CAPCOM Unit Timing Relationships

Depending on the operating mode of the compare timer 1, compare output signals can be generated with a maximum period and resolution as shown in **figure 6-24.** This example also demonstrates the reloading of the compare and period registers which occurs when compare timer 1 reaches the count value 0000_H.

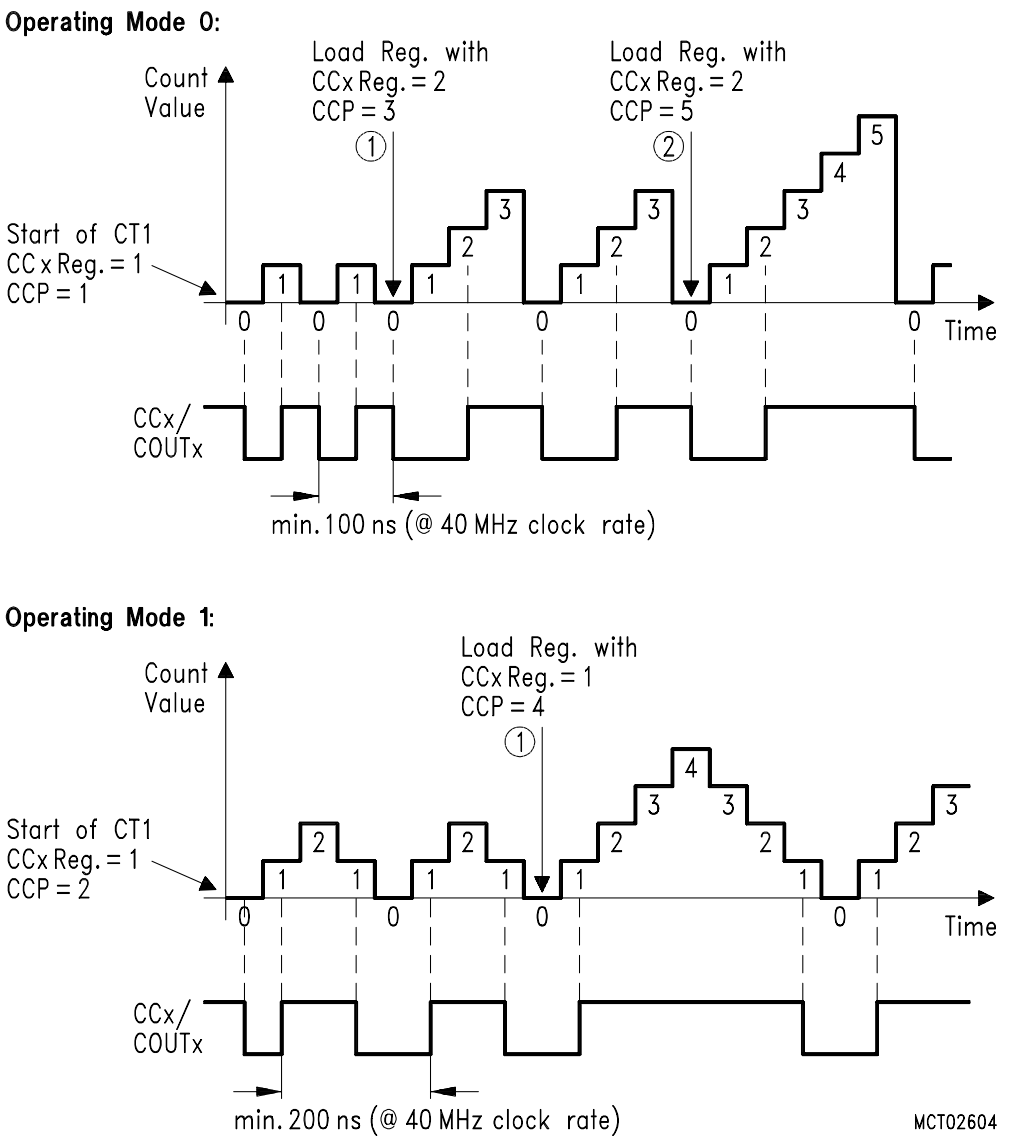


Figure 6-24
Maximum Period and Resolution of the Compare Timer 1 Unit

Table 6-5 shows the resolution and the period value range which depend on the selected compare timer 1 input clock prescaler ratio.

Table 6-5
Resolution and Period of the Compare Timer 1 (at f_{OSC} = 40 MHz)

Compare Timer 1 Input Clock	Operating Mode 0		Operating Mode 1	
	Resolution	Period	Resolution	Period
f_{OSC} / 2	50 ns	100ns - 3.28 ms	50 ns	200 ns - 6.55 ms
f_{OSC} / 4	100 ns	200 ns - 6.55 ms	100 ns	400 ns - 13.11 ms
f_{OSC} / 8	200 ns	400 ns - 13.11 ms	200 ns	800 ns - 26.21 ms
f_{OSC} / 16	400 ns	800 ns - 26.21 ms	400 ns	1.6 µs - 52.43 ms
f_{OSC} / 32	800 ns	1.6 µs - 52.43 ms	800 ns	3.2 µs - 104.86 ms
f_{OSC} / 64	1.6 µs	3.2 µs - 104.86 ms	1.6 µs	6.4 µs - 209.71 ms
f_{OSC} / 128	3.2 µs	6.4 µs - 209.72 ms	3.2 µs	12.8 µs - 419.42 ms
f_{OSC} / 256	6.4 µs	12.8 µs - 419.43 ms	6.4 µs	25.6 µs - 838.85 ms

Compare timer 1 period and duty cycle values can be calculated using the formulas below. In these formulas the following abbreviations are used :

pv = period value, stored in the period registers CCPH/CCPL
ov = offset value, stored in the offset registers CT1OFH/CT1OFL
cv = compare value, stored in the capture/compare registers CCHx/CCLx

Operating Mode 0 :

$$\text{Period value} = pv + 1$$

$$\text{Duty cycle of CCx outputs} = \left(1 - \frac{cv}{pv + 1}\right) \times 100\ \%$$

$$\text{Duty cycle of COUTx outputs} = \left(1 - \frac{cv - ov}{pv + 1}\right) \times 100\ \%$$

Operating Mode 1 :

$$\text{Period value} = 2 \times pv$$

$$\text{Duty cycle of CCx outputs} = \left(1 - \frac{cv}{pv}\right) \times 100\ \%$$

$$\text{Duty cycle of COUTx outputs} = \left(1 - \frac{cv - ov}{pv}\right) \times 100\ \%$$

6.3.2.5 Burst Mode of CAPCOM / COMP Unit

In the burst mode, both units of the CCU are combined in a way that the CAPCOM outputs COUTx or CCx and COUTx (controlled by bit BCMP in SFR BCON) are modulated by the output signal of the COMP unit. Using the burst mode, the CAPCOM unit operates in compare mode and the COMP unit provides a PWM signal which is switched to the COUTx outputs. This PWM signal typically has a higher frequency than the compare output signal of the CAPCOM unit. **Figure 6-25** shows the waveform generation using the burst mode.

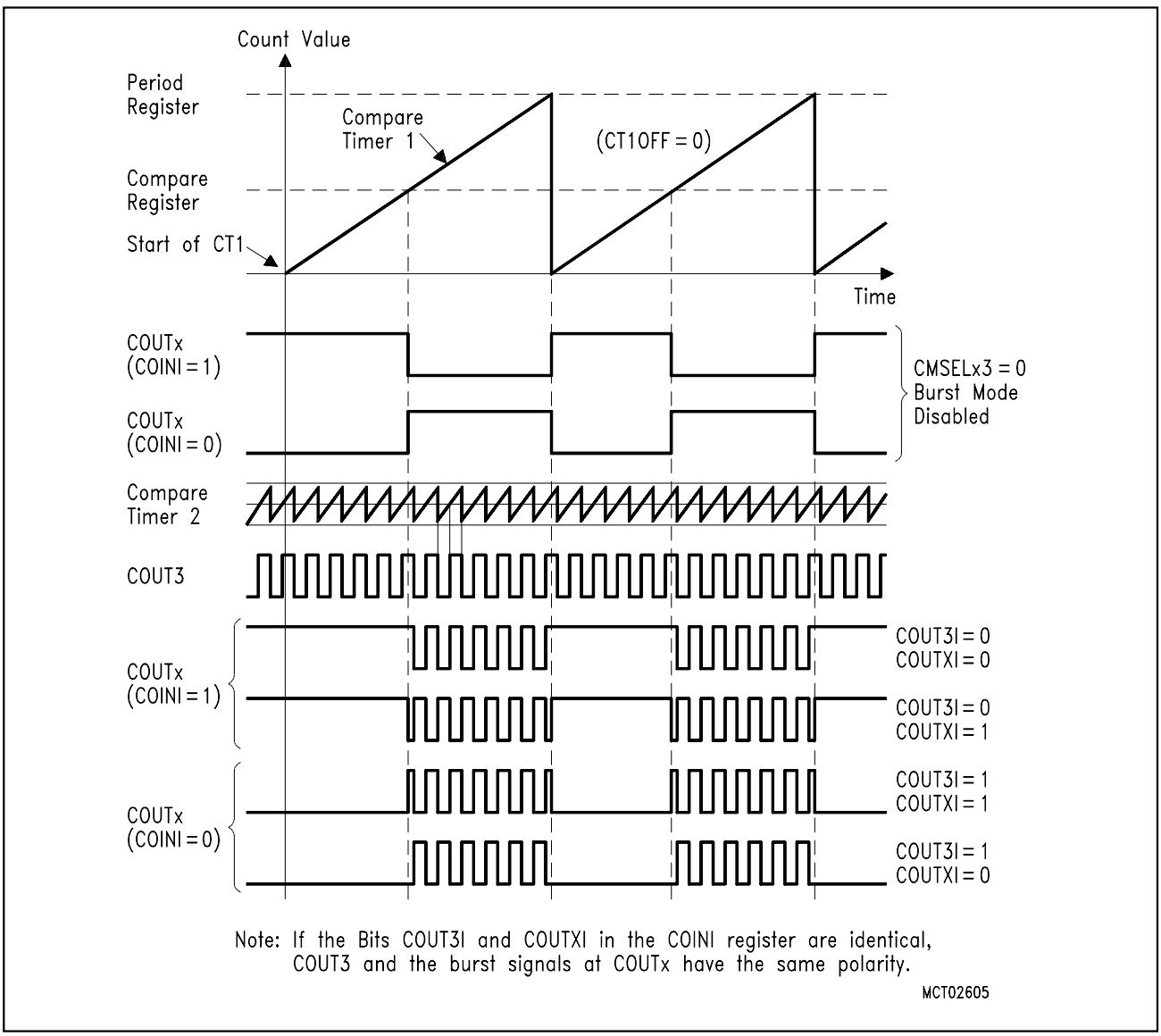


Figure 6-25
Burst Mode Operation

The burst mode of a COUTx output is enabled by the bit CMSELx3 which is located in the mode select registers CMSEL0 and CMSEL1. **Figure 6-25** shows four CAPCOM output signals with different initial logic states with burst mode disabled (CMSELx3=0) and burst mode enabled (CMSELx3=1). Generally, the CCx outputs cannot operate in burst mode. Optionally, the signal at COUTx may have inverted polarity than the PWM signal which is available at pin COUT3.

Depending on the corresponding initial compare output level bit in COINI, either a low or high level for the non-modulated state at the COUTx pins can be selected. Burst mode can be enabled in both operating modes of the compare timer 1. The burst mode as shown in **figure 6-25** is only valid if the block commutation mode of the CCU is disabled (bit BCEN of SFR BCON cleared).

The modulation of the compare output signals at COUTx is switched on (COUT3 signal is switched to COUTx) when the compare timer 1 content plus the value stored in the compare timer 1 offset register is equal or greater than the value stored in the compare register of CAPCOM channel x.

6.3.2.6 CAPCOM Unit in Capture Mode

The three channels of the CAPCOM unit can be individually programmed to operate in capture mode. In capture mode each CAPCOM channel offers one capture input at pin CCx. Compare timer 1 runs either in operating mode 0 or 1. A rising or/and falling edge at CCx will copy the actual value of the compare timer 1 into the compare/capture registers. Interrupts can be generated selectively at each transition of the capture input signal.

The capture mode is selected by writing the mode select registers CMSEL1 and CMSEL0 with the appropriate values. The bit combinations in CMSEL0 and CMSEL1 also define the signal transition type (falling/rising edge) which generates a capture event. If a CAPCOM channel is enabled for capture mode, its CCx input is sampled with $2/t_{CLCL}$ (= $f_{OSC}/2$ = half external CPU clock rate).

Consecutive capture events, generated through signal transitions at a CCx capture input, overwrite the corresponding 16-bit compare/capture register contents. This must be regarded when successive signal transitions are processed.

6.3.2.7 Trap Function of the CAPCOM Unit in Compare Mode

When a channel of the CAPCOM unit operates in compare mode its output lines can be decoupled in trap mode from the CAPCOM pulse generation. The trap mode is controlled by the external signal $\overline{\text{CTRAP}}$. The $\overline{\text{CTRAP}}$ signal is sampled once each 2nd oscillator clock cycle. If a low is detected, the trap flag TRF of register TRCON is set and CCx or COUTx compare outputs are switched immediately to the logic (inactive) state as defined by the bits in COINI. If CT1RES = 0, compare timer 1 continues its operation but no compare output signal will be generated. If CT1RES = 1, compare timer 1 is reset when $\overline{\text{CTRAP}}$ becomes active. When $\overline{\text{CTRAP}}$ is sampled inactive (high) again, the compare channel outputs are synchronously switched to the compare channel output signal generation when compare timer 1 has reached the count value 0000_H.

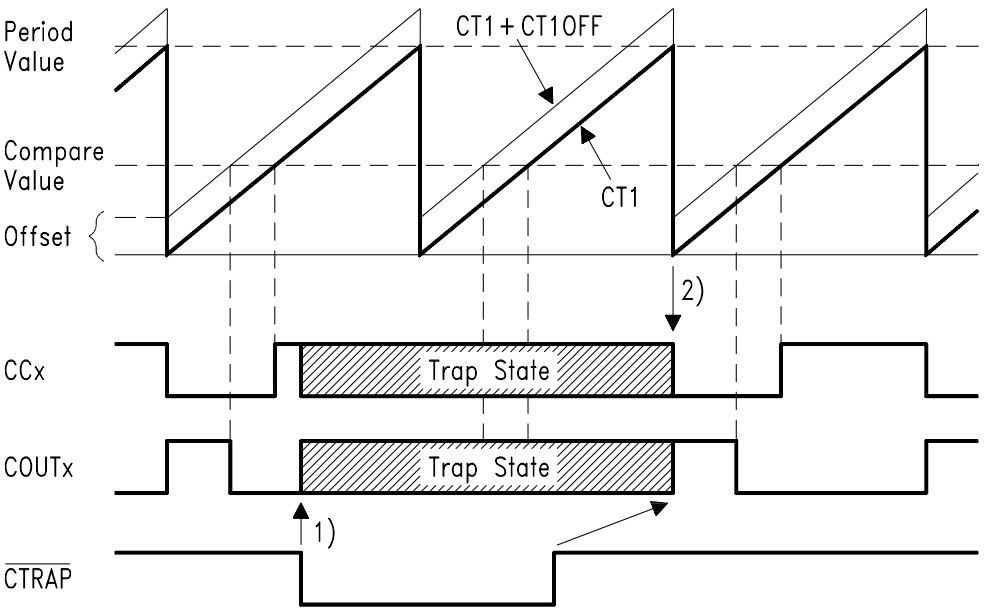
The trap function is controlled by bits in the TRCON register. The general enable function of the external $\overline{\text{CTRAP}}$ signal is controlled by one bit (TRPEN). Further, each CAPCOM compare channel output can be enabled/disabled selectively for trap function.

Figure 6-26 shows the trap function for the two outputs CCx and COUTx of one compare channel x. The timing diagram implies that the trap function is enabled at the CCx and COUTx outputs.

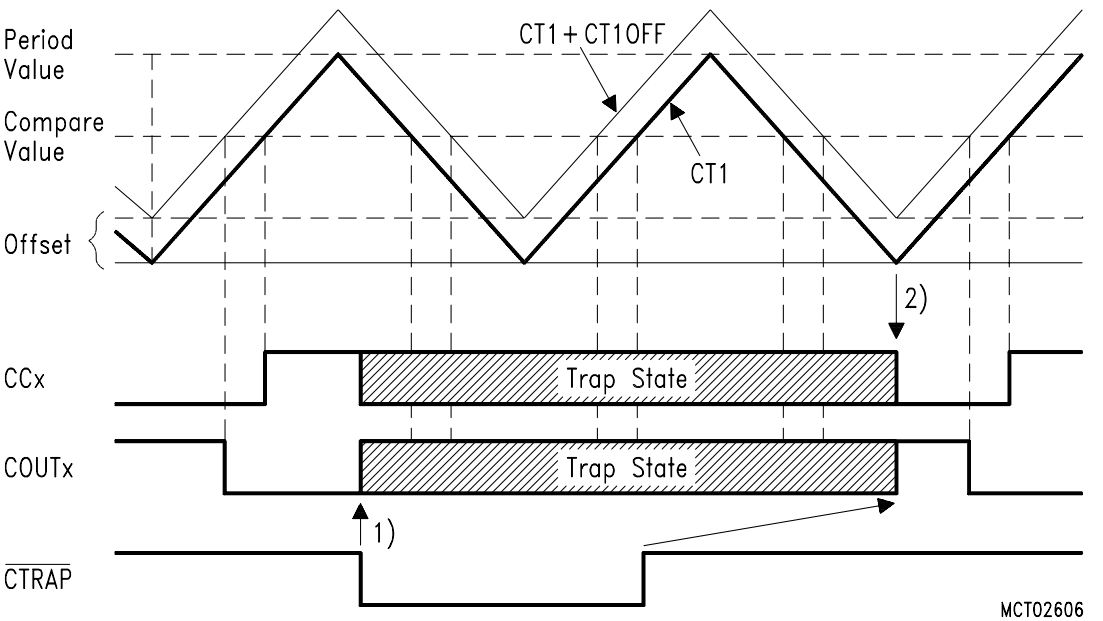
At reference point 1) in **figure 6-26** $\overline{\text{CTRAP}}$ becomes active and at reference point 2) the trap state is released again synchronously to the compare timer 1 count state 0000_H. If the trap function is enabled and $\overline{\text{CTRAP}}$ becomes active, bit TRF (trap flag) in SFR TRCON is set and a CCU emergency interrupt will be generated if the related interrupt enable bits are set. The flag TRF is level sensitive and must be cleared by software.

The trap function used in block commutation mode differs from the trap function described above. Especially the synchronization scheme is different (see **section 6.3.4.6**).

a) Trap Function in CAPCOM Operating Mode 0



b) Trap Function in CAPCOM Operating Mode 1



Note : The state of the CCx and COUTx signals in trap state is defined by the corresponding bits in COINI.

Figure 6-26
Trap Function of the CAPCOM Unit

6.3.2.8 CAPCOM Registers

The CAPCOM unit of the C504 contains several special function registers. **Table 6-6** gives an overview of the CAPCOM related registers.

Table 6-6
Special Function Registers of the CAPCOM Unit

Unit	Symbol	Description	Address
CAPCOM	CT1CON	Compare timer 1 control register	$E1_H$
Capture /	CCPL	Compare timer 1 period register, low byte	DE_H
Compare	CCPH	Compare timer 1 period register, high byte	DF_H
Unit	CT1OFL	Compare timer 1 offset register, low byte	$E6_H$
	CT1OFH	Compare timer 1 offset register, high byte	$E7_H$
	CMSEL0	Capture/compare mode select register 0	$E3_H$
	CMSEL1	Capture/compare mode select register 1	$E4_H$
	CCL0	Capture/compare register 0, low byte	$C2_H$
	CCH0	Capture/compare register 0, high byte	$C3_H$
	CCL1	Capture/compare register 1, low byte	$C4_H$
	CCH1	Capture/compare register 1, high byte	$C5_H$
	CCL2	Capture/compare register 2, low byte	$C6_H$
	CCH2	Capture/compare register 2, high byte	$C7_H$
	CCIR	Capture/compare interrupt request flag register	$E5_H$
	CCIE	Capture/compare interrupt enable register	$D6_H$
	COINI	Compare output initialization register	$E2_H$
	TRCON	Trap enable register	CF_H

The following sections describe the CAPCOM registers in detail.

Writing the CAPCOM Period/Offset/Compare Registers on-the-Fly

If compare timer 1 is running, period, offset or compare registers can be written with modified values for generating new periods or duty cycles of the compare output signals. For proper synchronization purposes a special mechanism for updating of the 16-bit offset, period, and compare registers is implemented in the C504. This mechanism is based on shadow latches. When new values for offset, period, or compare registers have been written into the shadow latches, the real register update operation must be initiated by setting bit STE1 (shadow transfer enable) in SFR CT1CON. When this bit is set, the content of the shadow latches is transferred to the real registers under the following conditions:

- Compare timer 1 operating mode 0 : Compare timer 1 has reached the period value stored in the CCPH/CCPL registers
- Compare timer 1 operating mode 1 : Compare timer 1 has reached the count value 0000_H

When the register transfer has been executed, STE1 is reset by hardware. So the software can recognize when the register transfer has occurred.

When compare timer 1 is started by setting the run bit CT1R the first time after reset, a shadow register transfer into the real registers is automatically executed. In this case STE1 must not be set.

Compare Timer 1 Control Register

The 16-bit compare timer 1 is controlled by the bits of the CT1CON register. With this register the count mode, the trap interrupt enable, the compare timer start/stop and reset, and the timer input clock rate is controlled.

Special Function Register CT1CON (Address $E1_H$) **Reset Value : 00010000_B**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$E1_H$	CTM	ETRP	STE1	CT1RES	CT1R	CLK2	CLK1	CLK0	CT1CON

Bit	Function
CTM	Compare timer 1 operating mode selection CTM=0 selects operating mode 0 (up count) and CTM=1 selects operating mode 1 (up/down count) for compare timer 1.
ETRP	CCU emergency trap interrupt enable If ETRP = 1, the emergency interrupt for the CCU trap signal is enabled.
STE1	CAPCOM unit shadow latch transfer enable When STE1 is set, the content of the compare timer 1 period, compare and offset registers (CCPH, CCPL, CCHx, CCLx, CT1OFH, CT1OFL) is transferred to its real registers when compare timer 1 reaches the next time the period value (operating mode 0) or value 0000_H (operating mode 1). After the shadow transfer event, STE1 is reset by hardware.
CLK2 CLK1 CLK0	Compare timer 1 input clock selection The input clock for the compare timer 1 is derived from the clock rate f_{OSC} of the C504 via a programmable prescaler. The following table shows the programmable prescaler ratios.

CLK2	CLK1	CLK0	Function
0	0	0	Compare timer 1 input clock is $f_{OSC}/2$
0	0	1	Compare timer 1 input clock is $f_{OSC}/4$
0	1	0	Compare timer 1 input clock is $f_{OSC}/8$
0	1	1	Compare timer 1 input clock is $f_{OSC}/16$
1	0	0	Compare timer 1 input clock is $f_{OSC}/32$
1	0	1	Compare timer 1 input clock is $f_{OSC}/64$
1	1	0	Compare timer 1 input clock is $f_{OSC}/128$
1	1	1	Compare timer 1 input clock is $f_{OSC}/256$

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>CT1RES
CT1R</td><td>Compare timer 1 reset control
Compare timer 1 run/stop control
These two bits control the start, stop, and reset function of compare timer 1. CT1RES is used to reset the compare timer and CT1R is used to start and stop the compare timer 1. The following table shows the functions of these two bits :
<table>
<tr><th>CT1RES</th><th>CT1R</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Compare timer 1 is stopped and holds its value; the compare outputs stay in the logic state as they are.</td></tr>
<tr><td>1</td><td>0</td><td>Compare timer 1 is stopped and reset; compare outputs are set to the logic state as defined in SFR COINI (default after reset).</td></tr>
<tr><td>0</td><td>0 → 1</td><td>Compare timer 1 starts. Before CT1R is set the first time, the CMSEL register should be programmed (enable capture/compare functions).</td></tr>
<tr><td>1</td><td>0 → 1</td><td>Compare timer 1 starts running from count value 0000_H; compare outputs are set to the logic state as defined in SFR COINI.</td></tr>
<tr><td>0</td><td>1 → 0</td><td>Compare timer 1 is stopped and holds its value; the compare outputs drive their actual logic state.</td></tr>
<tr><td>1</td><td>1 → 0</td><td>Compare timer 1 is stopped and reset to 0000_H; compare outputs are set to the logic state as defined in SFR COINI.</td></tr>
</table>
Note for capture mode :
Setting CT1R=0 and CT1RES=1 after a capture event will destroy the value stored in the capture register CCx. Therefore, CT1RES should be set to 0 in capture mode. Reason : if CT1R=0 and CT1RES=1 all shadow registers are transparent (switched directly) to the real registers.</td></tr>
</table>

Note : When software power down mode is entered with CT1RES bit of SFR CT1CON set, the compare timer 1 is reset after the execution of a wake-up from power-down mode procedure. When CT1RES is cleared before software power down mode is entered and a wake-up from power-down mode procedure has been executed, the compare timer 1 is not reset. Depending on the state of bit CT1R at power down mode entry, the compare timer 1 either stops (CT1R=0) or continues (CT1R=1) counting after a wake-up from power-down mode procedure. Further details of the power down mode are described in chapter 9.2 .

Compare Timer 1 Period Registers

The compare timer 1 period registers CCPH and CCPL store the 16-bit value for the compare timer 1 count period. CCPH holds the high byte of the 16-bit period value and CCPL holds the low byte. If CCPH/CCPL is written, always shadow latches are loaded. The content of these shadow latches is transferred to the real registers when STE1 is set and the compare timer 1 reaches its period value (operating mode 0) or count value 0000_H (operating mode 1). When the compare timer 1 period registers are read, always shadow latches are accessed.

Special Function Register CCPL (Address DE_H) **Reset Value : 00_H**
Special Function Register CCPH (Address DF_H) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
DE_H	.7	.6	.5	.4	.3	.2	.1	LSB	CCPL
DF_H	MSB	.6	.5	.4	.3	.2	.1	.0	CCPH

Bit	Function
CCPL.7 - 0	Compare timer 1 period value low byte The 8-bit value in the CCPL register is the low byte of the 16-bit period value of compare timer 1 (shadow latch).
CCPH.7 - 0	Compare timer 1 period value high byte The 8-bit value in the CCPH register is the high byte of the 16-bit period value of compare timer 1 (shadow latch).

Compare Timer 1 Offset Registers

The CT1OFH and CT1OFL registers contain the value for the compare timer 1. CT1OFH holds the high byte of the 16-bit offset value and CT1OFL holds the low byte. For the detection of a compare match event, which results in changing polarity of a COUTx compare output signal, the content of CT1OFH/CT1OFL is always added to the actual value of the compare timer 1: The value stored in the offset registers has no effect on the signal generation at the CCx compare outputs.

If the compare timer 1 offset registers are written, always shadow latches are loaded. The content of these shadow latches is transferred to the real registers when STE1 is set and the compare timer 1 reaches its period value (operating mode 0) or count value 0000_H (operating mode 1). When the compare timer 1 offset registers are read, always shadow latches are accessed.

Special Function Register CT1OFL (Address $E6_H$) **Reset Value : 00_H**
Special Function Register CT1OFH (Address $E7_H$) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$E6_H$	.7	.6	.5	.4	.3	.2	.1	LSB	CT1OFL
$E7_H$	MSB	.6	.5	.4	.3	.2	.1	.0	CT1OFH

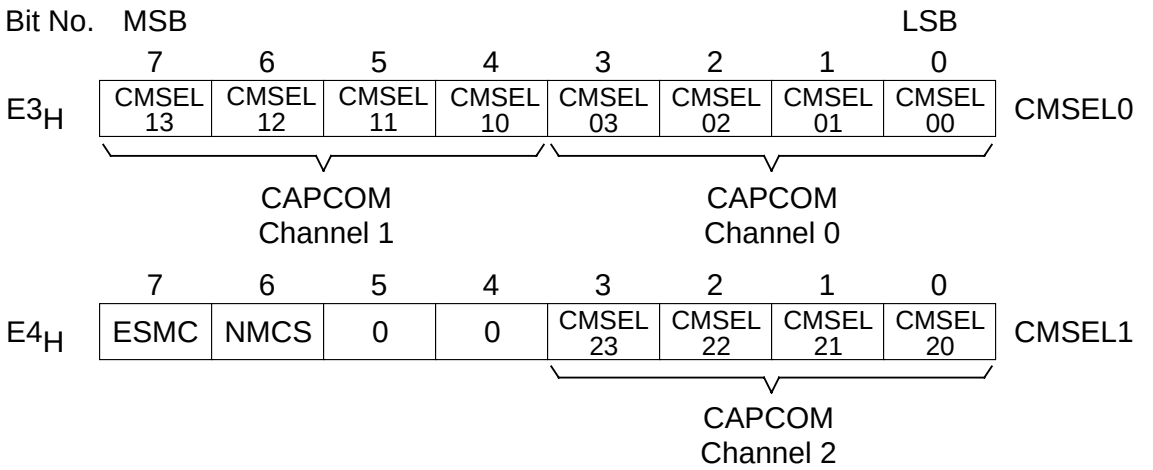
Bit	Function
CT1OFL.7 - 0	8-bit compare timer 1 offset value low byte The 8-bit value in the CT1OFL register is the low part of the offset value for compare timer 1 (shadow latch).
CT1OFH.7 - 0	8-bit compare timer 1 offset value high byte The 8-bit value in the CT1OFH register is the high part of the offset value for compare timer 1 (shadow latch).

In order to generate correct dead times for PWM signals the offset value stored in CT1OFH/ CT1OFL must be lower than the values stored in the compare registers !

Capture/Compare Channel Mode Select Registers

The capture/compare channels of the CAPCOM unit can operate individually either in compare mode or in capture mode. The CMSEL0 and CMSEL1 registers contain the mode select bits for the CAPCOM unit.

Special Function Register CMSEL0 (Address $E3_H$) **Reset Value : 00_H**
Special Function Register CMSEL1 (Address $E4_H$) **Reset Value : 00_H**



Bit	Function
ESMC	Enable software controlled multi-channel PWM modes If ESMC=0, switching of the follower state in 4-/5-/6-phase multi-channel PWM mode is controlled by compare timer 1 reaching its period value. If ESMC=1, switching of the follower state in 4-/5-/6-phase multi-channel PWM mode is controlled by bit NMCS.
NMCS	Next multi-channel PWM state Setting bit NMCS (with ESMC set) will select the follower state in the 4-/5-/6-phase multi-channel PWM mode, which is taken into account at the output pins, when compare timer 1 is 0. Bit NMCS is reset by hardware in the next clock cycle after it has been set.
CMSELx3 x=0-2	Switching compare timer 2 output signal to COUTx If CMSELx3 is set and compare mode is selected for the outputs COUTx, the output signal of the 10-bit compare unit, typically a higher frequency signal, is switched (modulated) to the COUTx pin. The state of the corresponding COINI bit at the start of compare timer 1 defines the logic level of the CAPCOM channel output signal at iwhich the COMP output signal is output to COUTx. COINI is set : The COMP output is switched to COUTx during the low phase of the CAPCOM channel X signal. COINI is cleared : The COMP output is switched to COUTx during the high phase of the CAPCOM channel X signal.

Bit	Function
CMSELx2- 0 x=0-2	CAPCOM capture / compare mode enable bits The CMSEL registers are used to select/enable the operating mode and the output/input pin configuration of the capture/compare channels. Each CAPCOM channel can be programmed individually either for compare or capture operation.

CMSEL x2	CMSEL x1	CMSEL x0	Mode
0	0	0	Compare outputs disabled; No compare output signal is generated; CCx and COUTx are normal I/O pins.
0	0	1	Compare output on pin CCx enabled; COUTx is normal I/O pin.
0	1	0	Compare output on pin COUTx enabled; CCx is normal I/O pin.
0	1	1	Compare outputs on pins CCx and COUTx enabled.
1	0	0	Capture mode enabled; signal transitions at CCx do not generate a capture event; COUTx is a normal I/O pin or analog input pin.
1	0	1	Capture mode enabled; CCx is configured as a capture input and a rising edge at CCx transfers compare timer 1 content into the capture register; COUTx is a normal I/O pin or analog input pin.
1	1	0	Capture mode enabled; CCx is configured as a capture input and a falling edge at CCx transfers compare timer 1 content into the capture register; COUTx is a normal I/O pin or analog input pin.
1	1	1	Capture mode enabled; CCx is configured as a capture input. Rising and falling edge at CCx transfer the compare timer 1 content into the capture register; COUTx is a normal I/O pin or analog input pin.

Note : only CC0 / COUT0 can be analog inputs if not selected as compare output.

In compare mode the two output signals of a CAPCOM channel can be enabled selectively. In capture mode the type of signal transition which will generate a capture event can be chosen.

Capture / Compare Registers of CAPCOM Unit

The capture/compare registers are 16-bit registers, organized as two 8-bit byte-wide registers. Each of the three CAPCOM channels has one capture/compare register. In compare mode they hold a compare value which typically defines the duty cycle of the output signals. In capture mode, the actual compare timer 1 value is transferred into the capture/compare registers at a capture event.

If CCLx/CCHx is written, always shadow latches are loaded. The content of these shadow latches is transferred to the real registers when STE1 is set and the compare timer 1 reaches its period value (operating mode 0) or count value 0000_H (operating mode 1). When the capture/compare registers are read, always the real registers are accessed because of capture mode.

Special Function Registers CCL0/CCH0 (Addresses $C2_H/C3_H$) **Reset Value : 00_H**
Special Function Registers CCL1/CCH1 (Addresses $C4_H/C5_H$) **Reset Value : 00_H**
Special Function Registers CCL2/CCH2 (Addresses $C6_H/C7_H$) **Reset Value : 00_H**

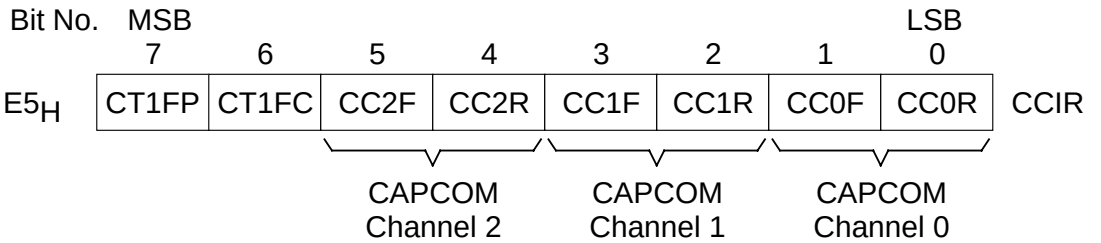
Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$C2_H$	.7	.6	.5	.4	.3	.2	.1	LSB	CCL0
$C3_H$	MSB	.6	.5	.4	.3	.2	.1	.0	CCH0
$C4_H$	.7	.6	.5	.4	.3	.2	.1	LSB	CCL1
$C5_H$	MSB	.6	.5	.4	.3	.2	.1	.0	CCH1
$C6_H$	.7	.6	.5	.4	.3	.2	.1	LSB	CCL2
$C7_H$	MSB	.6	.5	.4	.3	.2	.1	.0	CCH2

Bit	Function
CCLx.7 - 0 x=0-2	Capture/compare value low byte The 8-bit value in the CCLx register is the low part of the 16-bit capture/ compare value of channel x.
CCHx.7 - 0 x=0-2	Capture/compare value high byte The 8-bit value in the CCHx register is the low part of the 16-bit capture/ compare value of channel x.

Capture / Compare Interrupt Request Flags / Register

The interrupt flags of the CAPCOM capture/compare match and compare timer 1 interrupt are located in the register CCIR. All CAPCOM capture/compare match interrupt flags are set by hardware and must be cleared by software. A capture/compare match interrupt is generated with the setting of a CCxR bit (x=0-2) if the corresponding enable bits are set. The compare timer 1 interrupt is triggered by the CT1FP or CT1FC bits of SFR CCIR.

Special Function Register CCIR (Address $E5_H$) **Reset Value : 00_H**



Bit	Function
CT1FP	Compare timer 1 period flag Compare timer 1 operating mode 0 : CT1FP is set if compare timer 1 reaches the period value. Compare timer 1 operating mode 1 : CT1FP is set if compare timer 1 reaches the period value and changes the count direction from up- to down counting. Bit CT1FP must be cleared by software. If compare timer 1 interrupt is enabled, the setting of CT1FP will generate a compare timer 1 interrupt.
CT1FC	Compare timer 1 count direction change flag This flag can only be set if compare timer 1 runs in operating mode 1 (CTM=1). CT1FC is set when compare timer 1 reaches count value 0000_H and changes the count direction from down- to up-counting. If compare timer 1 interrupt is enabled, the setting of CT1FC will generate a compare timer 1 interrupt. Bit CT1FC must be cleared by software.
CCxR x=0-2	Capture/compare match on up-count flag Capture Mode : CCxR is set at a low-to-high transition (rising edge) of the corresponding CCx capture input signal. Compare Mode : CCxR is set if the compare timer 1 value matches the compare register CCx value during the up-count phase.

Bit	Function
CCxF x=0-2	Capture/compare match on down-count flag Capture Mode : CCxF is set at a high-to-low transition (falling edge) of the corresponding CCx capture input signal. Compare Mode : CCxF is set if the compare timer 1 value matches the compare register CCx value during the down-count phase (only in compare timer 1 operating mode 1).

Capture / Compare Interrupt Enable Register

The bits of the interrupt enable register CCIE control the specific interrupt enable/disable functions of the CAPCOM part of the capture/compare unit.
The bits ECTP and ECTC control the compare timer 1 period/count change interrupt. Depending on the mode in which compare timer 1 is running, interrupts can be generated at a period match or a count direction change event.
The lower 6 bits of CCIE are the CAPCOM channel specific interrupt enable/disable control bits for the capture or compare match interrupt. The functions of these bits depend on the selected mode (capture or compare) of a capture/compare channel. In compare mode, compare channel specific interrupts can be generated at a match event between compare register content and compare timer 1 count value during the up- or down-counting phase of compare timer 1. In capture mode, capture channel specific interrupts can be generated selectively at rising or falling or both edges of the capture input signals at CCx.

Special Function Registers CCIE (Address $D6_H$) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D6_H$	ECTP	ECTC	CC2FEN	CC2REN	CC1FEN	CC1REN	CC0FEN	CC0REN	CCIE

Bit	Function
ECTP	Enable compare timer 1 period interrupt If ECTP = 0, the compare timer 1 period interrupt is disabled. Compare timer 1 operating mode 0 : If ECTP = 1, an interrupt is generated when compare timer 1 reaches the period value. Compare timer 1 operating mode 1 : If ECTP = 1, an interrupt is generated when compare timer 1 reaches the period value and changes the count direction from up- to down-counting.
ECTC	Enable compare timer 1 count direction change interrupt status If ECTC = 0, the compare timer 1 count change interrupt is disabled. Compare timer 1 operating mode 0 : Bit has no effect on the interrupt generation. Compare timer 1 operating mode 1 : If ECTC = 1, an interrupt is generated when compare timer 1 reaches count value 0000_H and changes its count direction from down- to up-counting.

Bit	Function
CCxREN (x=0-2)	Capture / compare rising edge interrupt enable Capture Mode : If CCxREN is set, an interrupt is generated at a low-to-high transition (rising edge) of the corresponding CCx input signal. Compare Mode : If CCxREN is set, an interrupt is generated if the compare timer 1 value matches the compare register CCx value during the up-counting phase of the compare timer 1. This function is available in both compare timer 1 operating modes.
CCxFEN (x=0-2)	Capture / compare falling edge interrupt enable Capture Mode : If CCxFEN is set, an interrupt is generated at a high-to-low transition (falling edge) of the corresponding CCx input signal. Compare Mode : If CCxFEN is set, an interrupt is generated only in compare timer mode 1 if the compare timer 1 value matches the compare register CCx value during the down-counting phase of the compare timer 1. This function is available only in compare timer 1 operating mode 1.

Compare Output Initialization Register COINI

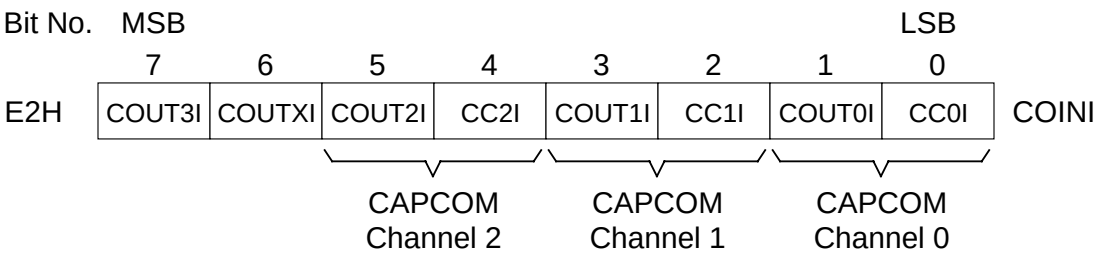
The six lower bits of the COINI register define the initial values (passive levels) of the port 1 lines, which are programmed to be used as a compare output. If an output of the CAPCOM unit is enabled for compare mode operation by writing the corresponding bit combination into the CMSEL0/ CMSEL1 registers, the compare output is switched into push-pull mode and starts driving an initial logic level as defined by the bits of the COINI register. The value of the bits of COINI may be is further selectively switched to the compare outputs during the trap state.

Bit COUTXI controls an inverter for the COMP unit output signal, when it is wired to the CCx and COUTx outputs in burst or multi-channel PWM mode. COUT3I defines the initial logic level at COUT3 before compare timer 2 is started as well as the logic state when COUT3 is disabled by setting bit ECT2O in SFR CT2CON (see **figure 6-27**).

The COINI register should be written prior to the starting of the compare timers. Any write operation to the COINI register when the compare timer is running will affect the compare output signals immediately and drive the logic value as defined by the bits of COINI.

A PWM output signal of the C504 basically consists of two phases, an inactive phase and an active phase. The inactive phase of a PWM output signal is defined by the bit in the register COINI. A 1 in a bit location 0 to 5 of COINI defines the high level of the corresponding PWM compare output signal as its inactive phase.With a 0 in a bit location of COINI a low level is selected as inactive phase.

Special Function Register COINI (Address $E2_H$) **Reset Value : FF_H**



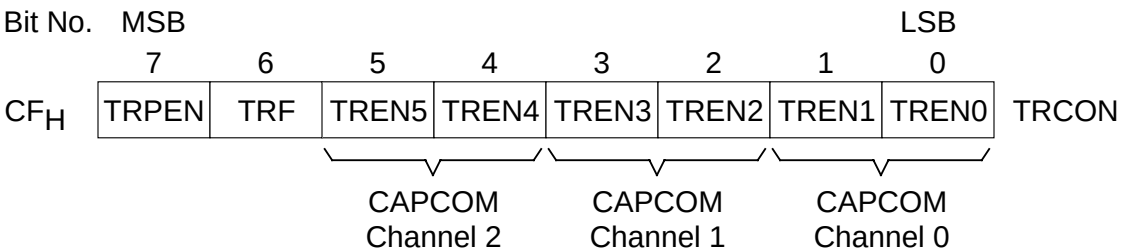
Bit	Function
COUT3I	COUT3 initial logic level This bit defines the initial logic state of the output COUT3 before compare timer 2 is started the first time. Further, COUT3I defines the logic state of output COUT3 when bit ECT2O (CT2CON.6) is reset (COUT3 disabled).
COUTXI	Compare timer 1 output signal inversion in burst and block commutation When COUTXI is set, the output signal of compare timer 2, which is wired to the compare outputs COUTx (x=0-2) in burst or block commutation mode is inverted.

Bit	Function
CCxI, COUTxI (x=0-2)	Compare output initial value / compare output level in trap condition Bits at even bit positions (0,2,4) are assigned to the CCx compare outputs. Bits at odd bit positions (1,3,5) are assigned to the COUTx compare outputs. CCxI, COUTxI = 0 : If compare timer 1 is not running (after reset), an output CCx/COUTx (x=0-2) is switched into push-pull mode and starts driving an initial value of “0“ when this CCx/ COUTx output is programmed as compare output. by writing the corresponding bit combination into the CMSEL0/CMSEL1 registers. If the compare timer runs and a bit of register TREN is set, a compare channel output will be switched to “0“ level in trap state. CCxI, COUTxI = 1 : If compare timer 1 is not running (after reset), an output CCx/COUTx (x=0-2) is switched into push-pull mode and starts driving an initial value of “1“ when this CCx/ COUTx output is programmed as compare output. by writing the corresponding bit combination into the CMSEL0/CMSEL1 registers. If the compare timer runs and a bit of register TREN is set, a compare channel output will be switched to “1“ level in trap state. The COINI values are only valid for capture/compare outputs, which are enabled for compare mode operation.

Trap Enable Register

The trap enable register TREN is used to enable selectively the compare outputs of the three CAPCOM channels for switching it into high or low level in the trap state as defined by the bits of the COINI register. Additionally, for a general enable of the trap function, bit TRPEN must be set. The TRF flag indicates when an low level is detected at the $\overline{\text{CTRAP}}$ input signal.

Special Function Register TRCON (Address CF_H) **Reset Value : 00_H**



Bit	Function
TRPEN	External $\overline{\text{CTRAP}}$ trap function enable bit This bit is a general enable bit for the trap function of the $\overline{\text{CTRAP}}$ input signal. TRPEN = 0 : External trap input $\overline{\text{CTRAP}}$ is disabled (default after reset). TRPEN = 1 : External trap input $\overline{\text{CTRAP}}$ is enabled;
TRF	Trap flag TRF is set by hardware if the trap function is enabled (TRPEN=1) and the $\overline{\text{CTRAP}}$ level becomes active (low). If enabled, an interrupt is generated when TRF is set. TRF must be reset by software.
TREN5-0	Trap enable control bits Bits at even bit positions (0,2,4) are assigned to the CCx compare outputs. Bits at odd bit positions (1,3,5) are assigned to the COUTx compare outputs. TRENx = 0 : Compare channel output provides CAPCOM output signal in trap state. TRENx = 1 : Compare channel output is enabled to set the logic level of the compare output CCx or COUTx in the trap state to a logic state as defined by the corresponding bits of the COINI register. When writing TREN0-5, bit TRF should be set to 0. Otherwise, setting TREN0-5 will generate a software trap interrupt.

6.3.3 Compare (COMP) Unit Operation

The Capture/Compare Unit CCU of the C504 also provides an 10-bit Compare Unit (COMP) which operates as a single channel pulse generator with a pulse width modulated output signal. This output signal is available at the output pin COUT3 of the C504. In the combined multi-channel PWM modes and in burst mode of the CAPCOM unit the output signal of the COMP unit can also be switched to the output signals COUTx or CCx. **Figure 6-27** shows the block diagram and the pulse generation scheme of the COMP unit (e.g. initial value of COUT3 is set to 0).

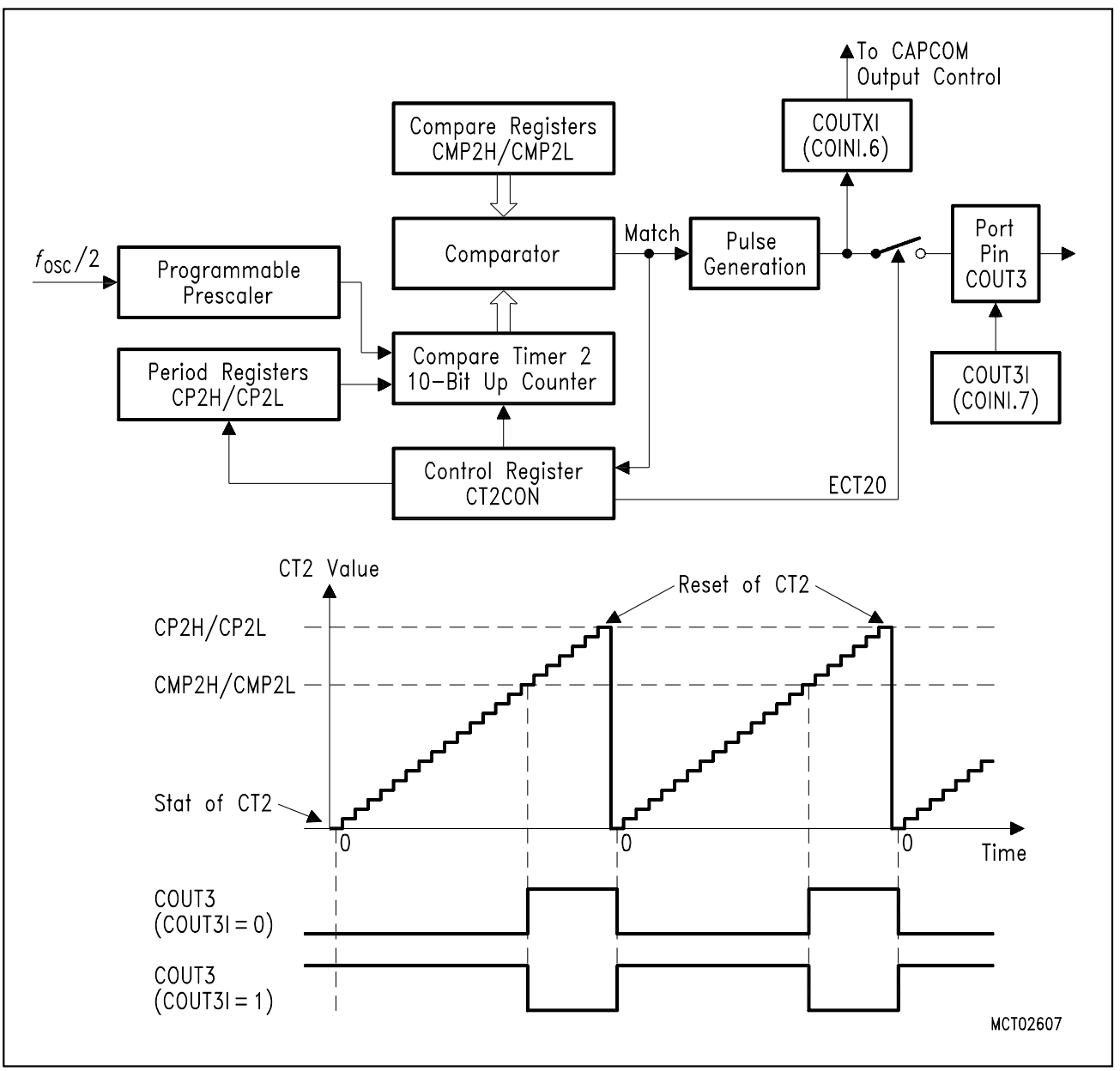


Figure 6-27
COMP Unit : Block Diagram and Pulse Generation Scheme

The COMP unit has a 10-bit up-counter (compare timer 2, CT2) which starts counting from 000_H up to the value stored in the period register and then is again reset. This compare timer 2 operation is equal to the operating mode 0 of compare timer 1. When the count value of CT2 matches the value

stored in the compare registers CMP2H/CMP2L, COUT3 toggles its logic state. When compare timer 2 is reset to 000_H, COUT3 toggles again its logic state.
COUT3 is only an output pin. After a reset operation COUT3 drives a high level as defined by the reset value (=1) of bit COUT3 I of SFR COINI. When compare timer 2 is running (bit CT2R in SFR CT2CON is set), bit ECT2O in SFR CT2CON allows the disconnection of COUT3 from compare timer 2 signal generation. In this case, the logic value of COUT3I (bit COINI.7) is put to the COUT3 output. When ECT2O is set thereafter, the compare timer 2 output signal is again switched to the COUT3 output.

In the combined multi-channel PWM modes and in the burst mode the compare timer 2 output signal can be also switched to the CAPCOM output pins COUT0, COUT1, and COUT3. In these modes, the polarity of the modulated output signal at COUT2-0 can be inverted by setting bit COUTXI (COINI.6)

6.3.3.1 COMP Registers

The COMP unit has five SFRs which are listed in **table 6-7**.

Table 6-7
Special Function Registers of the COMP Unit

Unit	Symbol	Description	Address
COMP Compare Unit	CT2CON	Compare timer 2 control register	$C1_H$
	CP2L	Compare timer 2 period register, low byte	$D2_H$
	CP2H	Compare timer 2 period register, high byte	$D3_H$
	CMP2L	Compare timer 2 compare register, low byte	$D4_H$
	CMP2H	Compare timer 2 compare register, high byte	$D5_H$

The compare timer 2 period and compare registers store a 10-bit value, organized in two bytes. For proper synchronization purposes, these registers are not written directly. Each value of a write operation to these registers is stored in shadow latches. The transfer of these shadow latches into the real registers is synchronized with the compare timer 2 value 000_H and controlled by bit STE2. When the period or compare value is changed by writing the corresponding SFR, the setting of bit STE2 (CT2CON.5) enables the write transfer of the shadow registers into the real registers. This shadow latch transfer happens when the compare timer 2 reaches the count value 000H the next time after STE2 has been set. With the automatic transfer of the shadow latches to the real registers, bit STE2 is reset by hardware. When the compare timer 2 period and compare registers are initialized after reset, bit STE2 must also be set to enable the shadow latch transfer when compare timer 2 is started the first time.

Note : Read operations with the compare timer 2 period and compare registers always access the shadow registers and not the real registers.

Compare Timer 2 Control Register

The 10-bit compare timer 2 is controlled by the bits of the CT2CON register. With this register the count mode, the timer input clock rate, and the compare timer reset function is controlled.

Special Function Register CT2CON (Address $C1_H$) **Reset Value : 00010000_B**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$C1_H$	CT2P	ECT2O	STE2	CT2RES	CT2R	CLK2	CLK1	CLK0	CT2CON

Bit	Function
CT2P	Compare timer 2 period flag When the compare timer 2 value matches with the compare timer 2 period register value bit CT2P is set. If the compare timer 2 interrupt is enabled, the setting of CT2P will generate a compare timer 2 interrupt. Bit CT2P must be cleared by software.
ECT2O	Enable compare timer 2 output When ECT2O is cleared and compare timer 2 is running, output COUT3 is put into the logic state as defined by bit COUT3I which is located in SFR COINI.6. When ECT2O is set and compare timer 2 is running, the compare timer 2 output COUT3 is enabled and outputs the PWM signal of the COMP unit.
STE2	COMP unit shadow latch transfer enable When STE2 is set, the content of the compare timer 2 period and compare latches (CP2H, CP2L, CMP2H, CMP2L) is transferred to its real registers when compare timer 2 reaches the next time the period value. After the shadow transfer event, STE2 is reset by hardware.

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>CT2RES
CT2R</td><td>Compare timer 2 reset control
Compare timer 2 run/stop control
These two bits controls the start, stop, and reset function of the compare timer 2. CT2RES is used to reset the compare timer and CT2R is used to start and stop the compare timer 2. The following table shows the functions of these two bits :
<table>
<tr><th>CT2RES</th><th>CT2R</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Compare timer 2 is stopped; compare output COUT3 stays in the logic state as it is.</td></tr>
<tr><td>0</td><td>1</td><td>Compare timer 2 is running. If CT2R is set the first time after reset, COUT3 is set to the logic state as defined by bit COUT3I of SFR COINI.</td></tr>
<tr><td>1</td><td>0</td><td>Compare timer 2 is stopped and reset. The output COUT3 is set to the logic state as defined by bit COUT3I of SFR COINI (default after reset).</td></tr>
<tr><td>1</td><td>1</td><td>Compare timer 2 is further running.</td></tr>
</table>
Note : ECT2O must be set for COUT3 signal output enable.</td></tr>
<tr><td>CLK2
CLK1
CLK0</td><td>Compare timer 2 input clock selection
The input clock for the compare timer 2 is derived from the clock rate f_{osc} of the C504 via a programmable prescaler. The following table shows the programmable prescaler ratios.
<table>
<tr><th>CLK2</th><th>CLK1</th><th>CLK0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Compare timer 2 input clock is $f_{osc}/2$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Compare timer 2 input clock is $f_{osc}/4$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Compare timer 2 input clock is $f_{osc}/8$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Compare timer 2 input clock is $f_{osc}/16$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Compare timer 2 input clock is $f_{osc}/32$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Compare timer 2 input clock is $f_{osc}/64$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Compare timer 2 input clock is $f_{osc}/128$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Compare timer 2 input clock is $f_{osc}/256$</td></tr>
</table></td></tr>
</table>

Note : With a reset operation (external or internal) compare timer 2 is reset (000_H) and stopped. When software power down mode is entered with CT2RES bit of SFR CT2CON set, the compare timer 2 is reset after the execution of a wake-up from power-down mode procedure. When CT2RES is cleared before software power down mode is entered and a wake-up from power-down mode procedure has been executed, the compare timer 2 is not reset. Depending on the state of bit CT2R at power down mode entry, the compare timer 2 either stops (CT2R=0) or continues (CT2R=1) counting after a wake-up from power-down mode procedure. Further details of the power down mode are described in chapter 9.2 .

Compare Timer 2 Period Registers

The compare timer 2 period registers CP2L/CP2H hold the 10-bit value for the compare timer 2 period. When the compare timer 2 value is equal to the value stored in the period register, the COUT3 signal changes from inactive to active state. If CP2H/CP2L is written, only shadow latches are written. The content of these latches is transferred to the real registers at compare timer count value 000_H using bit STE2 of SFR CT2CON.

When the compare timer 2 period registers CP2L/CP2H are read, always the shadow registers are accessed.

Special Function Register CP2L (Address $D2_H$) **Reset Value : 00_H**
Special Function Register CP2H (Address $D3_H$) **Reset Value : $XXXXXX00_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D2_H$	.7	.6	.5	.4	.3	.2	.1	.0	CP2L
$D3_H$	–	–	–	–	–	–	.1	.0	CP2H

Bit	Function
CP2L.7 - 0	Compare timer 2 period low byte The CMP2L register holds the lower 8 bits of the 10-bit compare value for compare timer 2 (shadow latch).
CP2H.1 - 0	Compare timer 2 period high bits The CMP2H register holds most significant two bits of the 10-bit compare value for compare timer 2 (shadow latch).
–	Reserved bits

Compare Timer 2 Compare Registers

The compare registers CMP2H/CMP2L of compare timer 2 hold the 10-bit compare value which defines the duty cycle of the output signal at COUT3. When the compare timer 2 value is equal to the value stored in the CMP2H/CMP2L register, the COUT3 signal changes from passive to active state. If CMP2H/CMP2L is written, only shadow latches are written. The content of these latches is transferred to the real registers when compare timer count value 000_H is reached and bit STE2 of SFR CT2CON has been set.

When the compare CMP2H/CMP2L registers are read, always the shadow registers are accessed.

Special Function Registers CMP2L (Address $D4_H$) **Reset Value : 00_H**
Special Function Registers CMP2H (Address $D5_H$) **Reset Value : $XXXXXX00_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D4_H$	.7	.6	.5	.4	.3	.2	.1	.0	CMP2L
$D5_H$	–	–	–	–	–	–	.1	.0	CMP2H

Bit	Function
CMP2L.7 - 0	Compare value low byte for compare timer 2 The CMP2L register holds the lower 8 bits of the 10-bit compare value for compare timer 2.
CMP2H.1 - 0	Compare value high bits for compare timer 2 The CMP2H register holds most significant two bits of the 10-bit compare value for compare timer 2.
–	Reserved bits

6.3.4 Combined Multi-Channel PWM Modes

The CCU of the C504 has been designed to support also motor control or inverter applications which have a demand for specific multi-channel PWM signal generation. In these combined multi-channel PWM modes the CAPCOM unit (compare timer 1) and the COMP unit (compare timer 2) of the C504 CCU are working together.

In the combined multi-channel PWM modes the signal generation of the CCx and COUTx PWM outputs can basically be controlled either by the interrupt inputs $\overline{INT0}$ to $\overline{INT2}$ (block commutation mode) or by the operation of compare timer 1 or by software (multi-channel PWM mode). In the active phase of a combined multi-channel PWM mode, compare timer 1 compare output signal or the compare timer 2 output signal or both can be switched selectively to the CCx or COUTx PWM output lines.

The combined multi-channel PWM modes are controlled by the BCON (block commutation control) register. **Figure 6-28** shows the block diagram of the multi-channel PWM mode logic which is integrated in the C504.

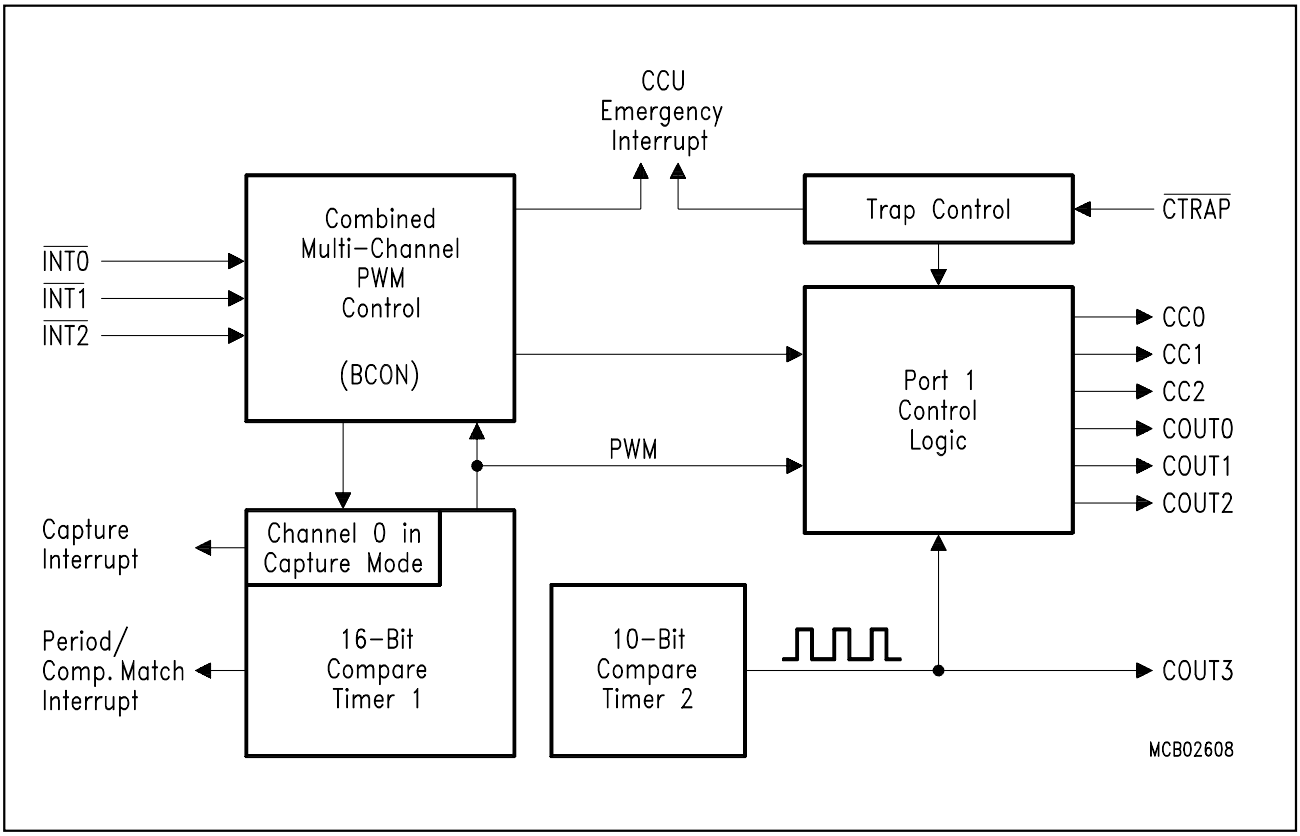


Figure 6-28
Block Diagram of the Combined Multi-Channel PWM Modes in the C504

In block commutation mode, a well defined incoming digital signal pattern of e.g. hall sensor signals, which are applied to the $\overline{INT0\text{-}2}$ inputs, is sampled. Each transition at the $\overline{INT0\text{-}2}$ inputs results in a change of the state of the PWM outputs. In block commutation mode, all six PWM output signals CCx and COUTx (x=0-2) are outputs. According to a block commutation table (**table 6-9**), the outputs CCx are put either to a low or high state while the outputs COUTx are switched to the PWM signal which is generated by the 10-bit compare timer 2 (COMP unit).

For monitoring of sensor input signal timing in block commutation mode, the signal transitions at $\overline{INT0\text{-}2}$ can also generate an interrupt (if enabled) and a capture event at channel 0 of the CAPCOM unit (compare timer 1). For emergency cases (trap function of $\overline{CTRAP}$ input signal) the six outputs CCx and COUTx can be put selectively to its inactive phase (COINI).

At the multi-channel PWM modes of the C504, a change of the PWM output states (active or inactive) is triggered by compare timer 1, which is running either in operating mode 0 or 1. If its count value reaches 0000_H, the PWM output signal changes its state according to a well defined state table. The multi-channel PWM modes are split up into three modes:

– 4-phase multi-channel PWM mode (4 PWM output signals)
– 5-phase multi-channel PWM mode (5 PWM output signals)
– 6-phase multi-channel PWM mode (6 PWM output signals)

6.3.4.1 Control Register BCON

The BCON register controls the selection of multi-channel PWM modes. It also contains the block commutation interrupt enable and status bit/flag.

Special Function Register BCON (Address $D7_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	7	6	5	4	3	2	1	0	
$D7_H$	BCMP BCEM	PWM1	PWM0	EBCE	BCERR	BCEN	BCM1	BCM0	BCON

Bit	Function
BCMP	In multi-channel PWM mode : Machine polarity If BCMP is set and multi-channel PWM mode is selected (PWM1,0 ≠ 0,0), all enabled compare outputs COUTx and CCx are switched to the compare timer 2 output signal during their active phase. If BCMP is cleared, only the COUTx outputs are switched to the compare timer 2 output signal during the active phase in multi-channel PWM mode. CMSELx3 must be set for that functionality.
BCEM	In block commutation mode : Error mode select bit If BCEM is set in block commutation mode, in rotate right or rotate left mode additionally a “wrong follower“ condition causes the setting of BCERR if EBCE is set.

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>PWM1
PWM0</td><td>Multi-channel PWM mode selection
These bits select the operating mode of the multi-channel PWM modes.
<table>
<tr><th>PWM1</th><th>PWM0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Block commutation mode (for hall sensor inputs)</td></tr>
<tr><td>0</td><td>1</td><td>4-phase multi-channel PWM mode</td></tr>
<tr><td>1</td><td>0</td><td>5-phase multi-channel PWM mode</td></tr>
<tr><td>1</td><td>1</td><td>6-phase multi-channel PWM mode</td></tr>
</table></td></tr>
<tr><td>EBCE</td><td>Enable interrupt of block commutation mode error
If EBCE is set, the emergency interrupt for a block commutation mode error condition of the CCU is enabled. In block commutation mode, an emergency error condition occurs if a false signal state at $\overline{INT2}$ - $\overline{INT0}$ or a wrong follower state (if selected by bit BCEM) is detected (see also table 6-9).</td></tr>
<tr><td>BCERR</td><td>Block commutation mode error flag
In block commutation mode BCERR is set in rotate right or rotate left mode if after a transition at $\overline{INTx}$ all $\overline{INTx}$ inputs are at high or low level. Additionally, in rotate right or rotate left mode a “wrong follower“ condition according table 6-9 can cause the setting of BCERR (see description of bit BCEM).
If the block commutation interrupt is enabled (EBCE=1), the setting of BCERR will generate a CCU emergency interrupt. BCERR must be reset by software.</td></tr>
<tr><td>BCEN</td><td>Block commutation enable
If BCEN is set, the multi-channel PWM modes of the CAPCOM unit as selected by the bits PWM1/PWM0 are enabled for operation. Before BCEN bit is set, all required PWM compare outputs should be programmed to operate as compare outputs by writing the registers CMSEL1/CMSEL0.</td></tr>
<tr><td>BCM1
BCM0</td><td>Multi-channel PWM mode output pattern selection
Additionally to bits PWM1 and PWM0, these two control bits select the output signal pattern in all multi-channel PWM modes. The detailed signal pattern information is given in table 6-9 to table 6-12.
<table>
<tr><th>BCM1</th><th>BCM0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Idle mode</td></tr>
<tr><td>0</td><td>1</td><td>Rotate right mode</td></tr>
<tr><td>1</td><td>0</td><td>Rotate left mode</td></tr>
<tr><td>1</td><td>1</td><td>Slow down mode</td></tr>
</table></td></tr>
</table>

Note : When a multi-channel PWM mode is initiated the first time after reset, BCON must be written twice : first write operation with bit BCEN cleared and all other bits set/cleared as required (BCM1,0´must be 0,0 for idle mode), followed by a second write operation with the same BCON bit pattern of the first write operation but with BCEN set. After this second BCON write operation, compare timer 1 can be started (setting CT1R in CT1CON) and thereafter BCM1,0 can be put into another mode than idle mode.

6.3.4.2 Signal Generation in Multi-Channel PWM Modes

The multi-channel PWM modes of the C504 use the pins CCx and COUTx for compare output signal generation. Before signal generation of a multi-channel PWM mode can be started, the COINI register should be programmed with the logic value of the multi-channel PWM inactive phase. After this, the output pins which are required for the multi-channel PWM signal generation must be programmed to operate as compare outputs by writing the mode select registers CMSEL0 and CMSEL1. **Table 6-8** shows the CMSEL0/CMSEL1 register bits which are required for the full operation of the multi-channel PWM modes.

Table 6-8
Programming of Multi-Channel PWM Compare Outputs

Multi-Channel PWM Mode	CMSEL1	CMSEL0
Block commutation / 6-phase multi-channel PWM	XXXX $Y011_B$	Y011 $Y011_B$
5-phase multi-channel PWM		Y010 $Y011_B$
4-phase multi-channel PWM		Y010 $Y001_B$

Note : The abbreviation “X“ means don’t care. The abrevation “Y“ (bit CMSELx.3) represents the burst mode bit. If Y=0 the signal generation at the COUTx pins is controlled by compare timer 1. If Y=1 the signal generation at the COUTx pins is also controlled by compare timer 1 but modulated by compare timer 2.

Output signals during the active phase

An active phase of a compare output signal in multi-channel PWM mode can be controlled either by the CAPCOM unit (compare timer 1) and/or modulated by compare timer 2. The selection is done by bit CMSELx.3 (see note below **table 6-8**).

Figure 6-29 shows the different possibilities for controlling the active phase of a compare output signal using compare timer 1. Compare timer 1 may operate either in mode 0 or mode 1. In multuí-phase mode, the block commutation logic switches from one state to the next state when compare timer 1 reaches the value 0000_H. As an active phase lasts always two states, the duration of an active phase is determined by compare timer 1 reaching 0000_H twice.

As shown in **figure 6-29a**, a compare output signal CCx or COUTx of a CAPCOM channel is either at low or high level during the whole active phase when the value stored in the compare timer 1 offset registers (CT1OFH, CT1OFL) and the value stored in its compare registers (CCHx, CCLx) is equal 0000_H. When the compare value is not equal 0000_H and less or equal the period value, the active phase of the related compare output signal CCx or COUTx is controlled by the CAPCOM unit as shown in **figure 6-29b**.

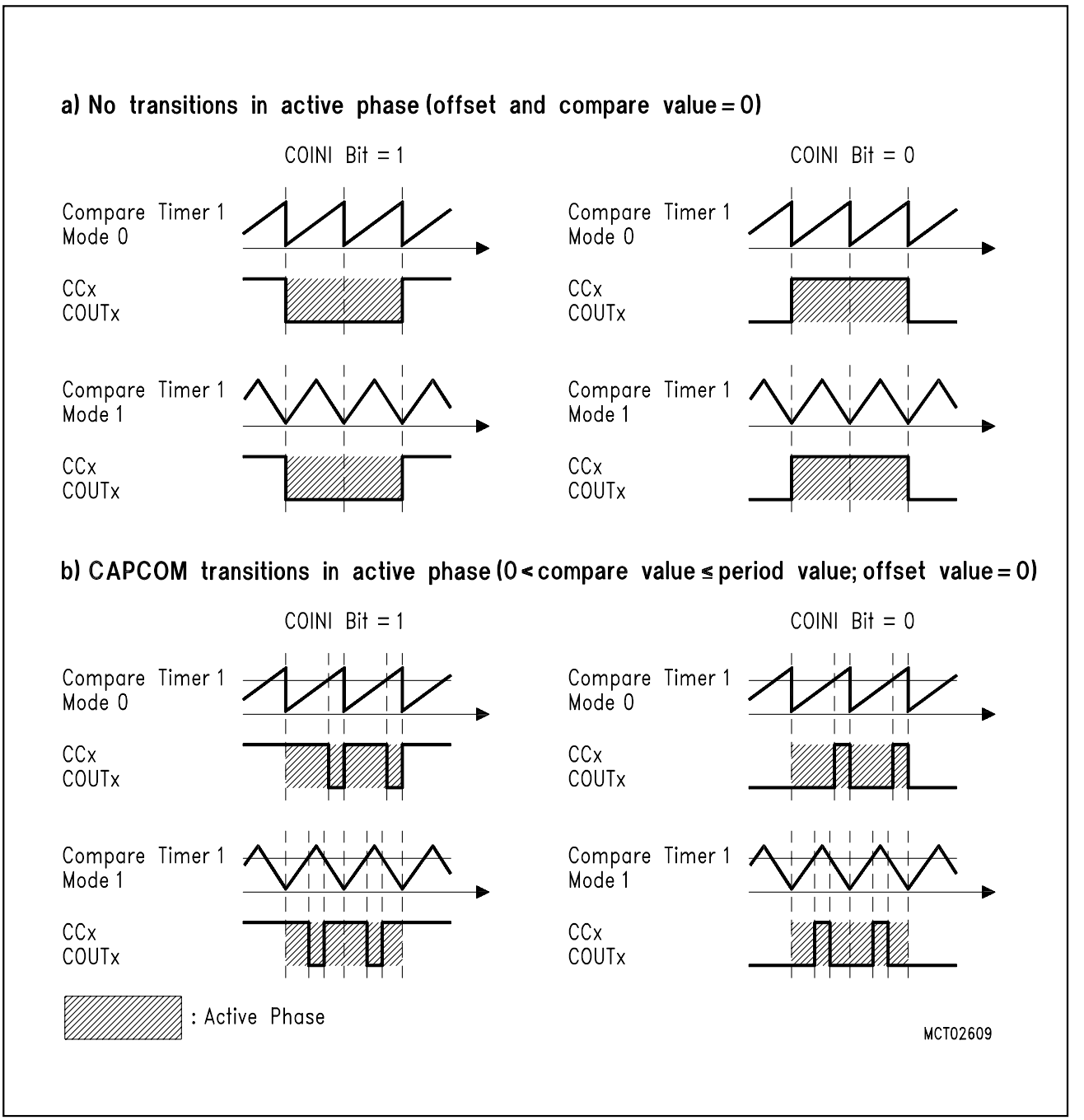


Figure 6-29
Compare Timer 1 Controlled Active Phase of the Multi-Channel PWM Modes (with CMSELx.3 = 0)

Figure 6-30 shows the different possibilities for controlling the active phase of a compare output signal using compare timer 2. In this operating mode, which is selected when bit CMSELx.3 is set, the compare timer 2 output signal is switched to the COUTx or CCx outputs during the active phase of a multi-channel PWM signal. Bit BCMP (BCON.7) defines whether only COUTx or COUTx and CCx are modulated by the compare timer 2 output signal.

Depending on the bits COUT3I and COUTXI of COINI, the polarity of COUT3 and the switched CCx/ COUTx active phase signal can be identical or inverted.

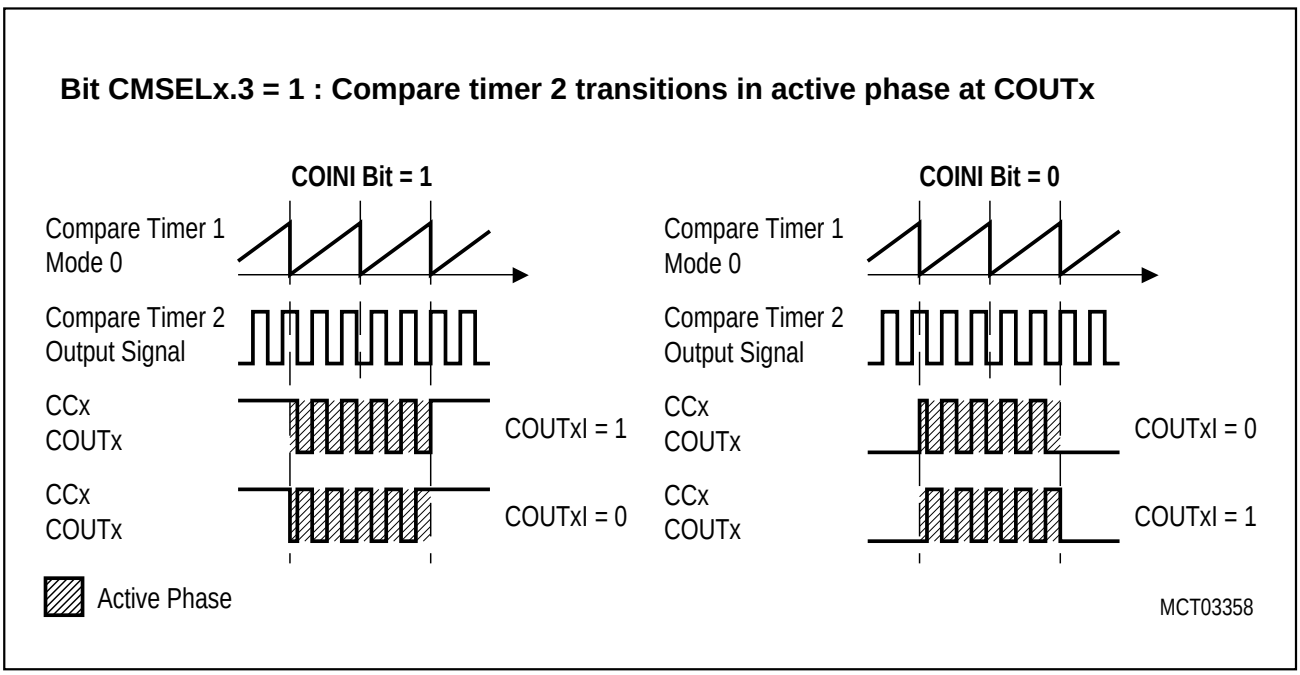


Figure 6-30
Compare Timer 2 Controlled Active Phase of the Multi-Channel PWM Modes (with CMSELx.3 = 1)

6.3.4.3 Block Commutation PWM Mode

In block commutation mode the $\overline{\text{INT0-2}}$ inputs are sampled once each processor cycle. If the input signal combination at $\overline{\text{INT0-2}}$ changes its state, the outputs CCx and COUTx are set to their new state according to **table 6-9**.

Table 6-9
Block Commutation Control Table

Mode (BCM1,BCM0)	$\overline{\text{INT0}}$ - $\overline{\text{INT2}}$ Inputs			CC0 - CC2 Outputs			COUT0 - COUT2 Outputs		
	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	CC0	CC1	CC2	COUT0	COUT1	COUT2
Rotate left 1) Rotate right 1)	0	0	0	inactive	inactive	inactive	inactive	inactive	inactive
	1	1	1	inactive	inactive	inactive	inactive	inactive	inactive
Rotate left	1	0	1	inactive	inactive	active	active	inactive	inactive
	1	0	0	inactive	active	inactive	active	inactive	inactive
	1	1	0	inactive	active	inactive	inactive	inactive	active
	0	1	0	active	inactive	inactive	inactive	inactive	active
	0	1	1	active	inactive	inactive	inactive	active	inactive
	0	0	1	inactive	inactive	active	inactive	active	inactive
Rotate right	1	1	0	active	inactive	inactive	inactive	active	inactive
	1	0	0	active	inactive	inactive	inactive	inactive	active
	1	0	1	inactive	active	inactive	inactive	inactive	active
	0	0	1	inactive	active	inactive	active	inactive	inactive
	0	1	1	inactive	inactive	active	active	inactive	inactive
	0	1	0	inactive	inactive	active	inactive	active	inactive
Slow down	X	X	X	inactive	inactive	inactive	active	active	active
Idle 2)	X	X	X	inactive	inactive	inactive	inactive	inactive	inactive

1) If one of these two combinations of $\overline{\text{INTx}}$ signals is detected in rotate left or rotate right mode, bit BCERR flag is set. If enabled, a CCU emergency interrupt can be generated. When these states (error states) are reached, immediately idle state is entered.

2) Idle state is also entered when a “wrong follower“ is detected (if bit BCON.7=BCEM is set). When idle state is entered, the BCERR flag is always set. Idle state can only be left when the BCERR flag is reset by software.

In block commutation mode CAPCOM channel 0 is automatically configured for capture mode. In block commutation mode any signal transition at $\overline{\text{INT0-2}}$ generates a capture pulse for CAPCOM channel 0 (CCH0/CCL0) independently on the selected $\overline{\text{INT0-2}}$ signal transition type (rising or falling edge) as defined in the SFR ITCON. SFR ITCON can be used to generate additional interrupts at an $\overline{\text{INT0-2}}$ signal transition.

Figure 6-31 gives an example of a block commutation mode timing (only COUTx outputs are modulated with compare timer 2 output signal). It shows the rotate left case (BCM1,BCM0 = 1,0) and rotate right case (BCM1,BCM0 = 0,1). For the timing shown in **figure 6-31** the COINI register is set to $XX111111_B$. This means that a high level is defined as inactive phase. The CMSELx.3 bits in the CMSEL0/CMSEL1 registers must also be set (compare timer 2 switched to COUTx during active phase). The timing shown below is directly derived from **table 6-9**.

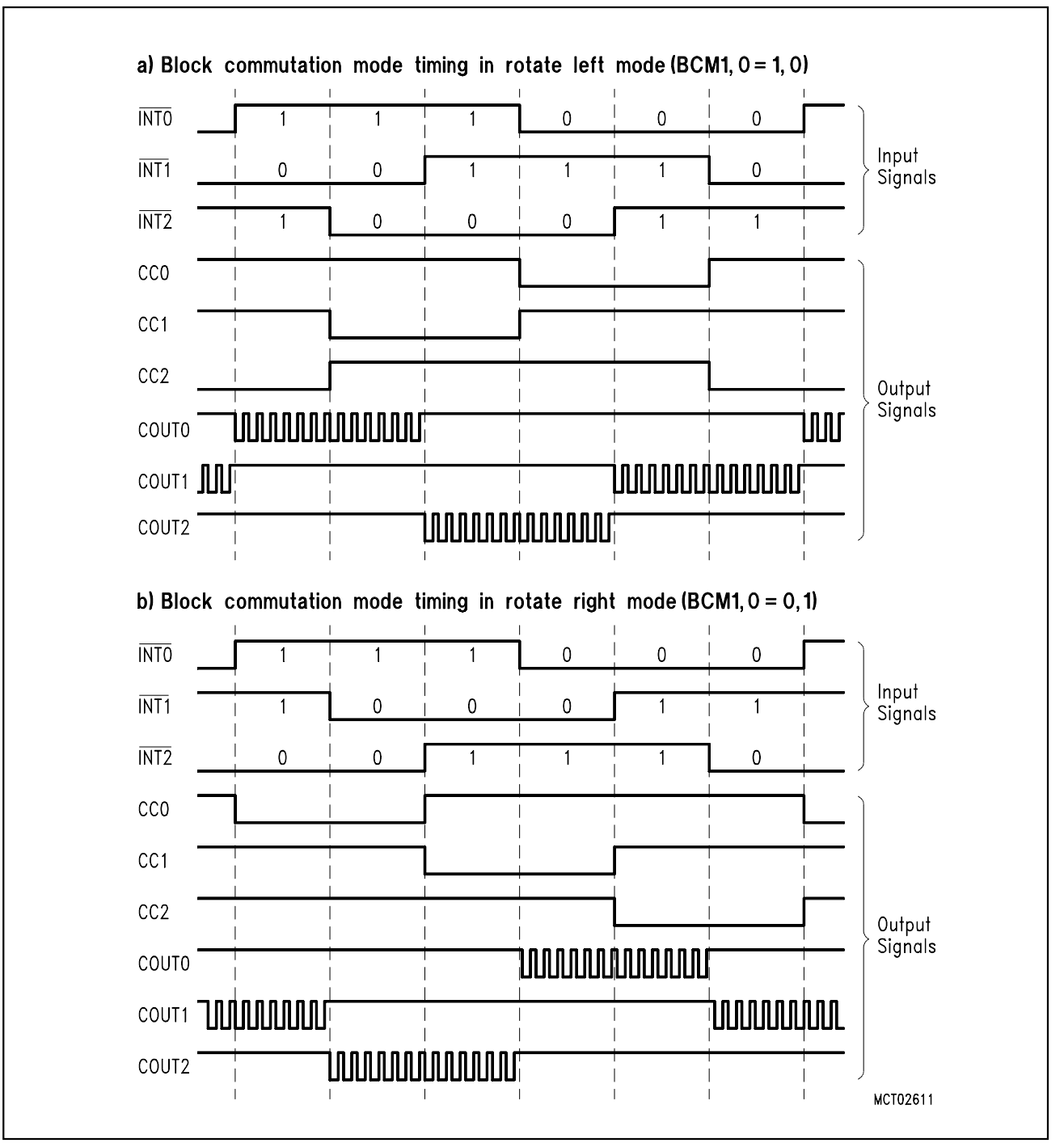


Figure 6-31
Block Commutation Mode Timing

6.3.4.4 Compare Timer 1 Controlled Multi-Channel PWM Modes

Using the multi-channel PWM modes of the C504, several compare timer 1 controlled PWM waveforms can be generated:

- 4-phase multi-channel PWM waveforms
- 5-phase multi-channel PWM waveforms
- 6-phase multi-channel PWM waveforms

The basic waveforms of these three compare timer 1 controlled PWM modes are shown the following three **figures 6-32** to **6-34**. The figures show waveforms for different COINI values with the resulting active/inactive phases and rotate right / rotate left condition. All three figures assume that compare timer 1 operates with 100% duty cycle (compare and offset registers = 0000_H) and without compare timer 2 modulation. Compare timer 1 duty cycles less than 100% or compare timer 2 modulation in the multi-channel PWM modes are shown in **figures 6-29** and **6-30**.

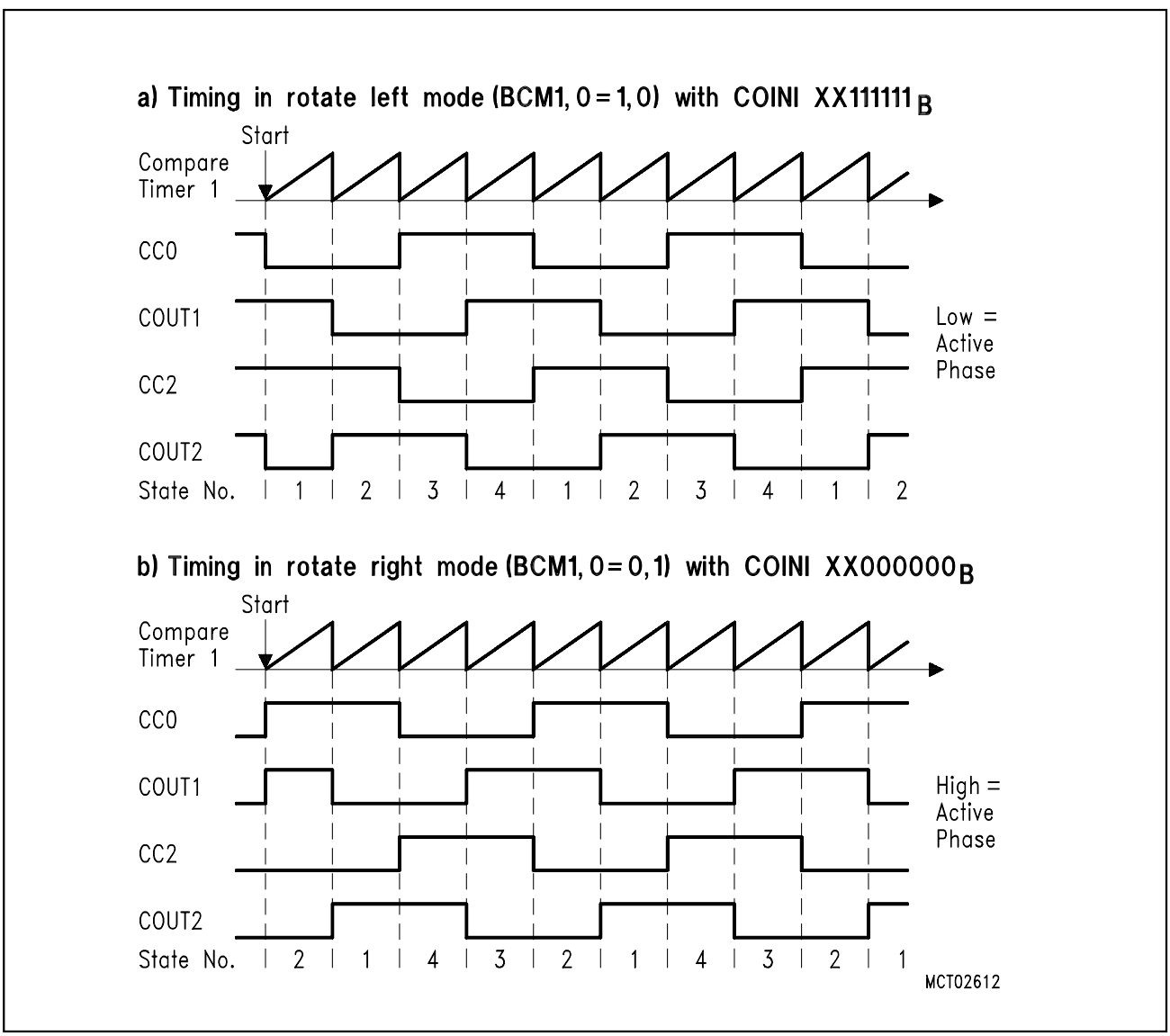


Figure 6-32
Basic Compare Timer 1 Controlled 4-Phase PWM Timing

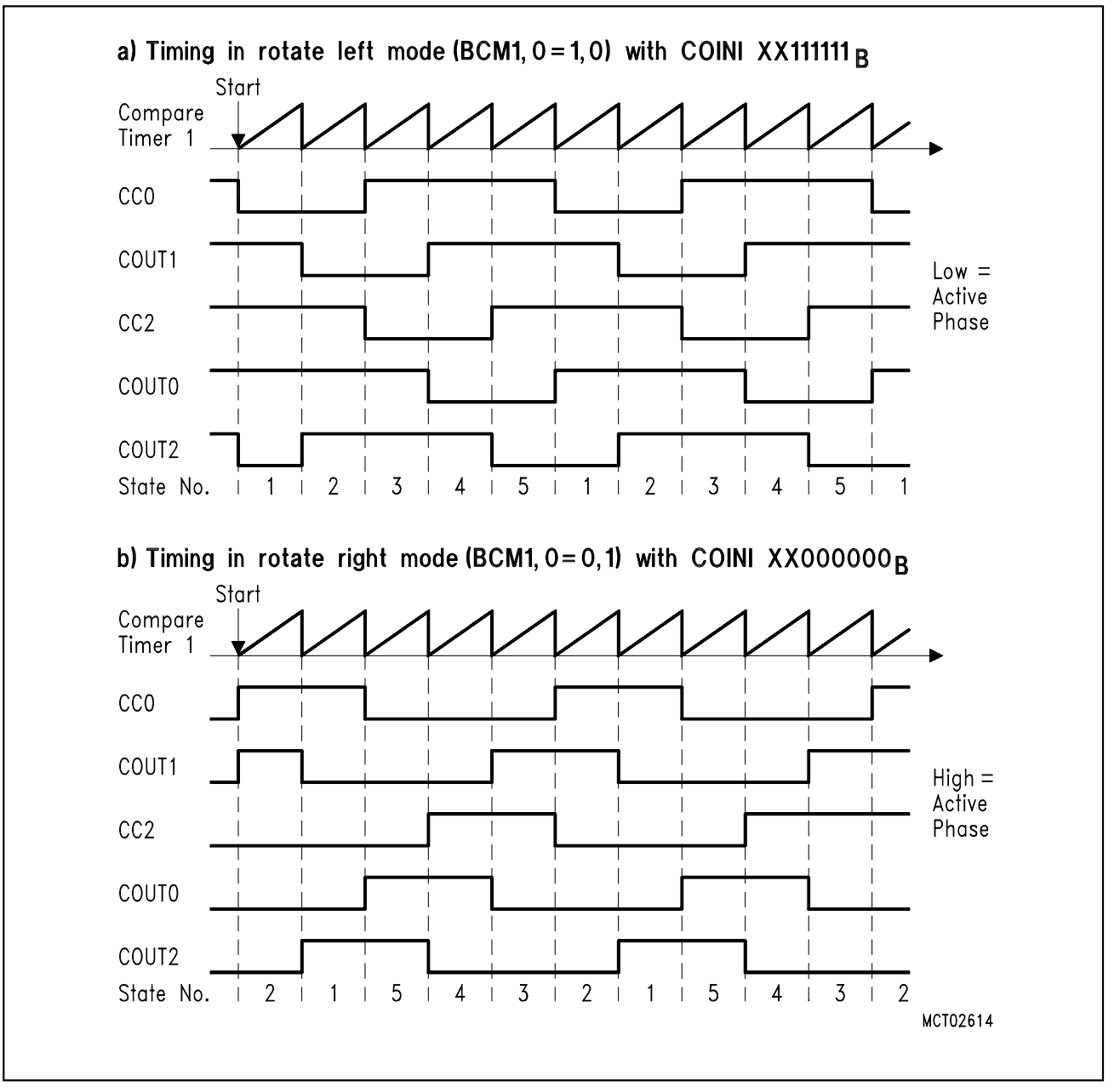


Figure 6-33
Basic Compare Timer 1 Controlled 5-Phase PWM Timing

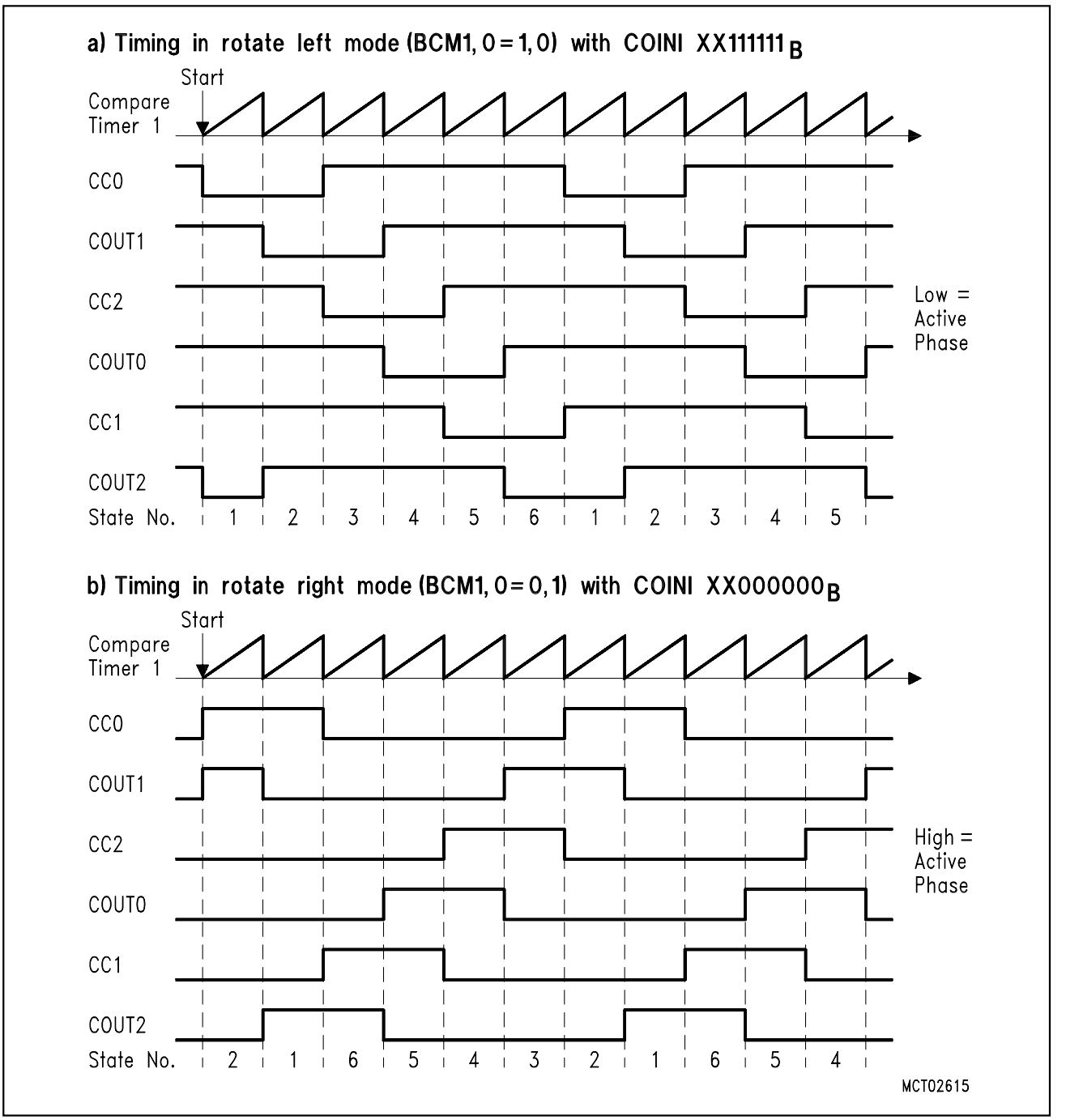


Figure 6-34
Basic Compare Timer 1 Controlled 6-Phase PWM Timing

Table 6-10 to **6-12** show as state tables the basic signal pattern definitions of the three multi-channel PWM modes. They also include the information of the slow down mode and the idle mode (bits BMC1,0 = 0,0 and 1,1).

Table 6-10
4-Phase PWM Timing State Table

Actual State and PWM Phase					Follower State (No.)			
No.	**Output Signals**				**BCM1, BCM0 =**			
	CC0	**COUT1**	**CC2**	**COUT2**	**0, 1**	**1, 0**	**0, 0**	**1, 1**
0	inactive	inactive	inactive	inactive	2	1	0	5
1	active	inactive	inactive	active	4	2	0	5
2	active	active	inactive	inactive	1	3	0	5
3	inactive	active	active	inactive	2	4	0	5
4	inactive	inactive	active	active	3	1	0	5
5	inactive	active	inactive	active	2	1	0	5

Note: In the inactive phase the PWM outputs drive a logic state as defined by the related bits in register COINI. During the active phase, the PWM outputs can be modulated by CT1 and/or CT2.

Table 6-11
5-Phase PWM Timing State Table

Actual State and PWM Phase						Follower State (No.)			
No.	**Output Signals**					**BCM1, BCM0 =**			
	CC0	**COUT1**	**CC2**	**COUT0**	**COUT2**	**0, 1**	**1, 0**	**0, 0**	**1, 1**
0	inactive	inactive	inactive	inactive	inactive	2	1	0	6
1	active	inactive	inactive	inactive	active	5	2	0	6
2	active	active	inactive	inactive	inactive	1	3	0	6
3	inactive	active	active	inactive	inactive	2	4	0	6
4	inactive	inactive	active	active	inactive	3	5	0	6
5	inactive	inactive	inactive	active	active	4	1	0	6
6	inactive	active	inactive	active	active	2	1	0	6

Note: In the inactive phase the PWM outputs drive a logic state as defined by the related bits in register COINI. During the active phase, the PWM outputs can be modulated by CT1 and/or CT2.

Table 6-12
6-Phase PWM Timing State Table

Actual State and PWM Phase							Follower State (No.)			
No.	Output Signals						BCM1, BCM0 =			
	CC0	COUT1	CC2	COUT0	CC1	COUT2	0, 1	1, 0	0, 0	1, 1
0	inactive	inactive	inactive	inactive	inactive	inactive	2	1	0	7
1	active	active	inactive	inactive	inactive	inactive	5	2	0	7
2	inactive	active	active	inactive	inactive	inactive	1	3	0	7
3	inactive	inactive	active	active	inactive	inactive	2	4	0	7
4	inactive	inactive	inactive	active	active	inactive	3	5	0	7
5	inactive	inactive	inactive	inactive	active	active	4	6	0	7
6	active	inactive	inactive	inactive	inactive	active	5	1	0	7
7	inactive	active	inactive	active	inactive	active	2	1	0	7

Note: In the inactive phase the PWM outputs drive a logic state as defined by the related bits in register COINI. During the active phase, the PWM outputs can be modulated by CT1 and/or CT2.

6.3.4.5 Software Controlled State Switching in Multi-Channel PWM Modes

In the 4-/5-/6-phase multi-channel PWM modes, the compare timer 1 overflow controlled switching of the follower state can be switched off. Instead of the compare timer 1 overflow, a setting of bit NMCS in SFR CMSEL1 selects the follower state, which is defined in the **tables 6-10** to **6-12**. Bit ESMC in SFR CMSEL1 enables the software controlled state switching.

If this software controlled 4-/5-/6-phase multi-channel PWM mode generation is selected, the compare timer 1 can be used for PWM signal generation (compare mode) in order to modulate the outputs. It can be further used for example for timer based interrupt generation. The waveforms of a PWM output signal in the multi-channel PWM modes can be selected as shown in **figure 6-29** (static low or high during active phase) or as shown in **figure 6-30** (compare timer 2 controlled modulation during active phase).

Figure 6-35 shows for the 5-pole PWM timing the possible waveforms of the active phase when the software controlled state switching in the multi-channel PWM modes is selected.

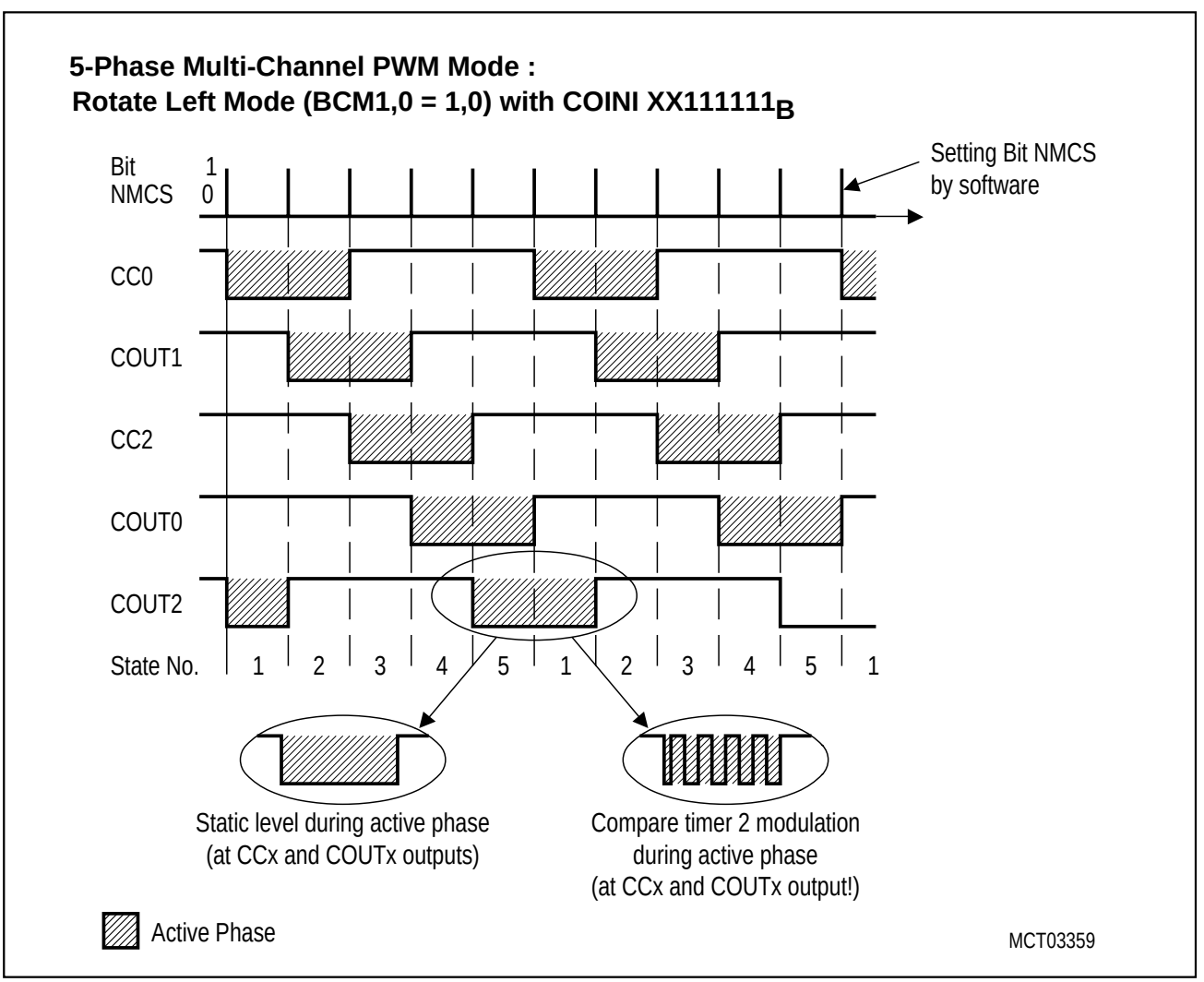


Figure 6-35
Software Controlled State Switching in 5-Phase Multi-Channel PWM Mode

Static level during active phase :

When bit ESMC in SFR CMSEL1 is set, static active or passive output levels during the active phase of a multi-phase PWM timing are generated when the following conditions are met :

- The 16-bit offset register of compare timer 1 must be 0000_H (CT1OFH = CT1OFL = 00_H)
- static active : compare values = 0000_H
  Static passive : compare values > period value
- The bits CMSELx3 (x=0-2) in the SFRs CMSEL0/CMSEL1 must be 0.

The logic state of the inactive/active phases at the CCx and COUTx outputs is defined by the bits in SFR COINI.

Compare timer 2 controlled active phase at COUTx :

When bit ESMC in SFR CMSEL1 is set, compare timer 2 controlled output levels at COUTx during the active phase of a multi-pole PWM timing are generated when the following conditions are met :

- The 16-bit offset register of compare timer 1 must be 0000_H (CT1OFH = CT1OFL = 00_H)
- The 16-bit capture/compare registers must be 0000_H
  (CCL0 = CCH0 = CCL1 = CCH1 = CCL2 = CCH2 = 00_H)
- Bits CMSELx3 (x=0-2) in the SFRs CMSEL0/CMSEL1 must be set
- Compare timer 2 must be enabled and initialized for compare output signal generation

Both, the CCx and the COUTx outputs can be controlled by compare timer 2.

A combination of outputs modulated by compare timer 1 and/or compare timer 2 is supported.

6.3.4.6 Trap Function in Multi-Channel Block Commutation Mode

The trap function in the block commutation mode operates comparable to the trap function as described in **chapter Table 6.3.2.7, “Trap Function of the CAPCOM Unit in Compare Mode,” on page 44**. But there is one difference : when $\overline{\text{CTRAP}}$ becomes inactive (high), the CCx and COUTx outputs are again switched back to the PWM pulse generation when compare timer 2 reaches the count value 000_H (instead of compare timer 1 in all other modes).

All other trap functions of the multi-channel PWM modes are identical as described in **chapter 6.3.2.7**.

6.4 Serial Interface (USART)

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at special function register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes (one synchronous mode, three asynchronous modes):

Mode 0, Shift Register (Synchronous) Mode:

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 data bits are transmitted/ received: (LSB first). The baud rate is fixed at $^1/_{12}$ of the oscillator frequency. (See section 6.3.3 for more detailed information)

Mode 1, 8-Bit USART, Variable Baud Rate:

10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in special function register SCON. The baud rate is variable. (See section 6.3.4 for more detailed information)

Mode 2, 9-Bit USART, Fixed Baud Rate:

11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in SCON) can be assigned to the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either $^1/_{32}$ or $^1/_{64}$ of the oscillator frequency. (See section 6.3.5 for more detailed information)

Mode 3, 9-Bit USART, Variable Baud Rate:

11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable. (See section 6.3.5 for more detailed information)

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incomming start bit if REN = 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1. The serial interfaces also provide interrupt requests when a transmission or a reception of a frame has completed. The corresponding interrupt request flags for serial interface 0 are TI or RI, resp. See chapter 7 of this user manual for more details about the interrupt structure. The interrupt request flags TI and RI can also be used for polling the serial interface 0 if the serial interrupt is not to be used (i.e. serial interrupt 0 not enabled).

6.4.1 Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is beeing addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the incoming data bytes.

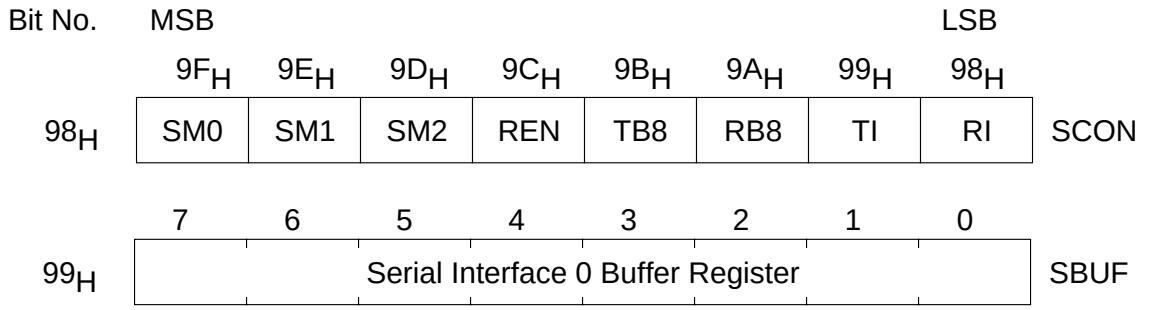
SM2 has no effect in mode 0, and in mode 1 can be used to check the validity of the stop bit. In a mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.4.2 Serial Port Registers

The serial port control and status register is the special function register SCON. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

SBUF is the receive and transmit buffer of serial interface 0. Writing to SBUF loads the transmit register and initiates transmission. Reading out SBUF accesses a physically separate receive register.

Special Function Register SCON (Address 98_H) **Reset Value : 00_H**
Special Function Register SBUF (Address 99_H) **Reset Value : XX_H**



Bit	Function
SM0 SM1	Serial port 0 operating mode selection bits

SM0	SM1	Selected operating mode
0	0	Serial mode 0 : Shift register, fixed baud rate (f_{osc}/12)
0	1	Serial mode 1 : 8-bit UART, variable baud rate
1	0	Serial mode 2 : 9-bit UART, fixed baud rate (f_{osc}/32 or f_{osc}/64)
1	1	Serial mode 3 : 9-bit UART, variable baud rate

SM2	Enable serial port multiprocessor communication in modes 2 and 3 In mode 2 or 3, if SM2 is set to 1 then RI0 will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0.
REN	Enable receiver of serial port 0 Enables serial reception. Set by software to enable serial reception. Cleared by software to disable serial reception.
TB8	Serial port transmitter bit 9 TB8 Is the 9th data bit that will be transmitted in modes 2 and 3. Set or cleared by software as desired.
RB8	Serial port receiver bit 9 In modes 2 and 3, RB8 is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Serial port transmitter interrupt flag TI is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. TI must be cleared by software.
RI	Serial port receiver interrupt flag RI0 is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (exception see SM2). RI must be cleared by software.

6.4.3 Baud Rates

There are several possibilities to generate the baud rate clock for the serial interface depending on the mode in which it is operated.

To clearify the terminology, something should be said about the differences between "baud rate clock" and "baud rate".

The serial interface requires a clock rate which is 16 times the baud rate for the internal synchronization. Therefore, the baud rate generators have to provide a "baud rate clock" to the serial interface which - there divided by 16 - results in the actual "baud rate". However, all formulas given in the following section are already include the factor and calculate the final baud rate.

The baud rate generation is further controlled by bit SMOD which is located in SFR PCON.

Special Function Register PCON (Address $87_{H)}$ **Reset Value : $000X0000_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
87_H	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE	PCON

The functions of the shaded bits are not described in this section.

Symbol	Function
SMOD	Baud rate double bit When set, the baud rate of the serial channel in mode 1,2,3 is doubled.

Mode 0

The baud rate in mode 0 is fixed:

Mode 0 baud rate = oscillator frequency/12 = $f_{OSC}/12$

Mode 2

The baud rate in mode 2 depends on the value of bit SMOD in special function register PCON (87_H). If SMOD = 0 (which is the value on reset), the baud rate is $f_{OSC}/64$. If SMOD = 1, the baud rate is $f_{OSC}/32$.

Mode 2 baud rate = $2^{SMOD}/64 \times (f_{OSC})$

Modes 1 and 3

The baud rates in mode1 and 3 are determined by the timer overflow rate. These baud rates can be determined by timer 1 or by timer 2 or by both (one for transmit and the other for receive).

6.4.3.1 Using Timer 1 to Generate Baud Rates

When timer 1 is used as the baud rate generator, the baud rates in modes 1 and 3 are determined by the timer 1 overflow rate and the value of SMOD as follows:

Modes 1,3 baud rate = $2^{SMOD}/32 \times$(timer 1 overflow rate)

The timer 1 interrupt should be disabled in this application. The timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD=0010B). In that case, the baud rate is given by the formula

Modes 1,3 baud rate = $2^{SMOD}/32 \times f_{OSC}/[12 \times (256 - TH1)]$

One can achieve very low baud rates with timer 1 by leaving the timer 1 interrupt enabled, and configuring the timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the timer 1 interrupt to do a 16-bit software reload.

Table 6-13 lists commonly used baud rates and how they can be obtained from timer 1.

Table 6-13
Timer 1 Generated Commonly Used Baud Rates

Baud Rate	f_{osc}	SMOD	Timer 1		
			C/T	Mode	Reload Value
Mode 0 max: 1 MHz	12 MHz	X	X	X	X
Mode 2 max: 375 K	12 MHz	1	X	X	X
Modes 1, 3: 62.5 K	12 MHz	1	0	2	FF_H
19.2 K	11.059 MHz	1	0	2	FD_H
9.6 K	11.059 MHz	0	0	2	FD_H
4.8 K	11.059 MHz	0	0	2	FA_H
2.4 K	11.059 MHz	0	0	2	$F4_H$
1.2 K	11.059 MHz	0	0	2	$E8_H$
110	6 MHz	0	0	2	72_H
110	12 MHz	0	0	1	$FEEB_H$

6.4.3.2 Using Timer 2 to Generate Baud Rates

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. Note then the baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts timer 2 into its baud rate generator mode, as shown in **figure 6-35**.

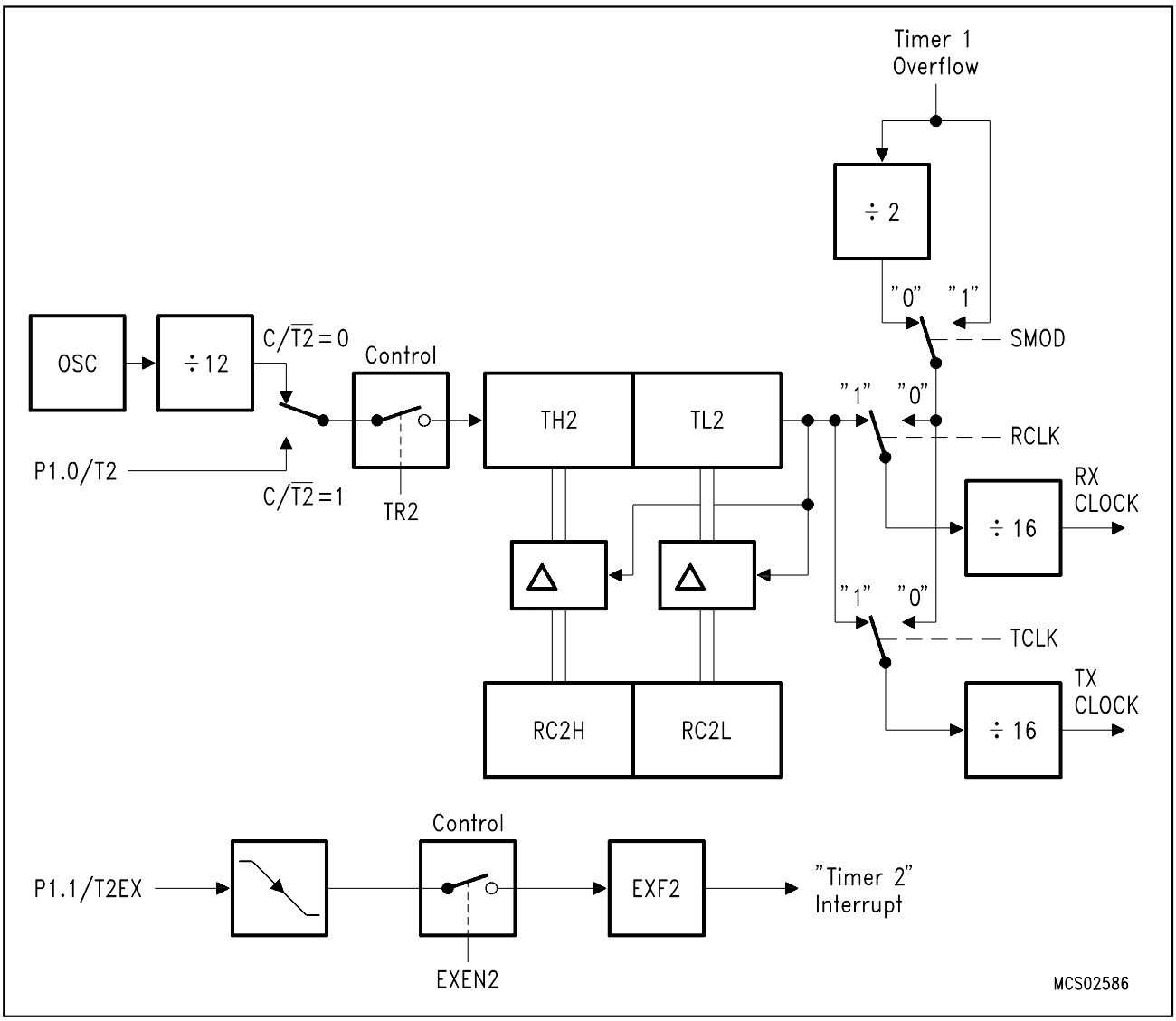


Figure 6-35
Timer 2 in Baud Rate Generator Mode

The baud rate generator mode is similar to the auto-reload mode, in that rollover in TH2 causes the timer 2 registers to be reloaded with the 16-bit value in registers RC2H and RC2L, which are preset by software.

Now the baud rates in modes 1 and 3 are determined by timer 2's overflow rate as follows:

Modes 1, 3 baud rate = timer 2 overflow rate/16

The timer can be configured for either "timer" or "counter" operation: In the most typical applications, it is configured for "timer" operation (C/T2 = 0). "Timer" operation is a little different for timer 2 when it's being used as a baud rate generator. Normally, as a timer it would increment every machine cycle (thus at $f_{OSC}/12$). As a baud rate generator, however, it increments every state time ($f_{OSC}/2$). In that case the baud rate is given by the formula

$$\text{Modes 1,3 baud rate} = f_{OSC}/32 \times [65536 - (\text{RC2H, RC2L})]$$

where (RC2H, RC2L) is the content of RC2H and RC2L taken as a 16-bit unsigned integer.

Note that the rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the timer 2 interrupt does not have to be disabled when timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX can be used as an extra external interrupt, if desired.

It should be noted that when timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the timer is being incremented every state time, and the results of a read or write may not be accurate. The RC registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the timer off (clear TR2) before accessing the timer 2 or RC registers, in this case.

6.4.4 Details about Mode 0

Serial data enters and exists through RXD. TXD outputs the shift clock. 8 data bits are transmitted/ received: (LSB first). The baud rate is fixed at $f_{OSC}/12$.

Figure 6-36a shows a simplyfied functional diagram of the serial port in mode 0. The associated timing is illustrated in **figure 6-36b**.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "WRITE to SBUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "WRITE to SBUF", and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0, and also enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1 and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift register are shifted to the right one position.

As data bits shift out to the right, zeroes come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initialy loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX control block to do one last shift and then deactivate SEND and set TI. Both of these actions occur at S1P1 of the 10th machine cycle after "WRITE to SBUF".

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX control unit writes the bits 1111 1110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bit comes in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared and RI is set.

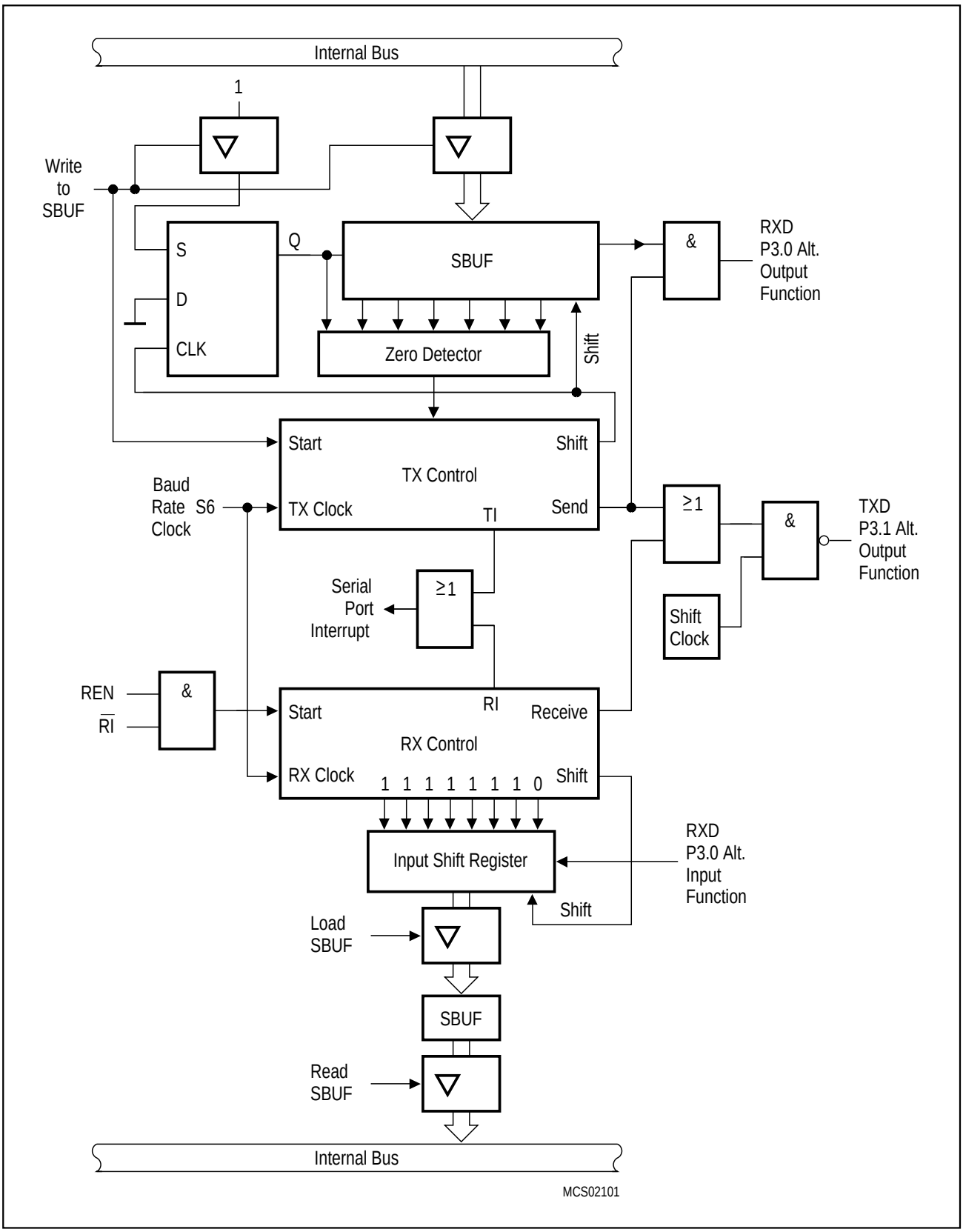


Figure 6-36a
Serial Interface, Mode 0, Functional Diagram

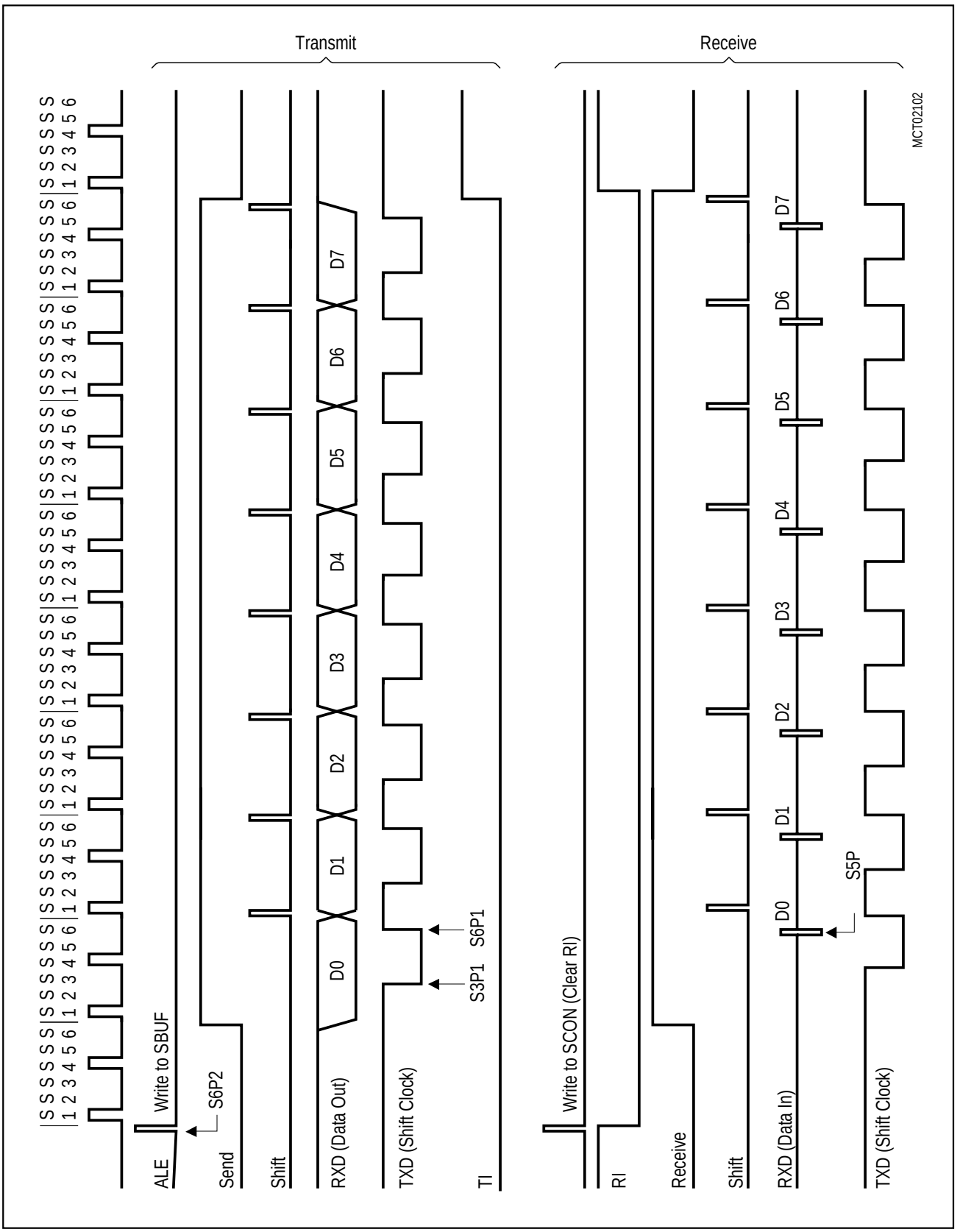


Figure 6-36b
Serial Interface, Mode 0, Timing Diagram

6.4.5 Details about Mode 1

Ten bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. The baud rate is determined either by the timer 1 overflow rate, or the timer 2 overflow rate, or both (one for transmit and the other for receive).

Figure 6-37a shows a simplified functional diagram of the serial port in mode 1. The assiociated timings for transmit receive are illustrated in **figure 6-37b**.

Transmission is initiated by an instruction that uses SBUF as a destination register. The "WRITE to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX control unit that a transmission is requested. Transmission starts at the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "WRITE to SBUF" signal).

The transmission begins with activation of $\overline{\text{SEND}}$, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeroes are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX control unit to do one last shift and then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the 10th divide-by-16 rollover after "WRITE to SBUF".

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and $1FF_H$ is written into the input shift register, and reception of the rest of the frame will proceed.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at latest 2 of the 3 samples. This is done for the noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection or false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register, (which in mode 1 is a 9-bit register), it flags the RX control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1) RI = 0, and
2) Either SM2 = 0, or the received stop bit = 1

If either of these two condtions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bit goes into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RXD.

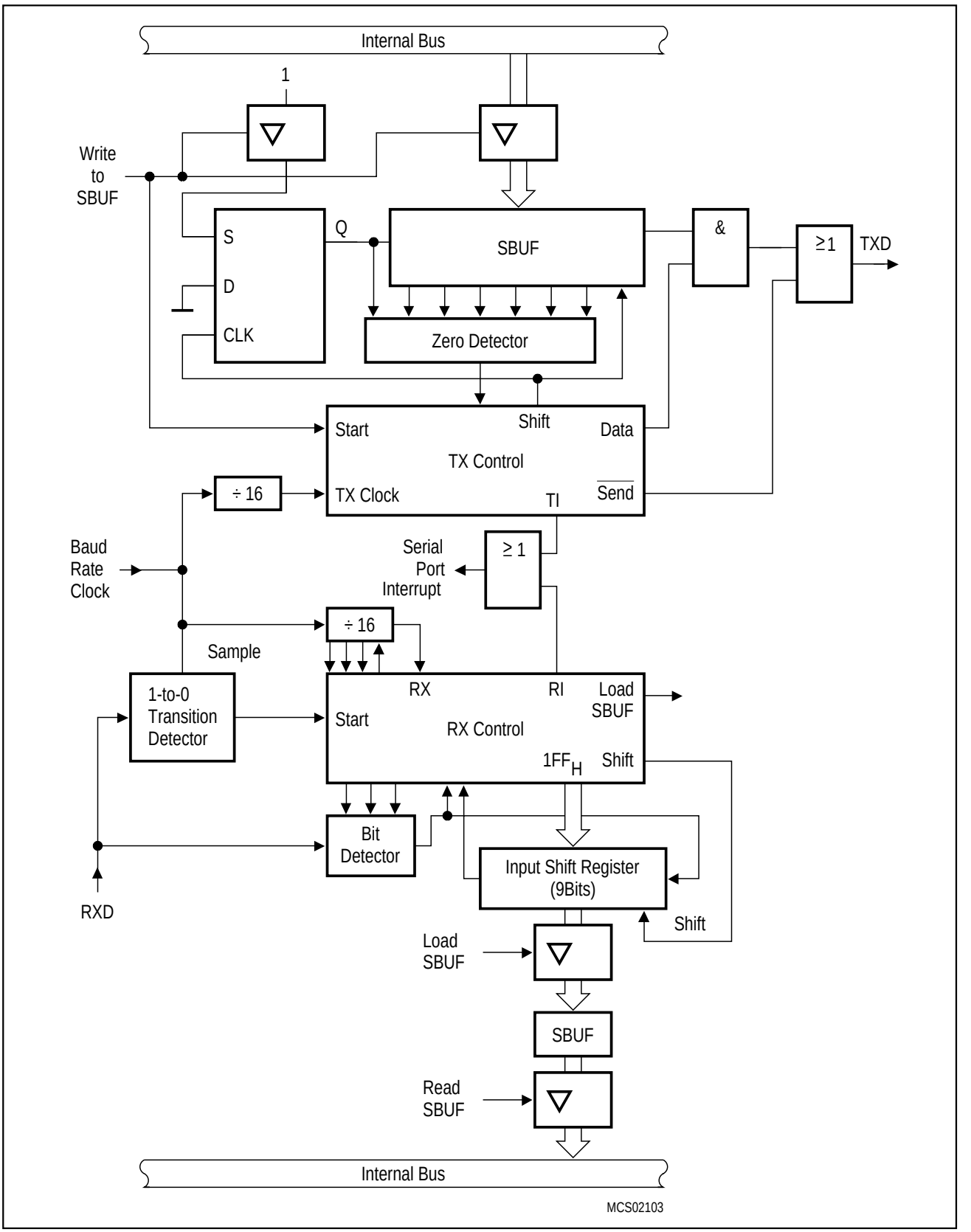


Figure 6-37a
Serial Interface, Mode 1, Functional Diagram

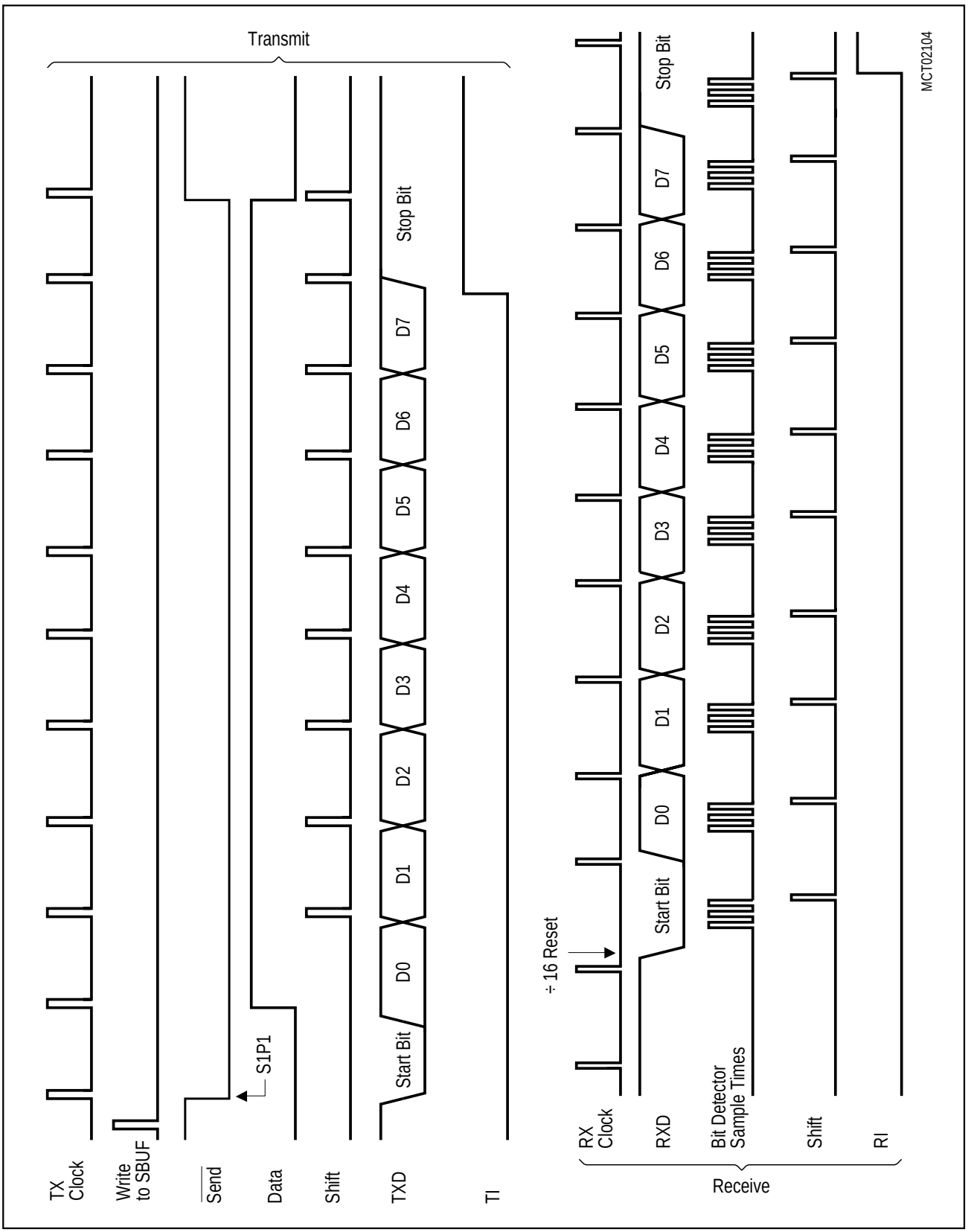


Figure 6-37b
Serial Interface, Mode 1, Timing Diagram

6.4.6 Details about Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in mode 2 (When bit SMOD in SFR PCON (87_H) is set, the baud rate is $f_{OSC}/32$). Mode 3 may have a variable baud rate generated from either timer 1 or 2 depending on the state of TCLK and RCLK (SFR T2CON).

Figure 6-38a shows a functional diagram of the serial port in modes 2 and 3. The receive portion is exactly the same as in mode 1. The transmit portion differs from mode 1 only in the 9th bit of the transmit shift register. The associated timings for transmit/receive are illustrated in **figure 6-38b**.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "WRITE to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX control unit that a transmission is requested. Transmission starts at the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "WRITE to SBUF" signal.)

The transmision begins with activation of SEND, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeroes are clocked in. Thus, as data bits shift out to the right, zeroes are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeroes. This conditon flags the TX control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after "WRITE to SBUF".

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and $1FF_H$ is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bit come from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in modes 2 and 3 is a 9-bit register), it flags the RX control block to do one last shift, load SBUF and RB8, and to set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

1) RI = 0, and
2) Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bit goes into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8 or RI.

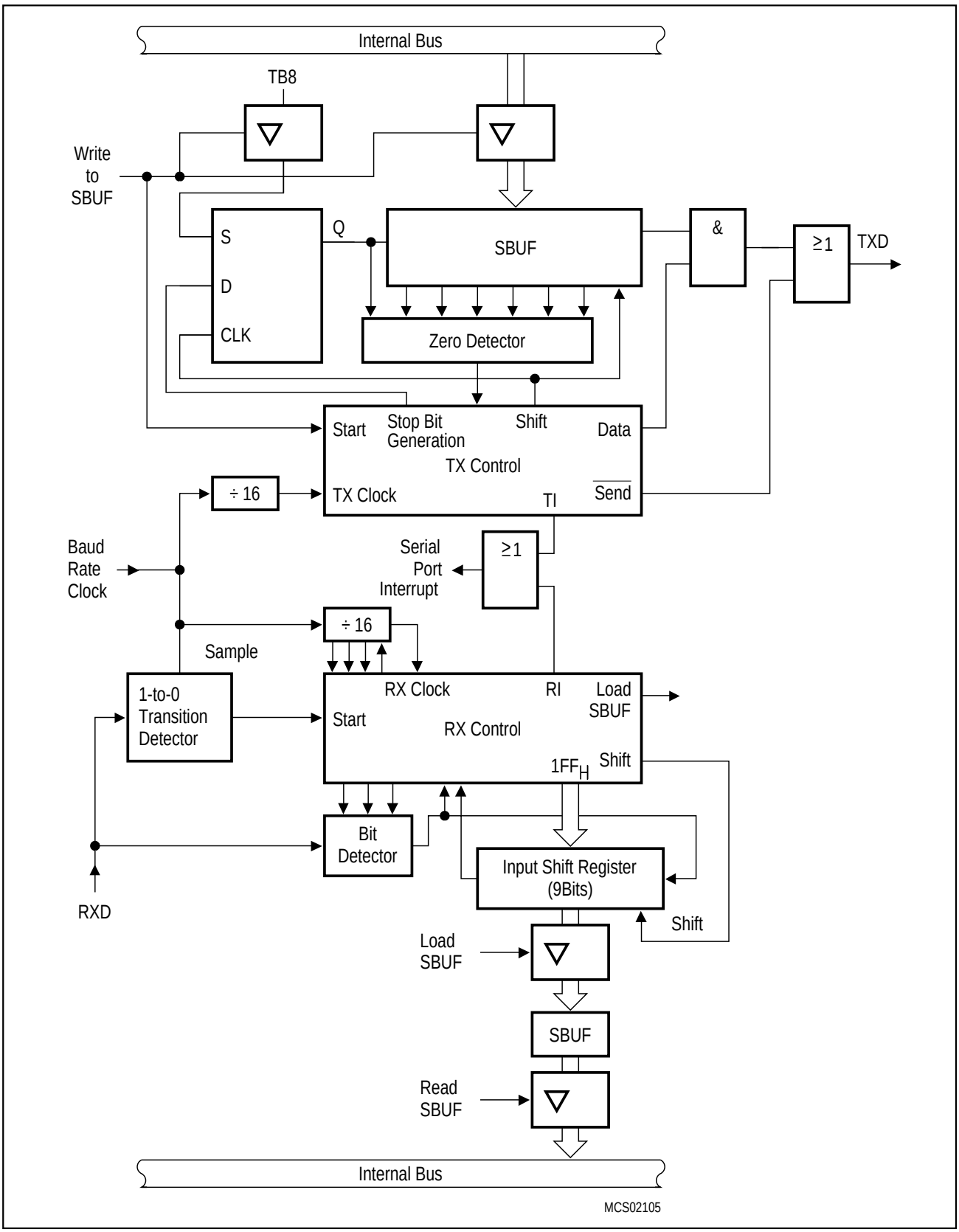


Figure 6-38a
Serial Interface, Mode 2 and 3, Functional Diagram

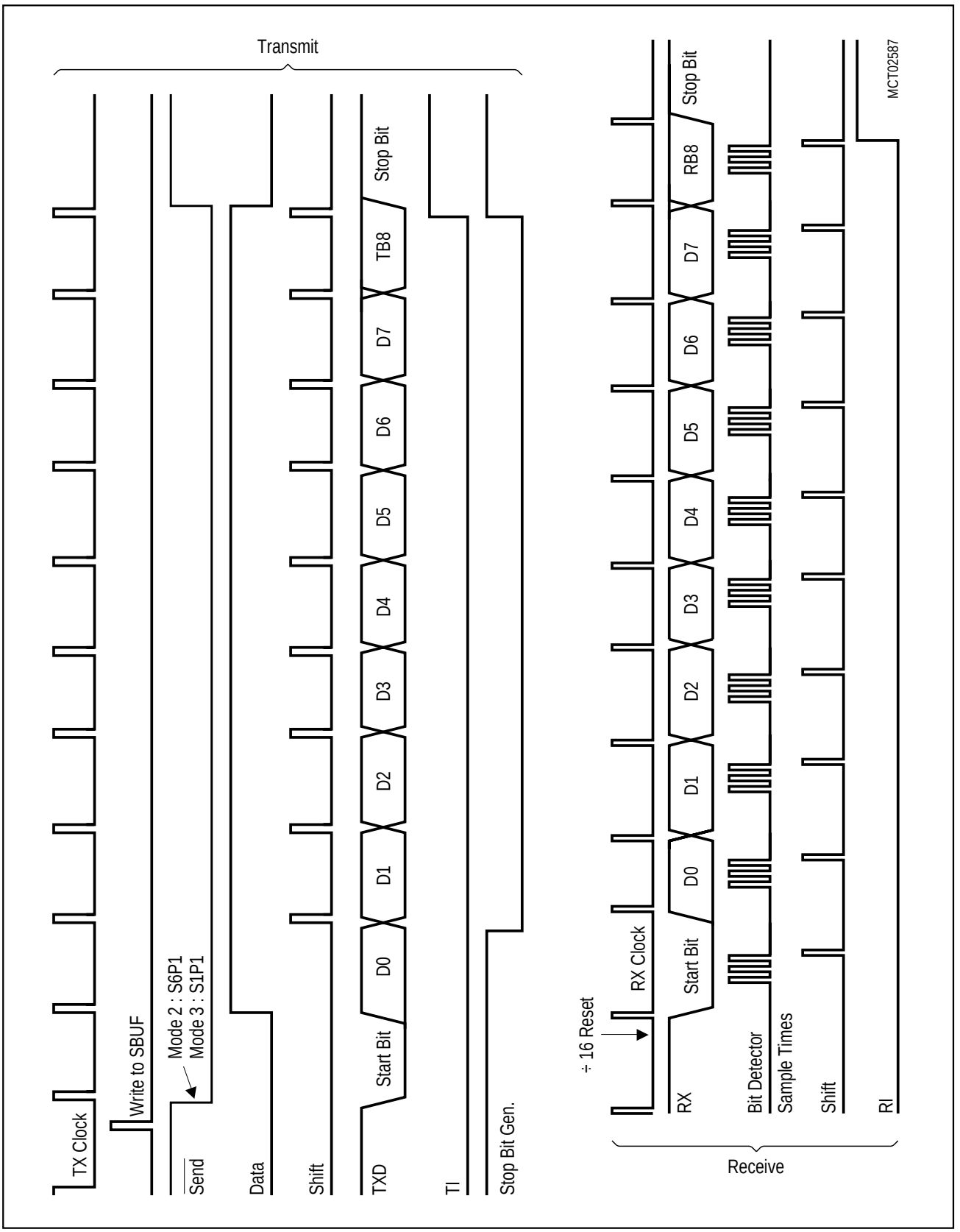


Figure 6-38b
Serial Interface, Mode 2 and 3, Timing Diagram

6.5 10-bit A/D Converter

The C504 includes a high performance / high speed 10-bit A/D-Converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 8 multiplexed input channels (port 1, 3), which can also be used as digital outputs/inputs
- 10-bit resolution
- Single or continuous conversion mode
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The externally applied reference voltage range has to be held on a fixed value within the specifications.The main functional blocks of the A/D converter are shown in **figure 6-39**.

6.5.1 A/D Converter Operation

An internal start of a single A/D conversion is triggered by a write-to-ADDATL instruction. The start procedure itself is independent of the value which is written to ADDATL. When single conversion mode is selected (bit ADM=0) only one A/D conversion is performed. In continuous mode (bit ADM=1), after completion of an A/D conversion a new A/D conversion is triggered automatically until bit ADM is reset.

The busy flag BSY (ADCON0.4) is automatically set when an A/D conversion is in progress. After completion of the conversion it is reset by hardware. This flag can be read only, a write has no effect. The interrupt request flag IADC (IRCON0.0) is set when an A/D conversion is completed.

The bits MX0 to MX2 in special function register ADCON0 and ADCON1 are used for selection of the analog input channel. The bits MX0 to MX2 are represented in both registers ADCON0 and ADCON1; however, these bits are present only once. Therefore, there are two methods of selecting an analog input channel: If a new channel is selected in ADCON1 the change is automatically done in the corresponding bits MX0 to MX2 in ADCON0 and vice versa.

Four lines of port 1 and 3 each are dual purpose input/output ports. These pins can be used either for digital I/O functions or as the analog inputs. If less than 8 analog inputs are required, the unused analog inputs at port 1 or 3 are free for digital I/O functions.

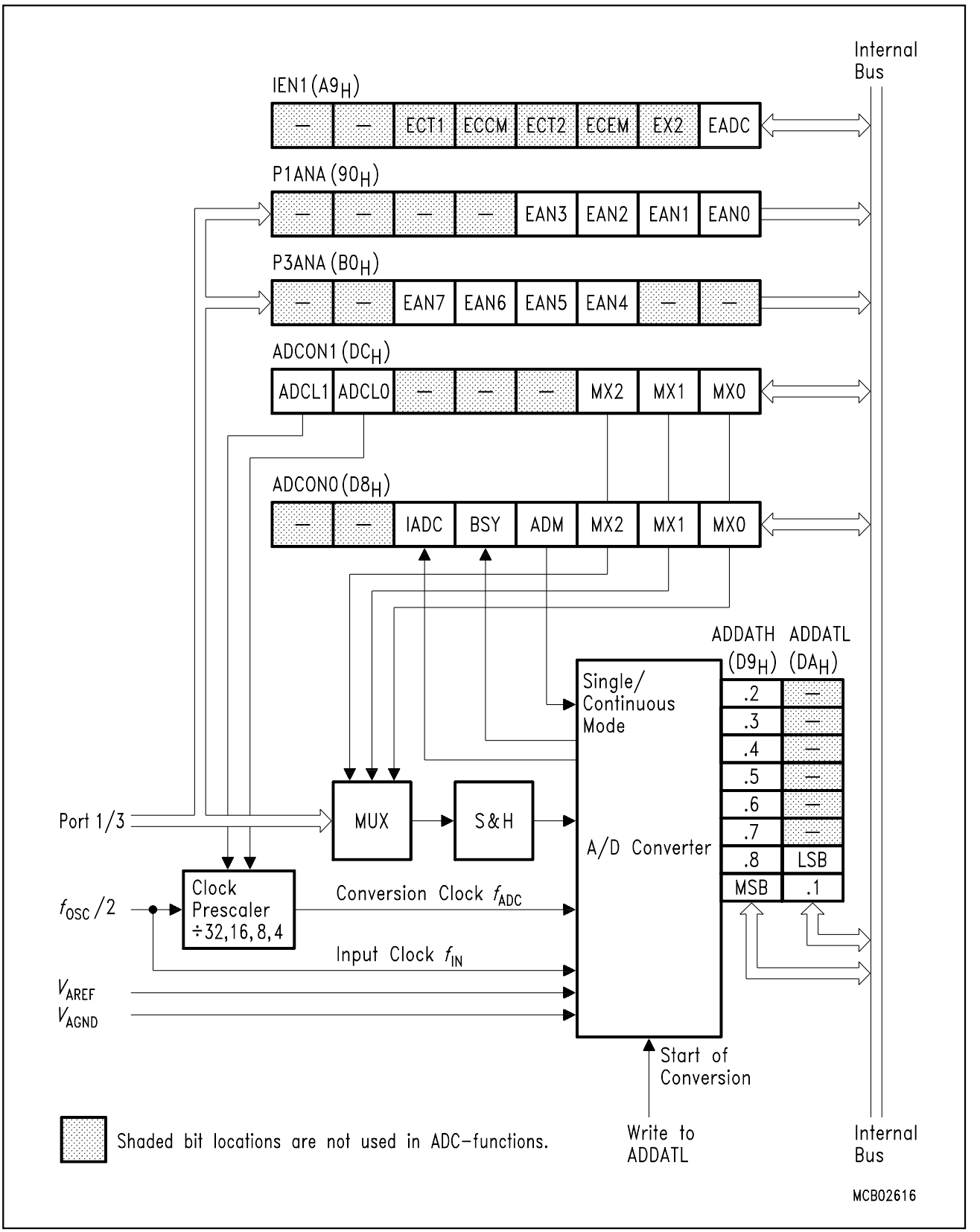


Figure 6-39
Block Diagram A/D Converter

6.5.2 A/D Converter Registers

This section describes the bits/functions of all registers which are used by the A/D converter.

Special Function Registers ADDATH (Address $D9_H$) **Reset Value : 00_H**
Special Function Registers ADDATL (Address DA_H) **Reset Value : $00XXXXXX_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D9_H$	MSB .9	.8	.7	.6	.5	.4	.3	.2	ADDATH
DA_H	.1	LSB .0	–	–	–	–	–	–	ADDATL

The registers ADDATH and ADDATL hold the 10-bit conversion result in left justified data format. The most significant bit of the 10-bit conversion result is bit 7 of ADDATH. The least significant bit of the 10-bit conversion result is bit 6 of ADDATL. To get a 10-bit conversion result, both ADDAT register must be read. If an 8-bit conversion result is required, only the reading of ADDATH is necessary. The data remains in ADDAT until it is overwritten by the next converted data. ADDAT can be read or written under software control. lf the A/D converter of the C504 is not used, register ADDATH can be used as an additional general purpose register.

Special Function Registers ADCON0 (Address $D8_H$) **Reset Value : $XX000000_B$**
Special Function Registers ADCON1 (Address DC_H) **Reset Value : $01XXX000_B$**
Special Function Registers IEN1 (Address $A9_H$) **Reset Value : $XX000000_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$D8_H$	–	–	IADC	BSY	ADM	MX2	MX1	MX0	ADCON0
DC_H	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0	ADCON1
$A9_H$	–	–	ECT1	ECCM	ECT2	ECEM	EX2	EADC	IEN1

The shaded bits are not used for A/D converter control.

Bit	Function
–	Reserved bits for future use
IADC	A/D converter interrupt request flag Set by hardware at the end of a A/D conversion. Must be cleared by software.
BSY	Busy flag This flag indicates whether a conversion is in progress (BSY = 1). The flag is cleared by hardware when the conversion is finished.
ADM	A/D conversion mode When set, a continous A/D conversion is selected. If cleared during a running A/D conversion, the conversion is stopped at its end.
MX2 - MX0	A/D converter input channel select bits Bits MX2-0 can be written or read either in ADCON0 or ADCON1. The channel selection done by writing to ADCON 1(0) overwrites the selection in ADCON 0(1) when ADCON 1(0) is written after ADCON 0(1). The analog inputs are selected according the following table :

MX2	MX1	MX0	Selected Analog Input
0	0	0	P1.0 / AN0
0	0	1	P1.1 / AN1
0	1	0	P1.2 / AN2
0	1	1	P1.3 / AN3
1	0	0	P3.2 / AN4
1	0	1	P3.3 / AN5
1	1	0	P3.4 / AN6
1	1	1	P3.5 / AN7

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>ADCL1
ADCL0</td><td>A/D converter clock prescaler selection
ADCL1 and ADCL0 select the prescaler ratio for the A/D conversion clock f_{ADC}. Depending on the clock rate f_{OSC} of the C504, f_{ADC} must be adjusted in a way that the resulting conversion clock f_{ADC} is less or equal 2 MHz (see section 6.5.3).
The prescaler ratio is selected according the following table :
<table>
<tr><th>ADCL1</th><th>ADCL0</th><th>Prescaler Ratio</th></tr>
<tr><td>0</td><td>0</td><td>divide by 4</td></tr>
<tr><td>0</td><td>1</td><td>divide by 8 (default after reset)</td></tr>
<tr><td>1</td><td>0</td><td>divide by 16</td></tr>
<tr><td>1</td><td>1</td><td>divide by 32</td></tr>
</table></td></tr>
<tr><td>EADC</td><td>Enable A/D converter interrupt.
If EADC = 0, the A/D converter interrupt is disabled</td></tr>
</table>

Note : Generally, before entering the power-down mode, an A/D conversion in progress must be stopped. If a single A/D conversion is running, it must be terminated by polling the BSY bit or waiting for the A/D conversion interrupt. In continuous conversion mode, bit ADM must be cleared and the last A/D conversion must be terminated before entering the power-down mode.

A single A/D conversion is started by writing to SFR ADDATL with dummy data. A continuous conversion is started under the following conditions :

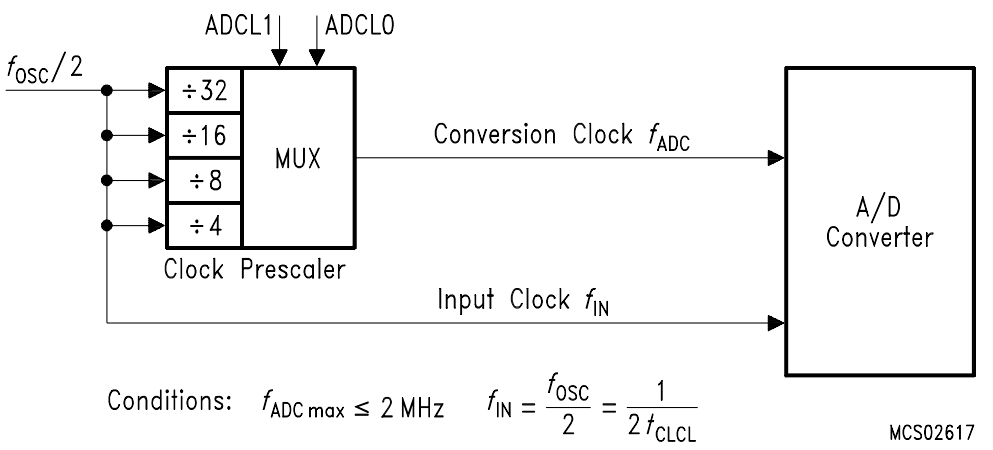
- By setting bit ADM during a running single A/D conversion
- By setting bit ADM when at least one A/D conversion has occured after the last reset operation.
- By writing ADDATL with dummy data after bit ADM has been set before (if no A/D conversion has occured after the last reset operation).

When bit ADM is reset by software in continuous conversion mode, the just running A/D conversion is stopped after its end.

6.5.3 A/D Converter Clock Selection

The ADC uses two clock signals for operation : the conversion clock f_{ADC} (=1/t_{ADC}) and the input clock f_{IN} (=1/t_{IN}). Both clock signals are derived from the C504 system clock f_{OSC} which is applied at the XTAL pins. The input clock f_{IN} is always $f_{OSC}/2$ while the conversion clock must be adapted to the input clock f_{OSC}. The conversion clock is limited to a maximum frequency of 2 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 2 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.

The table in **figure 6-40** shows the prescaler ratio which must be selected for typical system clock rates. Up to 16 MHz system clock the prescaler ratio 4 is selected. Up to 32 MHz a prescaler ratio of at least 8 must be selected, and beyond 32 MHz the prescaler ratio 16 has to be selected. The prescaler ratio 32 can be selected when the maximum performance of the A/D converter is not necessarily required or the input impedance of the analog source is to high to reach the maximum accuracy.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
3.5 MHz	1.75	÷ 4	.438	0	0
12 MHz	6	÷ 4	1.5	0	0
16 MHz	8	÷ 4	2	0	0
24 MHz	12	÷ 8	1.5	0	1
32 MHz	16	÷ 8	2	0	1
40 MHz	20	÷ 16	1.25	1	0

Figure 6-40
A/D Converter Clock Selection

The duration of an A/D conversion is a multiple of the period of the f_{IN} clock signal. The calculation of the A/D conversion time is shown in the next section.

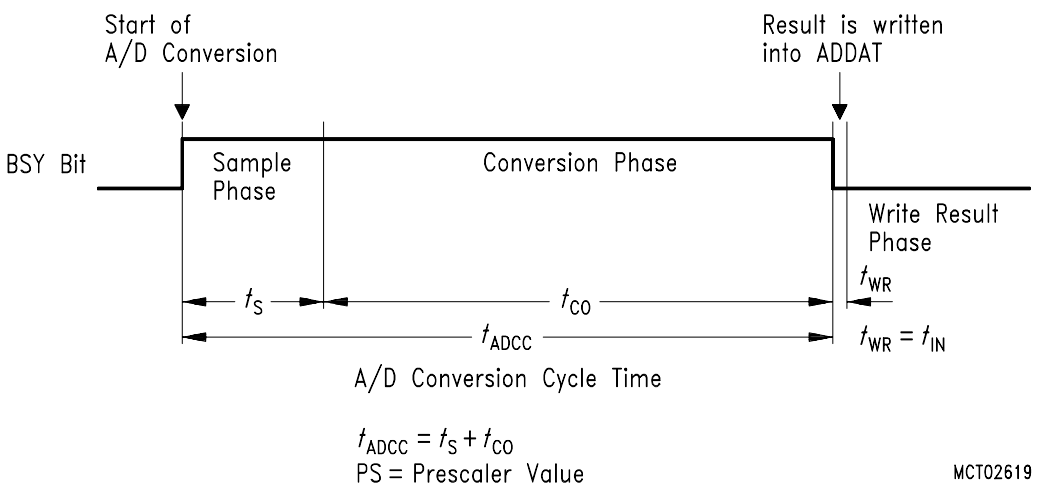
6.5.4 A/D Conversion Timing

An A/D conversion is internally started by writing into the SFR ADDATL with dummy data. A write to SFR ADDATL will start a new conversion even if a conversion is currently in progress. The conversion begins with the next machine cycle, and the BSY flag in SFR ADCON0 will be set.

The A/D conversion procedure is divided into three parts :

- Sample phase (t_S), used for sampling the analog input voltage.
- Conversion phase (t_{CO}), used for the A/D conversion (includes calibration)
- Write result phase (t_{WR}), used for writing the conversion result into the ADDAT registers.

The total A/D conversion time is defined by t_{ADCC} which is the sum of the two phase times t_S and t_{CO}. The duration of the three phases of an A/D conversion is specified by its specific timing parameter as shown in **figure 6-41**.



Prescaler Ratio (=PS)	t_S = 2 x PS x t_{IN}	t_{CO}	t_{ADCC}
32	64 x t_{IN}	320 x t_{IN}	384 x t_{IN}
16	32 x t_{IN}	160 x t_{IN}	192 x t_{IN}
8	16 x t_{IN}	80 x t_{IN}	96 x t_{IN}
4	8 x t_{IN}	40 x t_{IN}	48 x t_{IN}

Figure 6-41
A/D Conversion Timing

Sample Time t_S :
During this time the internal capacitor array is connected to the selected analog input channel and is loaded with the analog voltage to be converted. The analog voltage is internally fed to a voltage comparator. With beginning of the sample phase the BSY bit in SFR ADCON0 is set.

Conversion Time t_{CO} :
During the conversion time the analog voltage is converted into a 10-bit digital value using the successive approximation technique with a binary weighted capacitor network. During an A/D conversion also a calibration takes place. During this calibration alternating offset and linearity calibration cycles are executed (see also **section 6.5.5**). At the end of the conversion time the BSY bit is reset and the IADC bit in SFR ADCON0 is set indicating an A/D converter interrupt condition.

Write Result Time t_{WR} :
At the result phase the conversion result is written into the ADDAT registers.

Figure 6-42 shows how an A/D conversion is embedded into the microcontroller cycle scheme using the relation 6 x t_{IN} = 1 instruction cycle. It also shows the behaviour of the busy flag (BSY) and the interrupt flag (IADC) during an A/D conversion.

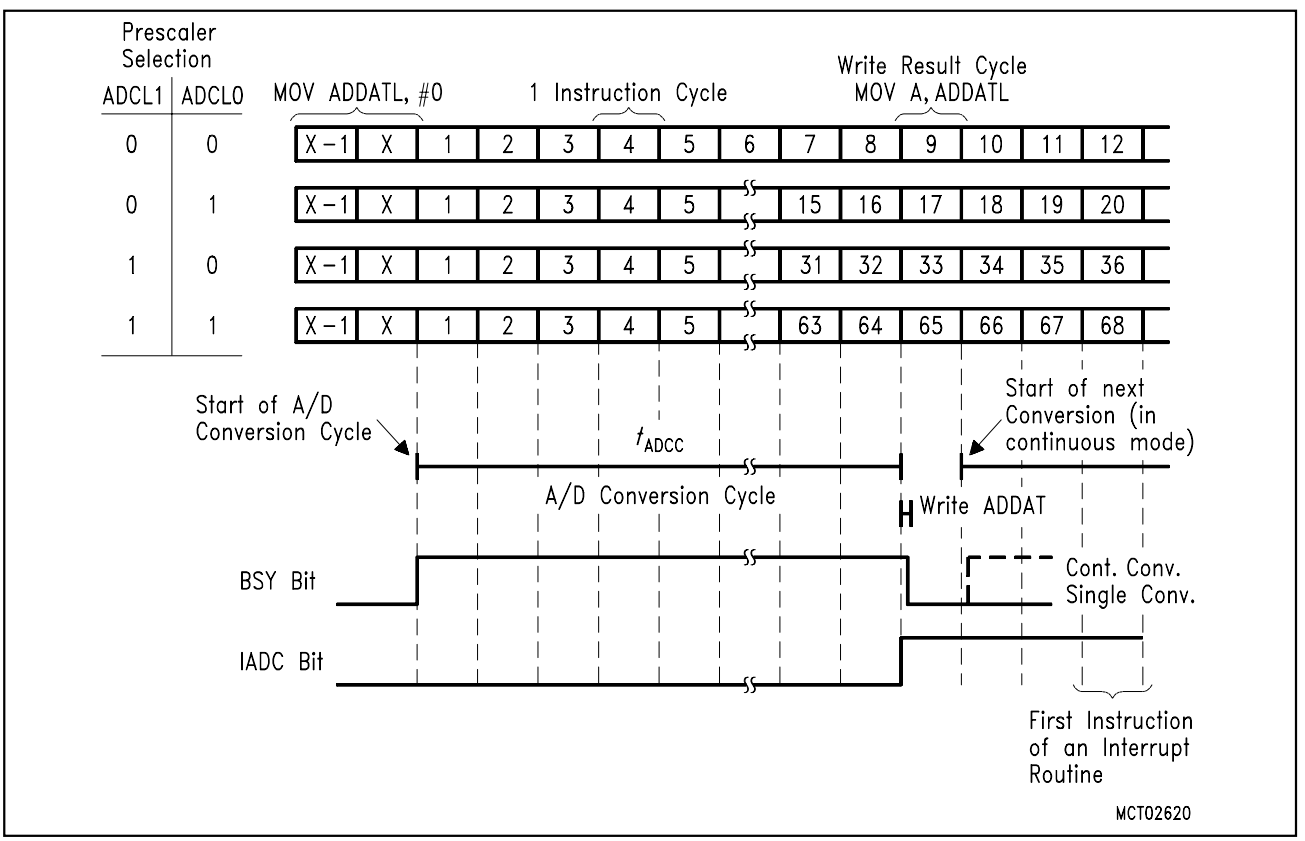


Figure 6-42
A/D Conversion Timing in Relation to Processor Cycles

Depending on the selected prescaler ratio (see **figure 6-40**), four different relationships between machine cycles and A/D conversion are possible. The A/D conversion is started when SFR ADDATL is written with dummy data. This write operation may take one or two machine cycles. In **figure 6-42**, the instruction MOV ADDATL,#0 starts the A/D conversion (machine cycle X-1 and X). The total A/D conversion (sample, conversion, and calibration phase) is finished with the end of the 8th, 16th, 32th, or 64th machine cycle after the A/D conversion start. In the next machine cycle the conversion result is written into the ADDAT registers and can be read in the same cycle by an instruction (e.g. MOV A,ADDATL). If continuous conversion is selected (bit ADM set), the next conversion is started with the beginning of the machine cycle which follows the writre result cycle.

The BSY bit is set at the beginning of the first A/D conversion machine cycle and reset at the beginning of the write result cycle. If continuous conversion is selected, BSY is again set with the beginning of the machine cycle which follows the write result cycle.

The interrupt flag IADC is set at the end of the A/D conversion. If the A/D converter interrupt is enabled and the A/D converter interrupt is priorized to be serviced immediately, the first instruction of the interrupt service routine will be executed in the third machine cycle which follows the write result cycle. IADC must be reset by software.

Depending on the application, typically there are three methods to handle the A/D conversion in the C504 .

- Software delay
  The machine cycles of the A/D conversion are counted and the program executes a software delay (e.g. NOPs) before reading the A/D conversion result in the write result cycle. This is the fastest method to get the result of an A/D conversion.
- Polling BSY bit
  The BSY bit is polled and the program waits until BSY=0. Attention : a polling JB instruction which is two machine cycles long, possibly may not recognize the BSY=0 condition during the write result cycle in the continuous conversion mode.
- A/D conversion interrupt
  After the start of an A/D conversion the A/D converter interrupt is enabled. The result of the A/D conversion is read in the interrupt service routine. If other C504 interrupts are enabled, the interrupt latency must be regarded. Therefore, this software method is the slowest method to get the result of an A/D conversion.

Depending on the oscillator frequency of the C504 and the selected divider ratio of the A/D converter prescaler the total time of an A/D conversion is calculated according **figure 6-41** and **table 6-14. Figure 6-43** on the next page shows the minimum A/D conversion time in relation to the oscillator frequency f_{OSC}. The minimum conversion time is 6 µs which can be achieved at f_{OSC} of 16 or 32 MHz.

Table 6-14
A/D Conversion Time for Dedicated System Clock Rates

f_{OSC} [MHz]	Prescaler Ratio PS	f_{ADC} [MHz]	Sample Time t_S [µs]	Total Conversion Time t_{ADCC} [µs]
3.5	4	.438	4.57	27.43
12	4	1.5	1.33	8
16	4	2	1	6
24	8	1.5	1.33	8
32	8	2	1	6
40	16	1.25	1.6	9.6

Note : The prescaler ratios in **table 6-14** are mimimum values. At system clock rates (f_{OSC}) up to 16 MHz the divider ratio 8, 16, or 32 can also be used. At system clock rates between 16 and 32 MHz the divider ratios 16 and 32 can be used. Using higher divider ratios than required increases the total conversion time but can be useful in applications which have voltage sources with higher input resistances for the analog inputs (increased sample phase).

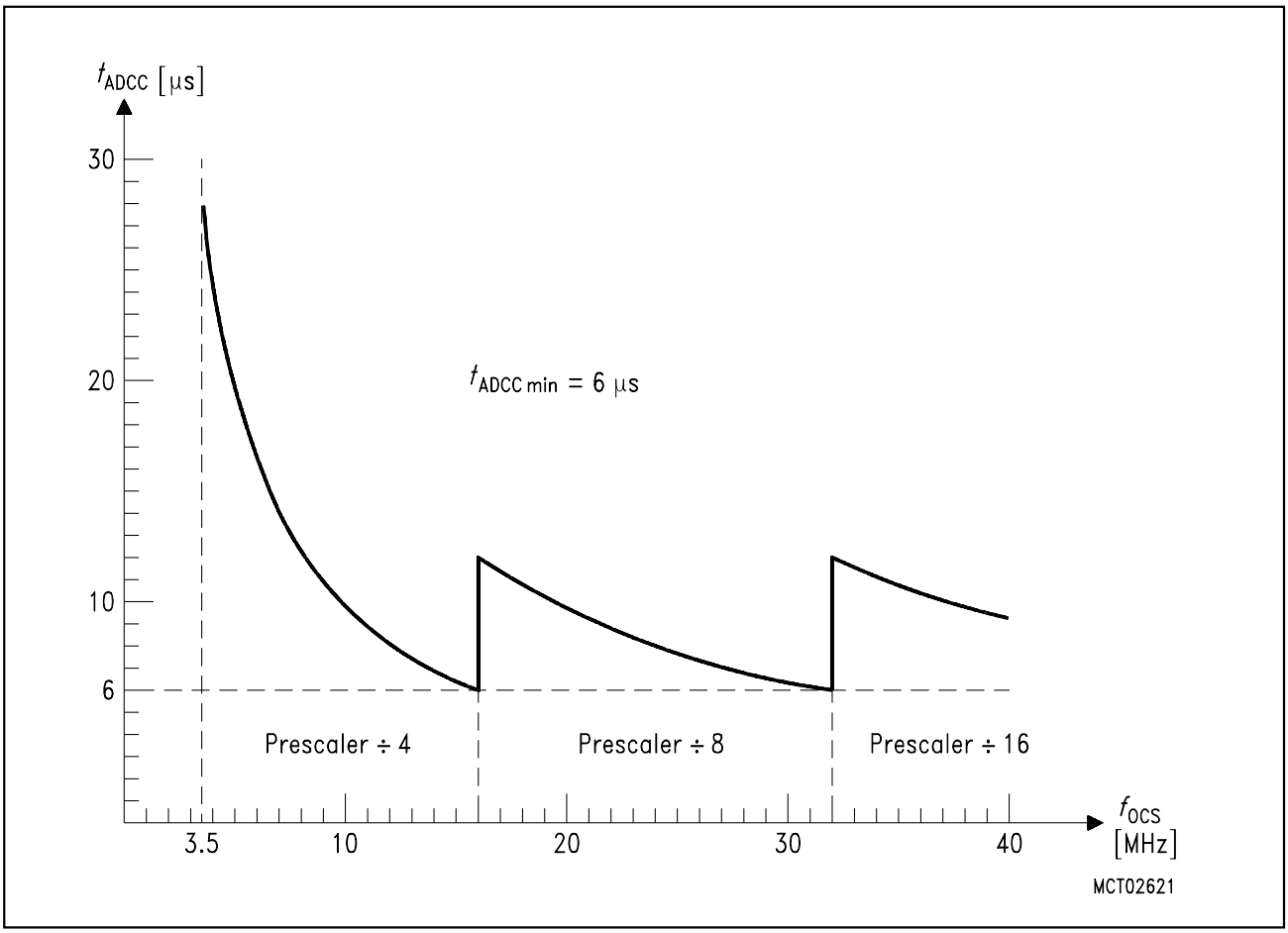


Figure 6-43
Minimum A/D Conversion Time in Relation to System Clock

6.5.5 A/D Converter Calibration

The C504 A/D converter includes hidden internal calibration mechanisms which assure a save functionality of the A/D converter according to the DC characteristics. The A/D converter calibration is implemented in a way that a user program which executes A/D conversions is not affected by its operation. Further, the user program has no control on the calibration mechanism. The calibration itself executes two basic functions :

- Offset calibration : compensation of the offset error of the internal comparator
- Linearity calibration : correction of the binary weighted capacitor network

The A/D converter calibration operates in two phases : calibration after a reset operation and calibration at each A/D conversion. The calibration phases are controlled by a state machine in the A/D converter. This state machine executes the calibration phases and stores the calibration results dynamically in a small calibration RAM

After a reset operation the A/D calibration is automatically started. This reset calibration phase which takes 3328 f_{ADC} clocks, alternating offset and linearity calibration is executed. Therefore, at 12 MHz oscillator frequency and with the default after reset prescaler value of 8, a reset calibration time of approx. 4.4 ms is reached. For achieving a proper reset calibration, the f_{ADC} prescaler value must satisfy the condition $f_{ADC\ max} \leq 2$ MHz. If this condition is not met at a specific oscillator frequency with the default prescaler value after reset, the f_{ADC} prescaler must be adjusted immediately after reset by setting bits ADCL1 and ADCL0 im SFR ADCON1 to a suitable value.

After the reset calibration phase the A/D converter is calibrated according to its DC characteristics. Nevertheless, during the reset calibration phase single or continuous A/D can be executed. In this case it must be regarded that the reset calibration is interrupted and continued after the end of the A/D conversion. Therefore, interrupting the reset calibration phase by A/D conversions extends the total reset calibration time. If the specified total unadjusted error (TUE) has to be valid for an A/D conversion, it is recommended to start the first A/D conversions after reset when the reset calibration phase is finished. Depending on the oscillator frequency used, the reset calibration phase can be possibly shortened by setting ADCL1 and ADCL0 (prescaler value) to its final value immediately after reset.

After the reset calibration, a second calibration mechanism is initiated. This calibration is coupled to each A/D conversion**.** With this second calibration mechanism alternatively offset and linearity calibration values, stored in the calibration RAM, are always checked when an A/D conversion is executed and corrected if required.

6.5.6 A/D Converter Analog Input Selection

The analog inputs are located at port 1 and port 3 (4 lines on each port). The corresponding port 1 and port 3 pins have a port structure, which allows to use it either as digital I/Os or analog inputs (see section 6.1.3.2 and 6.1..3.4). The analog input function of these digital/analog port lines is selected via the registers P1ANA and P3ANA. These two registers are mapped registers and can be accessed when bit RMAP in SFR SYSCON is set when writing to its address (90_H or $B0_H$). If the specific bit location of P1ANA or P3ANA is set, the corresponding port line is configured as an digital input. With a 0 in the bit location the port line operates as analog port.

Special Function Registers P1ANA (Mapped Address 90_H) **Reset Value : $XXXX1111_B$**
Special Function Registers P3ANA (Mapped Address $B0_H$) **Reset Value : $XX1111XX_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
90_H	–	–	–	–	EAN3	EAN2	EAN1	EAN0	P1ANA
$B0_H$	–	–	EAN7	EAN6	EAN5	EAN4	–	–	P3ANA

Bit	Function
EAN3 - 0	Enable analog port 1 inputs If EANx (x = 3-0) is cleared, port pin P1.x is enabled for operation as an analog input. If EANx is set, port pin P1.x is enabled for digital I/O function (default after reset).
EAN7 - 4	Enable analog port 1 input If EANx (x = 7-4) is cleared, port pin P3.x-2 is enabled for operation as an analog input. If EANx is set, port pin P3.x-2 is enabled for digital I/O function (default after reset).
–	Reserved bits

7 Interrupt System

The C504 provides 12 interrupt sources with two priority levels. Eight interrupts can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial interface, A/D converter, and capture/compare unit), and four interrupts may be triggered externally (P1.1/T2EX, P3.2/$\overline{\text{INT0}}$, P3.3/$\overline{\text{INT1}}$ and P3.6/$\overline{\text{INT2}}$). If the capture/compare unit is not used in an application, its capture features can be used to provide additional 3 external interrupt inputs. An additional non-maskable 13th interrupt is reserved for the external wake-up from power-down mode feature.

Compared with the C501, the functionality of the external interrupts is extended. In the edge triggered mode of the external interrupts it is possible to select between a falling, a rising, or a falling and rising edge interrupt trigger condition. The capture/compare unit provides four new interrupt vectors : an interrupt vector for the compare timer 1 reset/count direction change event, an interrupt vector for the compare timer 2 reset event, an interrupt vector for a capture or compare match event, and an interrupt vector for two emergency conditions of the CAPCOM unit (trap and block commutation error).

Figure 7-1 and **2** give a general overview of the interrupt sources and illustrate the request and control flags which are described in the next sections.

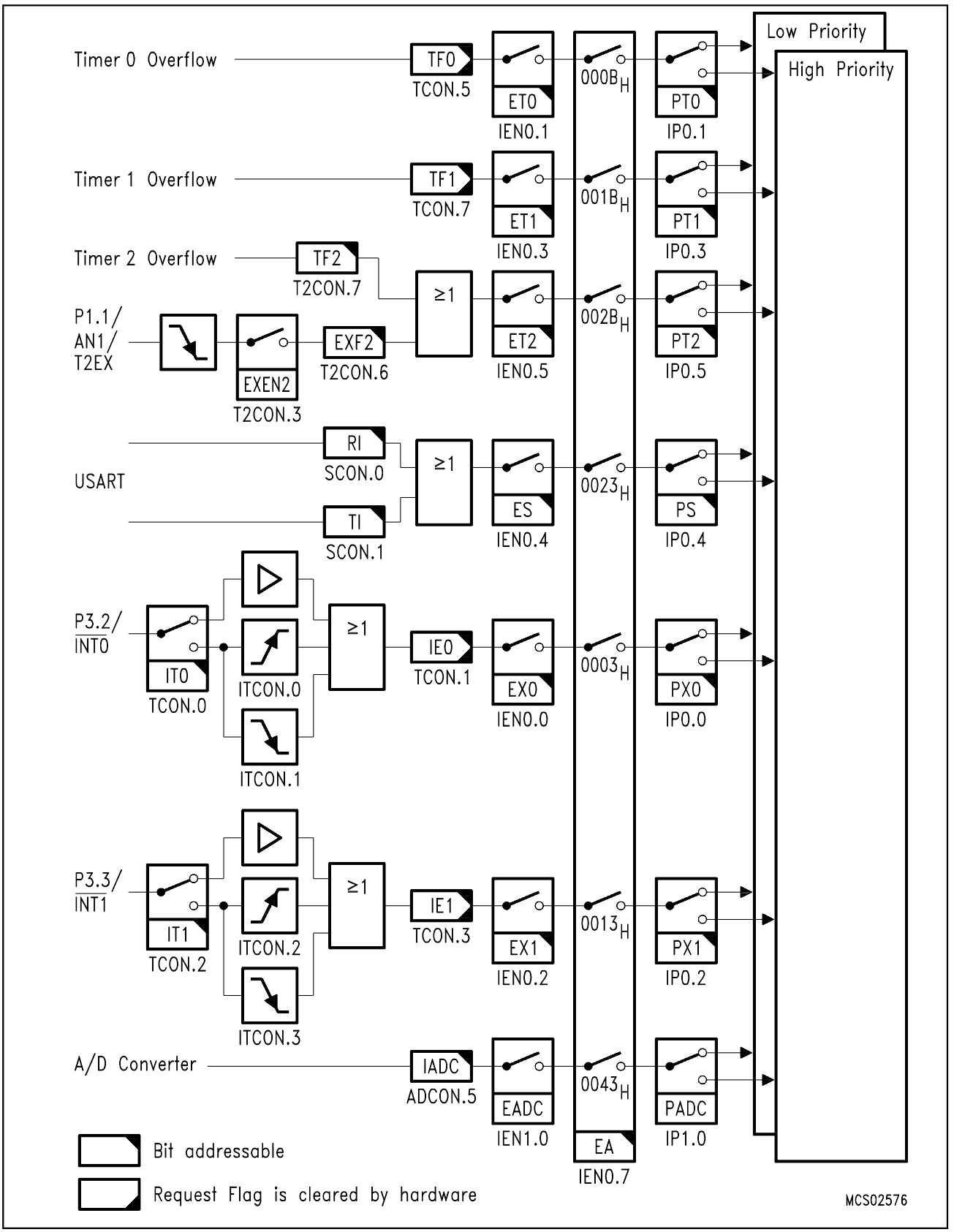


Figure 7-1
Interrupt Request Sources (Part 1)

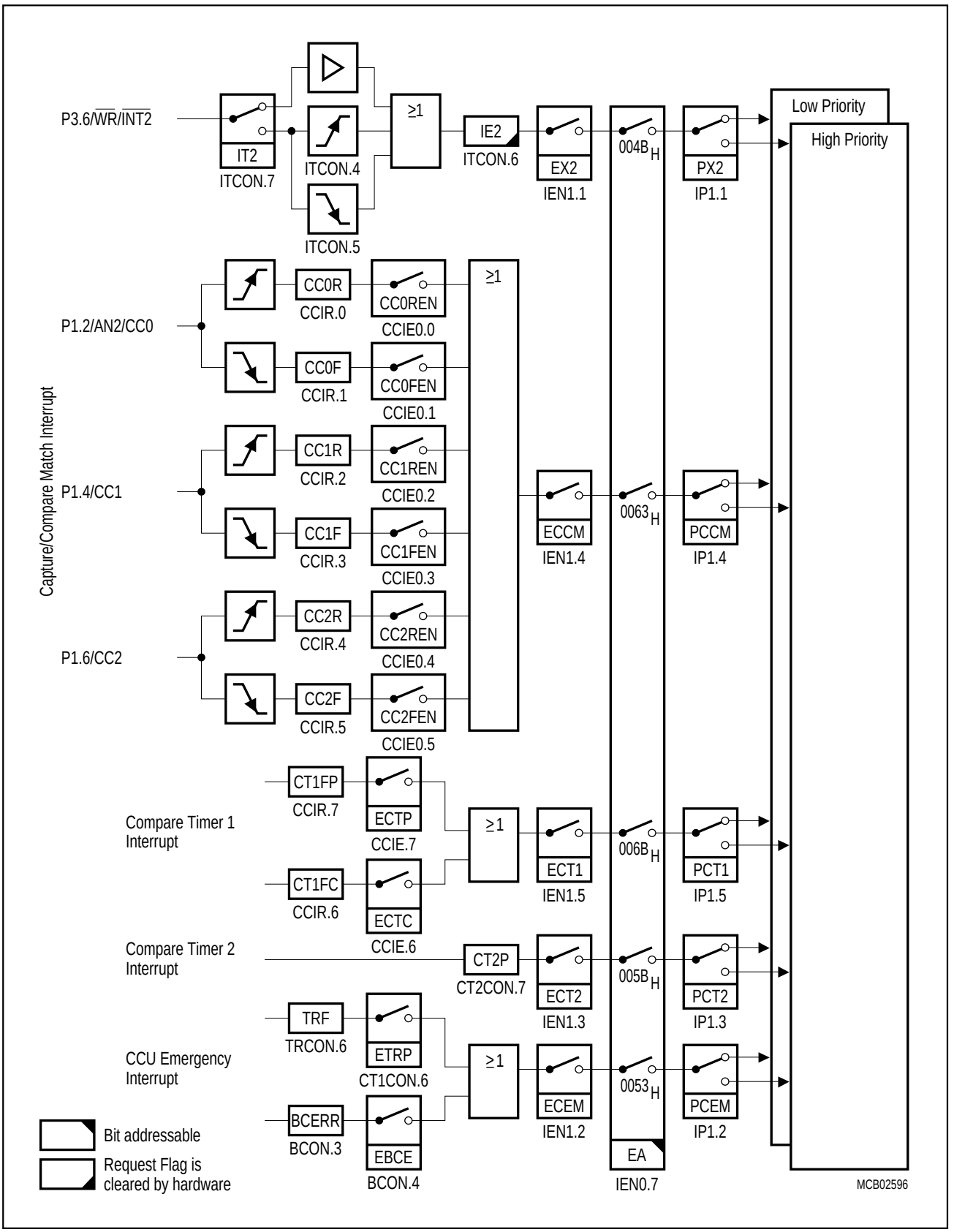


Figure 7-2
Interrupt Request Sources (Part 2)

7.1 Interrupt Structure

A common mechanism is used to generate the various interrupts Each interrupt source has its own request flag(s) located in a special function register (e.g. TCON, T2CON, SCON, ADCON0). Provided the peripheral or external source meets the condition for an interrupt, the dedicated request flag is set, whether an interrupt is enabled or not. For example, each timer 0 overflow sets the corresponding request flag TF0. If it is already set, it retains a one (1). But the interrupt is not necessarily serviced.

Now each interrupt requested by the corresponding flag can individually be enabled or disabled by the enable bits in the SFRs IEN0 and IEN1. This determines whether the interrupt will actually be performed. In addition, there is a global enable bit for all interrupts which, when cleared, disables all interrupts independent of their individual enable bits.

7.2 Interrupt Sources and Vectors

Each interrupt source has an interrupt vector address associated. This vector address is accessed first if the corresponding interrupt is serviced. More details about the interrupt servicing are given in **section 7.4**. **Table 7-1** lists these interrupts.

Table 7-1
Interrupt Vector Addresses

Request Flags	Interrupt Source	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	$002B_H$
IADC	A/D converter interrupt	0043_H
IE2	External interrupt 2	$004B_H$
TRF, BCERR	CAPCOM emergency interrupt	0053_H
CT2P	Compare timer 2 interrupt	$005B_H$
CC0F-CC2F, CC0R-CC2R	Capture / compare match interrupt	0063_H
CT1FP, CT1FC	Compare timer 1 interrupt	$006B_H$
–	Power-down interrupt	$007B_H$

A special interrupt source is the power-down mode interrupt. This interrupt is automatically enabled when the C504 is in power-down mode and bit EWPD (enable wake-up from power-down mode) in SFR PCON1 is set. If these two conditions are met and when the oscillator watchdog unit start-up phase after a wake-up condition ($\overline{INT0}$=0) is finished, the C504 starts with an interrupt at address $007B_H$. All other interrupts are now disabled until the RETI instruction of the power-down interrupt routine has been executed.

7.3 Interrupt Registers

7.3.1 Interrupt Enable Registers

Each interrupt vector can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0, IEN1. Register IEN0 also contains the global disable bit (EA), which can be cleared to disable all interrupts at once. Some interrupts sources have further enable bits (e.g. EXEN2, ECTR, etc.). Such interrupt enable bits are controlled by specific bits in the SFRs of the corresponding peripheral units (described in **chapter 6**).

The IEN0 register contains the general enable/disable flags of the external interrupts 0 and 1, the timer interrupts, the USART interrupt, and the AD converter interrupt. The external interrupt 2 and the four interrupts of the CCU are enabled/disabled by bits in the IEN1 register.

After reset the enable bits of IE0 and IE1 are set to 0. That means that the corresponding interrupts are disabled.

Special Function Registers IEN0 (Address $A8_H$) **Reset Value : $0X000000_B$**

Bit No.	MSB							LSB	
	AF_H	AE_H	AD_H	AC_H	AB_H	AA_H	$A9_H$	$A8_H$	
$A8_H$	EA	–	ET2	ES	ET1	EX1	ET0	EX0	IEN0

Bit	Function
EA	Disables all Interrupts If EA=0, no interrupt will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	Reserved bits for future use.
ET2	Timer 2 interrupt enable If ET2 = 1, the Timer 2 interrupt is enabled.
ES	Serial channel interrupt enable If ES = 1, the Serial Channel interrupt is enabled.
ET1	Timer 1 overflow interrupt enable If ET1 = 1, the Timer 1 interrupt is enabled.
EX1	External interrupt 1 enable If EX1 = 1, the external interrupt 1 is enabled.
ET0	Timer 0 overflow interrupt enable If ET0 = 1, the Timer 0 interrupt is enabled.
EX0	External interrupt 0 enable If EX0 = 1, the external interrupt 0 is enabled.

Special Function Registers IEN1 (Address $A9_H$) **Reset Value : $XX000000_B$**

Bit No.	MSB							LSB	
	7	6	5	4	3	2	1	0	
$A9_H$	–	–	ECT1	ECCM	ECT2	ECEM	EX2	EADC	IEN1

Bit	Function
–	Reserved bits for future use.
ECT1	Compare Timer 1 Interrupt enable If ECT1 = 1, the compare timer 1 interrupt is enabled.
ECCM	Capture/compare match interrupt If ECCM = 1, the capture/compare interrupt is enabled.
ECT2	Compare timer 2 interrupt enable If ECT2 = 1, the compare timer 2 interrupt is enabled.
ECEM	CCU emergency interrupt enable If ECEM = 1, the emergency interrupt of the CCU is enabled.
EX2	Timer 2 Interrupt Enable If EX2 = 1, the external interrupt 2 is enabled.
EADC	A/D converter interrupt enable If EADC = 1, the A/D Converter interrupt is enabled.

7.3.2 Interrupt Prioritiy Registers

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in the SFRs IP0 or IP1 (interrupt priority: 0 = low priority, 1 = high priority).

Special Function Register IP0 (Address $B8_H$) **Reset Value : $XX000000_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B8_H$	–	–	PT2	PS	PT1	PX1	PT0	PX0	IP0

Bit	Function
–	Reserved bits for future use.
PT2	Timer 2 interrupt priority level If PT2 = 0, the Timer 2 interrupt has a low priority.
PS	Serial channel interrupt priority level If PS = 0, the Serial Channel interrupt has a low priority.
PT1	Timer 1 overflow interrupt priority level If PT1 = 0, the Timer 1 interrupt has a low priority.
PX1	External interrupt 1 priority level If PX1 = 0, the external interrupt 1 has a low priority.
PT0	Timer 0 overflow interrupt priority level If PT0 = 0, the Timer 0 interrupt has a low priority.
PX0	External interrupt 0 priority level If PX0 = 0, the external interrupt 0 has a low priority.

Special Function Register IP1 (Address $B9_H$) **Reset Value : $XX000000_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B9_H$	–	–	PCT1	PCCM	PCT2	PCEM	PX2	PADC	IP1

Bit	Function
–	Reserved bits for future use.
PCT1	Compare timer 1 interrupt priority level If PCT1 = 0, the compare timer interrupt has a low priority.
PCCM	Capture/compare match interrupt priority level If PCCM = 0, the capture/compare match interrupt has a low priority.
PCT2	Compare timer 2 interrupt priority level If PCT2 = 0, the compare timer interrupt has a low priority.
PCEM	CCU emergency interrupt priority level If PCEM = 0, the CCU trap interrupt has a low priority.
PX2	External interrupt 2 priority level If PX2 = 0, the external interrupt 2 has a low priority.
PADC	A/D converter interrupt priority level If PADC = 0, the A/D Converter interrupt has a low priority.

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence (vertical and horizontal) as shown in **table 7-2** below. If e.g. the external interrupt 0 and the A/D converter interrupt have the same priority and if they are active simultaneously, the external interrupt 0 will be serviced first.

Table 7-2 :
Interrupt Source Structure

Interrupt Source		**Priority**
High Priority →	Low Priority	
External Interrupt 0	A/D Converter	High
Timer 0 Interrupt	External Interrupt 2	↓
External Interrupt 1	CCU Emergency Interrupt	
Timer 1 Interrupt	Compare Timer 2 Interrupt	
Serial Channel	Capture / Compare Match Interrupt	
Timer 2 Interrupt	Compare Timer 1 Interrupt	Low

7.3.3 Interrupt Request Flags

The interrupt request flags are located in different SFRs. **Table 7-3** shows the bit locations of the interrupt request flags. More detailed information about the interrupt request flags is given in the sections of **chapter 6** which describe the corresponding peripheral unit in detail.

Table 7-3 :
Locations of the Interrupt Request Flags

Interrupt Sources	Request Flags	SFR	Byte Address	Bit Address
External Interrupt 0	IE0	TCON	88_H	88_H
A/D converter IADC	IADC	ADCON0	$D8_H$	DD_H
Timer 0 Interrupt	TF0	TCON	88_H	$8D_H$
External Interrupt 1	IE1	TCON	88_H	$8B_H$
Timer 1 Interrupt	TF1	TCON	88_H	$8F_H$
Serial Channel	RI	SCON	98_H	98_H
	TI	SCON	98_H	99_H
Timer 2 Interrupt	TF2	T2CON	$C8_H$	CF_H
	EXF2	T2CON	$C8_H$	CE_H
External Interrupt 2	IT2	ITCON	$9A_H$	$9A_H$.7
Capture / Compare Match Interrupt	CCxR	CCIR	$E5_H$	$E5_H$.0/2/4
	CCxF	CCIR	$E5_H$	$E5_H$.1/3/5
Compare Timer 1 Interrupt	CT1FP	CCIR	$E5_H$	$E5_H$.7
	CT1FC	CCIR	$E5_H$	$E5_H$.6
Compare Timer 2 Interrupt	CT2P	CT2CON	$D2_H$	$D2_H$.7
CCU Emergency Interrupt	TRF	TRCON	$E7_H$	$E7_H$.6
	BCERR	BCON	$D7_H$	$D7_H$.3

7.4 How Interrupts are Handled

The interrupt flags are sampled at S5P2 in each machine cycle. The sampled flags are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceeding cycle, the polling cycle will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1) An interrupt of equal or higher priority is already in progress.
2) The current (polling) cycle is not in the final cycle of the instruction in progress.
3) The instruction in progress is RETI or any write access to registers IE0/IE1 or IP0/IP1.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress is completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any write access to registers IEN0/IEN1 or IP0/IP1, then at least one more instruction will be executed before any interrupt is vectored too; this delay guarantees that changes of the interrupt status can be observed by the CPU.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note that if any interrupt flag is active but not being responded to for one of the conditions already mentioned, or if the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle interrogates only the pending interrupt requests.

The polling cycle/LCALL sequence is illustrated in **figure 7-3**.

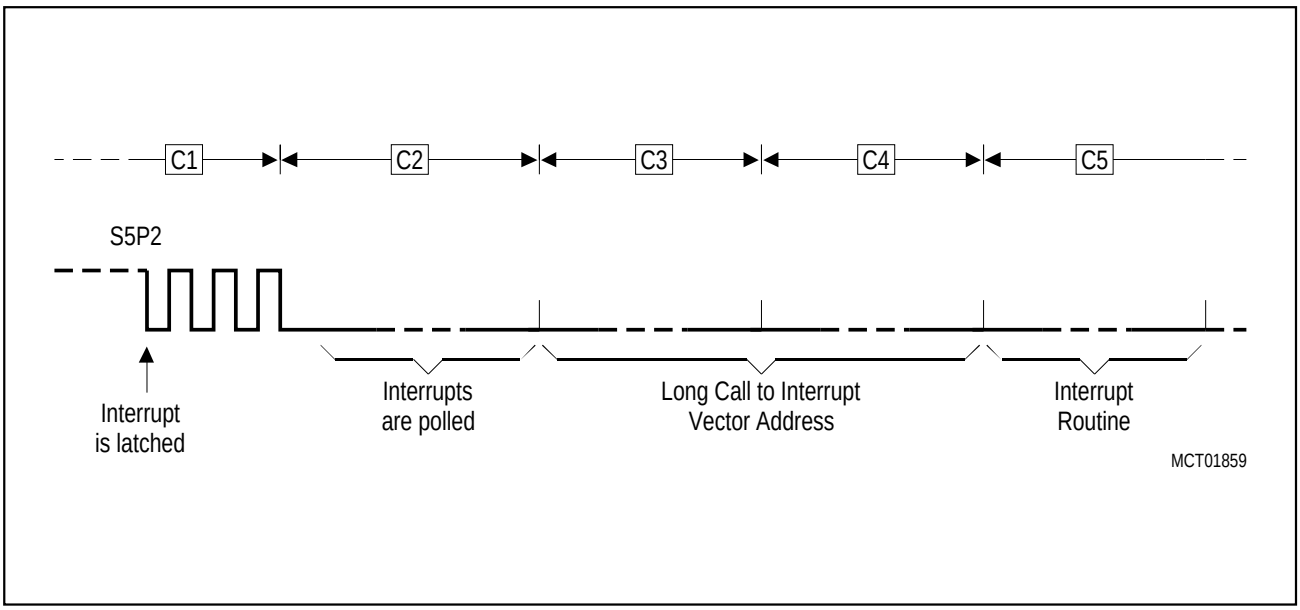


Figure 7-3
Interrupt Response Timing Diagram

Note that if an interrupt of a higher priority level goes active prior to S5P2 in the machine cycle labeled C3 in **figure 7-3** then, in accordance with the above rules, it will be vectored to during C5 and C6 without any instruction for the lower priority routine to be executed.

Thus, the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, while in other cases it does not; then this has to be done by the user's software. The hardware clears the external interrupt flags IEN0 and IEN1 only if they were transition-activated. The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with an address that depends on the source of the interrupt being vectored too.

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, then pops the two top bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt priority level. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress. In this case no interrupt of the same or lower priority level would be acknowledged.

7.5 External Interrupts

The external interrupts 0, 1, and 2 can be programmed to be level-activated or transition activated by setting or clearing bit IT0, IT1, or IT2, respectively in register TCON or ITCON. If ITx = 0 (x = 0 or 1), external interrupt x is triggered by a detected low level at the $\overline{\text{INTx}}$ pin. If ITx = 1, external interrupt x is edge-triggered. Further, in edge-triggered mode two bits of the ITCON register define the type of signal transition for which the external interrupt inputs are sensitive. Edge-triggered interrupt can be activated for an interrupt input signal at the rising edge, at the falling edge or at both signal transitions. In edge-triggered mode, if successive samples of the $\overline{\text{INTx}}$ pin show a different logic level in two consequent machine cycles, the corresponding interrupt request flag IEx in TCON/ ITCON is set. Flag bit IEx=1 then requests the interrupt.

If the external interrupt 0, 1, or 2 is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

The external timer 2 reload trigger interrupt request flag EXF2 will be activated by a negative transition at pin P1.1/T2EX but only if bit EXEN2 is set.

Since the external interrupt pins are sampled once in each machine cycle, an input low should be held for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated for negative transitions, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle to ensure that a negative transition (falling edge) is recognized so that the corresponding interrupt request flag will be set (see **figure 7-3**). In edge triggered mode the external interrupt request flags will automatically be cleared by the CPU when the service routine is called.

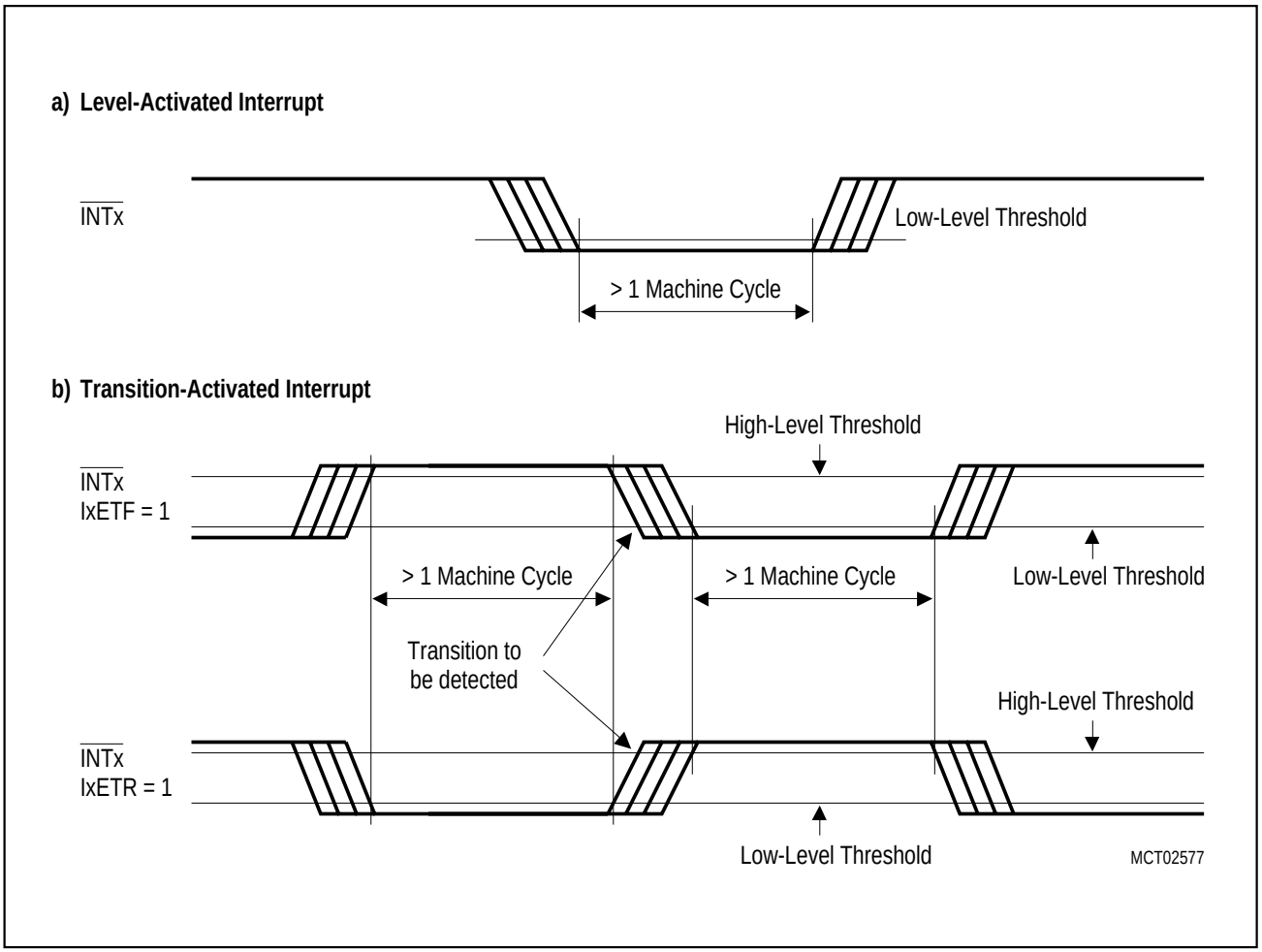
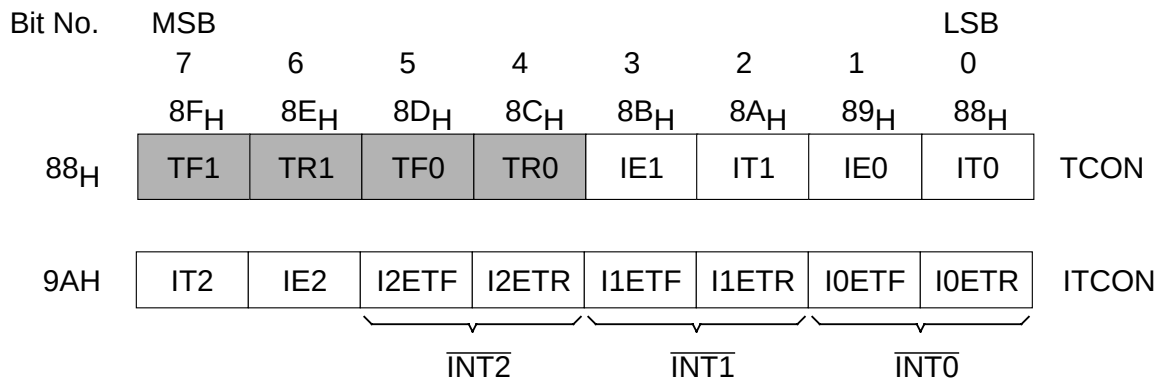


Figure 7-4
External Interrupt Detection

The edge-triggered interrupt mode selection for all three dedicated external interrupts and two $\overline{INT2}$ control bits are selected in the SFR ITCON (External Interrupt Trigger Condition Register). The edge-trigger mode selection is defined in a way (default value of ITCON after reset), that their function is upward compatible to the basic external interrupt functionality of the C501.

The $\overline{INT2}$ enable bit EX2 is located in IEN1 and the $\overline{INT2}$ priority bit is located in IP2. The level/ edge control bit and the IE2 flag for $\overline{INT2}$ is located in ITCON.

Special Function Register TCON (Address 88_H) **Reset Value : 00_H**
Special Function Registers ITCON (Address $9A_H$) **Reset Value : 00101010_B**



The shaded bits are not used for external interrupt control.

Bit	Function
IE1	External interrupt 1 request flag Set by hardware when an external interrupt 1 is detected. In edge triggered mode, this bit is reset by hardware when the interrupt is serviced.
IT1	External interrupt 1 level/edge trigger control flag If IT1 = 0, low level triggered mode for external interrupt 1 is selected. If IT1 = 1, edge triggered mode for external interrupt 1 is selected. In this mode, bits IxETF and IxETR in SFR ITCON further define the type of the interrupt sensitive edge (rising or/and falling) of external interrupt 1.
IE0	External interrupt 0 request flag Set by hardware when an external interrupt 0 is detected. In edge triggered mode, this bit is reset by hardware when the interrupt is serviced.
IT0	External interrupt 0 level/edge trigger control flag If IT0 = 0, low level triggered mode for external interrupt 0 is selected. If IT0 = 1, edge triggered mode for external interrupt 0 is selected. In this mode, bits IxETF and IxETR in SFR ITCON further define the type of the interrupt sensitive edge (rising or/and falling) of external interrupt 0.
IT2	External interrupt 2 level/edge trigger control flag If IT2 = 0, low level triggered mode for external interrupt 2 is selected. If IT2 = 1, edge triggered mode for external interrupt 2 is selected. In this mode, bits IxETF and IxETR in SFR ITCON further define the type of the interrupt sensitive edge (rising or/and falling) of external interrupt 2.
IE2	External interrupt 2 request flag Set by hardware when an external interrupt 2 is detected. In edge-triggered mode this bit is reset by hardware when the interrupt is serviced.

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>IxETF
IxETR</td><td>External interrupt edge trigger mode selection
(x=0-2 refers to $\overline{INT0}$ - $\overline{INT2}$)
<table>
<tr><th>IxETF</th><th>IxETR</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>$\overline{INTx}$ inputs are not sensitive for either rising or falling edge</td></tr>
<tr><td>0</td><td>1</td><td>$\overline{INTx}$ operates in rising edge-triggered mode</td></tr>
<tr><td>1</td><td>0</td><td>$\overline{INTx}$ operates in falling edge-triggered mode
(default after reset)</td></tr>
<tr><td>1</td><td>1</td><td>$\overline{INTx}$ operates in falling and rising edge-triggered mode</td></tr>
</table></td></tr>
</table>

7.6 Interrupt Response Time

If an external interrupt is recognized, its corresponding request flag is set at S5P2 in every machine cycle. The value is not polled by the circuitry until the next machine cycle. If the request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be next instruction to be executed. The call itself takes two cycles. Thus a minimum of three complete machine cycles will elapse between activation and external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would be obtained if the request was blocked by one of the three previously listed conditions. If an interrupt of equal or higer priority is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles since the longest instructions (MUL and DIV) are only 4 cycles long; and, if the instruction in progress is RETI or a write access to the registers IEN or IP the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction, if the instruction is MUL or DIV).

Thus a single interrupt system, the response time is always more than 3 cycles and less than 9 cycles.

8 Fail Safe Mechanisms

The C504 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

- a programmable watchdog timer (WDT), with variable time-out period from 512 µs up to approx. 1.1 s at 12 MHz.
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

8.1 Programmable Watchdog Timer

To protect the system against software upset, the user's program has to clear the watchdog within a previously programmed time period. If the software fails to do this periodical refresh of the Watchdog Timer, an internal hardware reset will be initiated. The software can be designed such that the watchdog times out if the program does not work properly. It also times out if a software error is based on hardware-related problems.

The Watchdog Timer in the C504 is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler. The divide-by-16 prescaler is enabled by setting bit WDTPSEL (bit 7 of SFR WDTREL). From the 15-bit Watchdog Timer count value only the upper 7 bits can be programmed.

Figure 8-1 shows the block diagram of the programmable Watchdog Timer.

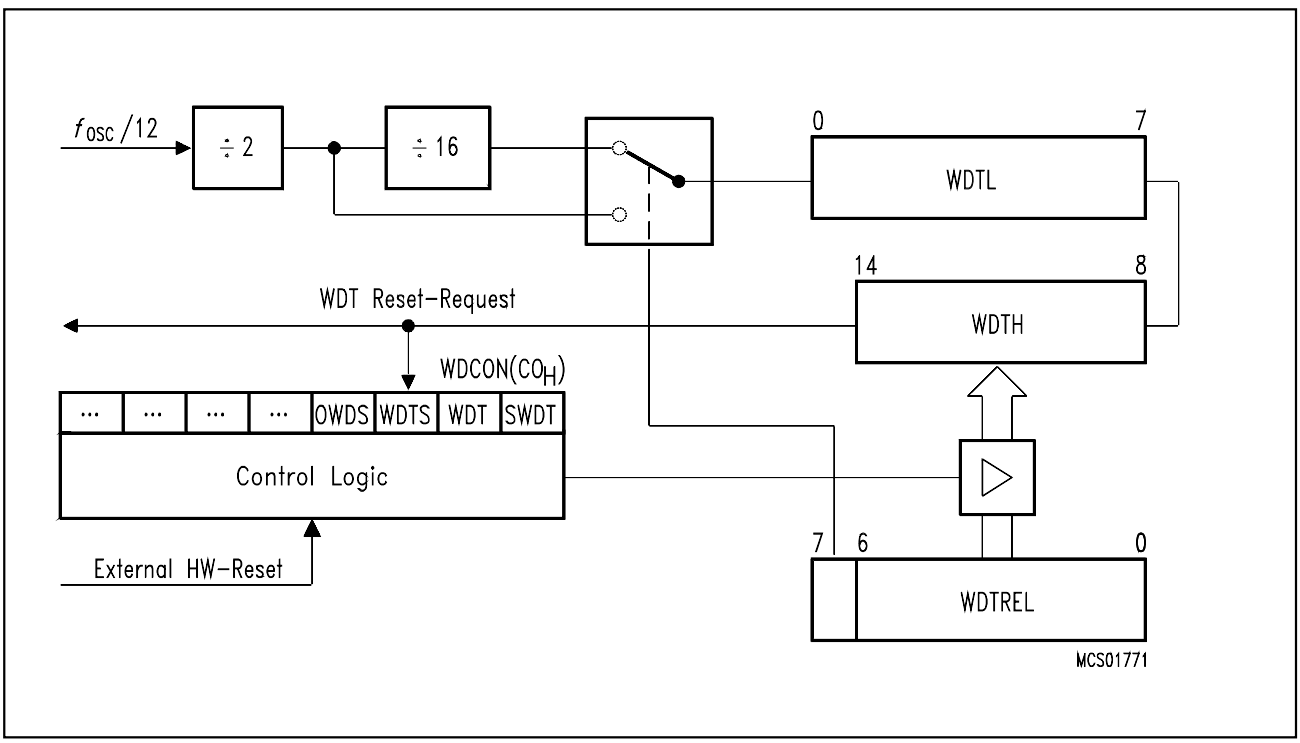


Figure 8-1
Block Diagram of the Programmable Watchdog Timer

Special Function Register WDTREL (Address 86_H) **Reset Value : 00_H**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
86_H	WDT PSEL	Watchdog Timer Reload Register							WDTREL

Bit	Function
WDTPSEL	Watchdog timer prescaler select bit. When set, the watchdog timer is clocked through an additional divide-by-16 prescaler .
WDTREL.6 - 0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to WDTH when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

Special Function Register WDCON (Address $C0_H$) **Reset Value : XXXX 0000_B**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$C0_H$	–	–	–	–	OWDS	WDTS	WDT	SWDT	WDCON

Bit	Function
–	Not implemented. Reserved for future use.
OWDS	Oscillator Watchdog Timer Status Flag. Set by hardware when an oscillator watchdog reset occured. Can be set and cleared by software.
WDTS	Watchdog Timer Status Flag. Set by hardware when a Watchdog Timer reset occured. Can be cleared and set by software.
WDT	Watchdog Timer Refresh Flag. Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer.
SWDT	Watchdog Timer Start Flag. Set to activate the Watchdog Timer. When directly set after setting WDT, a watchdog timer refresh is performed.

Immediately after start, the Watchdog Timer is initialized to the reload value programmed to WDTREL.0-WDTREL.6. After an external HW reset, an oscillator watchdog power on reset, or a watchdog timer reset, register WDTREL is cleared to 00_H. The lower seven bits of WDTREL can be loaded by software at any time.

Examples (given for 12- and 24-MHz external oscillator frequency):

Table 8-1
Watchdog Timer Time-Out Periods

WDTREL	Time-Out Period		Comments
	f_{osc} = 12 MHz	f_{osc} = 24 MHz	
00_H	65.535 ms	32.768 ms	This is the default value
80_H	1.1 s	0.55 s	Maximum time period
$7F_H$	512 µs	256 µs	Minimum time period

Starting the Watchdog Timer

The Watchdog Timer can be started by software (bit SWDT in SFR WDCON), but it cannot be stopped during active mode of the device. If the software fails to clear the watchdog timer an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software (status flag WDTS in WDCON is set). A refresh of the watchdog timer is done by setting bits WDT (SFR WDCON) and SWDT consecutively. This double instruction sequence has been implemented to increase system security.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes"). Therefore, it is possible to use the idle mode in combination with the watchdog timer function. But even the watchdog timer cannot reset the device when one of the power saving modes has been entered accidentally.

8.1.1 Refreshing the Watchdog Timer

At the same time the Watchdog Timer is started, the 7-bit register WDTH is preset by the contents of WDTREL.0 to WDTREL.6. Once started the Watchdog Timer cannot be stopped by software but can be refreshed to the reload value only by first setting bit WDT (WDCON) and by the next instruction setting SWDT (WDCON). Bit WDT will automatically be cleared during the third machine cycle after having been set. This double-instruction refresh of the Watchdog Timer is implemented to minimize the chance of an unintentional reset of the watchdog unit.
When the Watchdog Timer is started or refreshed, its non accessible lower 8 bits, stored in WDTL (see **figure 8-1**), are reset to 00_H.

The reload register WDTREL can be written at any time, as already mentioned. Therefore, a periodical refresh of WDTREL can be added to the above mentioned starting procedure of the Watchdog Timer. Thus a wrong reload value caused by a possible distortion during the write operation to WDTREL can be corrected by software.

8.1.2 Watchdog Reset and Watchdog Status Flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state $7FFC_H$. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS is set. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

8.2 Oscillator Watchdog Unit

The oscillator watchdog unit serves for three functions :

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Control of external wake-up from software power-down mode**
  When the power-down mode is left by a low level at the $\overline{\text{INT0}}$ pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

Note:

The oscillator watchdog unit is always enabled.

8.2.1 Detailed Description of the Oscillator Watchdog Unit

Figure 8-2 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

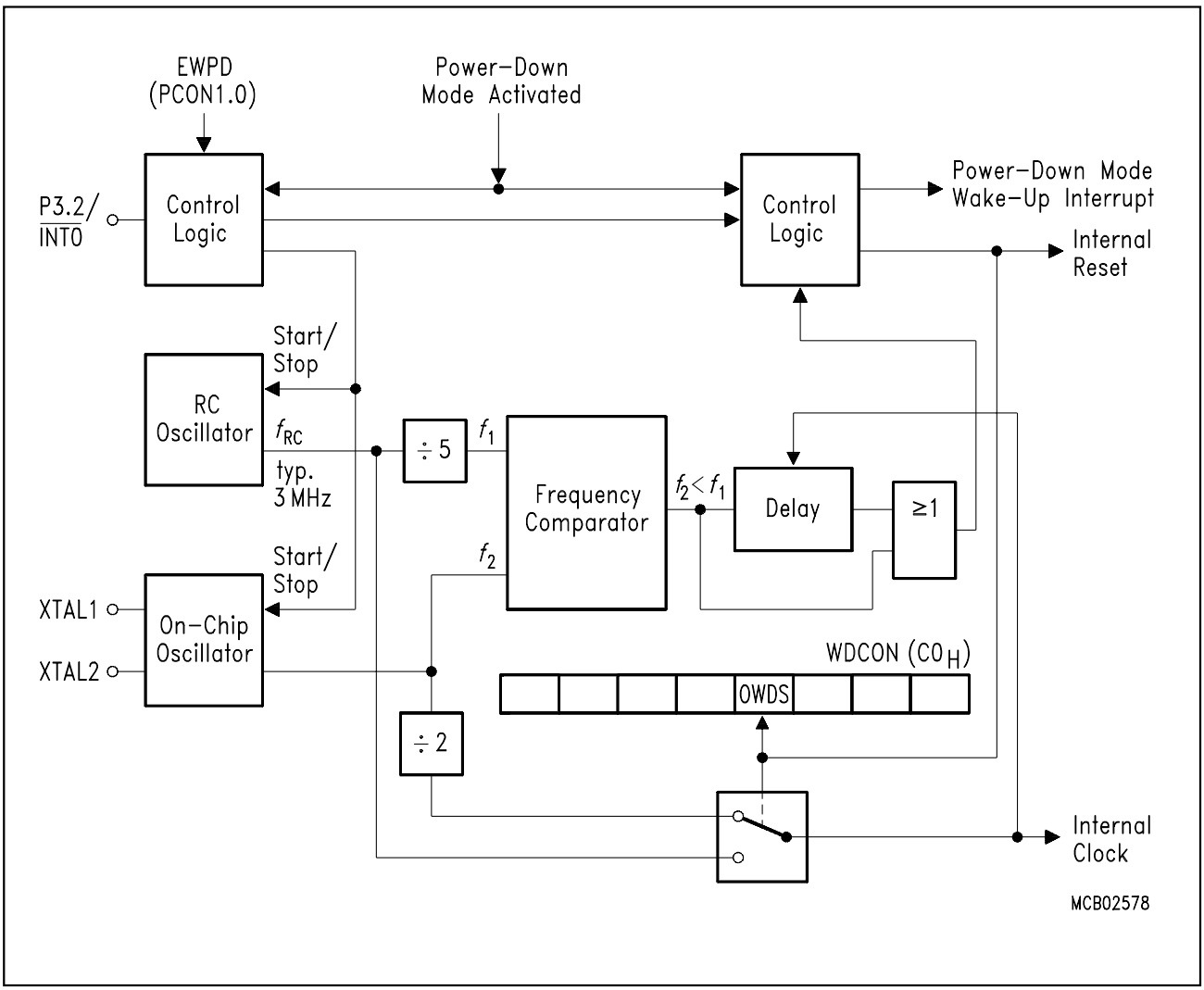


Figure 8-2
Functional Block Diagram of the Oscillator Watchdog

The frequency coming from the RC oscillator is divided by 5 and compared to the on-chip oscillator's frequency. If the frequency coming from the on-chip oscillator is found lower than the frequency derived from the RC oscillator the watchdog detects a failure condition (the oscillation at the on-chip oscillator could stop because of crystal damage etc.). In this case it switches the input of the internal clock system to the output of the RC oscillator. This means that the part is being clocked even if the on-chip oscillator has stopped or has not yet started. At the same time the watchdog activates the internal reset in order to bring the part in its defined reset state. The reset is performed because clock is available from the RC oscillator. This internal watchdog reset has the same effects as an externally applied reset signal with the following exceptions: The Watchdog Timer Status flag

WDTS is not reset (the Watchdog Timer however is stopped); and bit OWDS is set. This allows the software to examine error conditions detected by the Watchdog Timer even if meanwhile an oscillator failure occured.

The oscillator watchdog is able to detect a recovery of the on-chip oscillator after a failure. If the frequency derived from the on-chip oscillator is again higher than the reference the watchdog starts a final reset sequence which takes typ. 1 ms. Within that time the clock is still supplied by the RC oscillator and the part is held in reset. This allows a reliable stabilization of the on chip oscillator. After that, the watchdog toggles the clock supply back to the on-chip oscillator and releases the reset request. If no external reset is applied in this moment the part will start program execution. If an external reset is active, however, the device will keep the reset state until also the external reset request disappears.

Furthermore, the status flag OWDS is set if the oscillator watchdog was active. The status flag can be evaluated by software to detect that a reset was caused by the oscillator watchdog. The flag OWDS can be set or cleared by software. An external reset request, however, also resets OWDS (and WDTS).

If software power-down mode is activated the RC oscillator and the on-chip oscillator is stopped. Both oscillators are again started in power-down mode when a low level is detected at the $\overline{\text{INT0}}$ input pin and when bit EWPD in SFR PCON1 is set (wake-up from power-down mode enabled). After the start-up phase of the watchdog circuitry in power-down mode, a power-down mode wake-up interrupt is generated (instead of an internal reset).

8.2.2 Fast Internal Reset after Power-On

The C504 can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally the members of the 8051 family (e. g. SAB 80C52) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 10 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the C504 the oscillator watchdog unit avoids this situation. After power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 microseconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip. This allows correct resetting of the part and brings all ports to the defined state. The delay time between power-on and correct reset state is max 34 µs (more details see **chapter 5.2**).

9 Power Saving Modes

The C504 allows two power saving modes of the device:

- Idle mode
- Power-down mode.

The functions of the power saving modes are controlled by bits which are located in the special function registers PCON und PCON1. PCON is located at address 87_H. PCON1 is located in the mapped SFR area and is accessed with RMAP=1. Bit RMAP is located in SFR SYSCON ($B1_H$) bit 4.

The bits PDE, PDS and IDLE, IDLS located in SFR PCON select the power-down mode or the idle mode, respectively. If the power-down mode and the idle mode are set at the same time, power-down takes precedence.

Furthermore, register PCON contains two general purpose flags. For example, the flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an idle. Then an instruction that activates idle can also set one or both flag bits. When idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

Special Function Register PCON (Address $87_{H)}$ **Reset Value : $000X0000_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
87_H	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE	PCON

The function of the shaded bit is not described in this section.

Symbol	Function
PDS	Power-down start bit The instruction that sets the PDS flag bit is the last instruction before entering the power-down mode
IDLS	Idle start bit The instruction that sets the IDLS flag bit is the last instruction before entering the idle mode.
–	Not implemented. Reserved for future use.
GF1	General purpose flag
GF0	General purpose flag
PDE	Power-down enable bit When set, starting of the power-down is enabled
IDLE	Idle mode enable bit When set, starting of the idle mode is enabled

Special Function Register PCON1 (Mapped Address $88_{H)}$ **Reset Value : $0XXXXXXX_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
88_H	EWPD	–	–	–	–	–	–	–	PCON1

Symbol	Function
–	Reserved for future use.
EWPD	External wake-up from power-down enable bit Setting EWPD before entering power-down mode, enables the external wake-up from power-down mode capability via the pin $\overline{INT0}$ (more details see section 9.2).

9.1 Idle Mode

In the idle mode the oscillator of the C504 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, and all timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.

The reduction of power consumption, which can be achieved by this feature depends on the number of peripherals running.

If all timers are stopped and the A/D converter and the serial interface are not running, the maximum power reduction can be achieved. This state is also the test condition for the idle mode I_{CC}.

So the user has to take care which peripheral should continue to run and which has to be stopped during idle mode. Also the state of all port pins – either the pins controlled by their latches or controlled by their secondary functions – depends on the status of the controller when entering idle mode.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. This applies to the serial interface in case it cannot finish reception or transmission during normal operation. The control signals ALE and $\overline{\text{PSEN}}$ hold at logic high levels.

Table 9-1
Status of External Pins During Idle and Power-Down Mode

Outputs	Last Instruction Executed from Internal Code Memory		Last Instruction Executed from External Code Memory	
	Idle	**Power-Down**	**Idle**	**Power-Down**
ALE	High	Low	High	Low
$\overline{\text{PSEN}}$	High	Low	High	Low
PORT 0	Data	Data	Float	Float
PORT2	Data	Data	Address	Data
PORT3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output

As in normal operation mode, the ports can be used as inputs during idle mode. Thus a capture or reload operation can be triggered, the timers can be used to count external events, and external interrupts will be detected.

The idle mode is a useful feature which makes it possible to "freeze" the processor's status - either for a predefined time, or until an external event reverts the controller to normal operation, as discussed below. The watchdog timer is the only peripheral which is automatically stopped during idle mode.

The idle mode is entered by two consecutive instructions. The first instruction sets the flag bit IDLE (PCON.0) and must not set bit IDLS (PCON.5), the following instruction sets the start bit IDLS (PCON.5) and must not set bit IDLE (PCON.0). The hardware ensures that a concurrent setting of both bits, IDLE and IDLS, does not initiate the idle mode. Bits IDLE and IDLS will automatically be cleared after being set. If one of these register bits is read the value that appears is 0. This double instruction is implemented to minimize the chance of an unintentional entering of the idle mode which would leave the watchdog timer's task of system protection without effect.

Note:

PCON is not a bit-addressable register, so the above mentioned sequence for entering the idle mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000001B     ;Set bit IDLE, bit IDLS must not be set
ORL     PCON,#00100000B     ;Set bit IDLS, bit IDLE must not be set
```

The instruction that sets bit IDLS is the last instruction executed before going into idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

9.2 Power-Down Mode

In the power-down mode, the RC osciillator and the on-chip oscillator which operates with the XTAL pins is stopped. Therefore all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFR's are maintained. The port pins, which are controlled by their port latches, output the values that are held by their SFR's. The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power-down mode. ALE and $\overline{\text{PSEN}}$ hold at logic low level (see **table 9-1**). The power-down mode can be left either by an active reset signal or by a low signal at the $\overline{\text{INT0}}$ pin. Using reset to leave power-down mode puts the microcontroller with its SFRs into the reset state. Using the $\overline{\text{INT0}}$ pin for power-down mode maintains the state of the SFRs, which has been frozen when power-down mode is entered.

In the power-down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that is V_{CC} not reduced before the power-down mode is invoked, and that V_{CC} is restored to its normal operating level before the power-down mode is terminated.

9.2.1 Invoking Power-Down Mode

The power-down mode is entered by two consecutive instructions. The first instruction has to set the flag bit PDE (PCON.1) and must not set bit PDS (PCON.6), the following instruction has to set the start bit PDS (PCON.6) and must not set bit PDE (PCON.1). The hardware ensures that a concurrent setting of both bits, PDE and PDS, does not initiate the power-down mode. Bits PDE and PDS will automatically be cleared after having been set and the value shown by reading one of these bits is always 0. This double instruction is implemented to minimize the chance of unintentionally entering the power-down mode which could possibly ”freeze” the chip's activity in an undesired status.

PCON is not a bit-addressable register, so the above mentioned sequence for entering the power-down mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000010B     ;set bit PDE, bit PDS must not be set
ORL     PCON,#01000000B     ;set bit PDS, bit PDE must not be set, enter power-down
```

The instruction that sets bit PDS is the last instruction executed before going into power-down mode. When the double instruction sequence shown above is used and when bit EWPD in SFR PCON1 is 0, the power-down mode can only be left by a reset operation.

If the external wake-up from power-down capability should be used, its function must be enabled using the following instruction sequence prior to executing the double instruction sequence shown above.

```
ORL     SYSCON,#00010000B   ;set RMAP
ORL     PCON1,#80H          ;enable external wake-up from power-down by setting EWPD
ANL     SYSCON,#11101111B   ;reset RMAP (for future SFR accesses)
```

Notes : Before entering the power-down mode, an A/D conversion in progress should be stopped. Further, the port latch of SFR P3.2 (P3.2 / $\overline{\text{INT0}}$ pin) should contain a “1“ (pin operates as input). Otherwise, the wake-up sequence discussed in the next chapter will be started immediately when power-down mode is entered.

9.2.2 Exit from Power-Down

If power-down mode is exit via a hardware reset, the microcontroller with its SFRs is put into the hardware reset state and the content of RAM and XRAM are not changed. The reset signal that terminates the power-down mode also restarts the RC oscillator and the on-chip oscillatror. The reset operation should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Figure 9-1 shows the procedure which must is executed when power-down mode is left via the $\overline{\text{INT0}}$ wake-up capability.

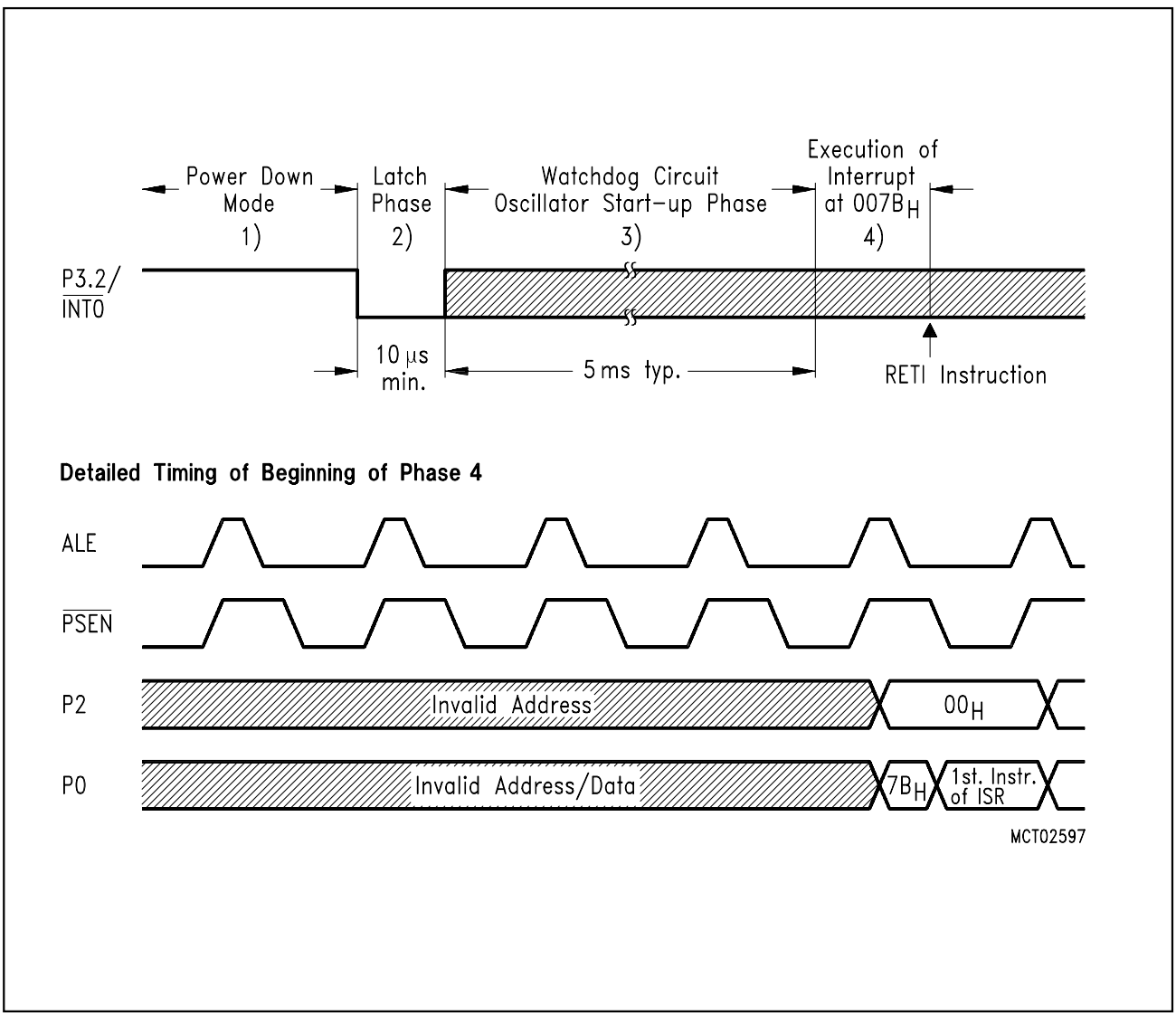


Figure 9-1
Wake-up from Power-Down Mode Procedure

When the power-down mode wake-up capability has been enabled (bit EWPD in SFR PCON1 set) prior to entering power down mode, the power-down mode can be exit via $\overline{INT0}$ while executing the following procedure :

1. In power-down mode pin $\overline{INT0}$ must be held at high level.
2. Power-down mode is left when $\overline{INT0}$ goes low. With $\overline{INT0}$ = low the internal RC oscillator is started. $\overline{INT0}$ is then latched by the RC oscillator clock signal. Therefore, $\overline{INT0}$ should be held at low level for at least 10 µs (latch phase). After this delay $\overline{INT0}$ can be set again to high level if required. Thereafter, the oscillator watchdog unit controls the wake-up procedure in its start-up phase.
3. The oscillator watchdog unit starts operation as described in **section 8.2.1**. When the on-chip oscillator clock is detected for stable nominal frequency, the microcontroller further waits for a delay of typically 5 ms and then starts again with its operation initiating the power-down wake-up interrupt. The interrupt address of the first instruction to be executed after wake-up is $007B_H$.
4. After the RETI instruction of the power-down wake-up interrupt routine has been executed, the instruction which follows the initiating power-down mode double instruction sequence will be executed. The peripheral units timer 0/1/2 , CCU, and WDT are frozen until end of phase 4.

All interrupts of the C504 are disabled from phase 2) until the end of phase 4). Other Interrupts can be first handled after the RETI instruction of the wake-up interrupt routine.

10 OTP Memory Operation

The C504-2E is the OTP version in the C504 microcontroller with a 16K byte one-time programmable (OTP) program memory. With the C504-2E fast programming cycles are achieved (1 byte in 100 µsec). Also several levels of OTP memory protection can be selected. The basic functionality of the C504-2E as microcontroller is identical to the C504-2R (ROM part) or C504-L (romless part) functionality. Therefore, the programmable C504-2E typically can be used for prototype system design as a replacement for the ROM-based C504-2R microcontroller.

10.1 Programming Configuration

During normal program execution the C504-2E behaves like the C504-2R/C504-L. For programming of the device, the C504-2E must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C504-2E operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5 V programming voltage.

In the programming mode port 0 provides the bidirectional data lines and port 2 is used for the multiplexed address inputs. The upper address information at port 2 is latched with the signal PALE. For basic programming mode selection the inputs RESET, $\overline{PSEN}$, $\overline{EA}/V_{PP}$, ALE, PMSEL1/0, and PSEL are used. Further, the inputs PMSEL1,0 are required to select the access types (e.g. program/verify data, write lock bits, ...) in the programming mode. In programming mode V_{CC}/V_{SS} and a clock signal at the XTAL pins must be applied to the C504-2E. The 11.5 V external programming voltage is input through the $\overline{EA}/V_{PP}$ pin.

Figure 10-1 shows the pins of the C504-2E which are required for controlling of the OTP programming mode.

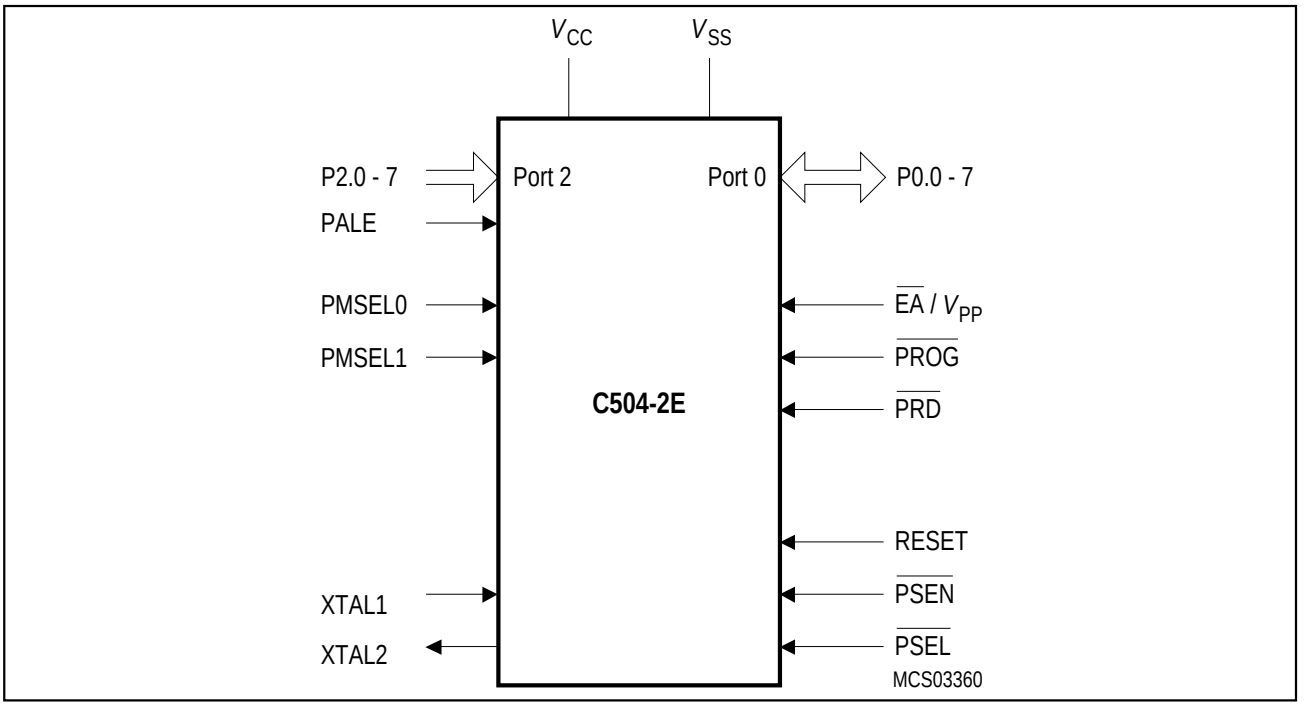


Figure 10-1
C504-2E Programming Mode Configuration

10.2 Pin Configuration

Figure 10-2 shows the detailed pin configuration of the C504-2E in programming mode.

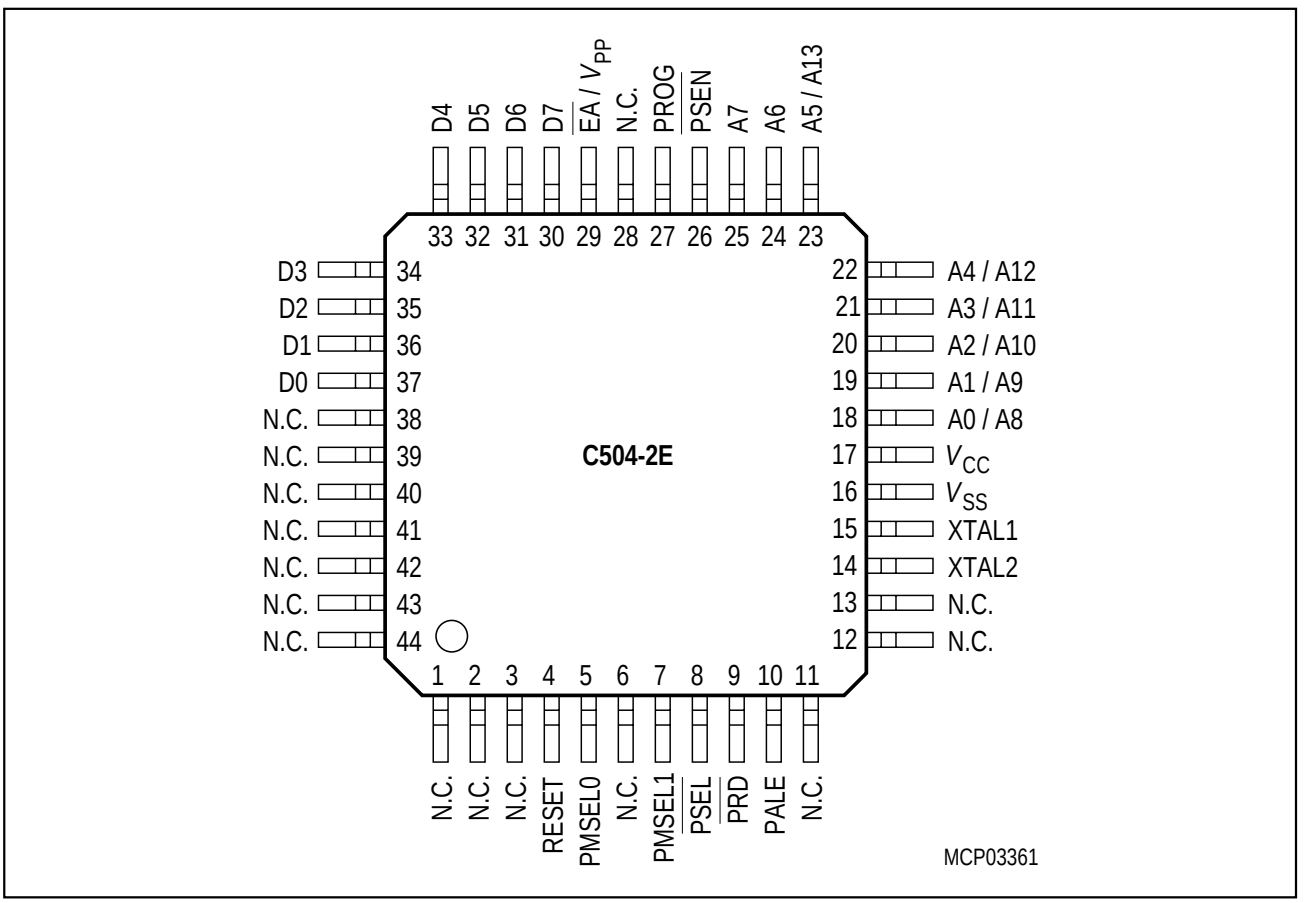


Figure 10-2
Pin Configuration of the C504-2E in Programming Mode (Top View)

10.3 Pin Definitions

The following **table 10-1** contains the functional description of all C504-2E pins which are required for OTP memory programming.

Table 10-1
Pin Definitions and Functions of the C504-2E in Programming Mode

Symbol	Pin Number P-MQFP-44	I/O*)	Function
RESET	4	I	**Reset** This input must be at static “1“ (active) level during the whole programming mode.
PMSEL0 PMSEL1	5 7	I I	**Programming mode selection pins** These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
$\overline{\text{PSEL}}$	8	I	**Basic programming mode select** This input is used for the basic programming mode selection and must be switched according **figure 10-3**.
$\overline{\text{PRD}}$	9	I	**Programming mode read strobe** This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.
PALE	10	I	**Programming address latch enable** PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level when the logic level of PMSEL1,0 is changed.
XTAL2	14	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	I	**XTAL1** Input to the oscillator amplifier.

PMSEL1	PMSEL0	Access Mode
0	0	Reserved
0	1	Read version bytes
1	0	Program/read lock bits
1	1	Program/read OTP memory byte

*) I = Input
O = Output

Table 10-1
Pin Definitions and Functions of the C504-2E in Programming Mode (cont'd)

Symbol	Pin Number P-MQFP-44	I/O*)	Function
V_{SS}	16	–	**Circuit ground potential** must be applied in programming mode.
V_{CC}	17	–	**Power supply terminal** must be applied in programming mode.
P2.0-7	18-25	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A13. A8-A13 must be latched with PALE.
$\overline{PSEN}$	26	I	**$\overline{Program\ store\ enable}$** This input must be at static "0" level during the whole programming mode.
$\overline{PROG}$	27	I	**$\overline{Programming\ mode\ write\ strobe}$** This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations During basic programming mode selection a low level must be applied to $\overline{PROG}$.
$\overline{EA}/V_{PP}$	29	–	**$\overline{External\ access}$ / programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at high level (V_{IH}). This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{EA}/V_{PP}$.
P0.7-0	30-37	I/O	**Data lines 0-7** During programming mode, data bytes are read or written from or to the C504-2E via the bidirectional D7-0 data lines which are located at port 0.
N.C.	1-3, 6, 11-13, 28, 38-44	–	**Not Connected** These pins should not be connected in programming mode.

*) I = Input
O = Output

10.4 Programming Mode Selection

The selection for the OTP programming mode can be separated into two different parts :

- Basic programming mode selection
- Access mode selection

With the basic programming mode selection the device is put into the mode in which it is possible to access the OTP memory through the programming interface logic. Further, after selection of the basic programming mode, OTP memory accesses are executed by using one of the access modes. These access modes are OTP memory byte program/read, version byte read, and program/read lock byte operations.

10.4.1 Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **figure 10-3**.

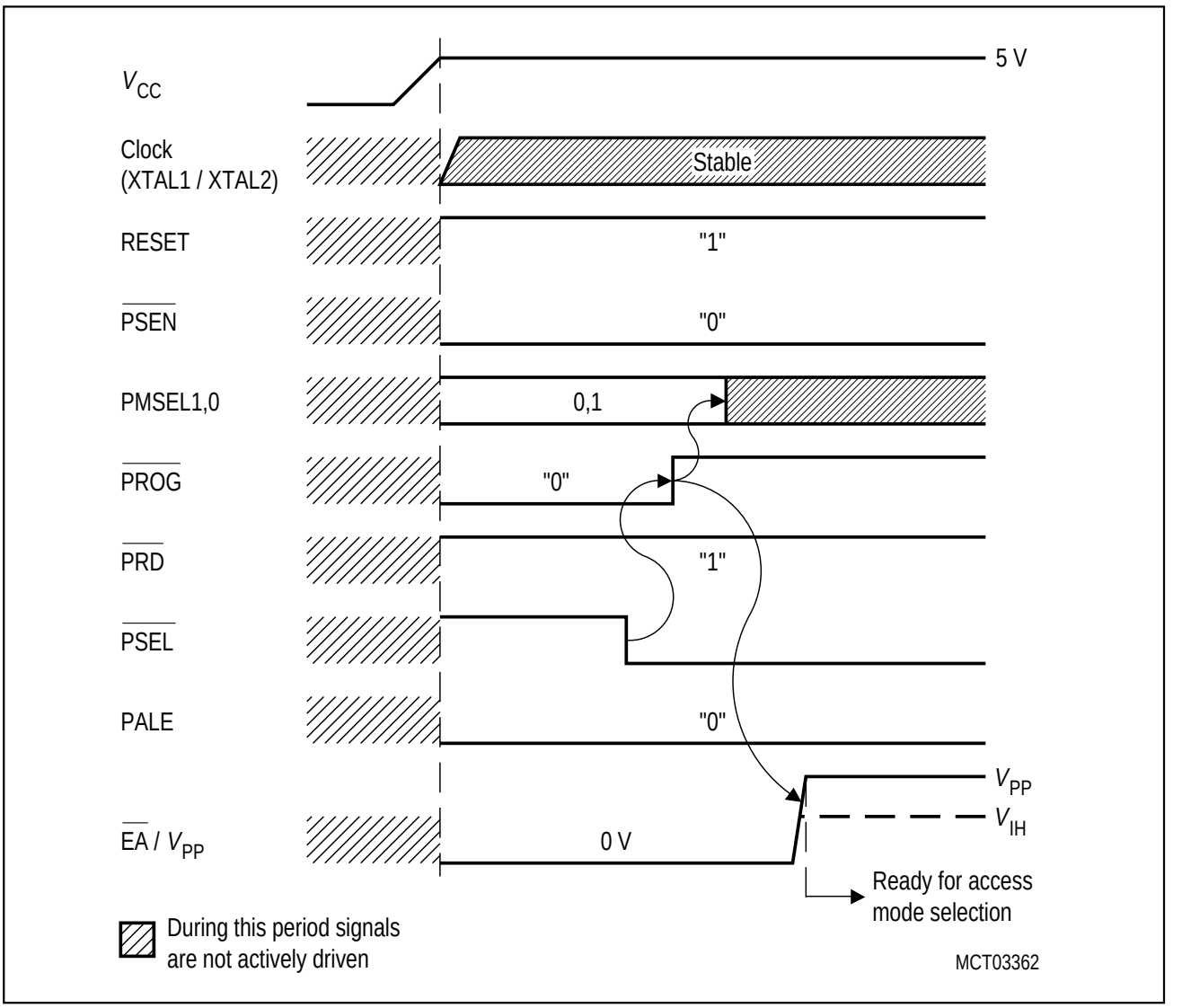


Figure 10-3
Basic Programming Mode Selection

The basic programming mode is selected by executing the following steps :

- With a stable Vcc a clock signal is applied to the XTAL pins; the RESET pin is set to “1“ level and the $\overline{PSEN}$ pin is set to “0“ level.
- $\overline{PROG}$, PALE, PMSEL1 and $\overline{EA}/V_{PP}$ are set to “0“ level; $\overline{PRD}$, $\overline{PSEL}$, and PMSEL0 are set to “1“ level.
- $\overline{PSEL}$ is set to from “1“ to “0“ level and thereafter $\overline{PROG}$ is switched to “1“ level.
- PMSEL1,0 can now be changed; after $\overline{EA}/V_{PP}$ has been set to V_{IH} high level or to V_{PP} the OTP memory is ready for access.

The pins RESET and $\overline{PSEN}$ must stay at “1“ respectively “0“ static signal level during the whole programming mode. With a falling edge of $\overline{PSEL}$ the logic state of $\overline{PROG}$ and $\overline{EA}/V_{PP}$ is internally latched. These two signals are now used as programming write pulse signal ($\overline{PROG}$) and as programming voltage input pin V_{PP}. After the falling edge of $\overline{PSEL}$, $\overline{PSEL}$ must stay at “0“ state during all programming operations.

Note: If protection level 1 to 3 has been programmed (see section 10.6) and the programming mode has been left, it is no more possible to enter the programming mode !

10.4.2 OTP Memory Access Mode Selection

When the C504-2E has been put into the programming mode using the basic programming mode selection, several access modes of the OTP memory programming interface are available. The conditions for the different control signals of these access modes are listed in **table 10-2**.

Table 10-2
Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-15	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1,D0 see **table 10-3**
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of version byte	D0-7

The access modes from the table above are basically selected by setting the two PMSEL1,0 lines to the required logic level. The $\overline{PROG}$ and $\overline{PRD}$ signal are the write and read strobe signal. Data is transfered via port 0 and addresses are applied to port 2.

The following sections describes the details of the different access modes.

10.5 Program / Read OTP Memory Bytes

The program/read OTP memory byte access mode is defined by PMSEL1,0 = 1,1. It is initiated when the PMSEL1,0 = 1,1 is valid at the rising edge of PALE. With the falling edge of PALE the upper addresses A8-A13 of the 14-bit OTP memory address are latched. After A8-A13 has been latched, A0-A7 is put on the address bus (port 2). A0-A7 must be stable when $\overline{\text{PROG}}$ is low or $\overline{\text{PRD}}$ is low. If subsequent OTP address locations are accessed with constant address information at the high address lines A8-13, A8-A13 must only be latched once (page address mechanism).

Figure 10-4 shows a typical OTP memory programming cycle with a following OTP memory read operation. In this example A0-A13 of the read operation are identical to A8-A13 of the preceeding programming operation.

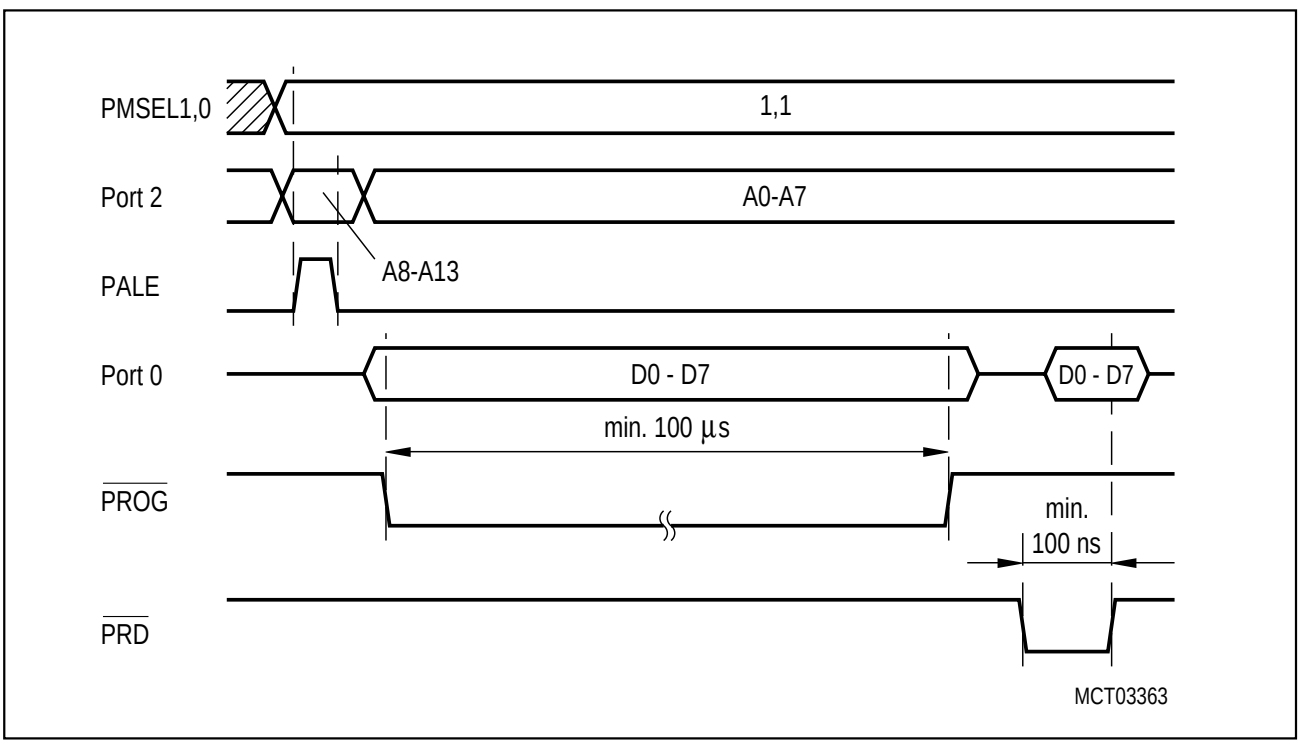


Figure 10-4
Programming / Verify OTP Memory Access Waveform

If the address lines A8-A13 must be updated, PALE must be activated for the latching of the new A8-A13 value. Control, address, and data information must only be switched when the $\overline{\text{PROG}}$ and $\overline{\text{PRD}}$ signals are at high level. The PALE high pulse must always be executed if a different access mode has been used prior to the actual access mode.

Figure 10-5 shows a waveform example of the program/read mode access for several OTP memory bytes. In this example OTP memory locations $3FD_H$ to 400_H are programmed. Thereafter, OTP memory locations 400_H and $3FD_H$ are read.

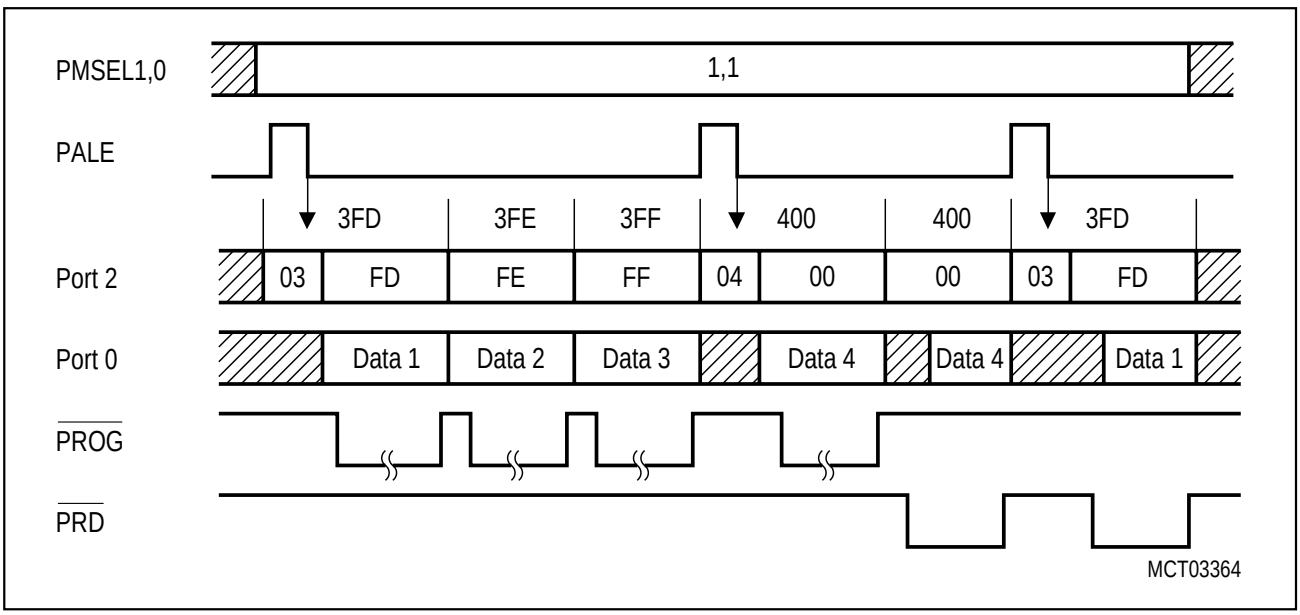


Figure 10-5
Typical OTP Memory Programming/Verify Access Waveform

10.6 Lock Bits Programming / Read

The C504-2E has two programmable lock bits which, when programmed according **tabie 10-3**, provide four levels of protection for the on-chip OTP program memory.

Table 10-3
Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	**D0**		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C504-2E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C504-2E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset.An OTP memory read operation is only possible according to ROM/OTP verification mode 2. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using ROM verification mode 2 is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C504-2E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

Note : A 1 means that the lock bit is unprogrammed. 0 means that lock bit is programmed.

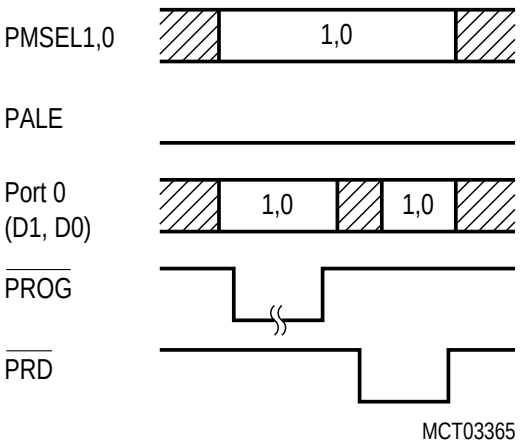
For a OTP verify operation at protection level 1, the C504-2E must be put into the ROM verification mode 2.

If a device is programmed with protection level 2 or 3, it is no more possible to verify the OTP content of a customer rejected (FAR) OTP device.

When a protection level has been activated by programming of the lock bits, the basic programming mode must be left for activation of the protection mechanisms. This means, after the activation of a protection level further OTP program/verify operations are still possible if the basic programming mode is maintained.

The state of the lock bits can always be read if protection level 0 is selected. If protection level 1 to 3 has been programmed and the programming mode has been left, it is no more possible to enter the programming mode: In this case, also the lock bits cannot be read anymore.

Figure 10-6 shows the waveform of a lock bit write/read access. For a simple drawing, the $\overline{PROG}$ pulse is shortened. In reality, for lock bit programming, a 100µs $\overline{PROG}$ low pulsw must be applied.



The example shows the programming and reading of a protection level 1.

Figure 10-6
Write/Read Lock Bit Waveform

10.7 Access of Version Bytes

The C504-2E and C504-2R provide three version bytes at address locations FC_H, FD_H, and FE_H. The information stored in the version bytes, is defined by the mask of each microcontroller step, Therefore, the version bytes can be read but not written. The three version bytes hold information as manufacturer code, device type, and stepping code.

For reading of the version bytes the control lines must be used according **table 10-2** and **figure 10-7**. The address of the version byte must be applied at the port 1 address lines. PALE must not be activated.

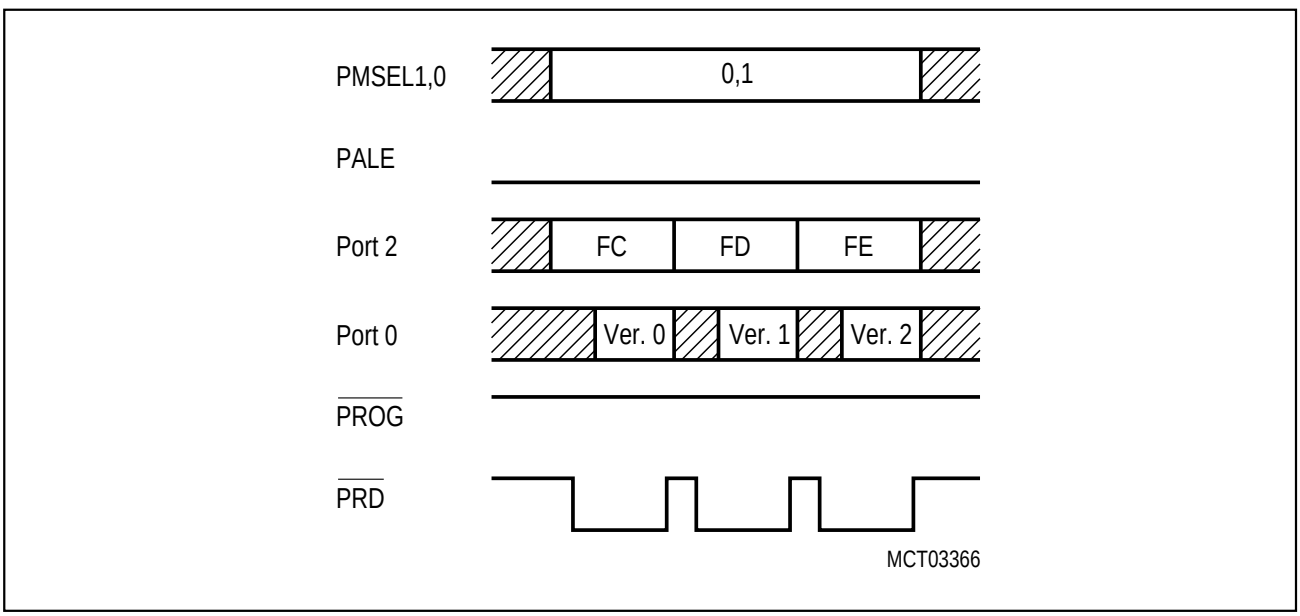


Figure 10-7
Read Version Byte(s) Waveform

Version bytes are typically used by programming systems for adapting the programming firmware to specifc device characteristics such as OTP size etc.

Note: The 3 version bytes are implemented in a way that they can be also read during normal program execution mode as a mapped SFR when bit RMAP in SFR SYSCON is set. The SFR addresses of the version bytes in normal mode are identical to the addresses which are used in programming mode. Therefore, in normal operating mode of the C504-2E or C504-2R, the SFR locations which hold the version bytes are also referenced as version registers.

The steppings of the C504 contain the following version byte/register information :

Table 10-4
Version Register/Byte Content

Stepping	Version Byte 0 = VR0 (mapped addr. FC_H)	Version Byte 1 = VR1 (mapped addr. FD_H)	Version Byte 2 = VR2 (mapped addr. FE_H)
C504-2R AC-Step	$C5_H$	04_H	01_H
C504-2E ES-AA-Step	$C5_H$	84_H	01_H
C504-2E AB-Step	$C5_H$	84_H	02_H

Future steppings of the C504 will typically have a different version byte 2 (incremented value).

11 Device Specifications

11.1 Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 ˚C to + 70 ˚C
Storage temperature (T_{ST}) .....– 65 ˚C to + 150 ˚C

Voltage on V_{CC} pins with respect to ground (V_{SS}) .....– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....– 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition.....– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....| 100 mA |

Power dissipation.....TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

11.2 DC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET, $\overline{CTRAP}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET, $\overline{CTRAP}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, RESET and $\overline{CTRAP}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	11)
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to RESET and $\overline{CTRAP}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3, COUT3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA 1)
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA 1)
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (ports 1,3 pins in push-pull mode and COUT3)	V_{OH1}	0.9 V_{CC}	–	V	I_{OH} = – 800 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH2}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA 2), I_{OH} = – 80 µA 2)
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	7) 8)
Programming voltage (C504-2E)	V_{PP}	10.9	12.1	V	11.5 V ± 5% 10)

Notes see next page

Power Supply Current

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ. [8]	max. [9]		
Active mode	C504-2R	24 MHz 40 MHz	I_{CC} I_{CC}	27.4 43.1	35.9 57.2	mA mA	[4]
	C504-2E	24 MHz 40 MHz	I_{CC} I_{CC}	20.9 31.0	27.9 41.5	mA mA	
Idle mode	C504-2R	24 MHz 40 MHz	I_{CC} I_{CC}	14.6 22.4	19.3 31.3	mA mA	[5]
	C504-2E	24 MHz 40 MHz	I_{CC} I_{CC}	12.3 16.1	16.1 20.9	mA mA	
Power-down mode	C504-2R		I_{PD}	1	30	µA	V_{CC} = 2…5.5 V [3]
	C504-2E		I_{PD}	35	60	µA	
At $\overline{EA}$/V_{PP} in prog. mode	C504-2E		I_{CCP}	–	30	mA	

Notes:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (power-down mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC} ; RESET = V_{SS} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; V_{AGND} = V_{SS} ; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = Port1 = RESET = V_{CC} ; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{CC} ; all other pins are disconnected;

6) Overload conditions occur if the standard operating conditions are exeeded, ie. the voltage on any pin exeeds the specified range (i.e. V_{OV} > V_{CC} + 0.5 V or V_{OV} < V_{SS} – 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

7) Not 100 % tested, guaranteed by design characterization

8) The typical I_{CC} values are periodically measured at T_A = +25 ˚C and V_{CC} = 5 V but not 100% tested.

9) The maximum I_{CC} values are measured under worst case conditions (T_A = 0 ˚C or -40 ˚C and V_{CC} = 5.5 V)

10) This V_{PP} specification is valid for devices with version byte 2 = 02H or higher. Devices with version byte 2 = 01H must be programmed with V_{PP} = 12V ± 5%.

11) For the C504-2E ES-AA-step the V_{IH} min for $\overline{EA}$ is 0.8 V_{CC}.

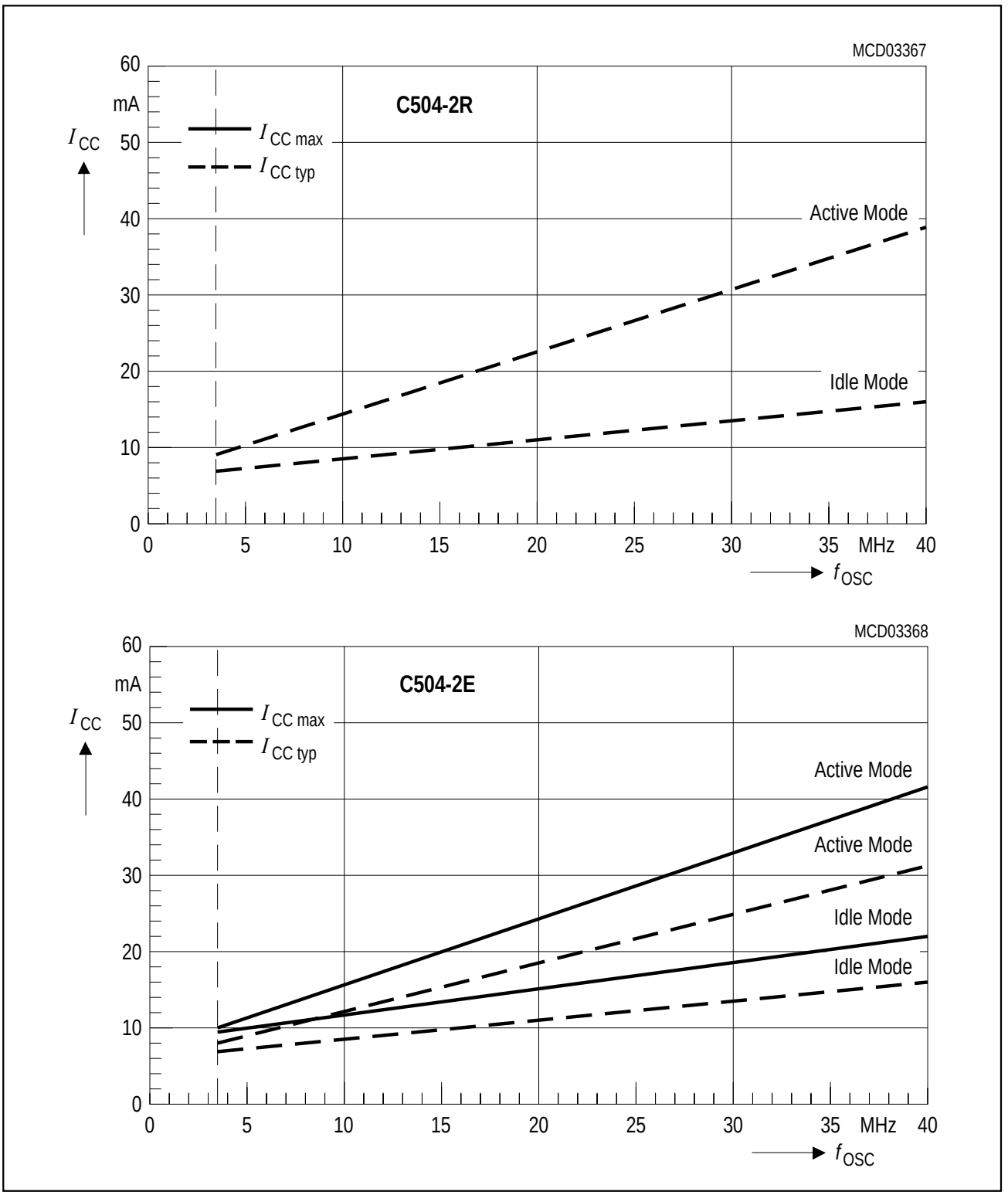


Figure 11-1
ICC Diagram

Power Supply Current Calculation Formulas

Parameter		Symbol	Formula
Active mode	C504-2R	$I_{CC\ typ}$ $I_{CC\ max}$	0.98 x f_{OSC} + 3.9 1.33 x f_{OSC} + 4.0
	C504-2E	$I_{CC\ typ}$ $I_{CC\ max}$	0.63 x f_{OSC} + 5.75 0.85 x f_{OSC} + 7.5
Idle mode	C504-2R	$I_{CC\ typ}$ $I_{CC\ max}$	0.51 x f_{OSC} + 2.35 0.75 x f_{OSC} + 1.3
	C504-2E	$I_{CC\ typ}$ $I_{CC\ max}$	0.24 x f_{OSC} + 6.5 0.30 x f_{OSC} + 8.86

Note : f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA.

11.3 A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
4V ≤ V_{AREF} ≤ V_{CC} + 0.1 V;
V_{SS} – 0.1 V ≤ V_{AGND} ≤ V_{SS} + 0.2 V;

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	384 x t_{IN} 192 x t_{IN} 96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS} + 0.5V ≤ V_{IN} ≤ V_{CC} – 0.5V 4)
		–	± 4	LSB	V_{SS} < V_{IN} < V_{SS} + 0.5V V_{CC} – 0.5V < V_{IN} < V_{CC} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 – 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 – 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	384 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	192 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
t_{IN} = 2 / f_{OSC} = 2 t_{CLCL}

Notes:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{CC} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100 % tested, but guaranteed by design characterization.

11.4 AC Characteristics for C504-L / C504-2R / C504-2E

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	30	–	$t_{CLCL} - 23$	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C504 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L / C504-2R / C504-2E (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	114	–	$2t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	294	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

11.5 AC Characteristics for C504-L24 / C504-2R24 / C504-2E24

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	17	–	$t_{CLCL} - 25$	–	ns
Address hold after ALE	t_{LLAX}	17	–	$t_{CLCL} - 25$	–	ns
ALE low to valid instr in	t_{LLIV}	–	80	–	$4t_{CLCL} - 87$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	22	–	$t_{CLCL} - 20$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	95	–	$3t_{CLCL} - 30$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	60	–	$3t_{CLCL} - 65$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	32	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	37	–	$t_{CLCL} - 5$	–	ns
Address to valid instr in	t_{AVIV}	–	148	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C504 to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L24 / C504-2R24 / C504-2E24 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	$6t_{CLCL} - 70$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	$6t_{CLCL} - 70$	–	ns
Address hold after ALE	t_{LLAX2}	56	–	$2t_{CLCL} - 27$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	118	–	$5t_{CLCL} - 90$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	$2t_{CLCL} - 20$	ns
ALE to valid data in	t_{LLDV}	–	200	–	$8t_{CLCL} - 133$	ns
Address to valid data in	t_{AVDV}	–	220	–	$9t_{CLCL} - 155$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$	t_{AVWL}	67	–	$4t_{CLCL} - 97$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 37$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	–	$7t_{CLCL} - 122$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	–	$t_{CLCL} - 27$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	294	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

11.6 AC Characteristics for C504-L40 / C504-2R40 / C504-2E40

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	$2t_{CLCL}$ – 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	t_{CLCL} – 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	t_{CLCL} – 15	–	ns
ALE low to valid instr in	t_{LLIV}	–	55	–	$4t_{CLCL}$ – 45	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	–	t_{CLCL} – 15	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	–	$3t_{CLCL}$ – 15	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	25	–	$3t_{CLCL}$ – 50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	20	–	t_{CLCL} – 5	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	20	–	t_{CLCL} – 5	–	ns
Address to valid instr in	t_{AVIV}	–	65	–	$5t_{CLCL}$ – 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the C504 to devices with float times up to 25 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L40 / C504-2R40 / C504-2E40 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	$6t_{CLCL} - 30$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	$6t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX2}	35	–	$2t_{CLCL} - 15$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	$5t_{CLCL} - 50$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	$2t_{CLCL} - 12$	ns
ALE to valid data in	t_{LLDV}	–	150	–	$8t_{CLCL} - 50$	ns
Address to valid data in	t_{AVDV}	–	150	–	$9t_{CLCL} - 75$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	$3t_{CLCL} - 15$	$3t_{CLCL} + 15$	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	$4t_{CLCL} - 30$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	$t_{CLCL} - 15$	$t_{CLCL} + 15$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 20$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	$7t_{CLCL} - 50$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	$t_{CLCL} - 20$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	294	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	10	ns
Fall time	t_{CHCL}	–	10	ns

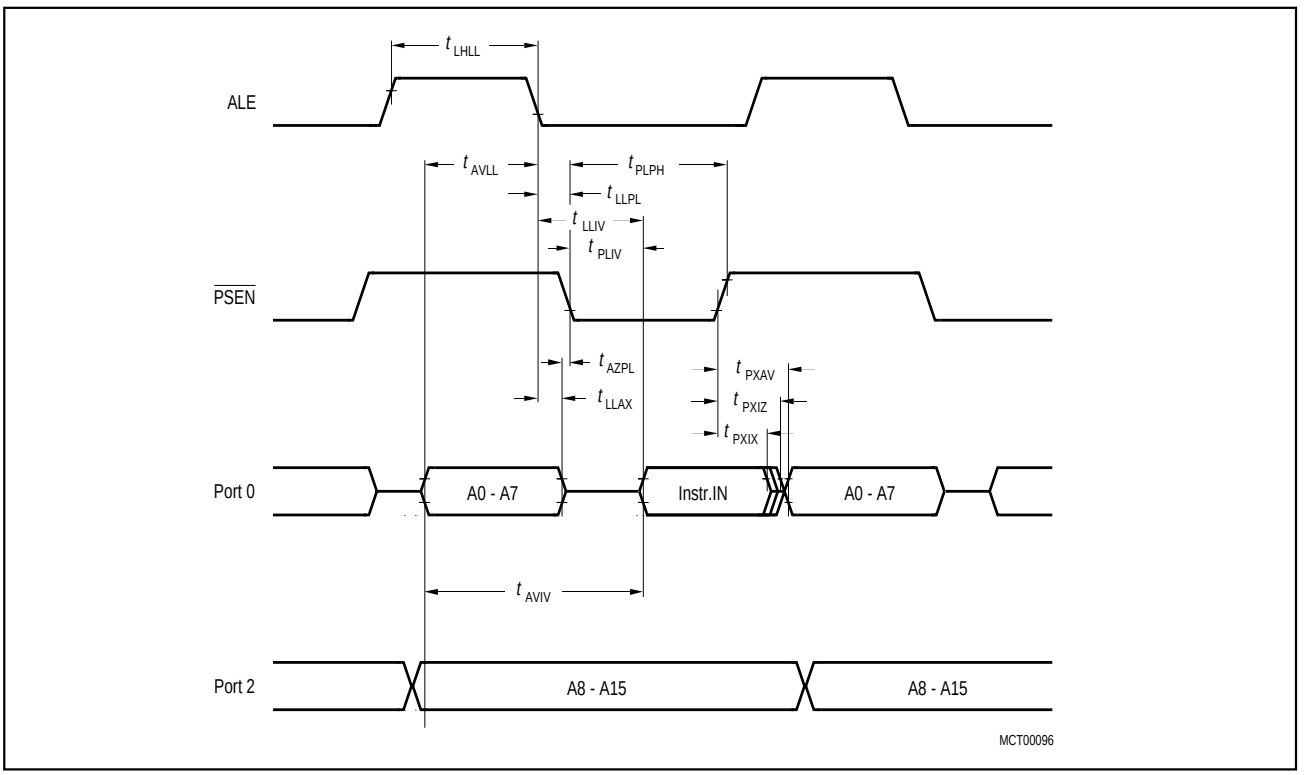


Figure 11-2
Program Memory Read Cycle

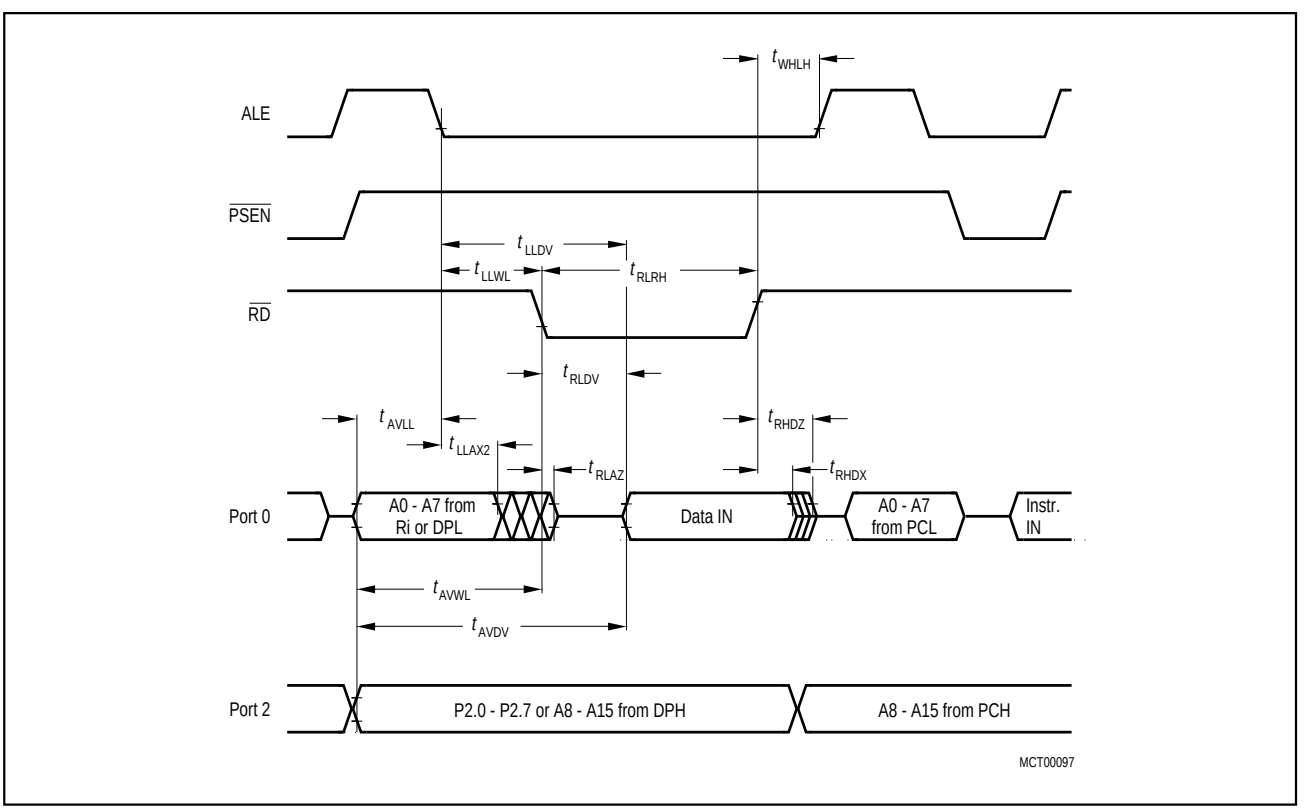


Figure 11-3
Data Memory Read Cycle

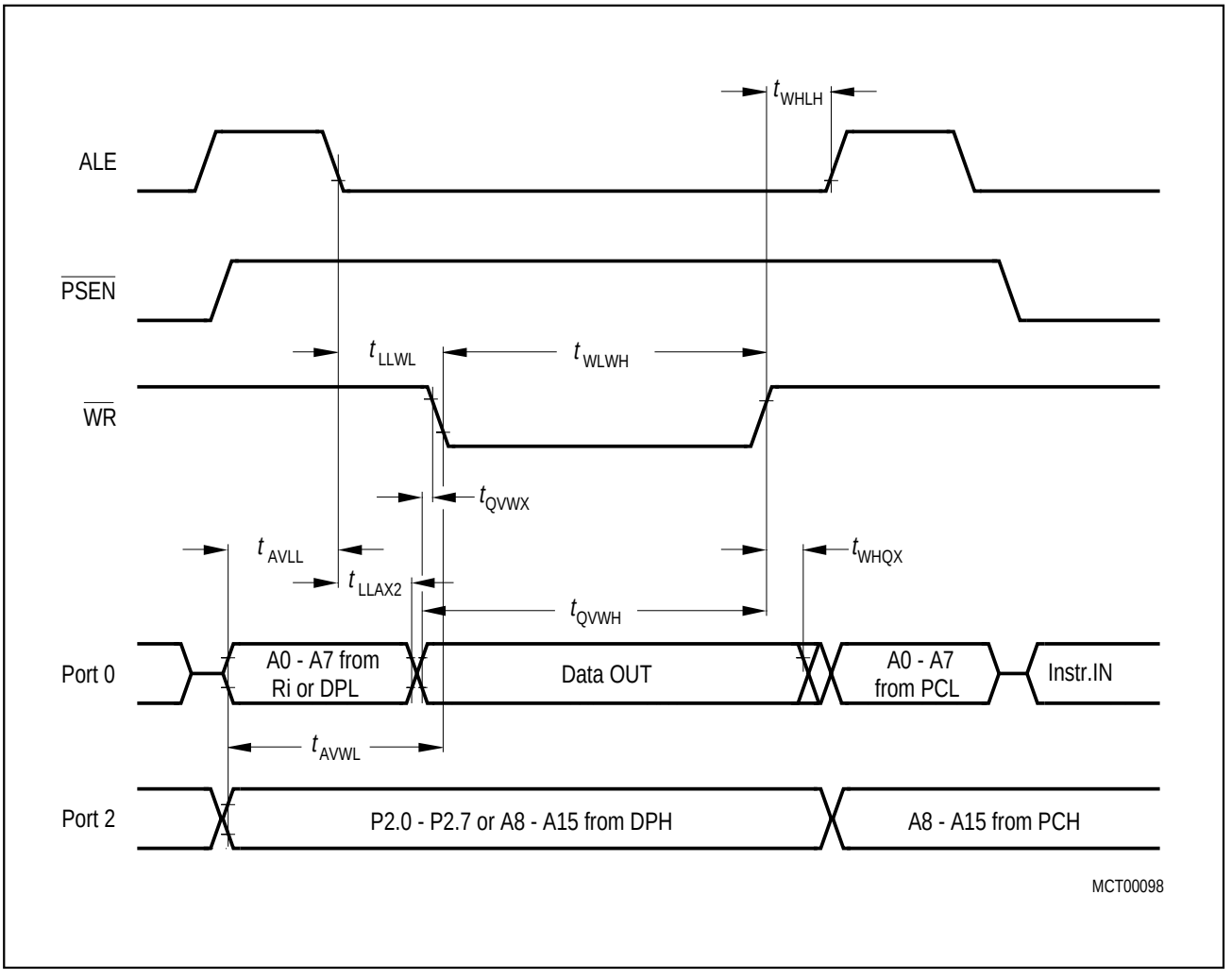


Figure 11-4
Data Memory Write Cycle

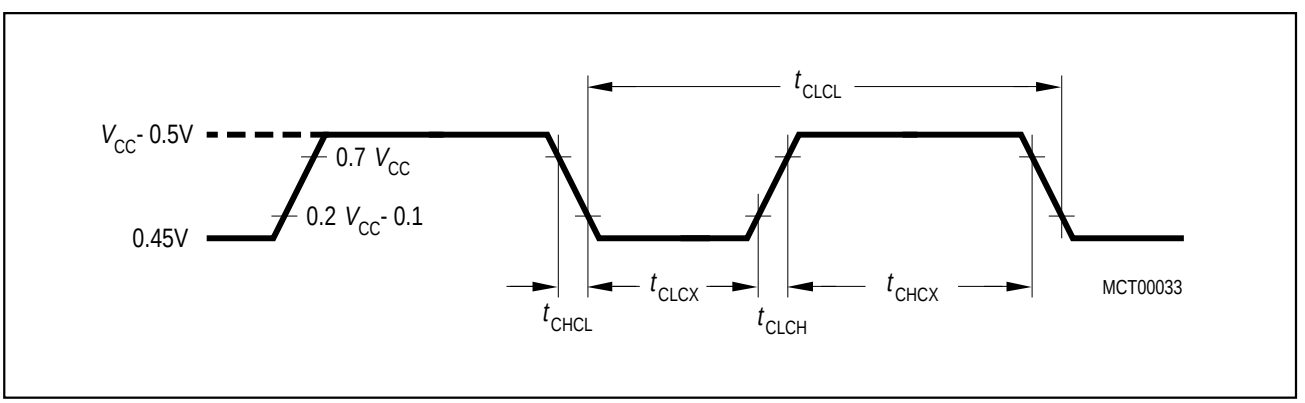


Figure 11-5
External Clock Cycle

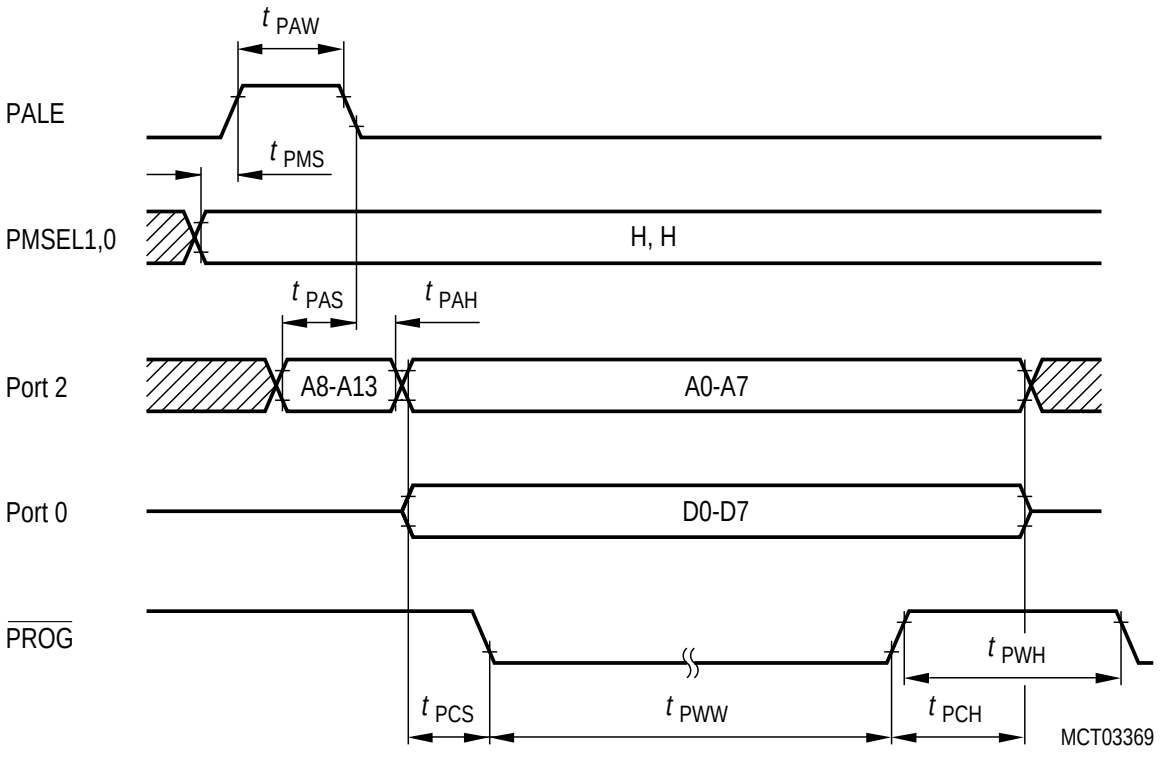
11.7 AC Characteristics of Programming Mode

V_{CC} = 5 V ± 10 %; V_{PP} = 11.5 V ± 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to ALE rising edge	t_{PMS}	10	–	
Address setup to ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100		ns
XTAL clock period	t_{CLKP}	3.5	12	MHz

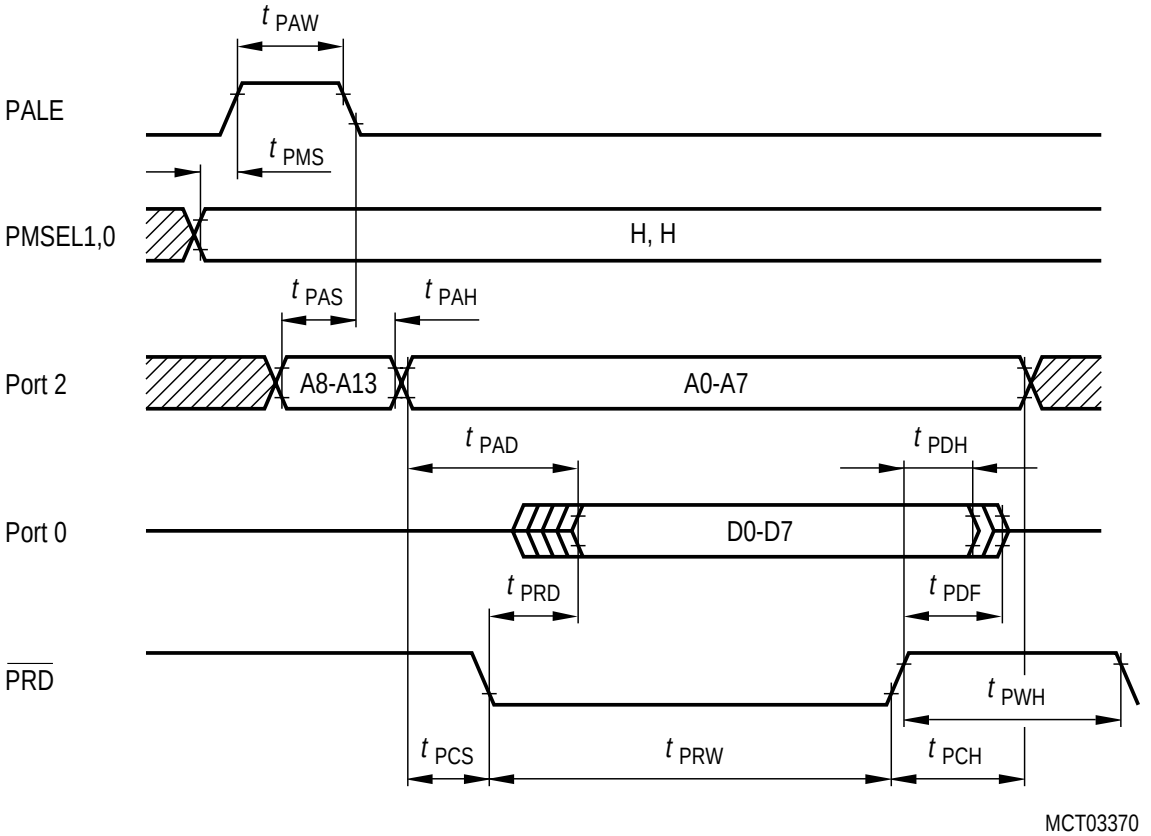
Note :

V_{PP} = 11.5 V ± 5% is valid for devices with version byte 2 = 02H or higher. Devices with version byte 2 = 01H must be programmed with V_{PP} = 12 V ± 5%.



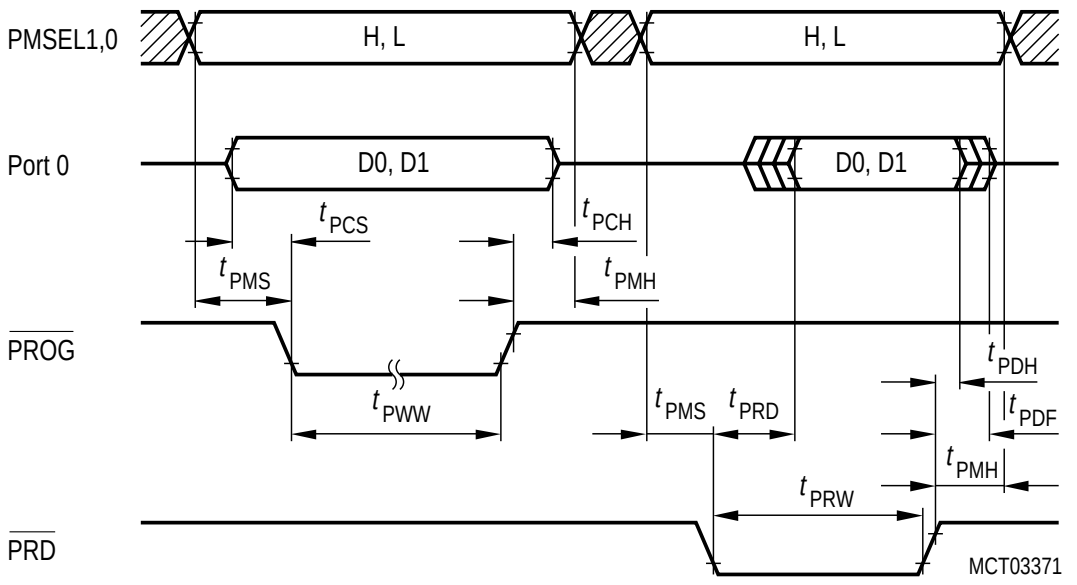
Notes : $\overline{PRD}$ must be high during a programming write cycle

Figure 11-6
Programming Code Byte - Write Cycle Timing



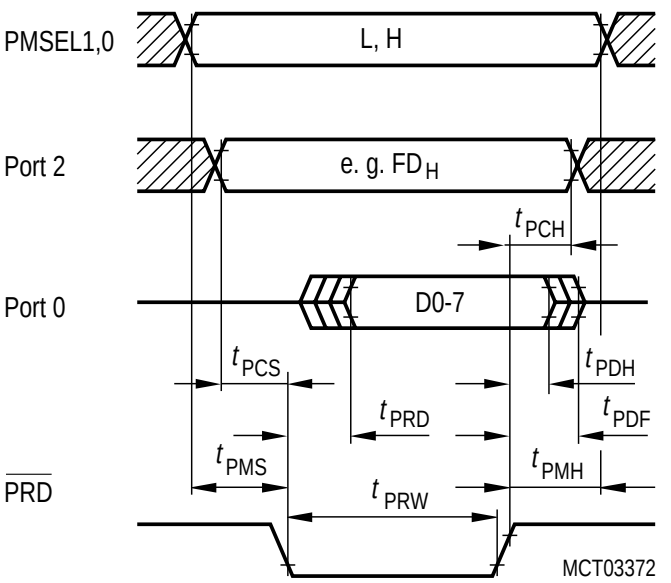
Notes : $\overline{\text{PROG}}$ must be high during a programming read cycle

Figure 11-7
Verify Code Byte - Read Cycle Timing



Note : PALE should be low during a lock bit read/write cycle

Figure 11-8
Lock Bit Access Timing



Note : $\overline{\text{PROG}}$ must be high during a programming read cycle

Figure 11-9
Version Byte Read Timing

11.8 ROM/OTP Verification Characteristics for C504-2R / C504-2E

ROM Verification Mode 1 (C504-2R only)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	10 t_{CLCL}	ns

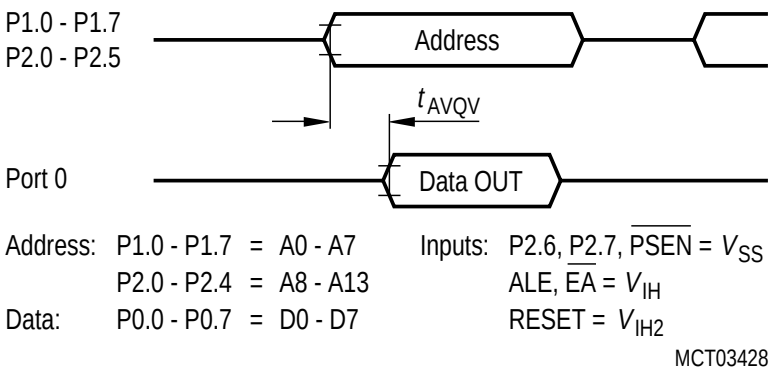


Figure 11-10
ROM Verification Mode 1

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	2 t_{CLCL}	–	ns
ALE period	t_{ACY}	–	12 t_{CLCL}	–	ns
Data valid after ALE	t_{DVA}	–	–	4 t_{CLCL}	ns
Data stable after ALE	t_{DSA}	8 t_{CLCL}	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CLCL}	–	ns
Oscillator frequency	$1/t_{CLCL}$	4	–	6	MHz

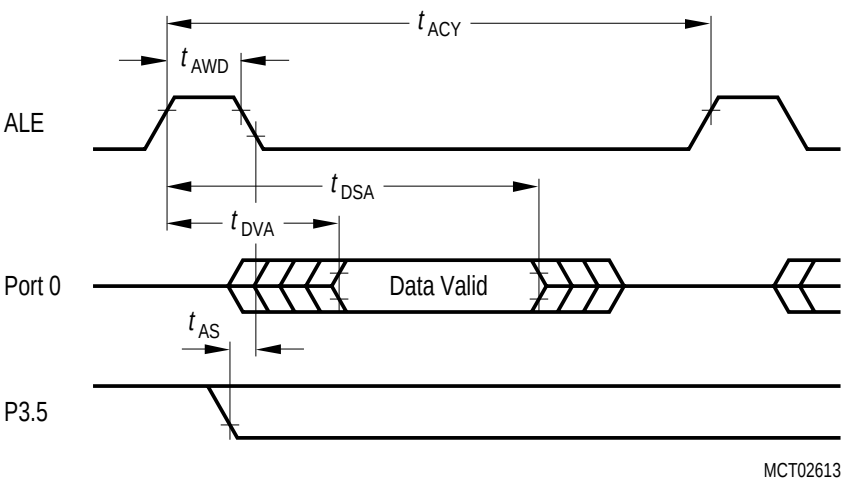
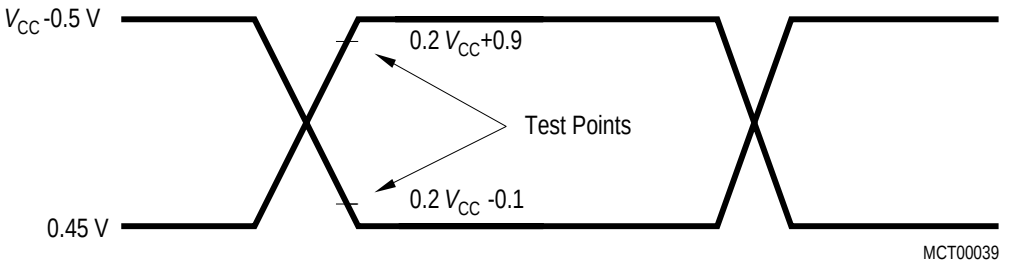
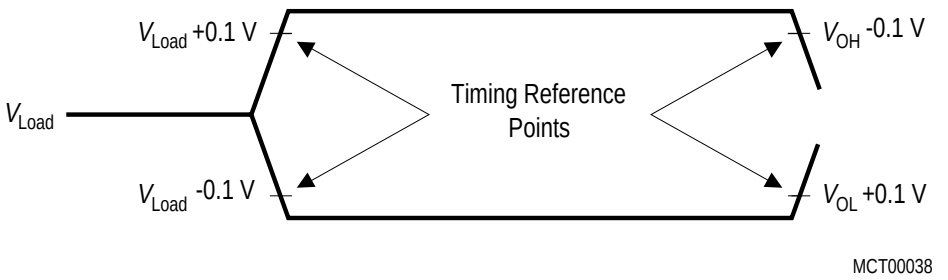


Figure 11-11
ROM Verification Mode 2



AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 11-12
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 11-13
AC Testing : Float Waveforms

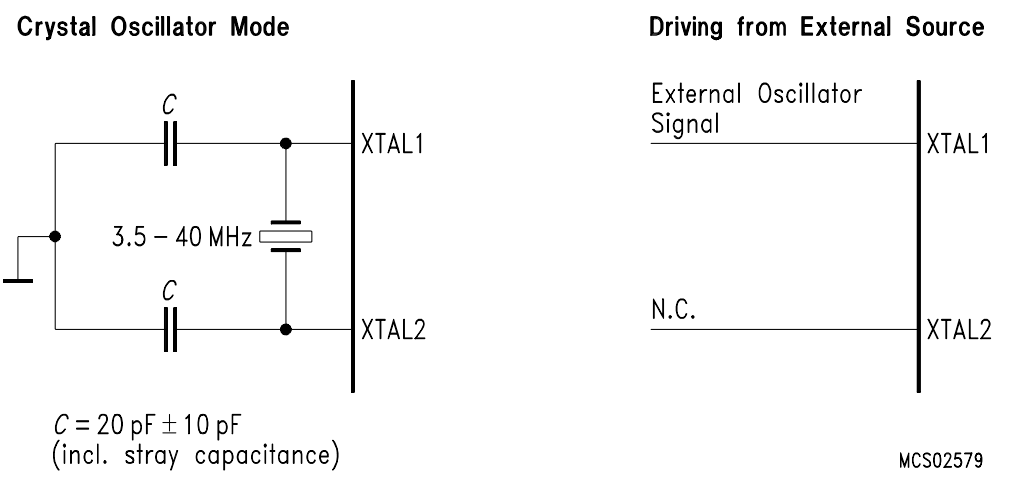


Figure 11-14
Recommended Oscillator Circuits for Crystal Oscillator

11.9 Package Information

P-MQFP-44 (SMD)
(Plastic Metric Quad Flat Package)

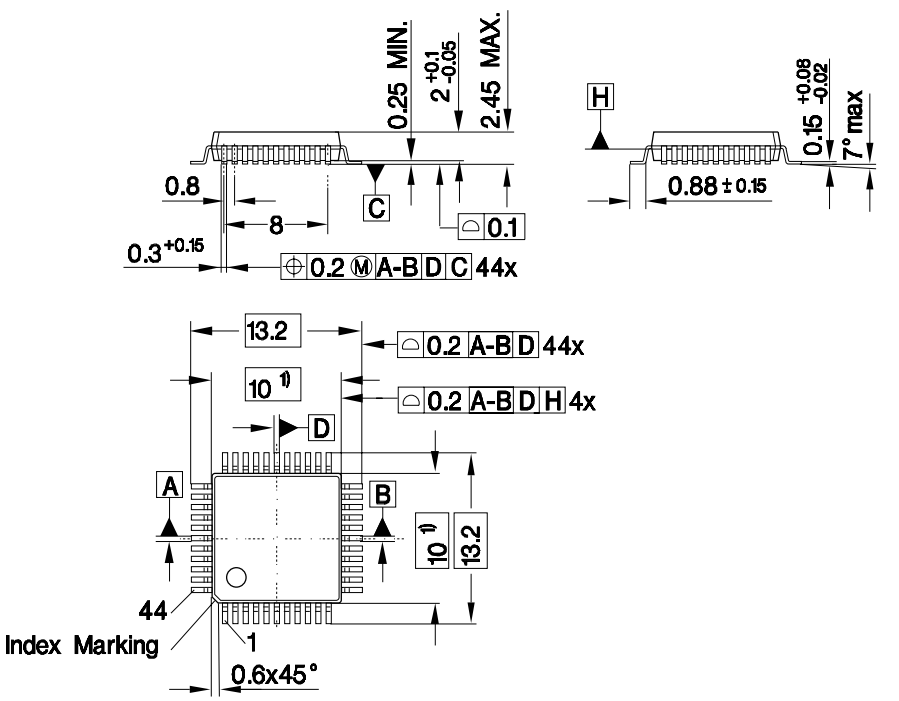


Figure 11-15
P-MQFP-44 Package Outline

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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Note : Bold page numbers refer to the main definition part of SFRs or SFR bits.

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