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April 1st, 2010
Renesas Electronics Corporation

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R2J20651ANP

Integrated Driver – MOS FET (DrMOS)

REJ03G1792-0200
Rev.2.00
Mar 12, 2010

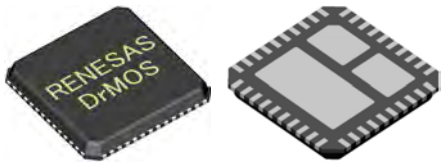
Description

The R2J20651ANP multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver, making this device suitable for large-current buck converters. The chip also incorporates a high-side bootstrap Schottky barrier diode (SBD), eliminating the need for an external SBD for this purpose.

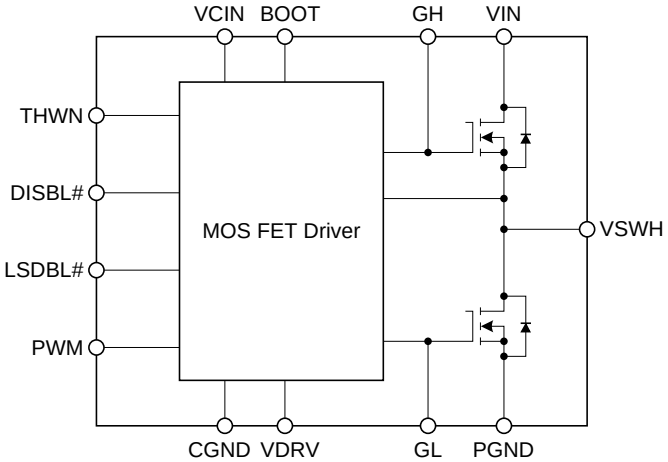
Features

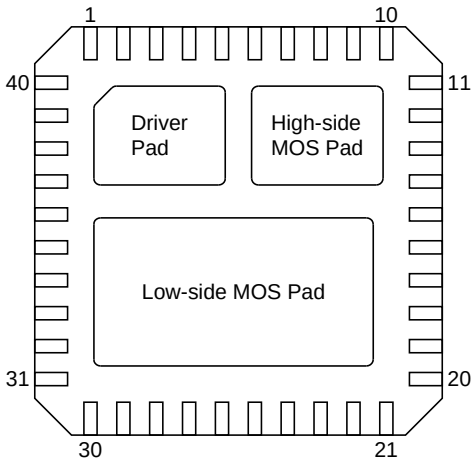
- Compliant with Intel 6 × 6 DrMOS specification
- Built-in power MOS FET suitable for applications with 5 V/12 V input
- Built-in driver circuit which matches the power MOS FET
- Built-in tri-state input function which can support a number of PWM controllers
- VIN operating-voltage range: 16 V max
- High-frequency operation (above 1 MHz) possible
- Large average output current (Max. 35 A)
- Achieve low power dissipation
- Controllable driver: Remote on/off
- Low-side MOS FET disabled function for DCM operation
- Built-in thermal warning
- Built-in Schottky diode for bootstrapping
- Small package: QFN40 (6 mm × 6 mm × 0.95 mm)
- Terminal Pb-free/Halogen-free

Outline



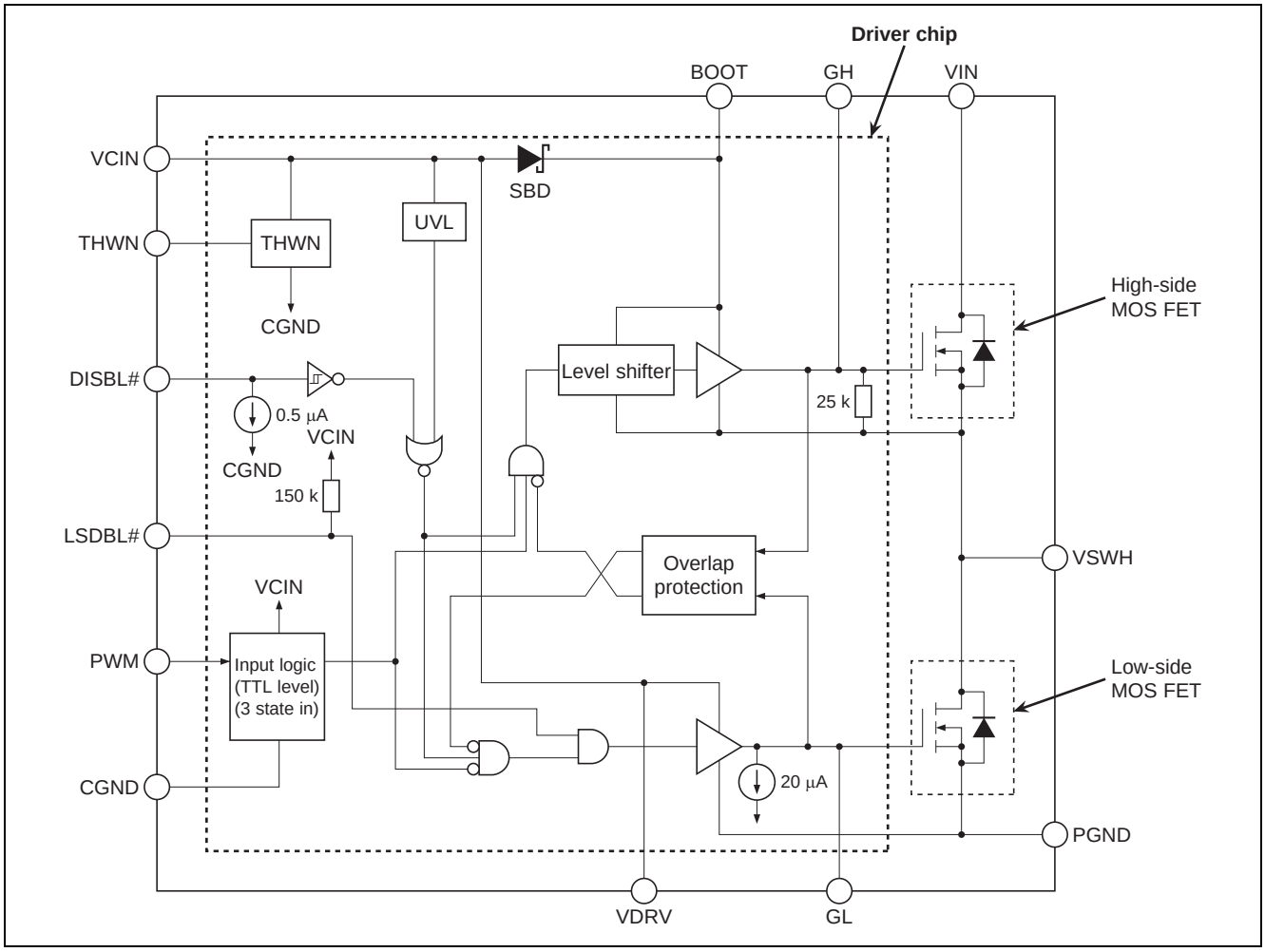
Integrated Driver-MOS FET (DrMOS)
QFN40 package 6 mm × 6 mm





(Bottom view)

Block Diagram



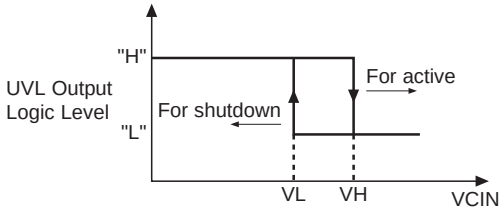
Notes: 1. Truth table for the DISBL# pin.

DISBL# Input	Driver Chip Status
"L"	Shutdown (GL, GH = "L")
"Open"	Shutdown (GL, GH = "L")
"H"	Enable (GL, GH = "Active")

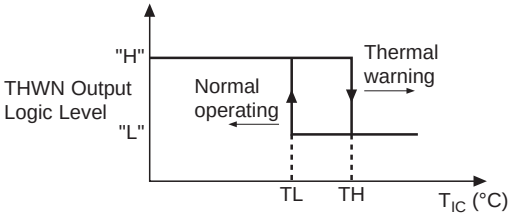
2. Truth table for the LSDBL# pin.

LSDBL# Input	GL Status
"L"	"L"
"Open"	"Active"
"H"	"Active"

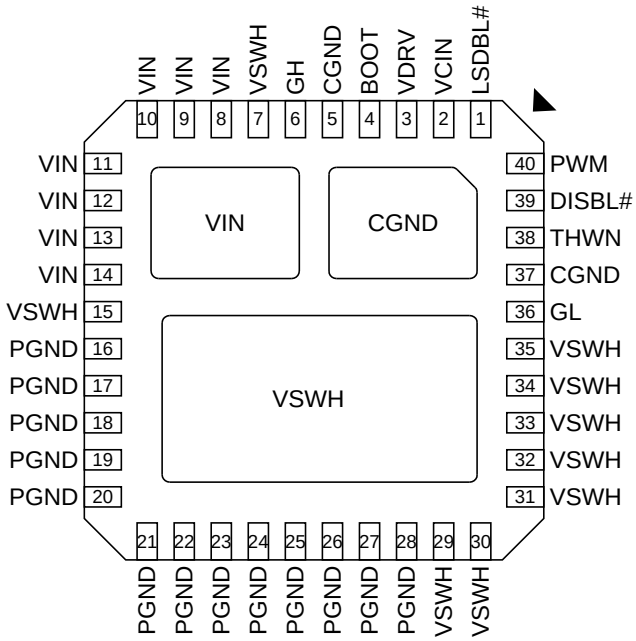
3. Output signal from the UVL block



4. Output signal from the THWN block



Pin Arrangement



(Top view)

Note: All die-pads (three pads in total) should be soldered to PCB.

Pin Description

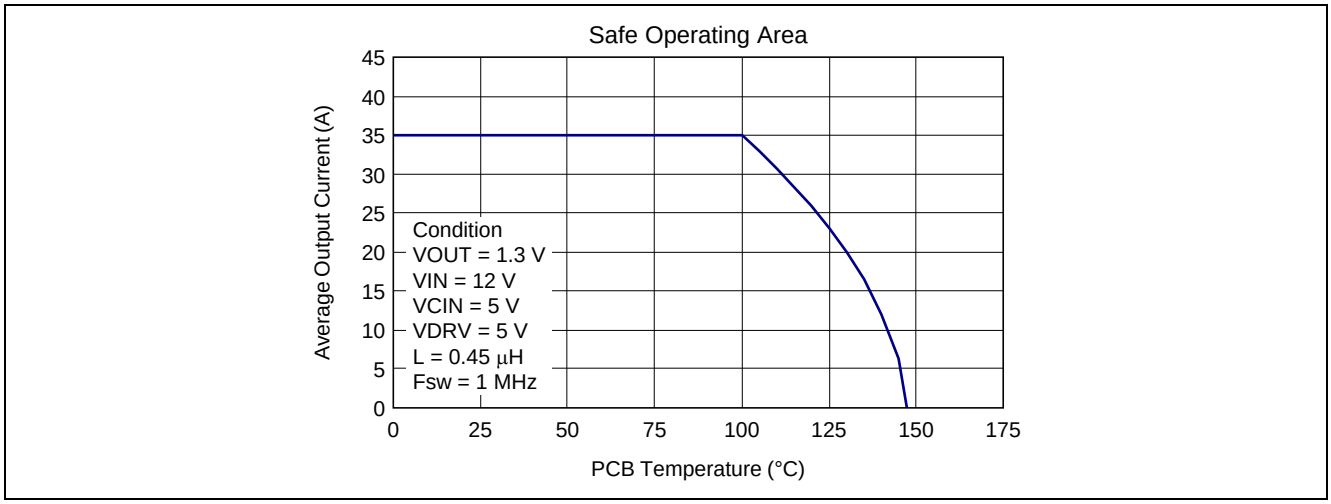
Pin Name	Pin No.	Description	Remarks
LSDBL#	1	Low-side gate disable	When asserted "L" signal, Low-side gate disable
VCIN	2	Control input voltage (+5 V input)	Driver Vcc input
VDRV	3	Gate supply voltage (+5 V input)	5 V gate drive
BOOT	4	Bootstrap voltage pin	To be supplied +5 V through internal SBD
CGND	5, 37, Pad	Control signal ground	Should be connected to PGND externally
GH	6	High-side gate signal	Pin for Monitor
VIN	8 to 14, Pad	Input voltage	
VSWH	7, 15, 29 to 35, Pad	Phase output/Switch output	
PGND	16 to 28	Power ground	
GL	36	Low-side gate signal	Pin for Monitor
THWN	38	Thermal warning	Thermal warning when over 130°C
DISBL#	39	Signal disable	Disabled when DISBL# is "L"
PWM	40	PWM drive logic input	5 V logic input

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Units	Note
Power dissipation	Pt(25)	25	W	1
	Pt(110)	8		
Average output current	Iout	35	A	
Input voltage	VIN (DC)	–0.3 to +16	V	2
	VIN (AC)	20		2, 3
Supply voltage & Drive voltage	VCIN & VDRV	–0.3 to +6	V	2
Switch node voltage	VSWH (DC)	16	V	2
	VSWH (AC)	25		2, 3
BOOT voltage	VBOOT (DC)	22	V	2
	VBOOT (AC)	25		2, 3
I/O voltage	Vpwm, Vdisble, Vlsdbl, Vthwn	–0.3 to VCIN + 0.3	V	2, 4
Operating junction temperature	Tj-opr	–40 to +150	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(110) represents 110°C.
2. Rated voltages are relative to voltages on the CGND and PGND pins.
3. The specification values indicated "AC" are limited within 100 ns.
4. VCIN + 0.3 V < 6 V



Recommended Operating Condition

Item	Symbol	Rating	Units	Note
Input voltage	VIN	4.5 to 14	V	
Supply voltage & Drive voltage	VCIN & VDRV	4.5 to 5.5	V	

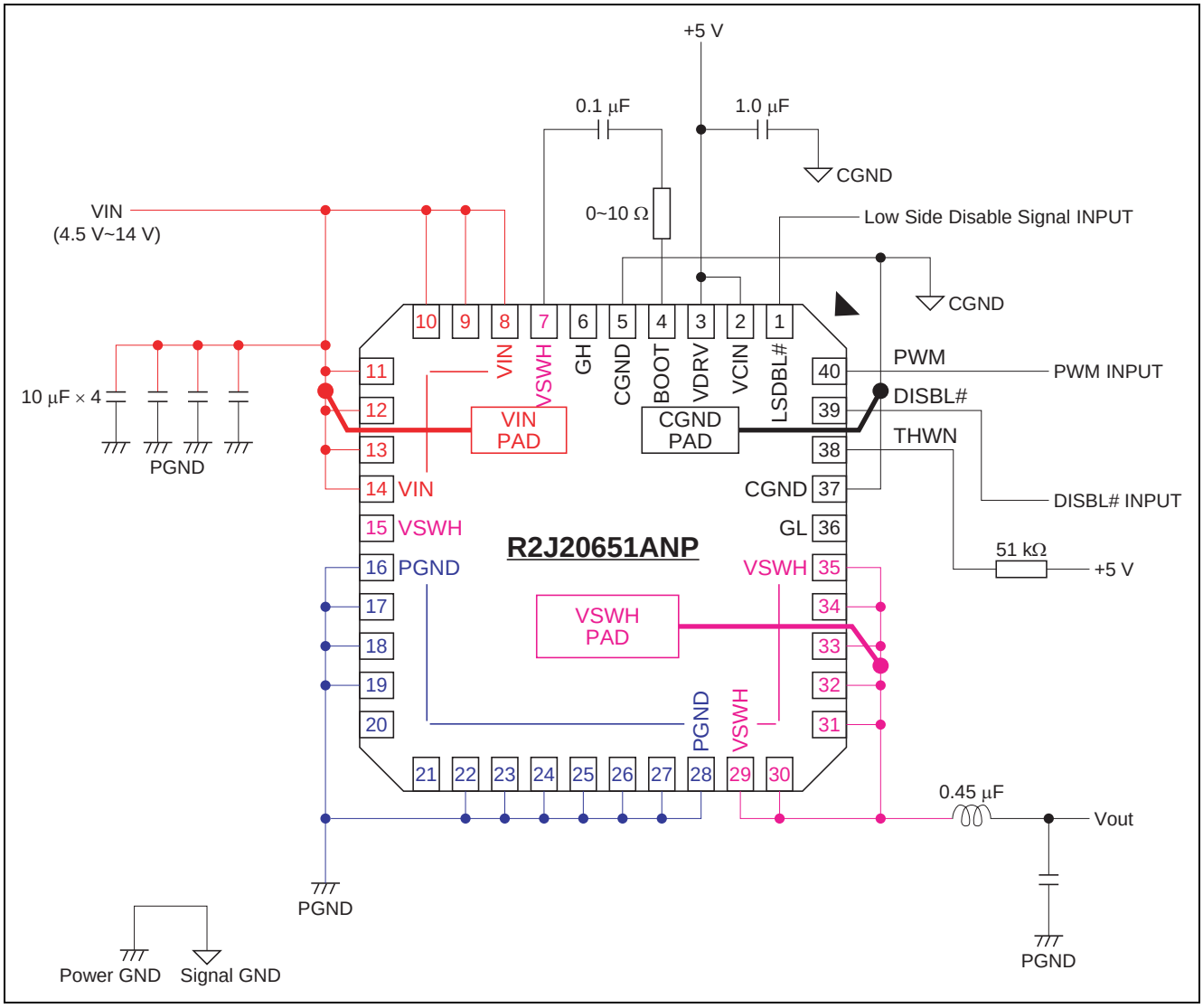
Electrical Characteristics

(Ta = 25°C, VCIN = 5 V, VDRV = 5 V, VSWH = 0 V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Units	Test Conditions
Supply	VCIN start threshold	V_H	3.1	3.5	3.9	V	
	VCIN shutdown threshold	V_L	2.7	3.0	3.3	V	
	UVLO hysteresis	dUVL	—	0.5	—	V	$V_H - V_L$
	VCIN operating current	I_{CIN}	—	29	—	mA	f_{PWM} = 1 MHz, Ton_pwm = 120 ns
	VCIN disable current	$I_{CIN-DISBL}$	—	—	50	μA	DISBL# = 0 V, PWM = 0 V, LSDBL# = Open
PWM input	PWM rising threshold	V_{H-PWM}	3.3	3.7	4.1	V	
	PWM falling threshold	V_{L-PWM}	0.9	1.2	1.5	V	
	PWM input resistance	R_{IN-PWM}	10	20	40	kΩ	PWM = 1 V
	Tri-state shutdown window	V_{IN-SD}	V_{L-PWM}	—	V_{H-PWM}	V	
	Shutdown hold-off time	$t_{HOLD-OFF}$ *1	—	100	—	ns	
DISBL# input	Disable threshold	V_{DISBL}	0.9	1.2	1.5	V	
	Enable threshold	V_{ENBL}	1.9	2.4	2.9	V	
	Input current	I_{DISBL}	—	0.5	2.0	μA	DISBL# = 1 V
LSDBL# input	Low-side activation threshold	V_{LSDBLH}	1.9	2.4	2.9	V	
	Low-side disable threshold	V_{LSDBLL}	0.9	1.2	1.5	V	
	Input current	I_{LSDBL}	–54	–27	–13.5	μA	LSDBL# = 1 V
Thermal warning	Warning temperature	T_{THWN} *1	110	130	—	°C	Driver IC temperature
	Temperature hysteresis	T_{HYS} *1	—	15	—	°C	
	THWN on resistance	R_{THWN} *1	1.0	2.5	4.0	kΩ	THWN = 1 V
	THWN leakage current	I_{LEAK}	—	0.001	1.0	μA	THWN = 5 V

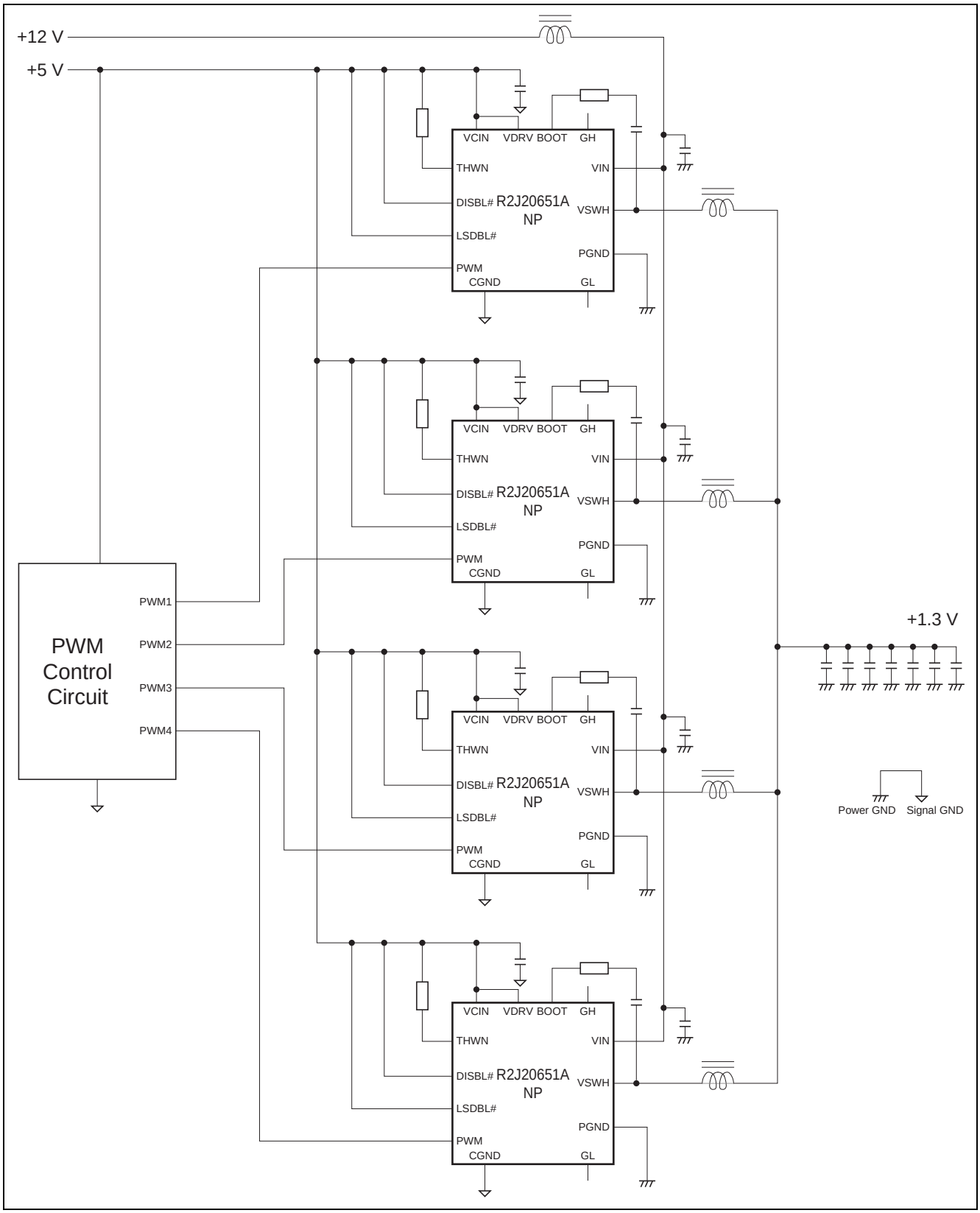
Note: 1. Reference values for design. Not 100% tested in production.

Pin Connection

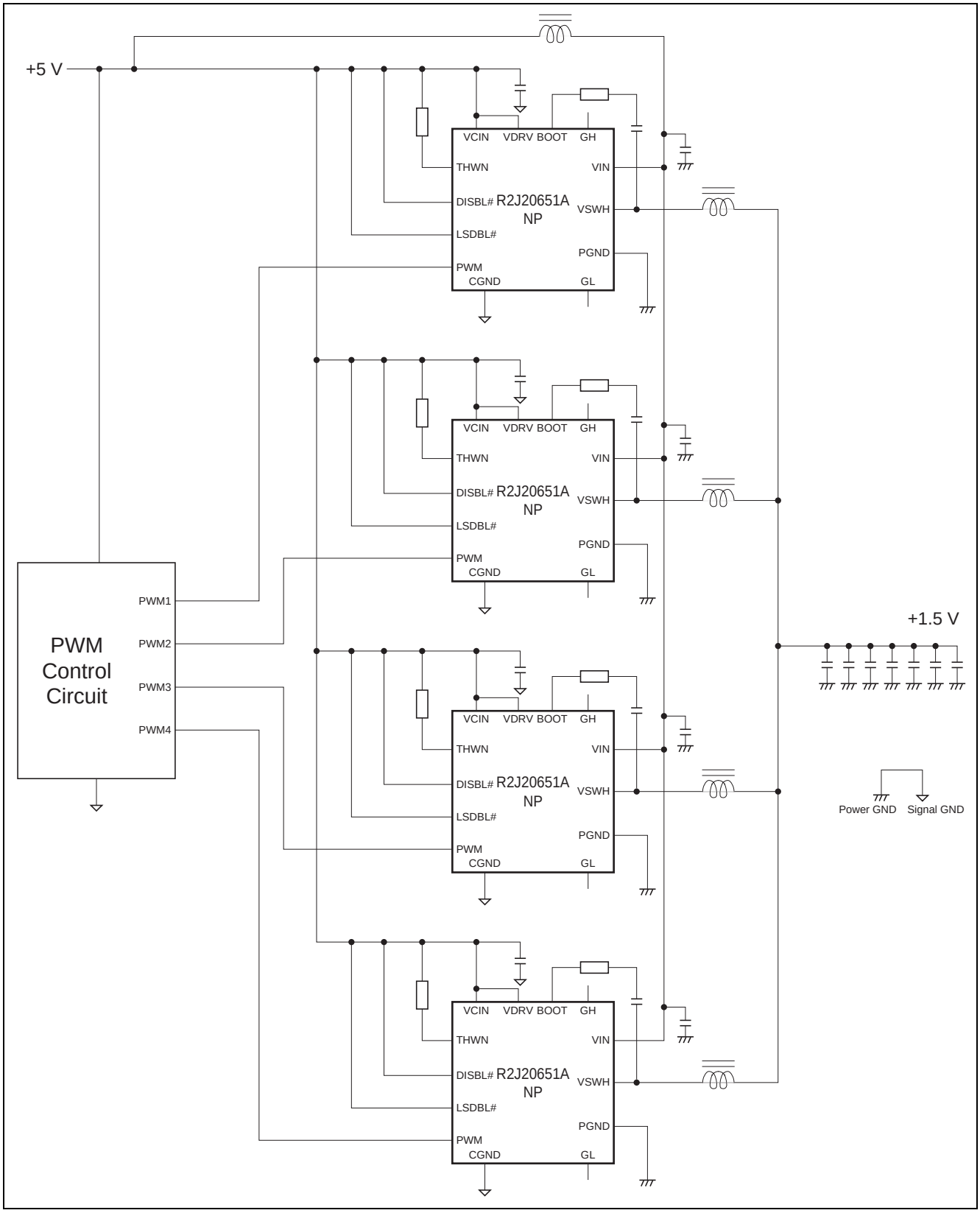


Typical Application

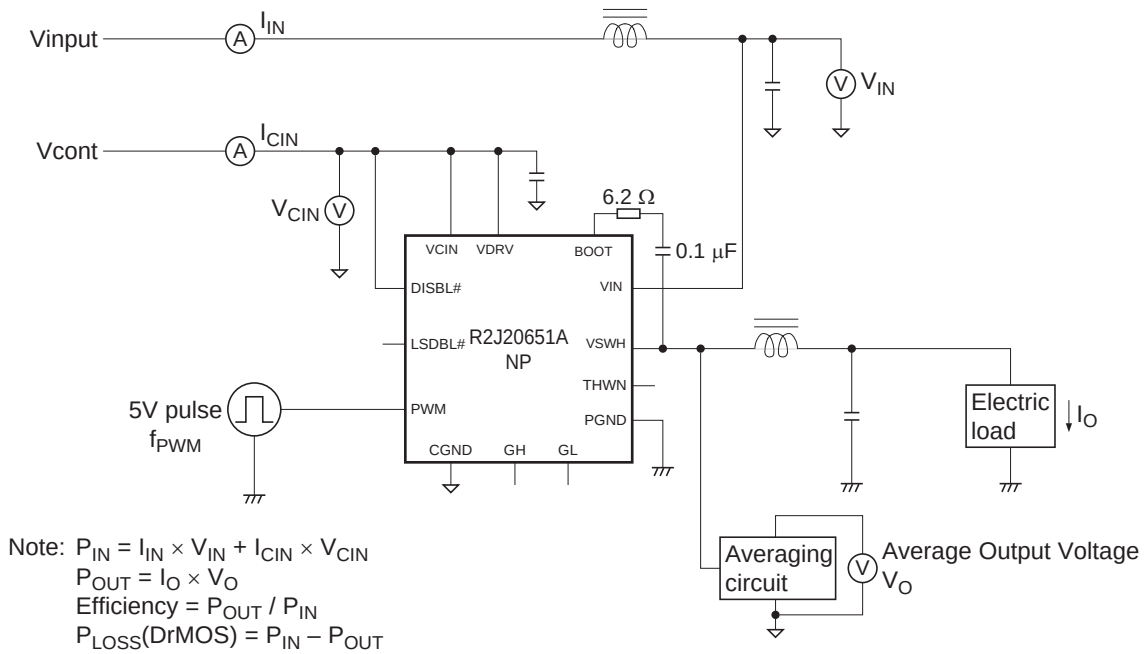
(1) 12 V Input Power



(2) 5 V Input Power

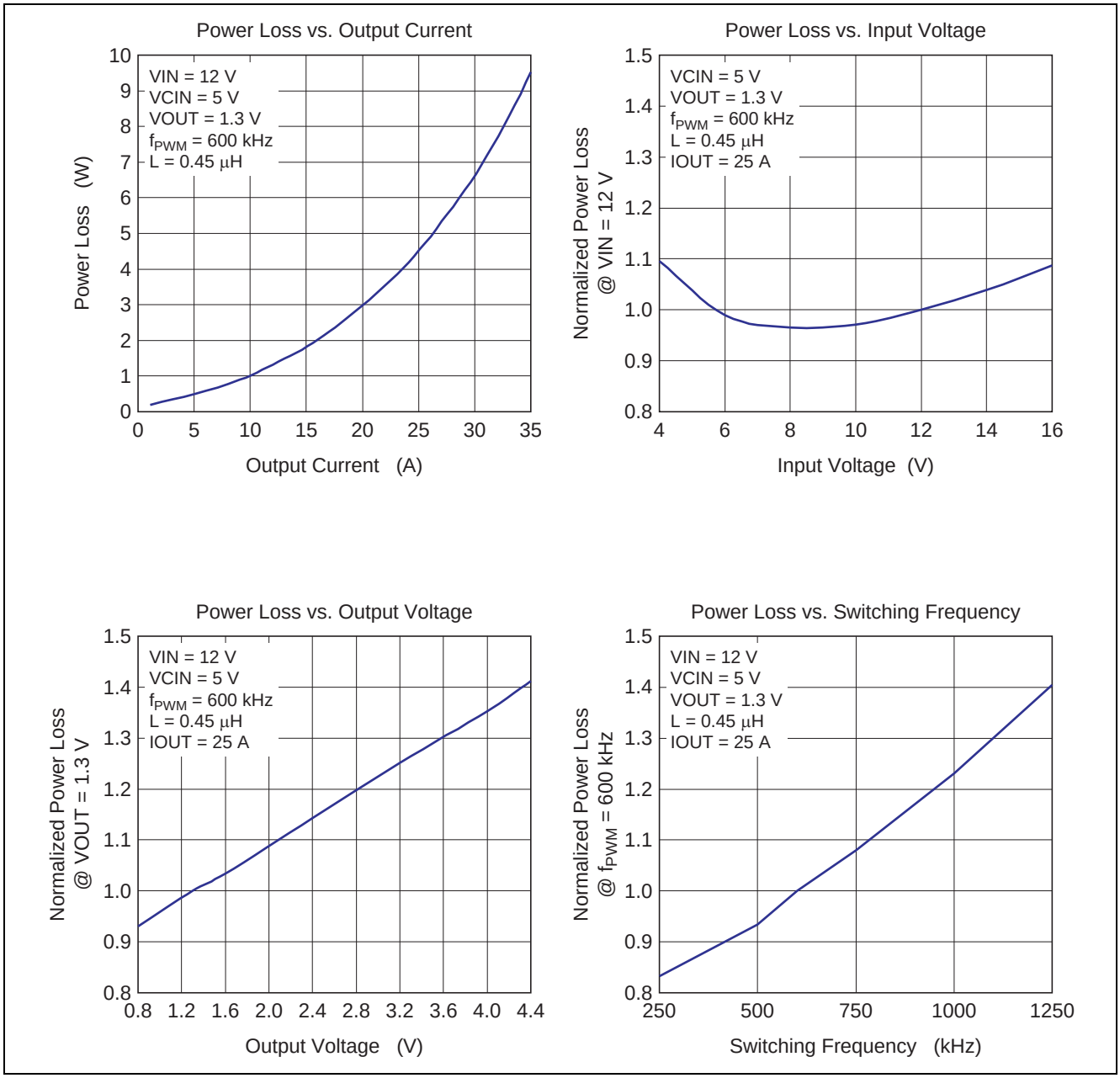


Test Circuit



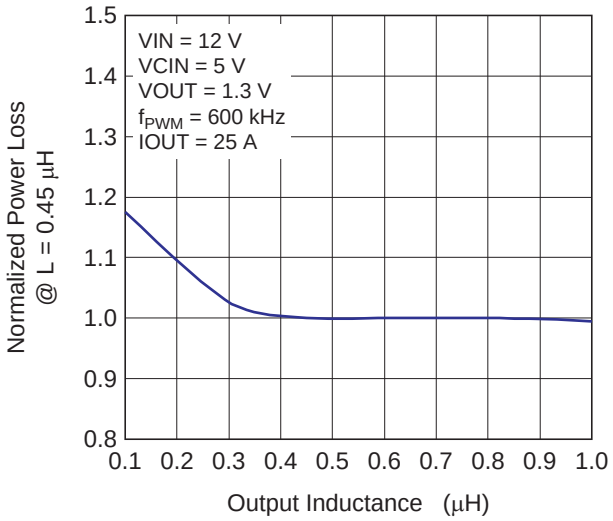
Note: $P_{IN} = I_{IN} \times V_{IN} + I_{CIN} \times V_{CIN}$
$P_{OUT} = I_O \times V_O$
Efficiency = P_{OUT} / P_{IN}
P_{LOSS}(DrMOS) = $P_{IN} - P_{OUT}$
Ta = 27°C

Typical Data

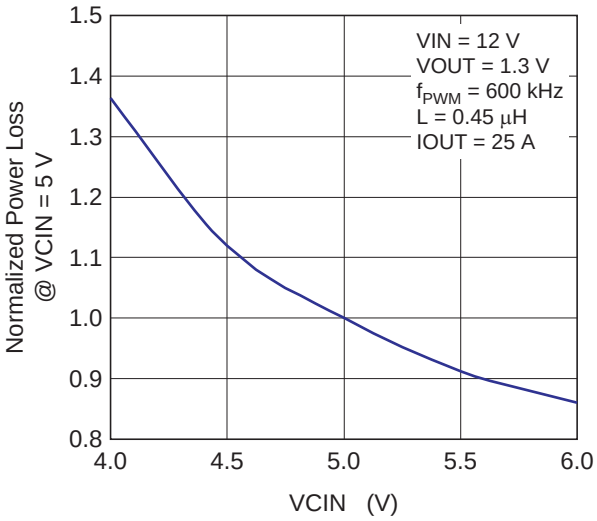


Typical Data (cont.)

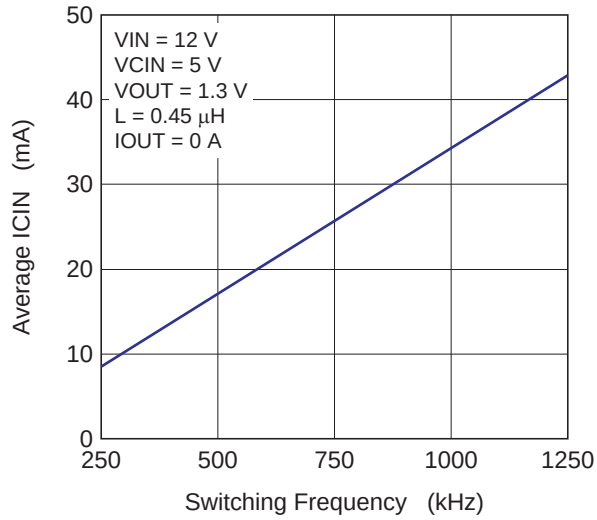
Power Loss vs. Output Inductance



Power Loss vs. VCIN



Average ICIN vs. Switching Frequency



Description of Operation

The DrMOS multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. Since the parasitic inductance between each chip is extremely small, the module is highly suitable for use in buck converters to be operated at high frequencies. The control timing between the high-side MOS FET, low-side MOS FET, and driver is optimized so that high efficiency can be obtained at low output-voltage.

VCIN & DISBL#

The VCIN pin is connected to the UVL (under-voltage lockout) module, so that the driver is disabled as long as VCIN is 3.5 V or less. On cancellation of UVL, the driver remains enabled until the UVL input is driven to 3.0 V or less. The signal on pin DISBL# also enables or disables the circuit.

Voltages from –0.3 V to VCIN can be applied to the DISBL# pin, so on/off control by a logic IC or the use of a resistor, etc., to pull the DISBL# line up to VCIN are both possible.

VCIN	DISBL#	Driver State
L	*	Disable (GL, GH = L)
H	L	Disable (GL, GH = L)
H	H	Active
H	Open	Disable (GL, GH = L)

PWM & LSDBL#

The PWM pin is the signal input pin for the driver chip. The input-voltage range is –0.3 V to (VCIN + 0.3 V). When the PWM input is high, the gate of the high-side MOS FET (GH) is high and the gate of the low-side MOS FET (GL) is low.

PWM	GH	GL
L	L	H
H	H	L

The LSDBL# pin is the low-side gate disable pin for "Discontinuous Conduction Mode (DCM)" when LSDBL# is low.

Figure 1 shows the typical high-side and low-side gate switching and inductor current (IL) during Continuous Conduction Mode (CCM) and low-side gate disabled when asserting low-side disable signal.

This pin is internally pulled up to VCIN with 150 kΩ resistor.

When low-side disable function is not used, keep this pin open or pulled up to VCIN.

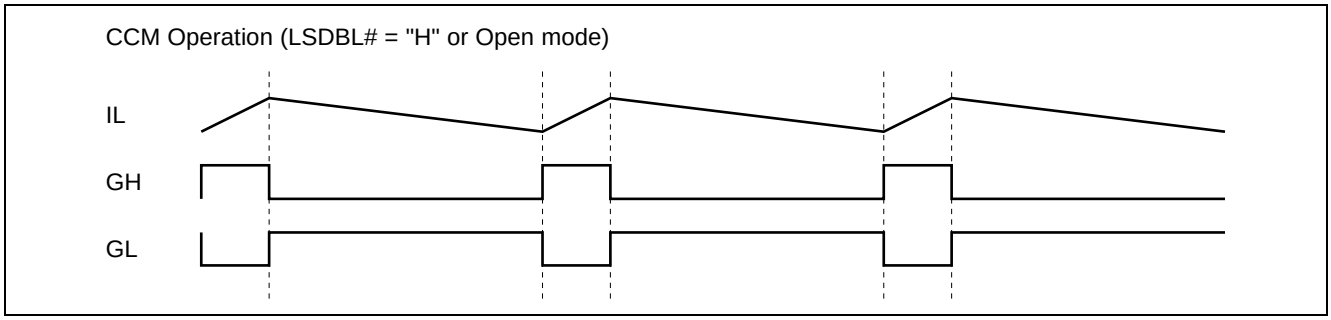


Figure 1.1 Typical Signals During CCM

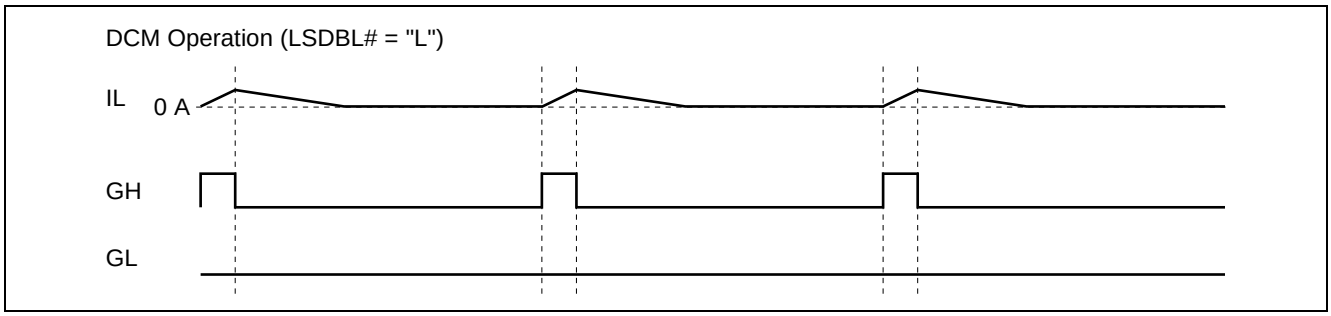


Figure 1.2 Typical Signals during Low-Side Disable Operation

The PWM input is TTL level and has hysteresis. When the signal route from the control IC is high impedance, the tri-state function turns off the high- and low-side MOS FETs. This function operates when the PWM input signal stays in the input hysteresis window for 100 ns (typ.). After the tri-state mode has been entered and GH and GL have become low, a PWM input voltage of 3.7 V or more is required to make the circuit return to normal operation.

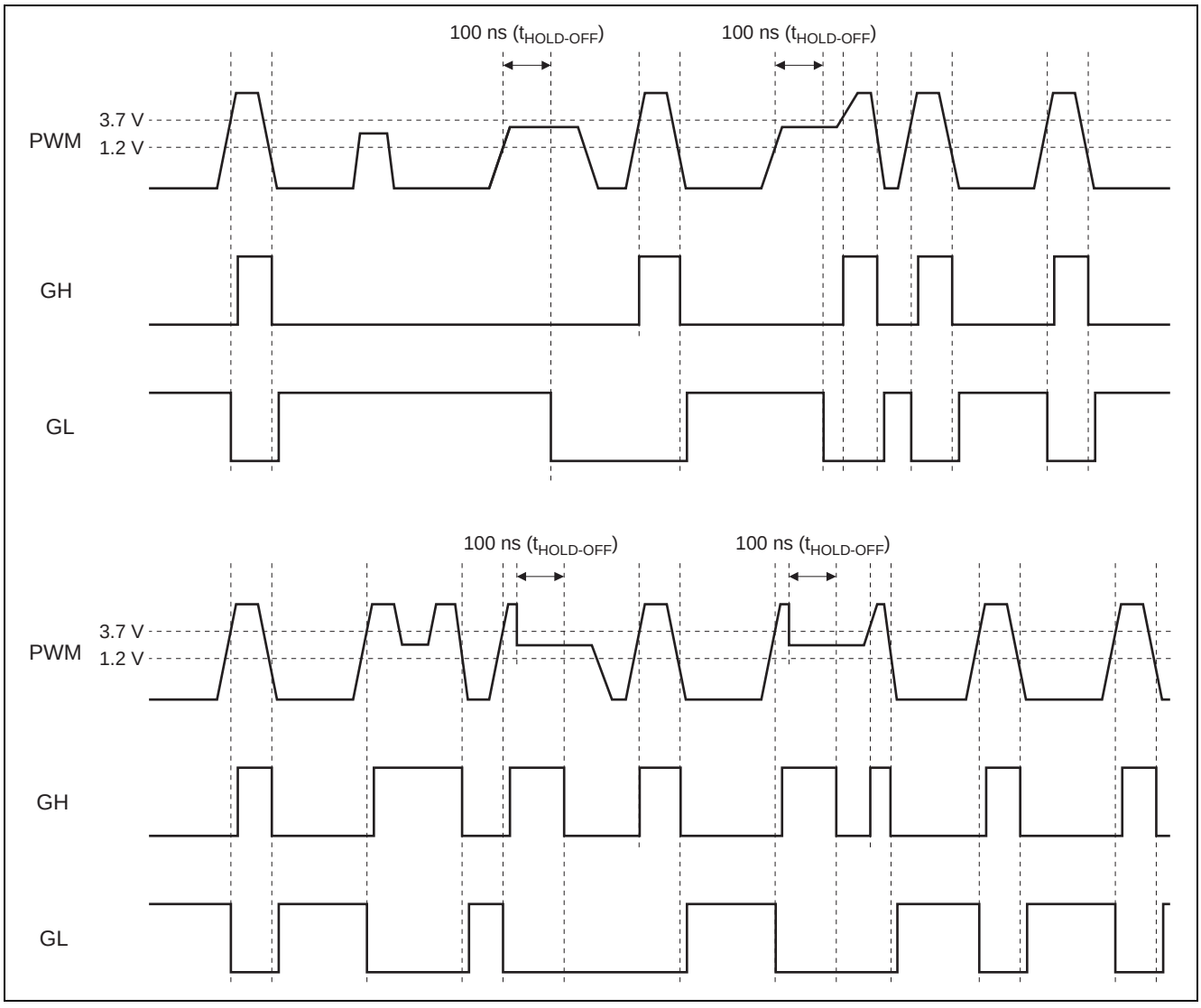


Figure 2

The equivalent circuit for the PWM-pin input is shown in the next figure. M1 is in the ON state during normal operation; after the PWM input signal has stayed in the hysteresis window for 100 ns (typ.) and the tri-state detection signal has been driven high, the transistor M1 is turned off.

When VCIN is powered up, M1 is started in the OFF state regardless of PWM Low or Open state. After PWM is asserted high signal, M1 becomes ON and shifts to normal operation.

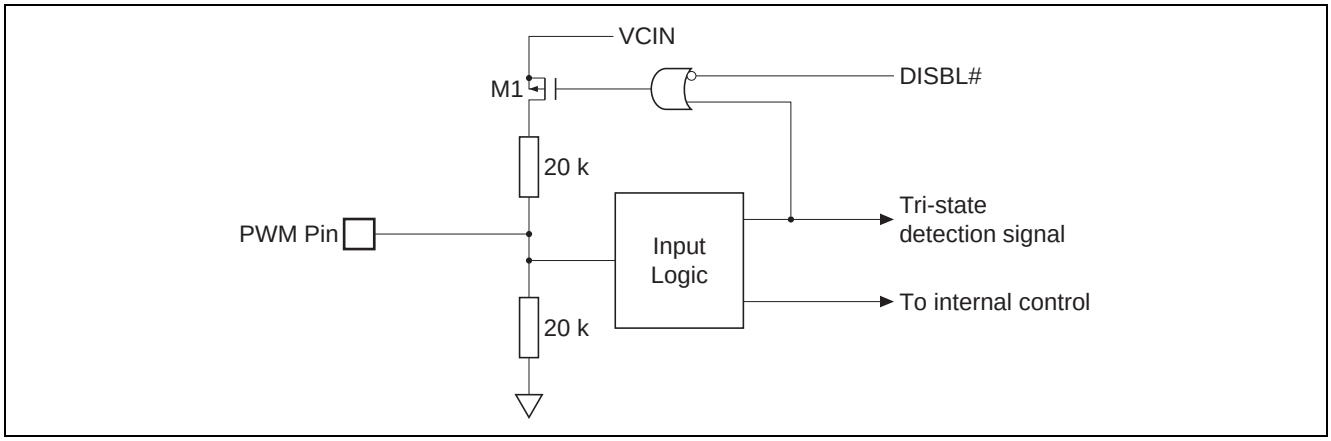


Figure 3 Equivalent Circuit for the PWM-pin Input

THWN

This thermal warning feature is the indication of the high temperature status.

THWN is an open drain logic output signal and need to connect a pull-up resistor (ex. 51 kΩ) to THWN for systems with the thermal warning implementation.

When the chip temperature of the internal driver IC becomes over 130°C, thermal warning function operates.

This signal is only indication for the system controller and does not disable DrMOS operation.

When thermal warning function is not used, keep this pin open.

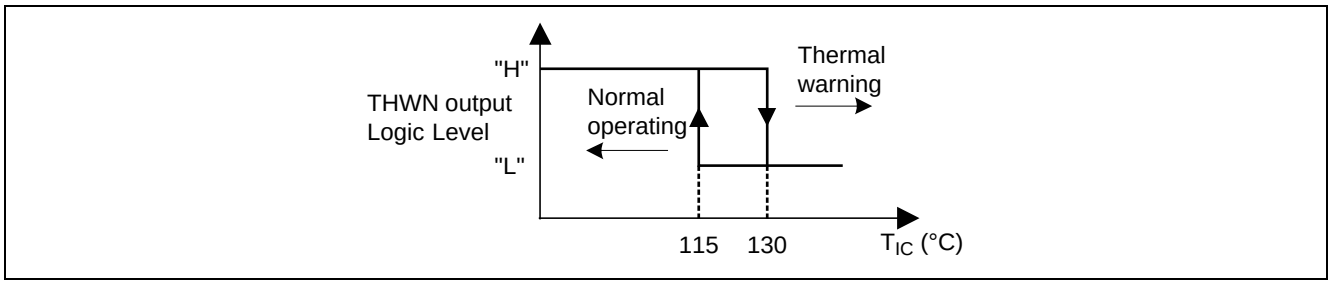


Figure 4

MOS FETs

The MOS FETs incorporated in R2J20651ANP are highly suitable for synchronous-rectification buck conversion. For the high-side MOS FET, the drain is connected to the VIN pin and the source is connected to the VSWH pin. For the low-side MOS FET, the drain is connected to the VSWH pin and the source is connected to the PGND pin.

PCB Layout Example

Figure 5 shows an example of the PCB layout for the R2J20651ANP. Placing several ceramic capacitors (e.g. 10 µF) between VIN and PGND can be expected to the decreasing switching noise and improvement of efficiency.

In that case, it is necessary to connect each GND pattern with low impedance by using other PCB layers.

Moreover, by taking the wide VSWH pattern, the effect of letting the heat from the low side MOS FET can be expected.

When R2J20651ANP is mounted on a small substrate like POL module, the temperature rising of the device could be eased if the thermal via-hole is added under the pad of VIN and VSWH.

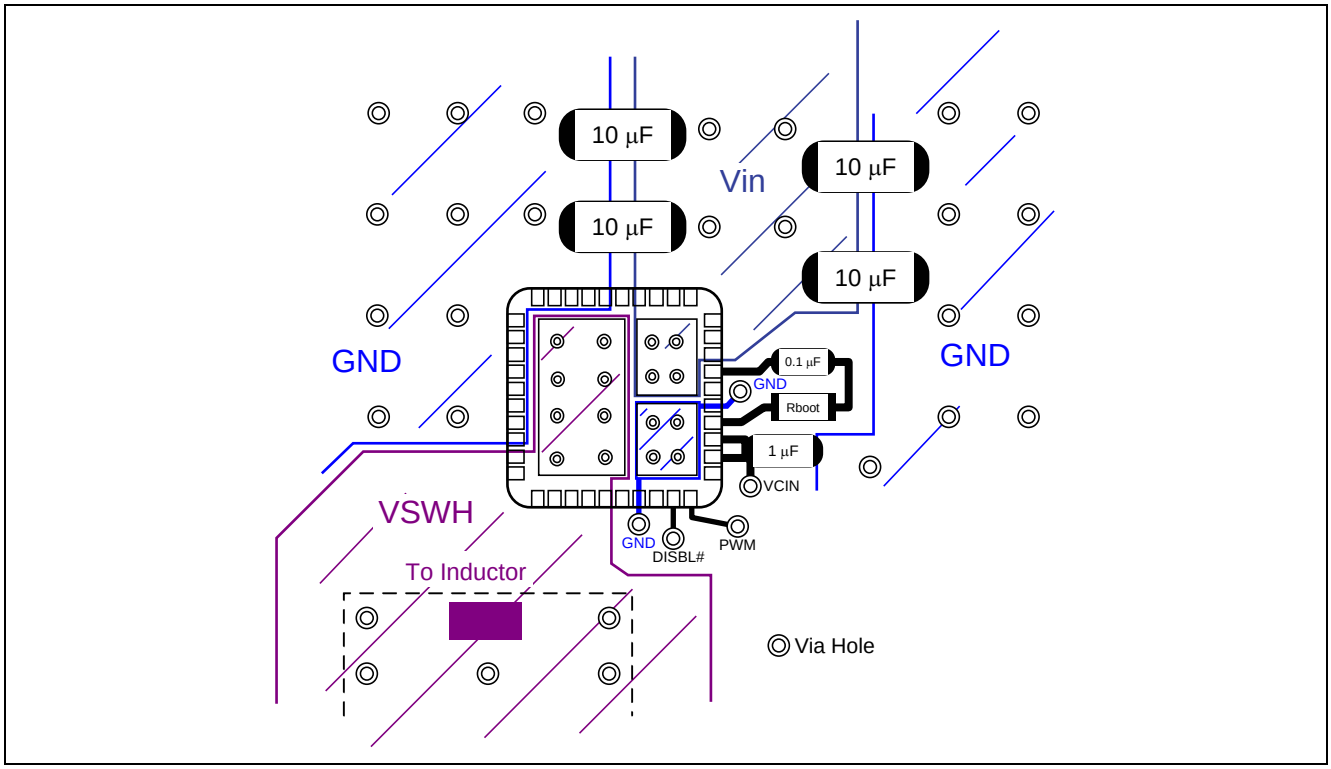


Figure 5 R2J20651ANP PCB Layout Example (Top View)

Footprint Example

(Unit: mm)

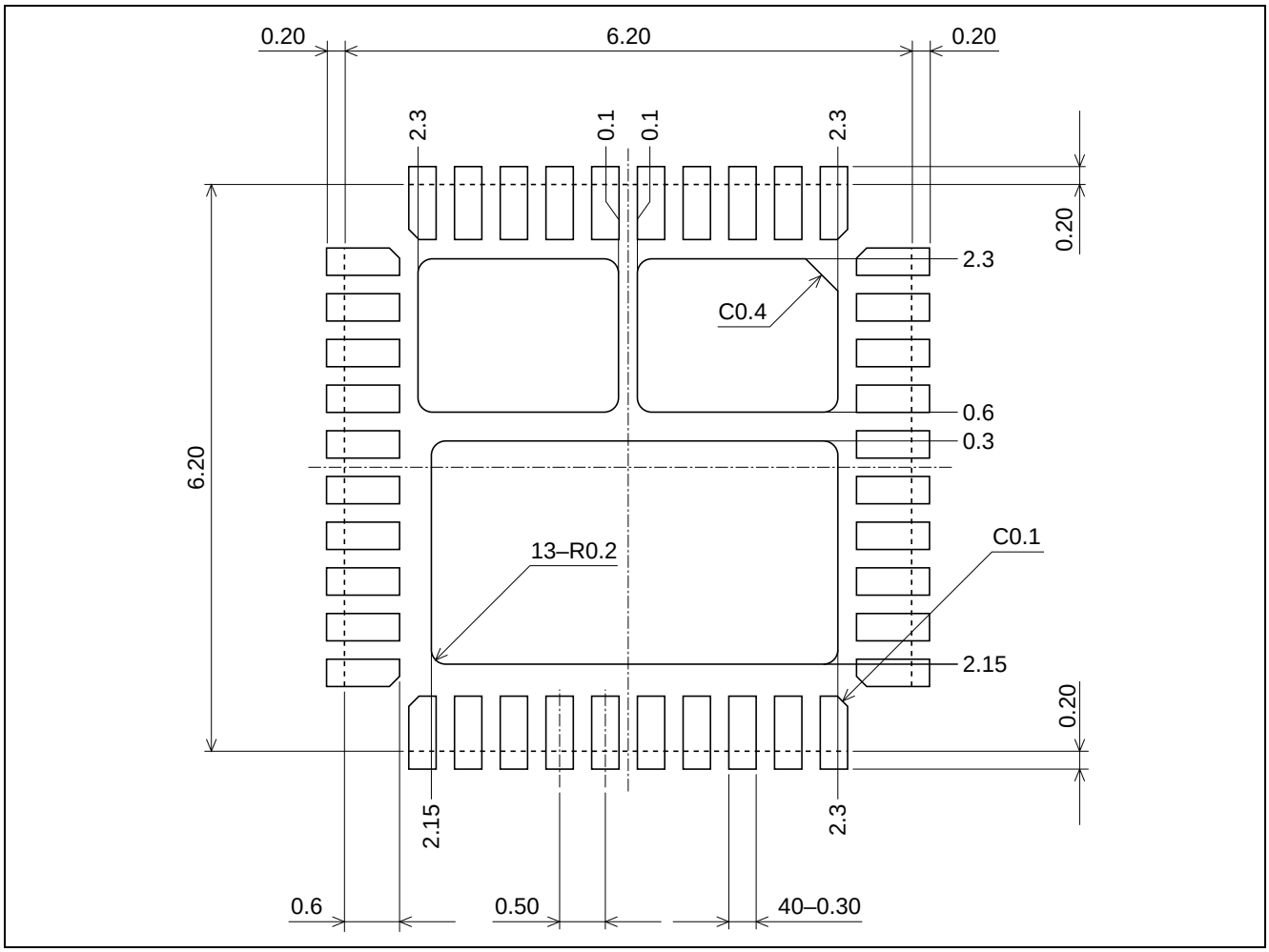
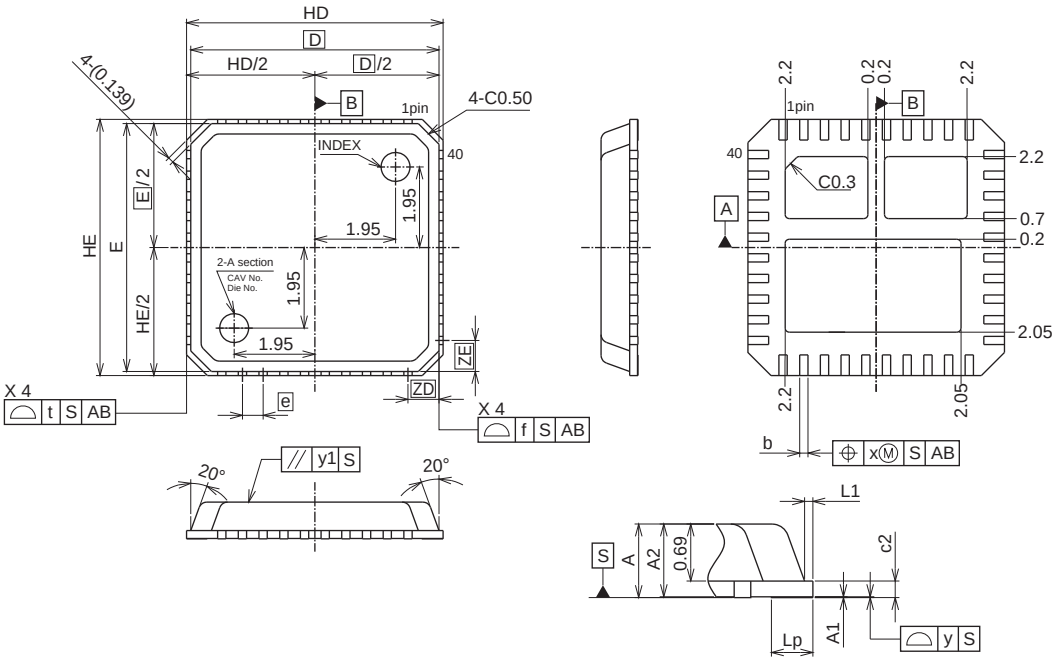


Figure 6 Footprint Example

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HVQFN40-p-0606-0.50	PVQN0040KC-A	—	—



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A2	0.87	0.89	0.91
f	—	—	0.20
A	0.865	0.91	0.95
A1	0.005	0.02	0.04
b	0.17	0.22	0.27
b1	0.16	0.20	0.24
e	—	0.50	—
Lp	0.40	0.50	0.60
x	—	—	0.05
y	—	—	0.05
y1	—	—	0.20
t	—	—	0.20
HD	6.15	6.20	6.25
HE	6.15	6.20	6.25
ZD	—	0.75	—
ZE	—	0.75	—
L1	0.06	0.10	0.14
c1	0.17	0.20	0.23
c2	0.17	0.22	0.27

Ordering Information

Part Name	Quantity	Shipping Container
R2J20651ANP#G3	2500 pcs	Taping Reel

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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