SN74LVC1T45-Q1 1.65-V to 5.5-V Single-Bit Dual-Supply Level Shifter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  – Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  – Device HBM ESD Classification Level H2
  – Device CDM ESD Classification Level C3B
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Maximum Data Rates
  – 420 Mbps (3.3-V to 5-V Translation)
  – 210 Mbps (Translate to 3.3 V)
  – 140 Mbps (Translate to 2.5 V)
  – 75 Mbps (Translate to 1.8 V)

2 Applications

- Head Units
- ADAS – Cameras
- Telematics

3 Description

The SN74LVC1T45-Q1 device is a single-bit, noninverting bus transceiver that uses two separate configurable power supply rails. The A-port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B-port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC1T45-Q1 device is a single-bit, non-inverting level translator. The fully configurable dual-rail design allows each port to overate over the full 1.65-V to 5.5-V power supply range. It is ideal for applications that need a wide bidirectional translation range.

The SN74LVC1T45-Q1 is designed so that the DIR input is powered by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

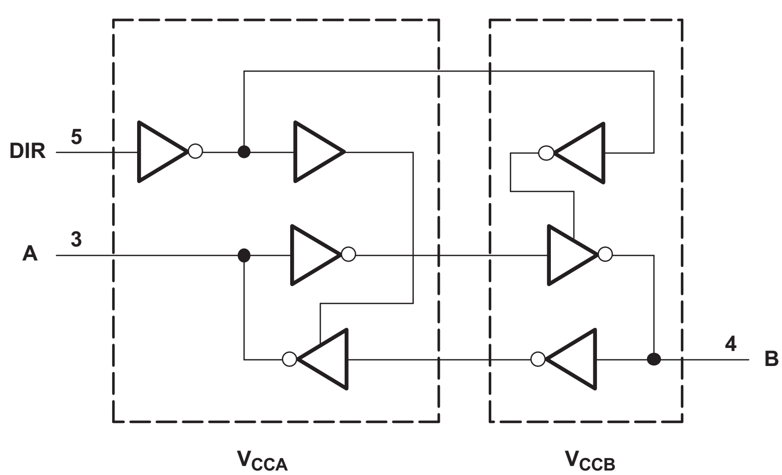
The V_{CC} isolation feature assures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1T45-Q1	SC70 (6)	1.25 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2016) to Revision D — **Page**

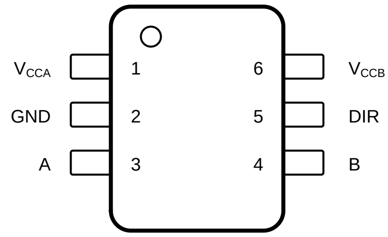
- Added Junction temperature, T_J in *Absolute Maximum Ratings* 4
- Added revised steps for power-up sequence in *Power Supply Recommendations* 20

Changes from Revision B (September 2012) to Revision C — **Page**

- Changed data sheet title From: SN74LVC1T45-Q1 Single-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs To: SN74LVC1T45-Q1 1.65-V to 5.5-V Single-Bit Dual-Supply Level Shifter 1
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section........ 1
- Deleted Ordering Information table; see POA the end of the data sheet........ 1

5 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



Not to scale

See mechanical drawings for dimensions.

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A	3	I/O	Output level depends on V_{CC1} voltage
B	4	I/O	Input threshold value depends on V_{CC2} voltage
DIR	5	I	GND (low level) determines B-port to A-port direction
GND	2	G	Device GND
V_{CCA}	1	P	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
V_{CCB}	6	P	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CCA}, V_{CCB}		–0.5	6.5	V
Input voltage, V_I[2]		–0.5	6.5	V
Voltage applied to any output in the high-impedance or power-off state, V_O[2]		–0.5	6.5	V
Voltage applied to any output in the high or low state, V_O[2][3]	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK} (V_I < 0)			–50	mA
Output clamp current, I_{OK} (V_O < 0)			–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See[1][2][3]

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		1.65	5.5	V
V_{CCB}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage, data inputs[4]	V_{CCI} = 1.65 V to 1.95 V	V_{CCI} × 0.65		V
		V_{CCI} = 2.3 V to 2.7 V	1.7		
		V_{CCI} = 3 V to 3.6 V	2		
		V_{CCI} = 4.5 V to 5.5 V	V_{CCI} × 0.7		
V_{IL}	Low-level input voltage, data inputs[4]	V_{CCI} = 1.65 V to 1.95 V		V_{CCI} × 0.35	V
		V_{CCI} = 2.3 V to 2.7 V		0.7	
		V_{CCI} = 3 V to 3.6 V		0.8	
		V_{CCI} = 4.5 V to 5.5 V		V_{CCI} × 0.3	
V_{IH}	High-level input voltage, DIR (referenced to V_{CCA})[5]	V_{CCI} = 1.65 V to 1.95 V	V_{CCA} × 0.65		V
		V_{CCI} = 2.3 V to 2.7 V	1.7		
		V_{CCI} = 3 V to 3.6 V	2		
		V_{CCI} = 4.5 V to 5.5 V	V_{CCA} × 0.7		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to assure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Recommended Operating Conditions (continued)

See[1][2][3]

				MIN	MAX	UNIT
V_{IL}	Low-level input voltage, DIR (referenced to V_{CCA})[5]		V_{CCI} = 1.65 V to 1.95 V		V_{CCA} × 0.35	V
			V_{CCI} = 2.3 V to 2.7 V		0.7	
			V_{CCI} = 3 V to 3.6 V		0.8	
			V_{CCI} = 4.5 V to 5.5 V		V_{CCA} × 0.3	
V_I	Input voltage			0	5.5	V
V_O	Output voltage			0	V_{CCO}	V
I_{OH}	High-level output current		V_{CCO} = 1.65 V to 1.95 V		–4	mA
			V_{CCO} = 2.3 V to 2.7 V		–8	
			V_{CCO} = 3 V to 3.6 V		–24	
			V_{CCO} = 4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current		V_{CCO} = 1.65 V to 1.95 V		4	mA
			V_{CCO} = 2.3 V to 2.7 V		8	
			V_{CCO} = 3 V to 3.6 V		24	
			V_{CCO} = 4.5 V to 5.5 V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	V_{CCI} = 1.65 V to 1.95 V		20	ns/V
			V_{CCI} = 2.3 V to 2.7 V		20	
			V_{CCI} = 3 V to 3.6 V		10	
			V_{CCI} = 4.5 V to 5.5 V		5	
		Control inputs, V_{CCI} = 1.65 V to 5.5 V			5	
T_A	Operating free-air temperature			–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1T45-Q1 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	286.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	94.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range with all limits at T_A = –40°C to 125°C (unless otherwise noted)(1)(2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$	I_{OH} = –100 µA, V_{CCA} = 1.65 V to 4.5 V, V_{CCB} = 1.65 V to 4.5 V		V_{CCO} – 0.1			V
		I_{OH} = –4 mA, V_{CCA} = 1.65 V, V_{CCB} = 1.65 V		1.2			
		I_{OH} = –8 mA, V_{CCA} = 2.3 V, V_{CCB} = 2.3 V		1.9			
		I_{OH} = –24 mA, V_{CCA} = 3 V, V_{CCB} = 3 V		2.3			
		I_{OH} = –32 mA, V_{CCA} = 4.5 V, V_{CCB} = 4.5 V		3.8			
V_{OL}	$V_I = V_{IL}$	I_{OL} = 100 µA, V_{CCA} = 1.65 V to 4.5 V, V_{CCB} = 1.65 V to 4.5 V				0.1	V
		I_{OL} = 4 mA, V_{CCA} = 1.65 V, V_{CCB} = 1.65 V				0.45	
		I_{OL} = 8 mA, V_{CCA} = 2.3 V, V_{CCB} = 2.3 V				0.4	
		I_{OL} = 24 mA, V_{CCA} = 3 V, V_{CCB} = 3 V				0.65	
		I_{OL} = 32 mA, V_{CCA} = 4.5 V, V_{CCB} = 4.5 V				0.65	
I_I	DIR at $V_I = V_{CCA}$ or GND, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V		T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±4	
I_{off}	V_I or V_O = 0 to 5.5 V	A port at V_{CCA} = 0 V, V_{CCB} = 0 to 5.5 V	T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±10	
		B port at V_{CCA} = 0 to 5.5 V, V_{CCB} = 0 V	T_A = 25°C			±1	
			T_A = –40°C to 125°C			±10	
I_{OZ}	A or B port at $V_O = V_{CCO}$ or GND, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V		T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±10	
I_{CCA}	$V_I = V_{CCI}$ or GND, I_O = 0	V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V				10	µA
		V_{CCA} = 5.5 V, V_{CCB} = 0 V				4	
		V_{CCA} = 0 V, V_{CCB} = 5.5 V				–10	
I_{CCB}	$V_I = V_{CCI}$ or GND, I_O = 0	V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V				10	µA
		V_{CCA} = 5.5 V, V_{CCB} = 0 V				–10	
		V_{CCA} = 0 V, V_{CCB} = 5.5 V				4	
$I_{CCA} + I_{CCB}$	$V_I = V_{CCI}$ or GND, I_O = 0, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V					20	µA
ΔI_{CCA}	V_{CCA} = 3 V to 5.5 V, V_{CCB} = 3 V to 5.5 V	A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open				50	µA
		DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND				50	
ΔI_{CCB}	B port at V_{CCB} – 0.6 V, DIR at GND, A port = open, V_{CCA} = 3 V to 5.5 V, V_{CCB} = 3 V to 5.5 V					50	µA
C_i	DIR at $V_I = V_{CCA}$ or GND, T_A = 25°C, V_{CCA} = 3.3 V, V_{CCB} = 3.3 V				2.5		pF
C_{io}	A or B port at $V_O = V_{CCA/B}$ or GND, T_A = 25°C, V_{CCA} = 3.3 V, V_{CCB} = 3.3 V				6		pF
C_{pdA} (3)	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	A-port input, B-port output	$V_{CCA} = V_{CCB}$ = 1.8 V		3		pF
			$V_{CCA} = V_{CCB}$ = 2.5 V		4		
			$V_{CCA} = V_{CCB}$ = 3.3 V		4		
			$V_{CCA} = V_{CCB}$ = 5 V		4		
		B-port input, A-port output	$V_{CCA} = V_{CCB}$ = 1.8 V		18		
			$V_{CCA} = V_{CCB}$ = 2.5 V		19		
			$V_{CCA} = V_{CCB}$ = 3.3 V		20		
			$V_{CCA} = V_{CCB}$ = 5 V		21		

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) Power dissipation capacitance per transceiver

Electrical Characteristics (continued)

over operating free-air temperature range with all limits at T_A = –40°C to 125°C (unless otherwise noted)(1)(2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_{pdB} (3)	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	A-port input, B-port output	V_{CCA} = V_{CCB} = 1.8 V		18		pF
			V_{CCA} = V_{CCB} = 2.5 V		19		
			V_{CCA} = V_{CCB} = 3.3 V		20		
			V_{CCA} = V_{CCB} = 5 V		21		
		B-port input, A-port output	V_{CCA} = V_{CCB} = 1.8 V		3		
			V_{CCA} = V_{CCB} = 2.5 V		4		
			V_{CCA} = V_{CCB} = 3.3 V		4		
			V_{CCA} = V_{CCB} = 5 V		4		

6.6 Switching Characteristics: V_{CCA} = 1.8 V ±0.15 V

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	3		20.7	ns
		V_{CCB} = 2.5 V ±0.2 V	2.2		13.3	
		V_{CCB} = 3.3 V ±0.3 V	1.7		11.3	
		V_{CCB} = 5 V ±0.5 V	1.4		10.2	
t_{PHL}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2.8		17.3	ns
		V_{CCB} = 2.5 V ±0.2 V	2.2		11.5	
		V_{CCB} = 3.3 V ±0.3 V	1.8		10.1	
		V_{CCB} = 5 V ±0.5 V	1.7		10	
t_{PLH}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	3		20.7	ns
		V_{CCB} = 2.5 V ±0.2 V	2.3		19	
		V_{CCB} = 3.3 V ±0.3 V	2.1		18.5	
		V_{CCB} = 5 V ±0.5 V	1.9		18.1	
t_{PHL}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	2.8		17.3	ns
		V_{CCB} = 2.5 V ±0.2 V	2.1		15.9	
		V_{CCB} = 3.3 V ±0.3 V	2		15.6	
		V_{CCB} = 5 V ±0.5 V	1.8		15.2	
t_{PHZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	5.2		22.7	ns
		V_{CCB} = 2.5 V ±0.2 V	4.8		21.5	
		V_{CCB} = 3.3 V ±0.3 V	4.7		21.4	
		V_{CCB} = 5 V ±0.5 V	5.1		20.1	
t_{PLZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	2.3		13.5	ns
		V_{CCB} = 2.5 V ±0.2 V	2.1		13.5	
		V_{CCB} = 3.3 V ±0.3 V	2.4		13.7	
		V_{CCB} = 5 V ±0.5 V	3.1		13.9	
t_{PHZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	7.4		27.9	ns
		V_{CCB} = 2.5 V ±0.2 V	4.9		14.5	
		V_{CCB} = 3.3 V ±0.3 V	3.6		13.3	
		V_{CCB} = 5 V ±0.5 V	2.3		11.2	
t_{PLZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	4.2		19	ns
		V_{CCB} = 2.5 V ±0.2 V	2.2		12.2	
		V_{CCB} = 3.3 V ±0.3 V	2.3		11.4	
		V_{CCB} = 5 V ±0.5 V	2		9.4	

Switching Characteristics: V_{CCA} = 1.8 V ±0.15 V (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PZH} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			39.7	ns
		V_{CCB} = 2.5 V ±0.2 V			31.2	
		V_{CCB} = 3.3 V ±0.3 V			29.9	
		V_{CCB} = 5 V ±0.5 V			27.5	
t_{PZL} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			45.2	ns
		V_{CCB} = 2.5 V ±0.2 V			30.4	
		V_{CCB} = 3.3 V ±0.3 V			28.9	
		V_{CCB} = 5 V ±0.5 V			26.4	
t_{PZH} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			34.2	ns
		V_{CCB} = 2.5 V ±0.2 V			26.8	
		V_{CCB} = 3.3 V ±0.3 V			25	
		V_{CCB} = 5 V ±0.5 V			24.1	
t_{PZL} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			40.7	ns
		V_{CCB} = 2.5 V ±0.2 V			33	
		V_{CCB} = 3.3 V ±0.3 V			31.5	
		V_{CCB} = 5 V ±0.5 V			30.1	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

6.7 Switching Characteristics: V_{CCA} = 2.5 V ±0.2 V

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2.3		19	ns
		V_{CCB} = 2.5 V ±0.2 V	1.5		11.5	
		V_{CCB} = 3.3 V ±0.3 V	1.3		9.4	
		V_{CCB} = 5 V ±0.5 V	1.1		8.1	
t_{PHL}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2.1		15.9	ns
		V_{CCB} = 2.5 V ±0.2 V	1.4		10.5	
		V_{CCB} = 3.3 V ±0.3 V	1.3		8.4	
		V_{CCB} = 5 V ±0.5 V	0.9		7.6	
t_{PLH}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	2.2		13.3	ns
		V_{CCB} = 2.5 V ±0.2 V	1.5		11.5	
		V_{CCB} = 3.3 V ±0.3 V	1.4		11	
		V_{CCB} = 5 V ±0.5 V	1		10.5	
t_{PHL}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	2.2		11.5	ns
		V_{CCB} = 2.5 V ±0.2 V	1.4		10.7	
		V_{CCB} = 3.3 V ±0.3 V	1.3		10	
		V_{CCB} = 5 V ±0.5 V	0.9		9.2	
t_{PHZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	3		11.1	ns
		V_{CCB} = 2.5 V ±0.2 V	2.1		11.1	
		V_{CCB} = 3.3 V ±0.3 V	2.3		11.1	
		V_{CCB} = 5 V ±0.5 V	3.2		11.1	
t_{PLZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	1.3		8.9	ns
		V_{CCB} = 2.5 V ±0.2 V	1.3		8.9	
		V_{CCB} = 3.3 V ±0.3 V	1.3		8.9	
		V_{CCB} = 5 V ±0.5 V	1		8.8	

Switching Characteristics: V_{CCA} = 2.5 V ±0.2 V (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	6.5		26.7	ns
		V_{CCB} = 2.5 V ±0.2 V	4.1		14.4	
		V_{CCB} = 3.3 V ±0.3 V	3		13.2	
		V_{CCB} = 5 V ±0.5 V	1.9		10.1	
t_{PLZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	3.5		21.9	ns
		V_{CCB} = 2.5 V ±0.2 V	2.2		12.6	
		V_{CCB} = 3.3 V ±0.3 V	2.5		11.4	
		V_{CCB} = 5 V ±0.5 V	1.6		8.3	
t_{PZH} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			35.2	ns
		V_{CCB} = 2.5 V ±0.2 V			24.1	
		V_{CCB} = 3.3 V ±0.3 V			22.4	
		V_{CCB} = 5 V ±0.5 V			18.8	
t_{PZL} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			38.2	ns
		V_{CCB} = 2.5 V ±0.2 V			24.9	
		V_{CCB} = 3.3 V ±0.3 V			23.2	
		V_{CCB} = 5 V ±0.5 V			19.3	
t_{PZH} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			27.9	ns
		V_{CCB} = 2.5 V ±0.2 V			20.4	
		V_{CCB} = 3.3 V ±0.3 V			18.3	
		V_{CCB} = 5 V ±0.5 V			16.9	
t_{PZL} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			27	ns
		V_{CCB} = 2.5 V ±0.2 V			21.6	
		V_{CCB} = 3.3 V ±0.3 V			19.5	
		V_{CCB} = 5 V ±0.5 V			18.7	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

6.8 Switching Characteristics: V_{CCA} = 3.3 V ±0.3 V

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2.1		18.5	ns
		V_{CCB} = 2.5 V ±0.2 V	1.4		11	
		V_{CCB} = 3.3 V ±0.3 V	0.7		8.8	
		V_{CCB} = 5 V ±0.5 V	0.7		7.4	
t_{PHL}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2		15.6	ns
		V_{CCB} = 2.5 V ±0.2 V	1.3		10	
		V_{CCB} = 3.3 V ±0.3 V	0.8		8	
		V_{CCB} = 5 V ±0.5 V	0.7		7	
t_{PLH}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	1.7		11.3	ns
		V_{CCB} = 2.5 V ±0.2 V	1.3		9.4	
		V_{CCB} = 3.3 V ±0.3 V	0.7		8.8	
		V_{CCB} = 5 V ±0.5 V	0.6		8.4	
t_{PHL}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	1.8		10.1	ns
		V_{CCB} = 2.5 V ±0.2 V	1.3		8.4	
		V_{CCB} = 3.3 V ±0.3 V	0.8		8	
		V_{CCB} = 5 V ±0.5 V	0.7		7.5	

Switching Characteristics: V_{CCA} = 3.3 V ±0.3 V (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	2.3		10.3	ns
		V_{CCB} = 2.5 V ±0.2 V	2.4		10.3	
		V_{CCB} = 3.3 V ±0.3 V	1.5		10.3	
		V_{CCB} = 5 V ±0.5 V	2.4		10.3	
t_{PLZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	1.8		8.6	ns
		V_{CCB} = 2.5 V ±0.2 V	1.6		8.6	
		V_{CCB} = 3.3 V ±0.3 V	1.9		8.7	
		V_{CCB} = 5 V ±0.5 V	2		8.7	
t_{PHZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	5.4		27.5	ns
		V_{CCB} = 2.5 V ±0.2 V	3.9		13.1	
		V_{CCB} = 3.3 V ±0.3 V	2.9		11.8	
		V_{CCB} = 5 V ±0.5 V	1.7		9.8	
t_{PLZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2.3		17.5	ns
		V_{CCB} = 2.5 V ±0.2 V	2.1		10.8	
		V_{CCB} = 3.3 V ±0.3 V	2.4		10.1	
		V_{CCB} = 5 V ±0.5 V	1.5		7.9	
t_{PZH} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			28.8	ns
		V_{CCB} = 2.5 V ±0.2 V			20.2	
		V_{CCB} = 3.3 V ±0.3 V			18.9	
		V_{CCB} = 5 V ±0.5 V			16.3	
t_{PZL} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			37.6	ns
		V_{CCB} = 2.5 V ±0.2 V			21.5	
		V_{CCB} = 3.3 V ±0.3 V			19.8	
		V_{CCB} = 5 V ±0.5 V			17.3	
t_{PZH} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			27.1	ns
		V_{CCB} = 2.5 V ±0.2 V			19.6	
		V_{CCB} = 3.3 V ±0.3 V			17.5	
		V_{CCB} = 5 V ±0.5 V			16.1	
t_{PZL} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			25.9	ns
		V_{CCB} = 2.5 V ±0.2 V			20.3	
		V_{CCB} = 3.3 V ±0.3 V			18.3	
		V_{CCB} = 5 V ±0.5 V			17.3	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

6.9 Switching Characteristics: V_{CCA} = 5 V ±0.5 V

over operating free-air temperature range (unless otherwise noted; see Figure 17)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	1.9		18.1	ns
		V_{CCB} = 2.5 V ±0.2 V	1		10.5	
		V_{CCB} = 3.3 V ±0.3 V	0.6		8.4	
		V_{CCB} = 5 V ±0.5 V	0.5		6.9	
t_{PHL}	From A (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	1.8		15.2	ns
		V_{CCB} = 2.5 V ±0.2 V	0.9		9.2	
		V_{CCB} = 3.3 V ±0.3 V	0.7		7.5	
		V_{CCB} = 5 V ±0.5 V	0.5		6.5	
t_{PLH}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	1.4		10.2	ns
		V_{CCB} = 2.5 V ±0.2 V	1		8.1	
		V_{CCB} = 3.3 V ±0.3 V	0.7		7.4	
		V_{CCB} = 5 V ±0.5 V	0.5		6.9	
t_{PHL}	From B (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	1.7		10	ns
		V_{CCB} = 2.5 V ±0.2 V	0.9		7.6	
		V_{CCB} = 3.3 V ±0.3 V	0.7		7	
		V_{CCB} = 5 V ±0.5 V	0.5		6.5	
t_{PHZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	2.1		8.4	ns
		V_{CCB} = 2.5 V ±0.2 V	2		8.4	
		V_{CCB} = 3.3 V ±0.3 V	2.2		8.5	
		V_{CCB} = 5 V ±0.5 V	2		8.4	
t_{PLZ}	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V	0.9		6.8	ns
		V_{CCB} = 2.5 V ±0.2 V	1		6.8	
		V_{CCB} = 3.3 V ±0.3 V	1		6.7	
		V_{CCB} = 5 V ±0.5 V	0.9		6.7	
t_{PHZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	4.8		26.2	ns
		V_{CCB} = 2.5 V ±0.2 V	2.5		14.8	
		V_{CCB} = 3.3 V ±0.3 V	1		11.5	
		V_{CCB} = 5 V ±0.5 V	1.7		9.5	
t_{PLZ}	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V	2.6		17.8	ns
		V_{CCB} = 2.5 V ±0.2 V	2		10.4	
		V_{CCB} = 3.3 V ±0.3 V	2.5		10	
		V_{CCB} = 5 V ±0.5 V	1.6		7.5	
t_{PZH} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			28	ns
		V_{CCB} = 2.5 V ±0.2 V			18.5	
		V_{CCB} = 3.3 V ±0.3 V			17.4	
		V_{CCB} = 5 V ±0.5 V			14.4	
t_{PZL} (1)	From DIR (input) to A (output)	V_{CCB} = 1.8 V ±0.15 V			36.2	ns
		V_{CCB} = 2.5 V ±0.2 V			22.4	
		V_{CCB} = 3.3 V ±0.3 V			18.5	
		V_{CCB} = 5 V ±0.5 V			16	
t_{PZH} (1)	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			24.9	ns
		V_{CCB} = 2.5 V ±0.2 V			17.3	
		V_{CCB} = 3.3 V ±0.3 V			15.1	
		V_{CCB} = 5 V ±0.5 V			13.6	

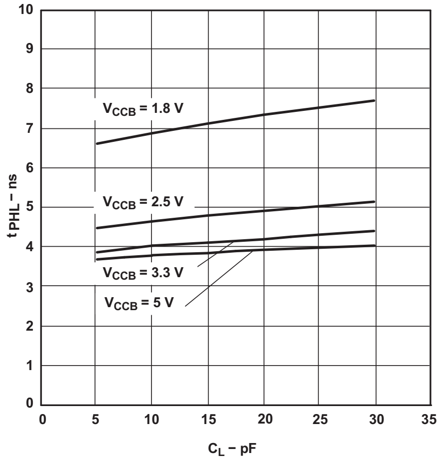
(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

Switching Characteristics: V_{CCA} = 5 V ±0.5 V (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 17)

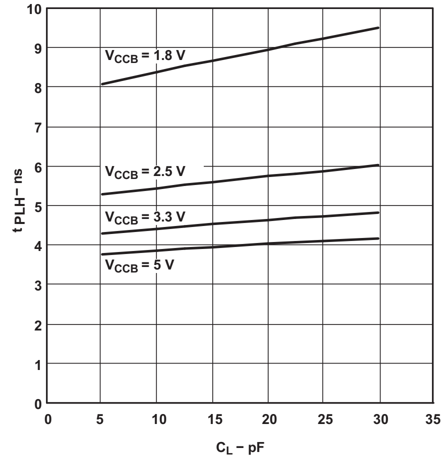
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PZL} [(1)]	From DIR (input) to B (output)	V_{CCB} = 1.8 V ±0.15 V			23.6	ns
		V_{CCB} = 2.5 V ±0.2 V			17.6	
		V_{CCB} = 3.3 V ±0.3 V			16	
		V_{CCB} = 5 V ±0.5 V			14.9	

6.10 Typical Characteristics



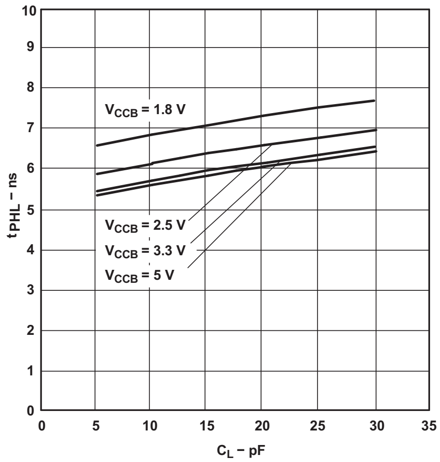
T_A = 25°C, V_{CCA} = 1.8 V

Figure 1. Typical Propagation Delay (A to B) vs Load Capacitance



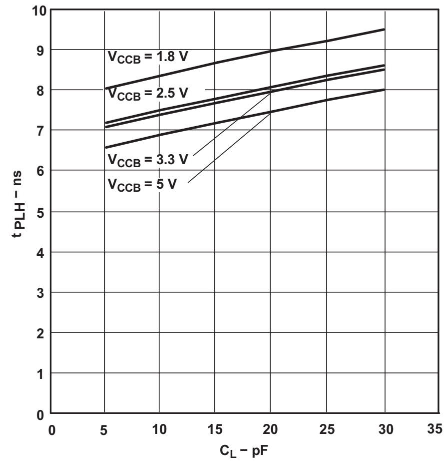
T_A = 25°C, V_{CCA} = 1.8 V

Figure 2. Typical Propagation Delay (A to B) vs Load Capacitance



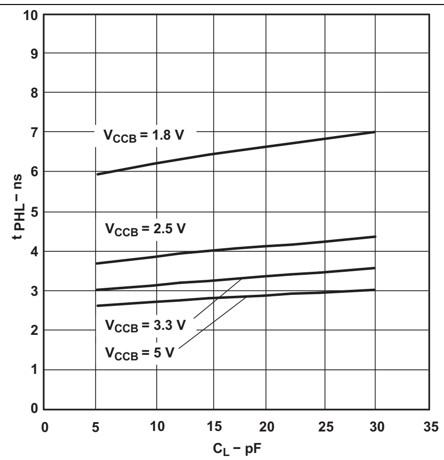
T_A = 25°C, V_{CCA} = 1.8 V

Figure 3. Typical Propagation Delay (B to A) vs Load Capacitance



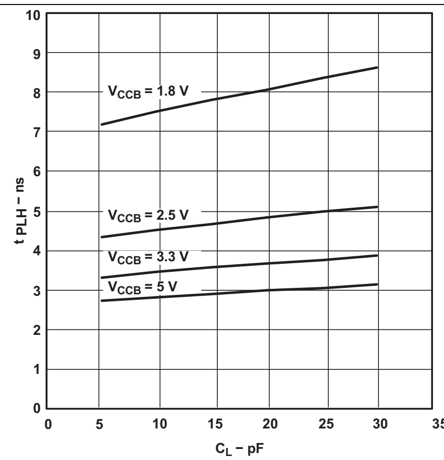
T_A = 25°C, V_{CCA} = 1.8 V

Figure 4. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 2.5 V

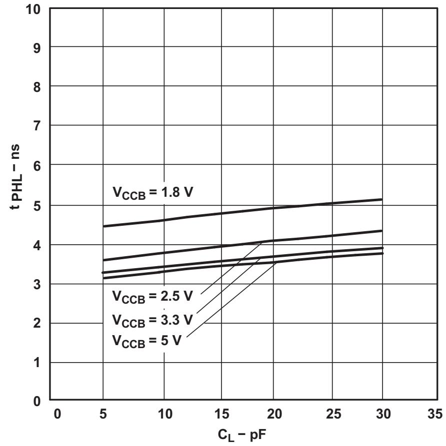
Figure 5. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 2.5 V

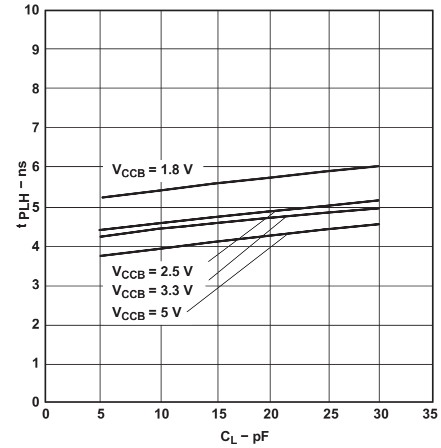
Figure 6. Typical Propagation Delay (A to B) vs Load Capacitance

Typical Characteristics (continued)



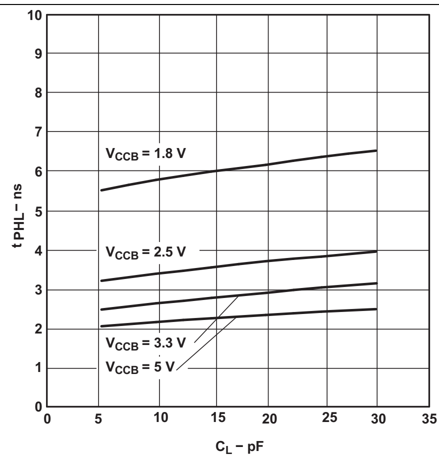
T_A = 25°C, V_{CCA} = 2.5 V

Figure 7. Typical Propagation Delay (B to A) vs Load Capacitance



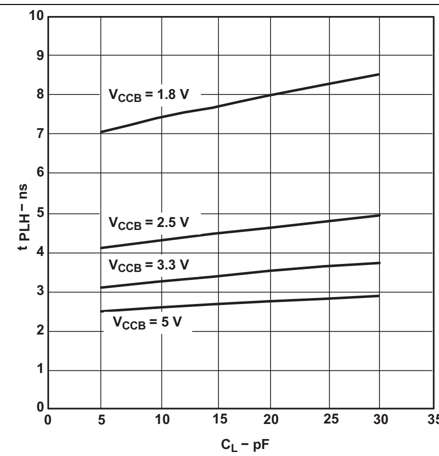
T_A = 25°C, V_{CCA} = 2.5 V

Figure 8. Typical Propagation Delay (B to A) vs Load Capacitance



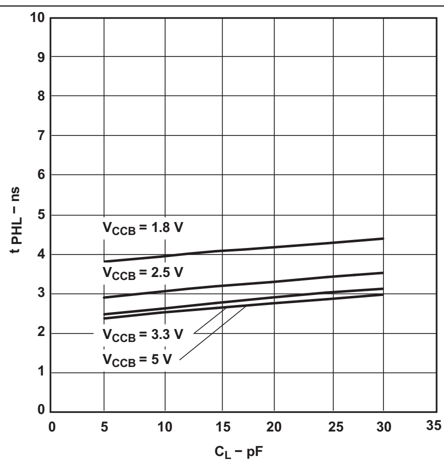
T_A = 25°C, V_{CCA} = 3.3 V

Figure 9. Typical Propagation Delay (A to B) vs Load Capacitance



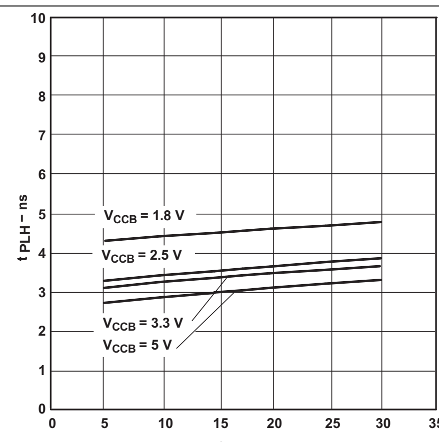
T_A = 25°C, V_{CCA} = 3.3 V

Figure 10. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3 V

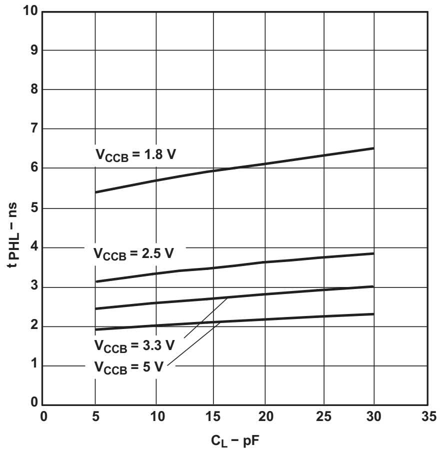
Figure 11. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3 V

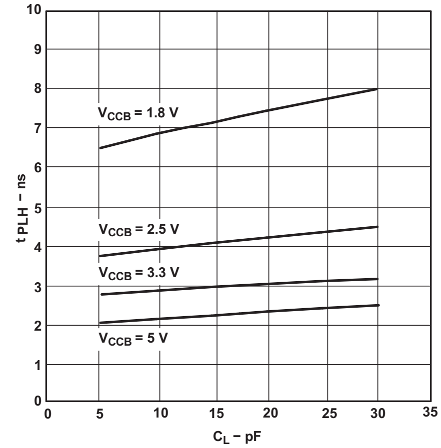
Figure 12. Typical Propagation Delay (B to A) vs Load Capacitance

Typical Characteristics (continued)



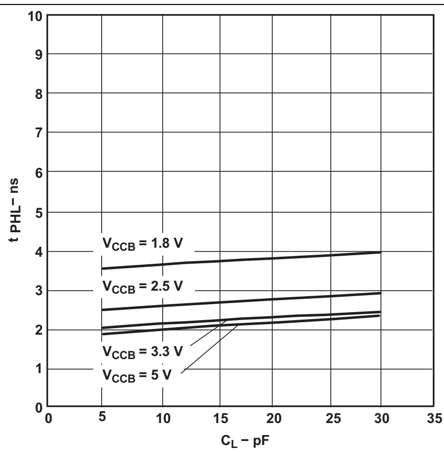
T_A = 25°C, V_{CCA} = 5 V

Figure 13. Typical Propagation Delay (A to B) vs Load Capacitance



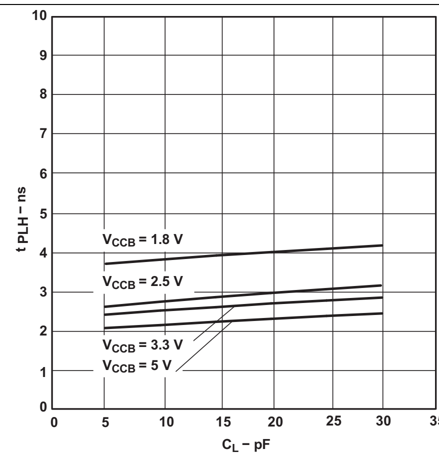
T_A = 25°C, V_{CCA} = 5 V

Figure 14. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

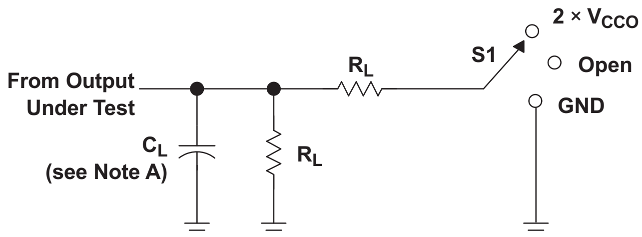
Figure 15. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

Figure 16. Typical Propagation Delay (B to A) vs Load Capacitance

7 Parameter Measurement Information

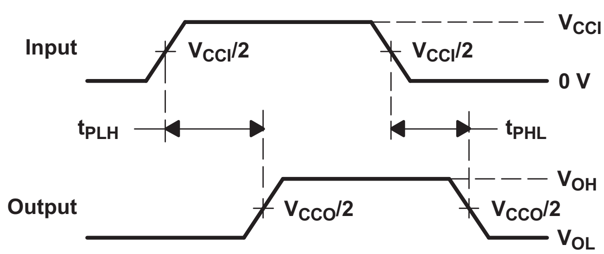


LOAD CIRCUIT

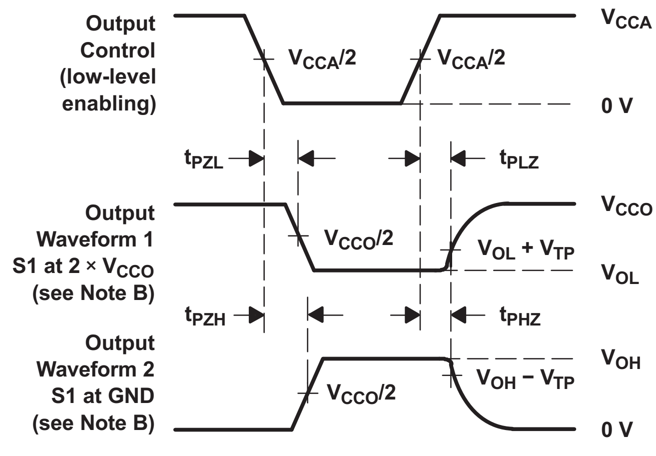
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 17. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1T45-Q1 is single-bit, dual-supply, non-inverting voltage level translation. Pin A and that direction control pin (DIR) are supported by V_{CCA} and pin B is supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on the DIR allows data transmissions from A to B and a low on the DIR allows data transmissions from B to A.

8.2 Functional Block Diagram

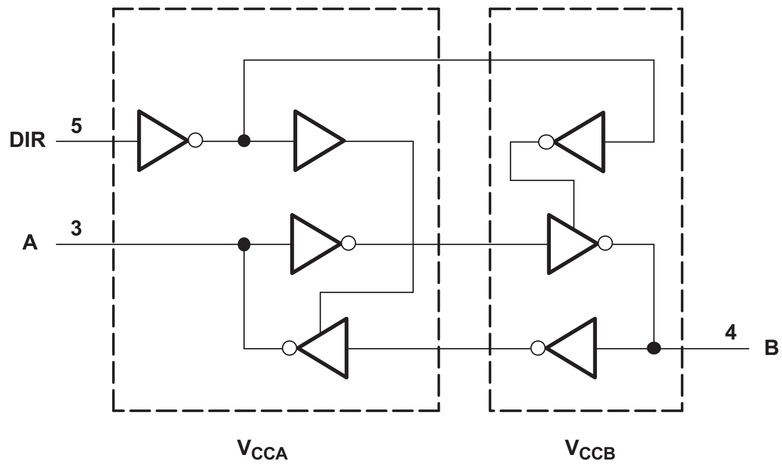


Figure 18. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74LVC1T45-Q1 has a fully configurable dual-rail design that allows each port to operate over the full 1.65-V to 5.5-V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8-V, 2.5-V, 3.3-V and 5-V).

SN74LVC1T45-Q1 can support high data rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5 V.

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

8.4 Device Functional Modes

Table 1 lists the operational modes of SN74LVC1T45-Q1.

Table 1. Function Table(1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The max data rate can be up to 420 Mbps when device translates signals from 3.3 V to 5 V.

9.1.1 Enable Times

Calculate the enable times for the SN74LVC1T45-Q1 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.2 Typical Applications

9.2.1 Unidirectional Logic Level-Shifting Application

Figure 19 shows an example of the SN74LVC1T45-Q1 being used in a unidirectional logic level-shifting application.

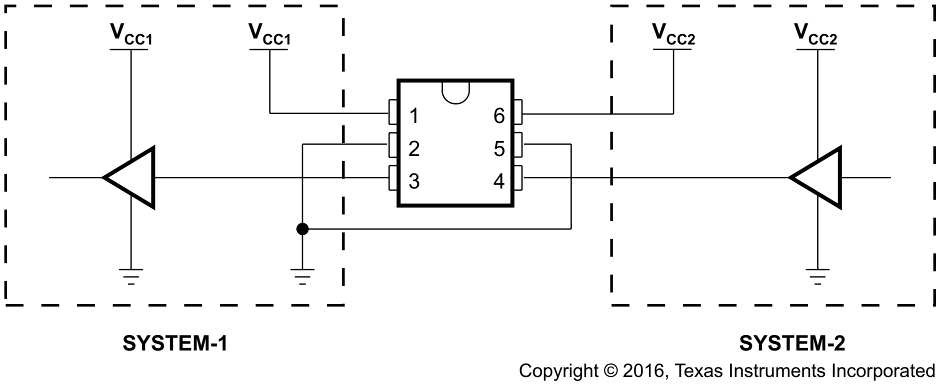


Figure 19. Unidirectional Logic Level-Shifting Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Input voltage	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC1T45 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC1T45 device is driving to determine the output voltage range.

9.2.1.3 Application Curve

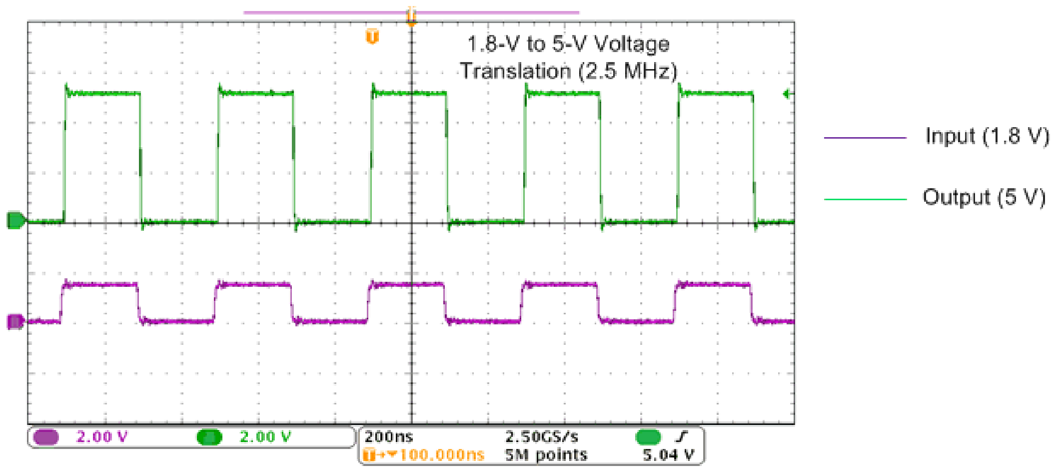


Figure 20. Translation Up (1.8 V to 5 V) at 2.5 MHz

9.2.2 Bidirectional Logic Level-Shifting Application

Figure 21 shows the SN74LVC1T45-Q1 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45-Q1 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

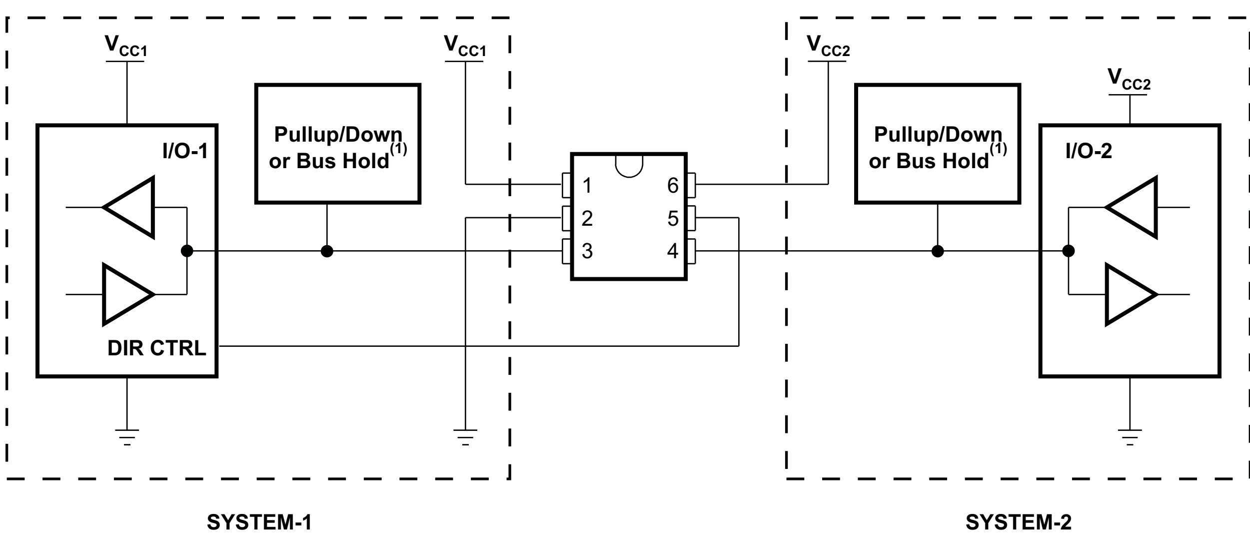


Figure 21. Bidirectional Logic Level-Shifting Application

9.2.2.1 Detailed Design Procedure

Table 3 shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 3. Data Transmission

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

9.2.2.2 Application Curve

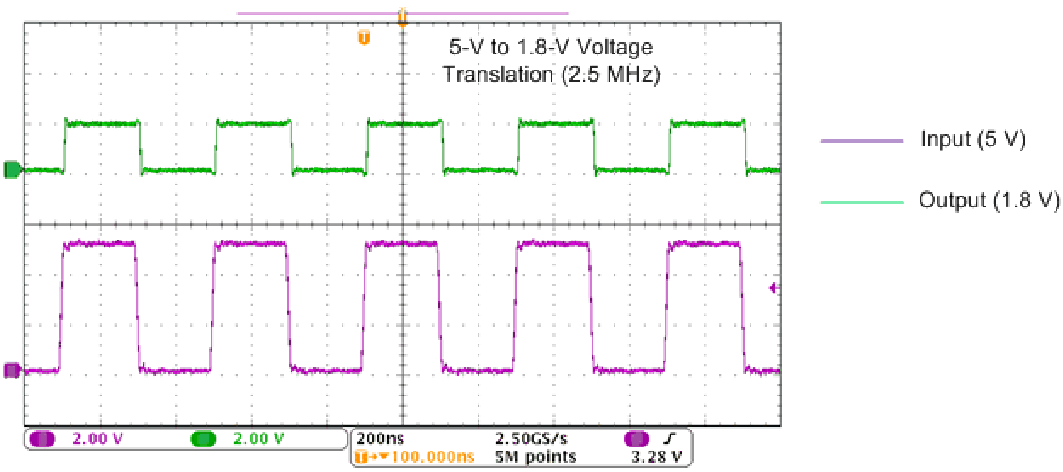


Figure 22. Translation Down (5 V to 1.8 V) at 2.5 MHz

10 Power Supply Recommendations

The SN74LVC1T45-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V, and V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For multiple V_{CC} pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

A proper power-up sequence is advisable as listed in the following:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCB}.
3. V_{CCA} can be ramped up along with V_{CCB}.

TI recommends that the inputs are grounded during power up. Take care to assure that any state changes do not affect system level operation.

11 Layout

11.1 Layout Guidelines

To assure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depends on the system requirements.

11.2 Layout Example

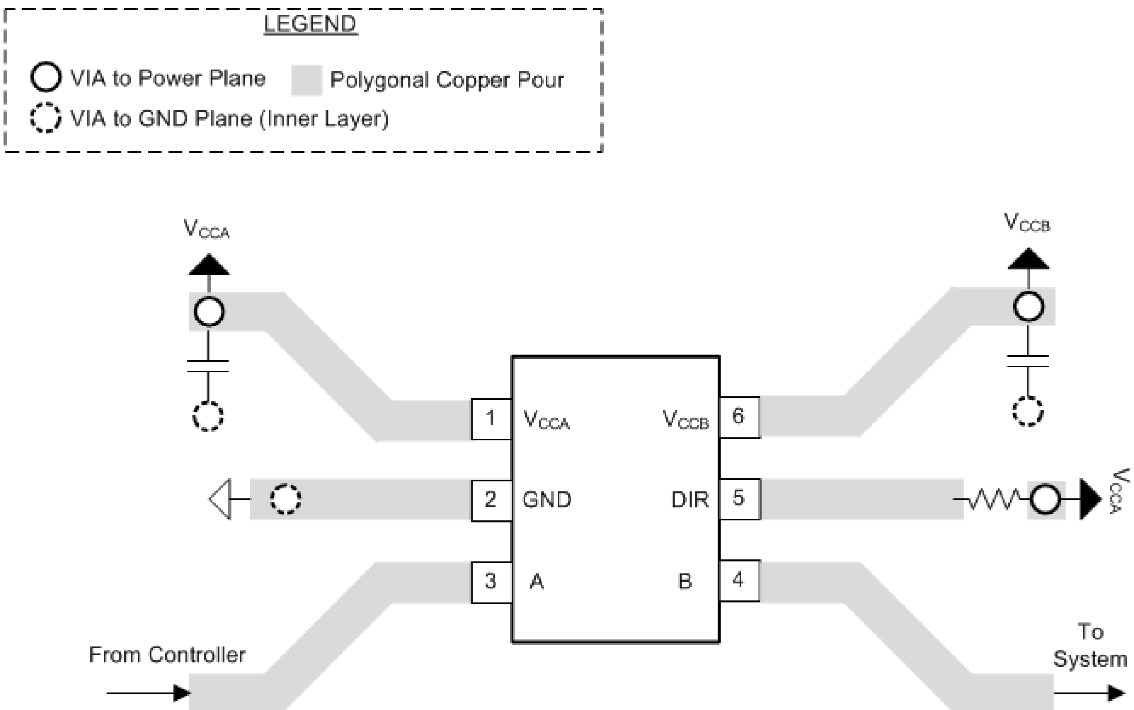


Figure 23. Layout Schematic

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1T45QDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5TR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1T45-Q1 :

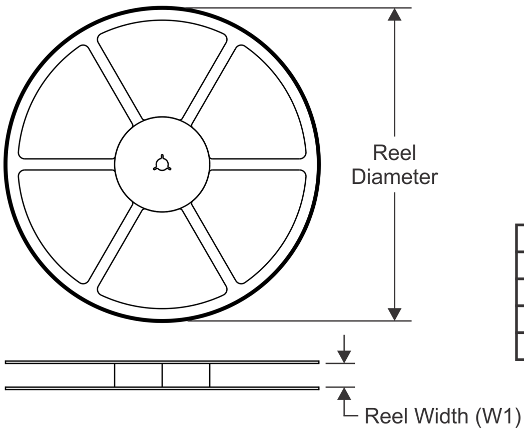
- Catalog: SN74LVC1T45
- Enhanced Product: SN74LVC1T45-EP

NOTE: Qualified Version Definitions:

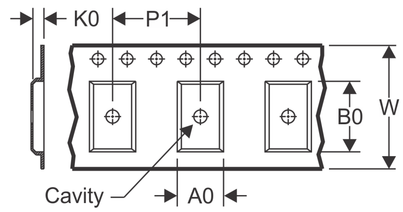
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

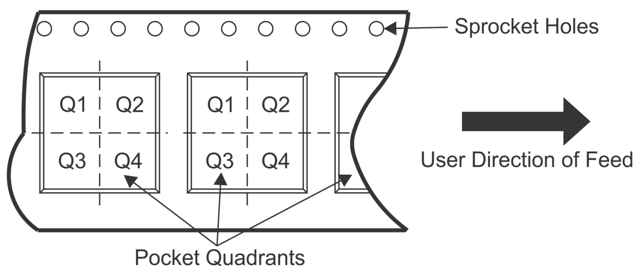


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

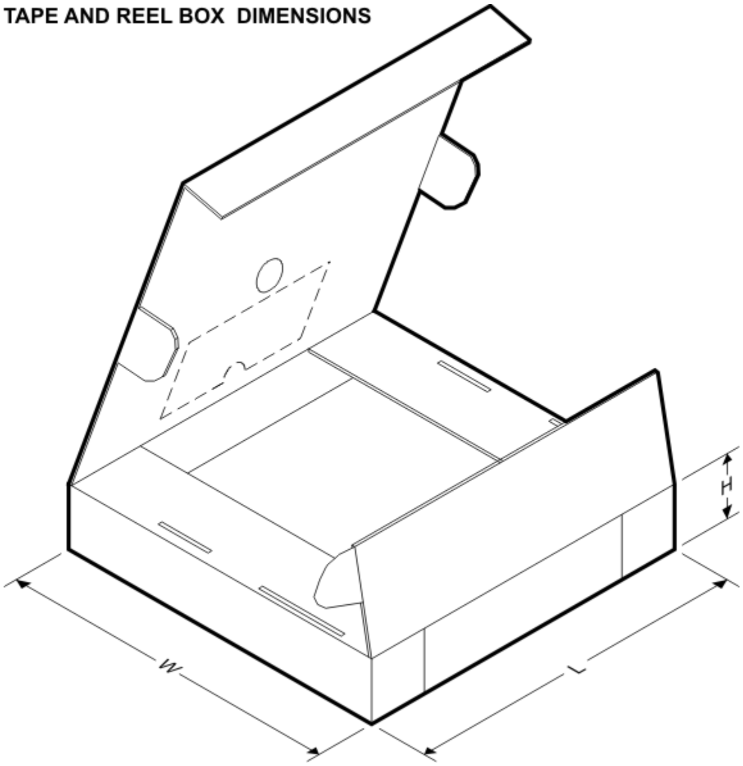
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

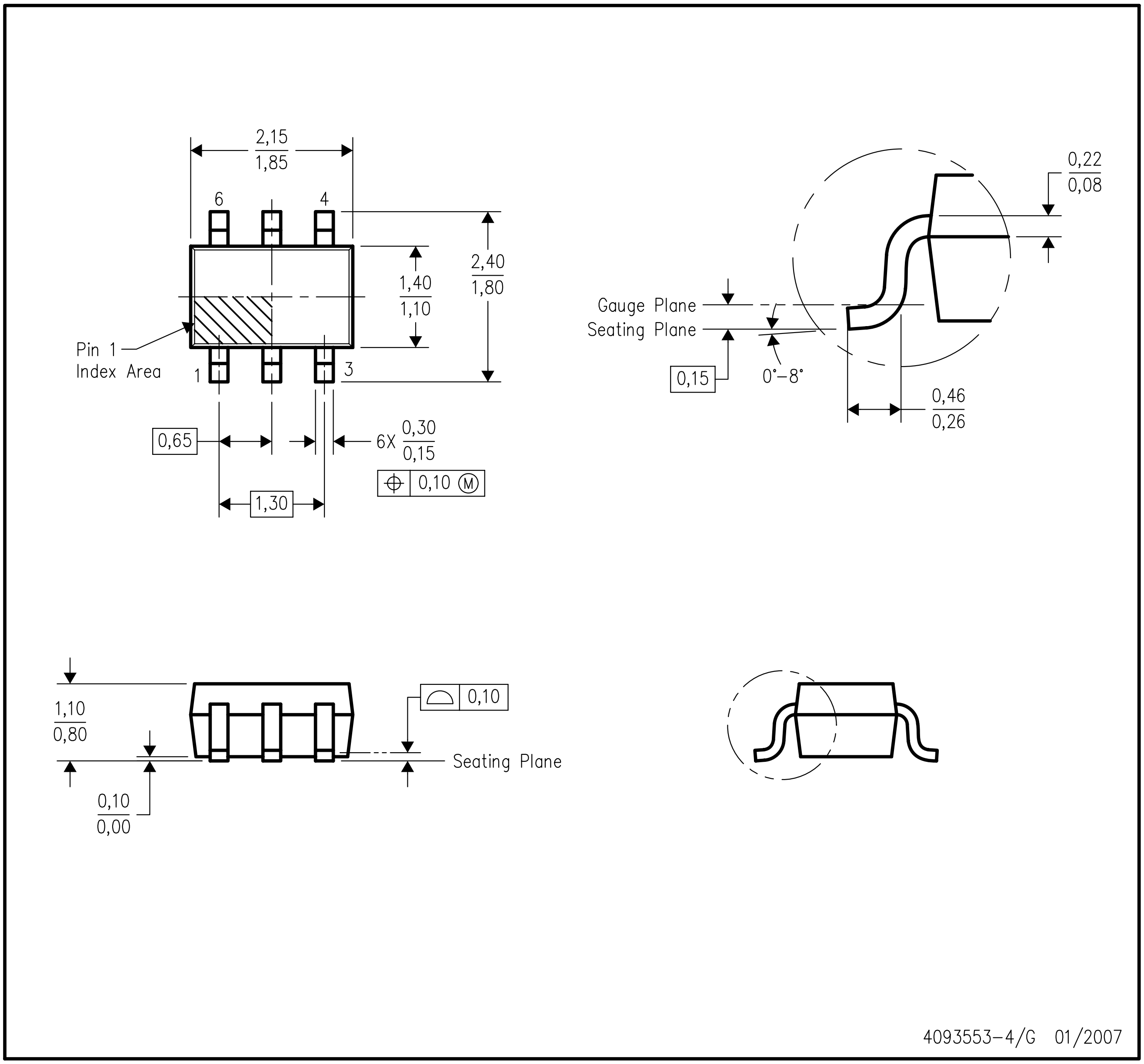
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

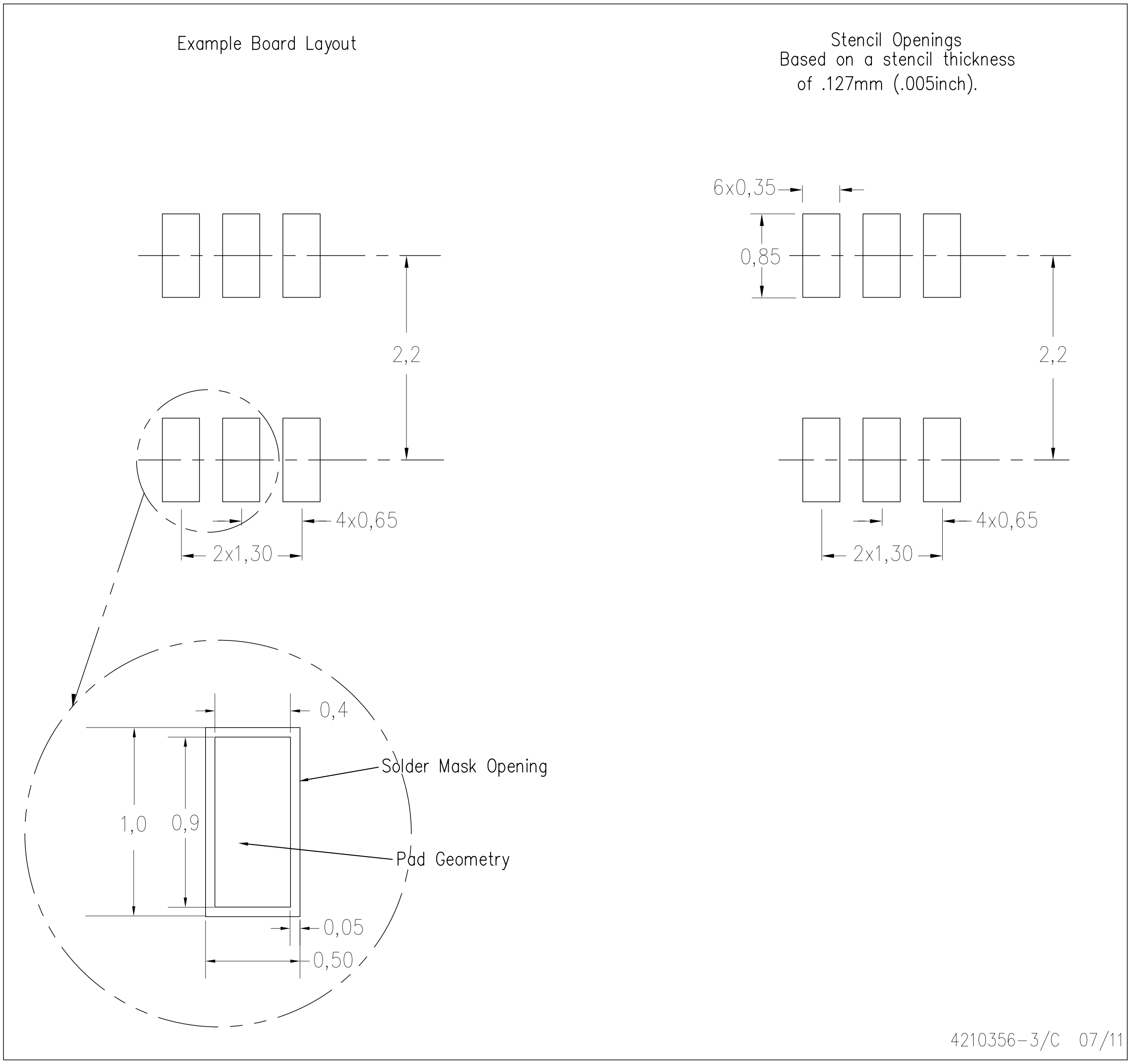
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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