AAT2512

Dual 1.4MHz, 400mA Synchronous Buck DC/DC Converter

General Description

The AAT2512 is a member of Skyworks' Total Power Management IC (TPMIC™) product family. It is a dual channel synchronous buck converter operating with an input voltage range of 2.7V to 5.5V, making it ideal for applications with single-cell lithium-ion/polymer batteries.

Both regulators have independent input and enable pins. Offered with fixed or adjustable output voltages, each channel is designed to operate with 27µA (typical) of quiescent current, allowing for high efficiency under light load conditions.

The AAT2512 requires only three external components (C_{IN}, C_{OUT}, and L_X) for each converter, minimizing cost and real estate. Both channels are designed to deliver 400mA of load current and operate with a switching frequency of 1.4MHz, reducing the size of external components.

The AAT2512 is available in a Pb-free, 12-pin TDFN33 package and is rated over the -40°C to +85°C temperature range.

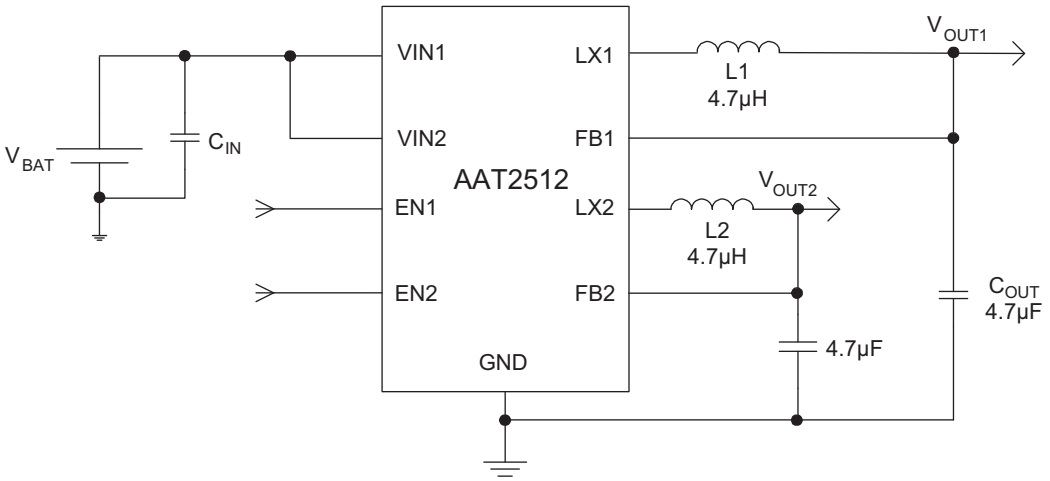
Features

- V_{IN} Range: 2.7V to 5.5V
- Output Current:
  - Channel 1: 400mA
  - Channel 2: 400mA
- 98% Efficient Step-Down Converter
- Integrated Power Switches
- 100% Duty Cycle
- 1.4MHz Switching Frequency
- Internal Soft Start
- 150µs Typical Turn-On Time
- Over-Temperature Protection
- Current Limit Protection
- Available in TDFN33-12 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor / DSP Core/ IO Power
- PDAs and Handheld Computers

Typical Application

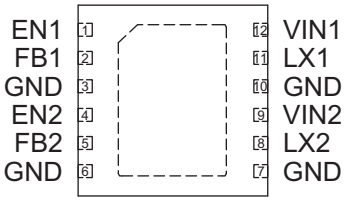


Pin Descriptions

Pin #	Symbol	Function
1	EN1	Enable pin for Channel 1. When connected low, it disables the channel and consumes less than 1µA of current. When connected high, normal operation.
2	FB1	Feedback input pin for Channel 1. This pin is connected to the converter output. It is used to see the output of the converter to regulate to the desired value via an external resistor divider.
3, 6, 7, 10	GND	Ground.
4	EN2	Enable pin for Channel 2. When connected low, it disables the channel and consumes less than 1µA of current. When connected high, normal operation.
5	FB2	Feedback input pin for Channel 2. This pin is connected to the converter output. It is used to see the output of the converter to regulate to the desired value via an external resistor divider.
8	LX2	Power switching node for Channel 2. Output switching node that connects to the output inductor.
9	VIN2	Input supply voltage for Channel 2. Must be closely decoupled.
11	LX1	Power switching node for Channel 2. Output switching node that connects to the output inductor.
12	VIN1	Input supply voltage for Channel 1. Must be closely decoupled.

Pin Configuration

TDFN33-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	Input Voltages to GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_P + 0.3	V
V_{FB}	FB1 and FB2 to GND	-0.3 to V_P + 0.3	V
V_{EN}	EN1 and EN2 to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation	2.0	W
θ_{JA}	Thermal Resistance[2]	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

V_{IN} = 3.6V; T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

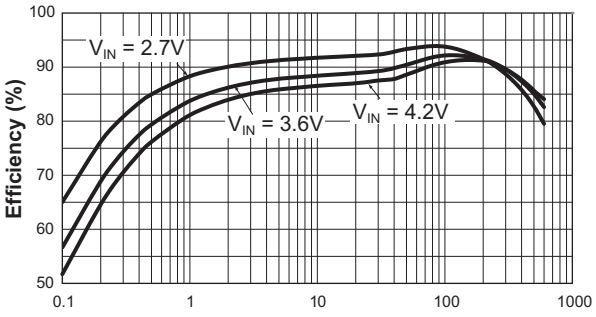
Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.7		5.5	V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0 to 400mA; V_{IN} = 2.7V to 5.5V	-3.0		3.0	%
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
I_Q	Quiescent Current	Per Channel		27	70	µA
I_{SHDN}	Shutdown Current	EN1 = EN2 = GND			1.0	µA
I_{LX_LEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}			1.0	µA
I_{FB}	Feedback Leakage	V_{FB} = 1.0V			0.2	µA
I_{LIM}	P-Channel Current Limit	Both Channels		1.2		A
$R_{DS(ON)H}$	High Side Switch On Resistance			0.45		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.40		Ω
ΔV_{LINE}	Line Regulation	V_{IN} = 2.7V to 5.5V		0.2		%
F_{OSC}	Oscillator Frequency			1.4		MHz
T_S	Start-Up Time	From Enable to Output Regulation; Both Channels		150		µs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
I_{EN}	Input Low Current	V_{IN} = V_{FB} = 5.5V	-1.0		1.0	µA

1. The AAT2512 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

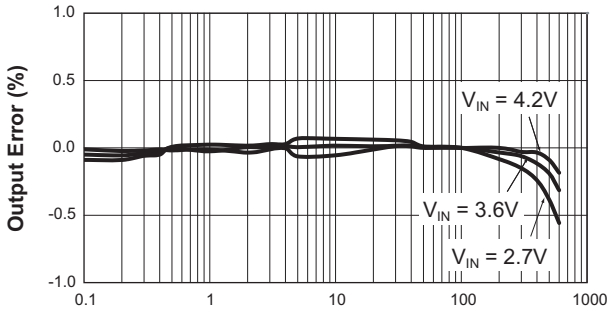
Typical Characteristics

EN1 = V_{IN}; EN2 = GND.

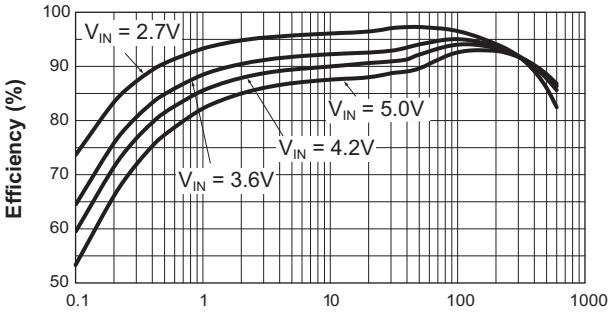
Efficiency vs. Load
(V_{OUT} = 1.8V; L = 4.7µH)



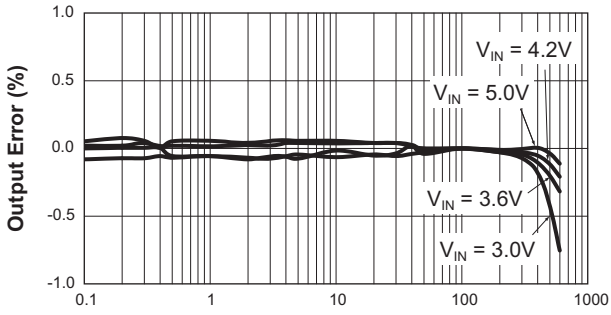
DC Regulation
(V_{OUT} = 1.8V)



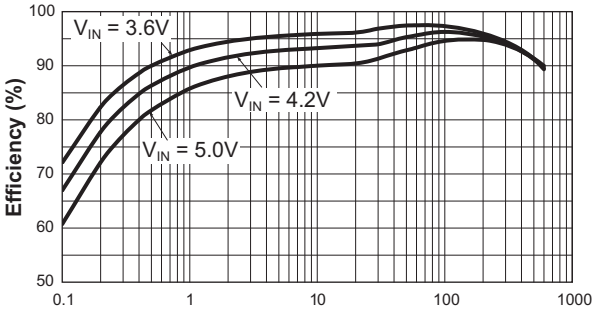
Efficiency vs. Load
(V_{OUT} = 2.5V; L = 6.8µH)



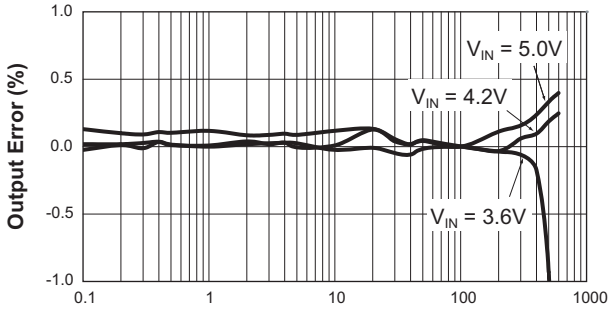
DC Regulation
(V_{OUT} = 2.5V)



Efficiency vs. Load
(V_{OUT} = 3.3V; L = 6.8µH)



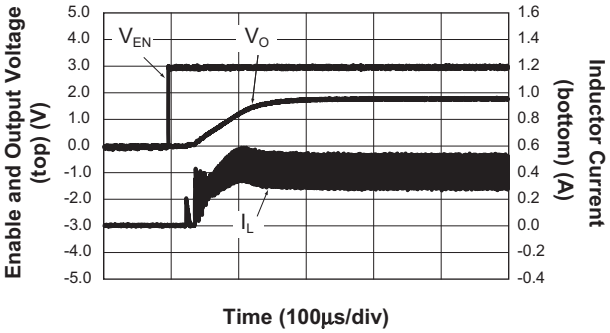
DC Regulation
(V_{OUT} = 3.3V; L = 6.8µH)



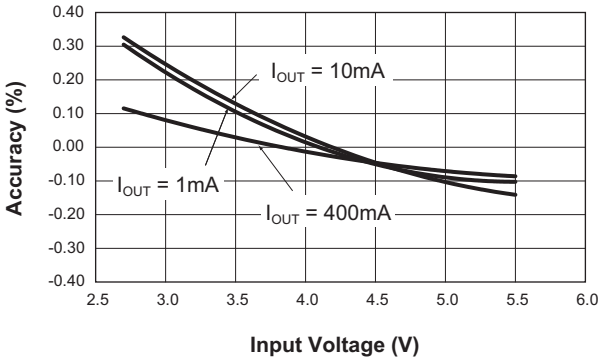
Typical Characteristics

EN1 = V_{IN}; EN2 = GND.

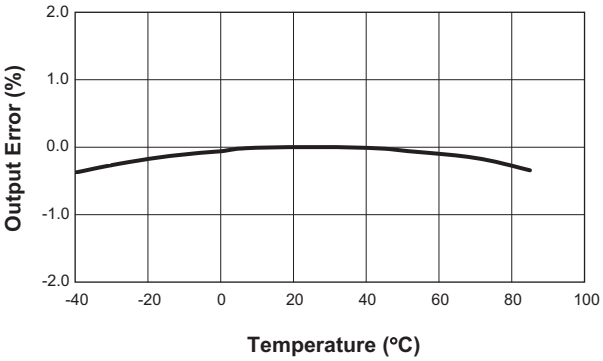
Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 400mA)



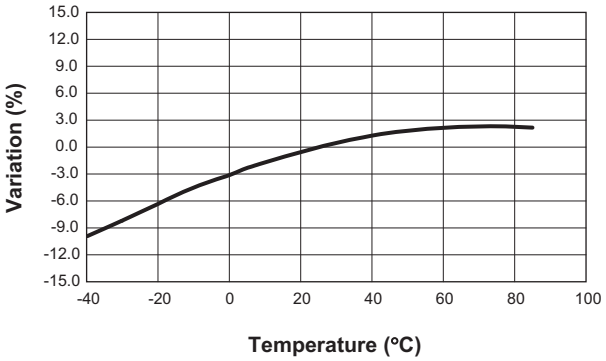
Line Regulation
(V_{OUT} = 1.8V)



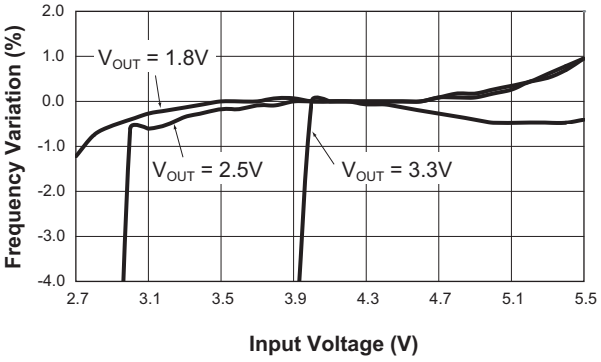
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_O = 1.8V; I_{OUT} = 400mA)



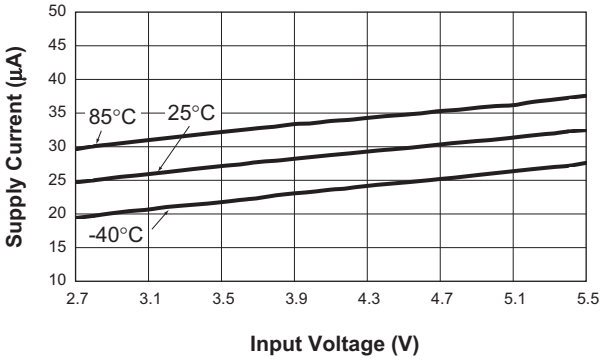
Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V)



Frequency vs. Input Voltage



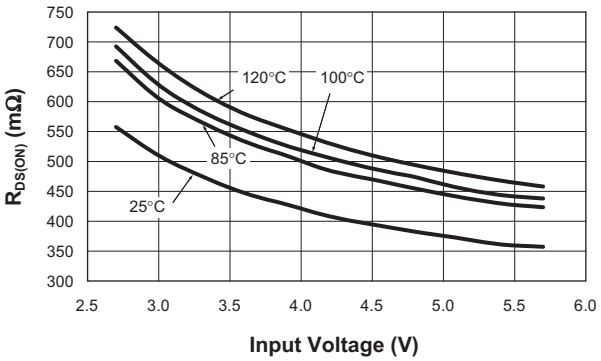
No Load Quiescent Current vs. Input Voltage



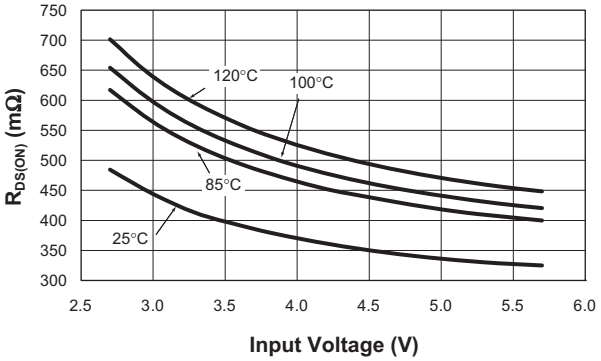
Typical Characteristics

EN1 = V_{IN}; EN2 = GND.

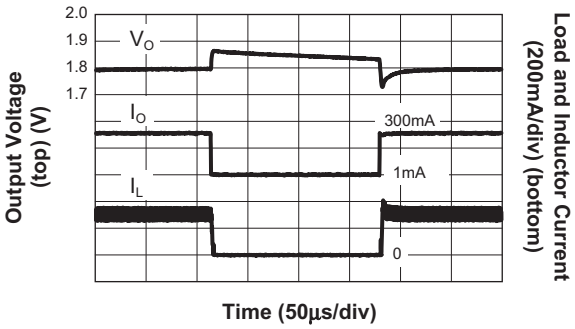
P-Channel $R_{DS(ON)}$ vs. Input Voltage



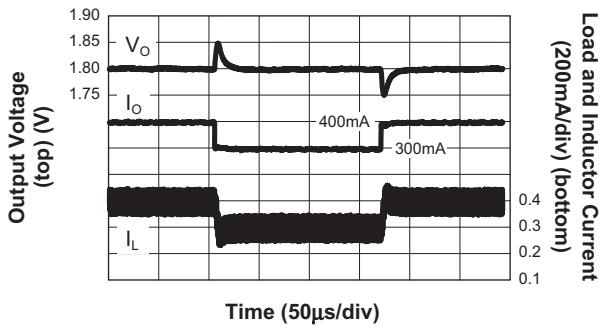
N-Channel $R_{DS(ON)}$ vs. Input Voltage



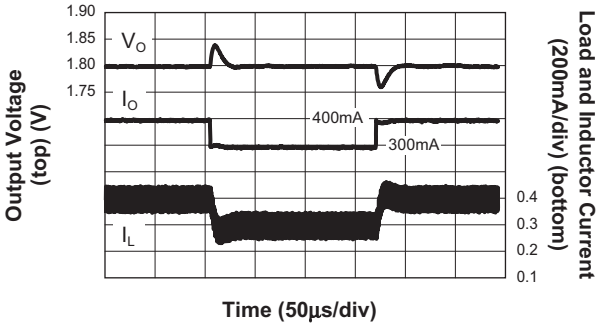
Load Transient Response
(1mA to 300mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_1 = 10µF; C_{FF} = 100pF)



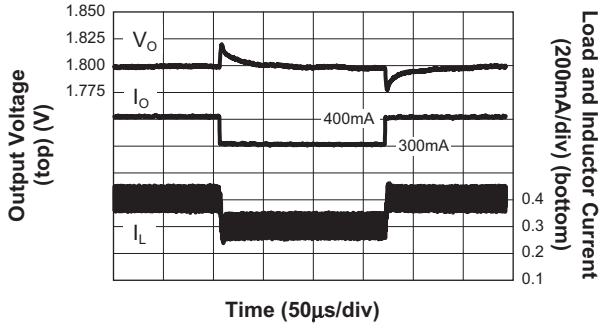
Load Transient Response
(300mA to 400mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_1 = 4.7µF)



Load Transient Response
(300mA to 400mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_1 = 10µF)



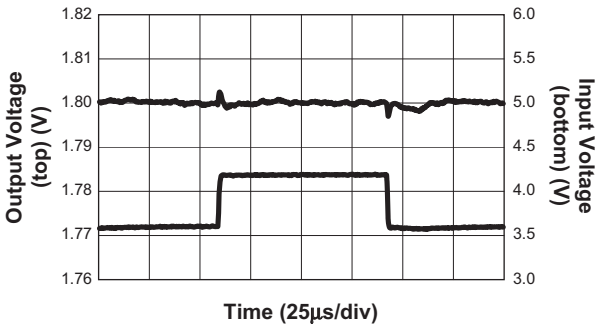
Load Transient Response
(300mA to 400mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_1 = 10µF; C_4 = 100pF)



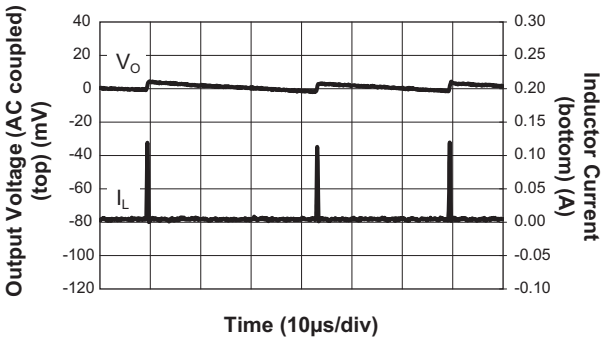
Typical Characteristics

EN1 = V_{IN}; EN2 = GND.

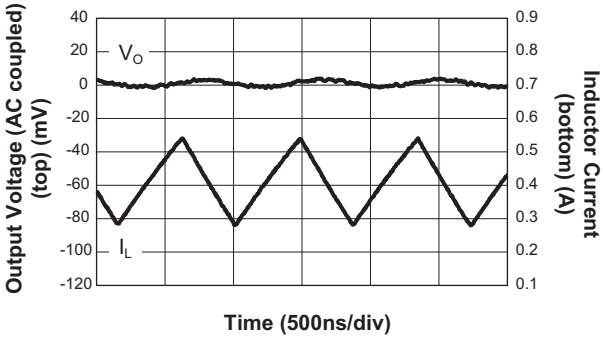
Line Response
(V_{OUT} = 1.8V @ 400mA)



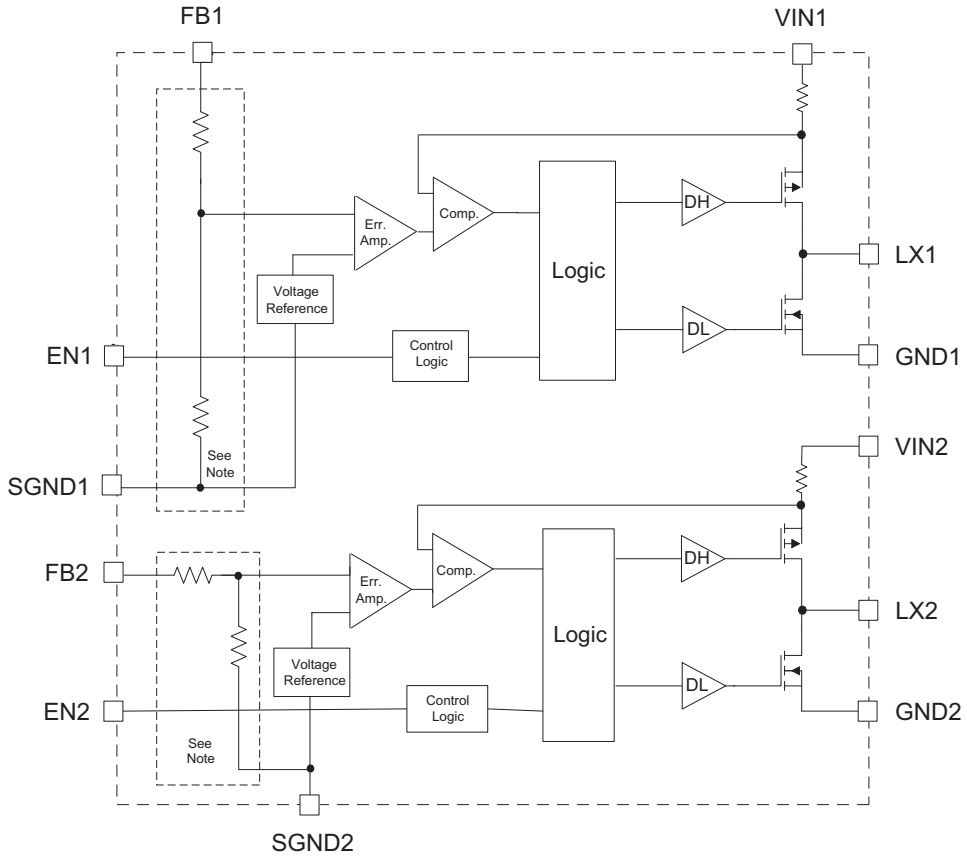
Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA)



Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 400mA)



Functional Block Diagram



Note: Internal resistor divider included for ≥1.2V versions. For low voltage versions, the feedback pin is tied directly to the error amplifier input.

Functional Description

The AAT2512 is a high performance power management IC comprised of two buck converters. Each channel has independent input voltages and enable/disable pins. Designed to operate at 1.4MHz of switching frequency, the converters require only three external components (C_{IN}, C_{OUT}, and L_X), minimizing cost and size of external components.

Both converters are designed to operate with an input voltage range of 2.7V to 5.5V. Typical values of the output filter are 4.7µH and 4.7µF ceramic capacitor. The output voltage operates to as low as 0.6V and is offered as both fixed and adjustable. Power devices are sized for 400mA current capability while maintaining over 90% efficiency at full load. Light load efficiency is maintained at greater than 80% down to 500µA of load current. Both channels have excellent transient response, load, and line regulation. Transient response time is typically less than 20µs.

The AAT2512 also features soft-start control to limit inrush current. Soft start increases the inductor current limit point in discrete steps when power is applied to the input or when the enable pins are pulled high. It limits the current surge seen at the input and eliminates output voltage overshoot. The enable input, when pulled low, forces the converter into a low power, non-switching state consuming less than 1µA of current.

For overload conditions, the peak input current is limited. As load impedance decreases and the output voltage falls closer to zero, more power is dissipated internally, raising the device temperature. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis. The under-voltage lockout guarantees sufficient V_{IN} bias and proper operation of all internal circuits prior to activation.

Applications Information

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low-voltage fixed versions of the AAT2512 is 0.24A/µsec. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.5V output and 4.7µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.5V}{4.7\mu H} = 0.24 \frac{A}{\mu sec}$$

This is the internal slope compensation for the adjustable (0.6V) version or low-voltage fixed version. When externally programming the 0.6V version to a 2.5V output, the calculated inductance would be 7.5µH.

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75V}{0.24A/\mu sec} \approx 3\frac{\mu sec}{A} \cdot V_O$$

$$= 3\frac{\mu sec}{A} \cdot 2.5V = 7.5\mu H$$

In this case, a standard 6.8µH value is selected. For high-voltage fixed versions (2.5V and above), m = 0.48A/µsec. Table 1 displays inductor values for the AAT2512 fixed and adjustable options.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 4.7µH CDRH3D16 series inductor selected from Sumida has a 105mΩ DCR and a 900mA DC current rating. At full load, the inductor DC loss is 17mW which gives a 2.8% loss in efficiency for a 400mA 1.5V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

This equation provides an estimate for the input capacitor required for a single channel.

The equation below solves for input capacitor size for both channels. It makes the worst-case assumptions that both converters are operating at 50% duty cycle and are synchronized.

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \bullet 4 \bullet F_S}$$

Because the AAT2512 channels will generally operate at different duty cycles and are not synchronized, the actual ripple will vary and be less than the ripple (V_{PP}) used to solve for the input capacitor in the equation above.

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF 6.3V X5R ceramic capacitor with 5V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{O1} \cdot \left(\sqrt{\frac{V_{O1}}{V_{IN}} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right)}\right) + I_{O2} \cdot \left(\sqrt{\frac{V_{O2}}{V_{IN}} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right)}\right)$$

Configuration	Output Voltage	Inductor
0.6V Adjustable With External Feedback	1V, 1.2V	2.2µH
	1.5V, 1.8V	4.7µH
	2.5V, 3.3V	6.8µH
Fixed Output	0.6V to 3.3V	4.7µH

Table 1: Inductor Values.

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current of both converters combined.

$$I_{RMS(MAX)} = \frac{I_{O1(MAX)} + I_{O2(MAX)}}{2}$$

This equation also makes the worst-case assumption that both converters are operating at 50% duty cycle and are synchronized. Since the converters are not synchronized and are not both operating at 50% duty cycle, the actual RMS current will always be less than this. Losses associated with the input ceramic capacitor are typically minimal.

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations. It is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2512. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize the stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C3 and C8) can be seen in the evaluation board layout in Figure 4. Since decoupling must be as close to the input pins as possible, it is necessary to use two decoupling capacitors. C3 provides the bulk capacitance required for both converters, while C8 is a high frequency bypass capacitor for the second channel (see C3 and C8 placement in Figure 4).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low ESR ceramic input capacitor, can create a high Q network that may affect converter performance.

This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short printed circuit board trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect converter performance, a high ESR tantalum or aluminum electrolytic capacitor should be placed in parallel with the low ESR, ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current the ceramic output capacitor alone supplies the load current until the loop responds. As the loop responds, the inductor current increases to match the load current demand. This typically takes two to three switching cycles and can be estimated by:

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = D \cdot (1 - D) = 0.5^2 = 0.25$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot spot temperature.

Adjustable Output Resistor Selection

For applications requiring an adjustable output voltage, the 0.6V version can be programmed externally. Resistors R1 through R4 of Figure 2 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string, the minimum suggested value for R2 and R4 is 59kΩ. Although a larger value will reduce the quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R2 and R4 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}}$$

The adjustable version of the AAT2512 in combination with an external feedforward capacitor (C4 and C5 of Figure 2) delivers enhanced transient response for extreme pulsed load applications. The addition of the feedforward capacitor typically requires a larger output capacitor (C1 and C2) for stability.

V_{OUT} (V)	R2, R4 = 59kΩ R1, R3 (kΩ)	R2, R4 = 221kΩ R1, R3
0.8	19.6	75K
0.9	29.4	113K
1.0	39.2	150K
1.1	49.9	187K
1.2	59.0	221K
1.3	68.1	261K
1.4	78.7	301K
1.5	88.7	332K
1.8	118	442K
1.85	124	464K
2.0	137	523K
2.5	187	715K
3.3	267	1.00M

Table 2: Adjustable Resistor Values For Use With 0.6V Version.

Thermal Calculations

There are three types of losses associated with the AAT2512 converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the dual converter losses is given by:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

I_Q is the AAT2512 quiescent current for one channel and t_{sw} is used to estimate the full load switching losses.

For the condition where channel one is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(LS)} \cdot [V_{IN} - V_{O1}])}{V_{IN}}$$

$$+ \frac{I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot [V_{IN} - V_{O2}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot [I_{O1} + I_{O2}] + 2 \cdot I_Q) \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN33-12 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \bullet \Theta_{JA} + T_{AMB}$$

PCB Layout

The following guidelines should be used to insure a proper layout.

1. Due to the pin placement of V_{IN} for both converters, proper decoupling is not possible with just one input capacitor. The large input capacitor C3 should connect as closely as possible to V_P and GND, as shown in Figure 4. The additional input bypass capacitor C8 is necessary for proper high frequency decoupling of the second converter.
2. The output capacitor and inductor should be connected as closely as possible. The connection of the inductor to the LX pin should also be as short as possible.
3. The feedback trace should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin. This prevents noise from being coupled into the high impedance feedback node.
4. The resistance of the trace from the load return to GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2mm grid.

Design Example

Specifications

V_{O1} = 2.5V @ 400mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 300mA
V_{O2} = 1.8V @ 400mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 300mA
V_{IN} = 2.7V to 4.2V (3.6V nominal)
F_S = 1.4 MHz
T_{AMB} = 85°C

2.5V V_{O1} Output Inductor

$$L1 = 3\frac{\mu sec}{A} \cdot V_{O1} = 3\frac{\mu sec}{A} \cdot 2.5V = 7.5\mu H \text{ (see Table 1)}$$

For Sumida inductor CDRH3D16, 10µH, DCR = 210mΩ.

$$\Delta I1 = \frac{V_O}{L1 \cdot F} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{2.5V}{10\mu H \cdot 1.4MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 72.3mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I1}{2} = 0.4A + 0.036A = 0.44A$$

$$P_{L1} = I_{O1}^2 \cdot DCR = 0.4A^2 \cdot 210m\Omega = 34mW$$

1.8V V_{O2} Output Inductor

$$L2 = 3\frac{\mu sec}{A} \cdot V_{O2} = 3\frac{\mu sec}{A} \cdot 1.8V = 5.4\mu H \text{ (see Table 1)}$$

For Sumida inductor CDRH3D16, 4.7µH, DCR = 105mΩ.

$$\Delta I2 = \frac{V_{O2}}{L \cdot F} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right) = \frac{1.8V}{4.7\mu H \cdot 1.4MHz} \cdot \left(1 - \frac{1.8V}{4.2V}\right) = 156mA$$

$$I_{PK2} = I_{O2} + \frac{\Delta I2}{2} = 0.4A + 0.078A = 0.48A$$

$$P_{L2} = I_{O2}^2 \cdot DCR = 0.4A^2 \cdot 105m\Omega = 17mW$$

2.5V Output Capacitor

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.3A}{0.2V \cdot 1.4MHz} = 3.2\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{2.5V \cdot (4.2V - 2.5V)}{10\mu H \cdot 1.4MHz \cdot 4.2V} = 21mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (21mA)^2 = 2.2\mu W$$

1.8V Output Capacitor

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.3A}{0.2V \cdot 1.4MHz} = 3.2\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{4.7\mu H \cdot 1.4MHz \cdot 4.2V} = 45mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (45mA)^2 = 10\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25mV.

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \bullet 4 \bullet F_S} = \frac{1}{\left(\frac{25mV}{0.8A} - 5m\Omega\right) \bullet 4 \bullet 1.4MHz} = 6.8\mu F$$

$$I_{RMS(MAX)} = \frac{I_{O1} + I_{O2}}{2} = 0.4Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.4A)^2 = 0.8mW$$

AAT2512 Losses

The maximum dissipation occurs at dropout where V_{IN} = 2.7V. All values assume an ambient temperature of 85°C and a junction temperature of 120°C.

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(LS)} \cdot (V_{IN} - V_{O1})) + I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot (V_{IN} - V_{O2}))}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_{O2} + 2 \cdot I_Q) \cdot V_{IN}$$

$$= \frac{0.4^2 \cdot (0.725\Omega \cdot 2.5V + 0.7\Omega \cdot (2.7V - 2.5V)) + 0.4^2 \cdot (0.725\Omega \cdot 1.8V + 0.7\Omega \cdot (2.7V - 1.8V))}{2.7V}$$

$$+ 5ns \cdot 1.4MHz \cdot 0.4A + 60\mu A) \cdot 2.7V = 239mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \bullet P_{LOSS} = 85°C + (50°C/W) \bullet 239mW = 97°C$$

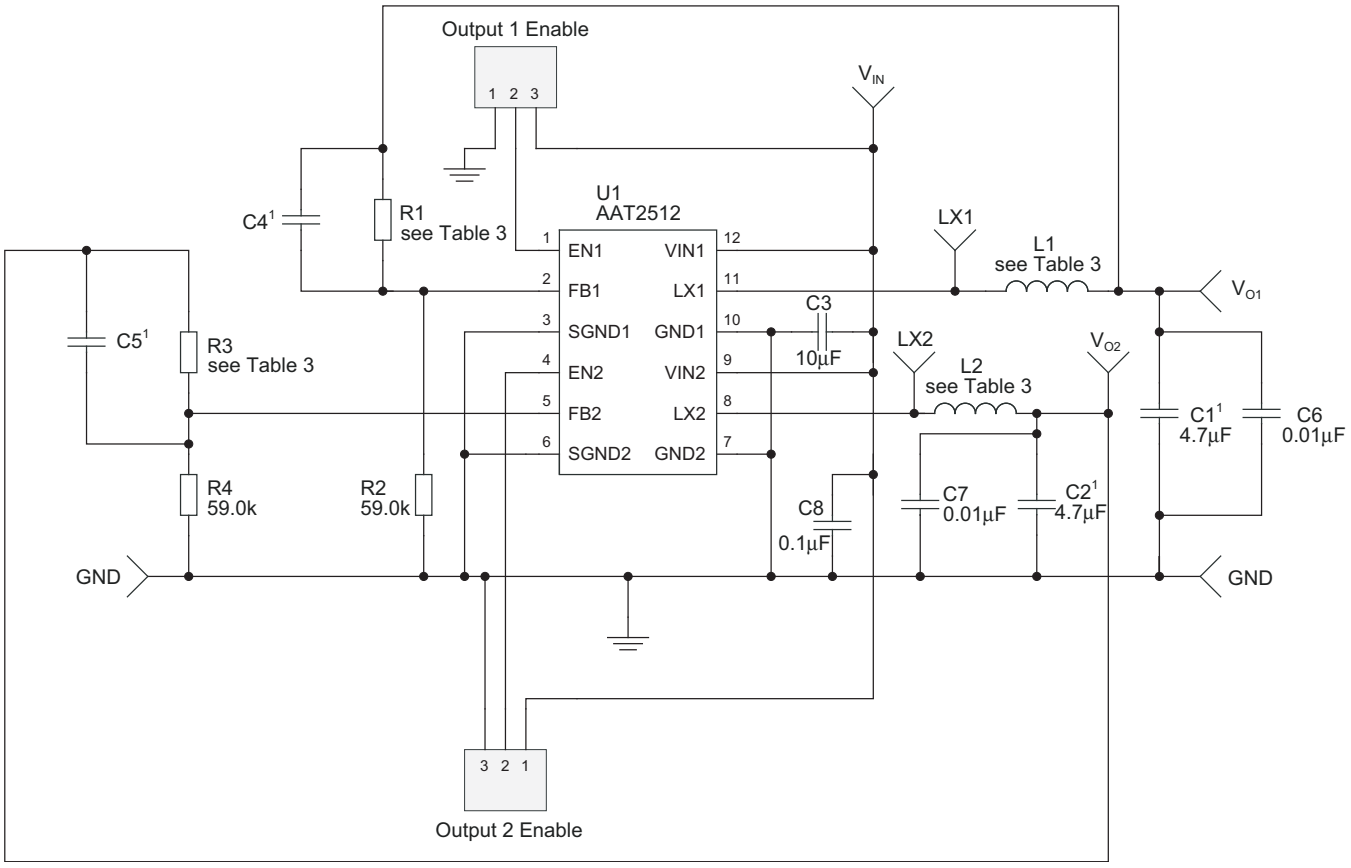


Figure 3: AAT2512 Evaluation Board Schematic.

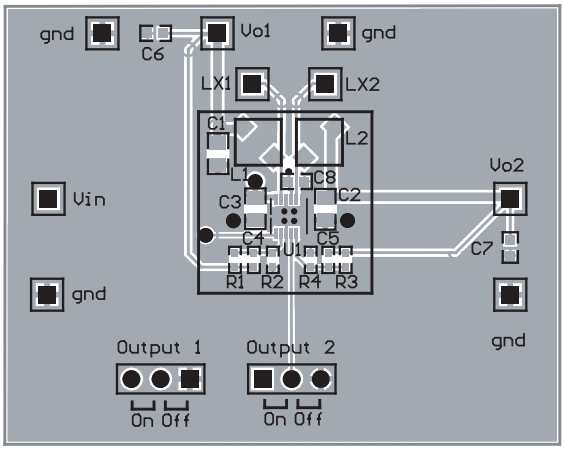


Figure 4: AAT2512 Evaluation Board Top Side.

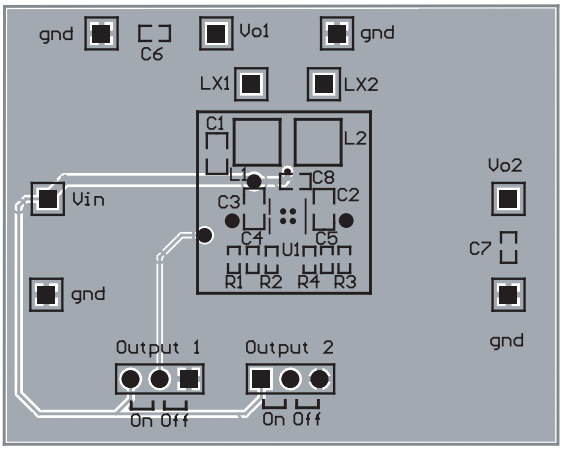


Figure 5: AAT2512 Evaluation Board Bottom Side.

1. For enhanced transient configuration C5, C4 = 100pF and C1, C2 = 10µF.

Adjustable Version (0.6V device)	R2, R4 = 59kΩ	R2, R4 = 221kΩ[1]	
V_{OUT} (V)	R1, R3 (kΩ)	R1, R3 (kΩ)	L1, L2 (µH)
0.8	19.6	75.0	2.2
0.9	29.4	113	2.2
1.0	39.2	150	2.2
1.1	49.9	187	2.2
1.2	59.0	221	2.2
1.3	68.1	261	2.2
1.4	78.7	301	4.7
1.5	88.7	332	4.7
1.8	118	442	4.7
1.85	124	464	4.7
2.0	137	523	6.8
2.5	187	715	6.8
3.3	267	1000	6.8
Fixed Version	**R2, R4 Not Used**		
V_{OUT} (V)	R1, R3 (kΩ)		L1, L2 (µH)
0.6-3.3V	0		4.7

Table 3: Evaluation Board Component Values.

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH3D16-2R2	2.2	1.20	0.072	3.8x3.8x1.8	Shielded
Sumida	CDRH3D16-4R7	4.7	0.90	0.105	3.8x3.8x1.8	Shielded
Sumida	CDRH3D16-6R8	6.8	0.73	0.170	3.8x3.8x1.8	Shielded
Murata	LQH2MCN4R7M02	4.7	0.40	0.80	2.0x1.6x0.95	Non-Shielded
Murata	LQH32CN4R7M23	4.7	0.45	0.20	2.5x3.2x2.0	Non-Shielded
Coilcraft	LPO3310-472	4.7	0.80	0.27	3.2x3.2x1.0	1mm
Coiltronics	SD3118-4R7	4.7	0.98	0.122	3.1x3.1x1.85	Shielded
Coiltronics	SD3118-6R8	6.8	0.82	0.175	3.1x3.1x1.85	Shielded
Coiltronics	SDRC10-4R7	4.7	1.30	0.122	5.7x4.4x1.0	1mm Shielded

Table 4: Typical Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
Murata	GRM219R61A475KE19	4.7µF	10V	X5R	0805
Murata	GRM21BR60J106KE19	10uF	6.3V	X5R	0805
Murata	GRM21BR60J226ME39	22uF	6.3V	X5R	0805

Table 5: Surface Mount Capacitors.

1. For reduced quiescent current, R2 and R4 = 221kΩ.

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2		
TDFN33-12	0.6V	0.6V	QKXYY	**AAT2512IWP-AA-T1**

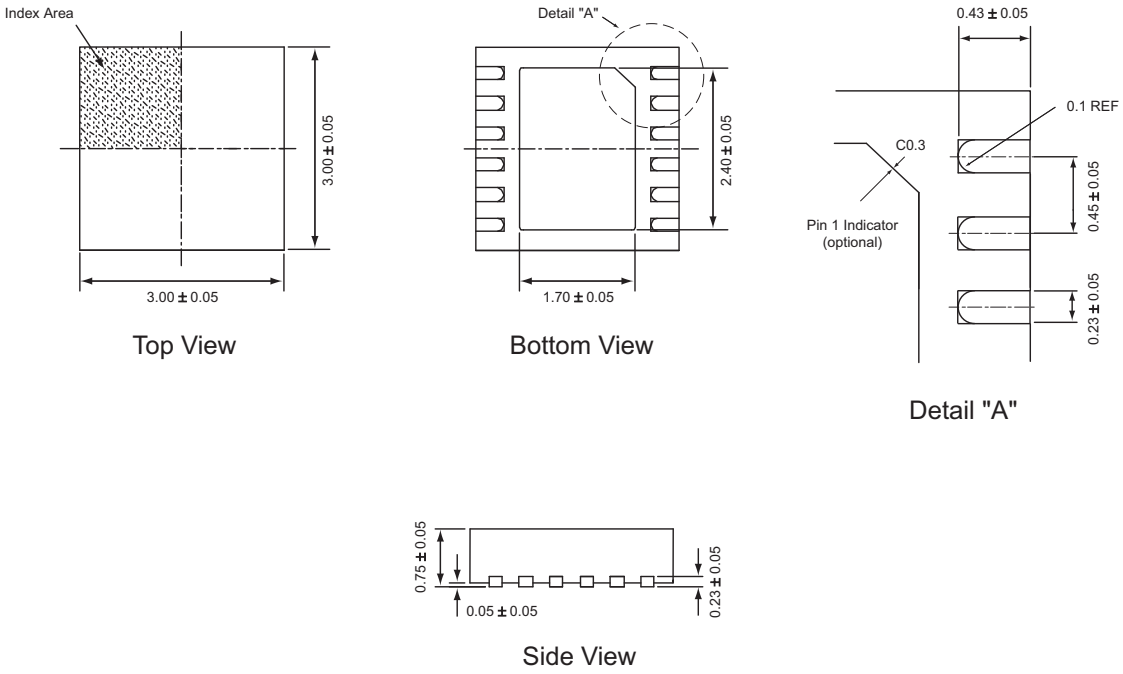
Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Legend	
Voltage	**Code**
Adjustable (0.6V)	A
0.9	B
1.2	E
1.5	G
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W
4.2	C

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information

TDFN33-12[1]



All dimensions in millimeters.

1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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