HMC612LP4 / 612LP4E

v01.0108

75 dB LOGARITHMIC DETECTOR / CONTROLLER, 50 Hz - 3000 MHz

Typical Applications

The HMC612LP4(E) is ideal for IF and RF applications in:

- Cellular/PCS/3G
- WiMAX, WiBro, WLAN, Fixed Wireless & Radar
- Power Monitoring & Control Circuitry
- Receiver Signal Strength Indication (RSSI)
- Automatic Gain & Power Control

Features

Wide Input Bandwidth: 50 Hz to 3 GHz

Wide Dynamic Range: Up to 74 dB

High Accuracy: ±1 dB with 60 dB Range Up to 0.9 GHz

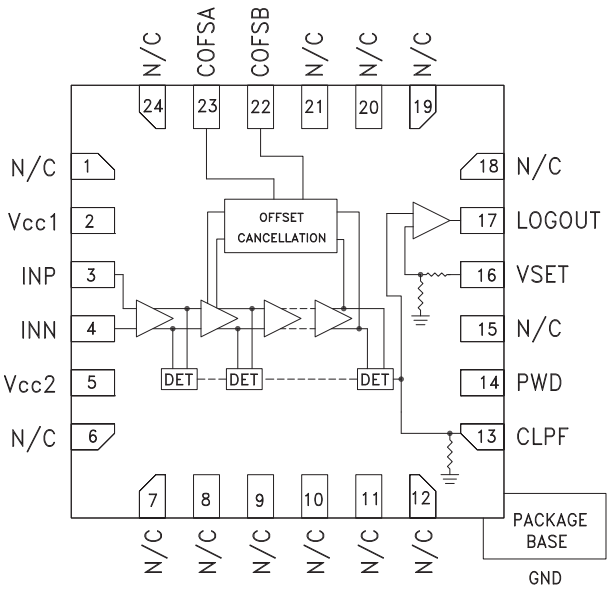
Supply Voltage: +2.7V to +5.5V

Excellent Stability over Temperature

Power-Down Mode

Compact 4x4mm Leadless SMT Package

Functional Diagram



General Description

The HMC612LP4(E) Logarithmic Detector/Controller is ideal for converting input signals with frequencies in the 50 Hz to 3 GHz range, to a proportional DC voltage at its output. The HMC612LP4(E) employs a successive compression technology which delivers extremely high dynamic range and conversion accuracy over a wide input frequency range. As the input signal is increased, successive amplifiers move into saturation one by one creating an accurate approximation of the logarithm function. The output of a series of square law detectors is summed, converted into voltage domain and buffered to drive the LOGOUT output. For detection mode, the LOGOUT pin is shorted to the VSET input and will provide a nominal logarithmic slope of 19 mV/dB and an intercept of -99 dBm. The HMC612LP4(E) can also be used in the controller mode where an external voltage is applied to the VSET pin, to create an AGC or APC feedback loop.

Electrical Specifications, T_A = +25C[1]

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	0.00005	0.0001	0.001	0.01	0.1	1	10	100	900	1900	2500	3000	MHz
±3 dB Dynamic Range	75	75	75	75	74	74	74	74	72	64	60	55	dB
±3 dB Dynamic Range Center						-30	-30	-30	-31	-33	-34	-34	dBm
±3 dB Dynamic Range Center	-45	-44.5	-45.5	-45	-45								dBV
±1 dB Dynamic Range	68	67	68	67	65	68	66	66	64	55	52	45	dB
Output Slope	19.7	19.7	19.6	19.6	19.8	19.7	19.8	19.8	19.4	19.4	19.8	20.8	mV/dB
Output Intercept						-94.5	-93.9	-93.8	-94.8	-92.5	-91.3	-86.4	dBm
Output Intercept	-110	-110.2	-110.6	-110.6	-110.0								dBV
Temperature Sensitivity @ -43 dBV Input [2]	-9.9	-11.9	-11.3	-11.3	-11.3								mdBV/°C
Temperature Sensitivity @ -30 dBm Input [2]						-12.5	-12.2	-11.7	-11.2	-11.7	-12.1	-13.4	mdBm/°C

[1] Detector mode measurements; LOGOUT (Pin 17) is shorted to VSET (Pin 18).

[2] Measured from T_A = -45C to T_A = +85C, Vdd1, Vdd2 = 5V

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Application Support: Phone: 1-800-ANALOG-D

Electrical Specifications, (continued)

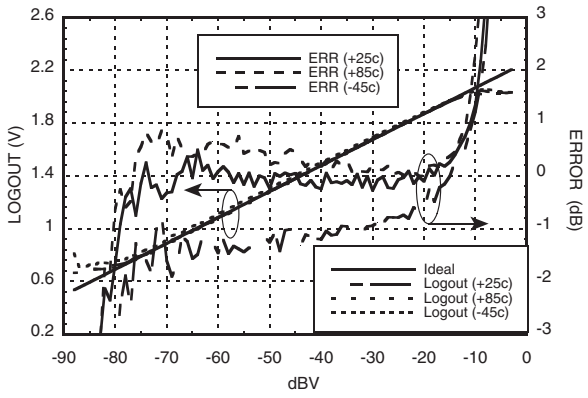
Parameter	Conditions	Min.	Typ.	Max.	Units
LOGOUT Interface					
Output Voltage Range		0		Vcc - 0.15	V
Output Rise Time/Fall Time @ -15 dBm	From 0% to 90%		19/100		ns
VSET Interface					
Input Impedance			30		kΩ
Input Voltage Range			0.6 to 1.9		V
Power Down (EN) Interface					
Voltage Range for Normal Mode		0		0.2 x Vcc	V
Voltage Range for Powerdown Mode		0.8 x Vcc		Vcc	V
Threshold Voltage			Vcc /2		V
Power Supply (Vcc1, Vcc2)					
Operating Voltage Range		2.7		5.5	V
Supply Current in Normal Mode			30		mA
Supply Current in Power Down Mode			1		mA

[1] Vdd1 = Vdd2 = 5V

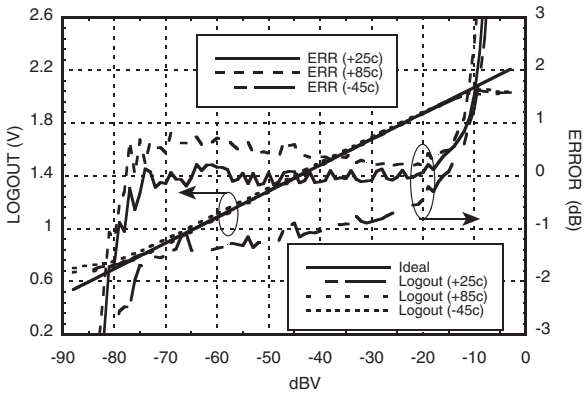
Test Conditions

Parameter	Condition
Vdd1 = Vdd2	+5V
Input Zo - w/ 68 Ω Term Resistor at IN+	50 Ω
T_A	+25 C
Fin	900 MHz
IN- Port connected to ground through a 10 µF capacitor	

LOGOUT Voltage & Error vs. Input Signal, Fin = 50 Hz



LOGOUT Voltage & Error vs. Input Signal, Fin = 100 Hz



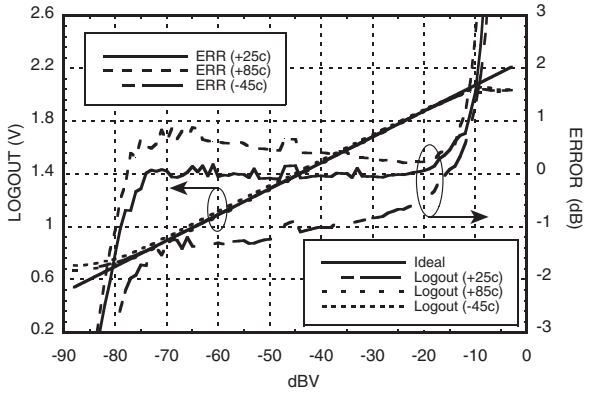
Vdd1 = Vdd2 = 5V

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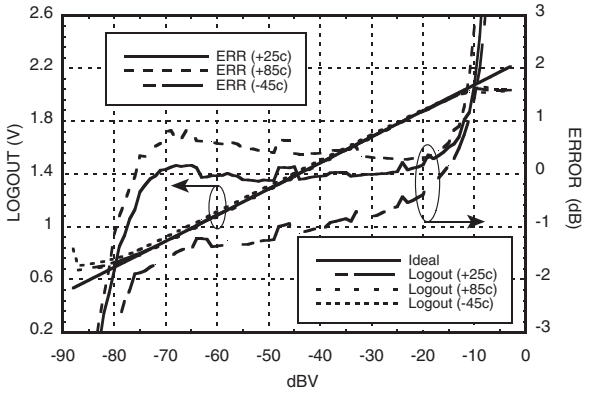
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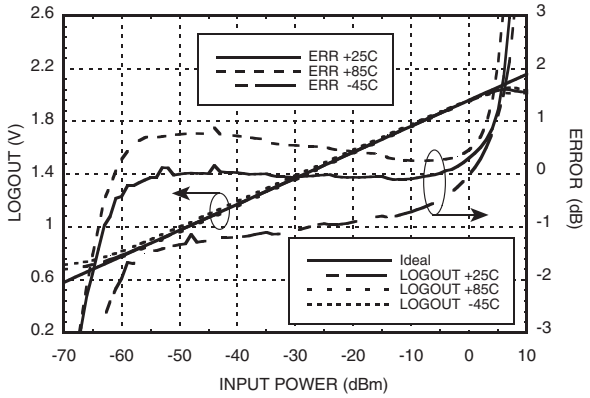
LOGOUT Voltage & Error vs. Input Signal, Fin = 1 kHz



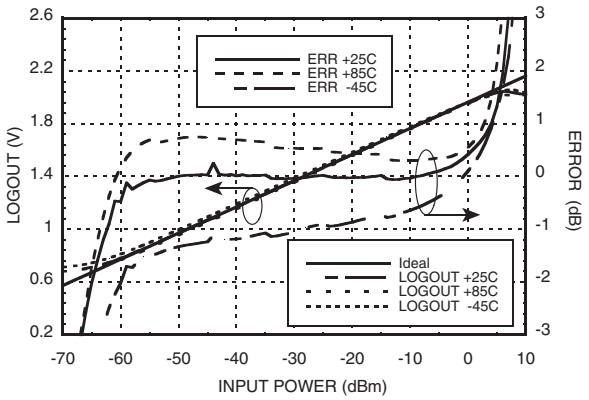
LOGOUT Voltage & Error vs. Input Signal, Fin = 100 kHz



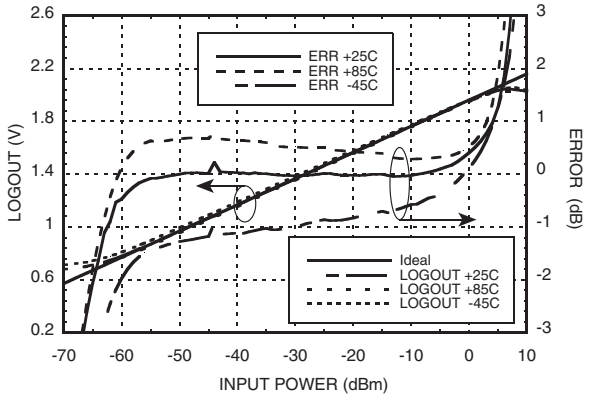
LOGOUT Voltage & Error vs. Input Power, Fin = 1 MHz



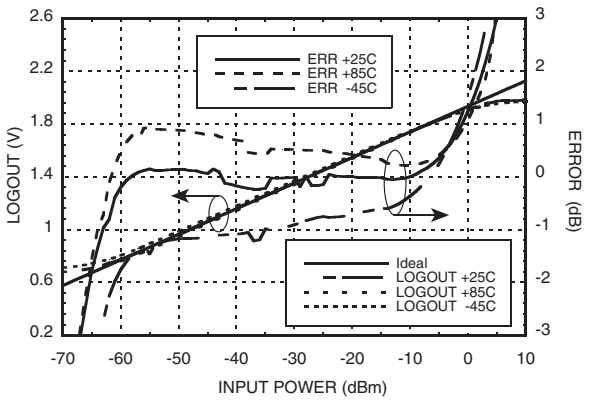
LOGOUT Voltage & Error vs. Input Power, Fin = 10 MHz



LOGOUT Voltage & Error vs. Input Power, Fin = 100 MHz



LOGOUT Voltage & Error vs. Input Power, Fin = 900 MHz



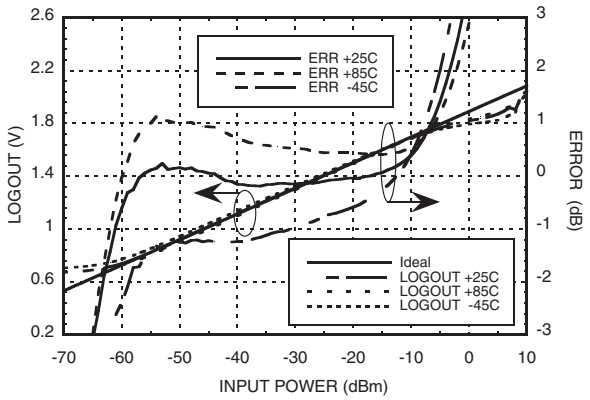
Vdd1 = Vdd2 = 5V

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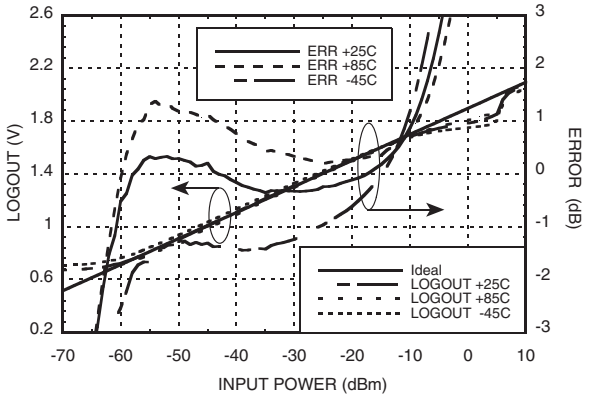
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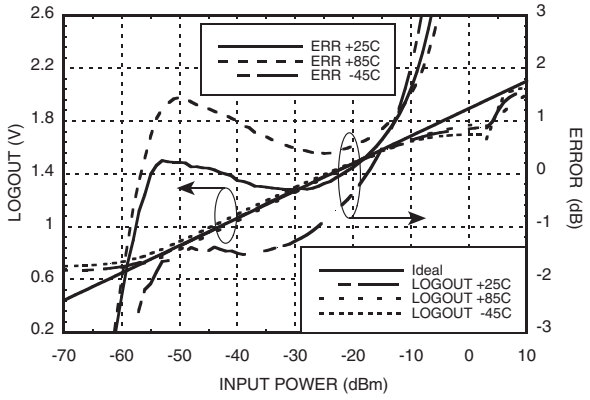
LOGOUT Voltage & Error vs. Input Power, Fin = 1900 MHz



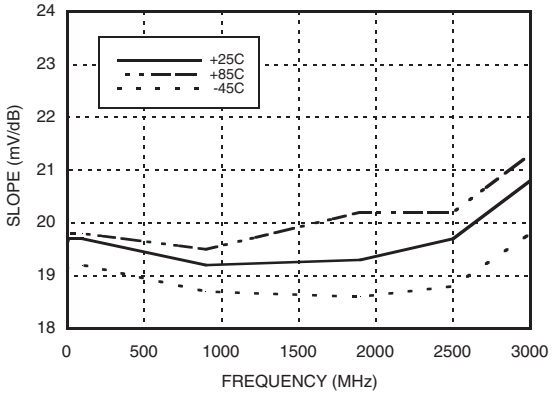
LOGOUT Voltage & Error vs. Input Power, Fin = 2500 MHz



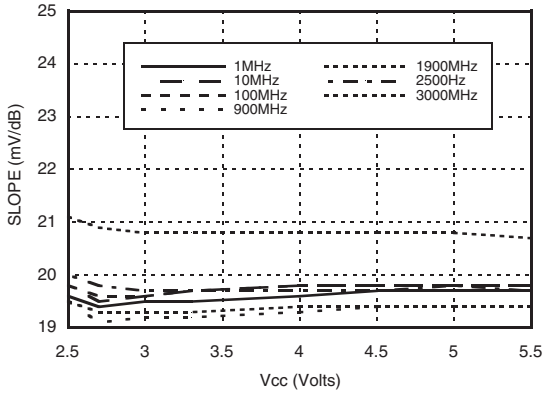
LOGOUT Voltage & Error vs. Input Power, Fin = 3000 MHz



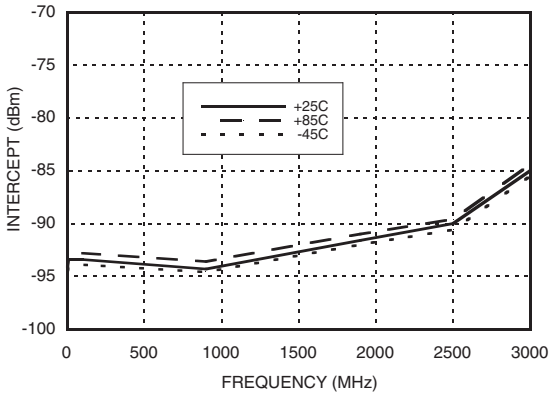
LOGOUT Slope vs. Frequency, Vcc= 3.3V



LOGOUT Slope vs. Supply Voltage, T_A= +25C



LOGOUT Intercept vs. Frequency, Vcc= 3.3V



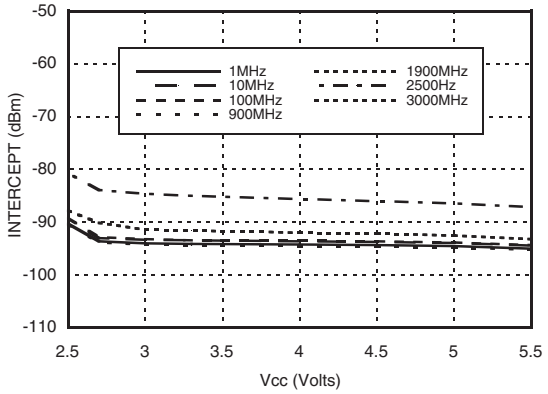
Vdd1 = Vdd2 = 5V

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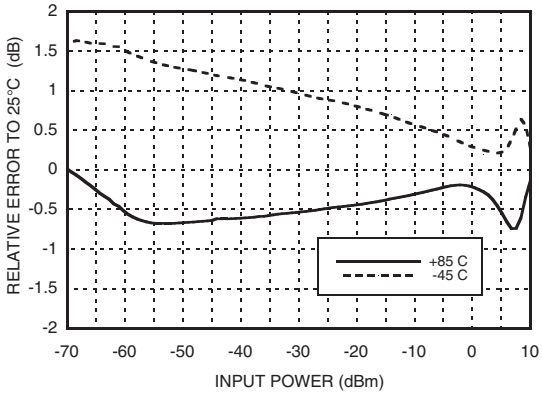
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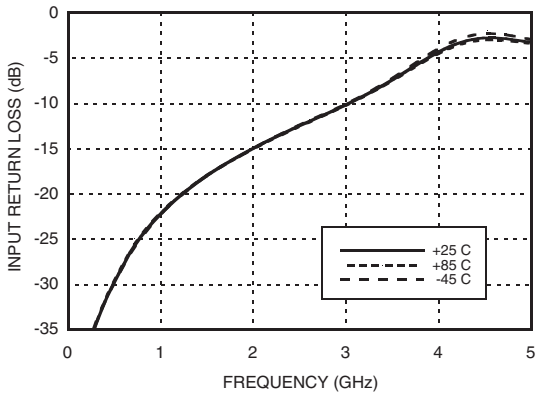
LOGOUT Intercept vs. Supply Voltage, T_A= +25C



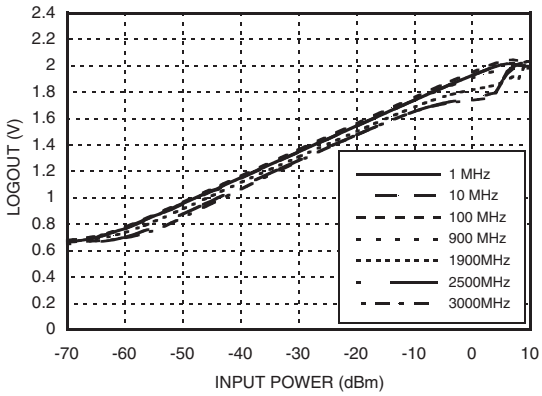
LOGOUT Error vs. Input Power, Normalized, Fin= 100 MHz [1]



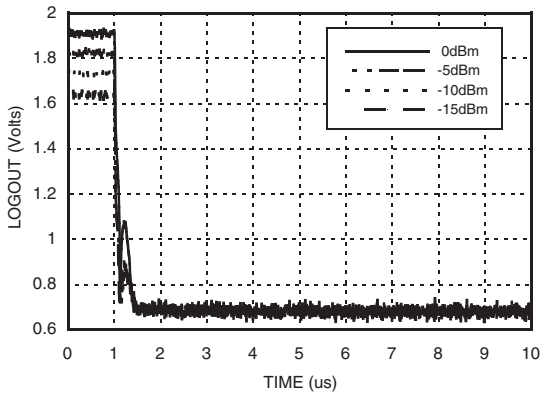
Input Return Loss vs. Frequency, Vcc= 3.3V



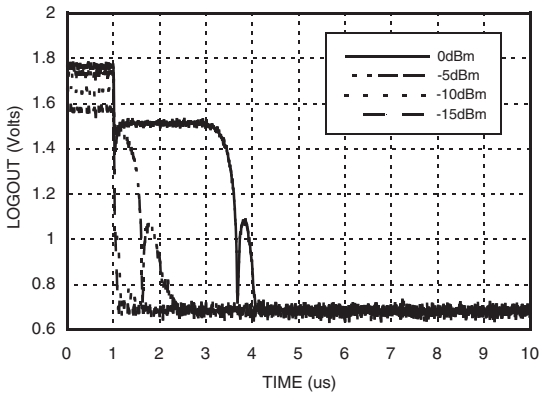
LOGOUT Voltage vs. Input Power & Frequency



Fall Time @ 600 MHz Over Power Level



Fall Time @ 2400 MHz Over Power Level [2]



[1] This data is relative to the room temperature performance of the HMC612LP4(E)

[2] Intermediate step up to 4 µs on falling-edge when operated beyond linear dynamic range.

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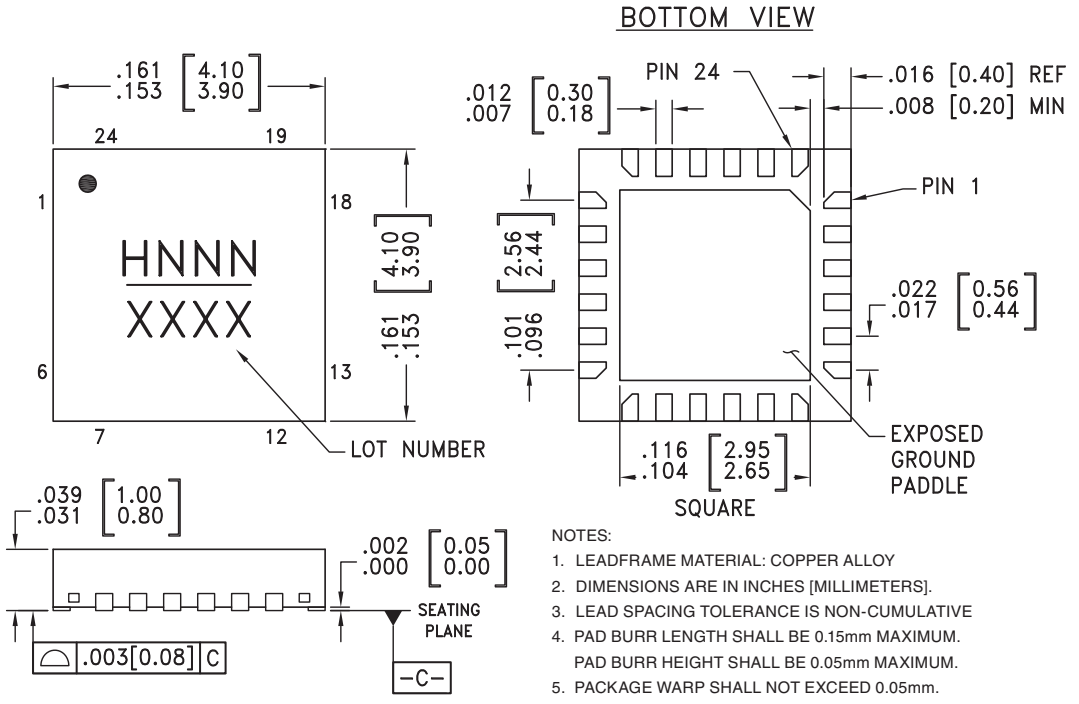
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Absolute Maximum Ratings

Vcc1, Vcc2	0V to +5.5V
PWD	0V to +5.5V
VSET Input Voltage	0V to +5.5V
LOGOUT Output Current	3 mA
RF Input Power	+10 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 7.95 mW/°C above 85°C)	0.32 Watts
Thermal Resistance (R_{th}) (junction to package base)	126 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-45 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

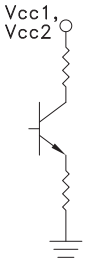
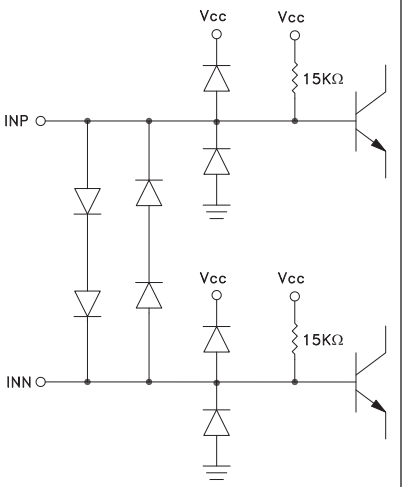
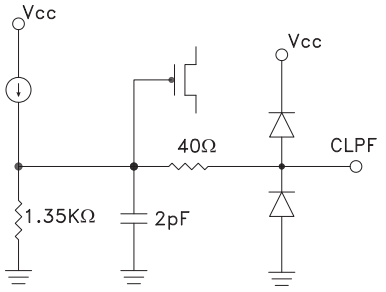
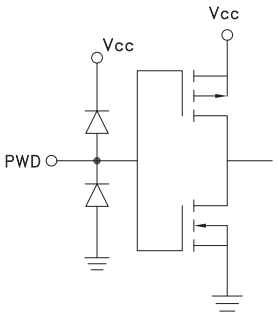
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC612LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H612 XXXX
HMC612LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H612 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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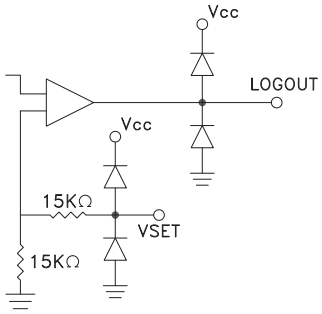
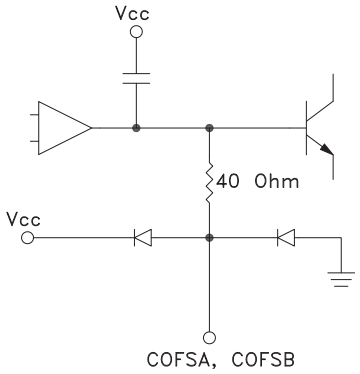
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 7 - 12, 15, 18 - 21	N/C	These pins are not connected internally; however, this product is specified with these pins connected to RF/DC ground.	
2, 5	Vcc1, Vcc2	Bias supply. Connect supply voltage to both pins.	
3, 4	INP, INN	RF Input pins. Connect RF to INP, and AC couple INN to ground for single-ended operation.	
13	CLPF	Loop filter capacitor for output ripple filtering.	
14	PWD	Connect to 0V for normal operation. Applying voltage >0.8 x Vcc will initiate a power saving shutdown mode.	

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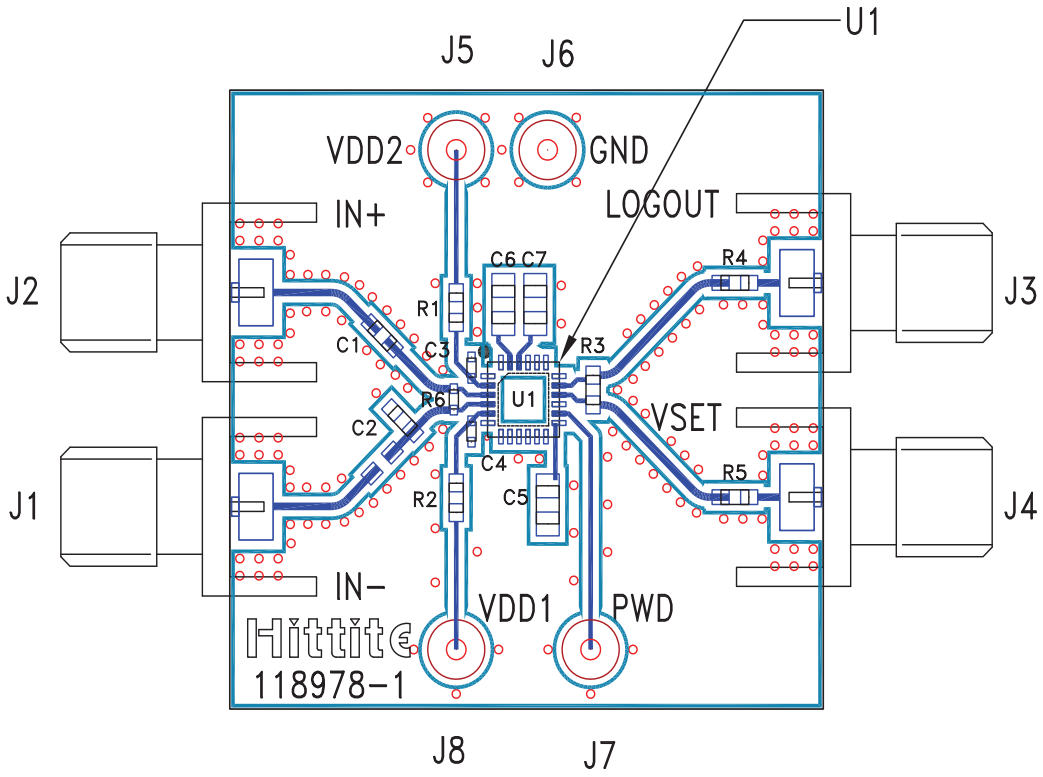
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
16	VSET	VSET input in controller mode. Short this pin to LOGOUT for detector mode.	
17	LOGOUT	Logarithmic output that converts the input power to a DC level in detector mode. Short this pin to VSET for detector mode.	
22, 23	COFSB, COFSA	External capacitor should be connected to these pins to reduce system high pass corner frequency for RF signal detection. Large capacitor is required for detecting low frequency signals.	
Package Base	GND	Exposed paddle must be connected to RF and DC ground.	

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Evaluation PCB



List of Materials for Evaluation PCB 118980 [1]

Item	Description
J1 - J4	PC Mount SMA Connector
J5 - J8	DC Pin
C1, C2	10 µF Capacitor, 0603 Pkg.
C3, C4	0.1 µF Capacitor, 0402 Pkg.
C5, C6, C7	47 µF Capacitor, 0805 Pkg.
R1, R2	6.8Ω Resistor, 0603 Pkg.
R3, R4, R5	0Ω Resistor, 0603 Pkg.
R6	49.9Ω Resistor, 0402 Pkg.
U1	HMC612LP4 / HMC612LP4E Logarithmic Detector / Controller
PCB [2]	118978 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

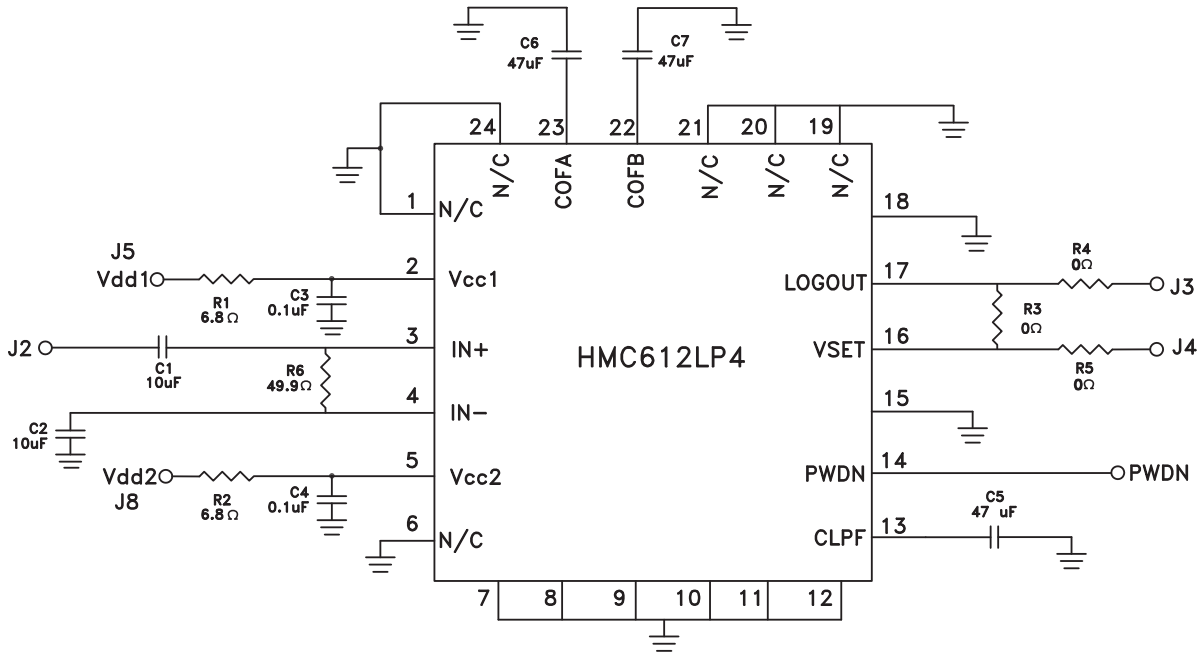
[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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Application & Evaluation PCB Schematic



Notes

Note 1: The HMC612LP4 & HMC612LP4E evaluation boards are pre-assembled for single-ended input, and detector/RSSI mode.

Note 2: For detector mode, connect high impedance volt meter to the LOGOUT port. VSET is shorted to LOGOUT by R3, as required for detector mode.

Note 3: For low frequency operation remove R6.

Note 4: Faster rise/fall time remove C6, C7 and C5

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