PCA9530

2-bit I²C-bus LED dimmer

Rev. 03 — 26 February 2009 Product data sheet

1. General description

The PCA9530 is a 2-bit I²C-bus and SMBus I/O expander optimized for dimming LEDs in 256 discrete steps for Red/Green/Blue (RGB) color mixing and backlight applications.

The PCA9530 contains an internal oscillator with two user programmable blink rates and duty cycles coupled to the output PWM. The LED brightness is controlled by setting the blink rate high enough (> 100 Hz) that the blinking cannot be seen and then using the duty cycle to vary the amount of time the LED is on and thus the average current through the LED.

The initial setup sequence programs the two blink rates/duty cycles for each individual PWM. From then on, only one command from the bus master is required to turn individual LEDs ON, OFF, BLINK RATE 1 or BLINK RATE 2. Based on the programmed frequency and duty cycle, BLINK RATE 1 and BLINK RATE 2 will cause the LEDs to appear at a different brightness or blink at periods up to 1.69 second. The open-drain outputs directly drive the LEDs with maximum output sink current of 25 mA per bit and 50 mA per package.

To blink LEDs at periods greater than 1.69 second, the bus master (MCU, MPU, DSP, chip set, etc.) must send repeated commands to turn the LED on and off as is currently done when using normal I/O Expanders like the NXP Semiconductors PCF8574 or PCA9554. Any bits not used for controlling the LEDs can be used for General Purpose parallel Input/Output (GPIO) expansion which provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, alarm monitoring, fans, etc.

The active LOW hardware reset pin ($\overline{\text{RESET}}$) and Power-On Reset (POR) initialize the registers to their default state causing the bits to be set HIGH (LED off).

One hardware address pin on the PCA9530 allows two devices to operate on the same bus.

2. Features

- 2 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.591 Hz and 152 Hz (1.69 seconds and 6.58 milliseconds)
- 256 brightness steps
- Input/output not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C-bus interface logic compatible with SMBus
- Internal power-on reset

founded by Philips

- Noise filter on SCL/SDA inputs
- Active LOW reset input ($\overline{\text{RESET}}$)
- 2 open-drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

3. Ordering information

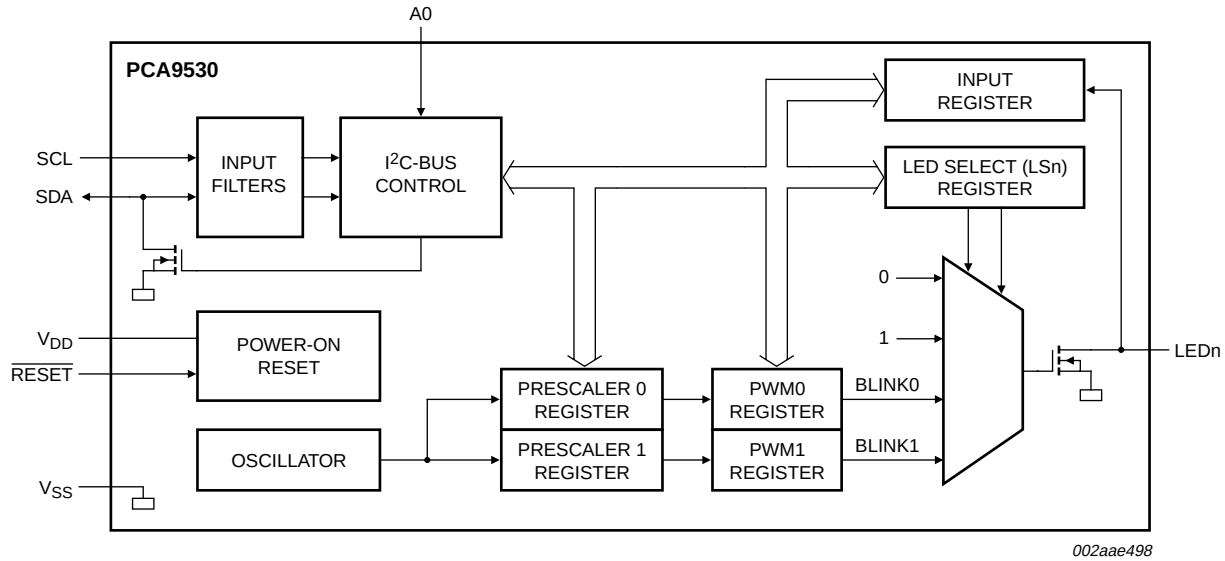
Table 1. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA9530D	PCA9530	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9530DP	9530	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] Also known as MSOP8.

4. Block diagram



Remark: Only one I/O shown for clarity.

Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

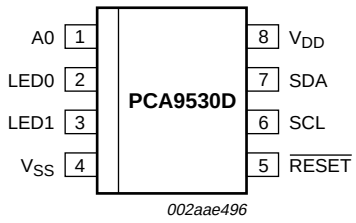


Fig 2. Pin configuration for SO8

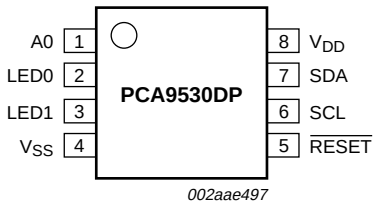


Fig 3. Pin configuration for TSSOP8 (MSOP8)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input 0
LED0	2	LED driver 0
LED1	3	LED driver 1
V_{SS}	4	supply ground
$\overline{RESET}$	5	active LOW reset input
SCL	6	serial clock line
SDA	7	serial data line
V_{DD}	8	supply voltage

6. Functional description

Refer to Figure 1 “Block diagram”.

6.1 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9530 is shown in Figure 4. To conserve power, no internal pull-up resistor is incorporated on the hardware selectable address pin and it must be pulled HIGH or LOW.

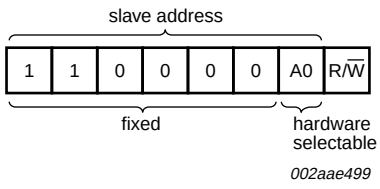


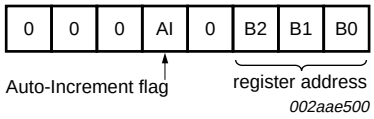
Fig 4. Slave address

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The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9530, which will be stored in the Control register.



Reset state: 00h

Fig 5. Control register

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the Auto-Increment flag is set, the three low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '000' after the last register is accessed.

When Auto-Increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from the Input register (B2 B1 B0 ≠ 0 0 0).

Only the 3 least significant bits are affected by the AI flag. Unused bits must be programmed with zeroes.

6.2.1 Control register definition

Table 3. Register summary

B2	B1	B0	Symbol	Access	Description
0	0	0	INPUT	read only	input register
0	0	1	PSC0	read/write	frequency prescaler 0
0	1	0	PWM0	read/write	PWM register 0
0	1	1	PSC1	read/write	frequency prescaler 1
1	0	0	PWM1	read/write	PWM register 1
1	0	1	LS0	read/write	LED selector

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6.3 Register descriptions

6.3.1 INPUT - Input register

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

Table 4. INPUT - Input register description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	LED1	LED0
Default	0	0	0	0	0	0	X	X

Remark: The default value 'X' is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to V_{DD}.

6.3.2 PCS0 - Frequency Prescaler 0

PSC0 is used to program the period of the PWM output.

The period of BLINK0 = (PSC0 + 1) / 152.

Table 5. PSC0 - Frequency Prescaler 0 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PSC0[7]	PSC0[6]	PSC0[5]	PSC0[4]	PSC0[3]	PSC0[2]	PSC0[1]	PSC0[0]
Default	0	0	0	0	0	0	0	0

6.3.3 PWM0 - Pulse Width Modulation 0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always HIGH (LED off).

The duty cycle of BLINK0 = PWM0 / 256.

Table 6. PWM0 - Pulse Width Modulation 0 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PWM0 [7]	PWM0 [6]	PWM0 [5]	PWM0 [4]	PWM0 [3]	PWM0 [2]	PWM0 [1]	PWM0 [0]
Default	1	0	0	0	0	0	0	0

6.3.4 PCS1 - Frequency Prescaler 1

PSC1 is used to program the period of the PWM output.

The period of BLINK1 = (PSC1 + 1) / 152.

Table 7. PSC1 - Frequency Prescaler 1 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PSC1[7]	PSC1[6]	PSC1[5]	PSC1[4]	PSC1[3]	PSC1[2]	PSC1[1]	PSC1[0]
Default	0	0	0	0	0	0	0	0

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6.3.5 PWM1 - Pulse Width Modulation 1

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always HIGH (LED off).

The duty cycle of BLINK1 = PWM1 / 256.

Table 8. PWM1 - Pulse Width Modulation 1 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PWM1 [7]	PWM1 [6]	PWM1 [5]	PWM1 [4]	PWM1 [3]	PWM1 [2]	PWM1 [1]	PWM1 [0]
Default	1	0	0	0	0	0	0	0

6.3.6 LS0 - LED selector

The LS0 LED select register determines the source of the LED data.

00 = output is set high-impedance (LED off; default)

01 = output is set LOW (LED on)

10 = output blinks at PWM0 rate

11 = output blinks at PWM1 rate

Table 9. LS0 - LED selector register bit description

*Legend: * default value.*

Register	Bit	Value	Description
LS0	7:4	1111*	reserved
	3:2	00*	LED1 selected
	1:0	00*	LED0 selected

6.4 Pins used as GPIOs

LEDn pins not used to control LEDs can be used as General Purpose I/Os (GPIOs).

For use as input, set LEDn to high-impedance (00) and then read the pin state via the INPUT register.

For use as output, connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LEDn output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the ‘LED selector’ register LS0. The output can be pulse-width controlled when PWM0 or PWM1 are used.

6.5 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9530 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9530 registers are initialized to their default states, all the outputs in the OFF state. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

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6.6 External $\overline{\text{RESET}}$

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9530 registers and I²C-bus state machine will be held in their default states until the $\overline{\text{RESET}}$ input is once again HIGH.

This input requires a pull-up resistor to V_{DD} if no active connection is used.

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

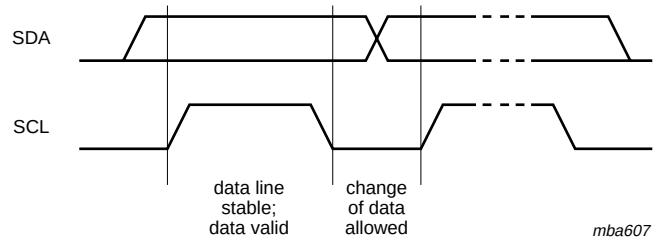


Fig 6. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 7).

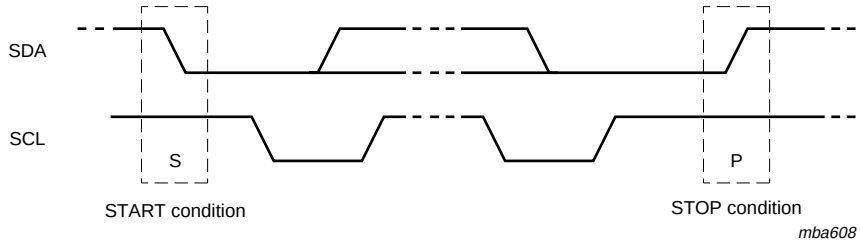


Fig 7. Definition of START and STOP conditions

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7.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 8).

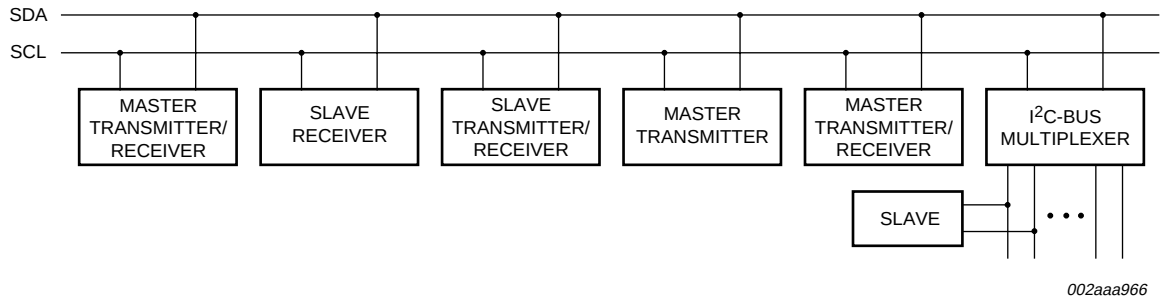


Fig 8. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

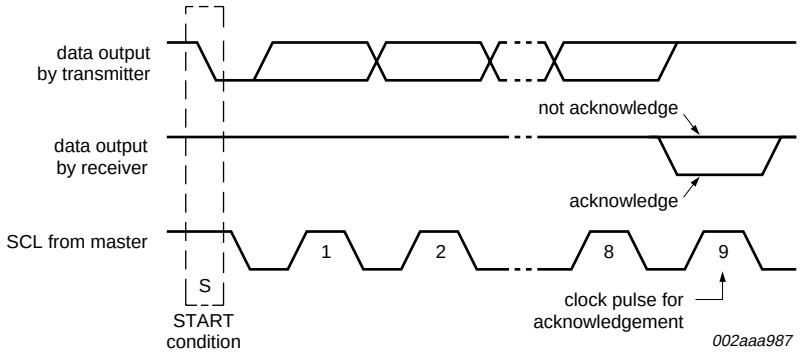


Fig 9. Acknowledgement on the I²C-bus

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7.4 Bus transactions

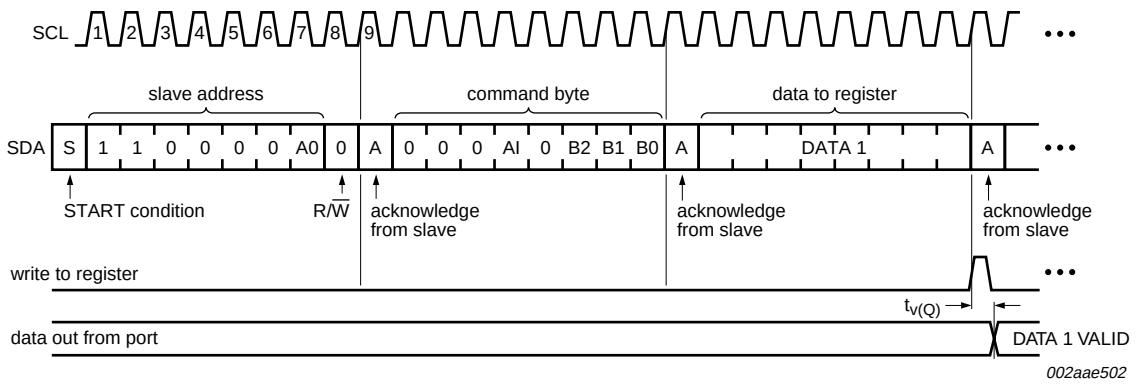


Fig 10. Write to register

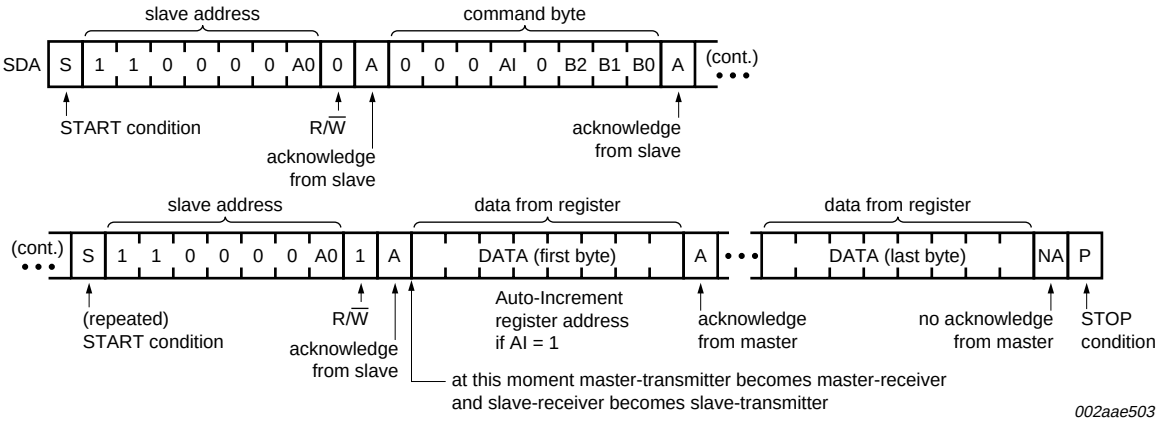
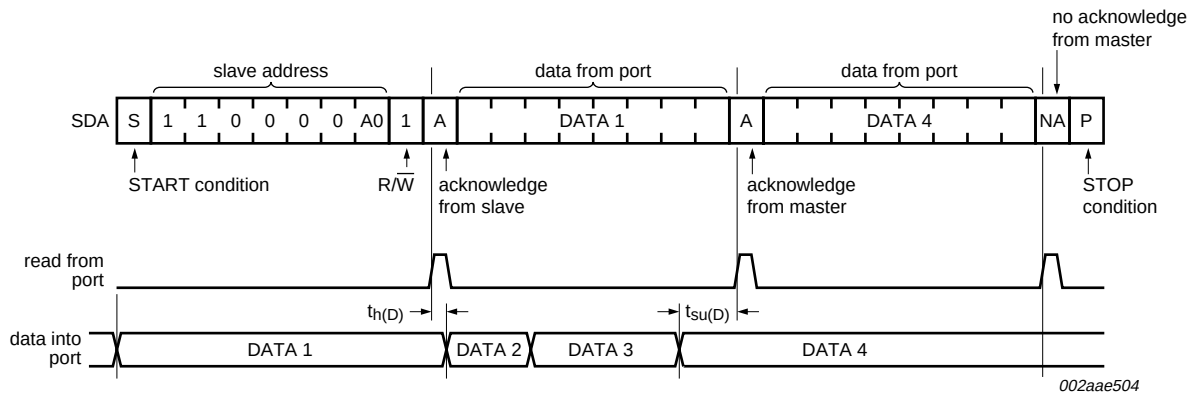


Fig 11. Read from register



Remark: This figure assumes the command byte has previously been programmed with 00h.

Fig 12. Read Input port register

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8. Application design-in information

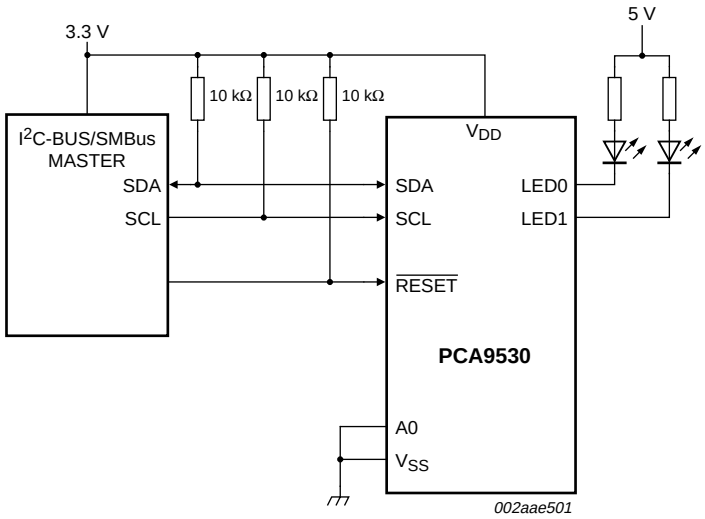


Fig 13. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD} and is specified as ΔI_{DD} in Table 12 “Static characteristics”.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevent additional supply current consumption when the LED is off.

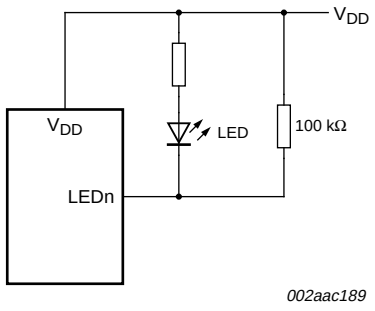


Fig 14. High value resistor in parallel with the LED

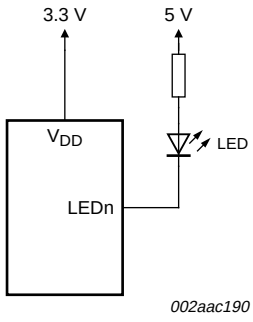


Fig 15. Device supplied by a lower voltage

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8.2 Programming example

The following example will show how to set LED0 to blink at 1 Hz at a 50 % duty cycle. LED1 will be set to be dimmed at 25 % of their maximum brightness (duty cycle = 25 %).

Table 10. Programming PCA9530

Program sequence	I²C-bus
START	S
PCA9530 address with A0 = LOW	C0h
PSC0 subaddress + Auto-Increment	11h
Set prescaler PSC0 to achieve a period of 1 second: $Blink\ period = 1 = \frac{PSC0 + 1}{152}$ PSC0 = 151	97h
Set PWM0 duty cycle to 50 %: $\frac{PWM0}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PCS1 to dim at maximum frequency: $Blink\ period = max$ PSC1 = 0	00h
Set PWM1 output duty cycle to 25 %: $\frac{PWM1}{256} = 0.25$ PWM1 = 64	40h
Set LED0 to PWM0, and set LED1 to blink at PWM1	0Eh
STOP	P

9. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} – 0.5	5.5	V
$I_{O(LEDn)}$	output current on pin LEDn		-	+25	mA
I_{SS}	ground supply current		-	50	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

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10. Static characteristics

Table 12. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		-	350	500	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz		-	1.9	5.0	µA
ΔI_{DD}	additional quiescent supply current	Standby mode; V_{DD} = 5.5 V; every LED I/O at V_I = 4.3 V; f_{SCL} = 0 kHz	[2]	-	-	200	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[3]	-	1.7	2.2	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	6.5	-	mA
I_L	leakage current	V_I = V_{DD} = V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	3.7	5	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V					
		V_{DD} = 2.3 V	[4]	9	-	-	mA
		V_{DD} = 3.0 V	[4]	12	-	-	mA
		V_{DD} = 5.0 V	[4]	15	-	-	mA
		V_{OL} = 0.7 V					
		V_{DD} = 2.3 V	[4]	15	-	-	mA
		V_{DD} = 3.0 V	[4]	20	-	-	mA
		V_{DD} = 5.0 V	[4]	25	-	-	mA
I_L	input leakage current	V_{DD} = 3.6 V; V_I = 0 V or V_{DD}		−1	-	+1	µA
C_{io}	input/output capacitance			-	2.1	5	pF
Select inputs A0, $\overline{\text{RESET}}$							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	2.3	5	pF

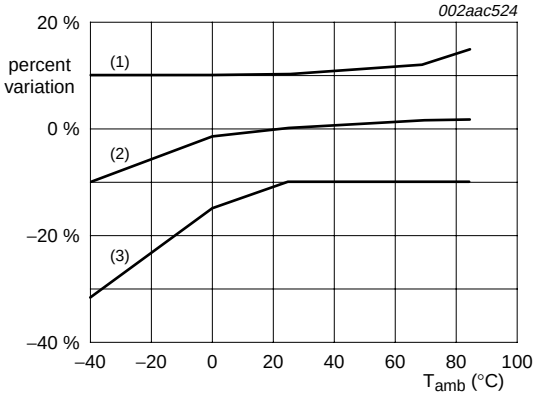
[1] Typical limits at V_{DD} = 3.3 V, T_{amb} = 25 °C.

[2] Additional current for one LED I/O at a time where V_I = 4.3 V,

[3] V_{DD} must be lowered to 0.2 V in order to reset part.

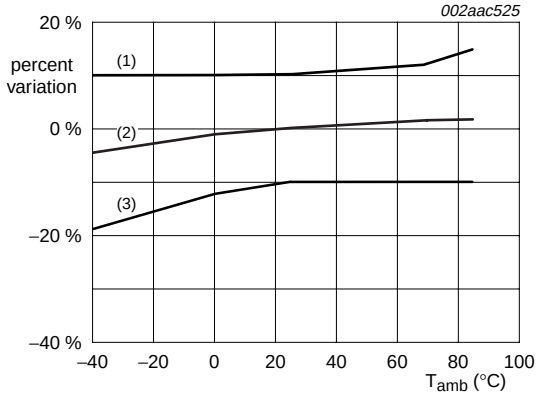
[4] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 50 mA.

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(1) maximum
(2) average
(3) minimum

Fig 16. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V



(1) maximum
(2) average
(3) minimum

Fig 17. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

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11. Dynamic characteristics

Table 13. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time		[1]	-	600	-	600	ns
$t_{VD;DAT}$	data valid time	LOW-level	[2]	-	600	-	600	ns
		HIGH-level	[2]	-	1500	-	600	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$ [3]	300	ns
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
$t_{v(Q)}$	data output valid time			-	200	-	200	ns
$t_{su(D)}$	data input set-up time			100	-	100	-	ns
$t_{h(D)}$	data input hold time			1	-	1	-	µs
Reset								
$t_{w(rst)}$	reset pulse width			6	-	6	-	ns
$t_{rec(rst)}$	reset recovery time			0	-	0	-	ns
t_{rst}	reset time		[4][5]	400	-	400	-	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data output to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

[4] Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.

[5] Upon reset, the full delay will be the sum of t_{rst} and the RC time constant of the SDA bus.

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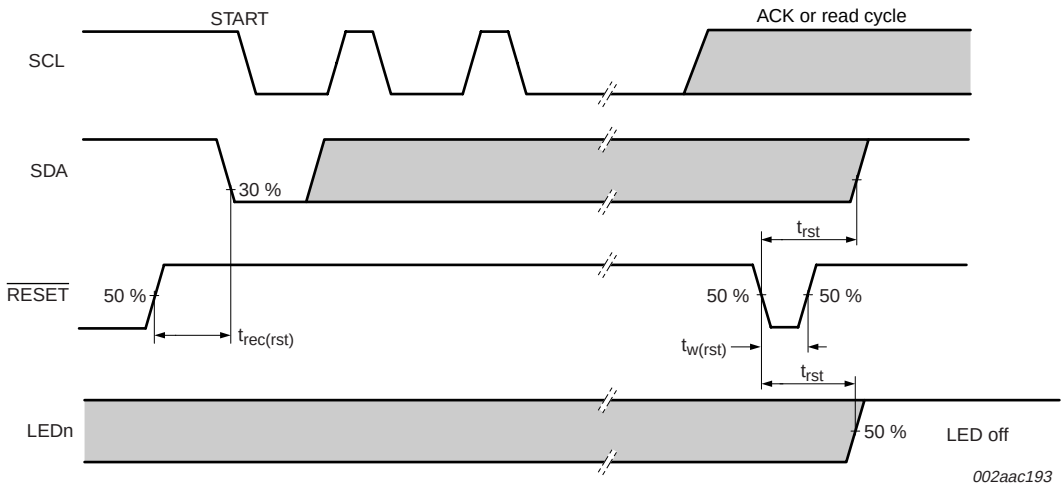


Fig 18. Definition of $\overline{\text{RESET}}$ timing

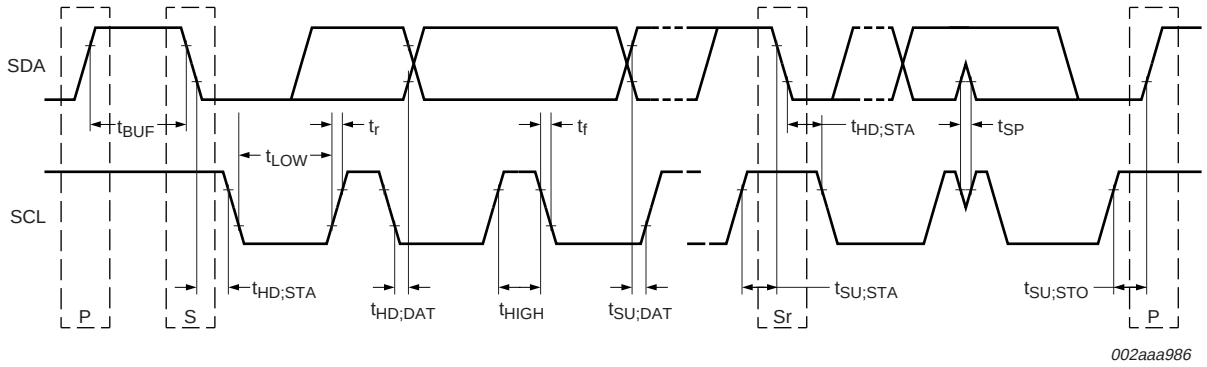
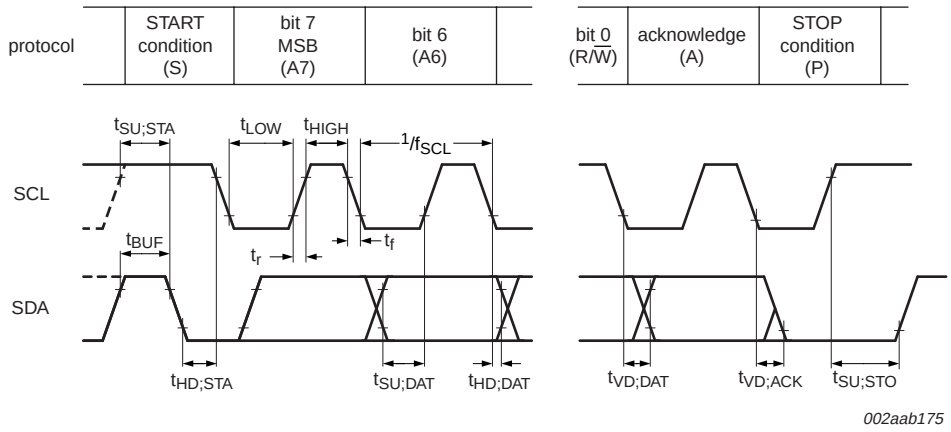


Fig 19. Definition of timing

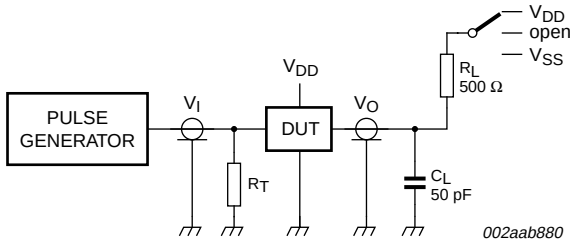
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Rise and fall times refer to V_{IL} and V_{IH}.

Fig 20. I²C-bus timing diagram

12. Test information



R_L = load resistor for LEDn. R_L for SDA and SCL > 1 kΩ (3 mA or less current).

C_L = load capacitance includes jig and probe capacitance.

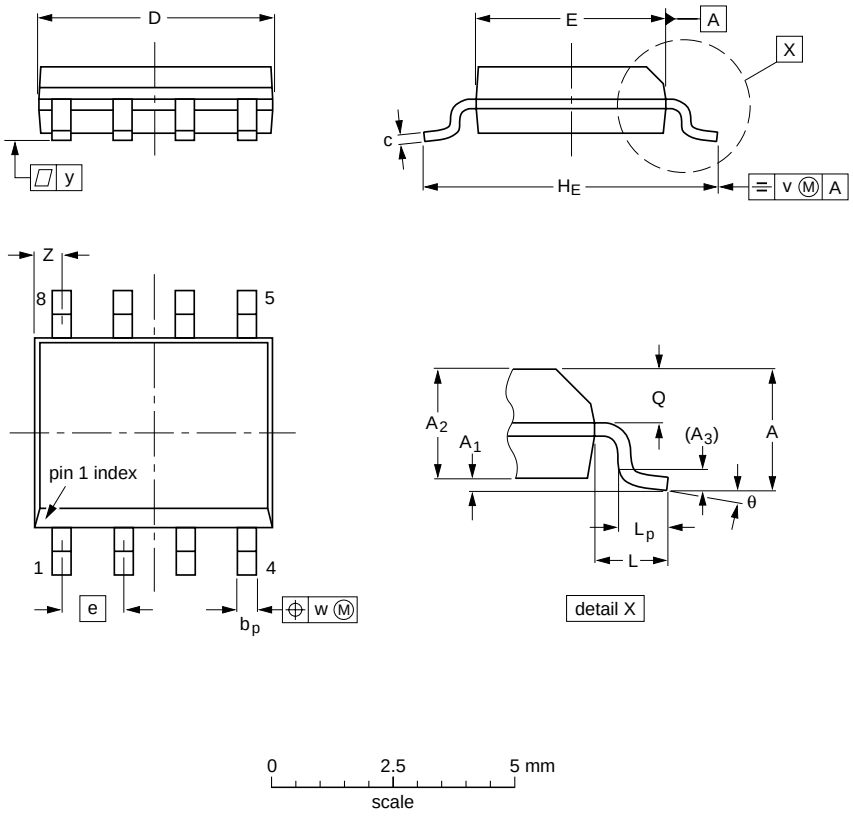
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 21. Test circuitry for switching times

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13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

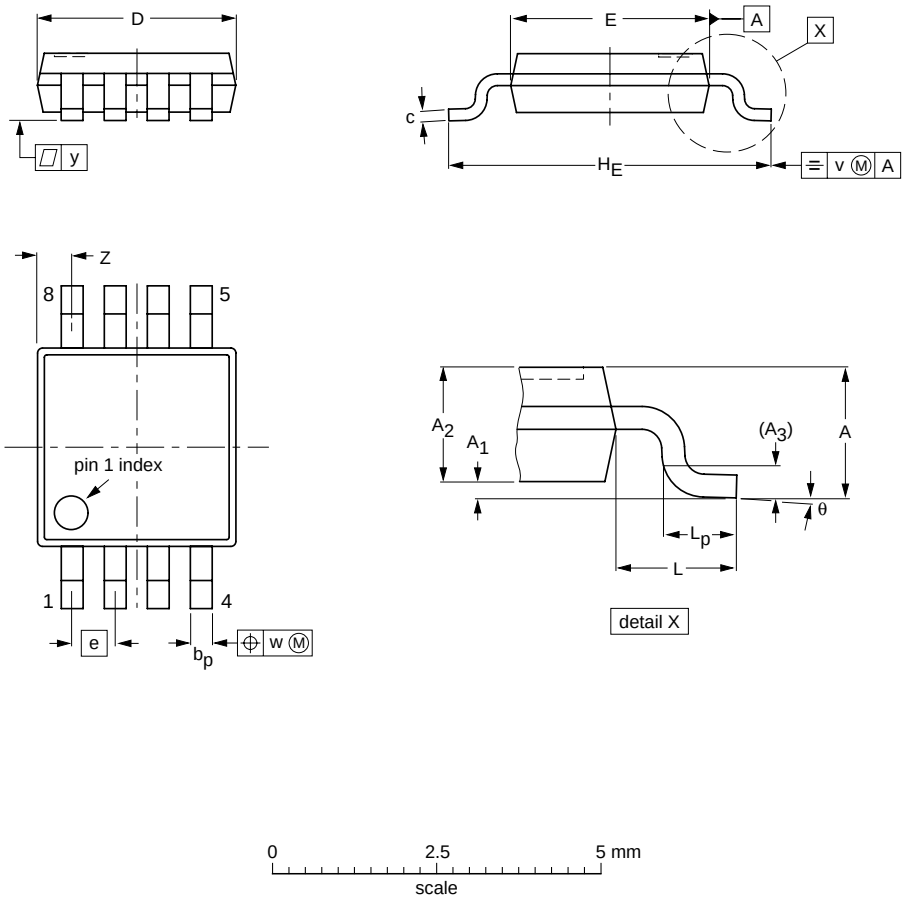
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 22. Package outline SOT96-1 (SO8)

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TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 23. Package outline SOT505-1 (TSSOP8)

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14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

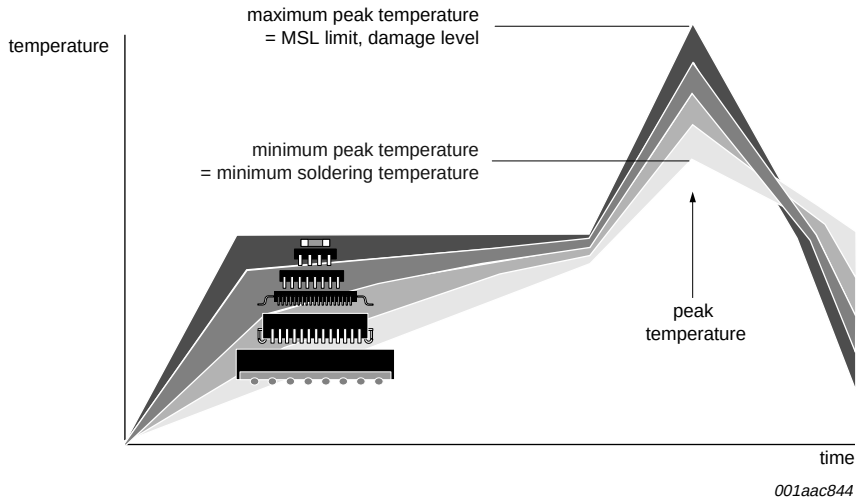
Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.

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MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 16. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CDM	Charged-Device Model
DSP	Digital Signal Processor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
MCU	MicroController Unit
MM	Machine Model
MPU	MicroProcessor Unit
POR	Power-On Reset
PWM	Pulse Width Modulator
RC	Resistor-Capacitor network
RGB	Red/Green/Blue
SMBus	System Management Bus

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17. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9530_3	20090226	Product data sheet	-	PCA9530_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 6.6 “External RESET”, 1st sentence: changed from “t_W” to “$t_{w(rst)}$” • Figure 10 “Write to register”: symbol changed from “t_{pv}” to “$t_{v(Q)}$” • Figure 11 “Read from register”: – symbol changed from “t_{ph}” to “$t_{h(D)}$” – symbol changed from “t_{ps}” to “$t_{su(D)}$” • Table 11 “Limiting values”: – parameter description for $V_{I/O}$ changed from “DC voltage on an I/O” to “voltage on an input/output pin” – symbol/parameter changed from “$I_{I/O}$, DC output current on an I/O” to “$I_{O(LEDn)}$, output current on pin LEDn” • Table 12 “Static characteristics”: – title of this table changed from “DC characteristics” to “Static characteristics” – descriptive line below table title: deleted “TYP at 3.3 V and 25 °C” (this is moved to new Table note [1], with its reference at column heading “Typ” – I_{stb} Max value changed from “3.0 µA” to “5.0 µA” – parameter description for symbol ΔI_{DD} changed from “additional standby current” to “additional quiescent standby current” – added (new) Table note [2], and its reference at ΔI_{DD} • Table 13 “Dynamic characteristics”: – changed parameter description for f_{SCL} from “operating frequency” to “SCL clock frequency” – (old) symbols “$t_{VD;DAT}$ (L)” and “$t_{VD;DAT}$ (H)” merged to “$t_{VD;DAT}$” and added separate conditions for LOW-level and HIGH-level – symbol/parameter changed from “t_{PV}, output data valid” to “$t_{v(Q)}$, data output valid time” – symbol/parameter changed from “t_{PS}, input data setup time” to “$t_{su(D)}$, data input set-up time” – symbol/parameter changed from “t_W, Reset pulse width” to “$t_{w(rst)}$, reset pulse width” – symbol/parameter changed from “t_{REC}, Reset recovery time” to “$t_{rec(rst)}$, reset recovery time” – symbol/parameter changed from “t_{RESET}, Time to reset” to “t_{rst}, reset time” • added soldering information • added Table 16 “Abbreviations”			
PCA9530_2 (9397 750 14093)	20041001	Product data sheet	-	PCA9530_1
PCA9530_1 (9397 750 13631)	20040914	Product data sheet	-	-

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18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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