UCC33410-Q1 Ultra-Small, 1.0W, 3.3V, 3kV$_{RMS}$ Isolation, Automotive DC/DC Module

1 Features

- 1.0W Maximum output power
- 4.5V to 5.5V input voltage operation range
- 3.3V, 3.7V regulated selectable output voltage
  - 3.3V: 300mA available load current
- 0.5% typical load regulation
- 2mV/V typical line regulation
- Robust isolation barrier:
  - Isolation rating: 3kV$_{RMS}$
  - Surge capability: 6.5kV$_{PK}$
  - Working voltage: 1159V$_{PK}$
  - 200V/ns common mode transient immunity
- Power dense isolated DC/DC module with integrated transformer technology
- Adaptive spread spectrum modulation (SSM)
- Meets CISPR32 Class B emission
- Strong magnetic fields immunity
- Overload and short circuit protection
- Thermal shutdown
- Low inrush current soft-start
- Enable pin with fault reporting mechanism
- Functional Safety-Capable
- Planned Safety-related certifications:
  - Basic isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 3kV$_{RMS}$ isolation for 1 minute per UL 1577
  - UL certification per IEC 62368-1, and IEC 60601-1 end equipment standards
  - CQC approval per GB4943.1-2022
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: –40°C to 125°C ambient operating temperature
- VSON-12 (4.0mm × 5.00mm) package

2 Applications

- Battery-Management Systems (BMS)
- HEV/EV OBC and DC/DC converter
- Isolated bias for isolated voltage and current sensors
- Isolated bias for digital isolators,
- Isolated bias for isolated RS-485, RS-422 and CAN transceivers

3 Description

UCC33410-Q1 is an automotive qualified DC/DC power module with integrated transformer technology designed to provide 1.0W of isolated output power. It can support an input voltage operation range of 4.5V to 5.5V and regulate 3.3V output voltage with a selectable headroom of 3.7V.

UCC33410-Q1 features a proprietary transformer architecture that achieves a 3kV$_{RMS}$ isolation rating, while simultaneously supporting low EMI and excellent load regulation.

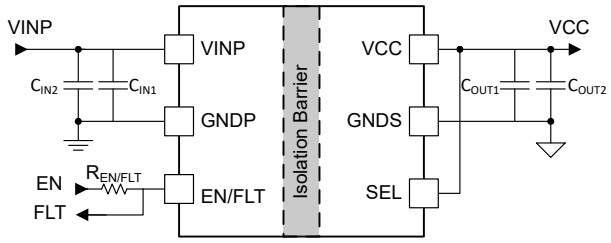
The UCC33410-Q1 integrates protection features for increased system robustness such as enable pin with fault reporting mechanism, short circuit protection and thermal shutdown.

The UCC33410-Q1 comes in a miniaturized, low-profile solution VSON (4.0mm × 5.00mm) package with 1.00mm height and > 4.1mm creepage and clearance

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC33410-Q1	VSON-FCRLF (12)	4.0mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Pin Configuration and Functions

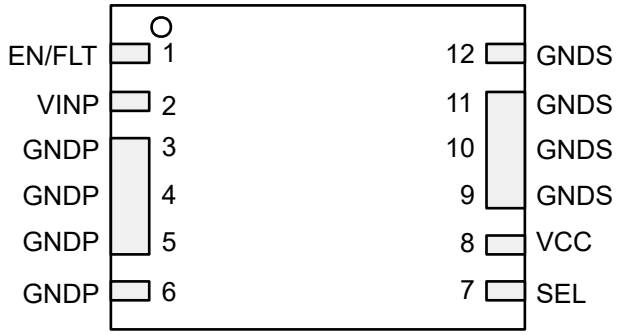


Figure 4-1. VSON-FCRLF12-pin Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
EN/FLT	1	I/O	Multi-function Enable input pin and fault output pin. Connect to microcontroller through an 18kΩ or greater pull-up resistor. Enable input pin: Forcing EN low disables the device. Pull high to enable normal device functionality. Fault output pin: This pin is pulled low for 200µs to alert that power converter is shutdown due to fault condition
VINP	2	P	Primary side input supply voltage pin. 2.2nF (C_{IN1}) and 22µF (C_{IN2}) ceramic bypass capacitors placed close to device pins are required between VINP and GNDP pins
GNDP	3	G	Power ground return connection for VINP.
	4		
	5		
	6		
SEL	7	I	VCC selection pin. VCC setpoint is 3.3V when SEL is connected to VCC, and 3.7V when SEL is shorted to GNDS
VCC	8	P	Isolated supply output voltage pin. 2.2nF (C_{OUT1}) and 22µF (C_{OUT2}) ceramic bypass capacitors placed close to device pins are required between VCC and GNDS pins
GNDS	9	G	Power ground return connection for VCC.
	10		
	11		
	12		

(1) P = Power, G = Ground, I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PIN	MIN	TYP	MAX	UNIT
VINP to GNDP(3)	–0.3		6	V
EN/FLT to GNDP	–0.3		6	V
VCC to GNDS (3)	–0.3		6	V
SEL to GNDS (3)	–0.3		6	V
Total VCC output power at T_A=25°C, $P_{OUT_VCC_MAX}$ (2)			1.1	W
Operating junction temperature range, T_J	–40		150	°C
Storage temperature, T_{stg}	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the VCC Load Recommended Operating Area section for maximum rated values across temperature and VINP conditions for different VCC output voltage settings.
(3) Less than 1ms. Extended time at this voltage can affect lifetime reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PIN		MIN	TYP	MAX	UNIT
V_{VINP}	Primary-side input voltage to GNDP	4.5		5.5	V
$V_{EN/FLT}$	EN/FLT pin voltage to GNDP	0		5.5	V
V_{VCC}	Secondary-side Isolated output voltage to GNDS	0		3.9	V
V_{SEL}	SEL pin input voltage to GNDS	0		3.9	V
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 3.3V, T_A=25°C - 85°C (1)		1		W
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 3.3V, T_A=105°C (1)		0.7		W
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 3.3V, T_A=125°C (1)		0.4		W
Static CMTI	Static Common mode transient immunity rating (dV/dt rate across the isolation barrier)			200	V/ns
Dynamic CMTI	Dynamic Common mode transient immunity rating (dV/dt rate across the isolation barrier)			200	V/ns
T_A	Ambient temperature	–40		125	℃
T_J	Junction temperature	–40		150	℃

(1) See the VCC Load Recommended Operating Area section for maximum rated values across temperature and VINP conditions for different VCC output voltage settings.

5.4 Thermal Information

THERMAL METRIC(1)		VSON-FCRLF 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	°C/W
Ψ_{JA}	Junction-to-ambient characterization parameter	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.2	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	> 4.1	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	> 4.1	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 50	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1159	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	820	V_{RMS}
		DC voltage	1159	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification)	4243	V_{PK}
		V_{TEST} = 1.2 × V_{IOTM} , t = 1s (100%) production	5091	V_{PK}
V_{IMP}	Impulse Voltage (3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1.	6500	V_{PK}
q_{pd}	Apparent charge (5)	Method a: After I/O safety test subgroup 2/3, Vini = V_{IOTM}, tini = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, Vini = V_{IOTM}, tini = 60s; $V_{pd(m)}$ = 1.3 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method b1: At routine test (100% production) and preconditioning (type test), Vini = 1.2 x V_{IOTM}, tini = 1s; $V_{pd(m)}$ = 1.5 × V_{IORM}, t_m = 1s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output (6)	V_{IO} = 0.4 sin (2πft), f = 1MHz	< 3	pF
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	Withstand isolation voltage V_{TEST} = V_{ISO} , t = 60s (qualification) V_{TEST} = 1.2 × V_{ISO} , t=1s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device

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5.6 Safety-Related Certifications

VDE	UL	UL	UL	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition program	Plan to certify according to IEC 62368-1	Plan to certify according to IEC 60601-1	Plan to certify according to GB4943.1-2022
Basic insulation Maximum transient isolation voltage, 4242V_{PK}; Maximum repetitive peak isolation voltage, 1159V_{PK}; Maximum surge isolation voltage, 6500V_{PK}	Single protection, 3000V_{RMS}	Basic insulation per UL 62368-1- 14 and IEC 62368-1 2nd Ed., 820V_{RMS} maximum working voltage (pollution degree 2, material group I)	Basic insulation per UL 60601- 1:14 and IEC 60601-1 d.3+A1,AAMI ES 60601- 1:2005/(R)2012 and A1:2012, C1:2009/(R)2012 and A2:2010/(R)2012 CSA C22.2 No. 60601-1:2014 IEC 60601-1:2012, 250V_{RMS} maximum working voltage, 1 MOPP (Means of patient protection)	Basic insulation , Altitude ≤ 5000m, Tropical Climate, 574V_{RMS} maximum working voltage
Certificate number: (planned)	Certificate number: (planned)	File number: (planned)	Certificate number: (planned)	Certificate number: (planned)

5.7 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, C_{IN1} = C_{OUT1} = 2.2nF, C_{IN2} = 10µF, C_{OUT2} = 22µF, SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
I_{VINP_Q}	VIN quiescent current,disabled	EN/FLT=Low, VINP=5.0V, no load			180	µA
I_{VINP_NL}	VIN operating current, no load	EN/FLT=High; VINP=4.5V-5.5V; VCC=3.3V no load		7	15	mA
		EN/FLT=High; VINP=4.5V-5.5V; VCC=3.7V no load		7	15	mA
I_{VINP_FL}	VIN operating current, full load	EN/FLT=High; VINP=5.0V; VCC=3.3V, I_{out}=300mA, T_A=25°C		400		mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VINP_UVLO_R}$	VINP under-voltage lockout rising threshold			2.8	2.9	V
$V_{VINP_UVLO_F}$	VINP under-voltage lockout falling threshold		2.6	2.7		V
V_{UVLO_H}	VINP under-voltage lockout hysteresis			0.1		V
OVLO COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VINP_OVLO_R}$	VINP over-voltage lockout rising threshold			5.77	5.9	V
$V_{VINP_OVLO_F}$	VINP over-voltage lockout falling threshold		5.55	5.72		V
V_{VINP_H}	VINP over-voltage lockout hysteresis			0.05		V
Switching Charactarestics						
f_{Sw}	DC-DC Converter switching frequency			76		MHz
PRIMARY SIDE THERMAL SHUTDOWN						
TSD_{P_R}	Primary-side over-temperature shutdown rising threshold		150	165		ºC
TSD_{P_F}	Primary-side over-temperature shutdown falling threshold		130			ºC
TSD_{P_H}	Primary-side over-temperature shutdown hysteresis			20		ºC

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Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, C_{IN1} = C_{OUT1} = 2.2nF, C_{IN2} = 10µF, C_{OUT2} = 22µF, SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN/FLT PIN						
V_{EN_R}	Enable voltage rising threshold	EN/FLT = 0V to 5.0V			2.1	V
V_{EN_F}	Enable voltage falling threshold	EN/FLT = 5.0V to 0V	0.8			V
I_{EN}	Enable pin input Current	EN/FLT = 5.0V			10	µA
V_{FLT}	EN/FLT pin voltage when faults occur	With a minimum 18kohm (10% tolerance) resistor connected to EN/FLT pin			0.5	V
t_{Fault}	EN/FLT pull down interval when faults occur	EN/FLT > 0.5V , Fault occur		200		µs
VCC OUTPUT VOLTAGE (Secondary-side. All voltages with respect to GNDS)						
V_{CC}	Isolated supply regulated output voltage	VINP = 5.0V; VCC = 3.3V, I_{out} = 0 - 300mA	3.2	3.3	3.4	V
		VINP = 5.0V; VCC = 3.7V, I_{out} = 0 - 270mA	3.59	3.7	3.81	V
	Isolated supply regulated output voltage accuracy	VINP = 4.5V - 5.5V; VCC = 3.3V / 3.7V	-4		4	%
V_{CC_Line}	V_{cc} DC line regulation	VINP = 4.5V - 5.5V; VCC = 3.3V, I_{out} = 150mA		2		mV/V
		VINP = 4.5V - 5.5V; VCC = 3.7V, I_{out} = 150mA		2		mV/V
V_{CC_Load}	V_{cc} DC load regulation	VINP = 5.0V; VCC = 3.3V, I_{out} = 0 - 303mA		0.5%		
		VINP = 5.0V; VCC = 3.7V, I_{out} = 0 - 270mA		0.5%		
V_{CC_Ripple}	Voltage ripple on isolated supply output	20-MHz bandwidth, VINP = 5.0V , VCC = 3.3V, I_{out} = 300mA, T_A=25°C		50	75	mV
EFF	Efficiency P_{VCC} to P_{VINP}	VINP = 5.0V, VCC = 3.3V, I_{out} = 300mA, T_A = 25°C		50		%
V_{CC_Rise}	VCC rise time from 10% - 90%	VINP = 5.0V, VCC = 3.3V, I_{out} = 70mA			500	µs
		VINP = 5.0V, VCC = 3.7V, I_{out} = 70mA			500	µs
VCC UVP UNDER -VOLTAGE PROTECTION (Secondary-side. All voltages with respect to GNDS)						
K_{VCC_UVP}	VCC under-voltage protection threshold ratio	V_{UVP} = VCC * 90%		90		%
V_{UVP_H}	VCC under-voltage protection hysteresis	VCC =3.3V	52	66	80	mV
V_{UVP_H}	VCC under-voltage protection hysteresis	VCC =3.7V	73	93	112	mV
VCC OVP OVER -VOLTAGE PROTECTION (Secondary-side. All voltages with respect to GNDS)						
$V_{VCC_OVP_R}$	VCC over-voltage protection rising threshold	VCC = 3.3V		3.75	3.8	V
$V_{VCC_OVP_H}$	VCC over-voltage protection hysterisis	VCC = 3.3V		0.1		V
$V_{VCC_OVP_R}$	VCC over-voltage protection rising threshold	VCC = 3.7V		4.2	4.25	V
$V_{VCC_OVP_H}$	VCC over-voltage protection hysterisis	VCC = 3.7V		0.1		V
SECONDARY SIDE THERMAL SHUTDOWN						
TSD_{S_R}	Secondary-side over-temperature shutdown rising threshold		150	165		ºC
TSD_{S_F}	Secondary-side over-temperature shutdown falling threshold		130			ºC
TSD_{S_H}	Secondary-side over-temperature shutdown hysteresis			20		ºC

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5.8 External BOM Components

Over recommended conditions

COMPONENT		NOTES	MIN	TYP	MAX	UNIT
C_{IN1}	VINP first decoupling capacitor			2.2		nF
C_{IN2}	VINP second decouling capacitor		10	22		µF
C_{OUT1}	VCC first decoupling capacitor			2.2		nF
C_{OUT2}	VCC second decoupling capacitor		10	22		µF

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6 Detailed Description

6.1 Overview

The UCC33410-Q1 device integrates a high-efficiency, low-emissions isolated DC/DC converter. Requiring minimum passive componenets to form a completely functional DC/DC power module, the device can deliver a maxiumum power of 1.0W across a $3kV_{RMS}$ basic isolation barrier over a wide range of operating temperatures in a low profile , high power density VSON - 12-pin package.

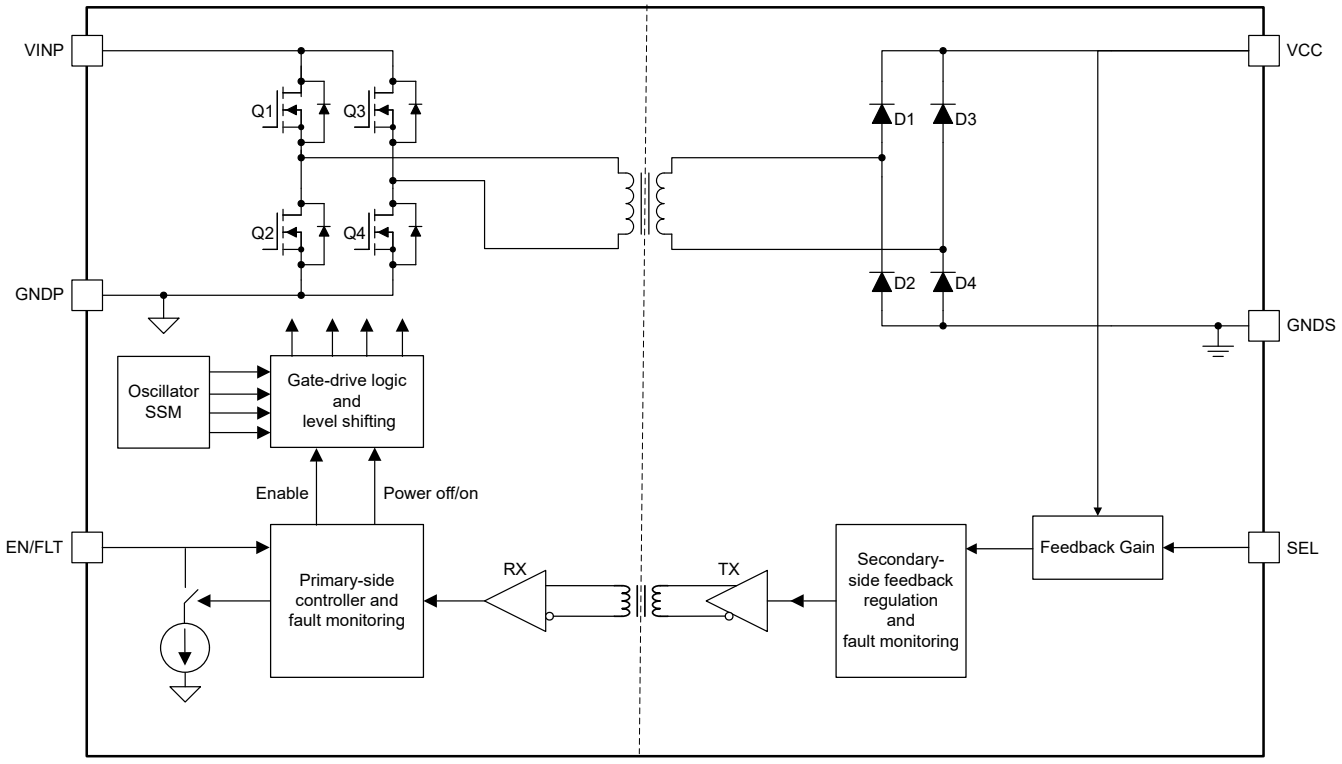
The easy-to-use feature, low profile and high power density promotes this device for size limited, cost sensitive systems with a minimum design effort replacing bulky and expensive transformer based designs.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency across all loading conditions. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The VINP supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified, and regulated using a fast hysteritic burst mode control scheme that monitors VCC and ensures it is kept within the hysterisis band under normal and transient loading events while maintaining efficient operation across all loading conditions. The VCC is regulated to 3.3V or 3.7V by SEL pin connection to have enough headrome for a post regulator LDO for tighter regulation or lower output ripple requirement applications .

The device has an enable pin to turn the device on or off depending on the system requirement. Pulling enable pin low will reduce the quiscent current significantly if the system wants to operate in a low power conumption mode. The enable pin can also be used as a fault reporting pin, when connected to 18kΩ, the pin will be pulled low for 200µs for any fault shutdown of the device. The device has a soft-start mechanism for a smooth and fast VCC ramp up with minimum input inrush current to avoid oversizing front-end power supplies powering the device's input.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Enable and Disable

Forcing EN/FLT pin low disables the device, which greatly reduces the VINP power consumption. Pull the EN/FLT pin high to enable normal device functionality. The EN/FLT pin has a weak internal pull-down resistor so it is not recommended to leave this pin floating in noisy systems.

6.3.2 Output Voltage Soft-Start and Steady-State Regulation

The UCC33410-Q1 has soft-start mechanism that ensures a smooth and fast soft-start operation with minimum input inrush current. The output voltage Soft-Start diagram is shown in Figure 6-1. After VINP > $V_{VINP_UVLO_R}$ and EN/FLT is pulled high, the soft-start sequence starts with a primary duty cycle open loop control. The power stage operates with a fixed burst frequency with an incremental increasing duty cycle starting at 6.5% . The rate of change of the duty cycle is pre-programmed in the part to reduce the input inrush current while building the output voltage VCC. The primary side limits the maximum duty cycle during this phase till the secondary side VCC voltage passes a certain threshold before releasing this duty cycle limit. This limit will ensure minimum input current in case the device starts on a short circuit and the VCC is not building up. Once the VCC reaches the regulation range, the duty cycle is no longer determined from the primary side controller but instead VCC hysteritic control is active to tightly regulate the output voltage within the defined hysterisis bands to reduce the output voltage ripple.

The soft-start time will vary depending on the output capacitors and loading conditions. During VCC regulation state, the burst frequency will change according to the output capacitors and loading conditions. The burst frequency will be highest at higher loading conditions and lowest at light loading conditions by which light load efficiency improvments can be achieved.

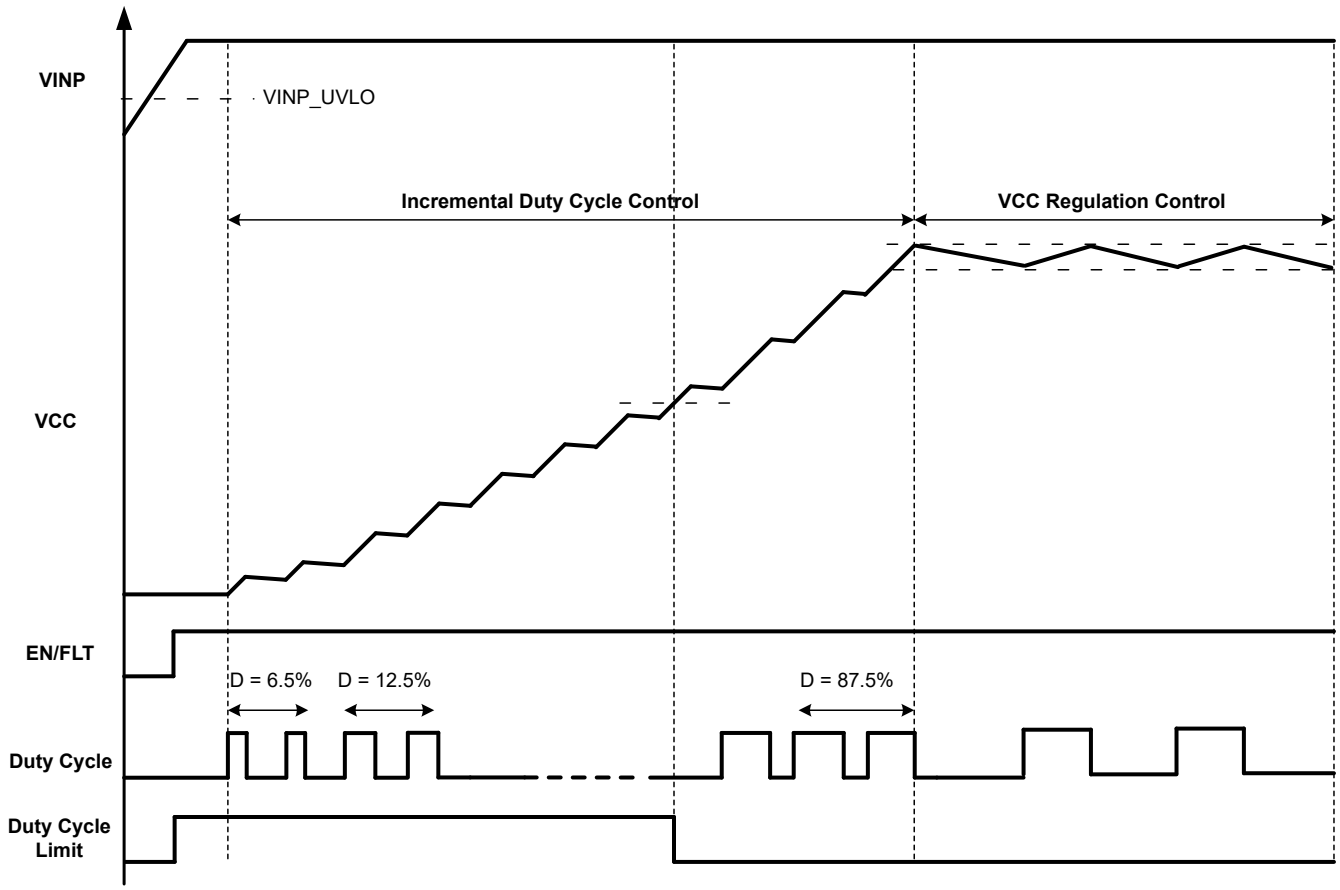


Figure 6-1. Output Voltage Soft-Start Diagram

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6.3.3 Protection Features

The UCC33410-Q1 is equipped with full feature of protection functions including input under-voltage lockout, input over-voltage lockout, output under-voltage protection and over-temperature protection. In addition, the device has a fault reporting mechanism that can be utilized on the system level to report faulty conditions of the device that caused a shutdown. Under certain faulty conditions the device will shutdown and attempt an auto-restart after defined duration.

6.3.3.1 Input Under-voltage and Over-Voltage Lockout

The UCC33410-Q1 can operate at input voltage range from 4.5V to 5.5V. If the VINP < $V_{VINP_UVLO_F}$ or VINP > $V_{VINP_OVLO_R}$ conditions occured, the converter will stop switching and part will shutdown. Once the VINP gets back in normal operation range , VINP > $V_{VINP_UVLO_R}$ or VINP < $V_{VINP_OVLO_F}$. The part will resume switching immediately without waiting for the auto-restart timer.

6.3.3.2 Output Under-Voltage Protection

The UCC33410-Q1 has under voltage protection feature to protect the part when overload condition occurs . If an overload or a short circuit occurs at VCC such that VCC < 0.9 ×VCC condition occurs, the converter will go into the duty cycle limit mode as in the soft-start operation then will shutdown after a certain deglitch time. The deglitch time is added to accommodate for any instantaneous overloading or short circuit conditions that might be removed quickly and normal operation can resume. Once the part shuts down, the part will attempt an auto-restart after 160ms. If the fault condition remains, the part will shutdown again and attempt another auto-restart.

6.3.3.3 Output Over-Voltage Protection

The UCC33410-Q1 has over voltage protection feature to protect the load against over-voltage conditions . If an over-voltage , the converter will go into the duty cycle limit mode as in the soft-start operation then will shutdown after a certain deglitch time. Once the part shuts down, the part will attempt an auto-restart after 160ms. If the fault condition remains, the part will shutdown again and attempt another auto-restart.

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6.3.3.4 Over-Temperature Protection

The UCC33410-Q1 integrates the primary-side, secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature higher than the ambient temperature. To ensure the safe operation of the power module, the device is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher TSD_{P_R}, or the secondary-side power stage temperature becomes higher than TSD_{S_R} , the module enters over-temperature protection mode. The module stops switching after a defined deglitch time, report the fault and attempt an auto-restart after 160ms.

6.3.3.5 Fault Reporting and Auto-Restart

The UCC33410-Q1 has a fault reporting mechanism that can alert a system level MCU or monitoring circuitry of faulty onditions on the device that resulted in a shutdown. If an input over-voltage , over-temperature or output under voltage protection faults occur. The primary-side controller and fault monitoring system will enable a current source that will sink I_{Fault} current for t_{Fault} duration. If a resistor >18kΩ is connected between the MCU and the EN/FLT pin, the V_{FLT} will be pulled low for the same t_{Fault} duration whenever one of the abovementioned faults occur that resulted in a shutdown of the device as shown in Figure 6-2. If the fault reporting mechanism is not required on the system, the EN/FLT pin can be connected directly to the enable source voltage without the 18kΩ resistor.

The device has a auto-restart feature that occur after the device is shutdown only due to when output under-voltage or over-temperature faults occur. After the t_{Fault} time expires, a 160ms timer will start and the part will attemp a new soft-start sequence as shown in Figure 6-3. If the fault has been removed, the VCC will soft-start to regulation successfully. If the fault remains , the part will shutdown again and report the fault. The device can continuously operate safely in hiccup mode as long as the fault occurs.

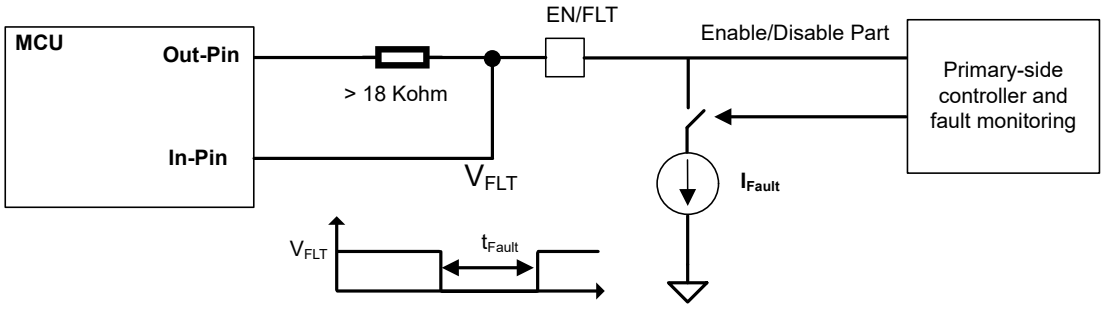


Figure 6-2. Fault Reporting Mechanism

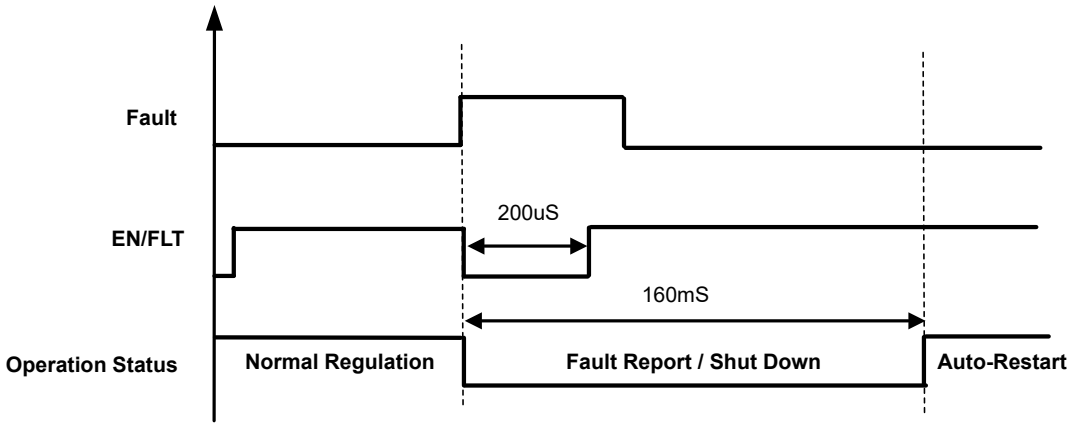


Figure 6-3. Auto-restart operation

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6.3.4 VCC Output Voltage Selection

The UCC33410-Q1 can program the VCC voltage accoring to the SEL pin connection. The SEL pin voltage is monitored during soft-start sequence. The output voltage is then programmed to 3.3V with SEL = VCC or 3.7V with SEL = GNDS. Note that after this initial monitoring, the SEL pin no longer affects the VCC output level. In order to change the output mode selection, either the EN/FLT pin must be toggled or the VINP power supply must be cycled off and back on.

6.3.5 VCC Load Recommended Operating Area

Figure 6-4 depicts the device VCC regulation behavior across the output load range, including when the output is overloaded. For proper device operation, ensure that the device VCC output load does not exceed the maximum output current I_{OUT_MAX}. The value for I_{OUT_MAX} over different temperature and V_{INP} conditions are shown from "TBD". If the UCC33410-Q1 is loaded beyond the recommended operating area, the VCC will drop and once it goes below the VCC_UVP threshold, the part enters a power limiting mode to avoid stressing the device till power stage stop switching and shutdown.

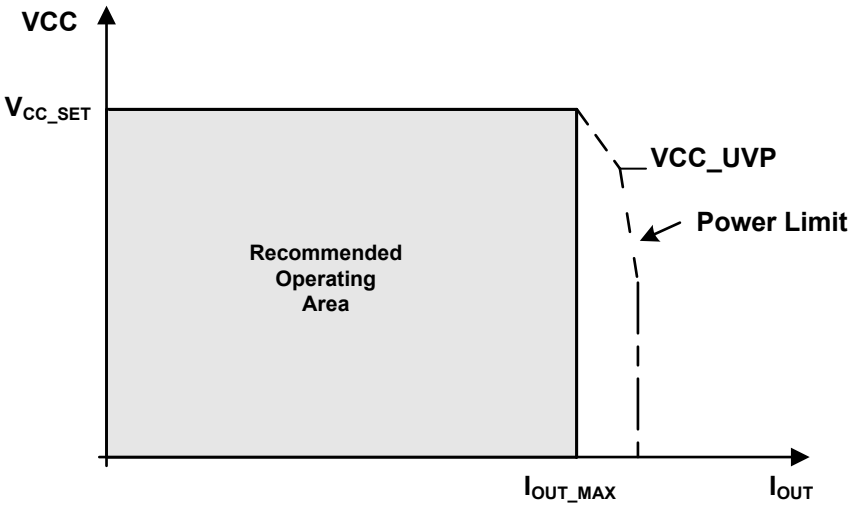


Figure 6-4. VCC Load Recommended Operating Area Description

6.3.6 Electromagnetic Compatibility (EMC) Considerations

UCC33410-Q1 devices use spread spectrum modulation algorithm for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x , CISPR 32 and CISPR-25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the device incorporates many chip-level design improvements for overall system robustness.

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6.4 Device Functional Modes

Table 6-1 lists the supply functional modes for this device.

Table 6-1. Device Functional Modes

INPUTS		Isolated Supply Output Voltage (VCC) Setpoint
EN/FLT	SEL	
HIGH	Shorted to VCC	3.3V
HIGH	Shorted to GNDS	3.7V
Low	x	0V
OPEN(1)	OPEN(1)	UNSUPPORTED

(1) The SEL and EN/FLT pins has an internal weak pull-down resistance to ground, but leaving this pin open is not recommended.

6.5 Pre-Production Samples Operating Limits

UCC33410-Q1 pre-production samples have the following operating limits. Production devices will have these limitations removed.

1. For ambient operating temperature < 0°C, the following sequence is required to allow the device reach regulation point during start-up. EN/FLT pin required to be high ($V_{EN/FLT}$ > V_{EN_R}) before applying input voltage VINP to the device. This can be achieved by connecting EN/FLT pin after the 18kΩ resistor directly to the VINP pin and applying VINP with rise time > 6ms on the device.
2. For ambient operating temperature < 0°C, the following protection features; short-circuit, UVP and OVP protections of VCC output are disabled. Fault reporting and auto-restart features due to these faults will be disabled as well. If the part shuts down as a result of fault condition, the part will require to follow the same condition in step 1 above to restart and reach regulation. This require to recycle VINP by falling below $V_{VINP_UVLO_F}$ and then rising above $V_{VINP_UVLO_R}$ with the same > 6ms rise time.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UCC33410-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

7.2 Typical Application

Typical Application shows the schematic for the UCC33410-Q1 device supplying an isolated load.

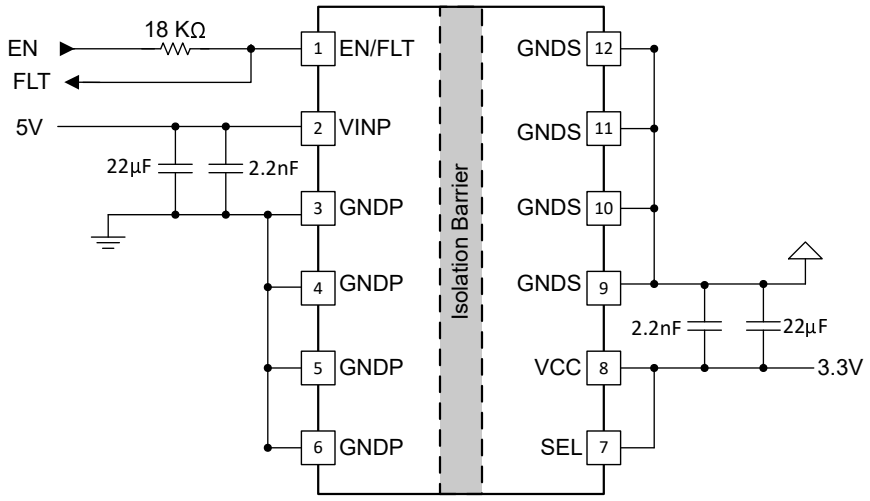


Figure 7-1. Typical Application

7.2.1 Design Requirements

To design using UCC33410-Q1, a few simple design considerations must be evaluated. Table 7-1 shows some recommended values for a typical application. See Section 7.3 and Section 7.4 sections to review other key design considerations for the UCC33410-Q1.

Table 7-1. Design Parameters

PARAMETER	RECOMMENDED VALUE
Input supply voltage, VINP	4.5V to 5.5V
First Decoupling capacitance between VINP and GNDP	2.2nF, 16V, ± 10%, X7R
Second Decoupling capacitance between VINP and GNDP	22µF, 16V, ± 10%, X7R
First Decoupling capacitance between VCC and GNDS	2.2nF, 16V, ± 10%, X7R
Second Decoupling capacitance between VCC and GNDS	22µF, 16V, ± 10%, X7R
EN/FLT pin resistor for fault reporting	18kΩ

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7.2.2 Detailed Design Procedure

The UCC33410-Q1 design procedure is very simple, the device requires two decoupling capacitors connected between VINP and GNDP pins for the input supply, and two decoupling capacitors for the isolated output supply placed between VCC and GNDS pins to form a completely functinoal DC/DC converter.

A low ESR, ESL ceramic capacitors are recommended to be connected close to the device pins. It should be noted that the effective burst frequency would be impacted by the selected VCC output capacitor

7.3 Power Supply Recommendations

The recommended input supply voltage (VINP) for the UCC33410-Q1 is between 4.5V and 5.5V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Place local bypass capacitors between the VINP and GNDP pins at the input, and between VCC and GNDS at the isolated output supply. The input supply must have an appropriate current rating to support output load required by the end application.

7.4 Layout

7.4.1 Layout Guidelines

The UCC33410-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Proper PCB layout is important in order to achieve optimum performance. Here is a list of recommendations:

- Place decoupling capacitors as close as possible to the device pins. For the input supply, place 0402 and 0805 ceramic capacitor between pin 2 (VINP) and pins 3, 4, 5 and 6 (GNDP). For the isolated output supply, place 0402 and 0805 ceramaic capacitora between pin 8 (VCC) and pins 9, 10, 11 and 12 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
- Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on all GNDP and GNDS pins for best heat-sinking. Placing vias close to the device pins and away from the high frequency path between the ceramic capacitors and the device pins is essential for better thermal performance.
- If space and layer count allow, it is also recommended to connect the VINP, GNDP, VCC and GNDS pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
- Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (GNDS) on the PCB outer layers. The effective creepage and or clearance of the system reduces if the two ground planes have a lower spacing than that of the device package.
- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC33410-Q1 device on the outer copper layers.

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7.4.2 Layout Example

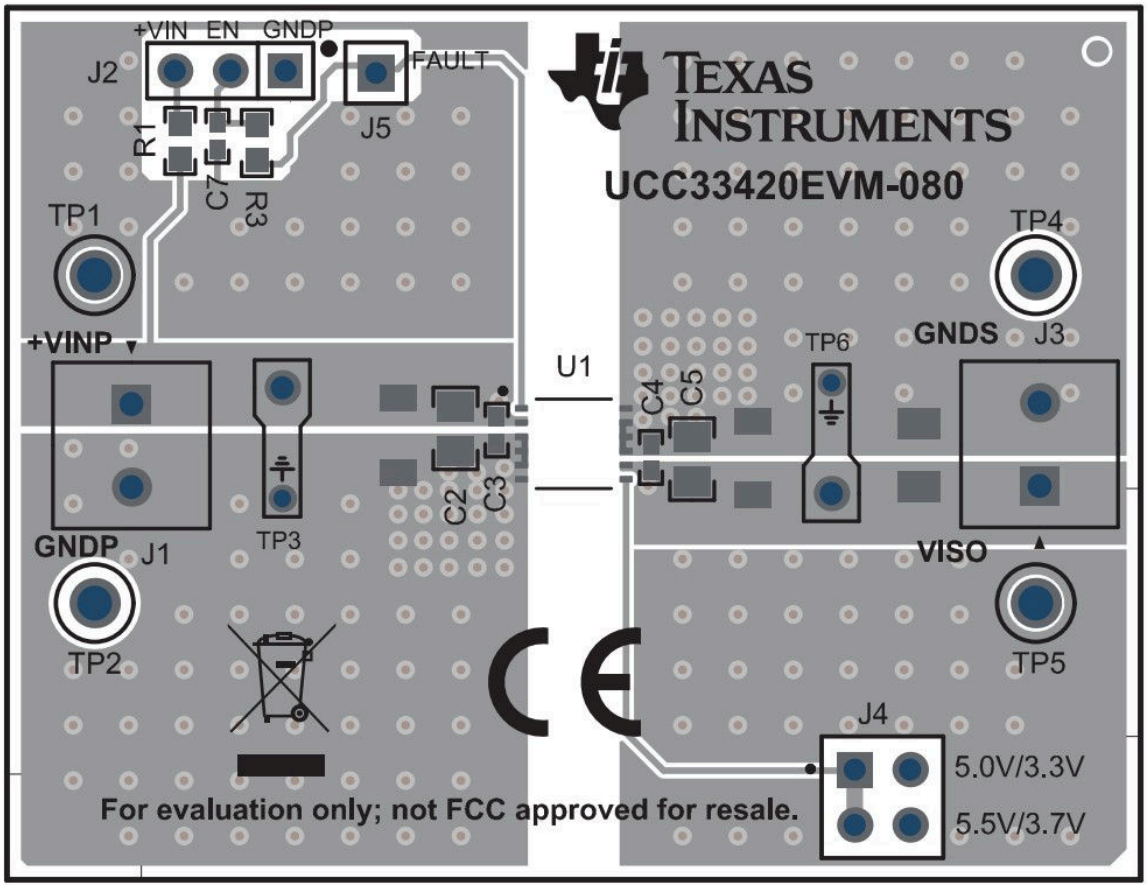


Figure 7-2. Layout Example

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8 Device and Documentation Support

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Isolation Glossary

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
June 2024	*	Advance Information Release

ADVANCE INFORMATION

10 Mechanical and Packaging Information

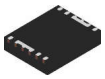
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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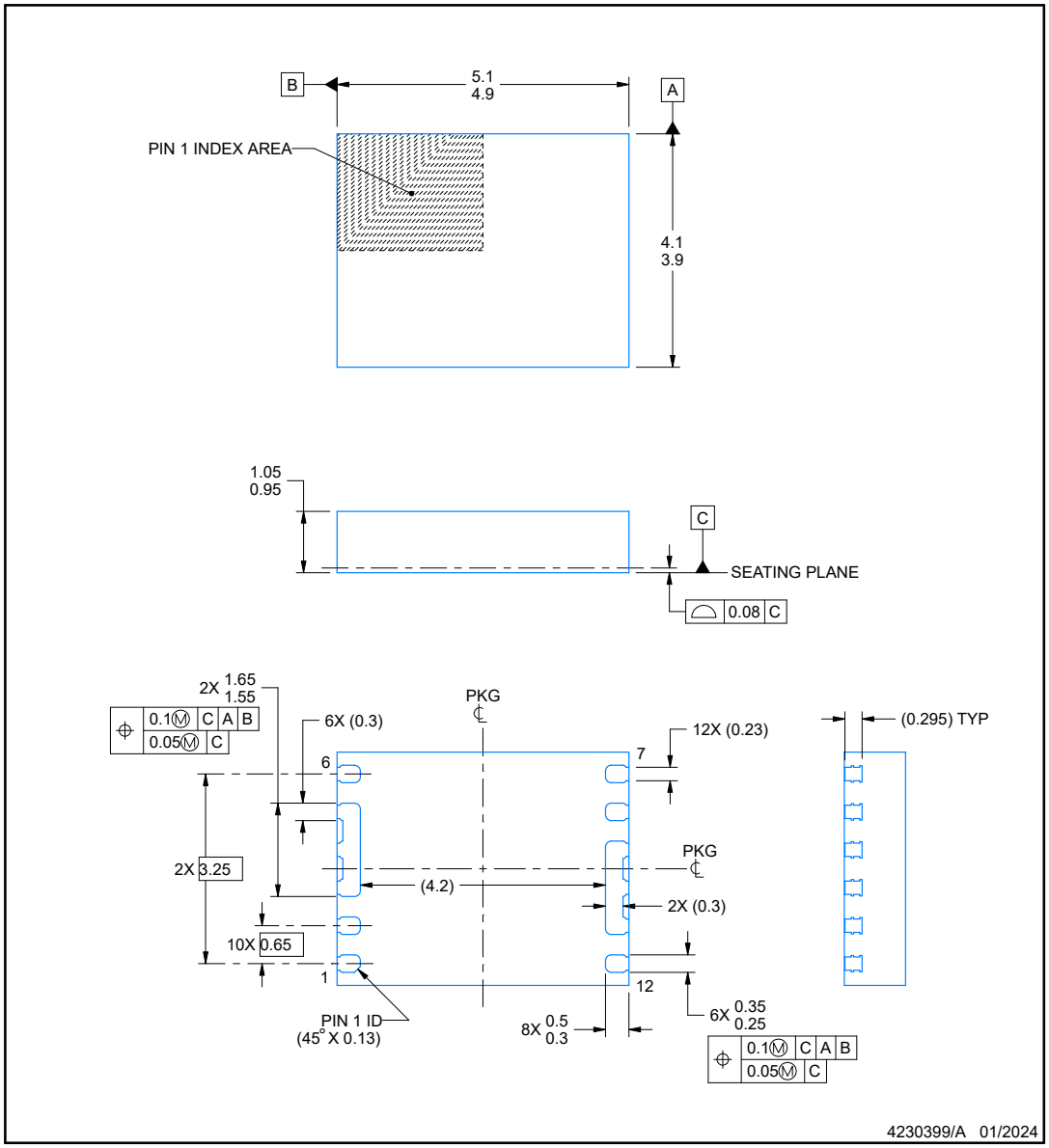
PACKAGE OUTLINE

RAQ0012C



VSON-FCRLF - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

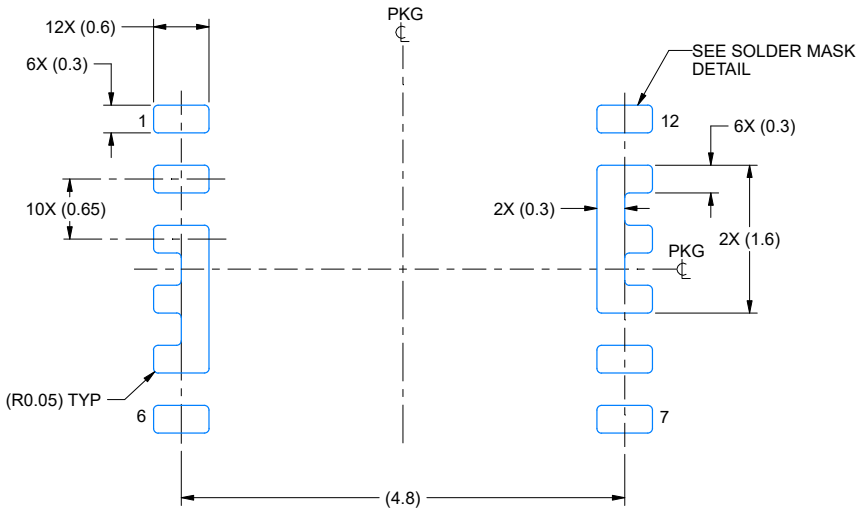
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ADVANCE INFORMATION

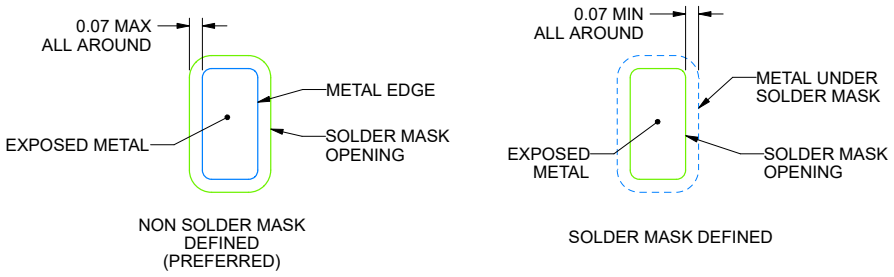
EXAMPLE BOARD LAYOUT

RAQ0012C — **VSON-FCRLF - 1.05 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4230399/A 01/2024

NOTES: (continued)

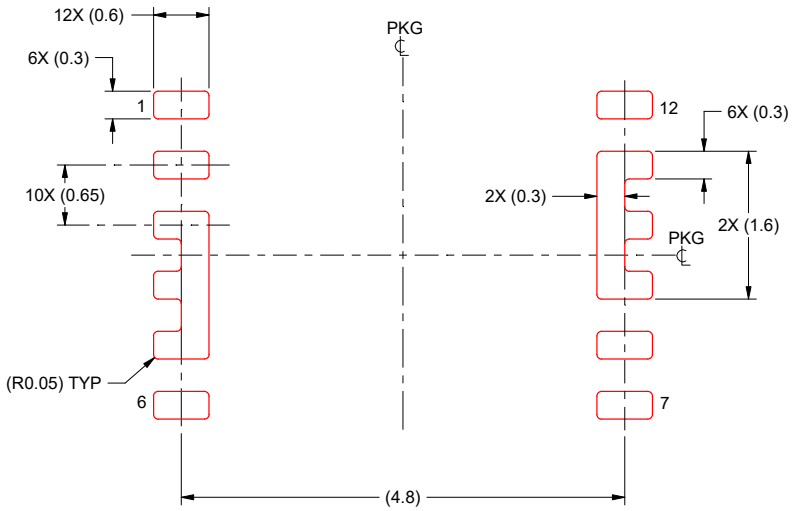
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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EXAMPLE STENCIL DESIGN

RAQ0012C — **VSON-FCRLF - 1.05 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

4230399/A 01/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC33410QRAQRQ1	Active	Preproduction	VSON-FCRLF (RAQ) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC33410QRAQRQ1.A	Active	Preproduction	VSON-FCRLF (RAQ) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC33410-Q1 :

- Catalog : UCC33410

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

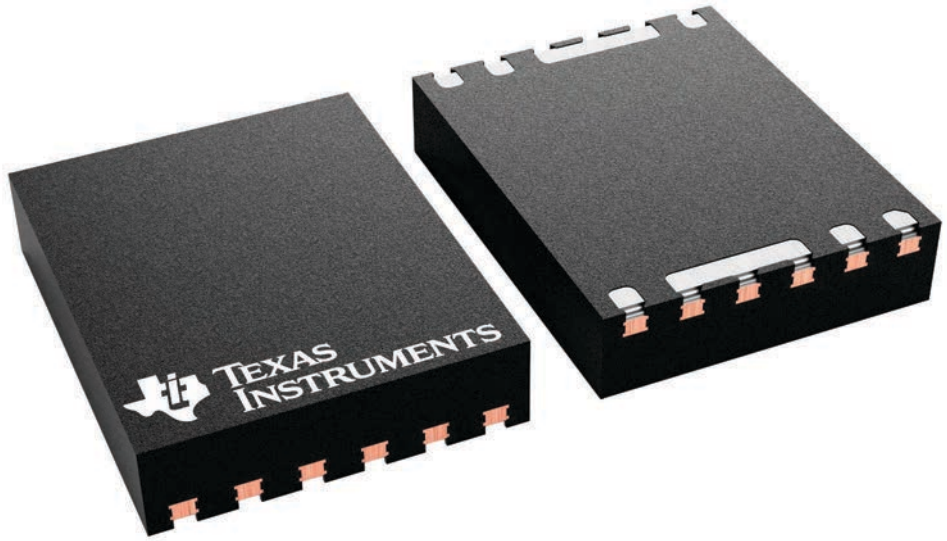
RAQ 12

VSON-FCRLF - 1.05 mm max height

5 x 4, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229417/A

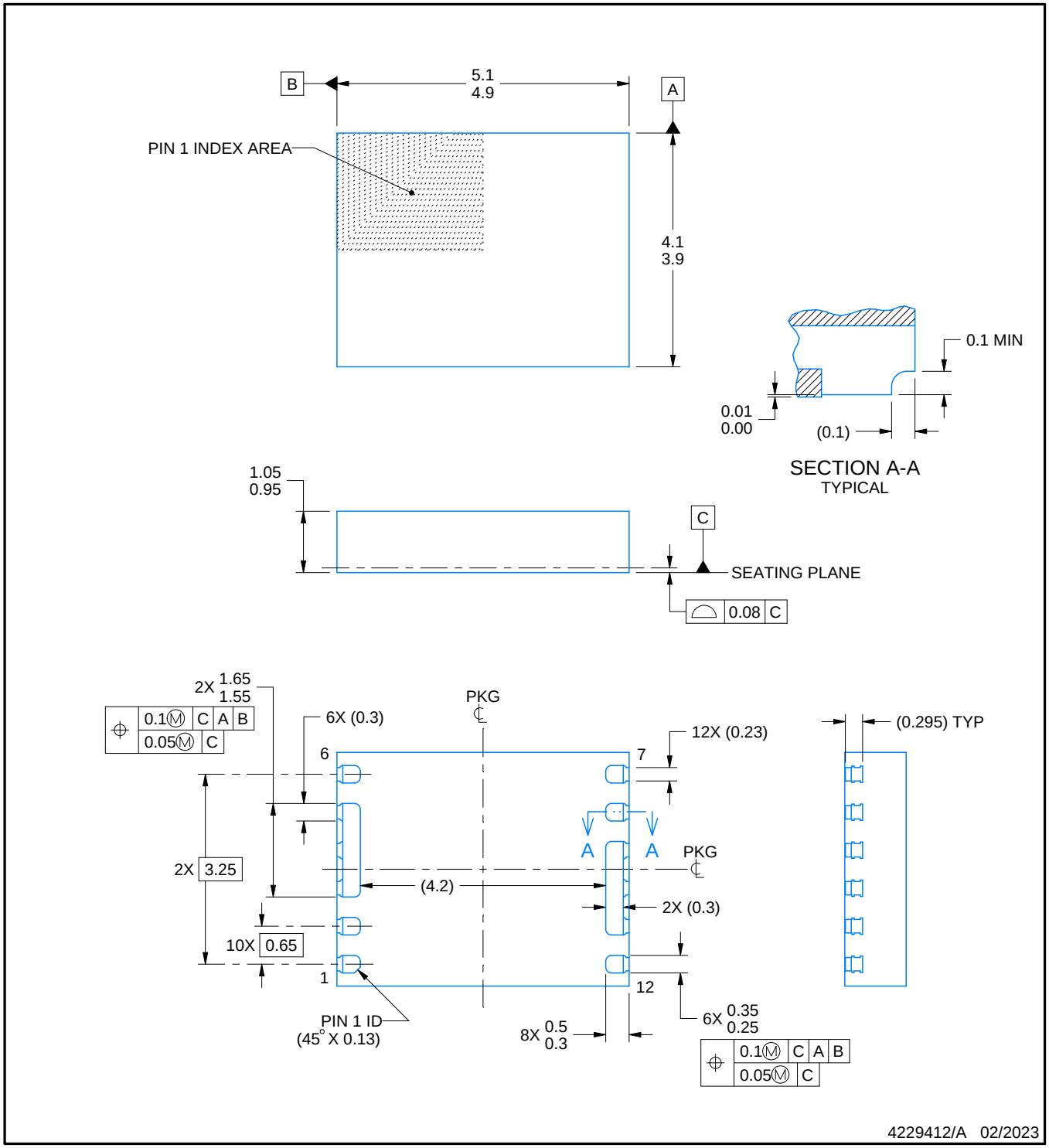
PACKAGE OUTLINE

RAQ0012B



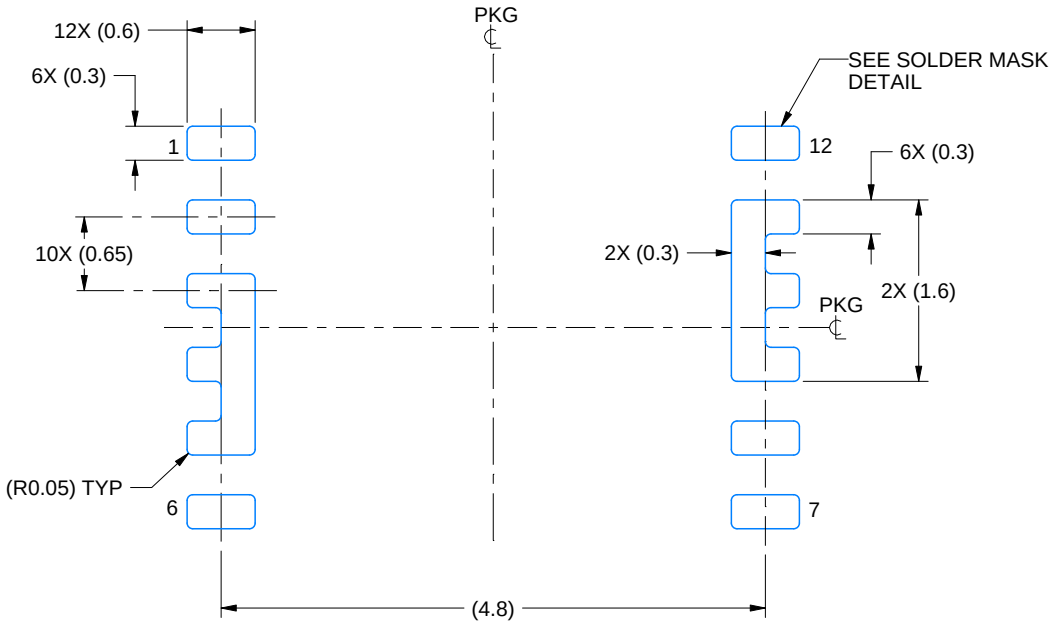
VSON-FCRLF - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229412/A 02/2023

NOTES: (continued)

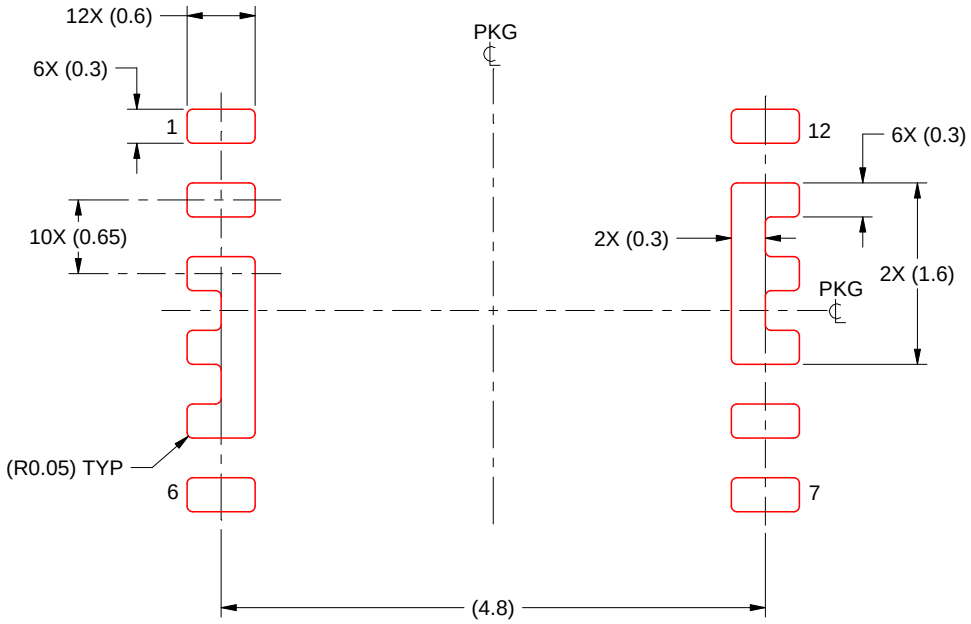
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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EXAMPLE STENCIL DESIGN

RAQ0012B

VSON-FCRLF - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

4229412/A 02/2023

NOTES: (continued)

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