austriamicrosystems AG

is now

ams AG

The technical content of this austriamicrosystems datasheet is still valid.

Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

AS1122

12-Channel LED Driver with Dot Correction and Greyscale PWM

1 General Description

The AS1122 is a 12-channel, constant current-sink LED driver. Each of the 12 channels can be individually adjusted by 4096-step greyscale PWM brightness control and 64-step constant-current sink (dot correction).

The dot correction circuitry adjusts the brightness variations between the AS1122 channels and other LED drivers. Greyscale control and dot correction circuitry are accessible via a simple SPI-compatible serial interface.

The open LED detection function indicates a broken or disconnected LED at one or more of the outputs. The overtemperature flag indicates that the device is in an overtemperature condition.

A single external resistor sets the maximum current value of all 12 channels.

The AS1122 is available in a 24-pin QFN 4x4mm package.

2 Key Features

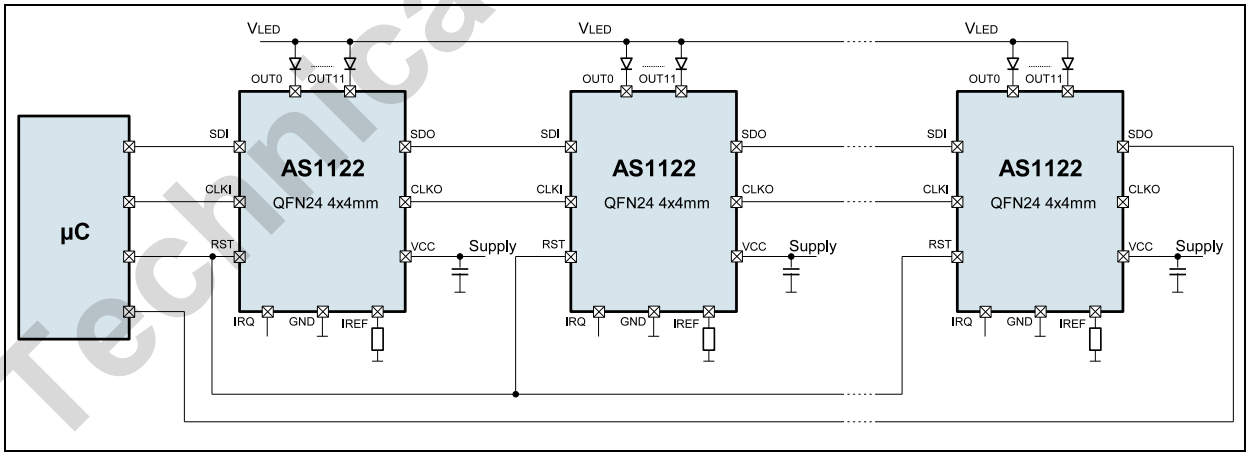
- Greyscale PWM Control: 12-Bit (4096 Steps)
- Dot Correction: 6-Bit (64 Steps)
- Drive Capability (Constant-Current Sink): 0 to 40mA
- LED Power Supply Voltage: up to 30V
- Supply Voltage Range: 2.7V to 3.6V
- Output Delay for controlled Inrush Current (factory set, can be turned off)
- Factory set rise- and fall-time for EMI improvement
- Internal PWM Clock: 10 MHz (typ)
- Data Transfer Clock Rate: up to 5 MHz
- CMOS Level I/O
- Diagnostic Features
- 24-pin QFN 4x4mm Package

3 Applications

The device is ideal for mono-, multi-, and full-color LED displays, LED signboards, and display backlights.

Technical content still valid ams AG

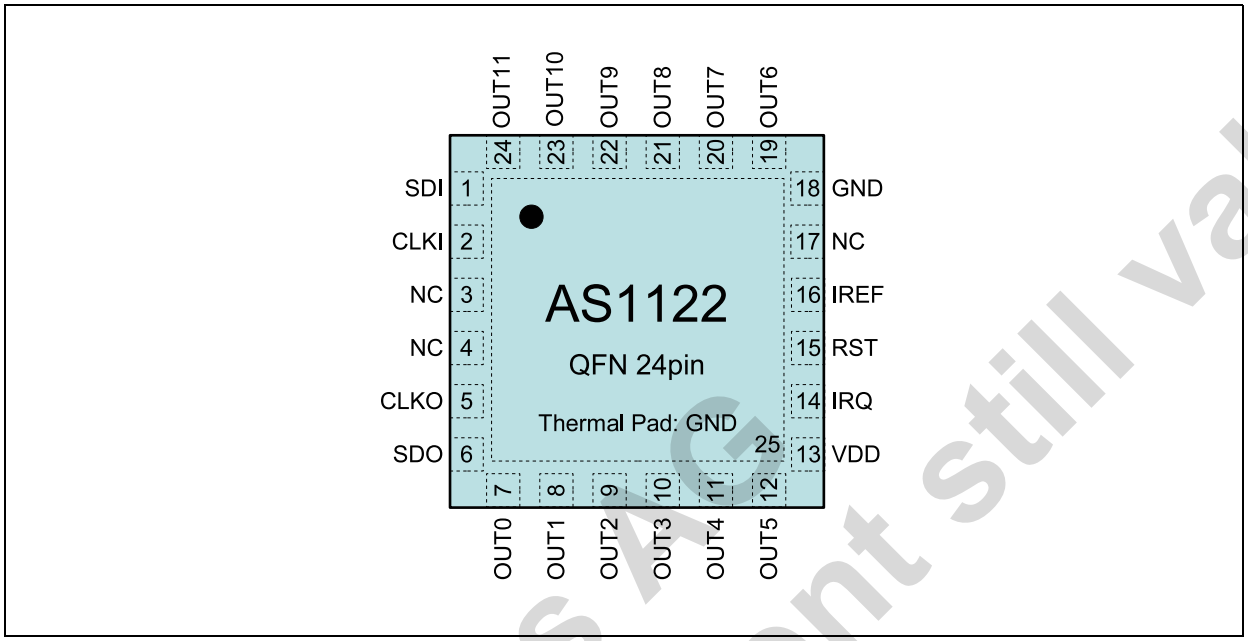
Figure 1. AS1122 - Typical Application Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	SDI	**Serial Data Input**
2	CLKI	**Serial Data Clock Input**
5	CLKO	**Serial Data Clock Output**
6	SDO	**Serial Data Output**
7:12, 19:24	OUT0:OUT11	**Constant-Current Outputs 0:11**
13	VDD	**Power Supply Voltage**
14	IRQ	**Interrupt Request Output.** Open drain pin, can be left open if not used.
15	RST	**Reset Input.** Pull this pin to high to reset all registers (set to default values) and to put the device into shutdown. Connect this pin to GND for normal operation.
16	IREF	**Reference Current Terminal.** A resistor connected to this pin sets the maximum output currents **(see Setting Maximum Channel Current on page 15)**.
18	GND	**Ground**
3, 4, 17	NC	**Not Connected.** Connect to GND if not used.
25	Thermal Pad	**Ground.** This pin must be connected to GND to ensure normal operation.

Technical content still valid ams AG

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VCC to GND	-0.3	5	V	
All other pins to GND	-0.3	VDD + 0.3	V	
VSDO to GND	-0.3	VDD + 0.3	V	
VOUT0 : VOUT11 to GND	-0.3	30	V	
Output Current		50	mA	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM	+/- 2		kV	Norm: MIL 883 E method 3015
Thermal Information				
Junction to ambient thermal resistance		37	°C/W	For more information about thermal metrics, see application note *AN01 Thermal Characteristics*.
Temperature Ranges and Storage Conditions				
Junction Temperature		+150	ºC	
Storage Temperature Range	-55	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	3			Represents a max. floor life time of 168h

Technical content still valid ams AG

6 Electrical Characteristics

VDD = +2.7V to +3.6V, Typical values are at TAMB = +25°C, VDD = 3.3V (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TAMB	Operating Temperature Range		-40		+85	°C
TJ	Operating Junction Temperature		-40		+125	°C
Input Supply						
VDD	Supply Voltage		2.7		3.6	V
ICC	Supply Current	All outputs on, RIREF = 1kΩ		9.5	12	mA
		All outputs on, RIREF = 10kΩ		4	6	
IPD	Power Down Current	RST = High, TAMB = +25°C		40		nA
Output						
RIREF	Reference Current Resistor		1		10	kΩ
VOUT	Voltage Applied to Output (OUT0:OUT11)				30	V
ICOC	Constant Output Current	All outputs on, VOUT = 1V, RIREF = 1kΩ	38	40	42	mA
ΔICOC	Constant Output Current Error	VOUT = 1V, RIREF = 1kΩ, OUT0:OUT11		±0.8	2	%
		VOUT = 1V, RIREF = 10kΩ, OUT0:OUT11		±1.5	4	
		Device to device, average current from OUT0:OUT11, VOUT = 1V, RIREF = 1kΩ		±0.5		
		Device to device, average current from OUT0:OUT11, VOUT = 1V, RIREF = 10kΩ		±0.6		
ILEAK	Leakage Output Current	All outputs off, VOUT = 30V, RIREF = 1kΩ, OUT0:OUT11		20		nA
ΔILNR	Line Regulation	VOUT = 1V, RIREF = 1kΩ OUT0:OUT11		±0.1	±1.5	%/V
		VOUT = 1V, RIREF = 10kΩ OUT0:OUT11		±0.2	±1.5	
ΔILDR	Load Regulation	VOUT = 1V to 4V, RIREF = 1kΩ, OUT0:OUT11		±0.1	±0.4	%/V
		VOUT = 1V to 4V, RIREF = 10kΩ, OUT0:OUT11		±0.01	±0.4	
Logic Levels						
VIH	High-Level Input Voltage		0.8 x VDD		VDD	V
VIL	Low-Level Input Voltage		GND		0.2 x VDD	V
VOH	High-Level Output Voltage	IOH = -1mA, SDO, CLKO	VDD -0.5			V
VOL	Low-Level Output Voltage	IOL = 1mA, SDO, CLKO			0.5	V
		IOL = 3mA, IRQ			0.5	V
VLOD	LED Open Detection Threshold			0.3	0.4	V
VIREF	Reference Voltage Output	RIREF = 1kΩ	1.24	1.27	1.30	V

ams AG
Technical content still valid

Timing Characteristics

V_{DD} = +2.7V to +3.6V, T_{AMB} = -40°C to +85ºC. Typical values are at T_{AMB} = +25°C, V_{DD} = 3.3V (unless otherwise specified).

Table 4. Output Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{R_OUT}	Rise Time OUT[1]			20		ns
t_{F_OUT}	Fall Time OUT[1]			20		ns
t_D[2]	Average Output Delay Time (can be turned off on request)			25		ns

1. Value can be factory trimmed for EMI improvement.
2. See Figure 24 on page 10.

Interface Characteristics

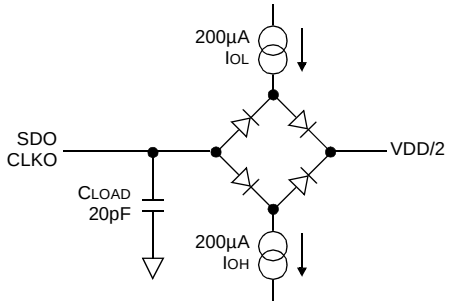
V_{DD} = +2.7V to +3.6V, T_{AMB} = -40°C to +85ºC. Typical values are at T_{AMB} = +25°C, V_{DD} = 3.3V (unless otherwise specified).

Table 5. Serial Interface Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator Frequency		8	10	12	MHz
f_{CLK}	Data Shift Clock Frequency		1		5	MHz
t_{LOW}[1]	CLK low time during data shift				1	µs
t_{CAPT}[1]	CLK low time for data capture		1.5	1.8	2.85	µs
t_{SETUP}[2]	Setup Time	SDI, CLKI	12			ns
t_{HOLD}[2]	Hold Time	SDI, CLKI	12			ns
t_{PD_rising}[2]	Delay CLKI to CLKO[3]	rising CLKI to rising CLKO	2	3.5	8	ns
$t_{PD_falling}$[2]	Delay CLKI to CLKO[3]	rising CLKI to falling CLKO	72	103.5	138	ns
t_{PD_SDO}[2]	Delay CLKO to SDO[3]	falling edge CLKO	0.8	1.5	3	ns
t_{H_CLKO}[2]	High Time of CLKO[3]		70	100	130	ns
t_{R_CLK}	Rise Time CLK[3]	C_{LOAD} = 20pF			10	ns
t_{R_DATA}	Rise Time Data[3]	C_{LOAD} = 20pF			10	ns

1. See Figure 24 on page 10
2. See Figure 36 on page 16 and Figure 37 on page 16
3. Guaranteed by design and not production tested.

Figure 3. Load Circuit for Digital Output Timing Specifications



Technical content still valid
ams AG

7 Typical Operating Characteristics

TAMB = +25°C, VDD = 3.0V, VOUT = 1.0V (unless otherwise specified)

Figure 4. Constant Output Current vs. Output Voltage

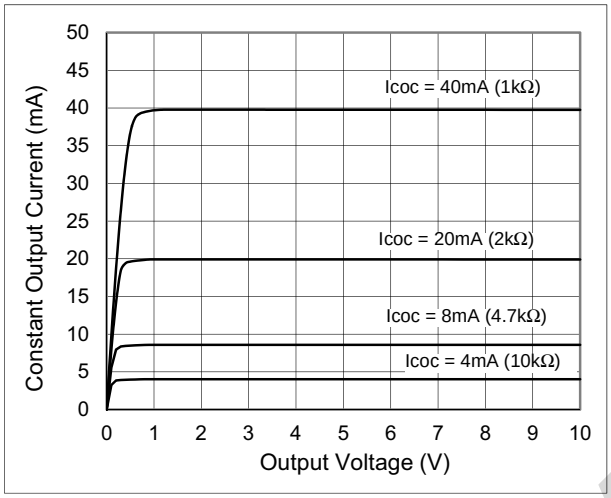


Figure 5. Constant Output Current vs. Output Voltage

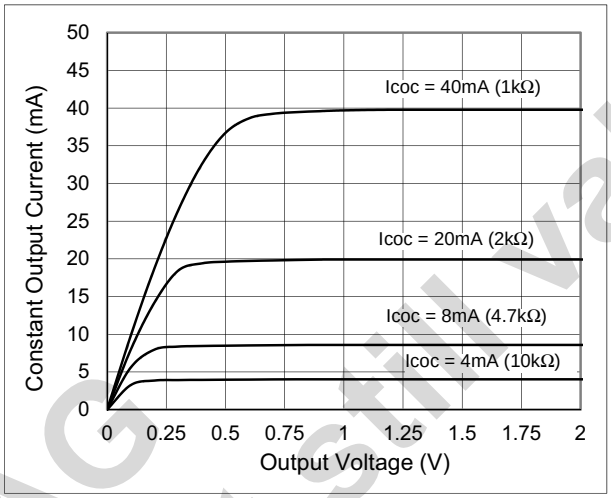


Figure 6. Constant Output Current vs. VOUT; REXT = 1kΩ

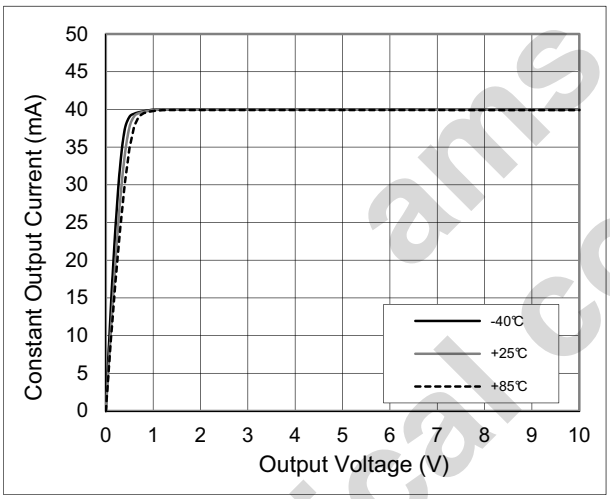


Figure 7. Constant Output Current vs. VOUT; REXT = 1kΩ

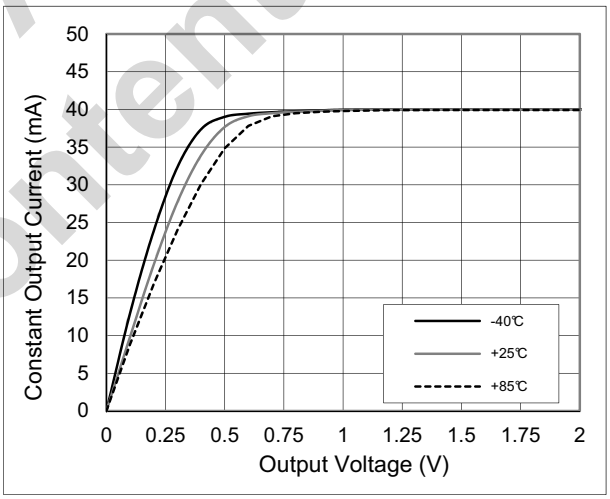


Figure 8. ICOC vs. Supply Voltage; REXT = 1kΩ

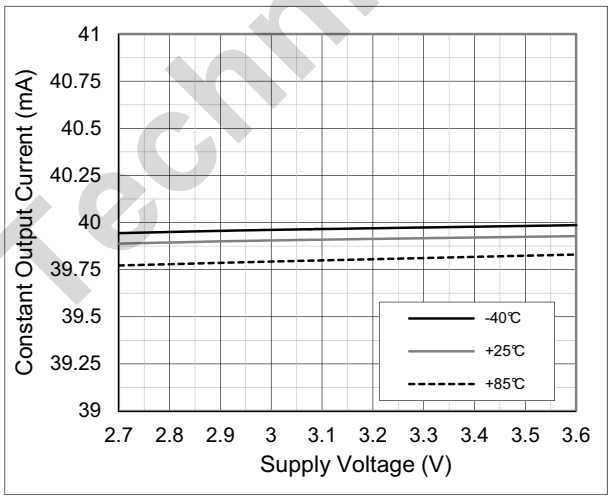
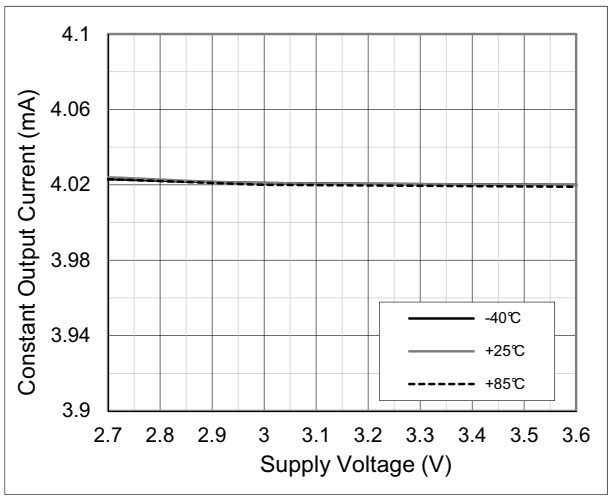


Figure 9. ICOC vs. Supply Voltage; REXT = 10kΩ



Technical content still valid ams AG

Figure 10. ICOC vs. Temperature; REXT = 1kΩ

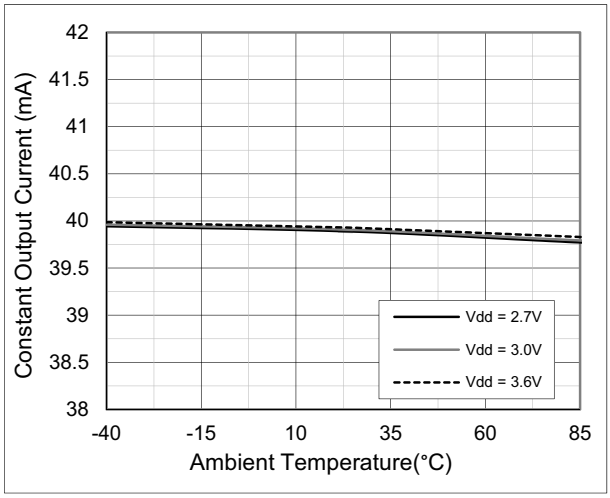


Figure 11. ICOC vs. Temperature; REXT = 10kΩ

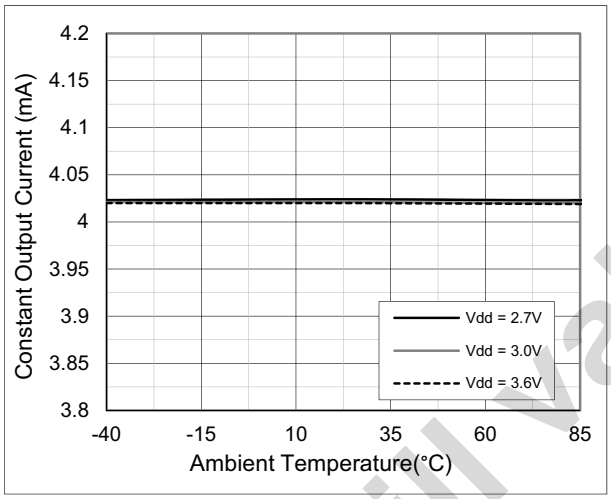


Figure 12. ICOC vs. REXT

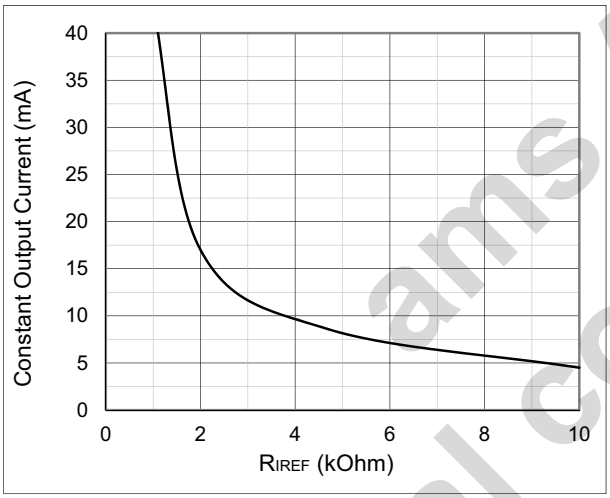


Figure 13. ICOC vs. Dot Correction; REXT = 1kΩ

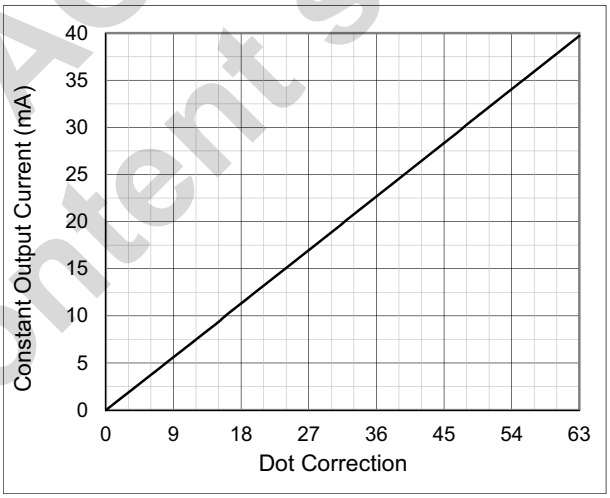


Figure 14. ICOC vs. PWM; REXT = 1kΩ

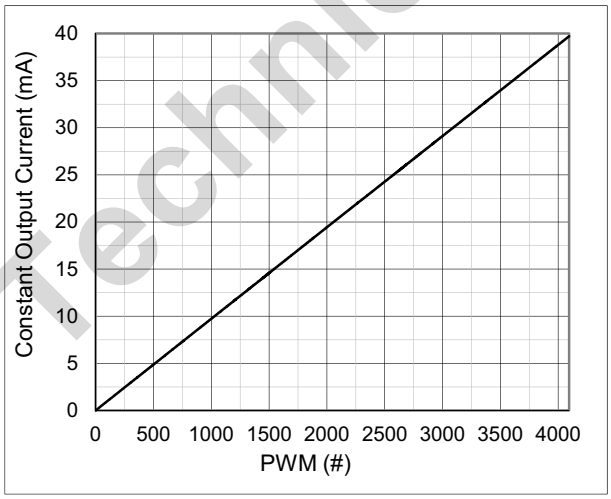
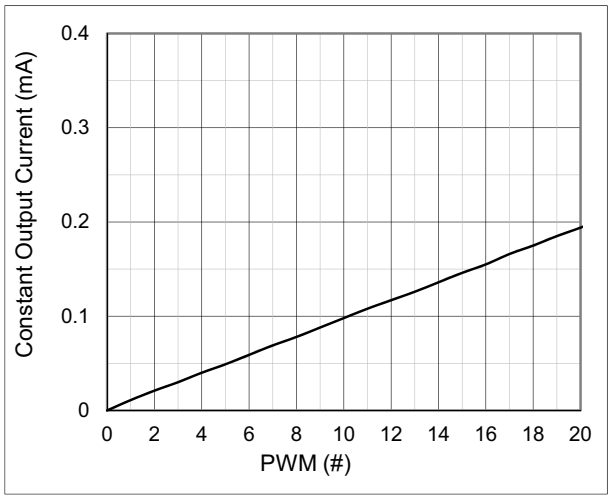


Figure 15. ICOC vs. PWM; REXT = 1kΩ



Technical content still valid
ams AG

Figure 16. ΔICOC vs. Constant Output Voltage; REXT = 1kΩ

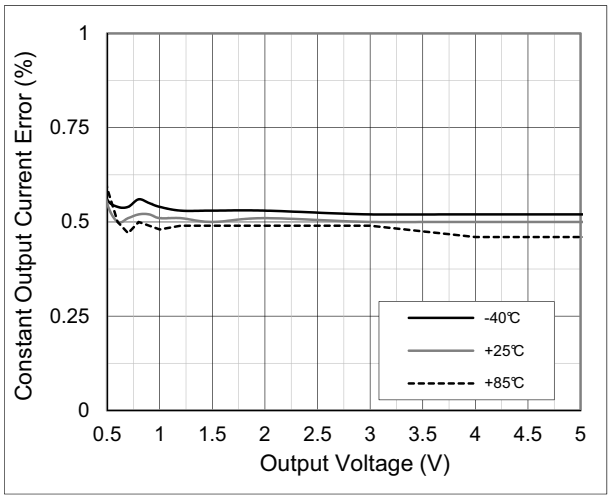


Figure 17. ΔICOC vs. Constant Output Voltage; REXT = 10kΩ

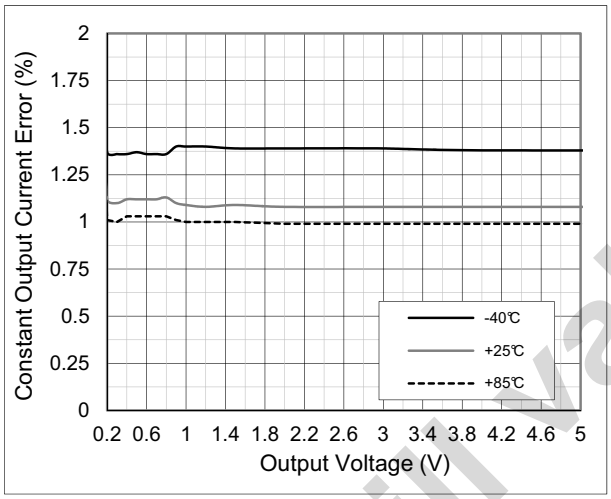


Figure 18. ΔICOC vs. Temperature; REXT = 1kΩ

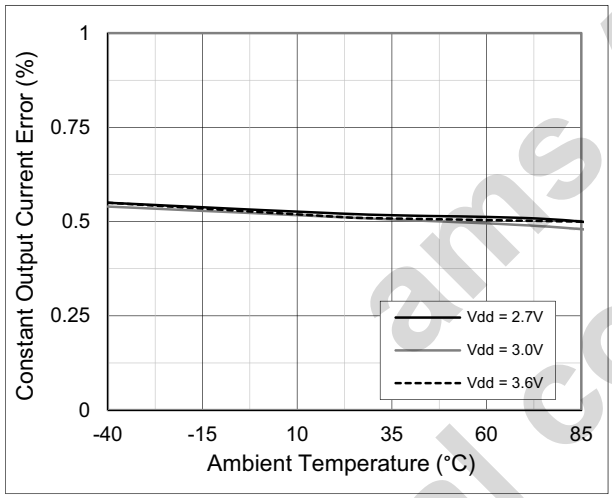


Figure 19. ΔICOC vs. Temperature; REXT = 10kΩ

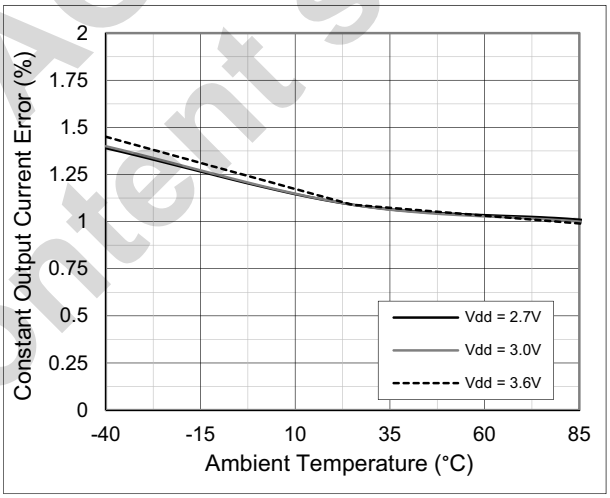


Figure 20. Supply Current vs. Temperature; REXT = 1kΩ

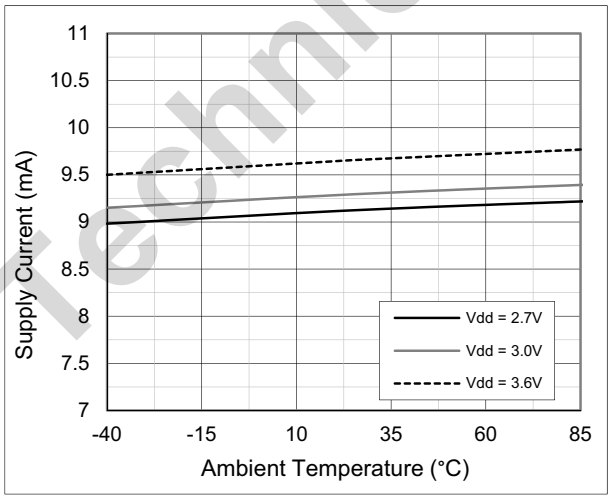
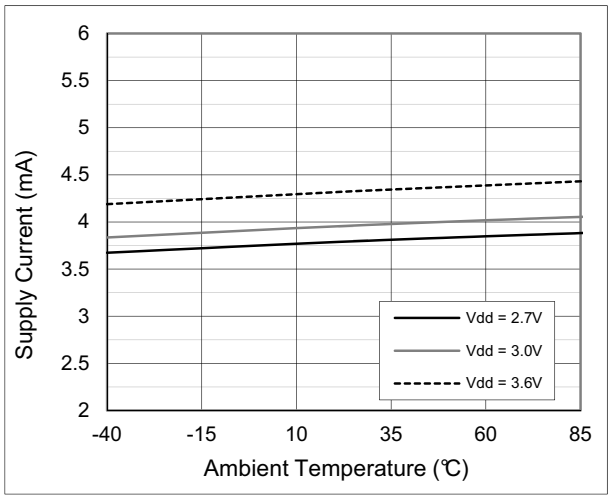


Figure 21. Supply Current vs. Temperature; REXT = 10kΩ



ams AG
Technical Content still valid

Figure 22. LED Open Detection Threshold vs. Temperature

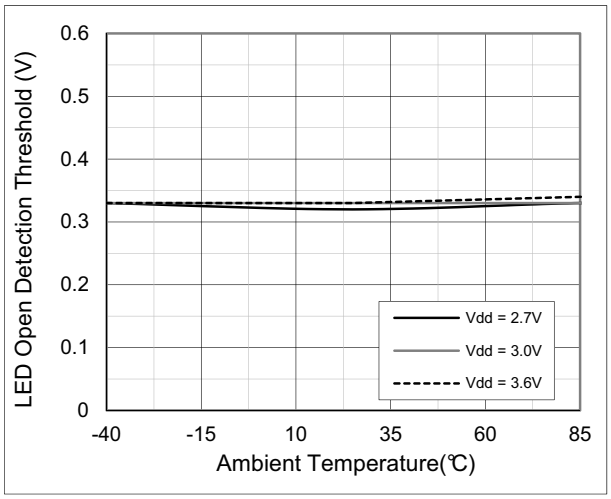
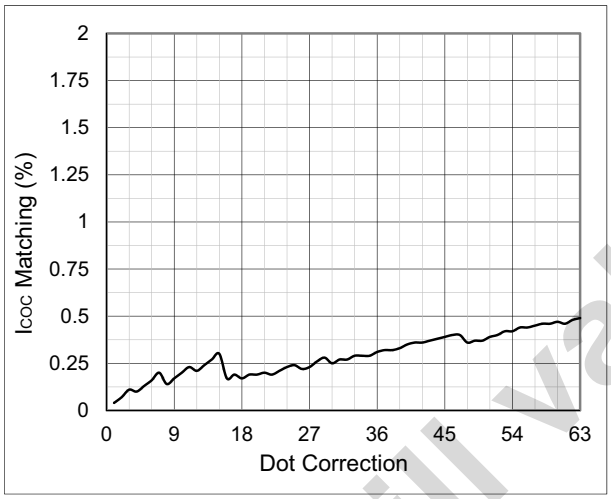


Figure 23. ΔIcoc Matching vs. Dot Correction; REXT = 1kΩ



ams AG
Technical content still valid

8 Detailed Description

Serial Interface

The AS1122 features a 4-pin (CLKI, CLKO, SDI, and SDO) serial interface, which can be connected to microcontrollers or digital signal processors.

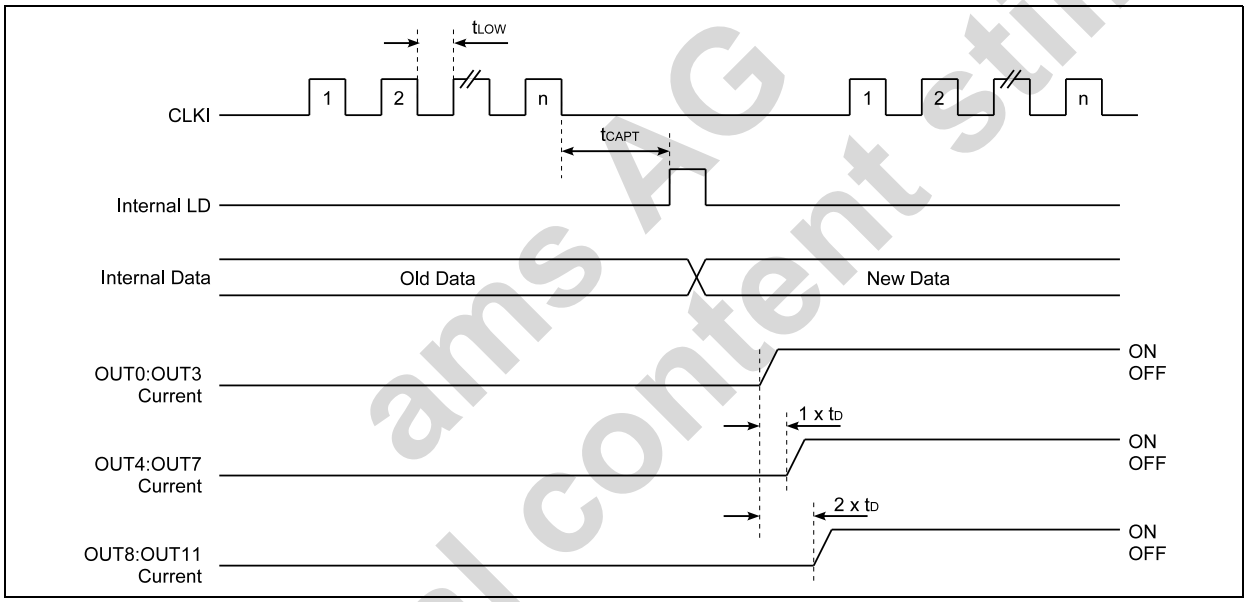
The rising edge of the CLKI signal shifts data from pin SDI to the internal register. After all data are clocked in, the serial data are latched into the internal registers at the rising edge of the internal LD signal (see Figure 24). The internal LD signal is triggered after the clk is low for a time t_{CAPT} and all Data are clocked in.

With the first 8 clk-cycles an 8 bit identifier needs to be send to the device to distinguish between Status Information, Dot Correction, PWM or command data.

After the internal LD signal the internal counter is set to 0 again and the data are latched into the register according to the prior identifier. If the LD triggers and the counter has no valid value (80 bit for Dot-Correction, 152 bit for PWM data or 16 bit for command data), the counter is set to 0 but the data will be ignored.

With the falling edge of the CLKO the data is shifted to SDO.

Figure 24. PWM Cycle Timing Diagram



Technical content still valid
ams AG

Register Access

Before data are accepted by the AS1122, an identifier needs to be send in advance. Only 3 defined identifiers will be recognized, all other bit combinations will be ignored.

Table 6. Identifier

Identifier	Bit								Data Section length	Description
	7	6	5	4	3	2	1	0		
Dot Correction Data	1	1	0	0	1 / 0	0	0	1	72 bits	writes Data into Dot Correction Register
PWM Data	1	1	0	0	1 / 0	0	1	0	144 bits	writes Data into PWM Register
Command Data	1	1	0	0	1 / 0	1	0	0	8 bits	writes Data into Command Register

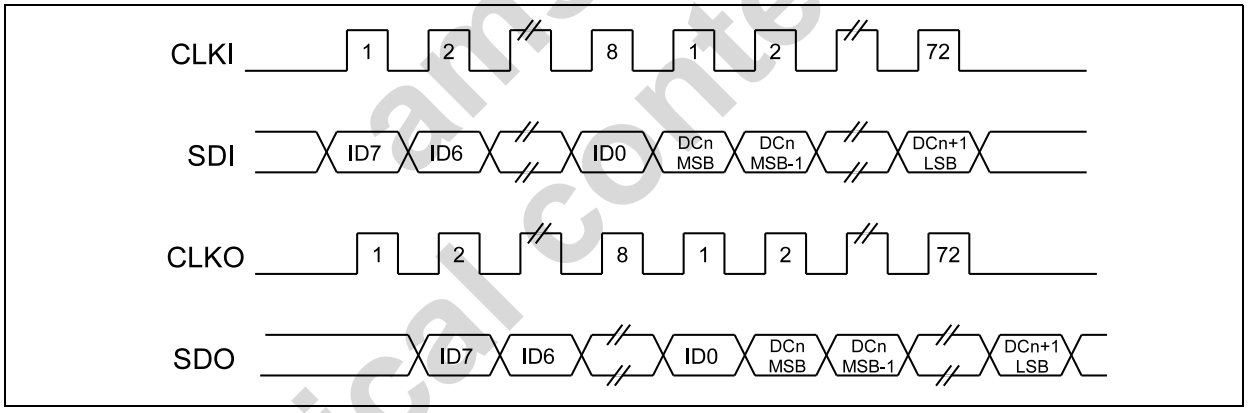
The identifier maps the input register to the identified register and all data on pin SDI will be clocked into this register. This selection is valid as long as no internal LD signal is triggered. When data is latched into the device the identifier selection is reset and for the next data word a new identifier needs to be send. Every identifier requires a certain data section length. If this length is not corresponding with the identifier, the data will be ignored.

Note: Bit3 of the identifier is an global on/off bit. When bit3 of any identifier is set to logic '0' and the OEN bit of the command register (see Figure 7 on page 14) is '0' (per default), the output channels are immediately turned on.

Dot Correction (DC)

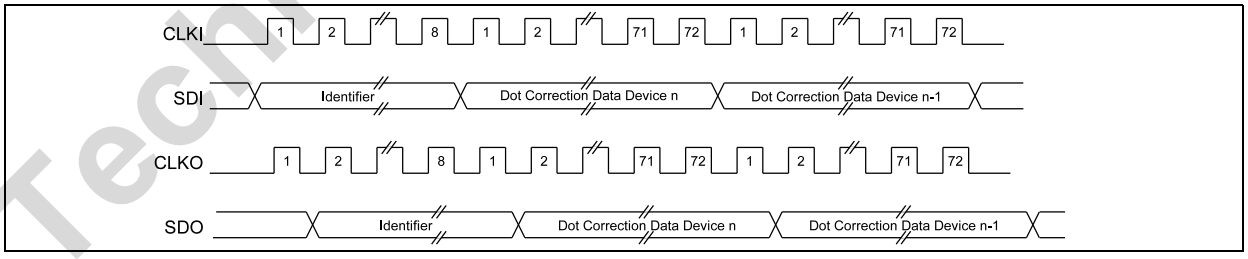
The AS1122 offers a 6 bit (64 steps) Dot Correction per Output channel. After sending the 8 bit identifier for access to the DC register the device is waiting for 72 bits to receive. If more or less bits are send the whole dataword will be ignored.

Figure 25. Dot Correction Input Timing Diagram



For n devices in a chain only one identifier needs to be send to set all n devices to the same register setting.

Figure 26. Dot Correction for n-devices

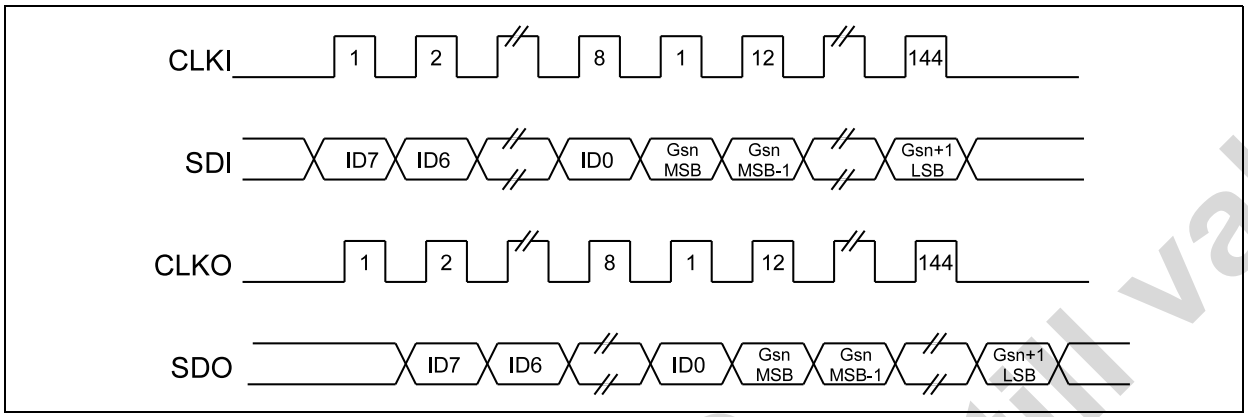


Technical content still valid
ams AG

PWM Data

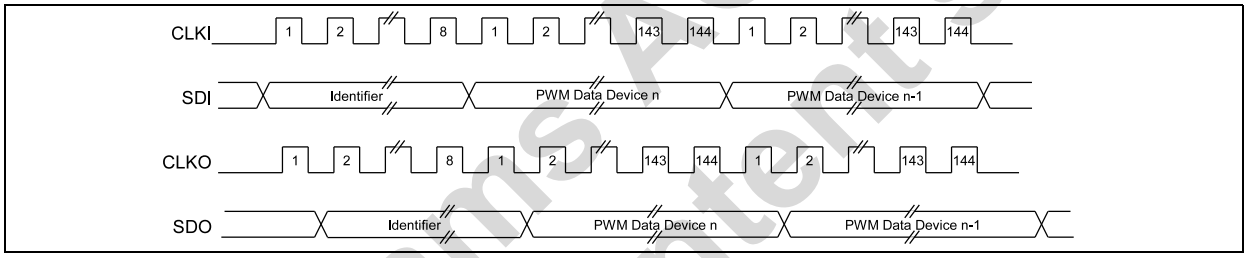
To set the PWM, 12 bit (4096 steps) per Output channel can be used. After sending the 8 bit identifier for access to the PWM Data register the device is waiting for 144 bits to receive. If more or less bits are send the whole dataword will be ignored.

Figure 27. PWM Input Timing Diagram



For n devices in a chain only one identifier needs to be send to set all n devices to the same register setting.

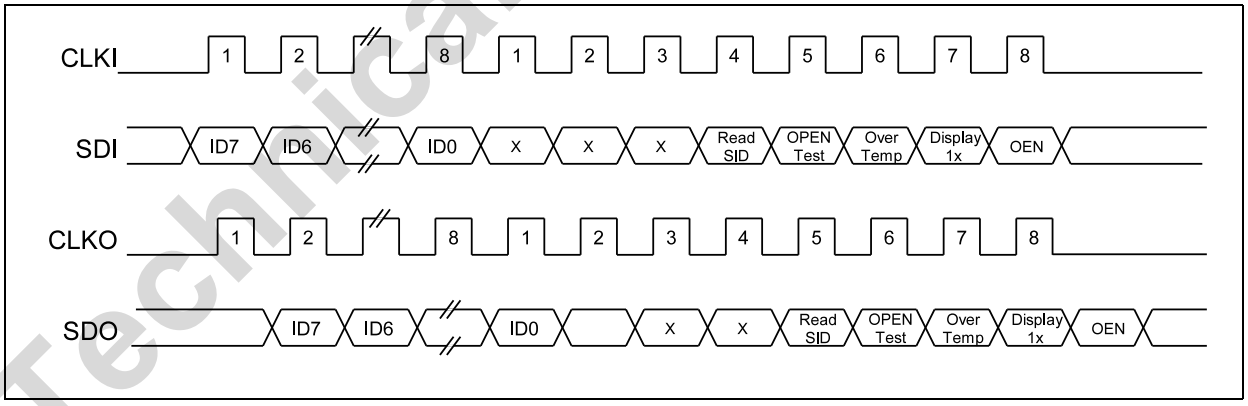
Figure 28. PWM Data for n-devices



Command Data

The AS1122 offers a command register for setting the configuration of the device. The command register is again accessible via an identifier and is 8 bits long. If more or less bits are send the whole dataword will be ignored.

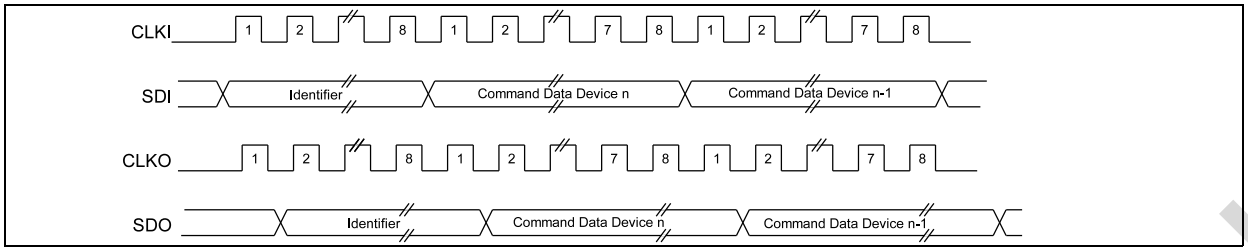
Figure 29. Command Input Timing Diagram



ams AG
Technical content still valid

For n devices in a chain only one identifier needs to be send to set all n devices to the same register setting.

Figure 30. Command Data for n-devices



Setting Dot Correction

The AS1122 can perform independent fine-adjustments to the output current of each channel. Dot correction is used to adjust brightness deviations of LEDs connected to the output channels (OUT0:OUT11).

The device powers up with the following default settings: DC = 0 and GS = 0.

The 12 channels can be individually programmed with a 6-bit word for Dot Correction. The channel output can be adjusted in 64 steps from 0 to 100% of the maximum output current (I_{MAX}). The output current for each OUT*n* channel can be calculated as:

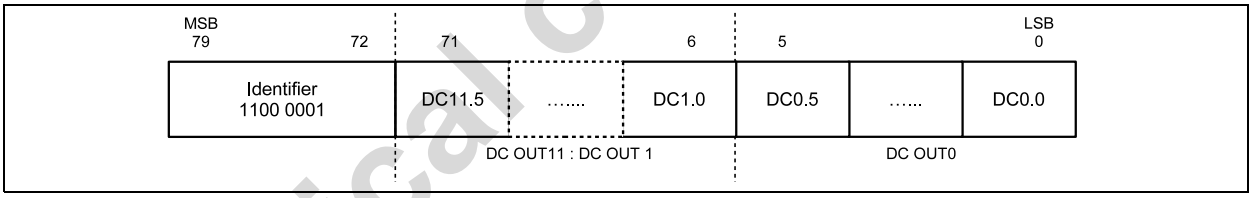
$$I_{OUTn} = I_{MAX} \times \frac{DCn}{63} \qquad \textit{(EQ 1)}$$

Where:

I_{MAX} is the maximum programmable output current for each output;
DC*n* is the programmed dot correction value for output (DC*n* = 0 to 63);
n = 0 to 11

Dot correction data are simultaneously entered for all channels. The complete dot correction data format consists of 12 x 6-bit words, which forms a 72-bit serial data packet (see Figure 31) and 8-bit for the identifier. Channel data is put on one by one, and the data is clocked in with the MSB first.

Figure 31. Dot Correction Data Packet Format



The Dot Correction data is only valid if the exact identifier byte was send. Otherwise the data will be ignored.

Setting Greyscale Brightness (PWM)

The brightness of each channel output can be adjusted using a 12 bits-per-channel PWM control scheme which results in 4096 brightness steps, from 0% to 100% brightness. The brightness level for each output is calculated as:

$$\%Brightness = \frac{GSn}{4095} \times 100 \qquad \textit{(EQ 2)}$$

Where:

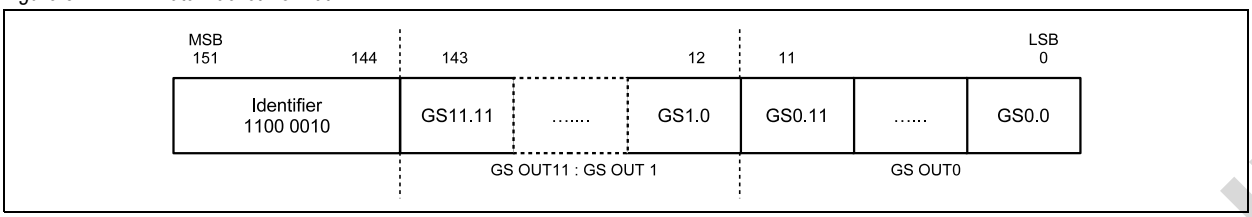
GS*n* is the programmed greyscale value for OUT*n* (GS*n* = 0 to 4095);
n = 0 to 11 greyscale data for all outputs.

The device powers up with the following default settings: GS = 0 and DC = 0.

ams AG
Technical content still valid

The input shift register shifts greyscale data into the greyscale register for all channels simultaneously. The complete greyscale data format consists of 12 x 12 bit words, which forms a 144-bit wide data packet (see Figure 32) plus the 8-bit for the identifier.

Figure 32. PWM Data Packet Format



The PWM data is only valid if the exact identifier byte was send. Otherwise the data will be ignored.

Command Data

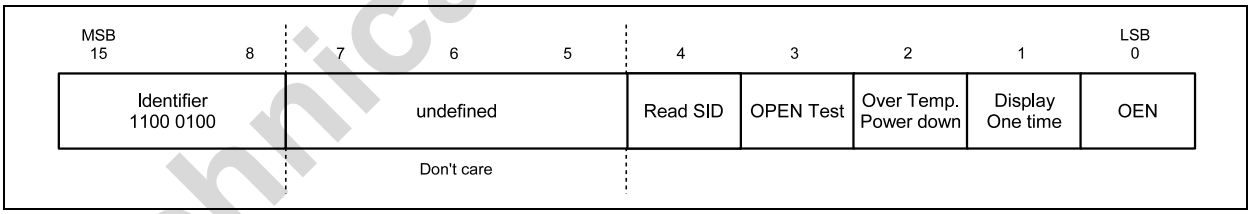
In the command register of the AS1122 some configuration of the device can be done. After sending the correct identifier the 8 bits of the command register are accessible.

Table 7. Command Register Format

Bit	Bit Name	Default	Access	Bit Description
7:5	-	000	n/a	
4	Read SID	0	W	0: normal operation 1: read Status Information Register (SID)
3	OPEN Test	0	W	0: no test is running 1: start OPEN test
2	Over Temperature Power down	0	W	0: If an overtemperature condition occurs the OUTn are NOT switched off automatically. 1: If an overtemperature condition occurs the OUTN are switched off automatically.
1	Display One Time	0	W	0: The PWM is running endless 1: The PWM is running for one cycle
0	OEN	0	W	0: This bit must be '0' as well as bit3 of the last valid identifier to turn ON all channels. 1: all channels are OFF

The complete status information data packet is shown in Figure 33.

Figure 33. Command Packet Format



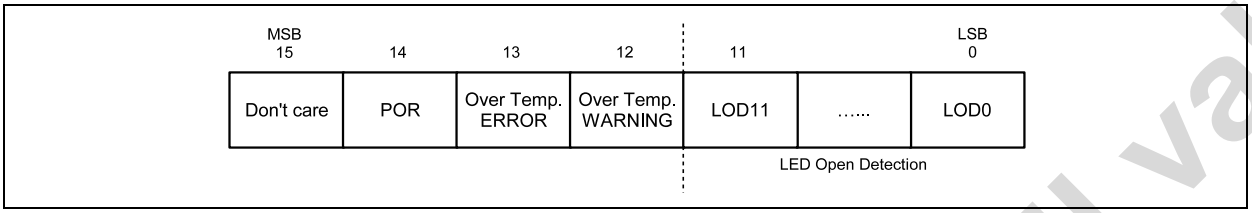
Technical content still valid
ams AG

Status Information Data (SID)

The AS1122 contains an integrated status information register. After latching the correct identifier with a 16 bit data word the input shift register data is replaced with status information data.

With the next 16 clock cycles the Open LED information, the Overtemperature-Warning and -Error flag as well as the power-on reset (POR) flag can be read out at pin SDO. The status information data packet is 16 bits wide. Bits 11:0 contain the open LED detection status of each channel. Bit 12 is the overtemperature-warning flag, bit 13 is the overtemperature-error flag and bit 14 indicates if the POR was triggered. The complete status information data packet is shown in Figure 34.

Figure 34. Status Information Data Packet Format

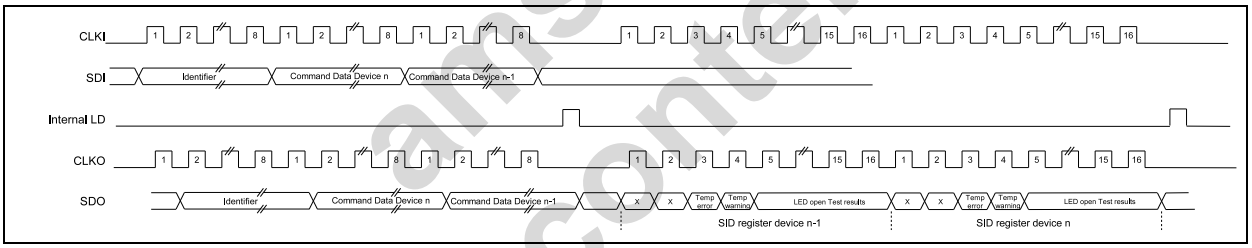


Note: Bit14 (POR) is set to '1' after start-up and after triggering a power-on reset due to a supply voltage drop. Must be set to '0' manually.

Readback the Status Information Data

To read out the SID the read bit in the command data needs to be set to "1". After the new command data is lachted into the device the SID is shifted to the SDO register and will be shifted out with the next running clk cycles on CLKI. After keeping the clk low for the time tlow, the device is reset again and can be programmed with need information.

Figure 35. Reading of the Status Information Register



Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor RIREF, which is placed between pin IREF and GND. The voltage on pin IREF is set by an internal band gap VIREF (1.27V typ). The maximum channel current is equivalent to the current flowing through RIREF multiplied by a factor of 31.5. The maximum output current is calculated as:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 31.5 \qquad \textit{(EQ 3)}$$

Where:

VIREF = 1.27V;
RIREF = User-selected external resistor.

ams AG
Technical content still valid

Timing for Cascading of n-devices

With the rising edge of CLKI the data will shifted from SDI into the device. The rising edge of CLKI is shifted through the devices to CLKO. After a factory fixed high-time (100ns) the falling edge of CLKO is triggered and the data are shifted out via SDO. This ensures a synchronous timing between CLKO and SDO. The CLK period (frequency) will stay the same only the duty cycle will be changed.

The fixed high-time will vary with +/- 30%.

Figure 36. Clock Handling with 5MHz Data-Clock

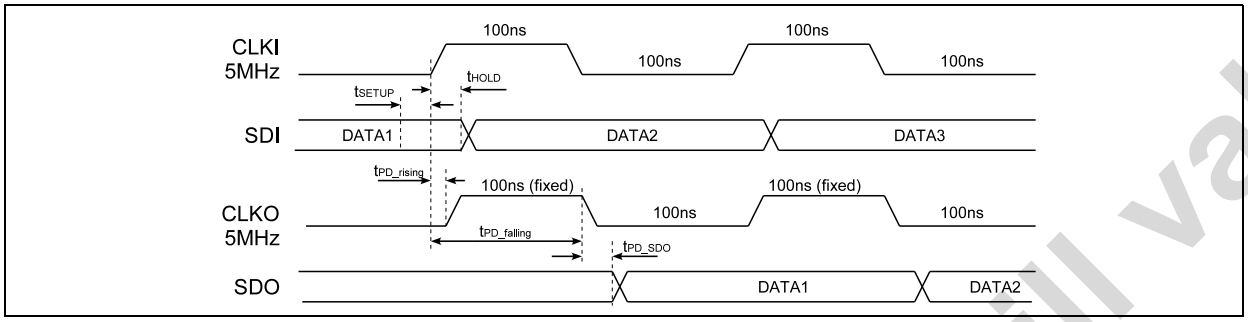
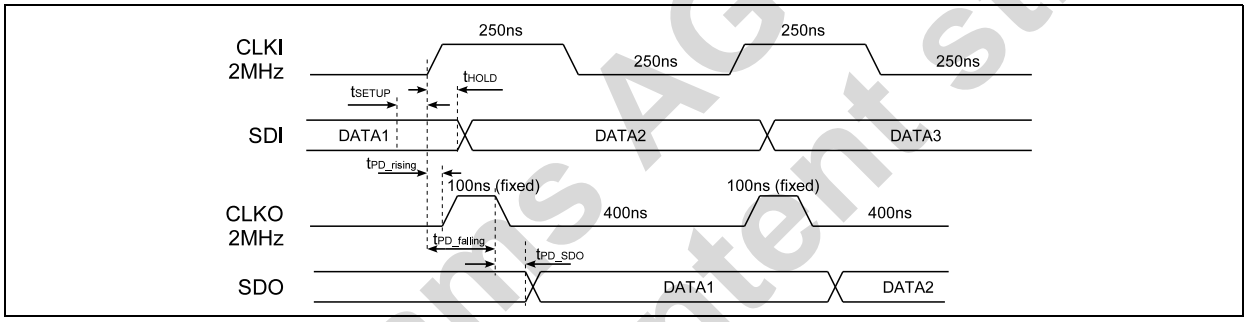


Figure 37. Clock Handling with 2MHz Data-Clock



ams AG
Technical content still valid

Scrambled PWM

General

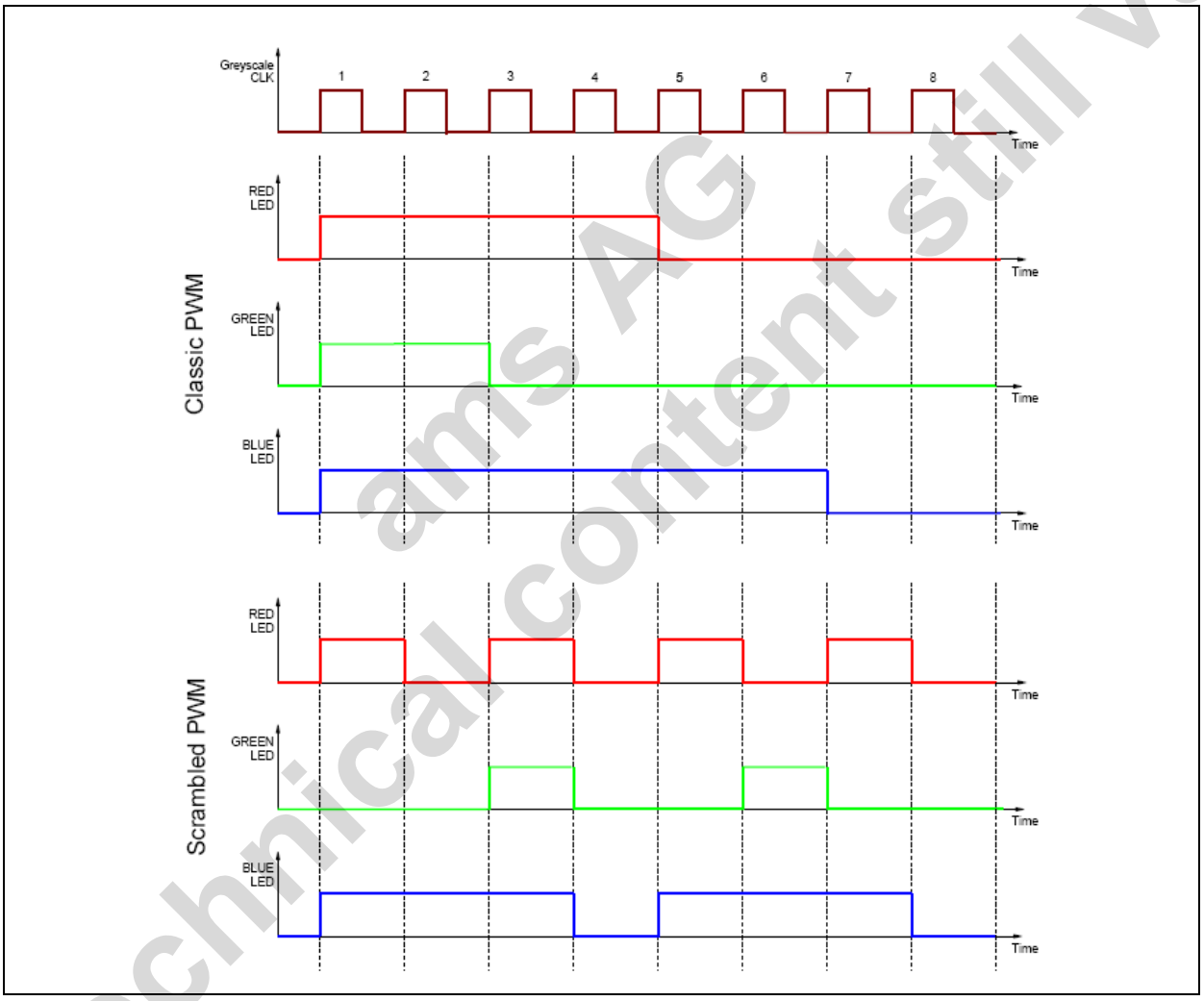
Due to the possibility to interrupt a running PWM cycle the AS1122 is useing a scrambled PWM. The advantage is, that the scrambled PWM will cause less error as the classical PWM when data is updated during a running PWM cycle.

As an example, we take a look on a system with a 8-bit PWM and three LEDs. The PWM for the red LED is set to 4, for green to 2 and for blue to 6. In the classical approach the red, green and blue channels are high according to their PWM setting (see Figure 38).

If this PWM cycle would be interrupted at the 4th clock, the red and the blue LED would be as bright as if the PWM setting were 8. The green LED also would be much brighter than desired.

In the scrambled PWM the on-times are divided evenly over the whole PWM cycle. So if the running PWM cycle is interrupted, the failure is less effective.

Figure 38. Classic PWM vs. scrambled PWM



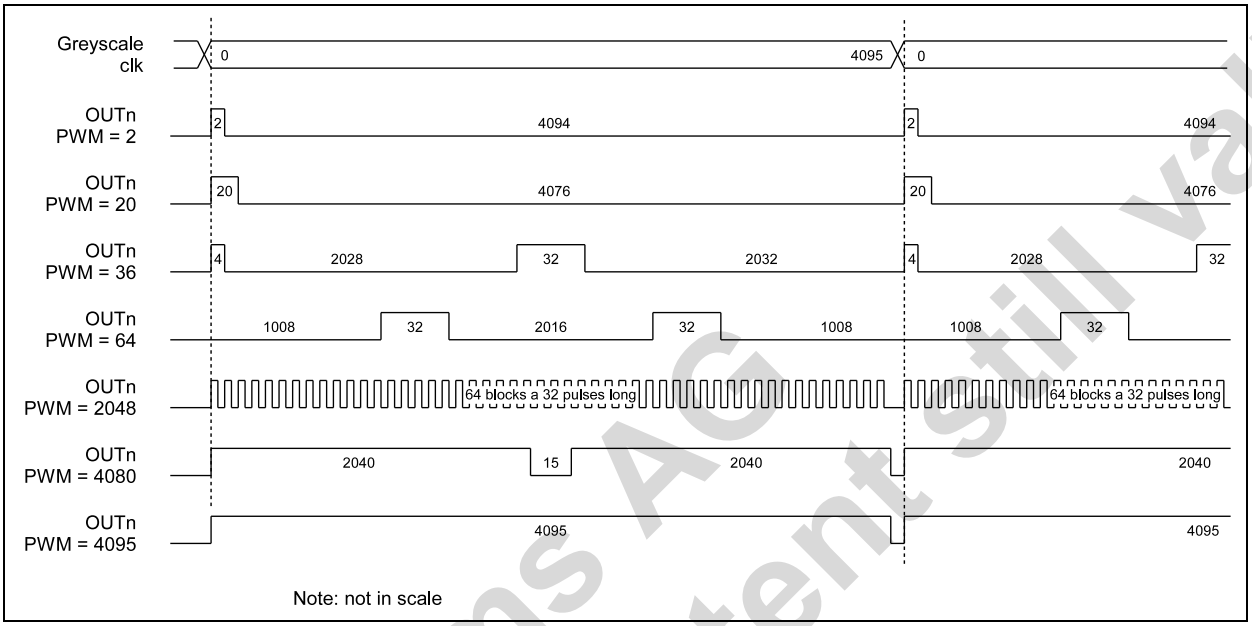
Technical content still valid
ams AG

PWM scheme of AS1122

The AS1122 uses a scrambled PWM scheme. Meaning the PWM value is divide into sup-periods (32 bits wide) and than evenly distributed over the whole PWM cycle. If the PWM setting can not be divided by 32, the rest is added at the beginning of the PWM cycle.

Figure 39 shows some examples how different PWM settings are distributed over one PWM cycle.

Figure 39. Different PWM Outputs of AS1122



The PWM clock is generated internally and is running with fOSZ (10MHz typ.). For a PWM value of 20 the OUT channel is high for 20 PWM-clock pulses (20 x 100ns) and stays then low for 4076 PWM-clock pulses (4076 x 100ns). After one PWM cycle (4096 pulses) the cycle is repeated endless until the output channels is turned off or updated with new PWM data.

Technical content still valid
ams AG

9 Package Drawings and Markings

Figure 40. 24-pin QFN 4x4mm Marking

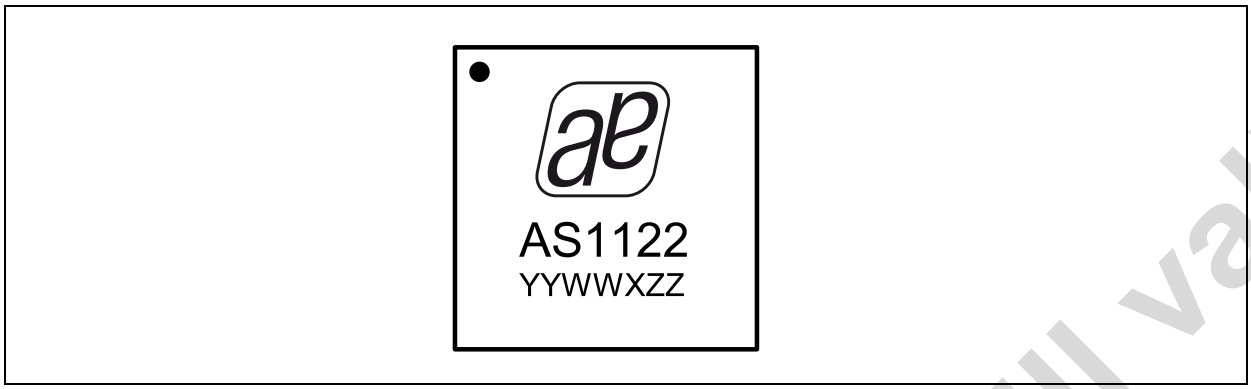
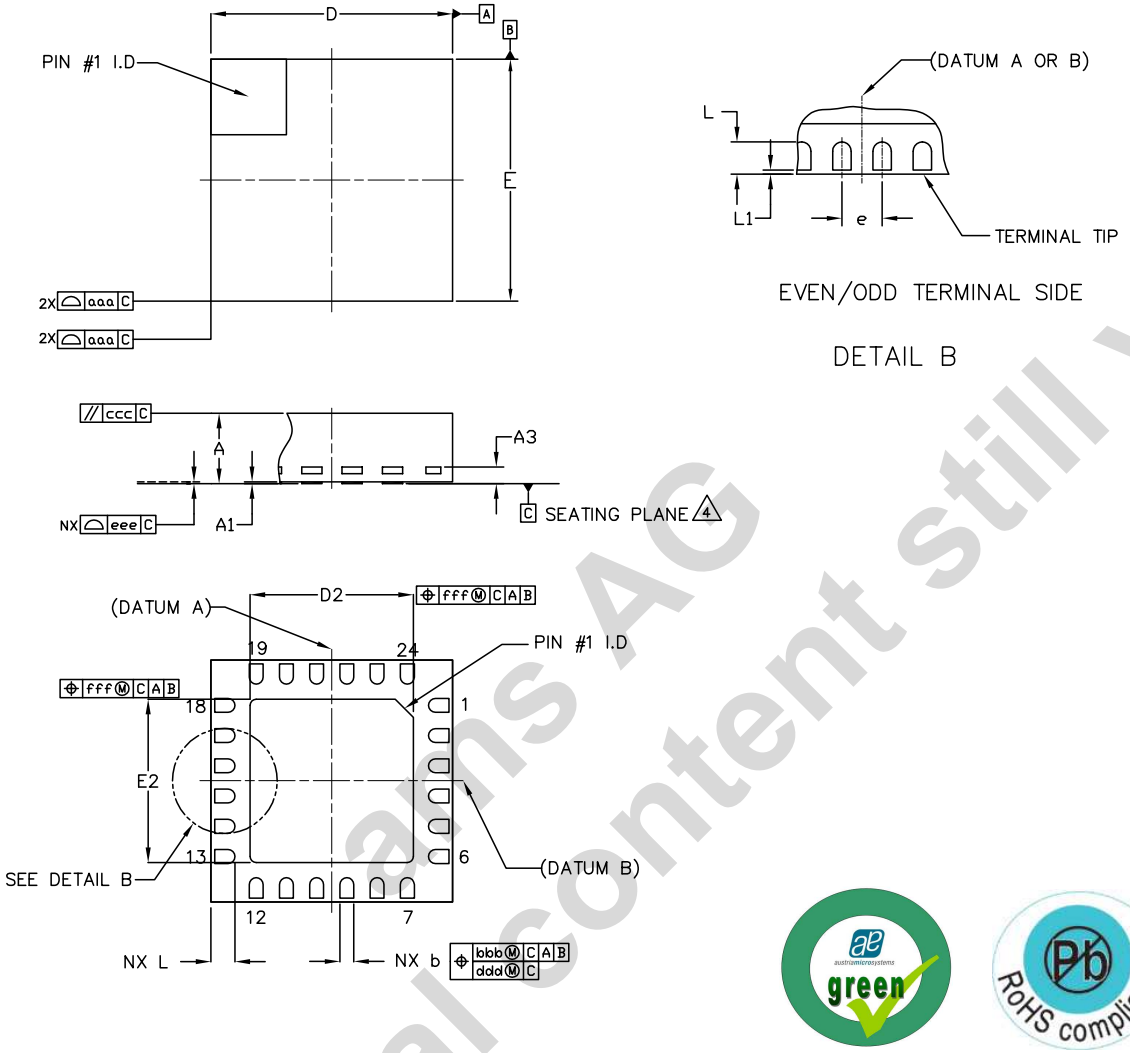


Table 8. Packaging Code YYWWXZZ

YY	WW	X	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

ams AG
Technical content still valid

Figure 41. 24-pin QFN 4x4mm Package



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	–	0.20 REF	–
L	0.35	0.40	0.45
L1	0	–	0.15
b	0.18	0.23	0.28
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		24	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

austriamicrosystems a leap ahead in analog			ASSEMBLY ENGINEERING	
DRAWN RH8	DATE 2010.10.29	REV. N/C	TITLE SAWN QFN, PULL BACK, 4x4x0.9mm 24 LEAD, 2.70mm SQ. ePAD	REFERENCE DOCUMENT JEDEC MO – 220 LATEST REVISION
CHECKED GBO	DATE 2010.10.29		DRAWING NO. QYK	UNIT
APPROVED MKR	DATE 2010.10.29	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

Technical content still valid
ams AG

10 Ordering Information

The device is available as the standard products shown in Table 9.

Table 9. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1122-BQFT	AS1122	12-Channel LED Driver with Dot Correction and Greyscale PWM	Tape and Reel	24-pin QFN 4x4mm
AS1122B-BQFT*	AS1122B	12-Channel LED Driver with Dot Correction and Greyscale PWM without Output Delay	Tape and Reel	24-pin QFN 4x4mm

*) on request

Note: All products are RoHS compliant and austriamicrosystems green.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is found at http://www.austriamicrosystems.com/Technical-Support

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

ams AG
Technical content still valid

Copyrights

Copyright © 1997-2012, austriamicrosystems AG, Tobelbaderstrasse 30, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

ams AG
Technical content still valid

austriamicrosystems

Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact